A VLSI Floorplanner

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Latest version: PARQUET-4.5

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Parquet is free open-source software for floorplanning based on Simulated Annealing, that has been used in a number of projects in Computer-Aided Design and Computer Architecture. While originally designed for fixed-outline floorplanning, it can also be applied to classical min-area block packing. The internal floorplan representation alternates between sequence pairs and B*-Trees. Parquet reads and writes a simple blocks/pl/nets format that most users learn by example. Floorplans can be visualized using gnuplot. For fixed-outline floorplanning with more than 50-100 blocks, consider using Capo 10 which now includes Parquet. For area-optimal packing use BloBB (hard blocks) or CompaSS (soft blocks). For floorplan legalization, use FLOORIST.

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Downloads

If you are using this software in a publication or a technical report, please cite one of publications [1-3] below in addition to the URL, since they describe the algorithms used by Parquet. The performance of Parquet with different floorplan representations (sequence pairs and B*-trees) was compared in a common Simulated Annealing framework in [4].

Latest source code and binaries will be provided upon request (except for certain geographic regions) --- send email to *Igor Markov* and *Jarrod Roy* at **capo.request@gmail.com** since Parquet has been integrated into Capo. If you are requesting binaries, please indicate your platform (Linux32, Linux64, Solaris32, Solaris64, or Windows32). We would appreciate (but do not require) any additional information, for example:

- Your name and affiliation
- Possible uses of Parquet and/or reason for interest
- Computing platform (OS, compiler version, etc)

Questions and comments on your experience with Parquet are always welcome. If you found a bug and describe it to us, we may be able to fix it.

Common Command-line Options

-f filename
-s int (give a fixed seed)
-n int (determine number of runs; default is 1)
-t double (set a time limit on the annealing run)
-savePl baseFilename (save .pl file of solution)
-plot (plot the output solution to out.gpl file)
-AR double (desired Aspect Ratio of fixed outline;
default: no Fixed Outline)
-maxWS double (maxWS(%) - in fixed-outline mode only)
-outline xMin,yMin,xMax,yMax (desired bounding box
instead of AR and maxWS)
-minWL (minimize WL default turned off)
-soft (soft Blocks present in input default no)
-solveMulti (solve as multiLevel heirarchy)
-maxWSHier double (maxWS(%) for each hierarchical block)
-FPrep "BTree/SeqPair/Best" (floorplan data structure;
default is Best)

A full list of command-line options is available here

Earlier Releases of Parquet

The main difference between Parquet-2 and Parquet-3 is that Parquet-3 has an alternative floorplan representation (B*-Trees). Parquet-3 has support for net-weights and enhanced support for soft blocks. Also, Parquet-3 has a higher probability of satisfying fixed-outline constraints. Each simulated annealing move in Parquet-3.1 is faster than 3.0, which reduces overall runtimes and allowed us to extend the temperature schedule so as to improve solution quality. In addition, the connectivity-based clustering algorithm used for multi-level floorplanning is enhanced in 3.1. Parquet-4.0 is somewhat faster than previous versions and has cleaner source code. Parquet-4.5 continues the speed and code improvements and also implements terminal pin scaling for free-outline floorplanning instances. Parquet-4.5 also introduces the "Best" floorplanning representation which chooses between "SeqPair" and "BTree" depending upon the input instance and optimization objectives. It has been found empirically that B*-Trees are better at packing than Sequence Pairs, so if wirelength is not being optimized or available whitespace is lower than 10%, "Best" chooses the B*-Tree representation. We have also found empirically that B*-Trees are faster than Sequence Pairs on instances with 100 or more blocks, so "Best" chooses B*-Tree over Sequence Pair in these cases as well.

Old Releases Old Binaries

Floorplanning Benchmarks

MCNC Benchmarks
GSRC Benchmarks

Publications

1. S. N. Adya and I. L. Markov, "Fixed-outline Floorplanning : Enabling Hierarchical Design" (.pdf), *IEEE Trans. on VLSI Systems*, vol 11(6), December 2003, pp. 1120-1135.
2. S. N. Adya and I. L. Markov, "Fixed-outline Floorplanning Through Better Local Search" (.pdf) *Int'l Conf. On Computer Design (ICCD 2001)*, pp. 328-333.
3. S. N. Adya and I. L. Markov, "Consistent Placement of Macro-Blocks using Floorplanning and Standard-Cell Placement", (.pdf), *Int'l Symposium on Physical Design (ISPD)*, pp. 12-17, San Diego, 2002.
4. S. N. Adya, S. Chaturvedi, J. A. Roy, D. A. Papa and I. L. Markov, "Unification of Partitioning, Floorplanning and Placement" (.pdf), *Intl. Conf. Computer-Aided Design (ICCAD 2004)*, pp. 550-557.
5. H. H. Chan, S. N. Adya and I. L. Markov, "Are Floorplan Representations Useful in Digital Design?" (.pdf), *Intl. Symposium on Physical Design (ISPD 2005)*, pp. 129-136.
6. A. N. Ng, I. L. Markov, R. Aggarwal and V. Ramachandran, "Solving Hard Instances of Floorplacement", (.pdf), *Int'l Symp. on Physical Design (ISPD 2006)*, pp. 170-177.
7. J. A. Roy, S. N. Adya, D. A. Papa and I. L. Markov, "Min-cut Floorplacement", (.pdf) *IEEE Trans. on Computer-Aided Design*, July 2006.

Citations

Publications citing Parquet related papers are available here (click on citation counts).