University of California Santa Cruz
Department of Computer Engineering
Lab Experiment Report # 1
Waveforms and the Basys 3 Board

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Due Date: 12/07/18

Objective
The purpose of this lab was to get familiar with using the oscilloscope and getting comfortable with adjusting the view settings to understand electric waveforms. The lab also was the first introduction in using the Basys 3 FPGA board and it's sister program vivado.

Part One: Using the Oscilloscope:

DISPLAYING A WAVE FORM: Following the Lab 1 outline, a bit file was downloaded from a provided link and was uploaded to the basys 3 board through the hardware manager on Vivado. Connecting wires and pins to the oscilloscope wands I connected the two hooks for the oscilloscope to pins JA-1 and JA-3 on the left side of the board. I connected the two ground wands to the ground pin JA-G also on the left side of the board.

RESULTS:

The wave form in input JA-3 and JA-1 will be referred to as input 3 and 1 respectively. Input 3 display a step function with a period of 10.24 microseconds and a voltage peak of 3.6V. It's step up and step down voltage were exactly half of the period ergo they both had a length of 5.12 microseconds.
(SEE APPENDIX FOR VISUAL)

Input 1's step function did not have the same symmetry as input 3. It's peak voltage was 36V and had a full period of 163.8 microseconds, but it's step up only lasted 10.24 microseconds, while the remaining period was at 0V. In between two step up parts of the wave form, there were also two anomalous spikes of 10V at 60 and 120 microseconds.
(SEE APPENDIX FOR VISUAL)

Part Two: Entering a Simple Schematic:

Creating our first schematic using Vivado with the programming language Verilog required a familiarity with the program Vivado. Upon following the provided instructions in the lab to create a new project, I found my bearings and created my first source using verilog to build a schematic. The design parameters requested from the lab were as follows:

- the AND of switch SW0 and SW1 should be the output to LED LD1.
- the OR of switch SW0 and SW1 should be the output to LED LD2.
- the XOR of switches SW0, SW1 and SW2 should be the output to LED LD3.
- the NOT of pushbutton BTNC should be output to LED LD0,

Using the knowledge from part 1 to upload the schematic to the FPGA board using the hardware manager on Vivado and my new knowledge on programming logic networks in Verilog I created the designs to follow these specifications using simple boolean logic.

RESULTS:

The logic networks needed to satisfy the parameters consisted of very basic boolean algebra, and only really required learning the syntax of Verilog. In the language AND’s = $, OR’s = |, XOR’s = ^, and NOT’s = ~. The inputs and outputs that use a port on the board need to be declared as such in the module parentheticals and we are using the command ASSIGN as treatment for relating outputs to inputs. After the module is created, the BIT file needs to be generated and the file is uploaded to the board. The exact syntax is provided in the appendix for the module as well as the schematic generated by Vivado.

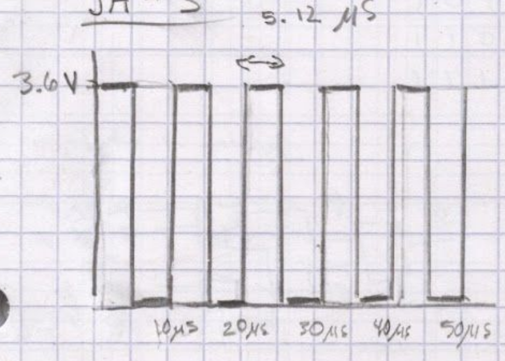
APPENDIX

LAB 1 CE 100

- Configuring Basys 3 board

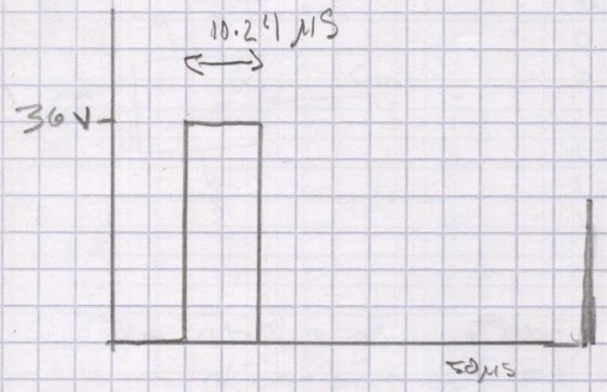
Downloading the provided bit file & using Vivado, I configured the Board to use the bit schematic. Once configured, I measured the outputs of ports JA-1 & JA-3 as shown below:

JA-3



Period: 10.24 μS
V_{pp} : 3.6V

JA-1



Period: 163.8 μS
V_{pp} : 36V

two 10V spikes in between periods

Zane Bradley
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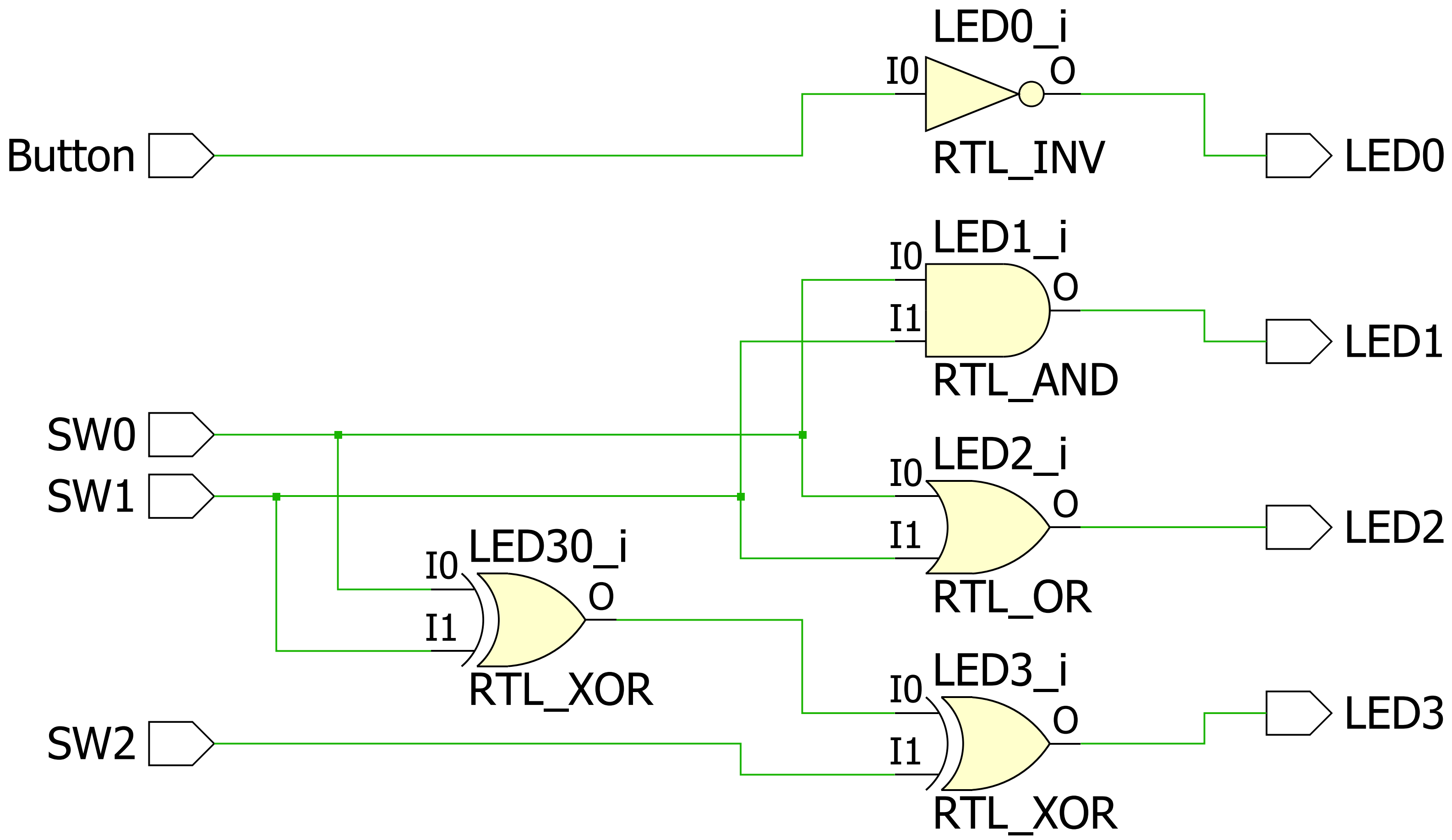
4340

Voltage Gain = 10 = $\frac{V_{out}}{V_{in}}$


LED0_i
I0
O
RTL_INV
Button
LED0
LED1_i
I0
I1
O
RTL_AND
LED1
SW0
SW1
LED2_i
I0
I1
O
RTL_OR
LED2
LED30_i
I0
I1
O
RTL_XOR
LED3_i
I0
I1
O
RTL_XOR
SW2
LED3

```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 01/08/2019 11:12:18 AM
// Design Name:
// Module Name: myAND
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module myAND(
    input Button,
    input SW0,
    input SW1,
    input SW2,

    output LED0,
    output LED1,
    output LED2,
    output LED3
);
    assign LED0 = ~Button;  // ld0 = not btnc
    assign LED1 = SW0 & SW1;  // ld1 = sw0 and sw1
    assign LED2 = SW0 | SW1;  // ld2 = sw0 or sw1
    assign LED3 = SW0 ^ SW1 ^ SW2;  // ld3 = XOR sw0, sw1, sw2
endmodule
```