University of California Santa Cruz
Department of Computer Engineering
Lab Experiment Report # 8
Breadboard Construction

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Objective

This lab uses a breadboard to implement an inverter circuit, and a d flip flop. The lab was the first introduction into actually building some of the logic networks programmed on Vivado. Building circuits by hand can be a very different experience than programming them. Using an Oscilloscope, the voltages were measured.

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Part 1: Measuring Propagation Delay

Using 9 inverters in series to create a ring oscillator, propagation delay was measured across one inverter.

Method:

Using two of the SN74LS04 chips, I created a circuit using the schematic included below. Creating the circuit required also plugging in a DC power source to a connector to the board. This was the voltage driver. A fuse was placed in between the positive voltage end of the power connector to prevent driving any current that might damage the IC chips.

Results:

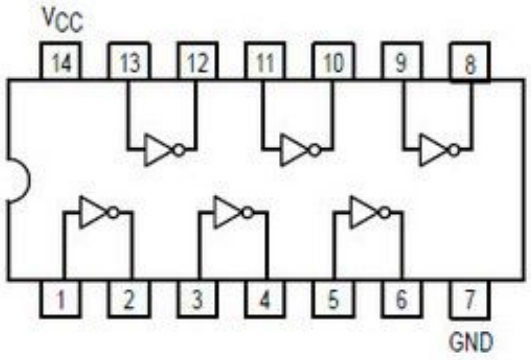
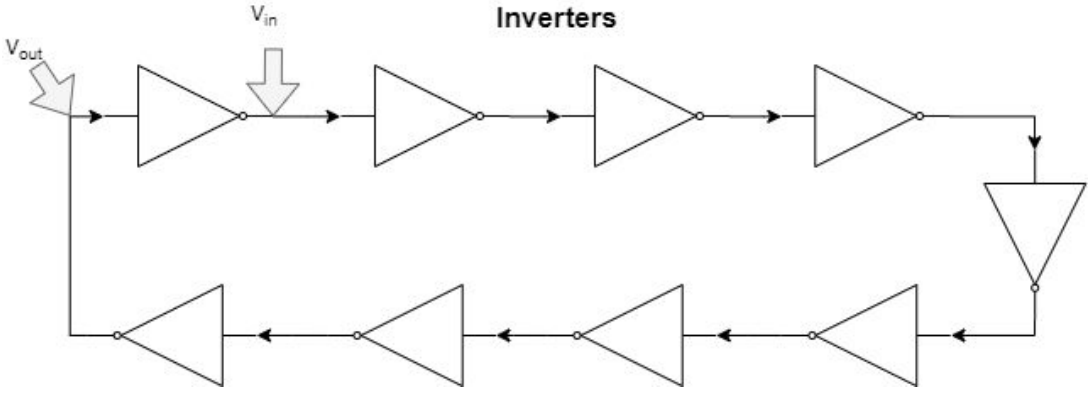


Image taken from TI SN74LS04 production manual



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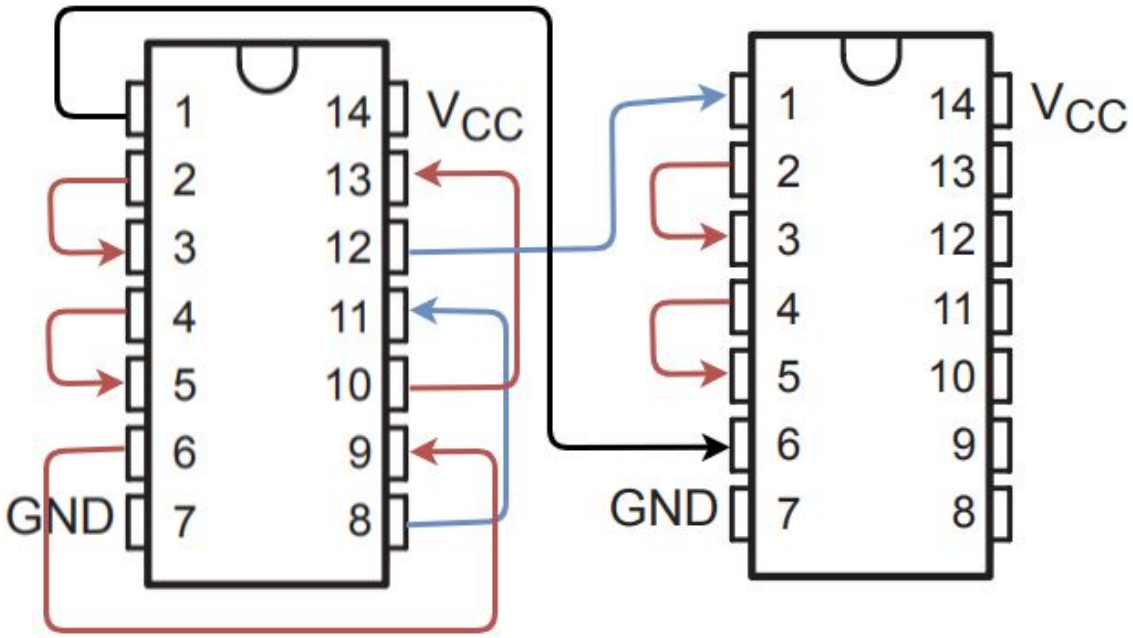

Q: What was the average propagation delay of an inverter in the IC?

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S04 SN74S04			UNIT
				MIN	TYP	MAX	
t_{PLH}	A	Y	R_L = 280 Ω, C_L = 15 pF		3	4.5	ns
t_{PHL}					3	5	
t_{PLH}	A	Y	R_L = 280 Ω, C_L = 50 pF		4.5		ns
t_{PHL}					5		

A: The total measured propagation delay was 85.6nS when measured going from a high voltage to a high voltage again. Because of irregularities in the high voltage levels, this was an easier way of measuring the delay, so the value was divided by 18 instead of 9 because the ring oscillator had to go around twice to get back to high voltage when starting at a high voltage. Therefore, calculated inverter propagation delay = 4.75nS. This is very comparable to the operating manual delay measurements above with a max of 5 nS.

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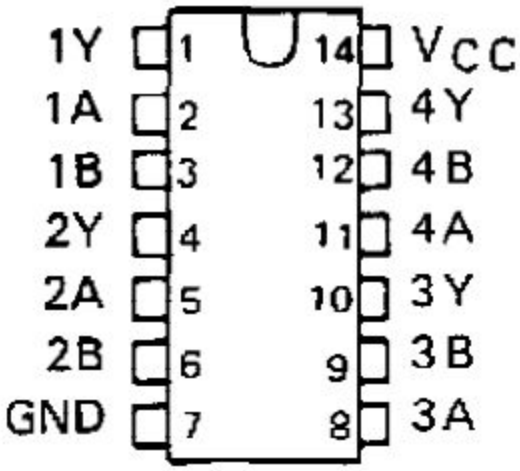
Part 2: Edge Triggered Flip Flop

Using just NOR's, an edge triggered D Flip Flop was made. The NOR implementation of the device made it a falling edge triggered flip flop, meaning the clock had to go from high to low to input the data signal.

Method:

Using two of the SN54AC02-SP IC chips, I implemented the schematic below. Two input a low or high voltage, the inputs had to either be connected to ground or a 5V input, both coming from the DC input.

Results:



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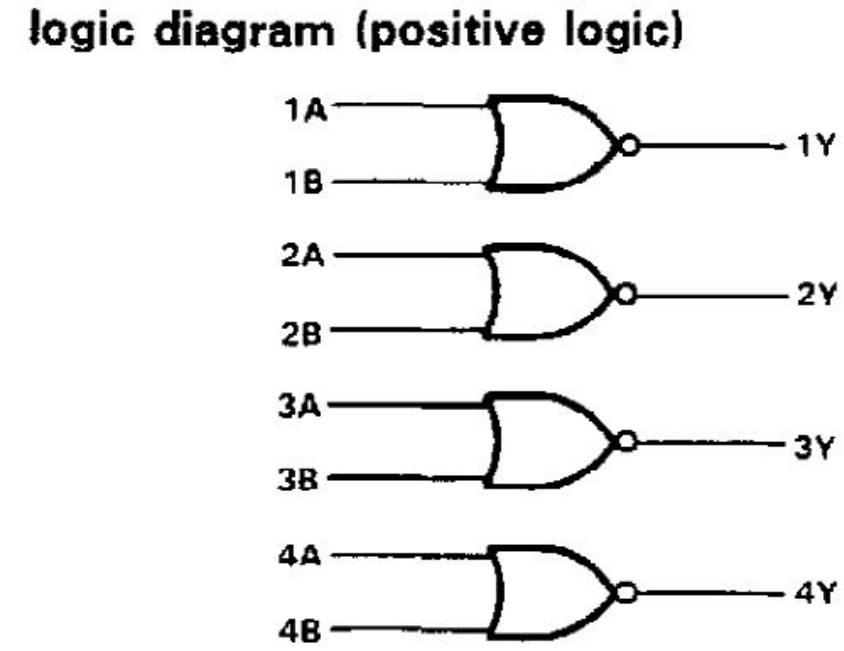

Both images above taken from SN54AC02-SP manual

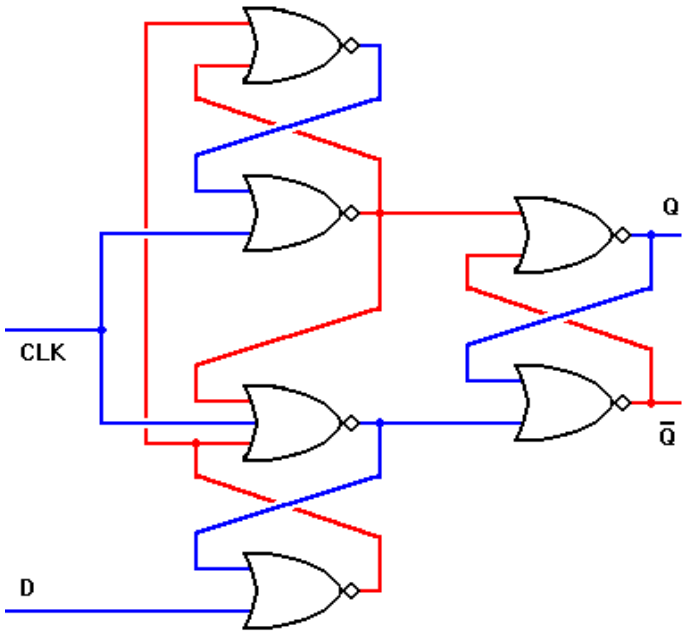

Image taken from ***http://www.play-hookey.com/digital/alt_flip_flops/d_nor_flip-flop.html***

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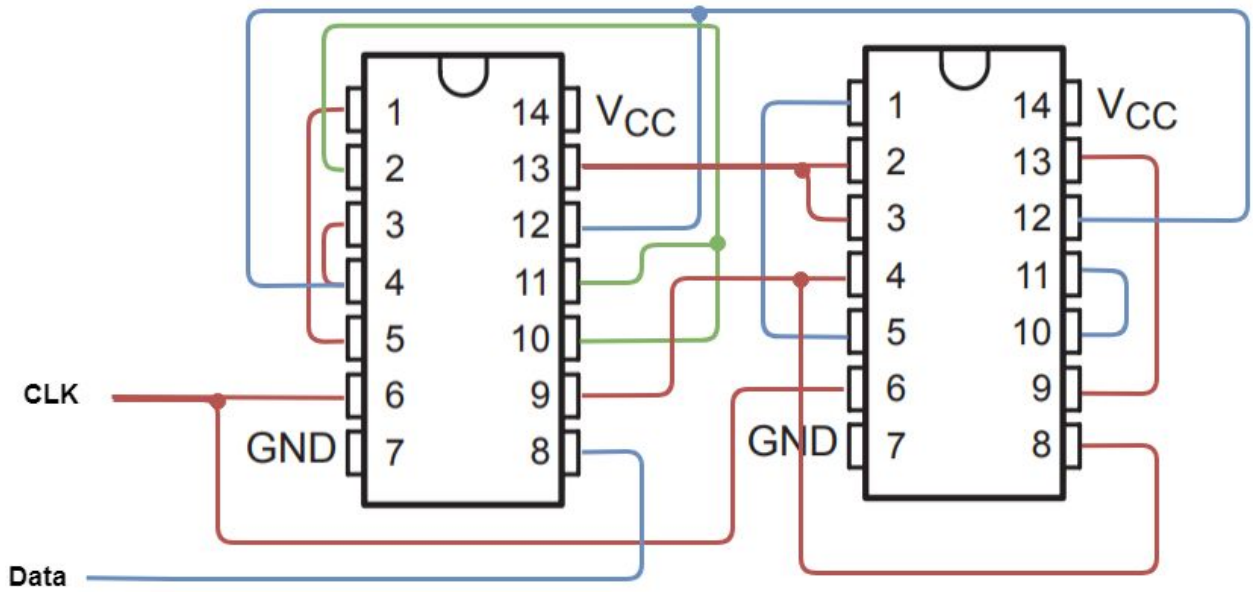
D Flip Flop



Pin 13 was Q and pin 10 was ~Q.

Q: What value of resistors were used?
A: The resistors provided in the lab were a 1K, 2K, and 500 Ohm resistor. Using The voltage law V = IR, current going through each of these resistors was 5mA, 2.5mA and 10mA respectively. The LED's had a max current intake of 20mA, so these signals did not violate this.