



Inspiring Excellence

# LAB ASSIGNMENT 3

CSE460: VLSI Design

Submitted By

**ARMAN HOSSAIN**

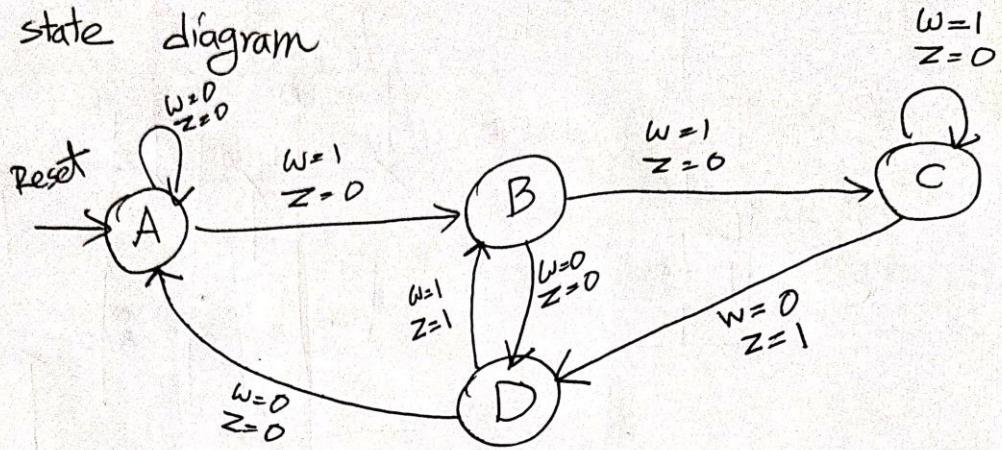
**18101707**

**Section: 03**

Problem 1

#18101707

state diagram



state table:

present state	Next state		output z	
	W=0	W=1	W=0	W=1
A	A	B	0	0
B	D	C	0	0
C	D	C	1	0
D	A	B	0	1

let's take

$$\begin{aligned} A &= 00 \\ B &= 01 \\ C &= 10 \\ D &= 11 \end{aligned}$$

state Assigned table:

present state	next state		output z	
	W=0	W=1	W=0	W=1
(A) 00	00	01	0	0
(B) 01	11	10	0	0
(C) 10	11	10	1	0
(D) 11	00	01	0	1

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 3/problem1\_18101707/problem1\_18101707 - [problem1\_18101707]

File Edit View Project Assignments Processing Tools Window Help

Tasks Row: Compilation

Task: problem1\_18101707.v

```

1 module problem1_18101707 (Clock, Resetn, w, z);
2
3   input Clock, Resetn, w;
4   output reg z;
5   reg [2:1]Y, Y;
6   parameter A = 2'b00, B = 2'b01, C=2'b10, D = 2'b11;
7
8
9   always @ (w, y)
10
11   case (y)
12     A: if (w)
13       begin
14         z = 0;
15         Y = B;
16       end
17     else
18       begin
19         z = 0;
20         Y = A;
21       end
22
23     B: if (w)
24       begin
25         z = 0;
26         Y = C;
27       end
28     else
29       begin
30         z = 0;
31         Y = D;
32       end
33
34     C: if (w)
35       begin
36         z = 0;
37         Y = C;
38       end
39     else
40       begin
41         z = 1;
42         Y = D;
43       end
44
45     D: if (w)
46       begin
47         z = 1;
48         Y = B;
49       end
50     else
51       begin
52         z = 0;
53         Y = A;
54       end
55
56   endcase
57
58   always @ (negedge Resetn, posedge Clock)
59     if (Resetn == 0) y <= A;
60     else y <= Y;
61
62 endmodule

```

Simulation Report - Simulation Waveforms

Messages

Type Message

- Info: Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 3/problem1\_18101707/problem1\_18101707.vwf"
- Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
- Info: Simulation partitioned into 1 sub-simulations
- Info: Simulation coverage is 89.47 %
- Info: Number of transitions in simulation is 1093
- Info: Quartus II Simulation was successful. 0 errors, 0 warnings

System (10) Processing (9) Extra Info (9) Info (9) Warning (1) Critical Warning (1) Error (1) Suppressed (1) Flag /

Message: 0 of 16

For Help, press F1

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 3/problem1\_18101707/problem1\_18101707 - [problem1\_18101707]

File Edit View Project Assignments Processing Tools Window Help

Tasks Row: Compilation

Task: problem1\_18101707.v

```

19 begin
20   z = 0;
21   Y = A;
22 end
23
24 B: if (w)
25   begin
26     z = 0;
27     Y = C;
28   end
29 else
30   begin
31     z = 0;
32     Y = D;
33   end
34
35 C: if (w)
36   begin
37     z = 0;
38     Y = C;
39   end
40 else
41   begin
42     z = 1;
43     Y = D;
44   end
45
46 D: if (w)
47   begin
48     z = 1;
49     Y = B;
50   end
51 else
52   begin
53     z = 0;
54     Y = A;
55   end
56
57 endcase
58
59 always @ (negedge Resetn, posedge Clock)
60   if (Resetn == 0) y <= A;
61   else y <= Y;
62
63 endmodule

```

Compilation Report - Flow Summary

Messages

Type Message

- Info: Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 3/problem1\_18101707/problem1\_18101707.vwf"
- Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
- Info: Simulation partitioned into 1 sub-simulations
- Info: Simulation coverage is 89.47 %
- Info: Number of transitions in simulation is 1093
- Info: Quartus II Simulation was successful. 0 errors, 0 warnings

System (12) Processing (51) Extra Info (47) Info (47) Warning (4) Critical Warning (1) Error (1) Suppressed (1) Flag /

Message: 0 of 150

For Help, press F1

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 3/problem1\_18101707/problem1\_18101707 - [Compilation Report - Flow Summary]

File Edit View Project Assignments Processing Tools Window Help

Tasks: problem1\_18101707

Flow: Compilation

Task List:

- Compile Design
- Analysis & Synthesis
- Filter (Place & Route)
- Assembler (Generate program)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Program)

Compilation Report

Flow Summary

Simulation Report - Simulation Waveforms

Compilation Report - Flow Summary

Row Status: Successful - Sun May 02 21:59:24 2021

Quartus II Version: 8.1 Build 163 10/28/2008 SJ Web Edition

Revision Name: problem1\_18101707

Top-level Entity Name: problem1\_18101707

Family: FLEX10KE

Met timing requirements: Yes

Total logic elements: 5 / 1,728 (< 1 %)

Total pins: 4 / 102 (4 %)

Total memory bits: 0 / 24,576 (0 %)

Total PLLs: 0

Device: EPF10K30ETC144-1

Timing Models: Final

Messages:

Type Message

System(12) Processing(51) Extra Info(47) Info(4) Critical Warning Error Suppressed(1) Flag /

Message: 0 of 150

For Help, press F1

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 3/problem1\_18101707/problem1\_18101707 - [Simulation Report - Simulation Waveforms]

File Edit View Project Assignments Processing Tools Window Help

Tasks: problem1\_18101707

Flow: Compilation

Task List:

- Compile Design
- Analysis & Synthesis
- Filter (Place & Route)
- Assembler (Generate program)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Program)

Simulation Report

Flow Summary

Simulator

Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 30.05 ns

Pointers: 474 ps Interval: -29.58 ns Start: End:

Waves:

Name	Value
0	0 ps
1	10.0 ns
2	20.0 ns
3	30.0 ns
4	40.0 ns
5	50.0 ns
6	60.0 ns
7	70.0 ns
8	80.0 ns
9	90.0 ns
10	100.0 ns
11	110.0 ns
12	120.0 ns
13	130.0 ns
14	140.0 ns
15	150.0 ns
16	160.0 ns
17	170.0 ns
18	180.0 ns
19	190.0 ns
20	200.0 ns

Messages:

Type Message

System(10) Processing(9) Extra Info(9) Info(9) Warning Critical Warning Error Suppressed Flag /

Message: 0 of 16

For Help, press F1

here if we see the waveform report we can see that, when the waveform gets two consecutive high and one low input the output gets one . and when it gets high low high input it gets a high output. and other cases output signal is low.

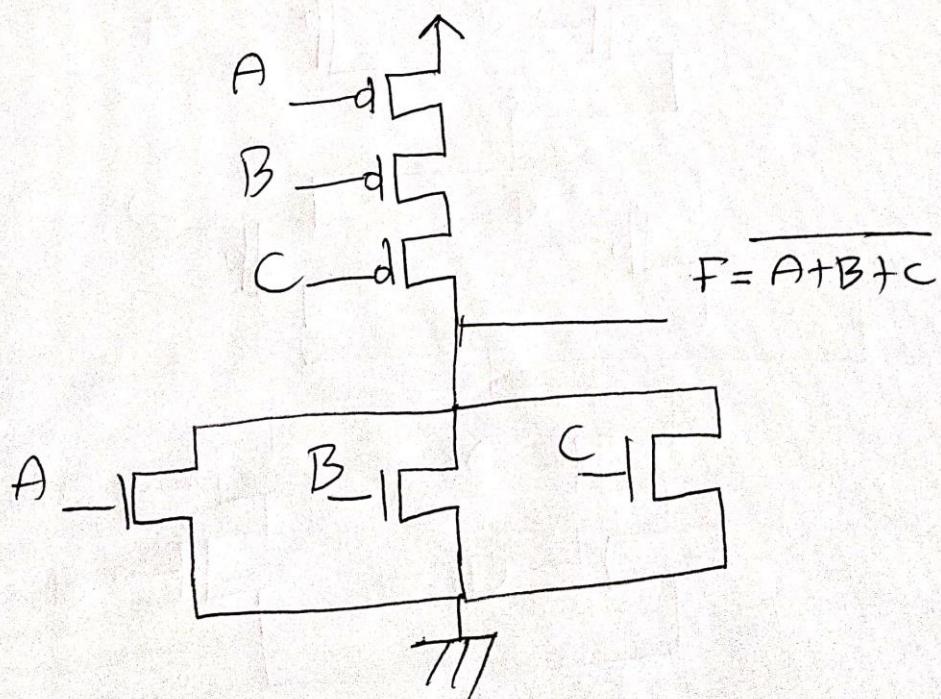
Problem 2

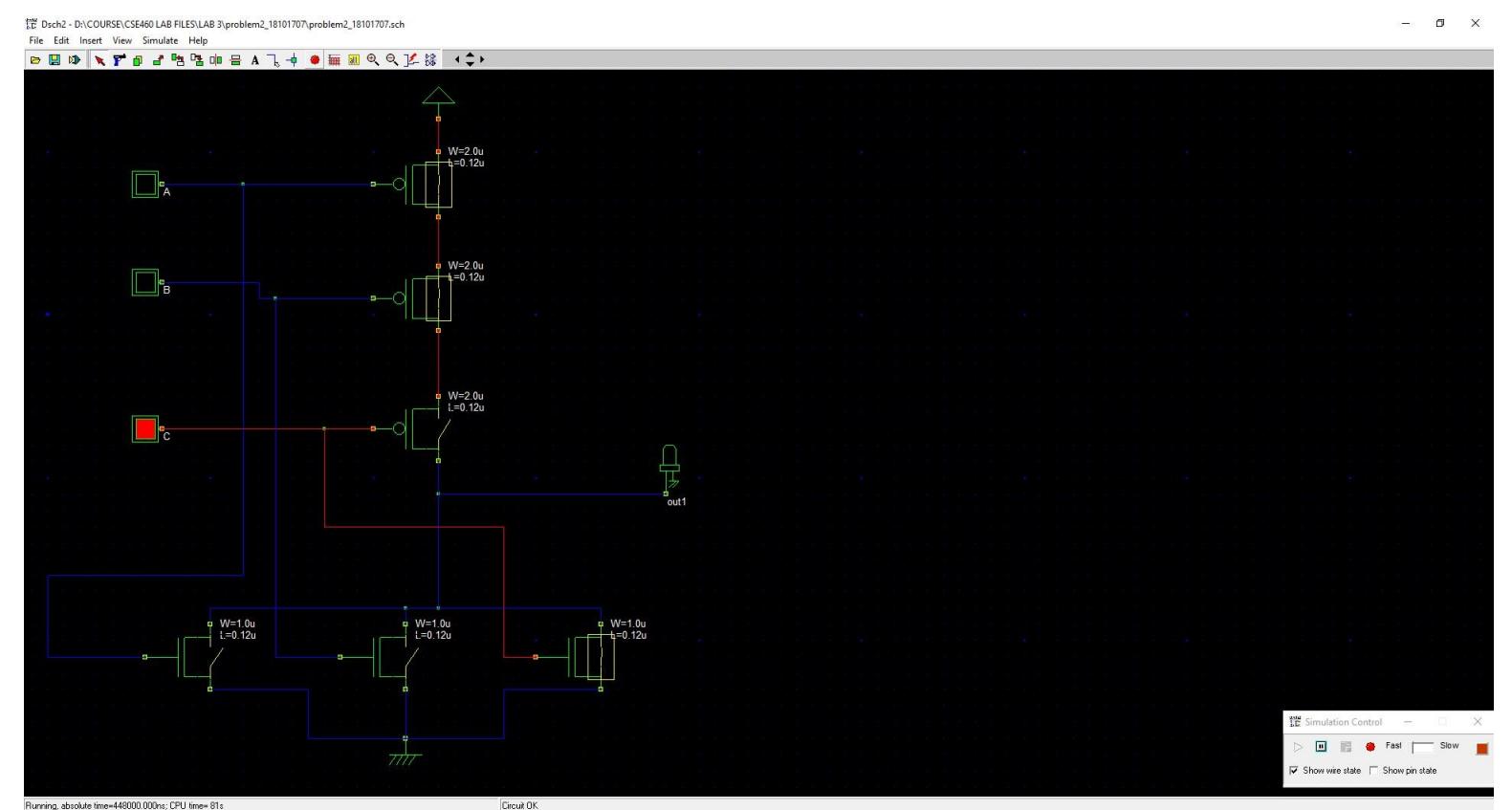
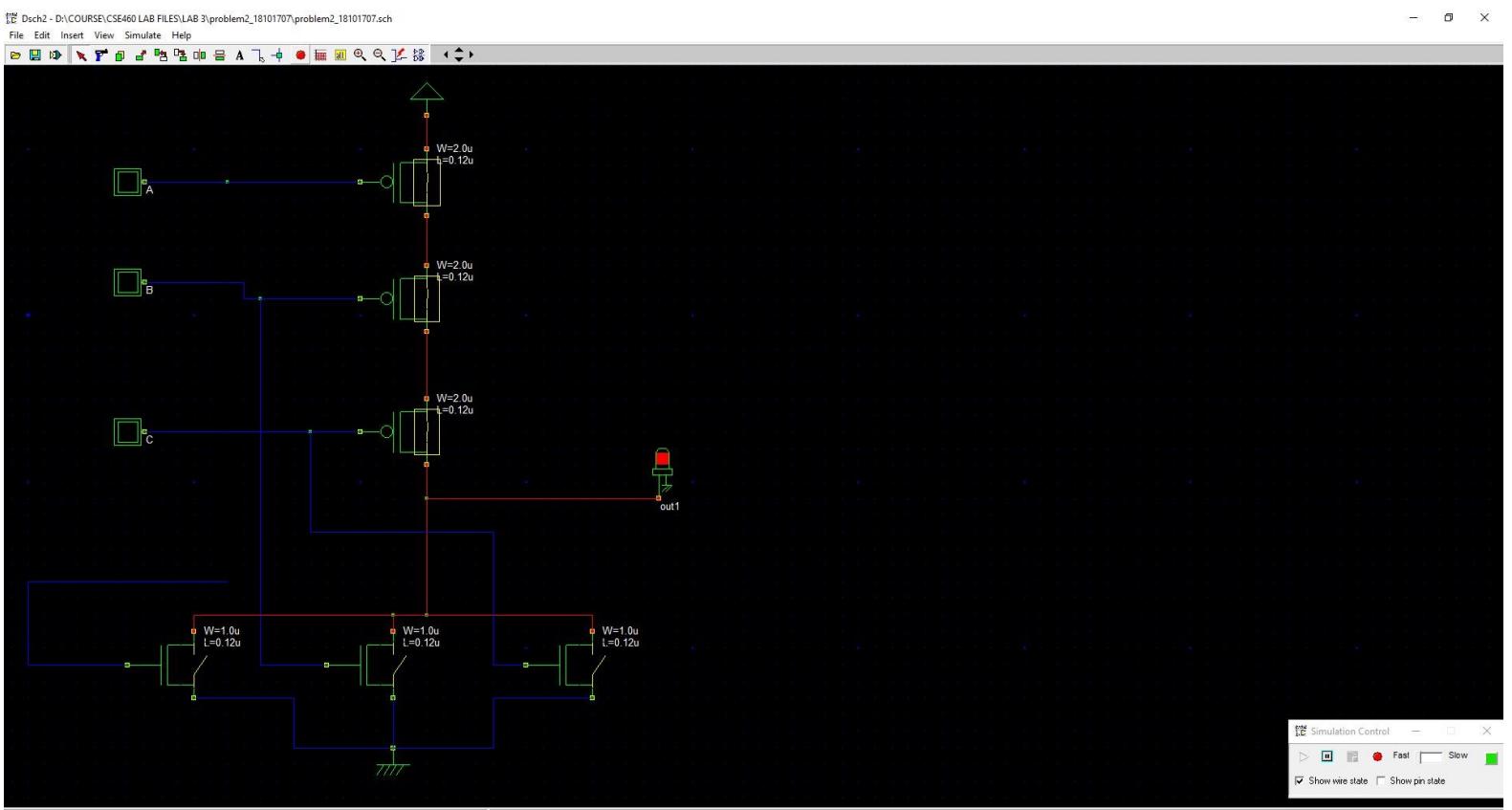
Here,  
 $F = \overline{A+B+C}$

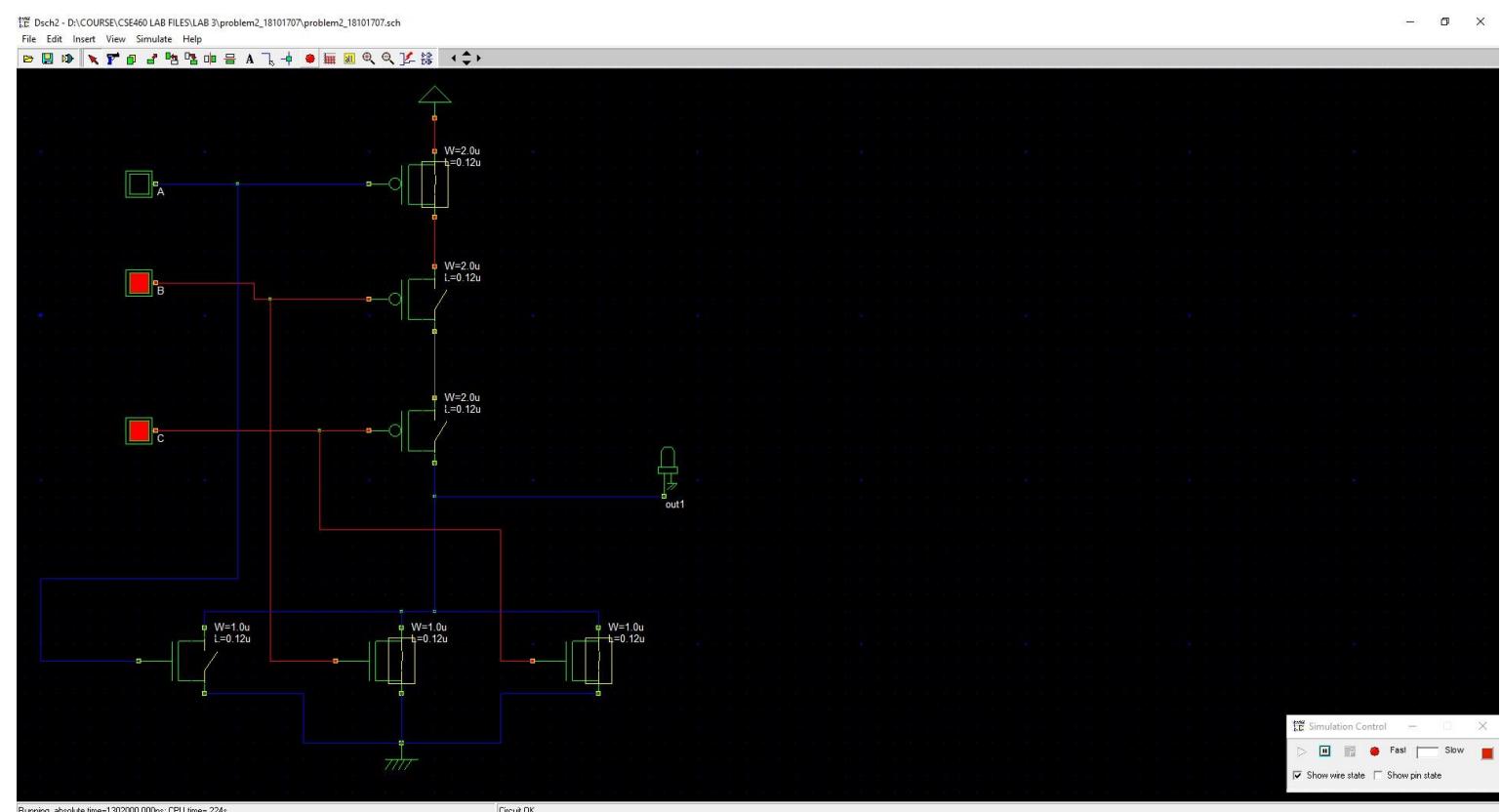
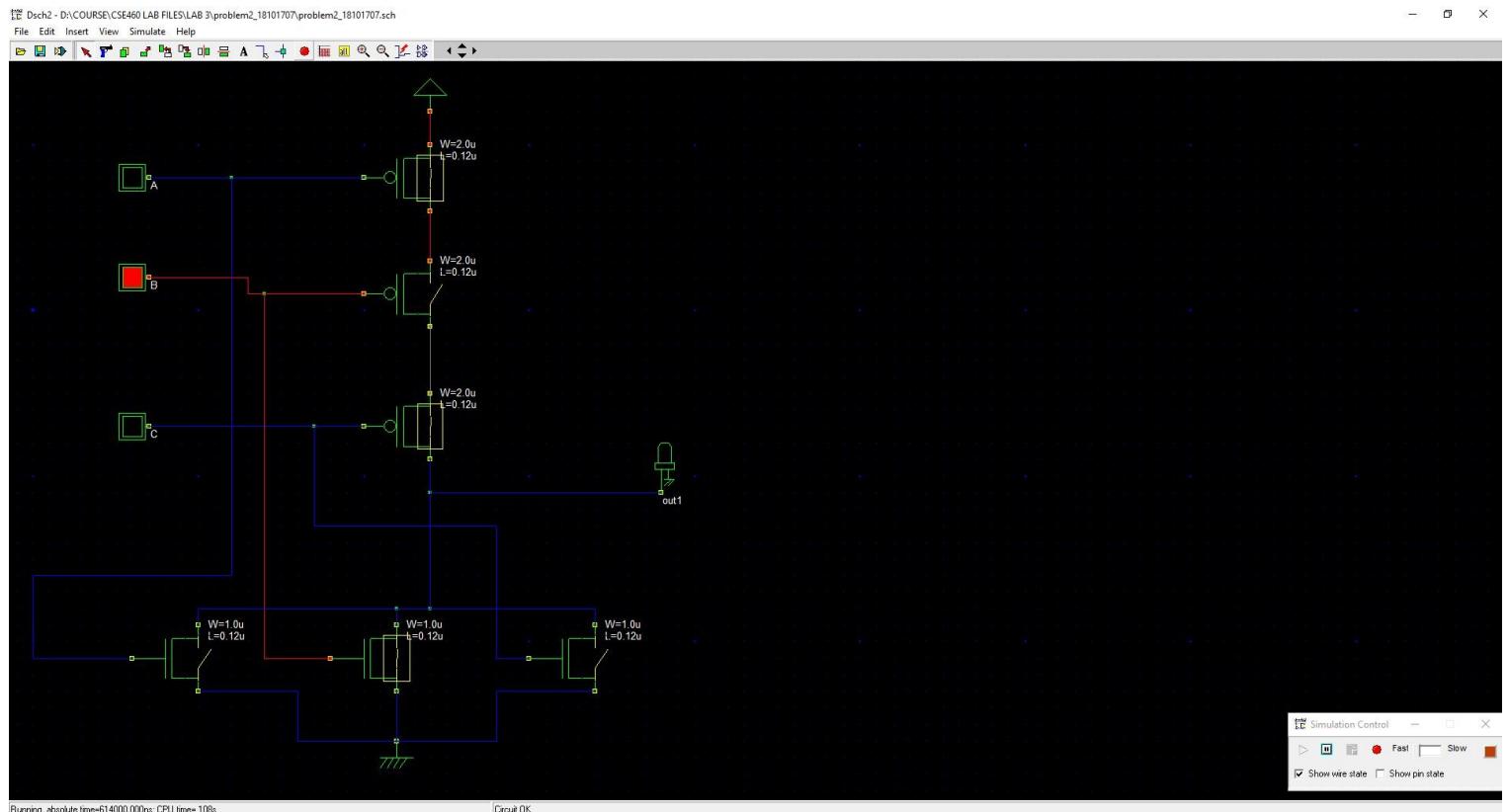
so, the truth table.

A	B	C	$F = \overline{A+B+C}$
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Here,

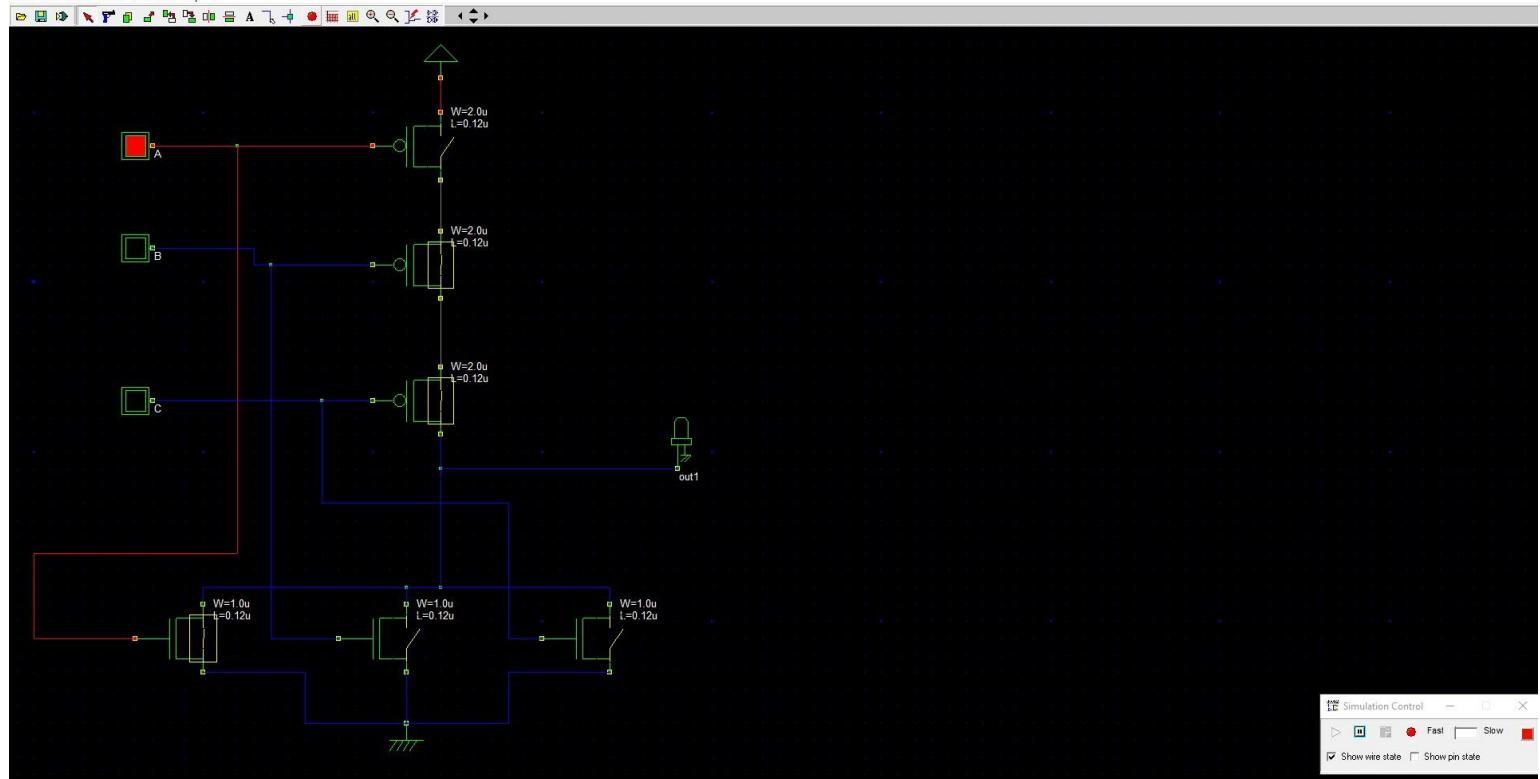






Dsch2 - D:\COURSE\CSE460 LAB FILES\LAB 3\problem2\_18101707\problem2\_18101707.sch

File Edit Insert View Simulate Help



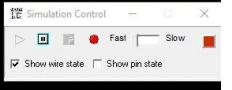
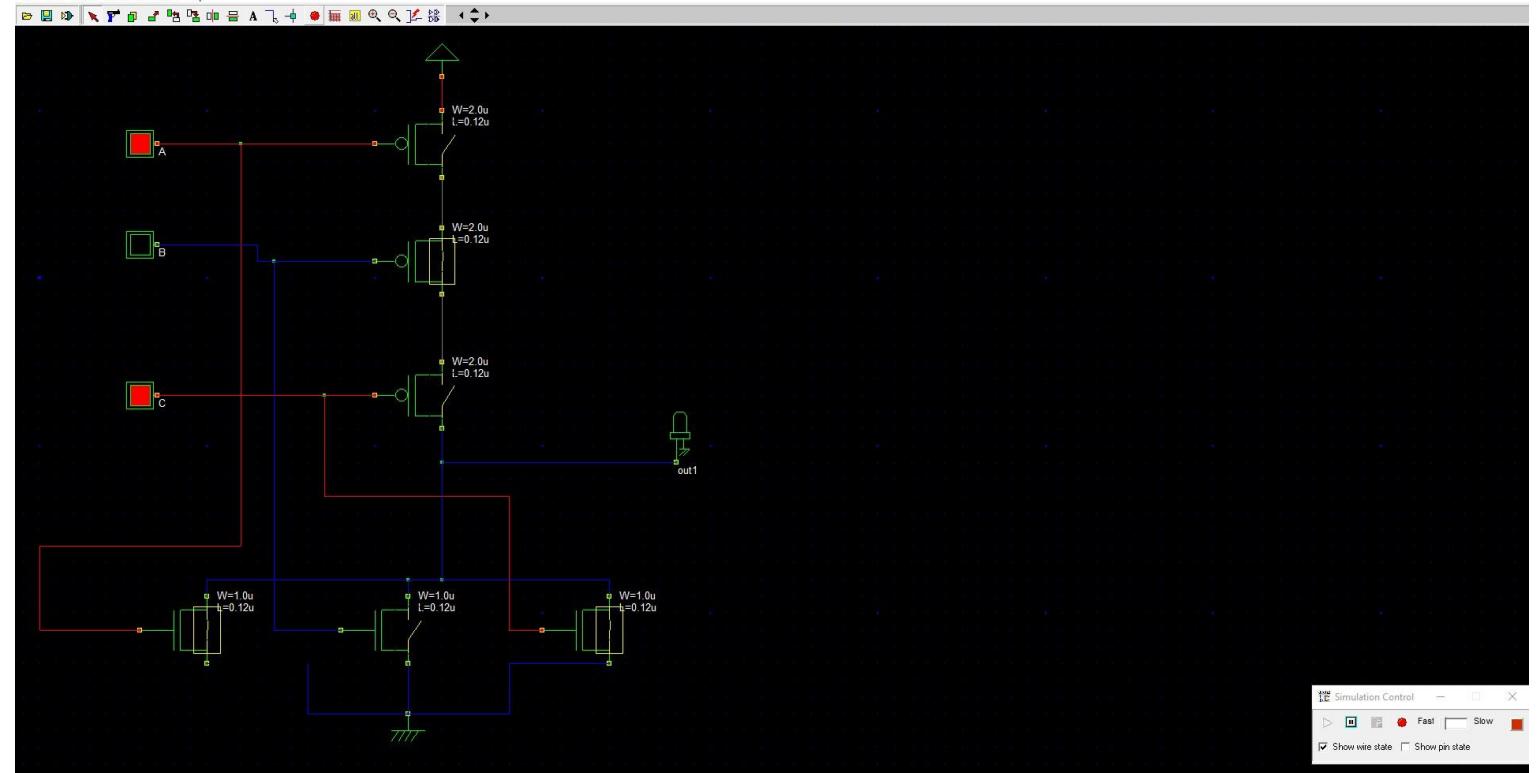
Running, absolute time=1464000.000ns; CPU time= 254s

Circuit OK



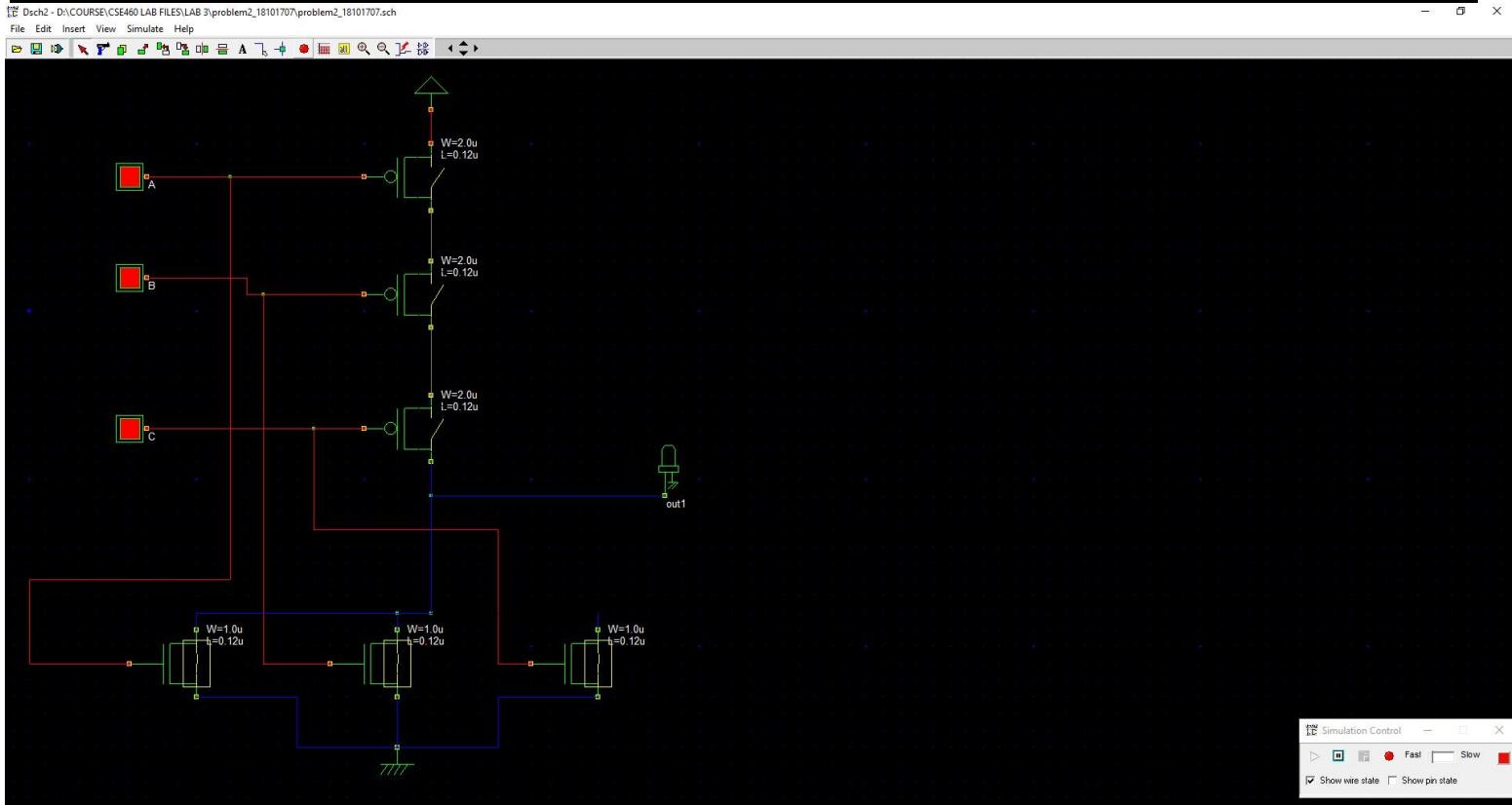
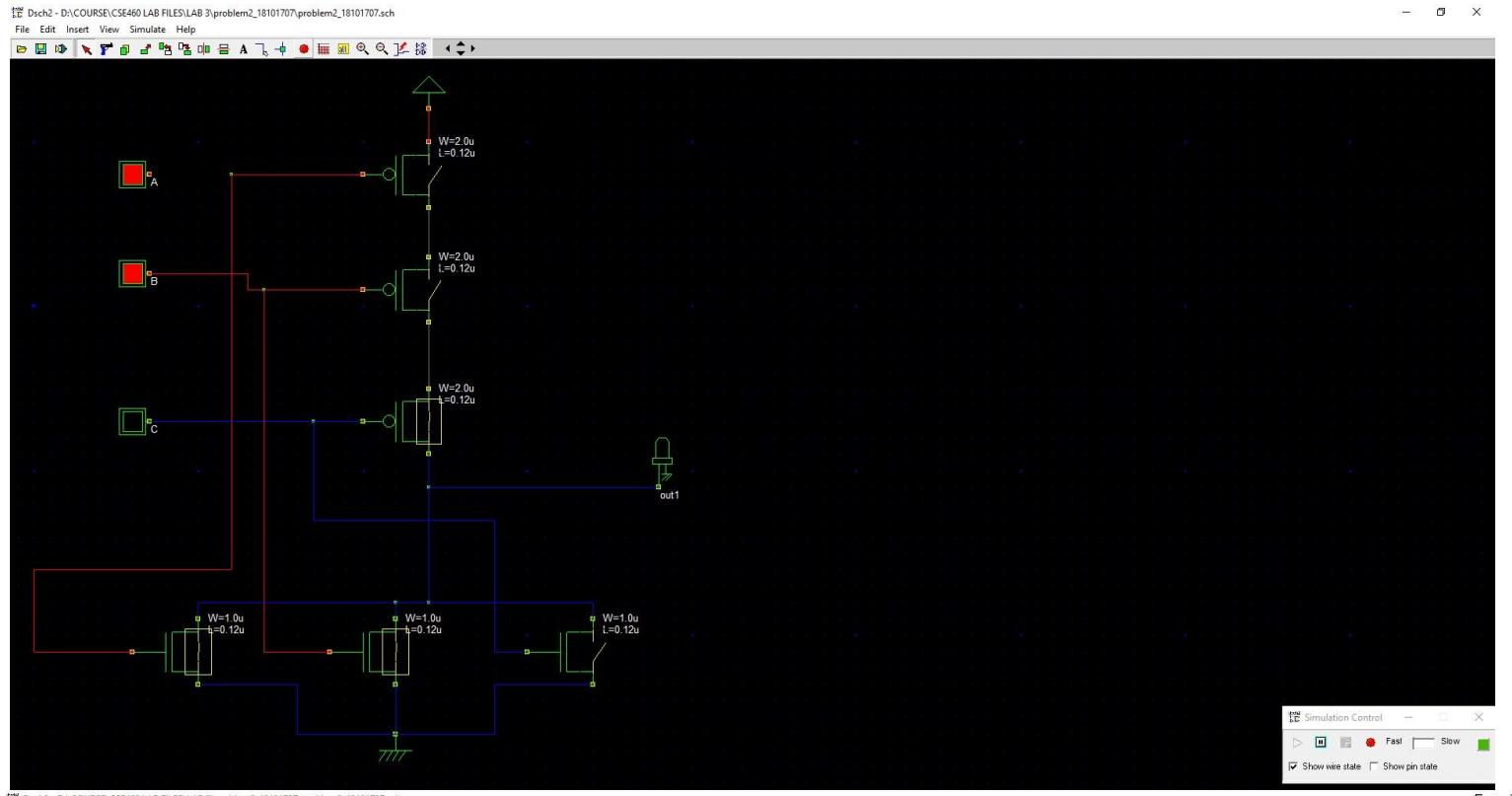
Dsch2 - D:\COURSE\CSE460 LAB FILES\LAB 3\problem2\_18101707\problem2\_18101707.sch

File Edit Insert View Simulate Help



Running, absolute time=1583000.000ns; CPU time= 277s

Circuit OK



Running, absolute time=2638000.000ns, CPU time= 473s

Circuit OK

From the truth table we can see that when ~~the~~  $\sim$  all inputs are low we get high output. The simulation result also gives us the same result.

~~AND~~  $\rightarrow$  ~~OR~~  $\rightarrow$  ~~NOT~~  $\rightarrow$  ~~AND~~  $\rightarrow$  ~~OR~~  $\rightarrow$  ~~NOT~~

I can do it  $\rightarrow$   $A \wedge B \rightarrow A \wedge \neg B \rightarrow \neg(A \wedge B) \rightarrow \neg A \vee \neg B$



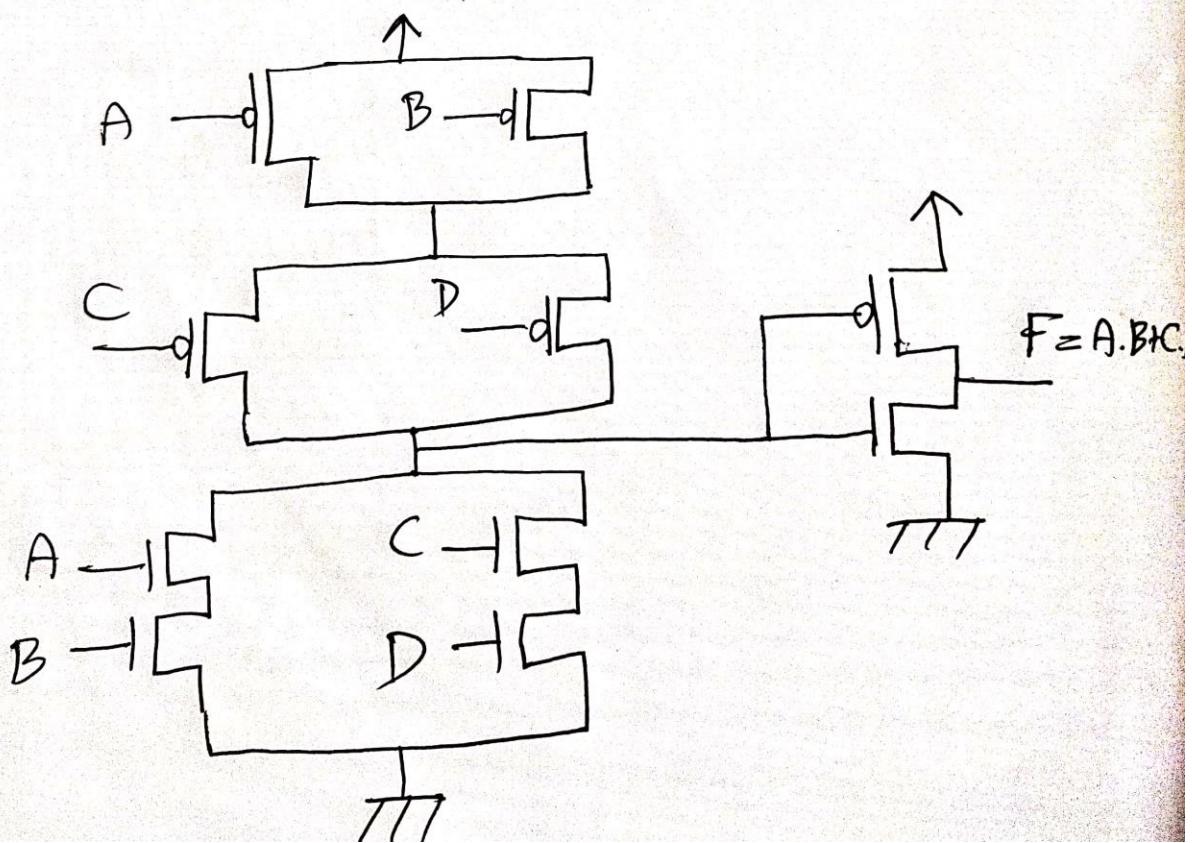
Problem 3

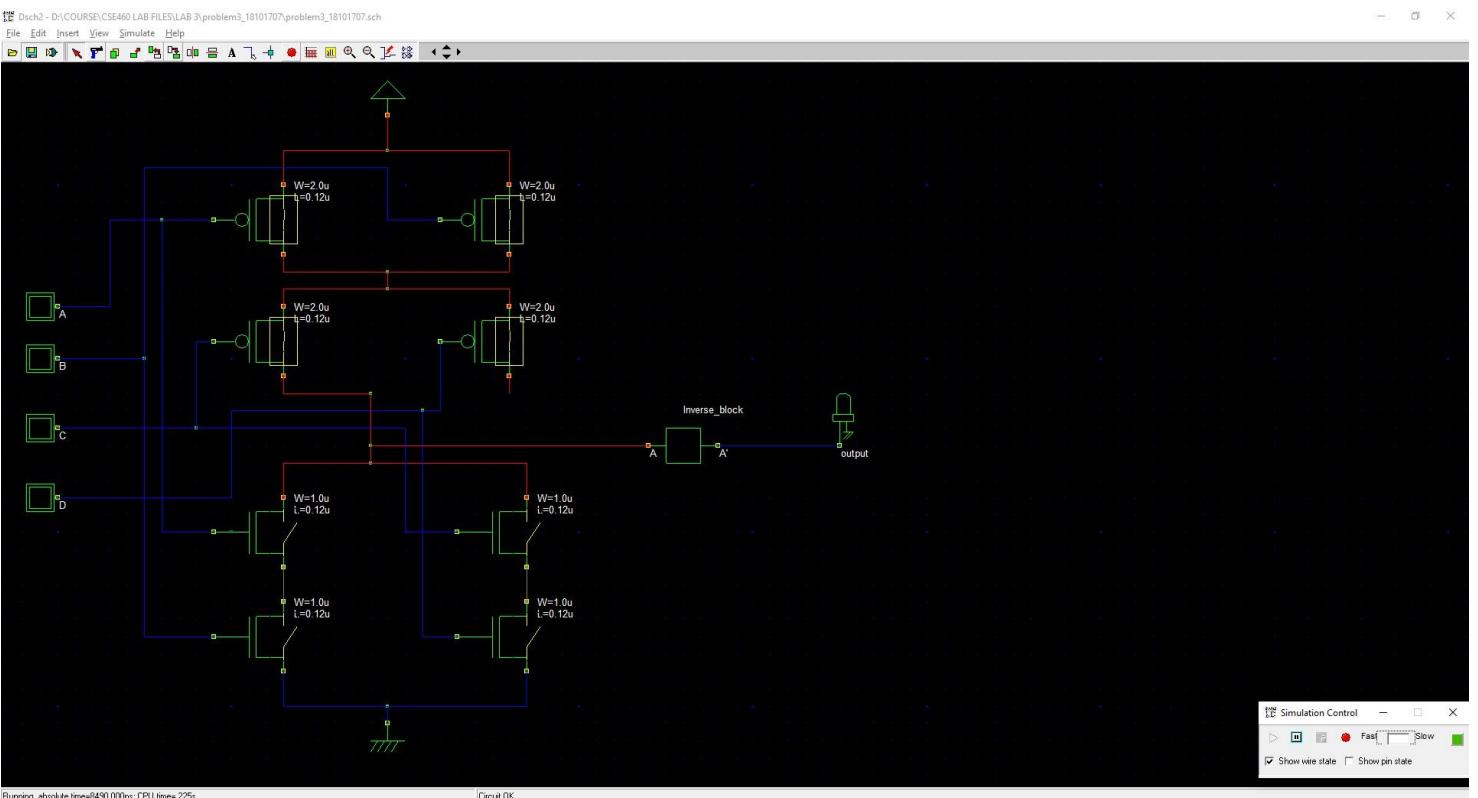
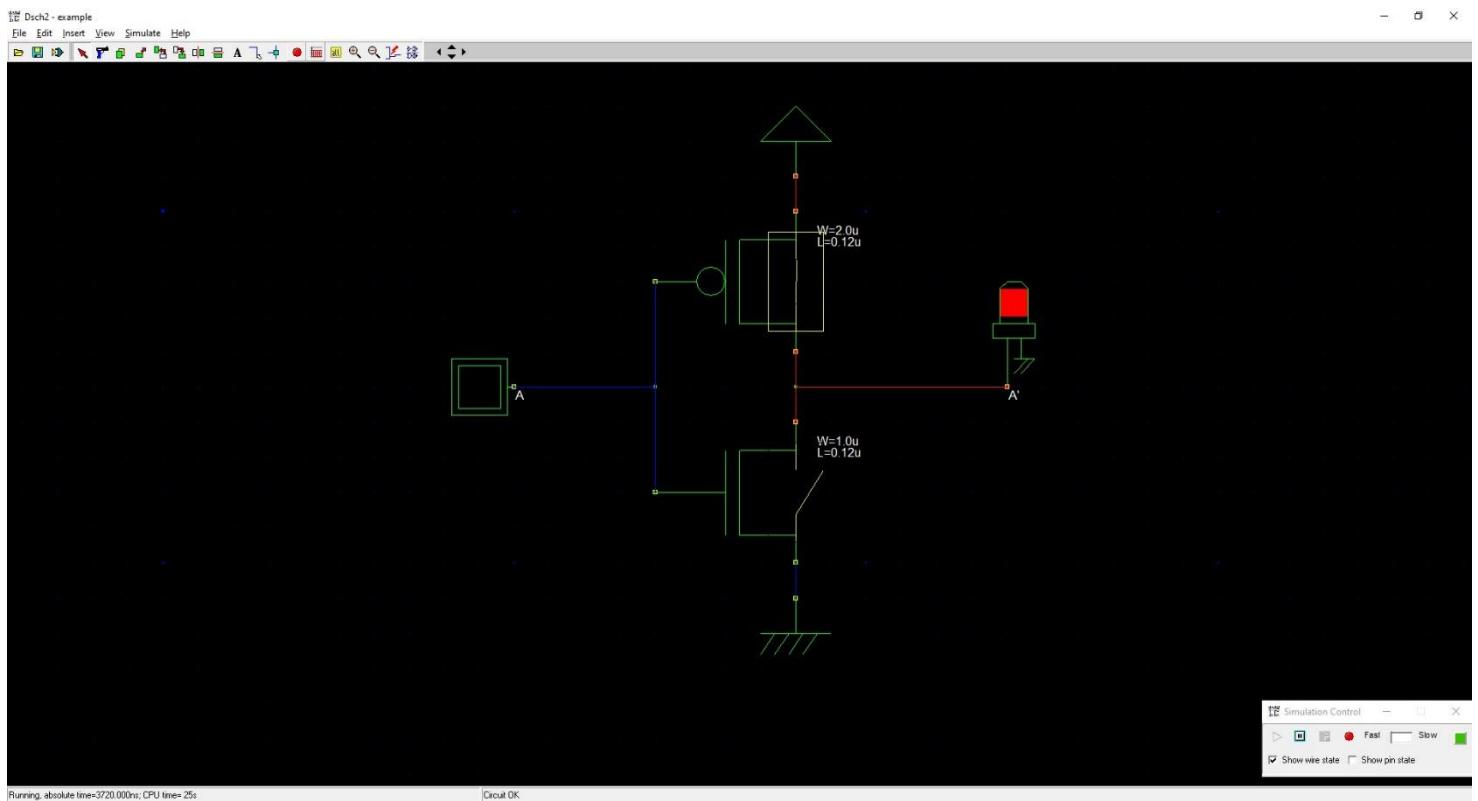
#18101707

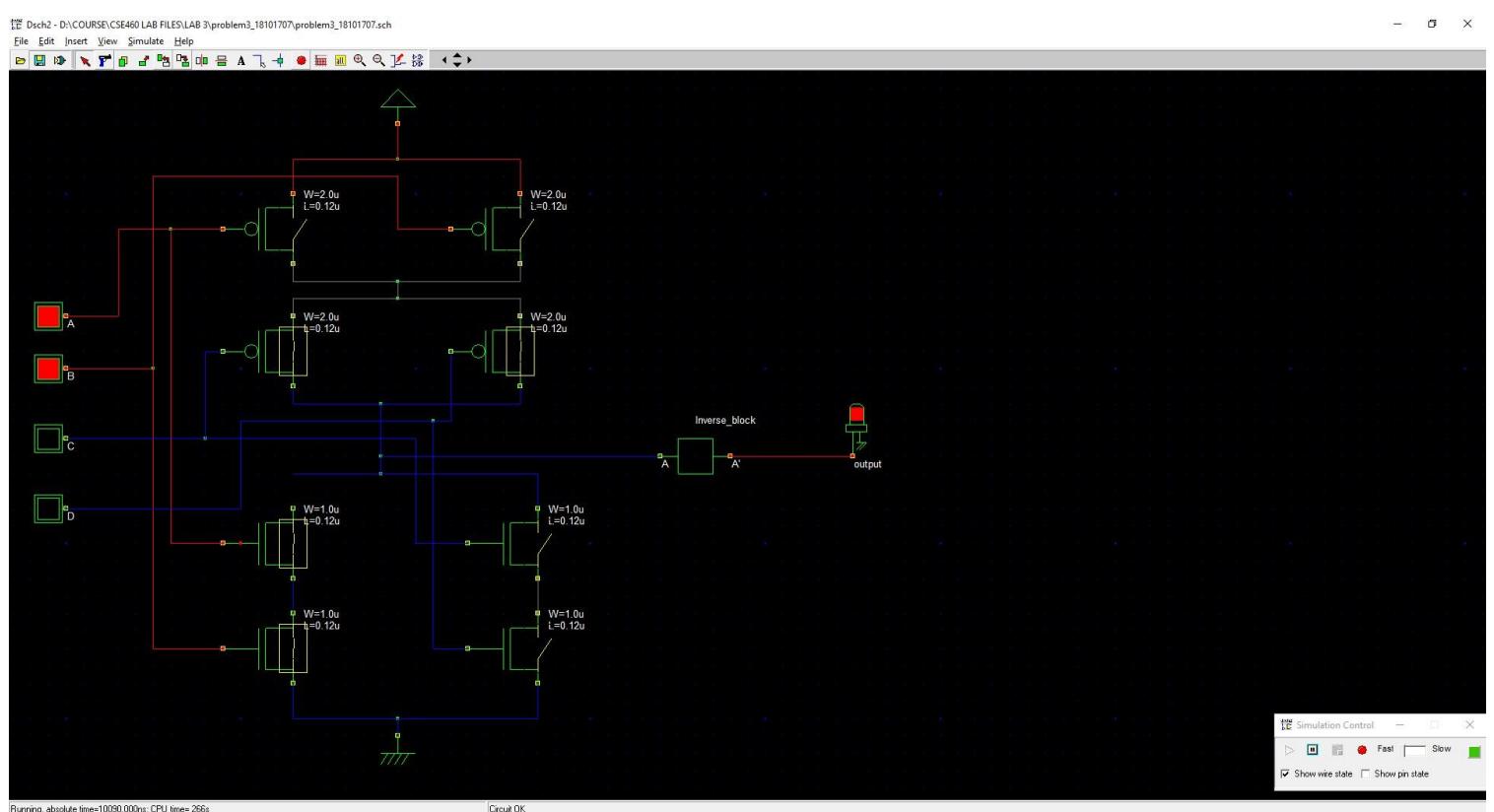
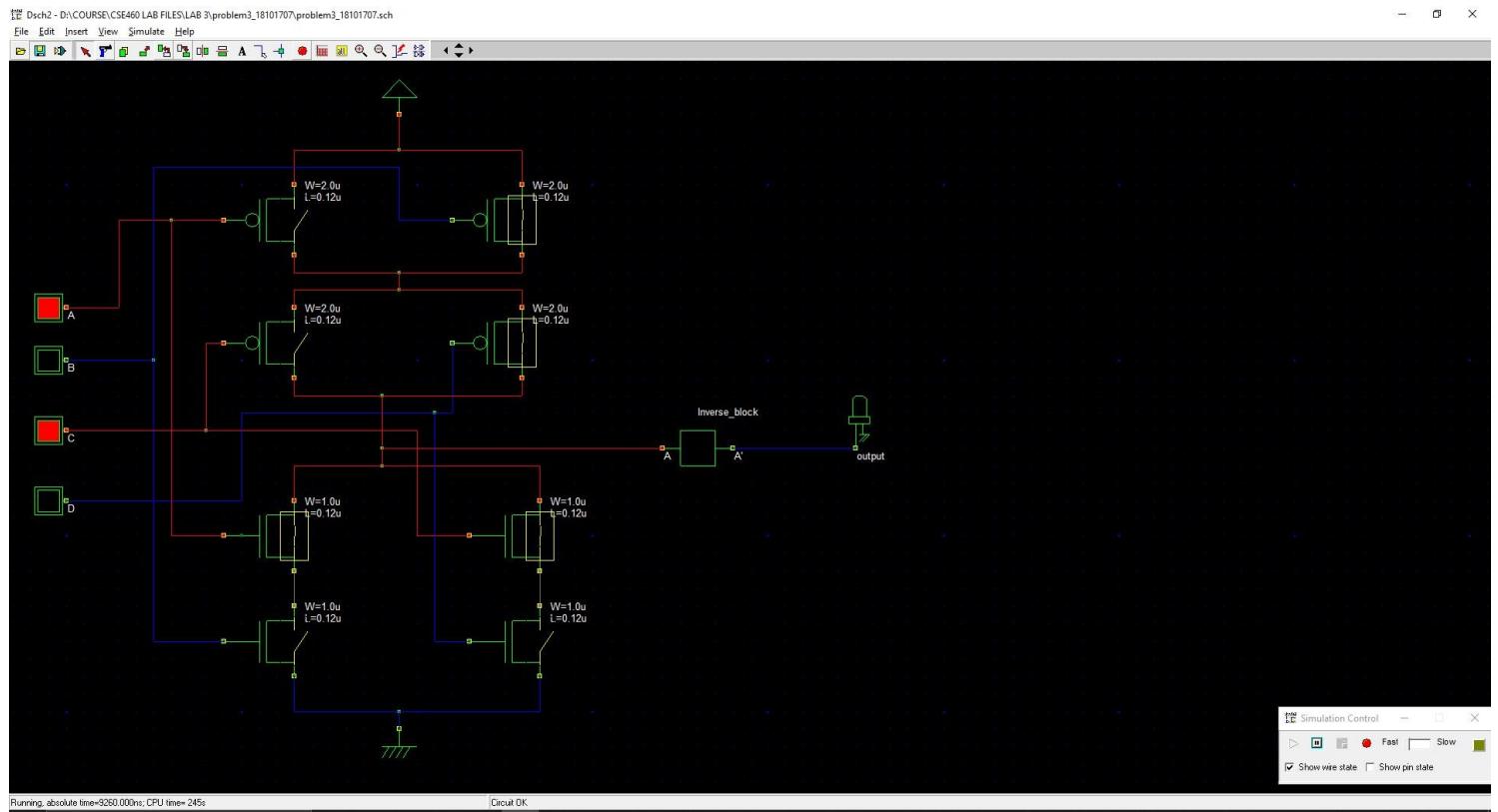
Here,

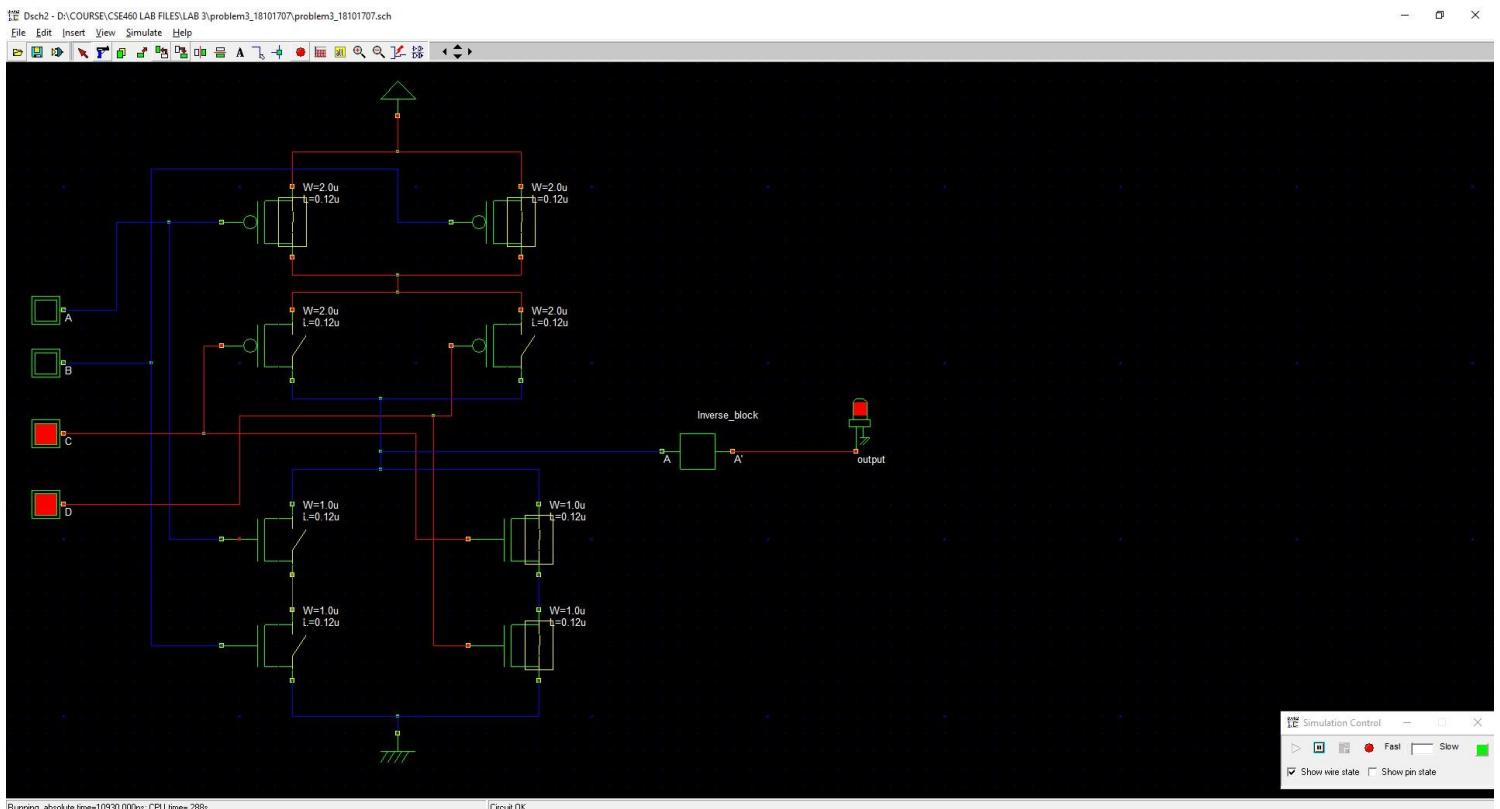
$$F = A \cdot B + C \cdot D$$

Here,  
 we are seeing that A, B are ANDed  
 and ; C, D are ANDed and their  
 output are ORed.  
 so, when A and B or C and D  
 will be high then output will  
 be high.



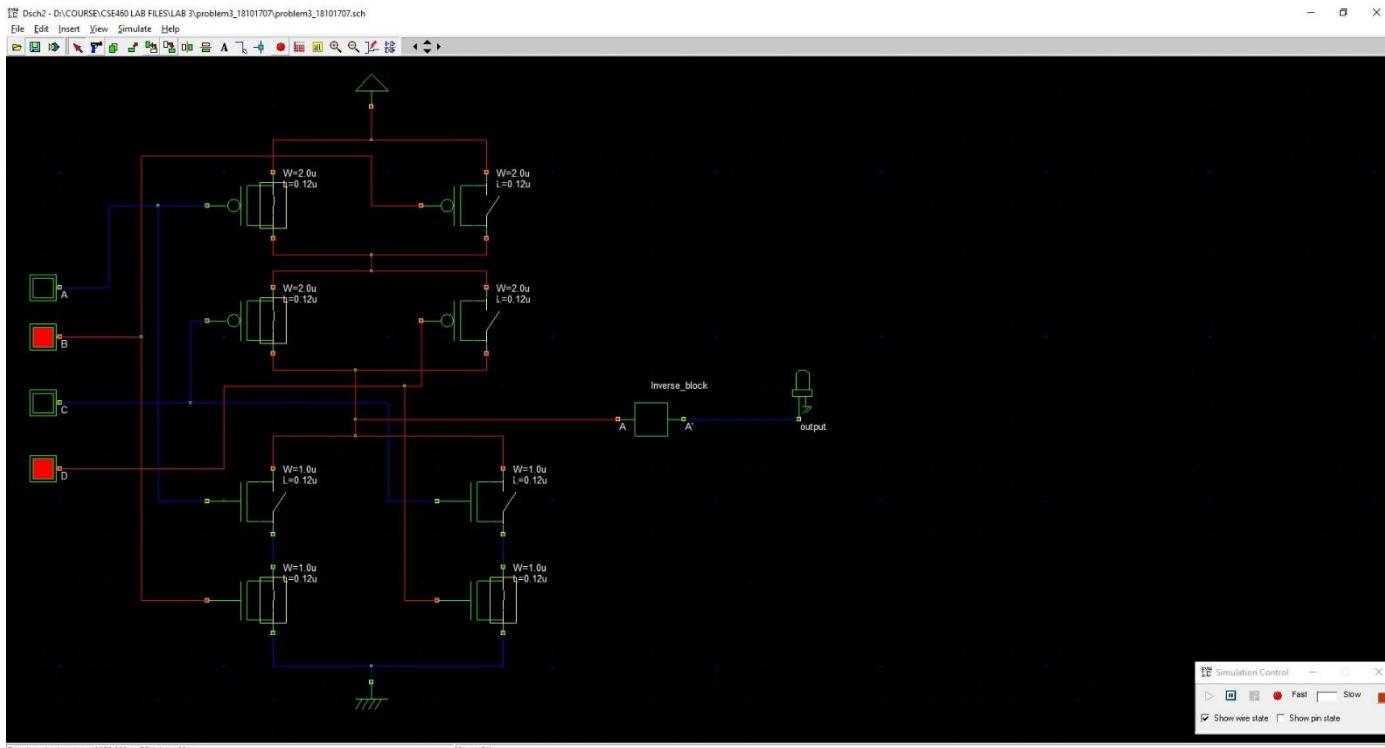






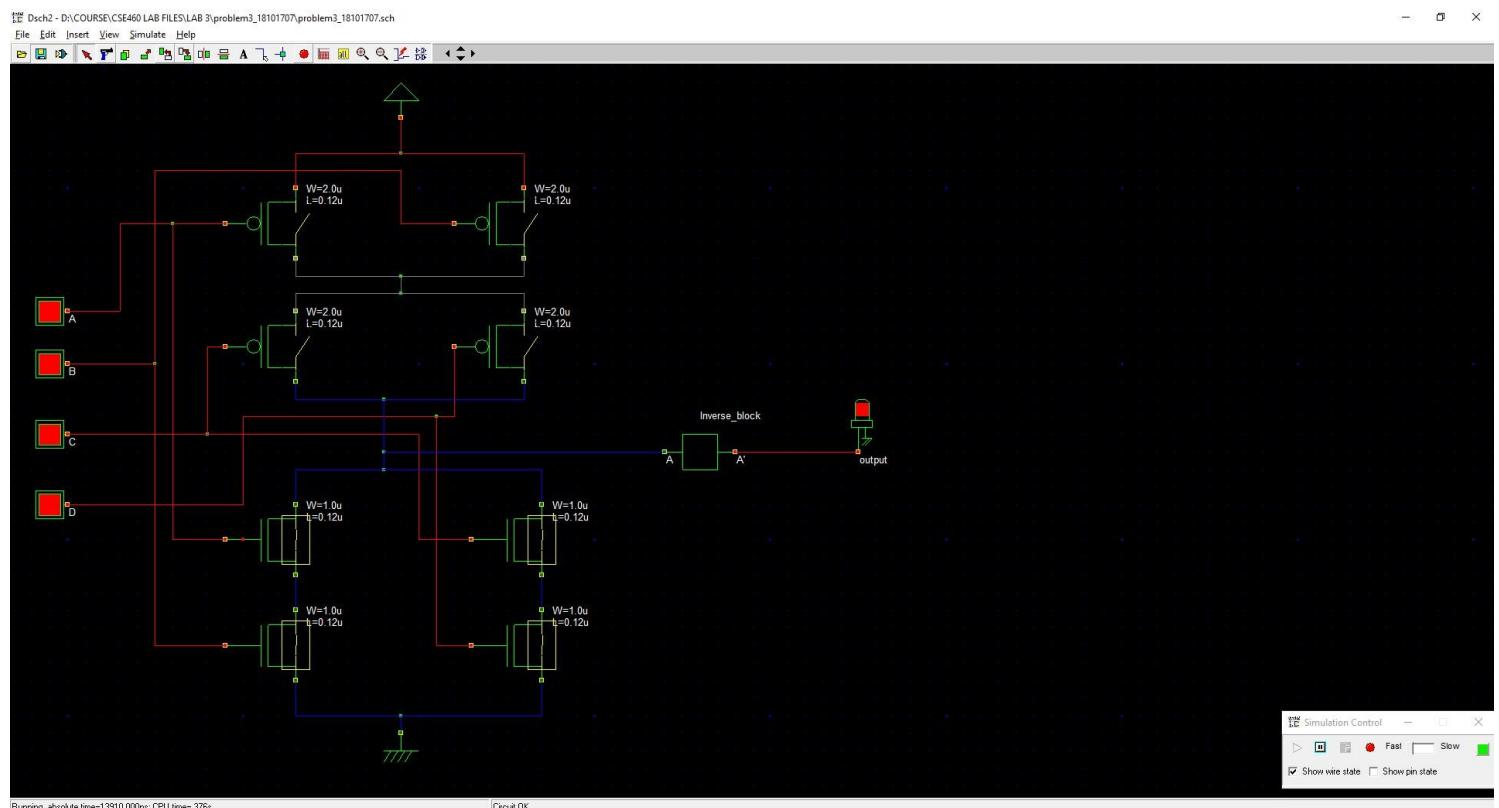
Running, absolute time=10930.000ns, CPU time= 288s

[Circuit OK]



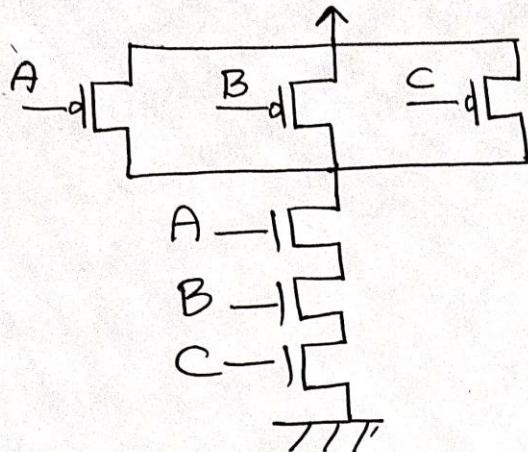
Running, absolute time=12070.000ns, CPU time= 321s

[Circuit OK]



Problem 4

#18101707



from stick diagram:

height

$$\text{width} = (5 \times 8) \lambda$$

$$= 40 \lambda$$

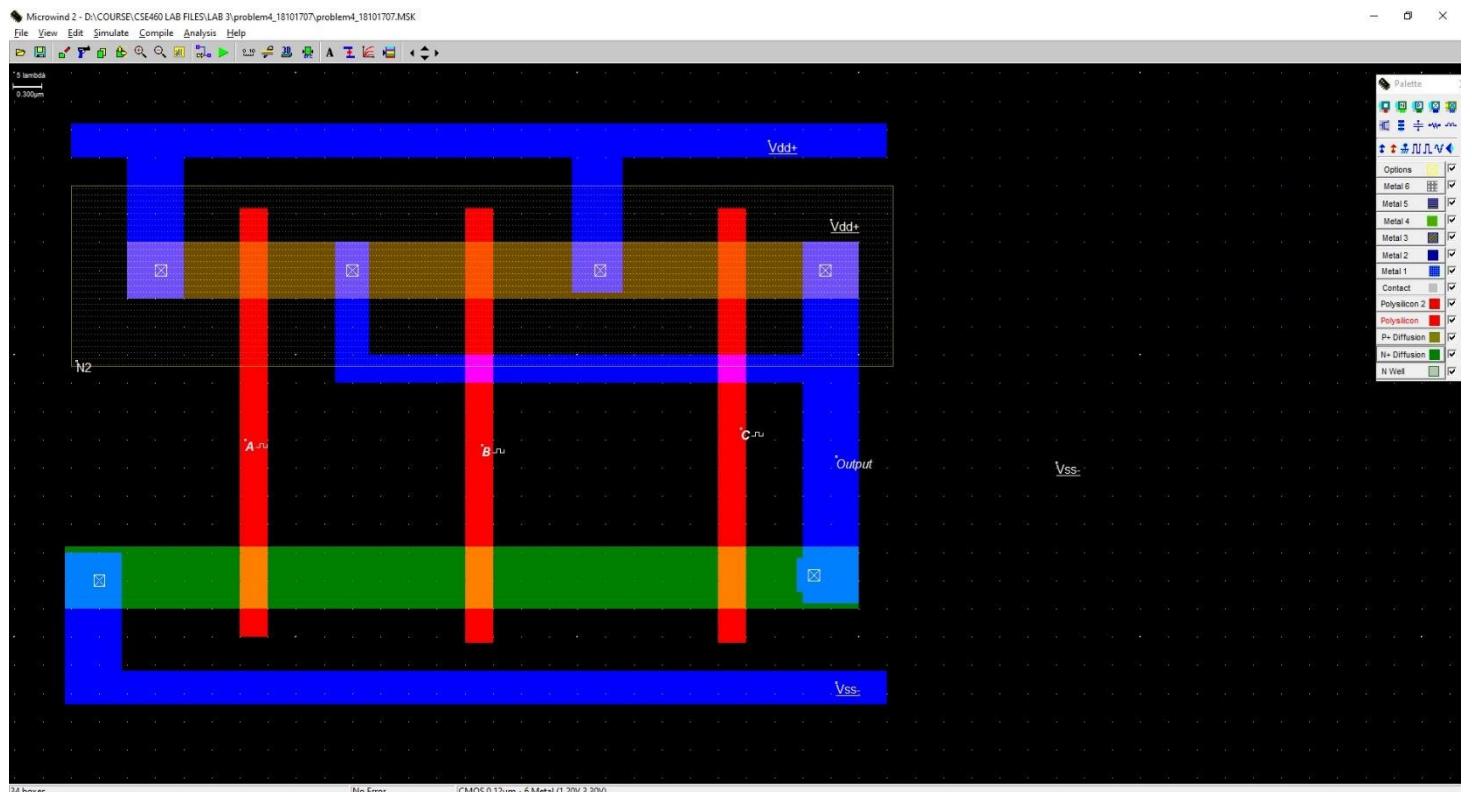
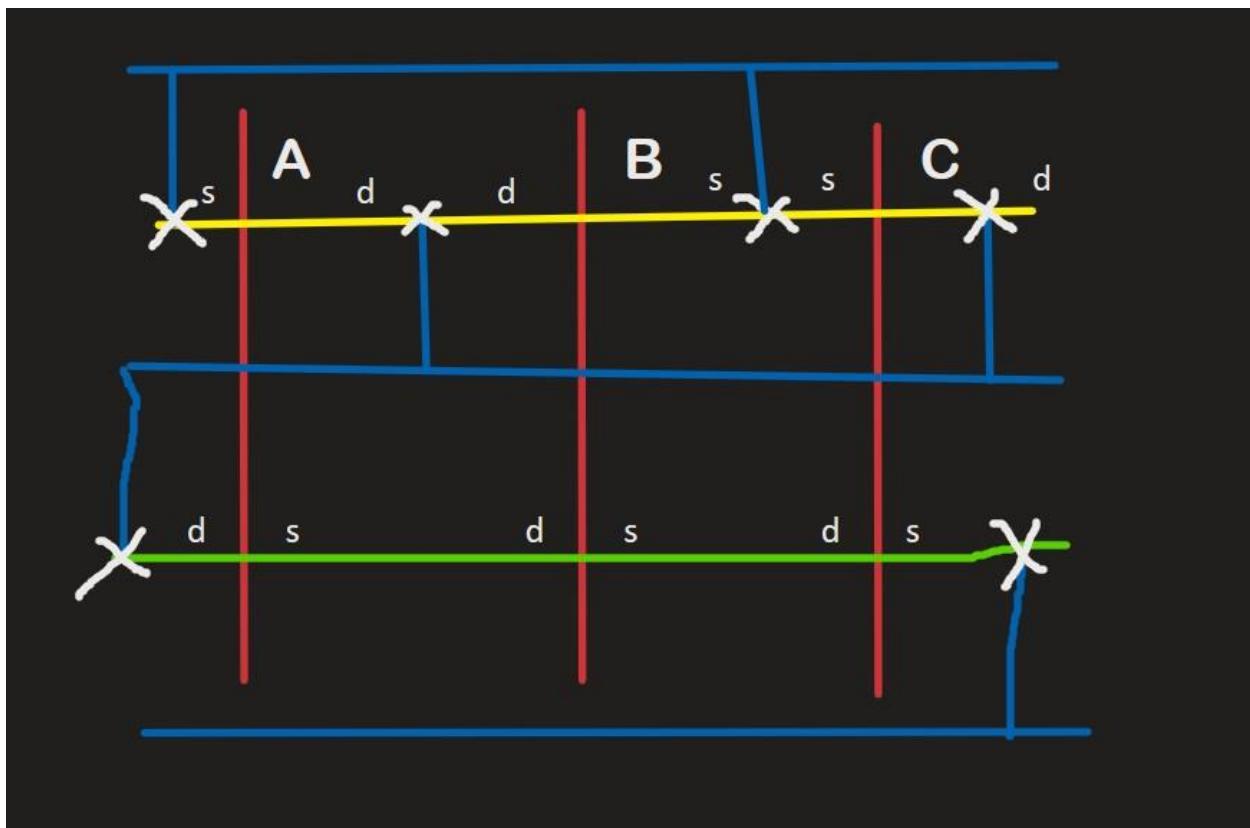
height =

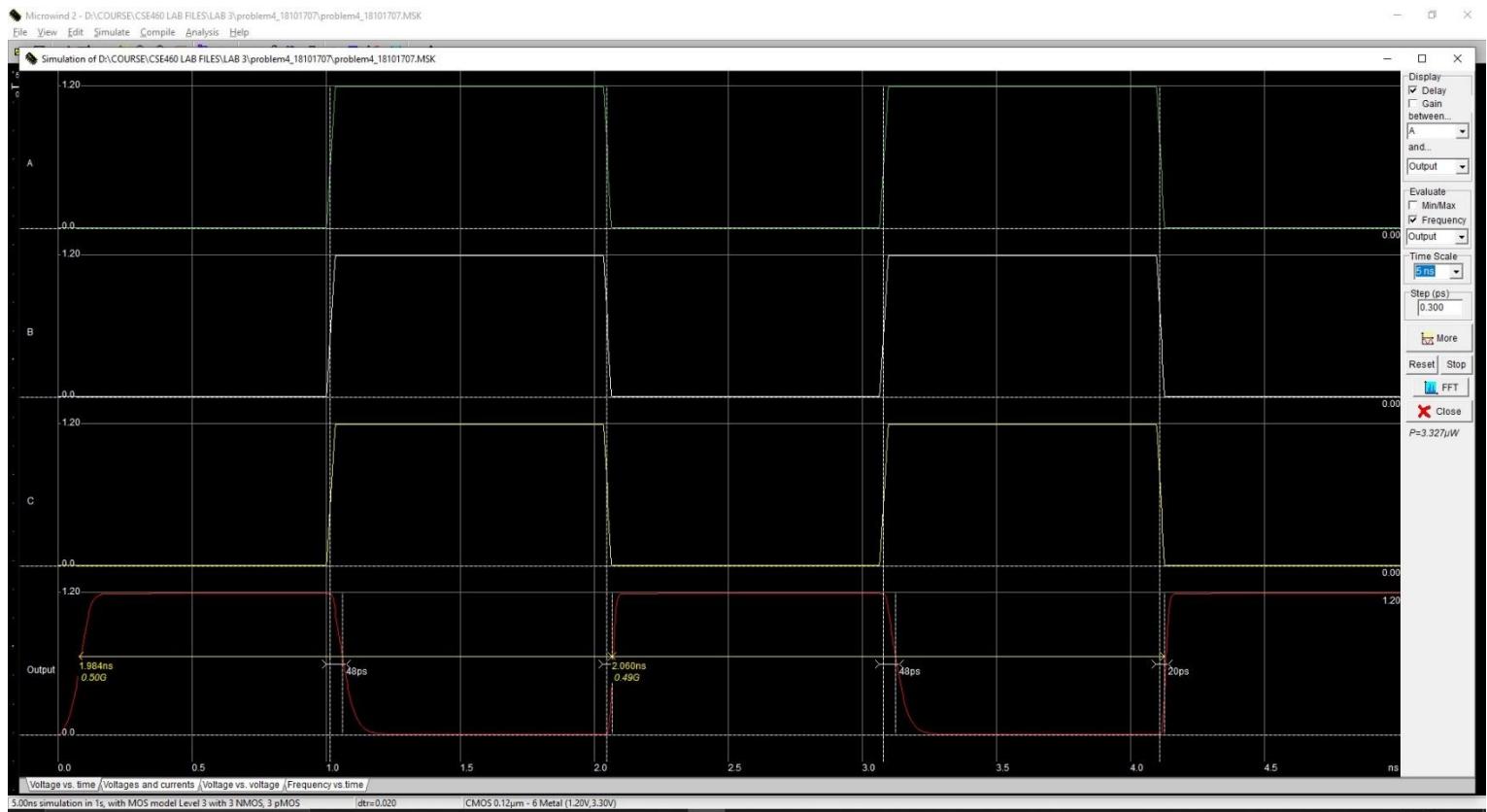
$$\text{width} = (4 \times 8) \lambda$$

$$= 32 \lambda$$

$$\text{Area} = (40\lambda \times 32\lambda)$$

$$= 1280 \lambda^2$$





For better design:

The feature size of the semiconductor is defined as the minimum length of the MOS transistor channel between the drain and source.

The design of the circuit gets better if we can decrease the feature size we can fit more circuit in same the area. The design will improve, the device would be smaller. (Explanations XOP -)

# THE END