CSE460

Lab Assignment 1

ARMAN HOSSAIN

section: 03

spring 2021

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem1_18101707/problem1_18101707 - problem1_18101707 - [problem1_18101707.v]

File Edit View Project Assignments Processing Tools Window Help

problem1_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
  - Program Device (Open Program

problem1_18101707.v | problem1_18101707.vwf | Simulation Report - Simulation Waveforms

```
1
2  module problem1_18101707(A,B,S,addorsub,cout);
3
4  input [4:0]A,B;
5  input addorsub;
6  output [4:0]S;
7  output cout;
8
9  wire [4:0]x;
10
11 xor(x[0],B[0],addorsub);
12 xor(x[1],B[1],addorsub);
13 xor(x[2],B[2],addorsub);
14 xor(x[3],B[3],addorsub);
15 xor(x[4],B[4],addorsub);
16
17 fulladd stage0(S[0],cout0,A[0],x[0],addorsub);
18 fulladd stage1(S[1],cout1,A[1],x[1],cout0);
19 fulladd stage2(S[2],cout2,A[2],x[2],cout1);
20 fulladd stage3(S[3],cout3,A[3],x[3],cout2);
21 fulladd stage4(S[4],cout ,A[4] ,x[4],cout3);
22 endmodule
23
24 module fulladd(s,cout,a,b,cin);
25
26 input a,b,cin;
27 output s,cout;
28
29 assign s=a^b^cin;
30 assign cout= ( a & b ) | ( cin & (a ^ b ));
31 endmodule
32
```

Type	Message
	Info: Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 1/problem1_18101707/problem1_18101707.vwf"
	Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
	Info: Simulation partitioned into 1 sub-simulations
	Info: Simulation coverage is 100.00 %
	Info: Number of transitions in simulation is 9237
	Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (5) | Processing (9) | Extra Info | Info (9) | Warning | Critical Warning | Error | Suppressed | Flag

Message: 0 of 16 | Location: | Locate

For Help, press F1 | Ln 1, Col 1 | Idle | NUM

Type here to search | ENG | 8:55 PM 2021-03-21

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem1_18101707/problem1_18101707 - problem1_18101707 - [Compilation Report - Flow Summary]

File Edit View Project Assignments Processing Tools Window Help

problem1_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Program

problem1_18101707.v | problem1_18101707.vwf | Simulation Report - Simulation Waveforms | **Compilation Report - Flow Summary**

- Compilation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
  - Flow Non-Default Global Se
  - Flow Elapsed Time
  - Flow OS Summary
  - Flow Log
  - Analysis & Synthesis
  - Fitter
  - Assembler
  - Timing Analyzer
  - EDA Netlist Writer

Flow Summary

Flow Status	Successful - Sun Mar 21 20:55:32 2021
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	problem1_18101707
Top-level Entity Name	problem1_18101707
Family	FLEX10KE
Met timing requirements	Yes
Total logic elements	10 / 1,728 (< 1 %)
Total pins	17 / 102 (17 %)
Total memory bits	0 / 24,576 (0 %)
Total PLLs	0
Device	EPF10K30ETC144-1
Timing Models	Final

Type | Message

```
Info: ******************************************************************
Info: Running Quartus II EDA Netlist Writer
Info: Command: quartus_eda --read_settings_files=off --write_settings_files=off problem1_18101707 -c problem1_18101707
Info: Generated files "problem1_18101707.vo" and "problem1_18101707_v.sdo" in directory "D:/COURSE/CSE460 LAB FILES/LAB 1/problem1_18101707/simulation/custom/" for EDA simulation tool
Info: Generated files "problem1_18101707.vo" and "problem1_18101707_v.sdo" in directory "D:/COURSE/CSE460 LAB FILES/LAB 1/problem1_18101707/timing/custom/" for EDA timing analysis tool
Info: Quartus II EDA Netlist Writer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 7 warnings
```

System (7) | **Processing (49)** | Extra Info | Info (42) | Warning (7) | Critical Warning | Error | Suppressed | Flag

Message: 0 of 97 | Location: | Locate

Messages

For Help, press F1 | Idle | NUM

Type here to search | ENG | 8:55 PM 2021-03-21

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem1_18101707/problem1_18101707 - problem1_18101707 - [Simulation Report - Simulation Waveforms]

File Edit View Project Assignments Processing Tools Window Help

problem1_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Program

problem1_18101707.v | problem1_18101707.vwf | Simulation Report - Simulation Waveforms

- Simulation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
  - Simulator
    - Summary
    - Settings
    - Simulation Waveforms
    - Simulation Coverage
    - INI Usage
    - Messages

Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 30.05 ns | Pointer: 704 ps | Interval: -29.35 ns | Start: | End:

	Name	0 ps	10.0 ns	20.0 ns	30.0 ns	30.05 ns			
0	A	[23]	[13]	[21]	[16]	[27]	[22]	[7]	[18]
6	B	[16]	[12]	[15]	[23]	[27]	[22]	[25]	[0]
12	S	[7]	[25]	[6]	[7]	[0]	[12]	[14]	[18]
18	cout								
19	addorsub								

Type	Message
	Info: Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 1/problem1_18101707/problem1_18101707.vwf"
	Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
	Info: Simulation partitioned into 1 sub-simulations
	Info: Simulation coverage is 100.00 %
	Info: Number of transitions in simulation is 9237
	Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (5) | Processing (9) | Extra Info | Info (9) | Warning | Critical Warning | Error | Suppressed | Flag

Message: 0 of 16 | Location: | Locate

For Help, press F1 | Idle | NUM

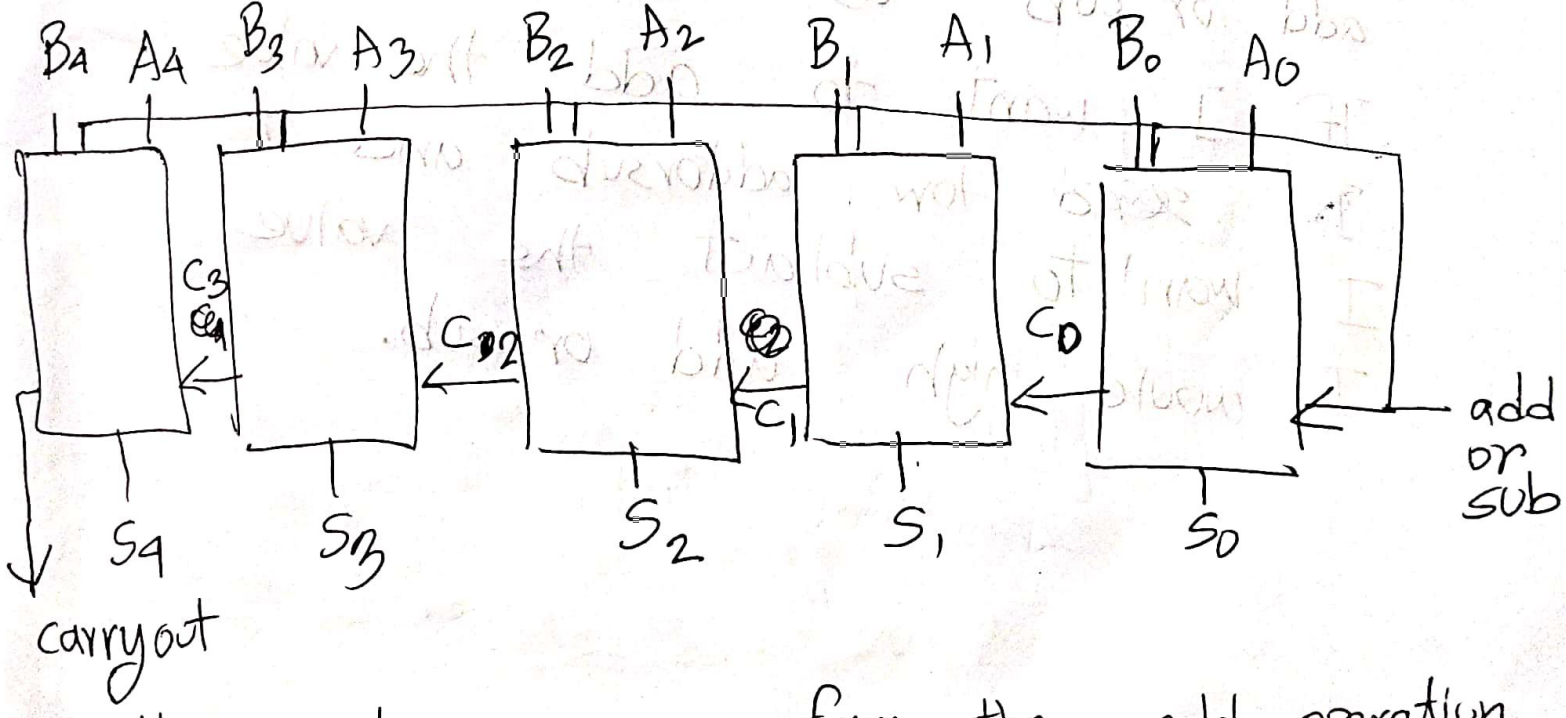
Type here to search | ENG | 8:54 PM 2021-03-21

Report of LAB assignment 1

#1810707
ARMAN HOSSAIN

Problem no 1

Here is the 5 bit adder subtractor block diagram which helped me to code.



Here when we perform the add operation add or sub will be low so, A and B will simply add.

But in terms of substraction, we need to use 2's compliment. In order to

achieve that, I am using XOR to every bit of input B. add XOR gate simply inverses the input and I sent a 1 as ~~carry~~ initial carry to do 2's compliment.

Here in the code I am using add or sub as the command. If I want to add the value I ~~send~~ low addorsub and if I want to subtract the value I would high add or sub.

#1810707

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem2_18101707/problem2_18101707 - problem2_18101707 - [problem2_18101707.v]

File Edit View Project Assignments Processing Tools Window Help

problem2_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Program

problem2_18101707.v | problem2_18101707.vwf | Compilation Report - Flow Summary | Simulation Report - Simulation Waveforms

```
1  module problem2_18101707(in,out);
2
3  input [3:0]in;
4  output reg [1:0]out;
5
6  always@(in)
7  begin
8      if(in[3])
9          out=2'b11;
10     else if(in[0])
11         out=2'b00;
12     else if(in[1])
13         out=2'b01;
14     else
15         out=2'b10;
16 end
17
18 endmodule
19
20
```

Type	Message
	Info: Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 1/problem2_18101707/problem2_18101707.vwf"
	Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
	Info: Simulation partitioned into 1 sub-simulations
	Info: Simulation coverage is 100.00 %
	Info: Number of transitions in simulation is 513
	Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (6) | Processing (9) | Extra Info | Info (9) | Warning | Critical Warning | Error | Suppressed | Flag

Message: 0 of 16 | Location: | Locate

Messages

For Help, press F1 | Ln 15, Col 19 | Idle | NUM

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem2_18101707/problem2_18101707 - problem2_18101707 - [Compilation Report - Flow Summary]

File Edit View Project Assignments Processing Tools Window Help

problem2_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Program

problem2_18101707.v | problem2_18101707.vwf | Compilation Report - Flow Summary | Simulation Report - Simulation Waveforms

- Compilation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
  - Flow Non-Default Global Se
  - Flow Elapsed Time
  - Flow OS Summary
  - Flow Log
  - Analysis & Synthesis
  - Fitter
  - Assembler
  - Timing Analyzer
  - EDA Netlist Writer

Flow Summary

Flow Status	Successful - Mon Mar 22 15:51:06 2021
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	problem2_18101707
Top-level Entity Name	problem2_18101707
Family	FLEX10KE
Met timing requirements	Yes
Total logic elements	2 / 1,728 (< 1 %)
Total pins	6 / 102 (6 %)
Total memory bits	0 / 24,576 (0 %)
Total PLLs	0
Device	EPF10K30ETC144-1
Timing Models	Final

Type	Message
	Info: Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 1/problem2_18101707/problem2_18101707.vwf"
	Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
	Info: Simulation partitioned into 1 sub-simulations
	Info: Simulation coverage is 100.00 %
	Info: Number of transitions in simulation is 513
	Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (6) | Processing (9) | Extra Info | Info (9) | Warning | Critical Warning | Error | Suppressed | Flag

Message: 0 of 16 | Location: | Locate

Messages

For Help, press F1 | Idle | NUM

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem2_18101707/problem2_18101707 - problem2_18101707 - [Simulation Report - Simulation Waveforms]

File Edit View Project Assignments Processing Tools Window Help

problem2_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Program

problem2_18101707.v | problem2_18101707.vwf | Simulation Report - Simulation Waveforms

- Simulation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
  - Simulator
    - Summary
    - Settings
    - Simulation Waveforms
    - Simulation Coverage
    - INI Usage
    - Messages

Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 30.05 ns | Pointer: 23.3 ns | Interval: -6.75 ns | Start: | End:

	Name
0	in
1	in[3]
2	in[2]
3	in[1]
4	in[0]
5	out
6	out[1]
7	out[0]

0 ps, 10.0 ns, 20.0 ns, 30.0 ns, 40.0 ns, 50.0 ns, 60.0 ns, 70.0 ns, 80.0 ns, 90.0 ns, 100.0 ns, 110.0 ns, 120.0 ns, 130.0 ns

30.05 ns

in: [14] [8] [2] [7] [12] [6] [3] [1] [11] [8] [3] [7] [15]

out: [3] [1] [0] [3] [1] [0] [3] [0] [3]

Type	Message
Info	Info: Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 1/problem2_18101707/problem2_18101707.vwf"
Info	Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Info: Simulation partitioned into 1 sub-simulations
Info	Info: Simulation coverage is 100.00 %
Info	Info: Number of transitions in simulation is 513
Info	Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (7) | Processing (9) | Extra Info | Info (9) | Warning | Critical Warning | Error | Suppressed | Flag

Message: 0 of 16 | Location: | Locate

For Help, press F1 | Idle | NUM

Problem no 2

Here, priority is $w[3] > w[0] > w[1] > w[2]$.

So, In my code firstly I checked if $w[3]$ bit is high or not if yes, then I assigned 11 to y. If no, then I checked does $w[0]$ is high or not. In this way I have checked the priority step by step and finally got my desired waveform.

Here, in the waveform we can see in first 10 ns, we getting 1110 = 14 as input so since $w[3] = 1$ so output is 11. And in 20-30 ns time frame input is 0010 so output is 01.

#18101707

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem3_18101707/problem3_18101707 - problem3_18101707 - [problem3_18101707.v]

File Edit View Project Assignments Processing Tools Window Help

problem3_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Program

problem3_18101707.v | Compilation Report - Flow Summary | problem3_18101707.vwf | Simulation Report - Simulation Waveforms

```
1  module problem3_18101707(i,z,selector);
2
3  input [8:0]i;
4  input [2:0]selector;
5
6  output reg z;
7
8  always@(i or selector)
9  begin
10
11 if (selector==0)
12     z=i[0];
13 else if(selector==1)
14     z=i[1];
15 else if(selector==2)
16     z=i[2];
17 else if(selector==3)
18     z=i[3];
19 else if(selector==4)
20     z=i[4];
21 else if(selector==5)
22     z=i[5];
23 else if(selector==6)
24     z=i[6];
25 else
26     z=i[7];
27
28 end
29
30
```

Type	Message
Info	Info: Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 1/problem3_18101707/problem3_18101707.vwf"
Info	Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Info: Simulation partitioned into 1 sub-simulations
Info	Info: Simulation coverage is 100.00 %
Info	Info: Number of transitions in simulation is 1559
Info	Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (11) | Processing (9) | Extra Info | Info (9) | Warning | Critical Warning | Error | Suppressed | Flag

Message: 0 of 16 | Location: | Locate

For Help, press F1 | Ln 26, Col 12 | Idle | NUM

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem3_18101707/problem3_18101707 - problem3_18101707 - [Compilation Report - Flow Summary]

File Edit View Project Assignments Processing Tools Window Help

problem3_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Program

problem3_18101707.v | Compilation Report - Flow Summary | problem3_18101707.vwf | Simulation Report - Simulation Waveforms

- Compilation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
  - Flow Non-Default Global Se
  - Flow Elapsed Time
  - Flow OS Summary
  - Flow Log
  - Analysis & Synthesis
  - Fitter
  - Assembler
  - Timing Analyzer
  - EDA Netlist Writer

Flow Summary

Flow Status	Successful - Mon Mar 22 15:32:16 2021
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	problem3_18101707
Top-level Entity Name	problem3_18101707
Family	FLEX10KE
Met timing requirements	Yes
Total logic elements	5 / 1,728 (< 1 %)
Total pins	13 / 102 (13 %)
Total memory bits	0 / 24,576 (0 %)
Total PLLs	0
Device	EPF10K30ETC144-1
Timing Models	Final

Type | Message

```
Info: Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 1/problem3_18101707/problem3_18101707.vwf"
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is      100.00 %
Info: Number of transitions in simulation is 1559
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
```

System (11) | Processing (9) | Extra Info | Info (9) | Warning | Critical Warning | Error | Suppressed | Flag

Message: 0 of 16 | Location: | Locate

Messages

For Help, press F1 | Idle | NUM

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem3_18101707/problem3_18101707 - problem3_18101707 - [Simulation Report - Simulation Waveforms]

File Edit View Project Assignments Processing Tools Window Help

problem3_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Program

problem3_18101707.v | Compilation Report - Flow Summary | problem3_18101707.vwf | **Simulation Report - Simulation Waveforms**

- Simulation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
  - Simulator
    - Summary
    - Settings
    - Simulation Waveforms
    - Simulation Coverage
    - INI Usage
    - Messages

Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 30.05 ns | Pointer: 2.66 ns | Interval: -27.39 ns | Start: | End:

	Name	0 ps	10.0 ns	20.0 ns	30.0 ns	40.0 ns	50.0 ns	60.0 ns	70.0 ns	80.0 ns	90.0 ns
					30.05 ns						
0	i	[1][167]	[0][20]	[0][238]	[0][139]	[1][239]	[0][7]	[0]&	[1][3]	[0][229]	[0][198]
1	i[8]										
2	i[7]										
3	i[6]										
4	i[5]										
5	i[4]										
6	i[3]										
7	i[2]										
8	i[1]										
9	i[0]										
10	selector	[0]	[3]	[1]	[4]	[1]	[4]	[1]	[5]	[1]	[3]
11	selector[2]										
12	selector[1]										
13	selector[0]										
14	z										

Type	Message
	Info: Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 1/problem3_18101707/problem3_18101707.vwf"
	Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
	Info: Simulation partitioned into 1 sub-simulations
	Info: Simulation coverage is 100.00 %
	Info: Number of transitions in simulation is 1559
	Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (11) | Processing (9) | Extra Info | Info (9) | Warning | Critical Warning | Error | Suppressed | Flag

Message: 0 of 16 | Location: | Locate

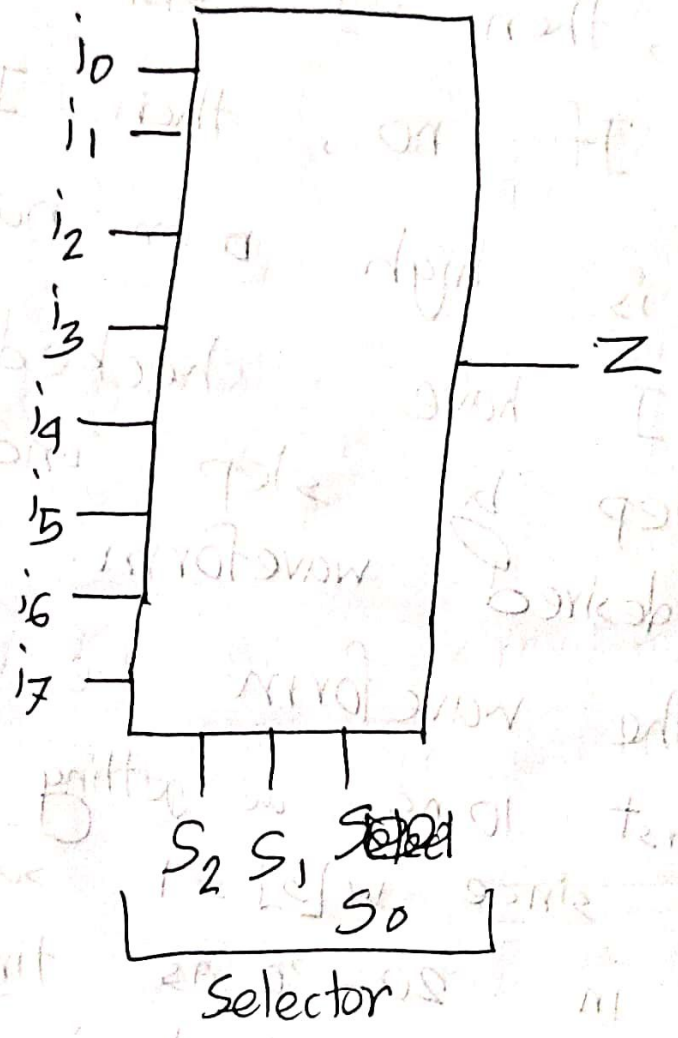
For Help, press F1 | Idle | NUM

#18101707

Problem no3

Here, I needed to design 8 to 1 Mux

Here is the block diggram.

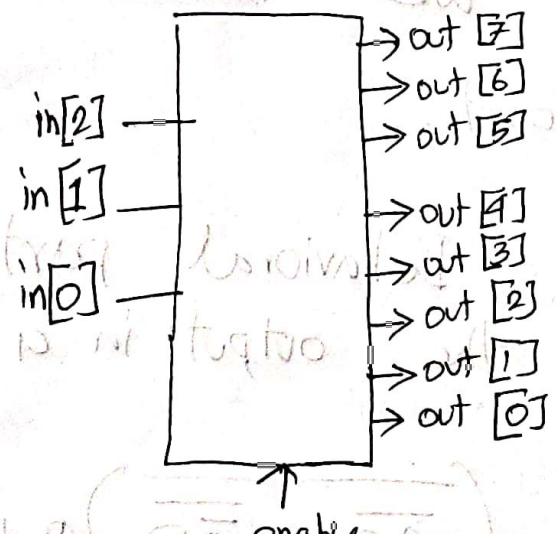


In the code, I have used conditional statement to check the value of the selectors and saved the value of I on Z, which is my output

If we look at the waveform, we see that, in first 10ns. selector is 0. so the value of i[0] which was 1, was re assigned to z.

Problem 4

Here, we need to design 3 to 8 Decoder.



there, in my code. I have used case statement to check my input; and then according to the input I have assigned the value to the corresponding output pin. Furthermore, there is also a enable pin to check if the decoder is on or not.

#18101707

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem4_18101707/problem4_18101707 - problem4_18101707 - [problem4_18101707.v]

File Edit View Project Assignments Processing Tools Window Help

problem4_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
  - Program Device (Open Program

problem4_18101707.v | problem4_18101707.vwf | Simulation Report - Simulation Waveforms

```
1  module problem4_18101707( in,out, enable);
2  input [2:0]in;
3  input enable;
4  output reg [7:0]out;
5
6
7   always @( in or enable)
8      begin
9
10       if (enable)
11         begin
12           out=8'd0;
13           case (in)
14               3'b000: out[0]=1'b1;
15               3'b001: out[1]=1'b1;
16               3'b010: out[2]=1'b1;
17               3'b011: out[3]=1'b1;
18               3'b100: out[4]=1'b1;
19               3'b101: out[5]=1'b1;
20               3'b110: out[6]=1'b1;
21               3'b111: out[7]=1'b1;
22               default: out=8'd0;
23           endcase
24       end
25 else
26 out=8'd0;
27 end
28 endmodule
```

Type	Message
i	Info: Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 1/problem4_18101707/problem4_18101707.vwf"
i	Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
i	Info: Simulation partitioned into 1 sub-simulations
i	Info: Simulation coverage is 96.43 %
i	Info: Number of transitions in simulation is 802
i	Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (5) | Processing (9) | Extra Info | Info (9) | Warning | Critical Warning | Error | Suppressed | Flag

Message: 0 of 16 Location: Locate

For Help, press F1 Ln 19, Col 35 Idle NUM

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem4_18101707/problem4_18101707 - problem4_18101707 - [Compilation Report - Flow Summary]

File Edit View Project Assignments Processing Tools Window Help

problem4_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Program

problem4_18101707.v | problem4_18101707.vwf | Simulation Report - Simulation Waveforms | **Compilation Report - Flow Summary**

- Compilation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
  - Flow Non-Default Global Se
  - Flow Elapsed Time
  - Flow OS Summary
  - Flow Log
  - Analysis & Synthesis
  - Fitter
  - Assembler
  - Timing Analyzer
  - EDA Netlist Writer

Flow Summary

Flow Status	Successful - Mon Mar 22 15:42:29 2021
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	problem4_18101707
Top-level Entity Name	problem4_18101707
Family	FLEX10KE
Met timing requirements	Yes
Total logic elements	8 / 1,728 (< 1 %)
Total pins	12 / 102 (12 %)
Total memory bits	0 / 24,576 (0 %)
Total PLLs	0
Device	EPF10K30ETC144-1
Timing Models	Final

Type | Message

```
Info: ******************************************************************
Info: Running Quartus II EDA Netlist Writer
Info: Command: quartus_eda --read_settings_files=off --write_settings_files=off problem4_18101707 -c problem4_18101707
Info: Generated files "problem4_18101707.vo" and "problem4_18101707_v.sdo" in directory "D:/COURSE/CSE460 LAB FILES/LAB 1/problem4_18101707/simulation/custom/" for EDA simulation tool
Info: Generated files "problem4_18101707.vo" and "problem4_18101707_v.sdo" in directory "D:/COURSE/CSE460 LAB FILES/LAB 1/problem4_18101707/timing/custom/" for EDA timing analysis tool
Info: Quartus II EDA Netlist Writer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 3 warnings
```

System (7) | **Processing (44)** | Extra Info | Info (41) | Warning (3) | Critical Warning | Error | Suppressed | Flag

Message: 0 of 87 | Location: | Locate

Messages

For Help, press F1 | Idle | NUM

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem4_18101707/problem4_18101707 - problem4_18101707 - [Simulation Report - Simulation Waveforms]

File Edit View Project Assignments Processing Tools Window Help

problem4_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Program

problem4_18101707.v | problem4_18101707.vwf | Simulation Report - Simulation Waveforms

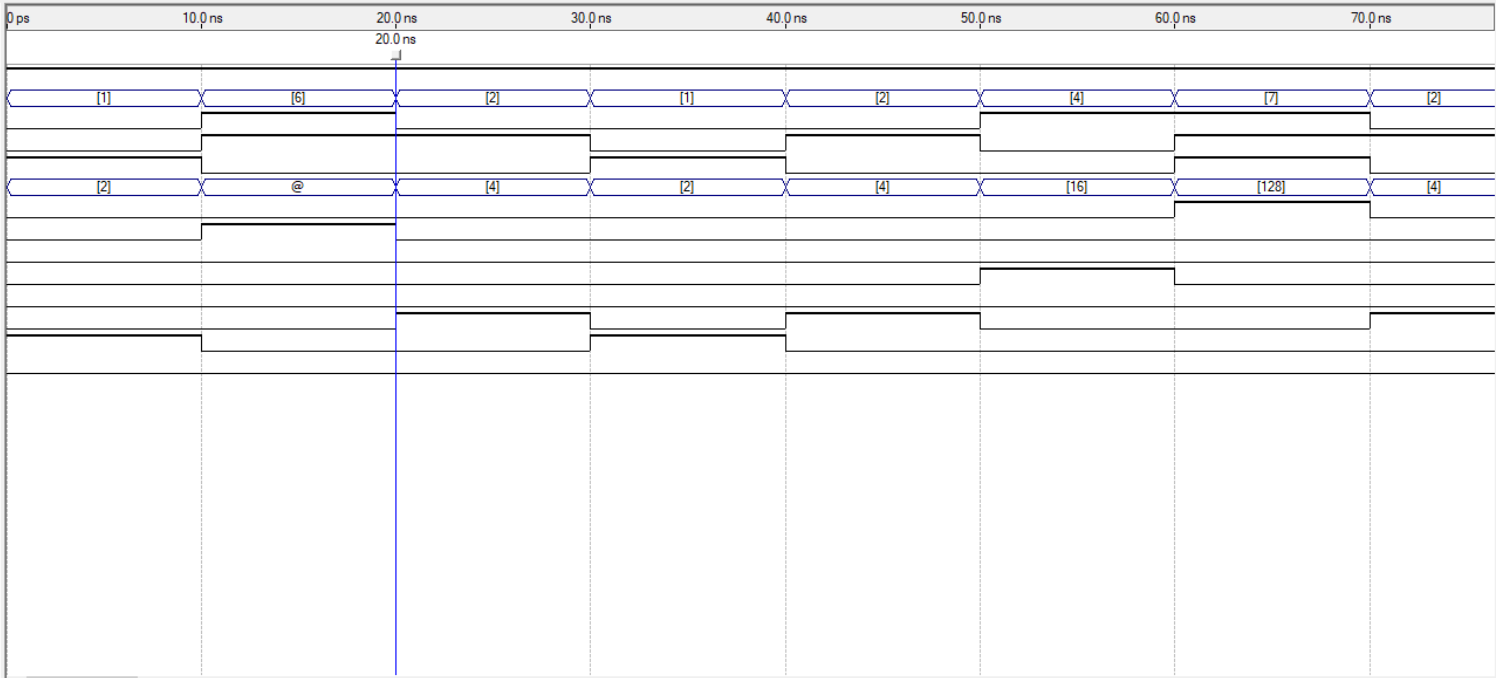
- Simulation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
- Simulator
  - Summary
  - Settings
  - Simulation Waveforms
  - Simulation Coverage
  - INI Usage
  - Messages

Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 20.0 ns | Pointer: 5.17 ns | Interval: -14.83 ns | Start: | End:

	Name
0	enable
1	in
2	in[2]
3	in[1]
4	in[0]
5	out
6	out[7]
7	out[6]
8	out[5]
9	out[4]
10	out[3]
11	out[2]
12	out[1]
13	out[0]



Type	Message
	Info: Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 1/problem4_18101707/problem4_18101707.vwf"
	Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
	Info: Simulation partitioned into 1 sub-simulations
	Info: Simulation coverage is 96.43 %
	Info: Number of transitions in simulation is 802
	Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (5) | Processing (9) | Extra Info | Info (9) | Warning | Critical Warning | Error | Suppressed | Flag

Message: 0 of 16 | Location: | Locate

For Help, press F1 | Idle | NUM

#1810707

Problem 5

Here first in structural circuit.

I generated a output of every gate and the finally I got my desire output.

As we seeing in code every gate has it's operation then gradually we reached to the output point.

However, in Behavioral part, we assigned the output in a sing line.

$$Q = \overline{\left(\overline{A.B} + \overline{\overline{C}D}\right)}.E$$

$$X = \left(\overline{A}B + \overline{\overline{C}D}\right).E$$

and Finally, I assigned same input wave in both files to check

If the output was generating the same waveform or not.

Since it matches so we can say our code is correct.

#18101707

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem5_18101707/problem5_18101707 - problem5_18101707 - [Compilation Report - Flow Summary]

File Edit View Project Assignments Processing Tools Window Help

problem5_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Program

problem5_18101707.v | problem5_18101707.vwf | Simulation Report - Simulation Waveforms | **Compilation Report - Flow Summary**

- Compilation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
  - Flow Non-Default Global Se
  - Flow Elapsed Time
  - Flow OS Summary
  - Flow Log
  - Analysis & Synthesis
  - Fitter
  - Assembler
  - Timing Analyzer
  - EDA Netlist Writer

Flow Summary

Flow Status	Successful - Mon Mar 22 16:06:52 2021
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	problem5_18101707
Top-level Entity Name	problem5_18101707
Family	FLEX10KE
Met timing requirements	Yes
Total logic elements	3 / 1,728 (< 1 %)
Total pins	7 / 102 (7 %)
Total memory bits	0 / 24,576 (0 %)
Total PLLs	0
Device	EPF10K30ETC144-1
Timing Models	Final

Type | Message

```
Info: ******************************************************************
Info: Running Quartus II EDA Netlist Writer
Info: Command: quartus_eda --read_settings_files=off --write_settings_files=off problem5_18101707 -c problem5_18101707
Info: Generated files "problem5_18101707.vo" and "problem5_18101707_v.sdo" in directory "D:/COURSE/CSE460 LAB FILES/LAB 1/problem5_18101707/simulation/custom/" for EDA simulation tool
Info: Generated files "problem5_18101707.vo" and "problem5_18101707_v.sdo" in directory "D:/COURSE/CSE460 LAB FILES/LAB 1/problem5_18101707/timing/custom/" for EDA timing analysis tool
Info: Quartus II EDA Netlist Writer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 6 warnings
```

System (7) | **Processing (47)** | Extra Info | Info (41) | Warning (6) | Critical Warning | Error | Suppressed | Flag

Message: 0 of 91 | Location: | Locate

Messages

For Help, press F1 | Idle | NUM

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem5_18101707/problem5_18101707 - problem5_18101707 - [Simulation Report - Simulation Waveforms]

File Edit View Project Assignments Processing Tools Window Help

problem5_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Program

problem5_18101707.v | problem5_18101707.vwf | Simulation Report - Simulation Waveforms

- Simulation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
  - Simulator
    - Summary
    - Settings
    - Simulation Waveforms
    - Simulation Coverage
    - INI Usage
    - Messages

Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 30.05 ns | Pointer: 7.27 ns | Interval: -22.78 ns | Start: | End:

	Name	Value at 30.05 ns
0	A	A 1
1	B	A 0
2	C	A 0
3	D	A 0
4	E	A 1
5	Q	A 0
6	X	A 1

0 ps | 10.0 ns | 20.0 ns | 30.0 ns | 40.0 ns | 50.0 ns | 60.0 ns

30.05 ns

Type	Message
Info	Info: Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 1/problem5_18101707/problem5_18101707.vwf"
Info	Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Info: Simulation partitioned into 1 sub-simulations
Info	Info: Simulation coverage is 58.33 %
Info	Info: Number of transitions in simulation is 1789
Info	Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (5) | Processing (9) | Extra Info | Info (9) | Warning | Critical Warning | Error | Suppressed | Flag

Message: 0 of 16 | Location: | Locate

Messages

For Help, press F1 | Idle | NUM

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem5_18101707/problem5_18101707 - problem5_18101707 - [problem5_18101707.v]

File Edit View Project Assignments Processing Tools Window Help

problem5_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Program

problem5_18101707.v | problem5_18101707.vwf | Simulation Report - Simulation Waveforms

```
1  module problem5_18101707(A,B,C,D,E,Q,X);
2
3  input A,B,C,D,E;
4  output Q,X;
5
6  nand(F,A,B);
7  nand(H,~C,D);
8  nor(I,F,H);
9  and(Q,I,E);
10 and(X,~I,E);
11
12 endmodule
13
```

Type	Message
Info	Info: Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 1/problem5_18101707/problem5_18101707.vwf"
Info	Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Info: Simulation partitioned into 1 sub-simulations
Info	Info: Simulation coverage is 58.33 %
Info	Info: Number of transitions in simulation is 1789
Info	Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (5) | Processing (9) | Extra Info | Info (9) | Warning | Critical Warning | Error | Suppressed | Flag

Message: 0 of 16 | Location: | Locate

Messages

For Help, press F1 | Ln 1, Col 1 | Idle | NUM

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem5b_18101707/problem5b_18101707 - problem5b_18101707 - [Compilation Report - Flow Summary]

File Edit View Project Assignments Processing Tools Window Help

problem5b_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Program

problem5b_18101707.v | problem5b_18101707.vwf | Compilation Report - Flow Summary | Simulation Report - Simulation Waveforms

Compilation Report

- Legal Notice
- Flow Summary
- Flow Settings
- Flow Non-Default Global Se
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Assembler
- Timing Analyzer
- EDA Netlist Writer

Flow Summary

Flow Status	Successful - Mon Mar 22 16:11:26 2021
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	problem5b_18101707
Top-level Entity Name	problem5b_18101707
Family	FLEX10KE
Met timing requirements	Yes
Total logic elements	3 / 1,728 (< 1 %)
Total pins	7 / 102 (7 %)
Total memory bits	0 / 24,576 (0 %)
Total PLLs	0
Device	EPF10K30ETC144-1
Timing Models	Final

Type | Message

```
Info: ******************************************************************
Info: Running Quartus II EDA Netlist Writer
Info: Command: quartus_eda --read_settings_files=off --write_settings_files=off problem5b_18101707 -c problem5b_18101707
Info: Generated files "problem5b_18101707.vo" and "problem5b_18101707_v.sdo" in directory "D:/COURSE/CSE460 LAB FILES/LAB 1/problem5b_18101707/simulation/custom/" for EDA simulation tool
Info: Generated files "problem5b_18101707.vo" and "problem5b_18101707_v.sdo" in directory "D:/COURSE/CSE460 LAB FILES/LAB 1/problem5b_18101707/timing/custom/" for EDA timing analysis tool
Info: Quartus II EDA Netlist Writer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 3 warnings
```

System (9) | Processing (44) | Extra Info | Info (41) | Warning (3) | Critical Warning | Error | Suppressed | Flag

Message: 0 of 88 | Location: | Locate

For Help, press F1 | Idle | NUM

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem5b_18101707/problem5b_18101707 - problem5b_18101707 - [Simulation Report - Simulation Waveforms]

File Edit View Project Assignments Processing Tools Window Help

problem5b_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Program

problem5b_18101707.v | problem5b_18101707.vwf | Compilation Report - Flow Summary | **Simulation Report - Simulation Waveforms**

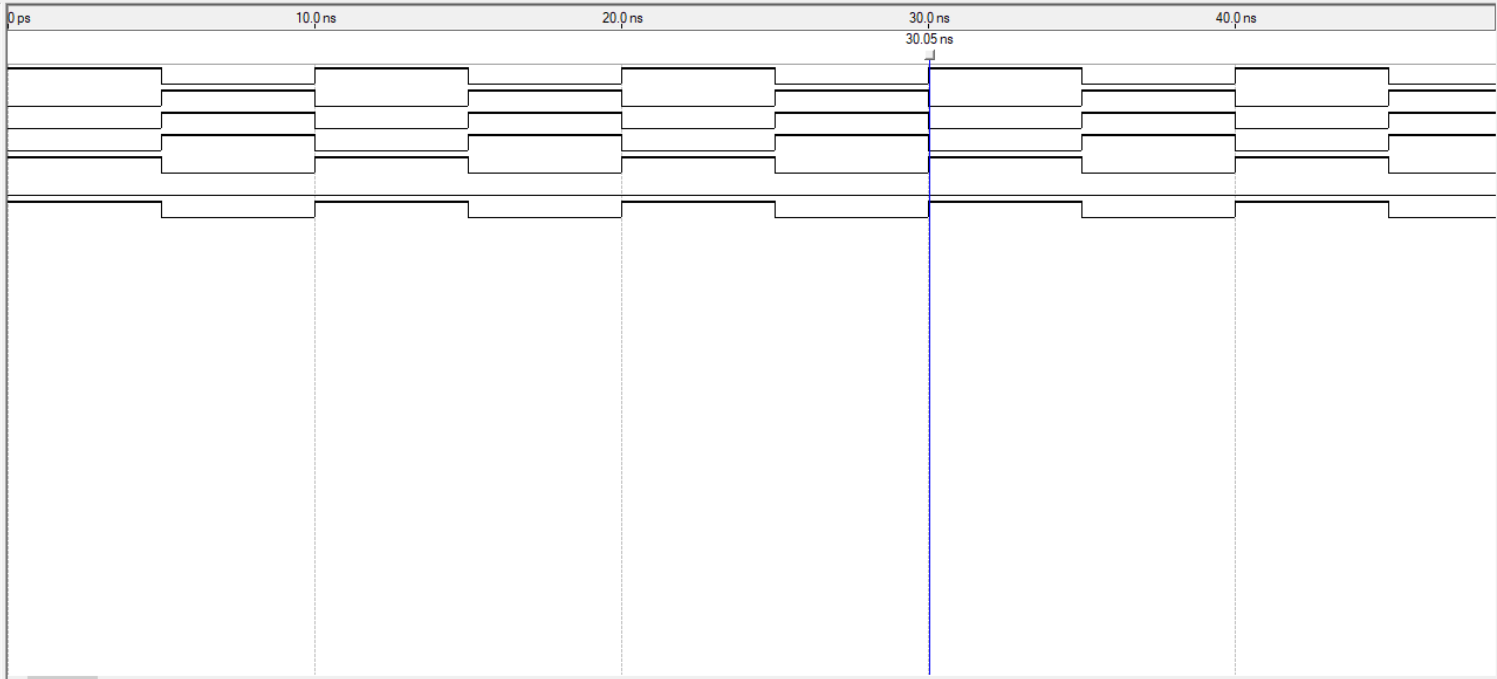
- Simulation Report
  - Legal Notice
  - Flow Summary
  - Flow Settings
  - Simulator
    - Summary
    - Settings
    - Simulation Waveforms
    - Simulation Coverage
    - INI Usage
    - Messages

Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 30.05 ns | Pointer: 228 ps | Interval: -29.82 ns | Start: | End:

	Name	Value at 30.05 ns
0	A	A 1
1	B	A 0
2	C	A 0
3	D	A 0
4	E	A 1
5	Q	A 0
6	X	A 1



Type	Message
Info	**********
Info	Running Quartus II EDA Netlist Writer
Info	Command: quartus_eda --read_settings_files=off --write_settings_files=off problem5b_18101707 -c problem5b_18101707
Info	Generated files "problem5b_18101707.vo" and "problem5b_18101707_v.sdo" in directory "D:/COURSE/CSE460 LAB FILES/LAB 1/problem5b_18101707/simulation/custom/" for EDA simulation tool
Info	Generated files "problem5b_18101707.vo" and "problem5b_18101707_v.sdo" in directory "D:/COURSE/CSE460 LAB FILES/LAB 1/problem5b_18101707/timing/custom/" for EDA timing analysis tool
Info	Quartus II EDA Netlist Writer was successful. 0 errors, 0 warnings
Info	Quartus II Full Compilation was successful. 0 errors, 3 warnings

System (9) | **Processing (44)** | Extra Info | Info (41) | Warning (3) | Critical Warning | Error | Suppressed | Flag

Message: 0 of 88 | Location: | Locate

For Help, press F1 | Idle | NUM

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 1/problem5b_18101707/problem5b_18101707 - problem5b_18101707 - [problem5b_18101707.v]

File Edit View Project Assignments Processing Tools Window Help

problem5b_18101707

Tasks

Flow: Compilation

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate progra
  - Classic Timing Analysis
  - EDA Netlist Writer
- Program Device (Open Program

problem5b_18101707.v | problem5b_18101707.vwf | Compilation Report - Flow Summary | Simulation Report - Simulation Waveforms

```
1  module problem5b_18101707(A,B,C,D,E,Q,X);
2
3  input A,B,C,D,E;
4  output Q,X;
5  assign Q = ( ~(~(A & B) |  ~(~C & D)) & E );
6  assign X = (  (~(A & B) |  ~(~C & D)) & E );
7
8  endmodule
9
```

Type	Message
Info:	**********
Info:	Running Quartus II EDA Netlist Writer
Info:	Command: quartus_eda --read_settings_files=off --write_settings_files=off problem5b_18101707 -c problem5b_18101707
Info:	Generated files "problem5b_18101707.vo" and "problem5b_18101707_v.sdo" in directory "D:/COURSE/CSE460 LAB FILES/LAB 1/problem5b_18101707/simulation/custom/" for EDA simulation tool
Info:	Generated files "problem5b_18101707.vo" and "problem5b_18101707_v.sdo" in directory "D:/COURSE/CSE460 LAB FILES/LAB 1/problem5b_18101707/timing/custom/" for EDA timing analysis tool
Info:	Quartus II EDA Netlist Writer was successful. 0 errors, 0 warnings
Info:	Quartus II Full Compilation was successful. 0 errors, 3 warnings

System (9) | Processing (44) | Extra Info | Info (41) | Warning (3) | Critical Warning | Error | Suppressed | Flag

Message: 0 of 88 | Location: | Locate

For Help, press F1 | Ln 1, Col 1 | Idle | NUM