



Inspiring Excellence

LAB ASSIGNMENT 2

CSE460: VLSI Design

Submitted By

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18101707

Section: 03

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 2/problem1_18101707/problem1_18101707 - [problem1_18101707.v]

File Edit View Project Assignments Processing Tools Window Help

problem1_18101707

Tasks Flow: Compilation

problem1_18101707.v | Compilation Report - Flow Summary | problem1_18101707.vwf | Simulation Report - Simulation Waveforms

Task List

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Classic Timing Analysis
- EDA Netlist Writer

Program Device (Open Program)

```
1 module problem1_18101707(d,load,clk,q);
2   input [3:0]d;
3   input load,clk;
4   output reg[3:0]q;
5   always @(negedge clk)
6     if (load)
7       q<=d;
8     else
9       //q[3:0]<={q[0],q[3:1]};
10      begin
11        q[2]<=q[3];
12        q[1]<=q[2];
13        q[0]<=q[1];
14        q[3]=1'b0;
15      end
16    endmodule
17
18
19
```

Type	Message
Info	Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 2/problem1_18101707/problem1_18101707.v"
Info	Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Simulation partitioned into 1 sub-simulations
Info	Simulation coverage is 66.67 %
Info	Number of transitions in simulation is 228
Info	Quartus II Simulator was successful. 0 errors, 0 warnings

Messages

System (6) | Processing (9) | Extra Info (9) | Info (9) | Warning | Critical Warning | Error | Suppressed | Flag |

Message: 0 of 16

For Help, press F1

Ln 8, Col 9 | Locate | NUM

Tasks
Flow: Compilation

problem1_18101707.v

Compilation Report - Flow Summary

problem1_18101707.vwf

Simulation Report - Simulation Waveforms

- Task Flow: Compilation
- ✓ ▶ Compile Design
 - ✓ ▶ Analysis & Synthesis
 - ✓ ▶ Fitter (Place & Route)
 - ✓ ▶ Assembler (Generate program)
 - ✓ ▶ Classic Timing Analysis
 - ✓ ▶ EDA Netlist Writer
- Program Device (Open Program)
- ✓ Compilation Report
 - Legal Notice
 - Flow Summary
 - Flow Settings
 - Flow Non-Default Global Settings
 - Flow Elapsed Time
 - Flow OS Summary
 - Flow Log
 - Analysis & Synthesis
 - Fitter
 - Assembler
 - Timing Analyzer
 - EDA Netlist Writer

Flow Summary

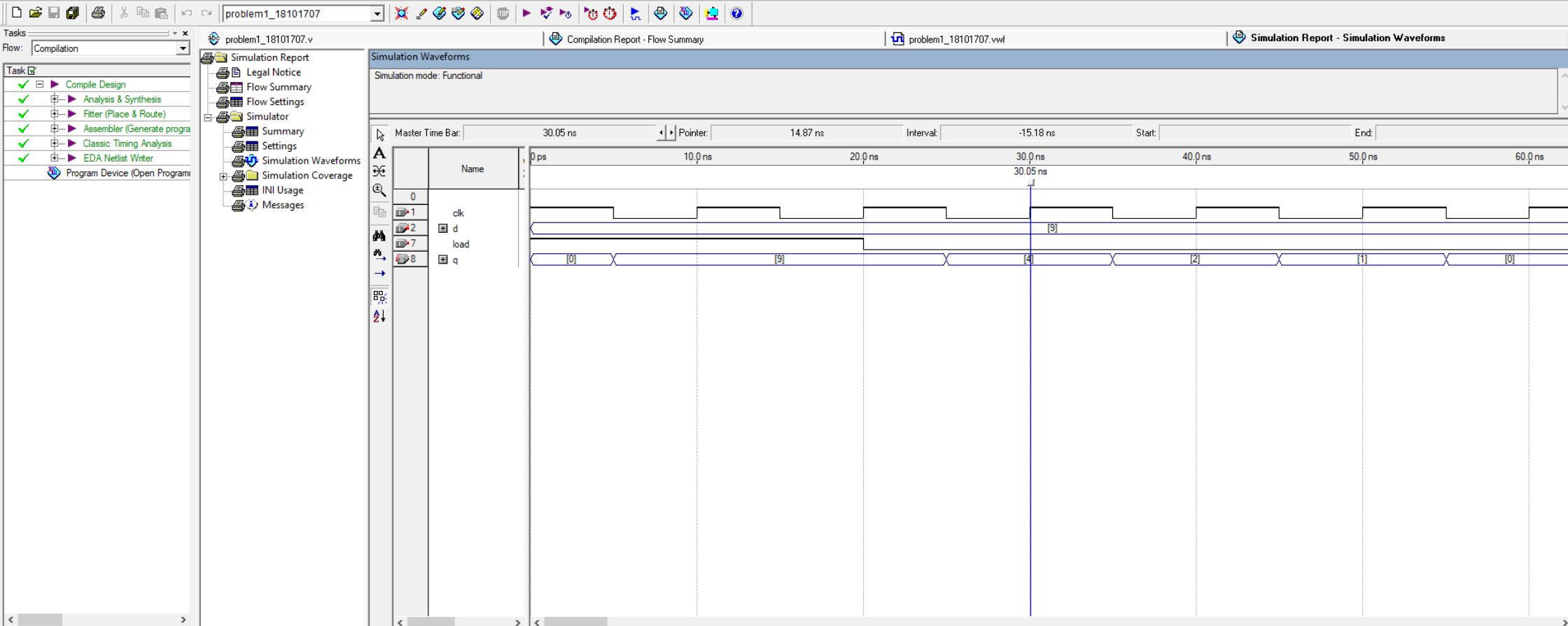
Flow Status Successful - Tue Mar 23 11:26:10 2021
Quartus II Version 8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name problem1_18101707
Top-level Entity Name problem1_18101707
Family FLEX10KE
Met timing requirements Yes
Total logic elements 4 / 1,728 (< 1 %)
Total pins 10 / 102 (10 %)
Total memory bits 0 / 24,576 (0 %)
Total PLLs 0
Device EPF10K30ETC144-1
Timing Models Final

Type	Message
Info	Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 2/problem1_18101707/problem1_18101707.vwf"
Info	Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Simulation partitioned into 1 sub-simulations
Info	Simulation coverage is 66.67 %
Info	Number of transitions in simulation is 228
Info	Quartus II Simulator was successful. 0 errors, 0 warnings

Messages System (6) Processing (9) Extra Info (9) Info (9) Warning Critical Warning Error Suppressed Flag /

Message: 0 of 16

Locate



Type	Message
Info	Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 2/problem1_18101707/problem1_18101707.vwf"
Info	Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Simulation partitioned into 1 sub-simulations
Info	Simulation coverage is 66.67 %
Info	Number of transitions in simulation is 228
Info	Quartus II Simulator was successful. 0 errors, 0 warnings

System (6) Processing (9) Extra Info (9) Info (9) Warning Critical Warning Error Suppressed Flag /

Messages: 0 of 16

Locate

problem no 1

(i) Here, I have to do a logical right shift. So, if I input 9 (1001).

after first shift I would get 0100 (4). Accordingly,

In third shift, 0010 (2)

" forth " , 0001 (1)

" last " , 0000 (0)

Here, in my code I have assigned my input $q[3]$ value to $q[2]$, then $q[2]$ to $q[1]$ and $q[1]$ to $q[0]$. Lastly, I have assigned 0 in the MSB.

If we see the waveform file we can see our output is perfect.

(ii) we have used non-blocking statement in problem one since it does not register until after the always block has executed.

If we used ~~non~~ blocking statement here, our value would have been updated immediately that would result in a loss of information to tackle this. So we must ~~use~~ save ~~the~~ information to use temp variable to the information before assignment which is not ideal.

That's why it is efficient to use non-blocking statements here.

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 2/problem2_18101707/problem2_18101707 - [problem2_18101707.v]

File Edit View Project Assignments Processing Tools Window Help

problem2_18101707

Tasks Flow: Compilation

problem2_18101707.v | Compilation Report - Flow Summary | problem2_18101707.vwf | Simulation Report - Simulation Waveforms

Task List

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Classic Timing Analysis
- EDA Netlist Writer

Program Device (Open Program)

```
1 module problem2_18101707(d,load,clk,q);
2   input [3:0]d;
3   input load,clk;
4   output reg[3:0]q;
5   always @(posedge clk)
6     if (load)
7       q<=d;
8     else
9       //q[3:0]<={q[0],q[3:1]};
10      begin
11        q[0]<=q[3];
12        q[3]<=q[2];
13        q[2]<=q[1];
14        q[1]<=q[0];
15      end
16    endmodule
17
18
19
```

Type	Message
Warning	Warning: Found clock-sensitive change during active clock edge at time 20.0 ns on register " problem2_18101707 q[1]~reg0"
Warning	Warning: Found clock-sensitive change during active clock edge at time 20.0 ns on register " problem2_18101707 q[3]~reg0"
Info	Info: Simulation partitioned into 1 sub-simulations
Info	Info: Simulation coverage is 72.22 %
Info	Info: Number of transitions in simulation is 794
Info	Info: Quartus II Simulator was successful. 0 errors, 2 warnings

Messages: System (6) | Processing (11) | Extra Info (9) | Info (9) | Warning (2) | Critical/Warning | Error | Suppressed | Flag /

Message: 0 of 18

For Help, press F1

Ln 1, Col 1 | Idle | NUM



Tasks

Flow: Compilation

problem2_18101707.v

Compilation Report - Flow Summary

problem2_18101707.vwf

Simulation Report - Simulation Waveforms

Task Compile Design

✓ Analysis & Synthesis

✓ Fitter (Place & Route)

✓ Assembler (Generate program)

✓ Classic Timing Analysis

✓ EDA Netlist Writer

Program Device (Open Program)

Compilation Report

- Legal Notice
- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Assembler
- Timing Analyzer
- EDA Netlist Writer

Flow Summary

Flow Status: Successful - Tue Mar 23 10:01:49 2021

Quartus II Version: 8.1 Build 163 10/28/2008 SJ Web Edition

Revision Name: problem2_18101707

Top-level Entity Name: problem2_18101707

Family: FLEX10KE

Met timing requirements: Yes

Total logic elements: 4 / 1,728 (< 1 %)

Total pins: 10 / 102 (10 %)

Total memory bits: 0 / 24,576 (0 %)

Total PLLs: 0

Device: EPF10K30ETC144-1

Timing Models: Final

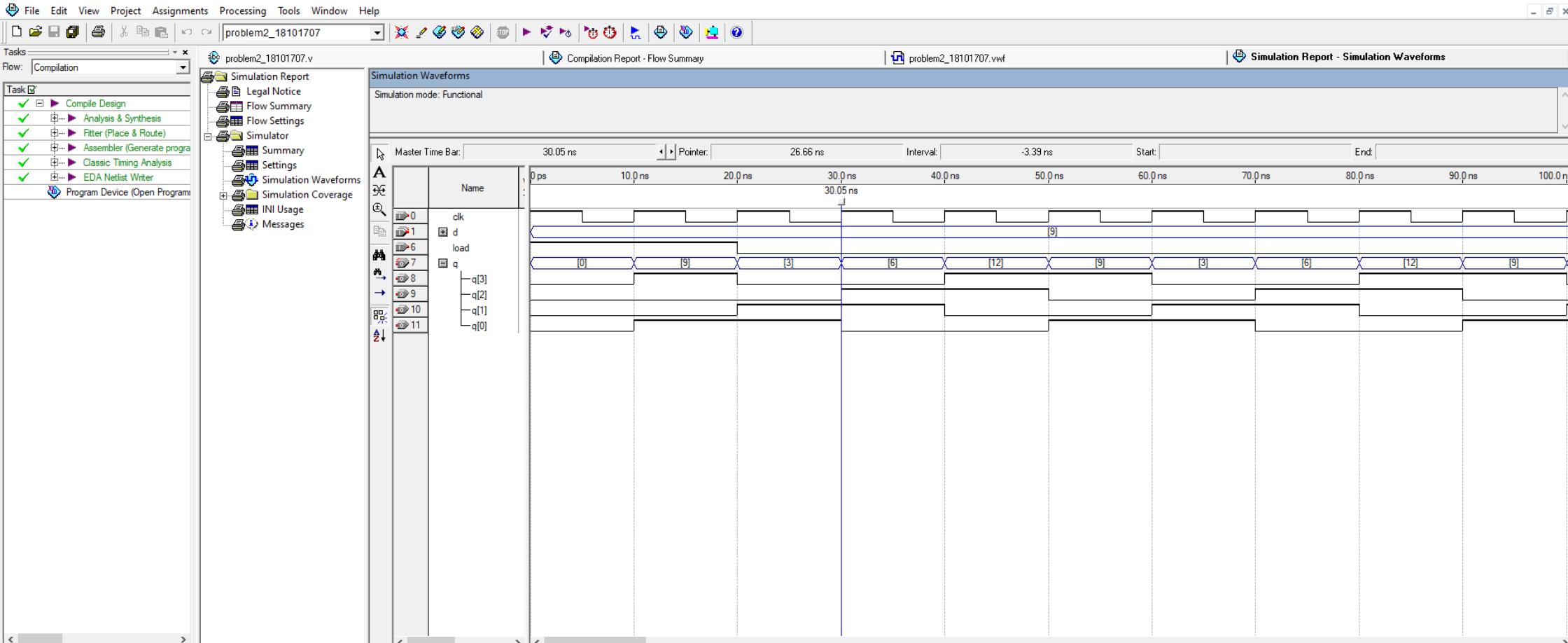
Type	Message
Warning	Warning: Found clock-sensitive change during active clock edge at time 20.0 ns on register " problem2_18101707 q[1]~reg0"
Warning	Warning: Found clock-sensitive change during active clock edge at time 20.0 ns on register " problem2_18101707 q[3]~reg0"
Info	Info: Simulation partitioned into 1 sub-simulations
Info	Info: Simulation coverage is 72.22 %
Info	Info: Number of transitions in simulation is 794
Info	Info: Quartus II Simulator was successful. 0 errors, 2 warnings

System (6) Processing (11) Extra Info (9) Warning (2) Critical/Warning Error Suppressed Flag /

Messages
Message: 0 of 18

For Help, press F1

Locate NUM



Type	Message
Warning	Warning: Found clock-sensitive change during active clock edge at time 20.0 ns on register "problem2_18101707 q[1]-reg0"
Warning	Warning: Found clock-sensitive change during active clock edge at time 20.0 ns on register "problem2_18101707 q[3]-reg0"
Info	Info: Simulation partitioned into 1 sub-simulations
Info	Info: Simulation coverage is 72.22 %
Info	Info: Number of transitions in simulation is 794
Info	Info: Quartus II Simulator was successful. 0 errors, 2 warnings

Messages

System (6) Processing (11) Extra Info (9) Info (2) Warning (2) Critical Warning Error Suppressed Flag /

Message: 0 of 18

Locate

For Help, press F1

Idle NUM

Problem 2



#18101707

Here, I was to do a circular left shift. ~~here~~, so, If I input (1001) 9 as a input.

1st shift = 00111(3)
2nd " = 0110 (6) repeat
3rd " = 1100 (12)
4th " = 1001 (9)

So, I have used non-blocking statements to assign the values of the output bits. Finally, looking at the waveform file I can say it is working perfectly.

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 2/problem3_18101707/problem3_18101707 - [problem3_18101707.v]

File Edit View Project Assignments Processing Tool Window Help

problem3_18101707

Tasks Flow: Compilation

problem3_18101707.v | Compilation Report - Flow Summary | problem3_18101707.vwf | Simulation Report - Simulation Waveforms

Task List

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Classic Timing Analysis
- EDA Nelist Writer

Program Device (Open Program)

```
1 module problem3_18101707(Clk,reset,Count);
2
3     //input ports and their sizes
4     input Clk,reset;
5     //output ports and their size
6     output [3 : 0] Count;
7     //Internal variables
8     reg [3 : 0] Count = 1;
9
10    always @ (posedge(Clk) or posedge(reset))
11        begin
12            if(reset == 1)
13                Count <= 1;
14            else
15
16                if(Count == 9)
17                    Count <= 1;
18                else
19
20                    Count <= Count + 2; //Increment Counter
21
22        end
23
24    endmodule
25
```

Type	Message
Info	Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 2/problem3_18101707/problem3_18101707.vwf"
Info	Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Simulation partitioned into 1 sub-simulations
Info	Simulation coverage is 77.27 %
Info	Number of transitions in simulation is 2628
Info	Quartus II Simulator was successful. 0 errors, 0 warnings

System (12) | Processing (9) | Extra Info (9) | Info (9) | Warning | Critical Warning | Error | Suppressed | Flag /

Messages: 0 of 16

For Help, press F1

Ln 25, Col 1

Idle

NUM

File Edit View Project Assignments Processing Tools Window Help

problem3_18101707

Tasks

Flow: Compilation

Task List

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Classic Timing Analysis
- EDA Netlist Writer

Program Device (Open Program)

problem3_18101707.v

Compilation Report - Flow Summary

problem3_18101707.vwf

Simulation Report - Simulation Waveforms

Flow Summary

Flow Status: Successful - Mon Mar 22 23:18:05 2021

Quartus II Version: 8.1 Build 163 10/28/2008 SJ Web Edition

Revision Name: problem3_18101707

Top-level Entity Name: problem3_18101707

Family: FLEX10KE

Met timing requirements: Yes

Total logic elements: 3 / 1,728 (< 1 %)

Total pins: 6 / 102 (6 %)

Total memory bits: 0 / 24,576 (0 %)

Total PLLs: 0

Device: EPF10K30ETC144-1

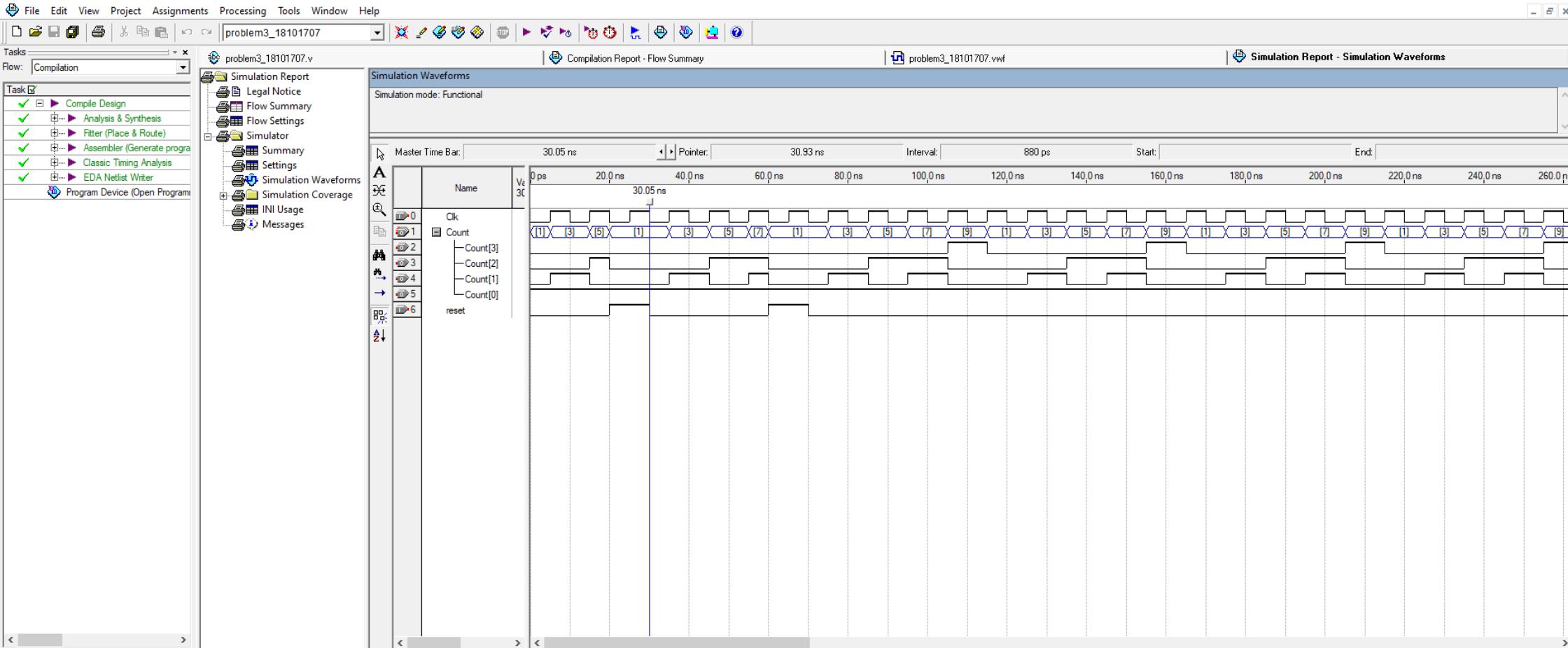
Timing Models: Final

Type	Message
Info	Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 2/problem3_18101707/problem3_18101707.vwf"
Info	Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Simulation partitioned into 1 sub-simulations
Info	Simulation coverage is 77.27 %
Info	Number of transitions in simulation is 2628
Info	Quartus II Simulator was successful. 0 errors, 0 warnings

System (12) Processing (9) Extra Info (9) Info (9) Warning Critical Warning Error Suppressed Flag /

Messages: 0 of 16

Locate



Type	Message
Info	Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 2/problem3_18101707/problem3_18101707.vwf"
Info	Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Info: Simulation partitioned into 1 sub-simulations
Info	Info: Simulation coverage is 77.27 %
Info	Info: Number of transitions in simulation is 2628
Info	Info: Quartus II Simulator was successful. 0 errors, 0 warnings

System (12) Processing (9) Extra Info (9) Info (9) Warning Critical Warning Error Suppressed Flag /

Messages

For Help, press F1

Idle NUM

Problem 3

Here, I have to design a odd up counter with a reset button. So, if reset button is disabled, our output would be 1, 3, 5, 7, 9, 1, 3, 5, 7, 9.

If Reset button is enabled, the value would start from 1.

Since it is to add up counter we would check if reset is on or off. If not, value would be 1. If not, 3 or not. It would increment 2.

If not, it would be 3. As we need only odd number. If the output is 0, and it would stop for assigned 1. In this way, we have achieved our desired output.

We can see the waveform picture to ensure that.

Tasks
Flow: Compilation

problem4_18101707.v

problem4_18101707.wrf

Compilation Report - Flow Summary

```
1 module problem4_18101707(x,sel,y);
2
3   input [0:15]x;
4   input [3:0]sel;
5   output reg y;
6
7   always @(x,sel)
8
9     case(sel)
10
11       4'b0000: y= x[0];
12       4'b0001: y= x[1];
13       4'b0010: y= x[2];
14       4'b0011: y= x[3];
15       4'b0100: y= x[4];
16       4'b0101: y= x[5];
17       4'b0110: y= x[6];
18       4'b0111: y= x[7];
19       4'b1000: y= x[8];
20       4'b1001: y= x[9];
21       4'b1010: y= x[10];
22       4'b1011: y= x[11];
23       4'b1100: y= x[12];
24       4'b1101: y= x[13];
25       4'b1110: y= x[14];
26       4'b1111: y= x[15];
27
28   endcase
29
30 endmodule
31
```

Type	Message
Info:	*****
Info:	Running Quartus II EDA Netlist Writer
Info:	Command: quartus_edt --read_settings_files=off --write_settings_files=off problem4_18101707 -c problem4_18101707
Info:	Generated files "problem4_18101707.vo" and "problem4_18101707.vsd" in directory "D:/COURSE/CSE460 LAB FILES/LAB 2/problem4_18101707/simulation/custom/" for EDA simulation tool
Info:	Generated files "problem4_18101707.vo" and "problem4_18101707.vsd" in directory "D:/COURSE/CSE460 LAB FILES/LAB 2/problem4_18101707/timing/custom/" for EDA timing analysis tool
Info:	Quartus II EDA Netlist Writer was successful. 0 errors, 0 warnings
Info:	Quartus II Full Compilation was successful. 0 errors, 3 warnings

Messages System (2) Processing (44) Extra Info (41) Info (41) Warning (3) Critical/Warning Error Suppressed Flag /

Message: 83 of 90

Locate

File Edit View Project Assignments Processing Tools Window Help

problem4_18101707

Tasks

Flow: Compilation

Task Compile Design

✓ Analysis & Synthesis

✓ Fitter (Place & Route)

✓ Assembler (Generate program)

✓ Classic Timing Analysis

✓ EDA Netlist Writer

Program Device (Open Program)

Compilation Report

- Legal Notice
- Flow Summary
- Flow Settings
- Flow Non-Default Global Settings
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Assembler
- Timing Analyzer
- EDA Netlist Writer

Compilation Report - Flow Summary

Flow Summary

Flow Status	Successful - Tue Mar 23 12:56:20 2021
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	problem4_18101707
Top-level Entity Name	problem4_18101707
Family	FLEX10KE
Met timing requirements	Yes
Total logic elements	10 / 1,728 (< 1 %)
Total pins	21 / 102 (21 %)
Total memory bits	0 / 24,576 (0 %)
Total PLLs	0
Device	EPF10K30ETC144-1
Timing Models	Final

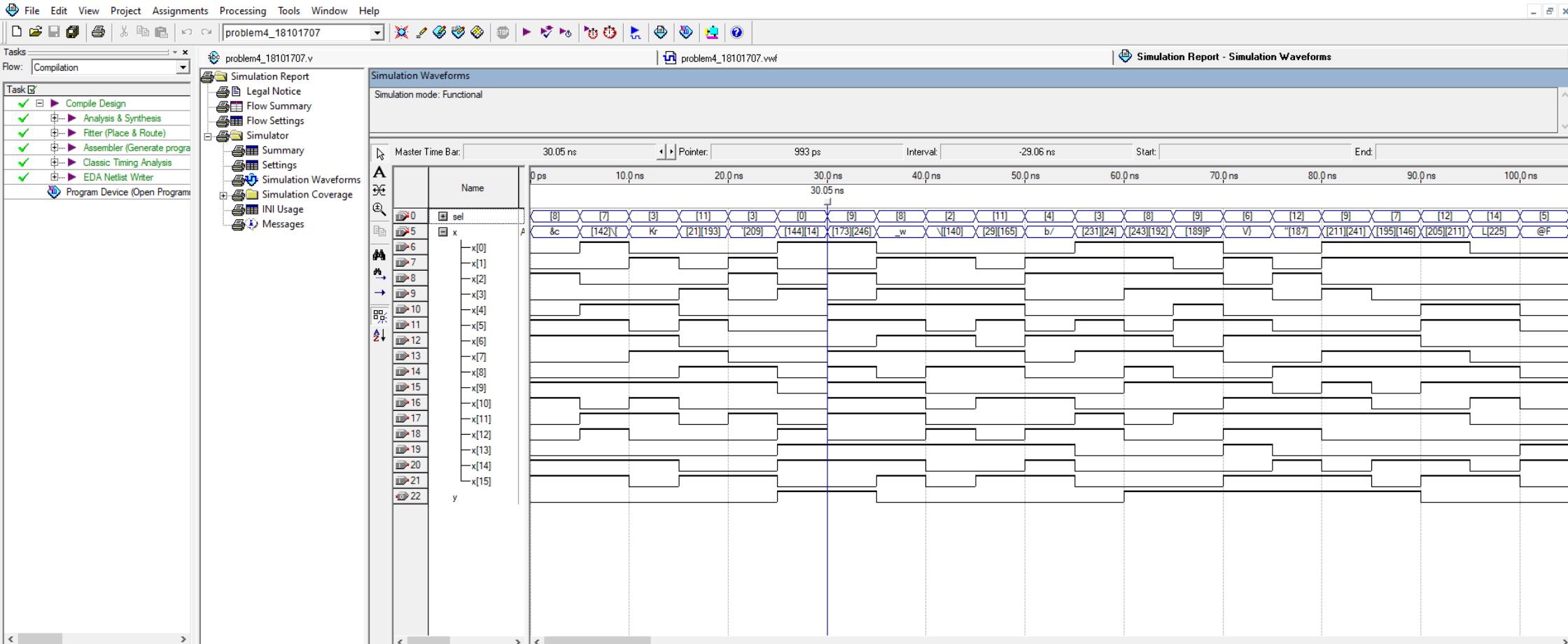
Messages

Type	Message
Info	*****
Info	Running Quartus II EDA Netlist Writer
Info	Info: Command: quartus_edt --read_settings_files=off --write_settings_files=off problem4_18101707 -c problem4_18101707
Info	Info: Generated files "problem4_18101707.vo" and "problem4_18101707_v.sdo" in directory "D:/COURSE/CSE460 LAB FILES/LAB 2/problem4_18101707/simulation/custom/" for EDA simulation tool
Info	Info: Generated files "problem4_18101707.vo" and "problem4_18101707_v.sdo" in directory "D:/COURSE/CSE460 LAB FILES/LAB 2/problem4_18101707/timing/custom/" for EDA timing analysis tool
Info	Info: Quartus II EDA Netlist Writer was successful. 0 errors, 0 warnings
Info	Info: Quartus II Full Compilation was successful. 0 errors, 3 warnings

System (2) Processing (44) Extra Info (41) Warning (3) Critical Warning Error Suppressed Flag /

Message: 0 of 90 Location: Locate

For Help, press F1



Type	Message
Info	Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 2/problem4_18101707/problem4_18101707.wvf"
Info	Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Simulation partitioned into 1 sub-simulations
Info	Simulation coverage is 100.00 %
Info	Number of transitions in simulation is 9099
Info	Quartus II Simulator was successful. 0 errors, 0 warnings

System (4) Processing (9) Extra Info (9) Info (9) Warning Critical Warning Error Suppressed Flag /

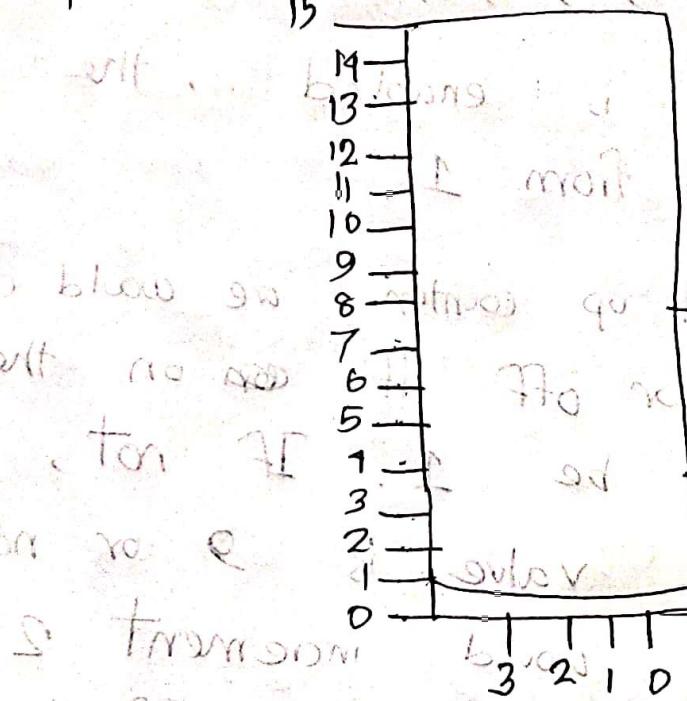
Messages Message: 0 of 16

Locate

Problem 4

We have to design 16 to 1 mux.

which would have 4 bit selector pin.



Since here, I was told to use case statement, I have used case of selector pins to represent the output.

Waveform files can verify that our code works perfectly.

Quartus II - D:/COURSE/CSE460 LAB FILES/LAB 2/problem5_18101707/problem5_18101707 - [problem5_18101707.v]

File Edit View Project Assignments Processing Tools Window Help

problem5_18101707

Tasks Flow: Compilation

problem5_18101707.v Compilation Report - Flow Summary problem5_18101707.vwf Simulation Report - Simulation Waveforms

Task List

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Classic Timing Analysis
- EDA Netlist Writer

Program Device (Open Program)

```
1 module problem5_18101707(Clk,reset,UpOrDown,Count);
2
3     input Clk,reset,UpOrDown;
4
5     output [3 : 0] Count;
6
7     reg [3 : 0] Count = 0;
8
9     always @ (posedge(Clk) or posedge(reset))
10    begin
11        if(reset == 1)
12            Count <= 0;
13        else
14            if(UpOrDown == 1)
15                if(Count == 15)
16                    Count <= 0;
17                else
18                    Count <= Count + 1;
19            else
20                if(Count == 0)
21                    Count <= 15;
22                else
23                    Count <= Count - 1;
24
25    end
26
27 endmodule
28
29
```

Type	Message
Info	Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 2/problem5_18101707/problem5_18101707.vwf"
Info	Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Simulation partitioned into 1 sub-simulations
Info	Simulation coverage is 73.91 %
Info	Number of transitions in simulation is 13041
Info	Quartus II Simulator was successful. 0 errors, 0 warnings

Messages

System (6) Processing (9) Extra Info (9) Info (9) Warning Critical Warning Error Suppressed Flag /

Message: 0 of 16

For Help, press F1

Ln 16, Col 32

Idle NUM

File Edit View Project Assignments Processing Tool Window Help

problem5_18101707

Tasks
Flow: Compilation

Task List

- ✓ ▶ Compile Design
- ✓ ▶ Analysis & Synthesis
- ✓ ▶ Fitter (Place & Route)
- ✓ ▶ Assembler (Generate program)
- ✓ ▶ Classic Timing Analysis
- ✓ ▶ EDA Netlist Writer
- Program Device (Open Program)

problem5_18101707.v

Compilation Report - Flow Summary

problem5_18101707.vwf

Simulation Report - Simulation Waveforms

Flow Summary

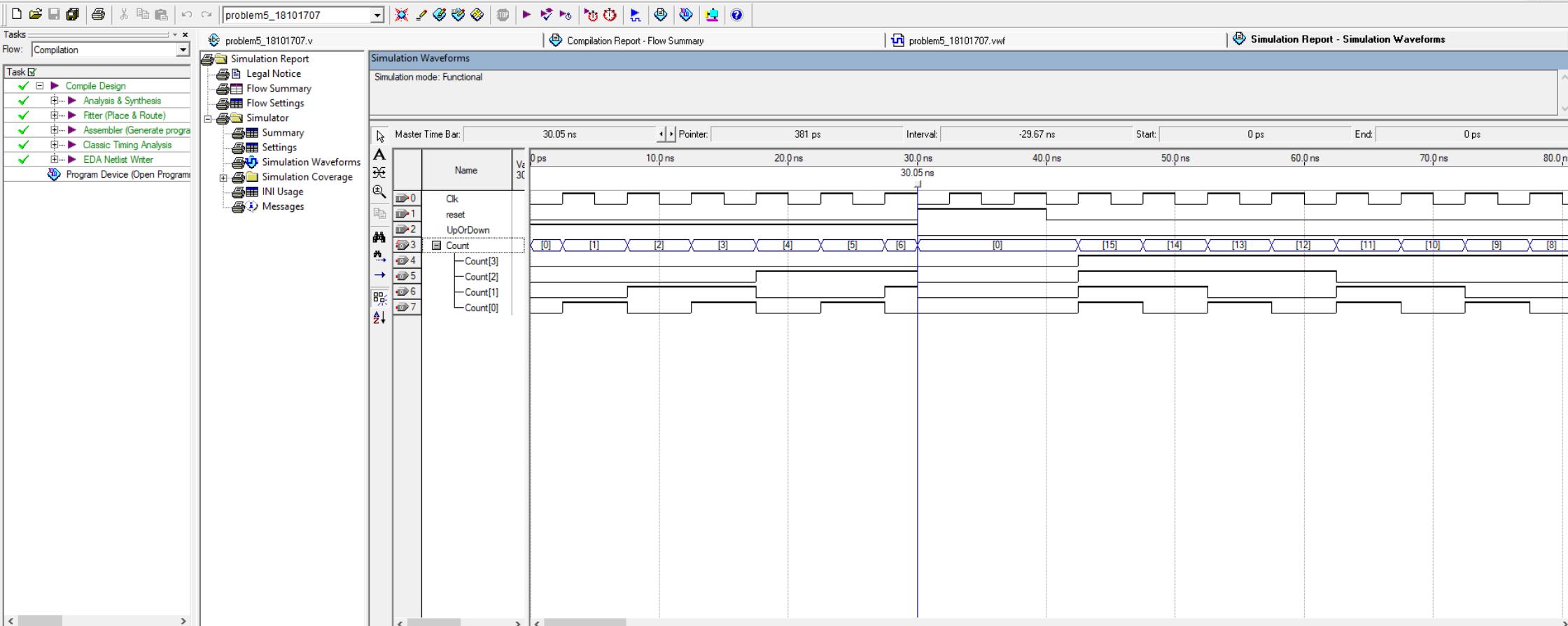
Flow Status	Successful - Tue Mar 23 11:32:15 2021
Quartus II Version	8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name	problem5_18101707
Top-level Entity Name	problem5_18101707
Family	FLEX10KE
Met timing requirements	Yes
Total logic elements	4 / 1,728 (< 1 %)
Total pins	7 / 102 (7 %)
Total memory bits	0 / 24,576 (0 %)
Total PLLs	0
Device	EPF10K30ETC144-1
Timing Models	Final

Type	Message
Info	Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 2/problem5_18101707/problem5_18101707.vwf"
Info	Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Simulation partitioned into 1 sub-simulations
Info	Simulation coverage is 73.91 %
Info	Number of transitions in simulation is 13041
Info	Quartus II Simulator was successful. 0 errors, 0 warnings

System (6) Processing (9) Extra Info (3) Warning Critical Warning Error Suppressed Flag /

Messages: 0 of 16

Locate



Type	Message
Info	Using vector source file "D:/COURSE/CSE460 LAB FILES/LAB 2/problem5_18101707/problem5_18101707.vwf"
Info	Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info	Simulation partitioned into 1 sub-simulations
Info	Simulation coverage is 73.91 %
Info	Number of transitions in simulation is 13041
Info	Quartus II Simulator was successful. 0 errors, 0 warnings

System (6) Processing (9) Extra Info (9) Info (9) Warning Critical Warning Error Suppressed Flag /

Messages: 0 of 16

Locate

problem 5

Here I was told to find the mistakes, since we are using the count inside the always block so it would need reg. after always, block '@' should be used.

I also ~~were~~ removed begin and end block to ~~be~~ them in the else statement.

Finally code ~~compile~~ compile and we can see the waveform file to verify.