Trigger Experiment

I. Experimental Purpose

1. Test the function test for a S-R Latch.
2. Test the function test for a D-FF.
3. Test the function test for a JK-FF.

II. Instruments and Materials

1. Software: Quartus II 13.1.
2. Integrated chips

74LS00	NAND gate
74LS74	double D Flip-Flop
74LS112	double JK Flip-Flop

III. Experimental Contents

1. Test the function for a basic S-R latch

A basic S-R latch can be constructed though two NAND gates, showed in Figure 1.

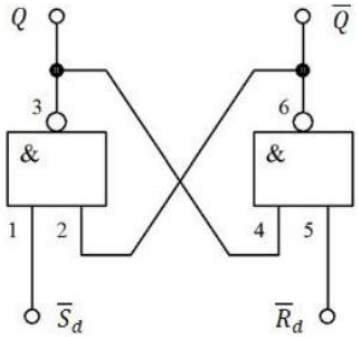

Fig. 1 A basic S-R latch constructed by NAND gates

(1) Input different signals with $\overline{S_d}$ and $\overline{R_d}$, and fill the results in the Table 1.

Table 1. The logical function table of a S-R latch

$\bar{S}_d$	$\bar{R}_d$	Q	$\overline{Q}$	Function
0	0			
0	1			
1	0			
1	1			

(2) According to logical function in Table 1 for a S-R latch, answer the questions as follows?

a. What are the main functions for a S-R latch?

b. How many valid states does a S-R latch have?

c. What is the invalid state for a S-R latch? It will result in a what constraint for the inputs of this latch.

2. Test the function for a D-FF

A positive edge D-FF is shown in Fig. 2, we can find it in a 74LS74 integrated chip.

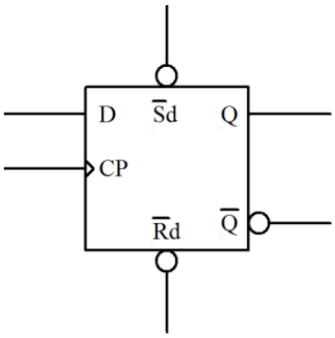

Fig. 2 A positive edge D-FF

(1) Investigate the functions for this type of D-FF in a simulation through different inputs, pls fill the results in Table 2. Note that the clock signal is set to 1.

Table 2. The logical function table of a D-FF

$\bar{S}_d$	$\bar{R}_d$	CP	D	Q^n	Q^{n+1}	*Function*
0	1	X	X	0		
				1		
1	0	X	X	0		
				1		
1	1	↑	0	0		
				1		
1	1	↑	0	0		
				1		

(2) Inputting a periodical clock pulse, pls present the output wave in Fig. 3, and investigate the conscience with the results in Table 2.

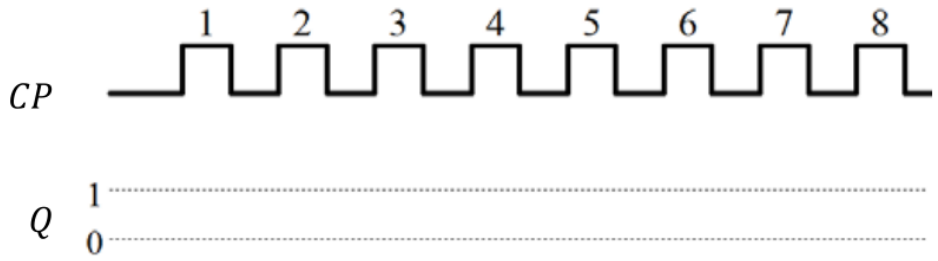

Fig. 3 The output wave of a D-FF when there is a periodical clock pulse.

3. Test the function for a JK-FF

A negative edge JK-FF is shown in Fig. 4, we can find it in a 74LS112 integrated chip.

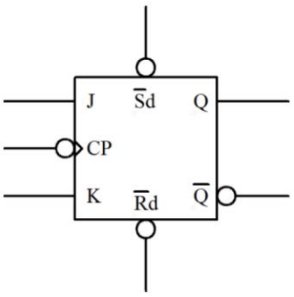

Fig. 2 A positive edge JK-FF

(1) Investigate the functions for this type of JK-FF in a simulation through different inputs, pls fill the results in Table 3.

Table 3. The logical function table of a JK-FF

$\bar{S}_d$	$\bar{R}_d$	**CP**	**J**	**K**	Q^n	Q^{n+1}	*Function*
0	1	X	X	X	X		
1	0	X	X	X	X		
1	1	↓	**0**	**0**	0		
					1		
1	1	↓	0	1	X		
1	1	↓	1	0	X		
1	1	↓	1	1	0		
					1		

(2) Inputting a periodical clock pulse, pls present the output wave in Fig. 4, and investigate the conscience with the results in Table 3.

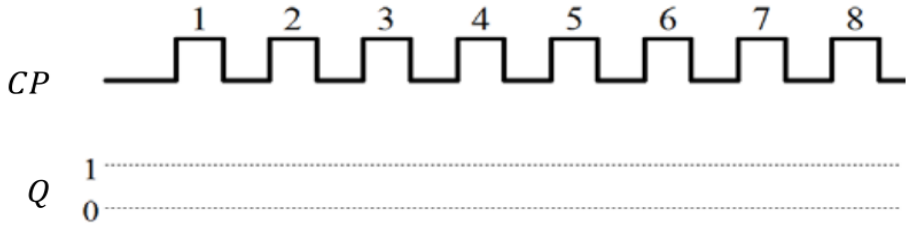

Fig. 4 The output wave of a JK-FF when there is a periodical clock pulse.

(3) Inputting a periodical clock pulse, pls present the output wave in Fig. 6 when **J=K=1**. Pls summary the function of this JK-FF under this scenario.

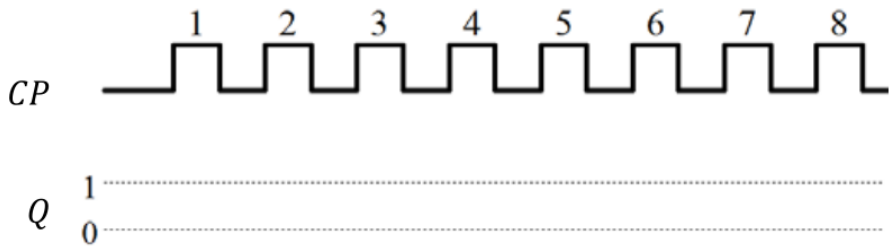

Fig. 4 The output wave of a JK-FF when J=K=1.