ERICA RUGGIERO

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Education

MIT Sloan School of Management **2015 – Present**
Candidate for MBA, June 2017 *Cambridge, MA*

- Enterprise Management Track: Consulting for national Internet service provider on Smart City technology strategy
- Volunteer Lead and Organizing Committee Member for Breaking the Mold Conference, Sloan Women in Management
- Active member of the Management Consulting and Technology Clubs

Cornell University **2008 – 2012**
BS in Electrical and Computer Engineering, magna cum laude *Ithaca, NY*

- GPA: 3.92/4.3, Dean's List seven semesters
- Chair of the Society of Women Engineers Outreach Committee

Experience

Intel Corporation **2011 – 2015**
Digital Design Engineer (Promoted from Grade 3 to Grade 5 in 18 months, 6 months early) *Hudson, MA*

- Designed and led development for a test chip to be used in corporation-wide process technology research; design was the most complex to be implemented on a test chip in team's history
- Influenced management to supply a multi-discipline team of three engineers to assist in test chip project execution in order to meet tight 6-month deadline and ensure highest quality standards
- Built consensus between team and internal stakeholders who commissioned the test chip through weekly discussions about feasibility of chip features; led a rigorous final design review with customers and senior technical leadership
- Persuaded multiple managers to expand personal responsibilities to a dual logical and physical design role; reduced time to converge design by 30%, increased cross-functional knowledge sharing, and piloted dual role for future projects
- Streamlined code-generation process that resulted in 50% reduction in engineering hours per week; maintained the code database which was used by over 60 engineers across three Intel projects
- Converged functional unit blocks to design milestones across four Intel Xeon microprocessors and Omni-Path products; ramped up quickly on each new project to meet tight turnaround time of one to two months between milestones
- Co-led the Women at Intel Network Hudson chapter: organized volunteer opportunities, professional development workshops and networking events, negotiated with corporate and site groups for over $6K in funding

Intel Corporation **2010 – 2011**
Physical Design Intern *Hudson, MA*

- Modeled timing and power consumption for chip critical paths and proposed optimal routing schemes for those paths
- Developed chip power plan after pooling input from cross-site team members; plan implemented across all chip SKUs

Additional Information

- Patent holder, US Patent 9,138,339: a tool gripper device that adapts items like eating utensils to a larger handle circumference, allowing people with handicaps to easily maneuver those items; developed tool gripper in High School
- Budget Buddies Coach: taught financial literacy to low-income women from the community (2013-2015)
- Interests: Amateur painter and hiker, seasoned traveler (Asia, Europe and Americas regions)