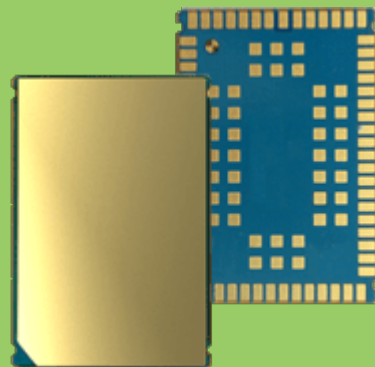




CINTERION
a Gemalto company

Differences between BGS2 Rel.1 and BGS2 Rel.2

Version: 01
DocID: BGS2_rel2_migration_v01



Product Comparison

Document Name: **Differences between BGS2 Rel.1 and BGS2 Rel.2**

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0 Document History

New document: "Differences between BGS2 Rel.1 and BGS2 Rel.2", Version 01

Chapter	What is new
---	Initial document setup.

1 Introduction

This document¹ compares the Cinterion wireless modules BGS2 Rel.1 and BGS2 Rel.2. It lists hardware related differences between these modules.

The aim of the document is to provide guidance on how to migrate from BGS2 Rel.1 to BGS2 Rel.2. Chapter 4 gives advice on designing one common hardware platform for smooth transition between all described products.

BGS2 Rel.1 and BGS2 Rel.2 in this document refer to the product variants BGS2-E and BGS2-W. Where necessary a note is made to differentiate between these two product variants.

1.1 Related Documents

- [1] BGS2 Rel.1 Hardware Interface Description
- [2] BGS2 Rel.2 Hardware Interface Description
- [3] BGS2 Rel.1 AT Command Set
- [4] BGS2 Rel.2 AT Command Set
- [5] BGS2 Rel.2 Release Note

1.2 Type Approval

BGS2 Rel.1 and BGS2 Rel.2 comply with the same standards and directives – except for

- Standards of North American type approval that are not applicable to BGS2-E

For more regulatory and type approval information see [1] and [2].

¹ The document is effective only if listed in the appropriate Release Notes as part of the technical documentation delivered with your Cinterion wireless product.

2 Software Related Differences

An overview of new software features as well as known issues can be found in the latest BGS2 Rel.2 Release Note, [5].

For detailed information on all AT command differences between BGS2 Rel.1 and BGS2 Rel.2 please refer to the respective AT Command Specifications, i.e., [3] for BGS2 Rel.1, [4] for BGS2 Rel.2.

3 Hardware Related Differences

The focus of this chapter is on hardware differences between BGS2 Rel.1 and BGS2 Rel.2.

3.1 Feature Overview

The following table compares general properties and features of BGS2 Rel.1 and BGS2 Rel.2. It lists differences between the modules. Where appropriate, these differences are described in more detail in the next sections.

Table 1: Feature overview

Feature/Property	BGS2 Rel.1	BGS2 Rel.2
Interface Properties		
Module interface	For pad assignments see Chapter 4.	
Serial interface (ASC0)	Voltage level 1.8V or 2.85V configurable for all interface lines	Voltage level 1.8V or 2.85V configurable for TXD0, RXD0, CTS0, RTS0 and RING0 lines Voltage level 1.8V set fix for DTR0, DSR0 and DCD0 lines
Digital audio interface	Not supported	One DAI/PCM interface
GPIO interface	10 GPIO lines shared with an I ² C interface, LED signaling and PWM functionality	6 GPIO lines shared with an I ² C interface, LED signaling and PWM functionality
Fast shutdown	Not supported	Dedicated line

3.2 Application Interface

3.2.1 ASC0 Interface

With BGS2 Rel.1 and BGS2 Rel.2 the voltage level of the ASC0 interface can be configured to either 1.8V or 2.85V:

- If the VDIG signal (i.e., application interface pad 10) is connected to the V180 line (i.e., application interface pad 35) the ASC0 interface starts up with a 1.8V signal level. All lines of the BGS2 Rel.1 and BGS2 Rel.2 ASC0 interface will now be on the 1.8V signal level.
- If the VDIG signal (i.e., application interface pad 10) is connected to the V285 line (i.e., application interface pad 22), the ASC0 interface runs with a 2.85V signal level. With BGS2 Rel.1 all lines of the ASC0 interface will now be on the 2.85V signal level. With BGS2 Rel.2 the TXD0, RXD0, CTS0, RTS0, RING0 lines will now also be on the 2.85V signal level, but the DTR0, DSR0 and DCD0 lines will remain at the 1.8V signal level.

The following table shows further ASC0 interface differences between the modules.

Table 2: ASC0 start-up/reset signal states²

ASC0 interface lines	BGS2 Rel.1	BGS2 Rel.2
RXD0	T / PU (-204µA at 0.05V)	T / PU (-204µA at 0.05V)
TXD0	T / PU (-204µA at 0.05V)	T / PU (-204µA at 0.05V)
CTS0	T / PD (+51µA at 1.75V)	T / PD (+51µA at 1.75V)
RTS0	T / 10k PU	T / 10k PU
DTR0	T / PD (+103µA at 1.75V)	T / PU (-102µA at 0.05V)
DCD0	T / PU (-102µA at 0.05V)	T / PU (-102µA at 0.05V)
DSR0	T / PD (+27µA at 1.75V)	T / PU (-102µA at 0.05V)
RING0	T / 10k PU	T / 10k PU

For more information on the interface and its start-up timings please refer to the respective "Hardware Interface Description".

² T = Tristate; PU = Pull-up; PD = Pull-down

3.2.2 Digital Audio Interface

BGS2 Rel.1 does not support a digital audio interface.

BGS2 Rel.2 has a digital audio interface (DAI). The digital audio interface is implemented as a pulse code modulation (PCM) interface. Basic characteristics are listed in the tables below. For more information on the interface and its start-up timings please refer to the BGS2 Rel.2 “Hardware Interface Description”.

Table 3: PCM characteristics

Characteristics	BGS2 Rel.2
PCM Audio mode	Master mode, 256kHz clock, long frame

Table 4: DAI start-up/reset signal states

DAI interface lines	BGS2 Rel.2
RXDDAI	T / PD (+51µA at 1.75V)
TXDDAI	T / PD (+51µA at 1.75V)
TFSDAI	T / PD (+51µA at 1.75V)
SCLK	T / PU (-55µA at 0.05V)

3.2.3 GPIO Interface

BGS2 Rel.1 and BGS2 Rel.2 differ in the number and assignment of their GPIO lines as listed in the table below.

Table 5: GPIO lines

GPIO lines	BGS2 Rel.1	BGS2 Rel.2
GPIO1	GPIO1	Not available (used as DTR0)
GPIO2	GPIO2	Not available (used as DCD0)
GPIO3	GPIO3	Not available (used as DSR0)
GPIO4	GPIO4	Not available (used as FAST_SHTDWN)
GPIO5	GPIO5 / LED	GPIO5 / LED
GPIO6	GPIO6 / PWM	GPIO6 / PWM
GPIO7	GPIO7 / PWM	GPIO7 / PWM
GPIO8	GPIO8	GPIO8
GPIO9	GPIO9 / I2CCLK (shared)	GPIO9 / I2CCLK (shared)
GPIO10	GPIO10 / I2CDAT (shared)	GPIO10 / I2CDAT (shared)

For more information on the interface and its start-up timings please refer to the respective "Hardware Interface Description".

3.2.4 Fast Shutdown

BGS2 Rel.1 does not provide a dedicated fast shutdown line.

BGS2 Rel.2 supports such a FAST_SHTDWN signal. If enabled by using the AT command AT^SCFG "MEShutdown/Fso", a low impulse >10ms on the FAST_SHTDWN line starts the fast shutdown. The fast shutdown procedure still finishes any data activities on the module's flash file system, thus ensuring data integrity, but will no longer deregister gracefully from the network, thus saving the time required for network deregistration.

Please note that if enabled, the normal software controlled shutdown using AT^SMSO will also be a fast shutdown, i.e., without network deregistration. However, in this case no URCs including shutdown URCs will be provided by the AT^SMSO command.

Table 6: FAST_SHTDWN characteristics

FAST_SHTDWN	BGS2 Rel.2
V _{IH} max	1.9V
V _{IH} min	1.35V
V _{IL} max	0.34V I _{IH} min < -200μA at V _{IH} min



For more information on the fast shutdown line please refer to the BGS2 Rel.2 "Hardware Interface Description" and "AT Command Set".

4 Common Footprint Design

The following chapter shows the pad assignment differences between BGS2 Rel.1 and BGS2 Rel.2. It notes the modifications a possible common footprint design will have to allow for in order to provide an easy migration path from one product to the next one.

The following figures show that only few changes are required to adapt an existing hardware platform to meet the requirements of another product.

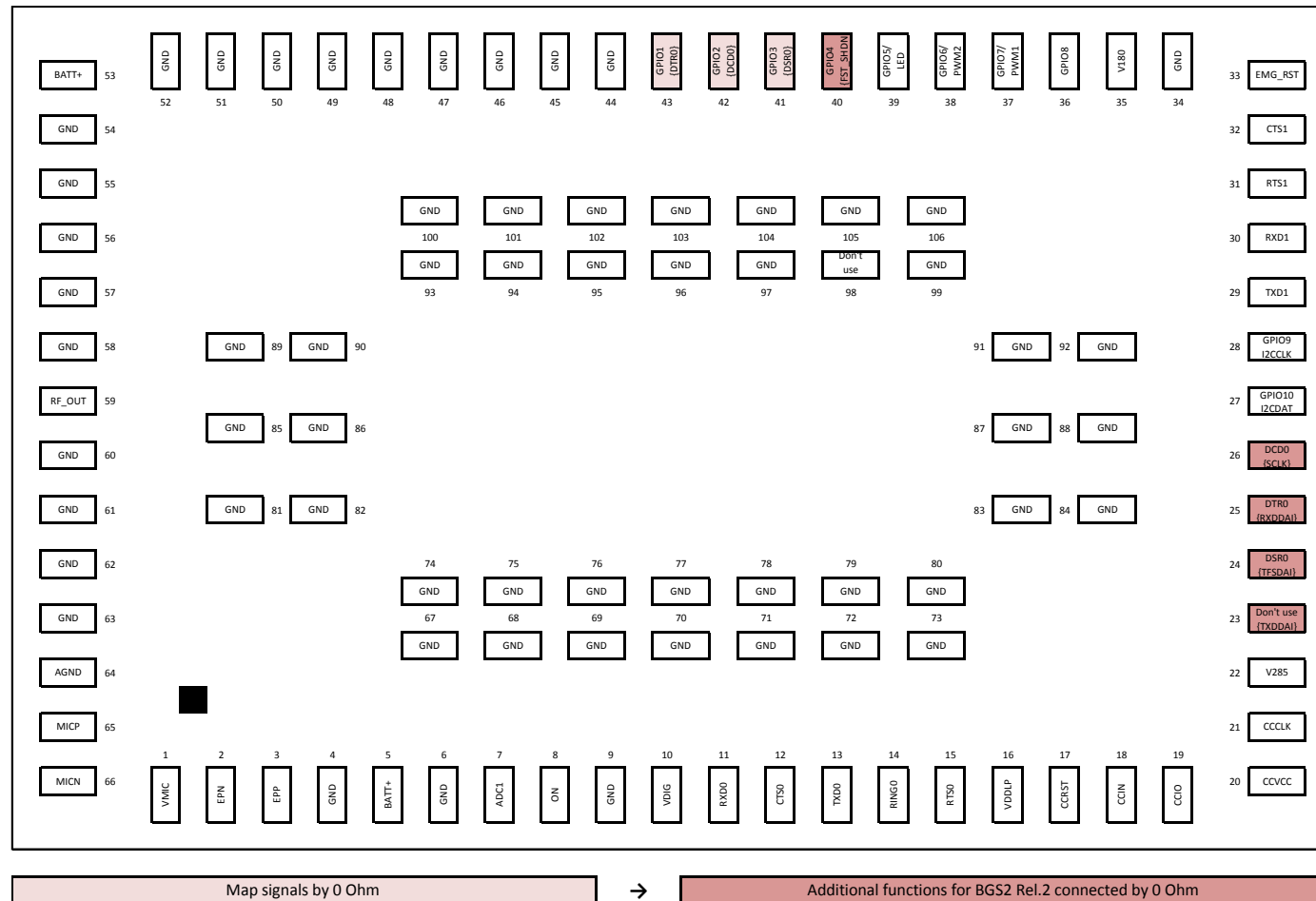
When using the same footprint for BGS2 Rel.1 and BGS2 Rel.2 take care that the following requirements be met:

- Some pads should be connected via 0 Ohm resistors to easily activate or deactivate product specific functions for smooth transition.
These pads are marked (light) pink   in the figure below.

Pad assignments shown in curly brackets signify a possible alternative assignment/functionality for a pad in a common footprint. For example {SCLK} indicates a pad that should be connected via 0 Ohm resistors to easily activate or deactivate the pad's alternative digital audio interface line functionality for the appropriate module. The pad's other serial interface functionality (DCD0) may also be connected via 0 Ohm resistors to be able to activate or deactivate it for another module.

Differences between BGS2 Rel.1 and BGS2 Rel.2

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	BGS2r1	BGS2r2
DCD0	26	42
DTR0	25	43
DSR0	24	41

Figure 1: Common footprint for migration from BGS2 Rel.1 to BGS2 Rel.2 (bottom view)