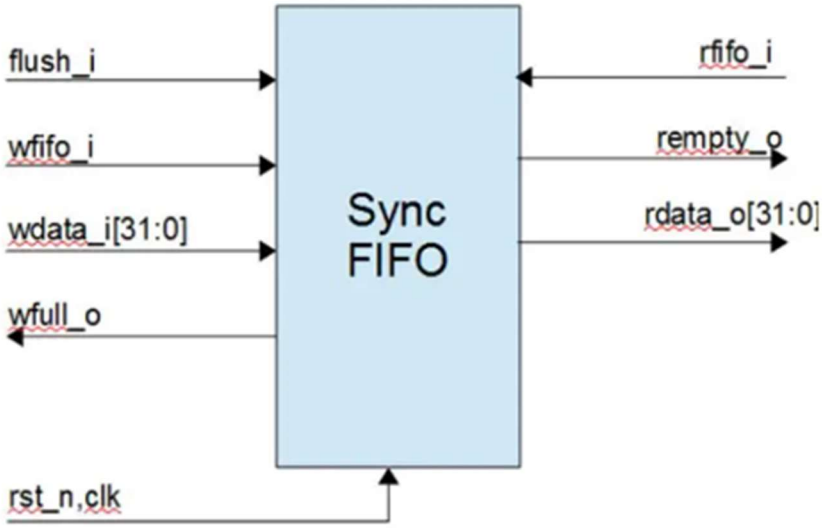
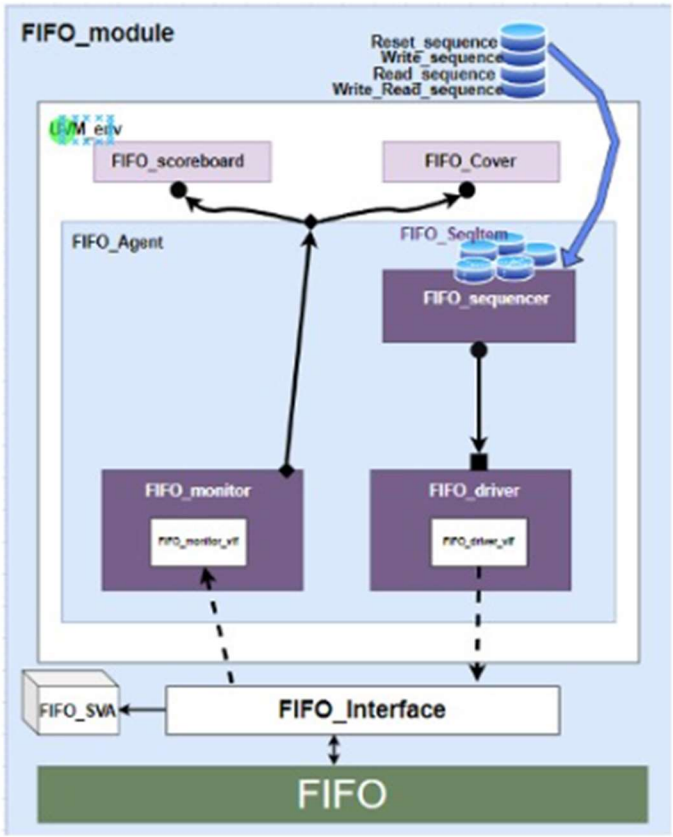
Technical report

RTL:



Testbench structure



Explanation:

. FIFO.sv

- *Purpose: This is the main module that describes the synchronous FIFO (First-In, First-Out) design. It includes the logic for storing data, managing read and write operations, and controlling flags (like full and empty).*

2. FIFO_if_pkg.sv

- *Purpose: This file defines the interface for the FIFO. It includes signal declarations that connect the FIFO to other components, like inputs (data in, write enable) and outputs (data out, flags).*

3. FIFO_assertions.sv

- *Purpose: This file contains assertions that check the correctness of the FIFO's behavior during simulation. Assertions help ensure that certain conditions (like not reading from an empty FIFO) are met.*

4. FIFO_seq_item.sv

- *Purpose: This defines the structure of the transactions that will be sent to the FIFO. Each transaction might include data to be written or control signals.*

5. FIFO_sequence.sv

- *Purpose: This file contains sequences that define the order and timing of transactions. It tells the testbench when and what data to send to the FIFO for writing or reading.*

6. fifo_config_obj_pkg.sv

- *Purpose: This package includes configuration objects that hold parameters for the testbench, such as FIFO depth and width. These parameters can be used throughout the testbench to ensure consistency.*

7. sequencer.sv

- *Purpose: This file defines the sequencer, which manages the flow of transactions from the sequence to the driver. It coordinates when transactions are sent to the FIFO.*

8. FIFO_driver.sv

- *Purpose: The driver takes transactions from the sequencer and applies them to the FIFO. It translates the sequence items into actual signal changes on the DUT (Design Under Test).*

9. FIFO_monitor.sv

- *Purpose: This component observes the DUT's outputs and collects data. It monitors the FIFO's behavior and can help in generating coverage data or reporting errors.*

10. FIFO_agent.sv

- *Purpose: The agent combines the driver, sequencer, and monitor into a single unit. It acts as a facilitator for all interactions between the testbench and the FIFO.*

11. shared_pkg.sv

- *Purpose: This package contains common definitions or utilities that can be shared across multiple components in your testbench. It might include types or functions that are used in various places.*

12. FIFO_scoreboard.sv

- *Purpose: The scoreboard checks whether the FIFO's output matches the expected results. It compares what the DUT produces with what it should produce based on the transactions sent to it.*

13. fifo_coverage_pkg.sv

- *Purpose: This package includes definitions for coverage collection. It specifies which scenarios (like full, empty conditions) need to be tracked to ensure that all important behaviors of the FIFO are tested.*

14. FIFO_env.sv

- *Purpose: This file sets up the entire test environment. It instantiates the agent, scoreboard, and any other components required for testing the FIFO.*

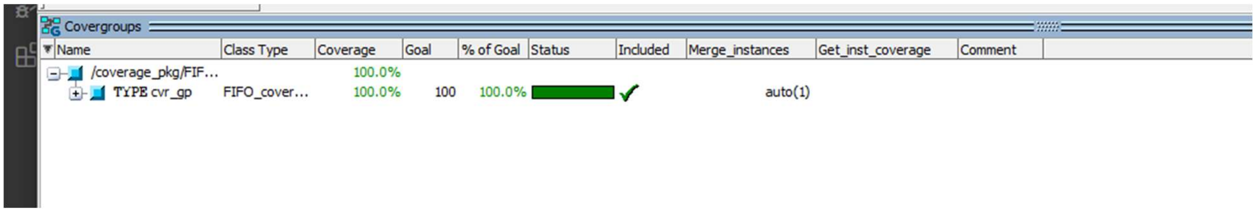
15. FIFO_test.sv

- *Purpose: This is the main test class that initializes the environment and runs the tests. It defines what tests will be executed and manages the overall testing process.*

16. top.sv

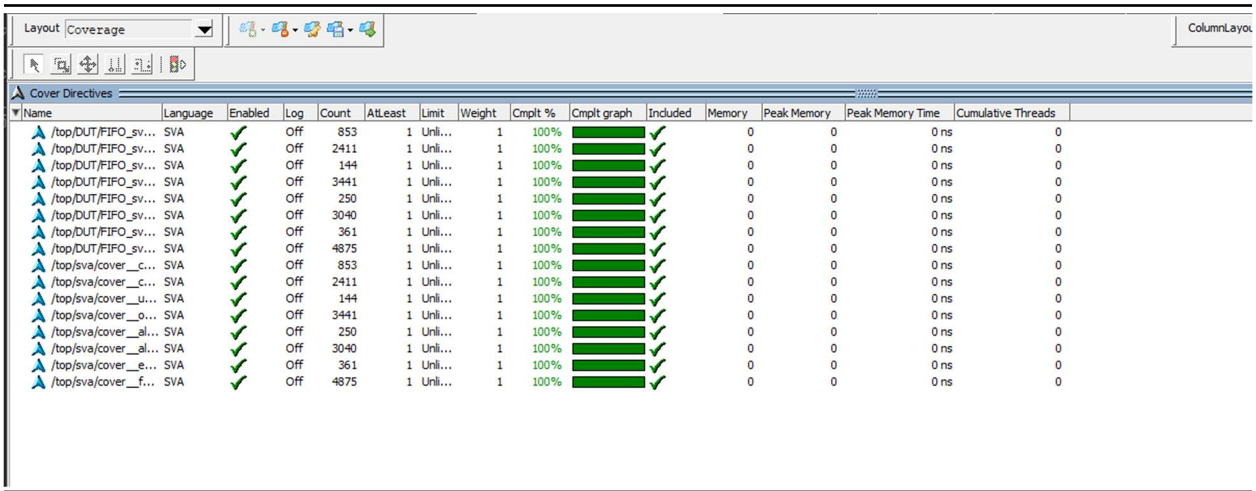
- *Purpose: The top module that brings everything together. It instantiates the DUT and the UVM environment, connecting them to run the entire testbench.*

Results:



Covergroups

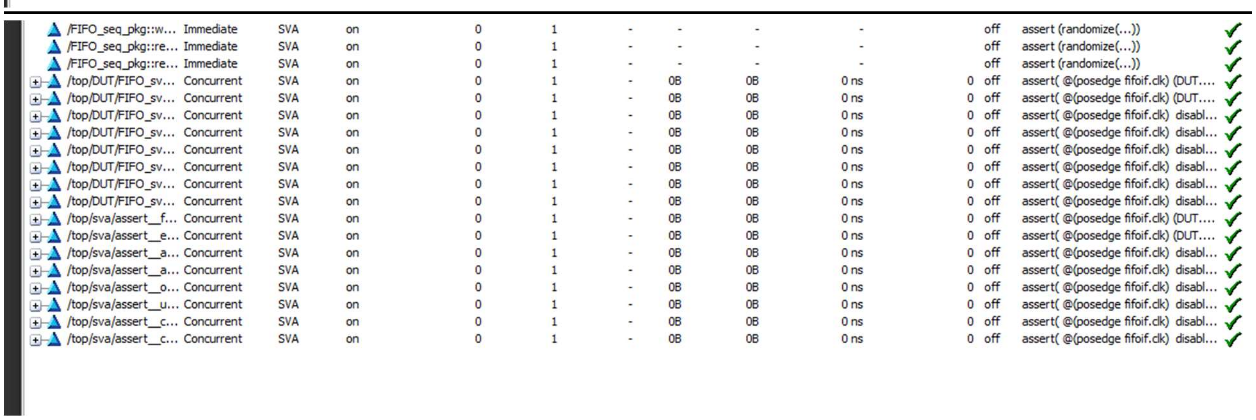
Name	Class Type	Coverage	Goal	% of Goal	Status	Included	Merge_instances	Get_inst_coverage	Comment
/coverage_pkg/FIF…		100.0%							
TYPE cvr_gp	FIFO_cover…	100.0%	100	100.0%		✓		auto(1)	



Layout Coverage

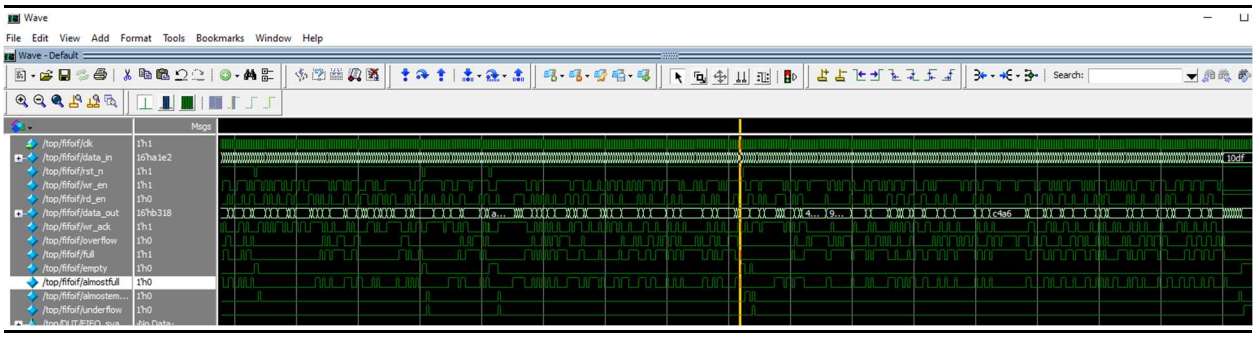
Cover Directives

Name	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads
/top/DUT/FIFO_sv…	SVA	✓	Off	853	1	Unli…	1	100%		✓	0	0	0 ns	0
/top/DUT/FIFO_sv…	SVA	✓	Off	2411	1	Unli…	1	100%		✓	0	0	0 ns	0
/top/DUT/FIFO_sv…	SVA	✓	Off	144	1	Unli…	1	100%		✓	0	0	0 ns	0
/top/DUT/FIFO_sv…	SVA	✓	Off	3441	1	Unli…	1	100%		✓	0	0	0 ns	0
/top/DUT/FIFO_sv…	SVA	✓	Off	250	1	Unli…	1	100%		✓	0	0	0 ns	0
/top/DUT/FIFO_sv…	SVA	✓	Off	3040	1	Unli…	1	100%		✓	0	0	0 ns	0
/top/DUT/FIFO_sv…	SVA	✓	Off	361	1	Unli…	1	100%		✓	0	0	0 ns	0
/top/DUT/FIFO_sv…	SVA	✓	Off	4875	1	Unli…	1	100%		✓	0	0	0 ns	0
/top/sva/cover__c…	SVA	✓	Off	853	1	Unli…	1	100%		✓	0	0	0 ns	0
/top/sva/cover__c…	SVA	✓	Off	2411	1	Unli…	1	100%		✓	0	0	0 ns	0
/top/sva/cover__u…	SVA	✓	Off	144	1	Unli…	1	100%		✓	0	0	0 ns	0
/top/sva/cover__o…	SVA	✓	Off	3441	1	Unli…	1	100%		✓	0	0	0 ns	0
/top/sva/cover__al…	SVA	✓	Off	250	1	Unli…	1	100%		✓	0	0	0 ns	0
/top/sva/cover__al…	SVA	✓	Off	3040	1	Unli…	1	100%		✓	0	0	0 ns	0
/top/sva/cover__e…	SVA	✓	Off	361	1	Unli…	1	100%		✓	0	0	0 ns	0
/top/sva/cover__f…	SVA	✓	Off	4875	1	Unli…	1	100%		✓	0	0	0 ns	0



/FIFO_seq_pkg::w…	Immediate	SVA	on	0	1	-	-	-	-		off	assert (randomize(...))	✓
/FIFO_seq_pkg::re…	Immediate	SVA	on	0	1	-	-	-	-		off	assert (randomize(...))	✓
/FIFO_seq_pkg::re…	Immediate	SVA	on	0	1	-	-	-	-		off	assert (randomize(...))	✓
/top/DUT/FIFO_sv…	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) (DUT.…	✓
/top/DUT/FIFO_sv…	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) (DUT.…	✓
/top/DUT/FIFO_sv…	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disabl…	✓
/top/DUT/FIFO_sv…	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disabl…	✓
/top/DUT/FIFO_sv…	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disabl…	✓
/top/DUT/FIFO_sv…	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disabl…	✓
/top/DUT/FIFO_sv…	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disabl…	✓
/top/DUT/FIFO_sv…	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disabl…	✓
/top/sva/assert__f…	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) (DUT.…	✓
/top/sva/assert__e…	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) (DUT.…	✓
/top/sva/assert__a…	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disabl…	✓
/top/sva/assert__a…	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disabl…	✓
/top/sva/assert__o…	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disabl…	✓
/top/sva/assert__u…	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disabl…	✓
/top/sva/assert__c…	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disabl…	✓
/top/sva/assert__c…	Concurrent	SVA	on	0	1	-	0B	0B	0 ns	0	off	assert(@(posedge fifoif.clk) disabl…	✓

```
#
# UVM_INFO verilog_src/questa_uvm_pkg-1.2/src/questa_uvm_pkg.sv(215) @ 0: reporter [Questa UVM] QUESTA_UVM-1.2.3
# UVM_INFO verilog_src/questa_uvm_pkg-1.2/src/questa_uvm_pkg.sv(217) @ 0: reporter [Questa UVM]  questa_uvm::init(+struct)
# UVM_INFO @ 0: reporter [RNTST] Running test FIFO_test...
# UVM_INFO FIFO_test.sv(41) @ 0: uvm_test_top [run_phase] Reset Asserted
# UVM_INFO FIFO_test.sv(43) @ 8: uvm_test_top [run_phase] Reset Deasserted
# UVM_INFO FIFO_test.sv(45) @ 8: uvm_test_top [run_phase] Stimulus Generation Started
# UVM_INFO FIFO_test.sv(47) @ 808: uvm_test_top [run_phase] Write seq finished
# UVM_INFO FIFO_test.sv(49) @ 1608: uvm_test_top [run_phase] Read seq finished
# UVM_INFO FIFO_test.sv(51) @ 81608: uvm_test_top [run_phase] Write Read seq finished
# UVM_INFO FIFO_test.sv(52) @ 81608: uvm_test_top [run_phase] Stimulus Generation Ended
# UVM_INFO verilog_src/uvm-1.1d/src/base/uvm_objection.svh(1268) @ 81608: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
# UVM_INFO FIFO_scoreboard.sv(148) @ 81608: uvm_test_top.env.sb [report_phase] Total successful transactions: 10201
# UVM_INFO FIFO_scoreboard.sv(149) @ 81608: uvm_test_top.env.sb [report_phase] Total failed transactions: 0
#
```



```
ASSERTION RESULTS:
---------------------------------------------------------
Name                 File(Line)           Failure Pass
                                          Count   Count
---------------------------------------------------------
/top/DUT/FIFO_sva_inst/assert__count_decrement_assertion
                     FIFO_assertions.sv(58)       0     1
/top/DUT/FIFO_sva_inst/assert__count_increment_assertion
                     FIFO_assertions.sv(50)       0     1
/top/DUT/FIFO_sva_inst/assert__underflow_assertion
                     FIFO_assertions.sv(42)       0     1
/top/DUT/FIFO_sva_inst/assert__overflow_assertion
                     FIFO_assertions.sv(34)       0     1
/top/DUT/FIFO_sva_inst/assert__almostempty_assertion
                     FIFO_assertions.sv(27)       0     1
/top/DUT/FIFO_sva_inst/assert__almostfull_assertion
                     FIFO_assertions.sv(20)       0     1
/top/DUT/FIFO_sva_inst/assert__empty_assertion
                     FIFO_assertions.sv(13)       0     1
/top/DUT/FIFO_sva_inst/assert__full_assertion
                     FIFO_assertions.sv(6)        0     1
/top/sva/assert__count_decrement_assertion
                     FIFO_assertions.sv(58)       0     1
/top/sva/assert__count_increment_assertion
                     FIFO_assertions.sv(50)       0     1
/top/sva/assert__underflow_assertion
                     FIFO_assertions.sv(42)       0     1
/top/sva/assert__overflow_assertion
                     FIFO_assertions.sv(34)       0     1
/top/sva/assert__almostempty_assertion
                     FIFO_assertions.sv(27)       0     1
/top/sva/assert__almostfull_assertion
                     FIFO_assertions.sv(20)       0     1
/top/sva/assert__empty_assertion
                     FIFO_assertions.sv(13)       0     1
/top/sva/assert__full_assertion
                     FIFO_assertions.sv(6)        0     1
/FIFO_seq_pkg/write_sequence/body/#ublk#225236087#34/immed__37
                     FIFO_sequence.sv(37)         0     1
/FIFO_seq_pkg/read_sequence/body/#ublk#225236087#53/immed__56
                     FIFO_sequence.sv(56)         0     1
```

```
COVERGROUP COVERAGE:
----------------------------------------------------------------------------------------------------
Covergroup                                          Metric      Goal    Status

----------------------------------------------------------------------------------------------------
 TYPE /coverage_pkg/FIFO_coverage/cvr_gp            100.0%       100    Covered
    covered/total bins:                                 60        60
    missing/total bins:                                  0        60
    % Hit:                                          100.0%       100
    Coverpoint cvr_gp::cp_wr_en                     100.0%       100    Covered
        covered/total bins:                              2         2
        missing/total bins:                              0         2
        % Hit:                                      100.0%       100
        bin wr_en_0                                   3081         1    Covered
        bin wr_en_1                                   7023         1    Covered
    Coverpoint cvr_gp::cp_rd_en                     100.0%       100    Covered
        covered/total bins:                              2         2
        missing/total bins:                              0         2
        % Hit:                                      100.0%       100
        bin rd_en_0                                   7019         1    Covered
        bin rd_en_1                                   3085         1    Covered
    Coverpoint cvr_gp::cp_underflow                 100.0%       100    Covered
        covered/total bins:                              2         2
        missing/total bins:                              0         2
        % Hit:                                      100.0%       100
        bin underflow_0                               9960         1    Covered
        bin underflow_1                                144         1    Covered
    Coverpoint cvr_gp::cp_overflow                  100.0%       100    Covered
        covered/total bins:                              2         2
        missing/total bins:                              0         2
        % Hit:                                      100.0%       100
        bin overflow_0                                6635         1    Covered
        bin overflow_1                                3469         1    Covered
    Coverpoint cvr_gp::cp_empty                     100.0%       100    Covered
        covered/total bins:                              2         2
        missing/total bins:                              0         2
        % Hit:                                      100.0%       100
        bin empty_0                                   9932         1    Covered
        bin empty_1                                    172         1    Covered
    Coverpoint cvr_gp::cp_full                      100.0%       100    Covered
        covered/total bins:                              2         2
        missing/total bins:                              0         2
        % Hit:                                      100.0%       100
```

bin auto[1]	3085	1	Covered
Coverpoint cvr_gp::#seq_item_cov.almostempty__2#			
	100.0%	100	Covered
covered/total bins:	2	2	
missing/total bins:	0	2	
% Hit:	100.0%	100	
bin auto[0]	9848	1	Covered
bin auto[1]	256	1	Covered
Coverpoint cvr_gp::#seq_item_cov.almostfull__3#			
	100.0%	100	Covered
covered/total bins:	2	2	
missing/total bins:	0	2	
% Hit:	100.0%	100	
bin auto[0]	7031	1	Covered
bin auto[1]	3073	1	Covered
Cross cvr_gp::cross_cvr_full	100.0%	100	Covered
covered/total bins:	6	6	
missing/total bins:	0	6	
% Hit:	100.0%	100	
bin <wr_en_0,rd_en_0,full_0>	1116	1	Covered
bin <wr_en_0,rd_en_1,full_0>	975	1	Covered
bin <wr_en_1,rd_en_0,full_0>	992	1	Covered
bin <wr_en_1,rd_en_1,full_0>	2110	1	Covered
bin <wr_en_0,rd_en_0,full_1>	990	1	Covered
bin <wr_en_1,rd_en_0,full_1>	3921	1	Covered
illegal_bin ignore_full_invalid	0		ZERO
Cross cvr_gp::cross_cvr_almostfull	100.0%	100	Covered
covered/total bins:	8	8	
missing/total bins:	0	8	
% Hit:	100.0%	100	
bin <wr_en_0,rd_en_0,auto[0]>	1459	1	Covered
bin <wr_en_0,rd_en_0,auto[1]>	647	1	Covered
bin <wr_en_1,rd_en_0,auto[0]>	4580	1	Covered
bin <wr_en_1,rd_en_0,auto[1]>	333	1	Covered
bin <wr_en_0,rd_en_1,auto[0]>	559	1	Covered
bin <wr_en_0,rd_en_1,auto[1]>	416	1	Covered
bin <wr_en_1,rd_en_1,auto[0]>	433	1	Covered
bin <wr_en_1,rd_en_1,auto[1]>	1677	1	Covered
Cross cvr_gp::cross_cvr_empty	100.0%	100	Covered
covered/total bins:	6	6	
missing/total bins:	0	6	
% Hit:	100.0%	100	
bin <wr_en_0,rd_en_0,empty_0>	2070	1	Covered

```
                                        FIFO_assertions Verilog  SVA  FIFO_assertions.sv(51)
                                                                              2411 Covered
/top/DUT/FIFO_sva_inst/cover__underflow_assertion
                                        FIFO_assertions Verilog  SVA  FIFO_assertions.sv(43)
                                                                               149 Covered
/top/DUT/FIFO_sva_inst/cover__overflow_assertion
                                        FIFO_assertions Verilog  SVA  FIFO_assertions.sv(35)
                                                                              3441 Covered
/top/DUT/FIFO_sva_inst/cover__almostempty_assertion
                                        FIFO_assertions Verilog  SVA  FIFO_assertions.sv(28)
                                                                               251 Covered
/top/DUT/FIFO_sva_inst/cover__almostfull_assertion
                                        FIFO_assertions Verilog  SVA  FIFO_assertions.sv(21)
                                                                              3041 Covered
/top/DUT/FIFO_sva_inst/cover__empty_assertion
                                        FIFO_assertions Verilog  SVA  FIFO_assertions.sv(14)
                                                                               367 Covered
/top/DUT/FIFO_sva_inst/cover__full_assertion
                                        FIFO_assertions Verilog  SVA  FIFO_assertions.sv(7)
                                                                              4875 Covered
/top/sva/cover__count_decrement_assertion
                                        FIFO_assertions Verilog  SVA  FIFO_assertions.sv(59)
                                                                               861 Covered
/top/sva/cover__count_increment_assertion
                                        FIFO_assertions Verilog  SVA  FIFO_assertions.sv(51)
                                                                              2411 Covered
/top/sva/cover__underflow_assertion     FIFO_assertions Verilog  SVA  FIFO_assertions.sv(43)
                                                                               149 Covered
/top/sva/cover__overflow_assertion      FIFO_assertions Verilog  SVA  FIFO_assertions.sv(35)
                                                                              3441 Covered
/top/sva/cover__almostempty_assertion   FIFO_assertions Verilog  SVA  FIFO_assertions.sv(28)
                                                                               251 Covered
/top/sva/cover__almostfull_assertion    FIFO_assertions Verilog  SVA  FIFO_assertions.sv(21)
                                                                              3041 Covered
/top/sva/cover__empty_assertion         FIFO_assertions Verilog  SVA  FIFO_assertions.sv(14)
                                                                               367 Covered
/top/sva/cover__full_assertion          FIFO_assertions Verilog  SVA  FIFO_assertions.sv(7)
                                                                              4875 Covered

TOTAL DIRECTIVE COVERAGE: 100.0%  COVERS: 16

ASSERTION RESULTS:
---------------------------------------------------------
```