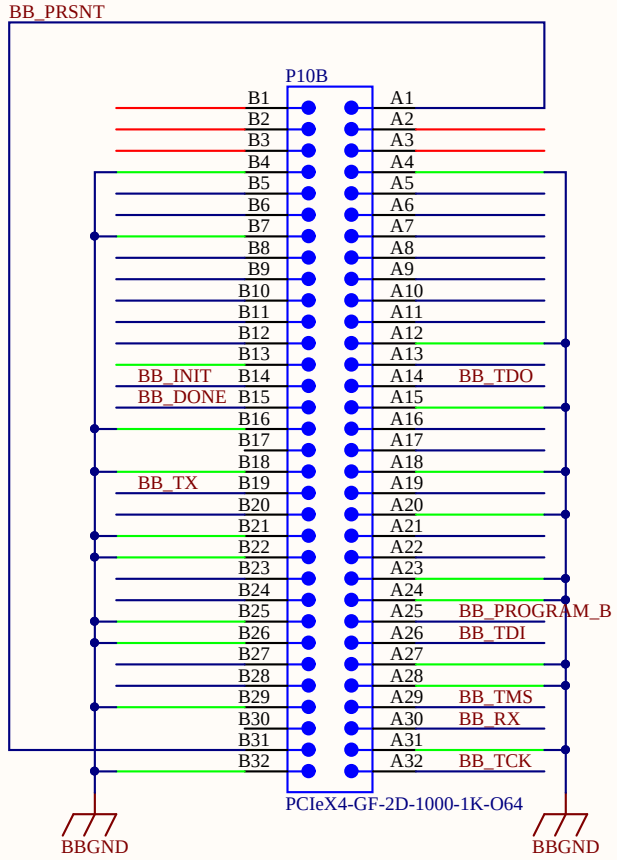

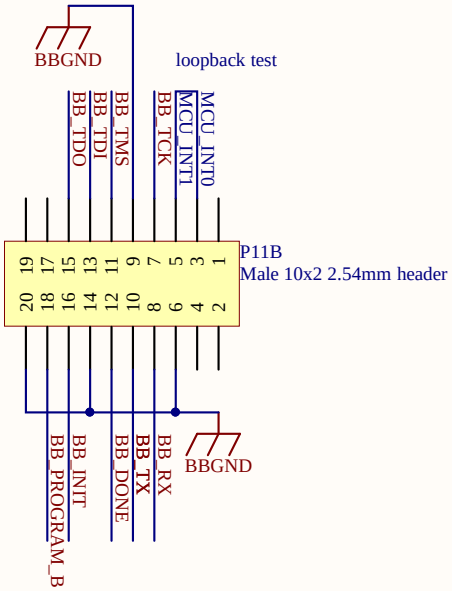

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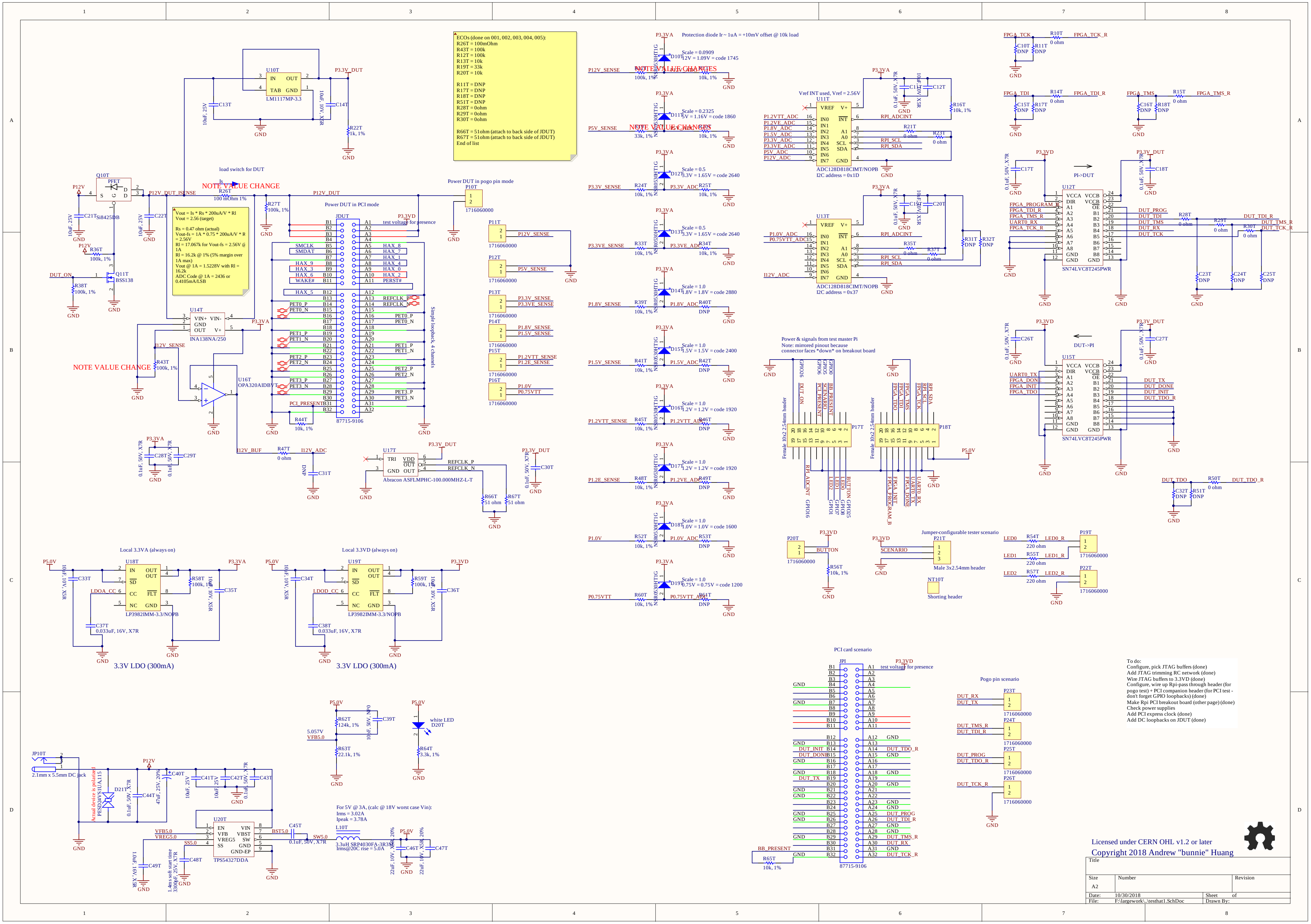
Size A	Number	Revision
Date: 10/30/2018		Sheet of
File: F:\largework\..\pi2pci.SchDoc		Drawn By:



ECOs (done on 001, 002, 003, 004, 005):
R26T = 100mOhm
R43T = 100k
R12T = 100k
R13T = 10k
R19T = 33k
R20T = 10k
R11T = DNP
R17T = DNP
R18T = DNP
R51T = DNP
R28T = 0ohm
R29T = 0ohm
R30T = 0ohm
R66T = 51ohm (attach to back side of JDUT)
R67T = 51ohm (attach to back side of JDUT)
End of list
load switch for DUT
NOTE VALUE CHANGE
Vout = Is * Rs * 200uA/V * Rl
Vout = 2.56 (target)
Rs = 0.47 ohm (actual)
Vout-fs = 1A * 0.75 * 200uA/V * R = 2.56V
Rl = 17.067k for Vout-fs = 2.56V @ 1A
Rl = 16.2k @ 1% (5% margin over 1A max)
Vout @ 1A = 1.5228V with Rl = 16.2k
ADC Code @ 1A = 2436 or 0.4105mA/LSB
Power DUT in pogo pin mode
Power DUT in PCI mode
Simple loopback, 4 channels
Protection diode Ir ~ 1uA = +10mV offset @ 10k load
NOTE VALUE CHANGES
Vref INT used, Vref = 2.56V
I2C address = 0x1D
I2C address = 0x37
PI->DUT
DUT->PI
Power & signals from test master Pi
Note: mirrored pinout because connector faces *down* on breakout board
Jumper-configurable tester scenario
Male 3x2.54mm header
Shorting header
Local 3.3VA (always on)
Local 3.3VD (always on)
3.3V LDO (300mA)
3.3V LDO (300mA)
2.1mm x 5.5mm DC jack
Actual device is polarized
For 5V @ 3A, (calc @ 18V worst case Vin):
Irms = 3.02A
Ipeak = 3.78A
3.3uH SRP4030FA-3R3M
Irms@20C rise = 5.0A
1.4ms soft start time
white LED
PCI card scenario
Pogo pin scenario
To do:
Configure, pick JTAG buffers (done)
Add JTAG trimming RC network (done)
Wire JTAG buffers to 3.3VD (done)
Configure, wire up Rpi-pass through header (for pogo test) + PCI companion header (for PCI test - don't forget GPIO loopbacks) (done)
Make Rpi PCI breakout board (other page) (done)
Check power supplies
Add PCI express clock (done)
Add DC loopbacks on JDUT (done)
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Title
Size A2
Number
Revision
Date: 10/30/2018
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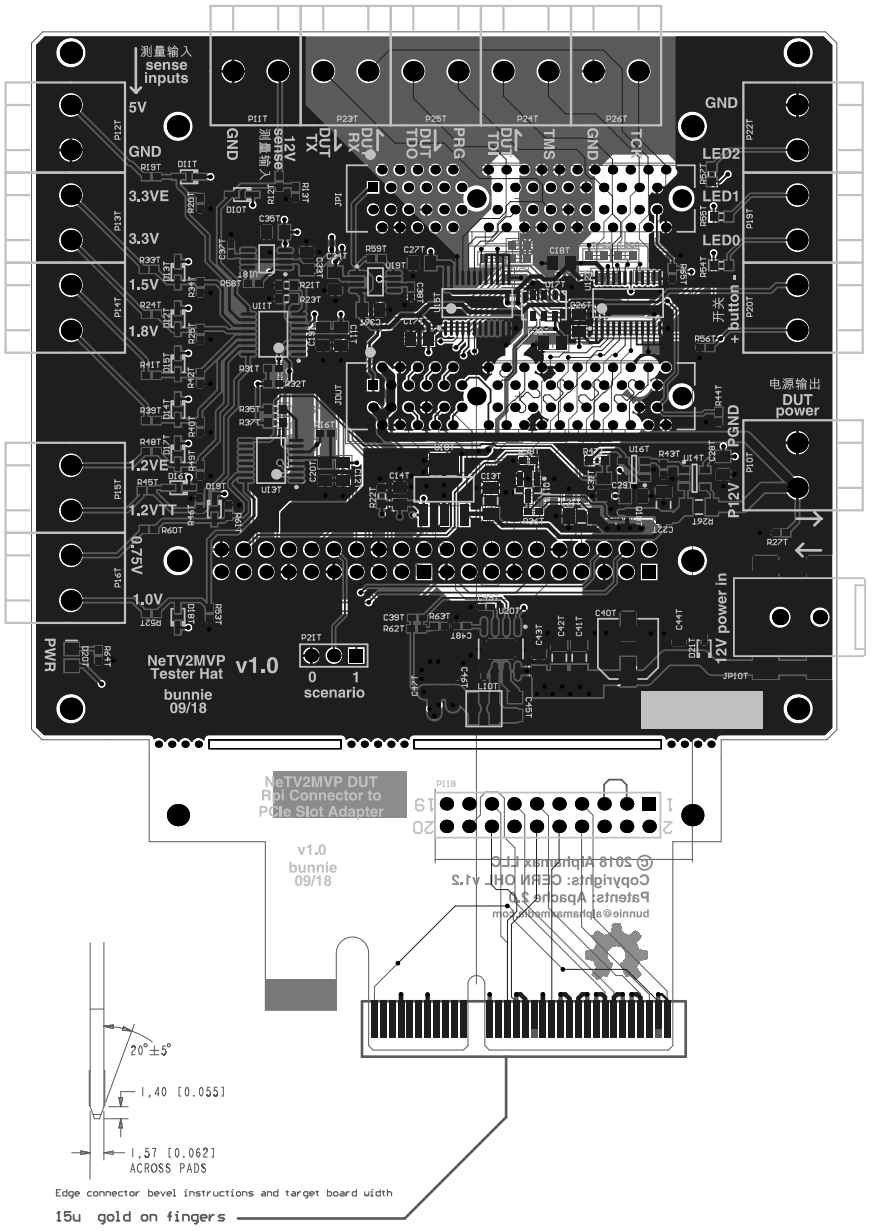
File: F:\largework\...\testhat1.SchDoc
Drawn By:



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	TopOverlay				
2	TopSolder	Solder Resist	0.010mm	3.5	
3	L1	Copper	0.045mm		
4	Dielectric1	FR-4	0.100mm	4.3	
5	L2	Copper	0.036mm		
6	Dielectric4	FR-4	1.200mm	4.3	
7	L5	Copper	0.036mm		
8	Dielectric5	FR-4	0.100mm	4.2	
9	L6	Copper	0.045mm		
10	BottomSolder	Solder Resist	0.010mm	3.5	
11	BottomOverlay				

Impedance control: 50 ohm = 0.1mm +/- 10%

Soldermask: green

Silkscreen: white

Finish: HASL except on gold fingers as indicated in drawing

- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI_Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.