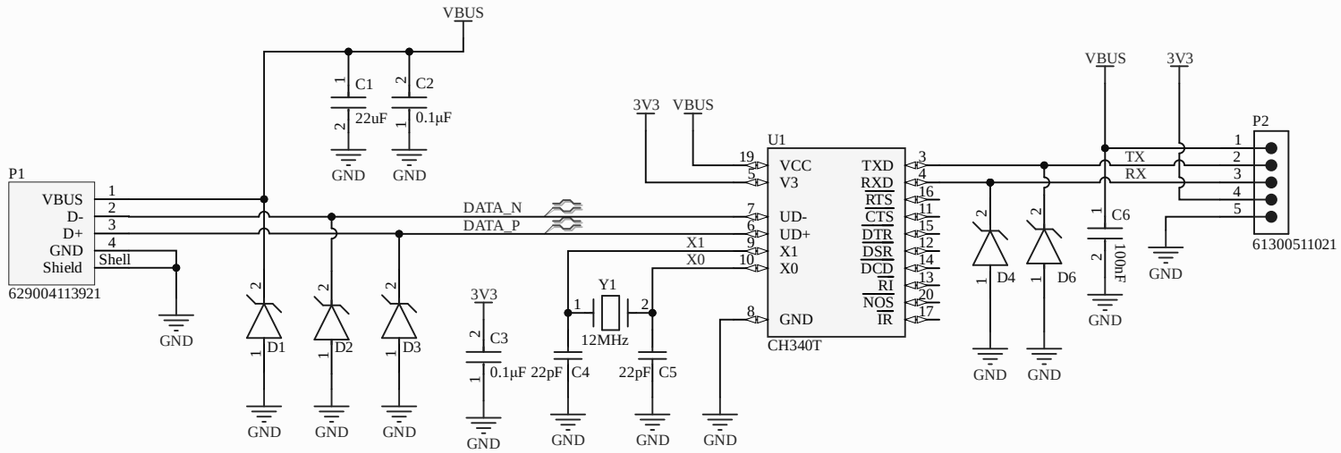
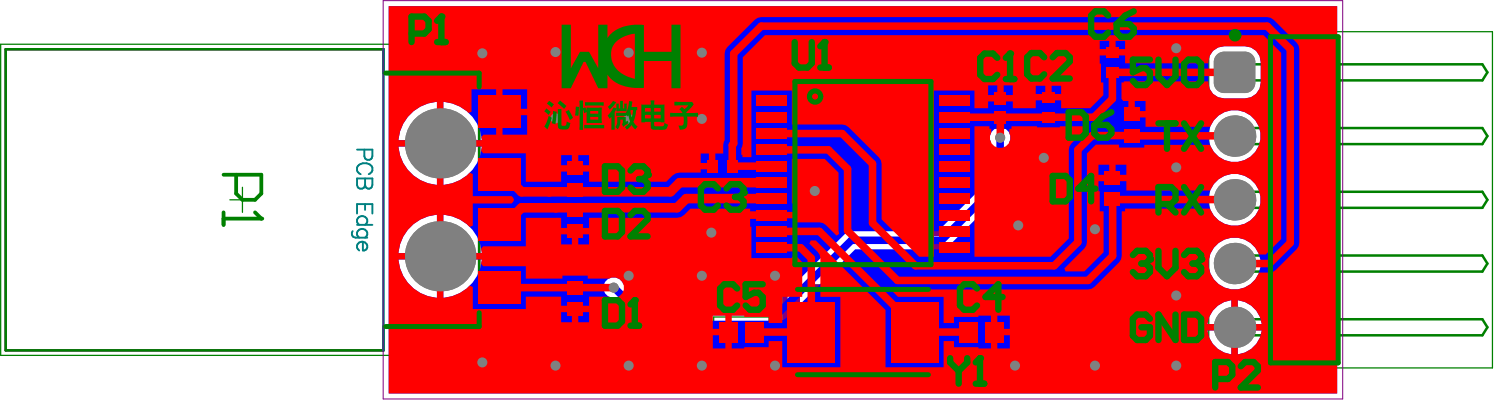
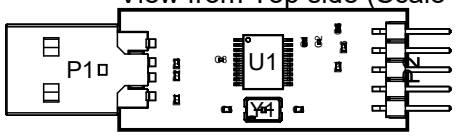
WDH_CH340_USB_To_UART



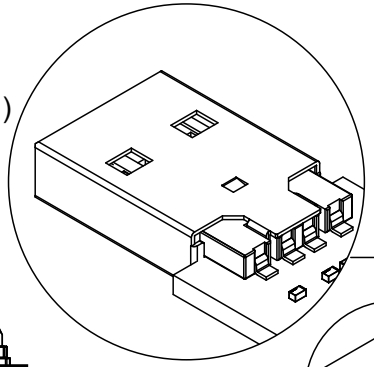
Title		
Size: B	Number	Revision
Date: 3/25/2025	Sheet of	
File: D:\Altium Design Projects\..\CH340_USB_To_UART.SchDoc	Drawn By:	


P1
沁恒微电子
U1
C1
C2
C6
5V0
TX
RX
3V3
GND
P2
D3
D2
D1
C3
C5
C4
Y1
D4
PCB Edge

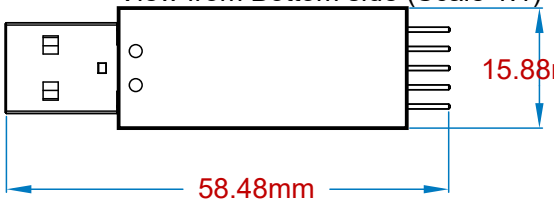
View from Top side (Scale 1:1)



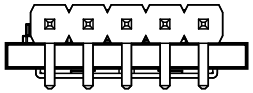
View from Front side (Scale 1:1)

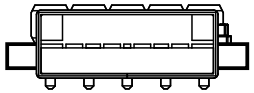


View from Bottom side (Scale 1:1)

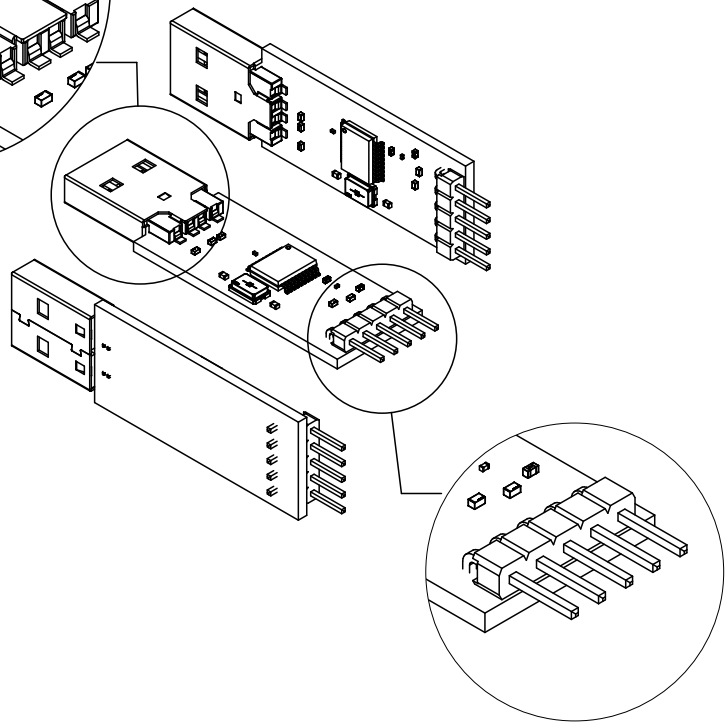


View from Right side (Scale 2:1)

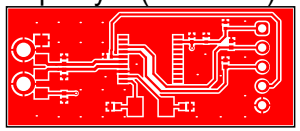




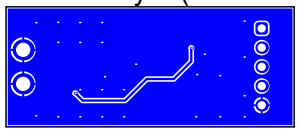
View from Left side (Scale 2:1)



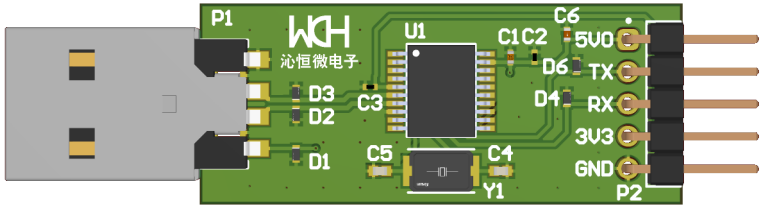
Top Layer (Scale 1:1)



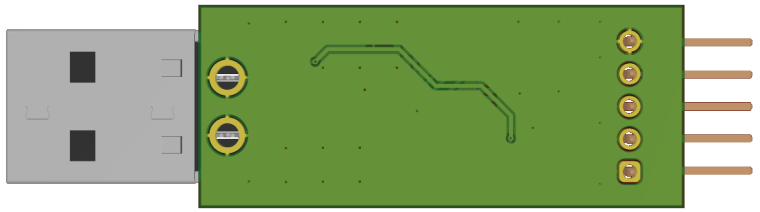
Bottom Layer (Scale 1:1)



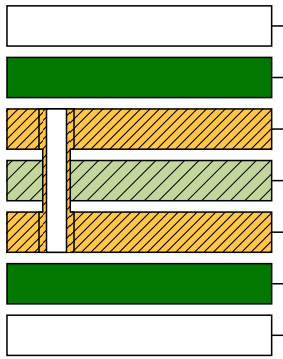
Realistic View



Realistic View

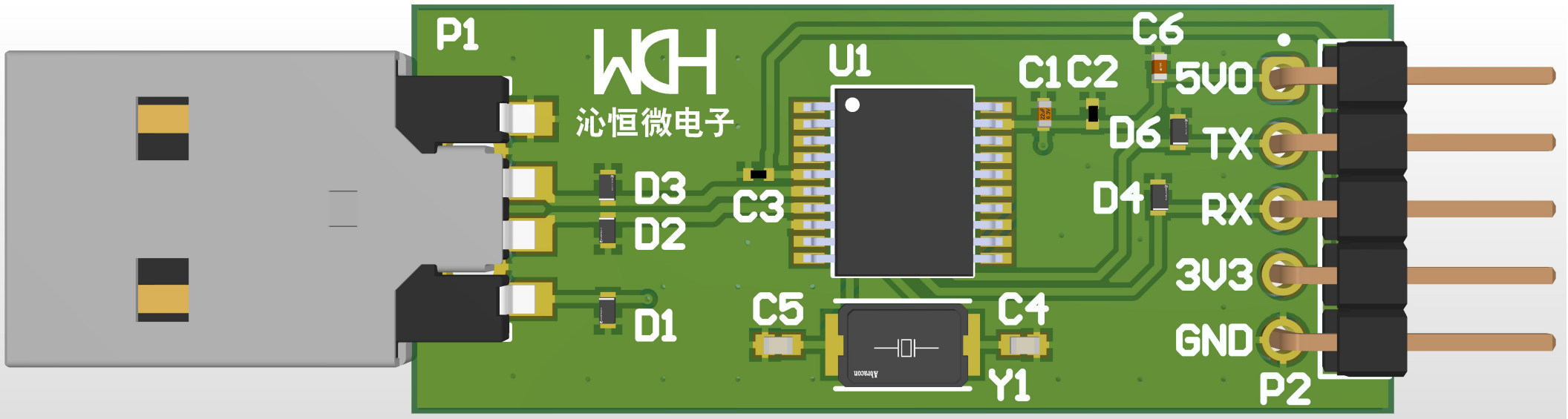


Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type
	Top Overlay			Legend
Surface Material	Top Solder	0.01mm	Solder Resist	Solder Mask
Copper	**Top Layer**	**0.04mm**		**Signal**
Core FR-4		*1.50mm*	*FR-4*	*Dielectric*
Copper	**Bottom Layer**	**0.04mm**		**Signal**
Surface Material	Bottom Solder	0.01mm	Solder Resist	Solder Mask
	Bottom Overlay			Legend

Total thickness: 1.59mm


P1
沁恒微电子
U1
C6
C1
C2
5V0
D6
TX
D3
C3
D4
RX
D2
3V3
D1
C5
C4
GND
Y1
P2

Design Rules Verification Report

Filename : D:\Altium Design Projects\CH340_USB_To_UART\CH340_USB_To_UART.PcbD(

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=8mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=10mil) (Preferred=10mil) (InNetClass('3V3') And InNetClass('VBUS') And	0
Width Constraint (Min=5.906mil) (Max=11.811mil) (Preferred=7.874mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=1mil) (All),(All)	0
Silk To Solder Mask (Clearance=8mil) (IsPad),(All)	0
Silk to Silk (Clearance=10mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	0