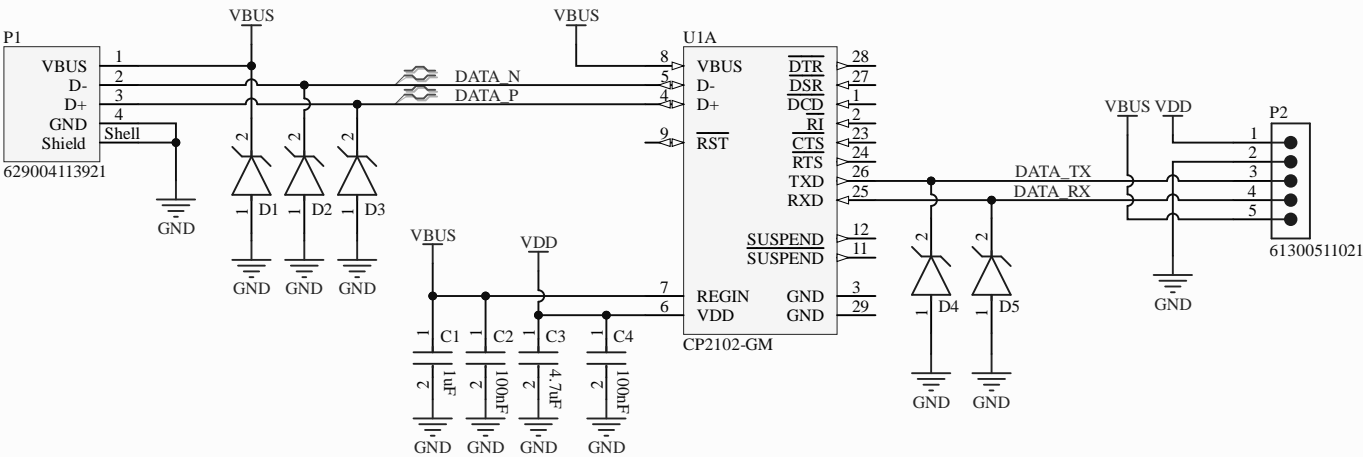
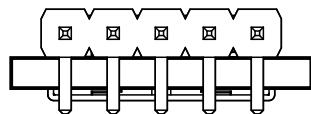
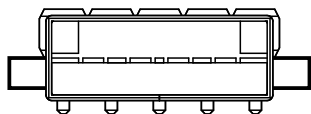
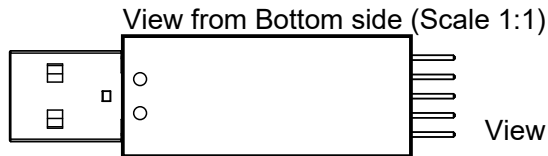
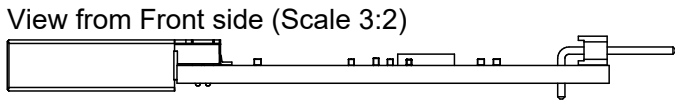
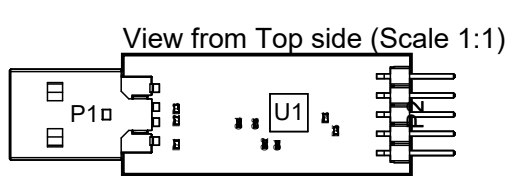


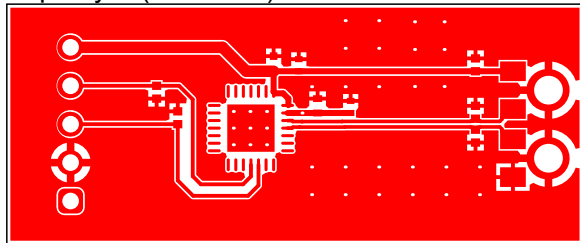
Silicon Labs\_CP2102\_USB\_To\_UART



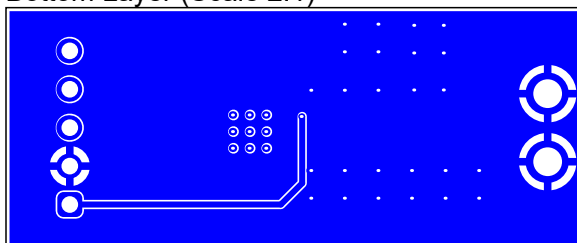
Title		
Size	Number	Revision
B		
Date:	3/25/2025	Sheet of
File:	D:\Altium Design Projects\...\CP2102_USB_To_UART.SchDoc	



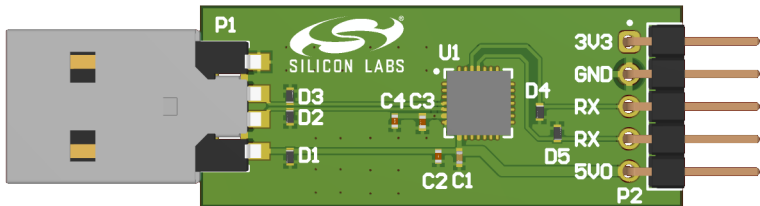
Top Layer (Scale 2:1)



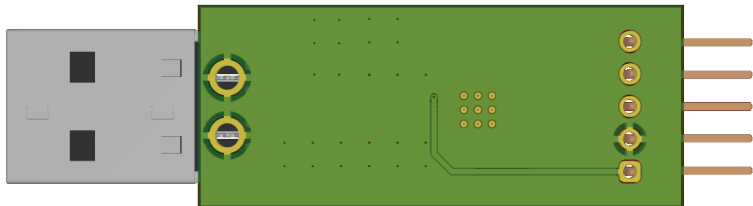
Bottom Layer (Scale 2:1)



Realistic View



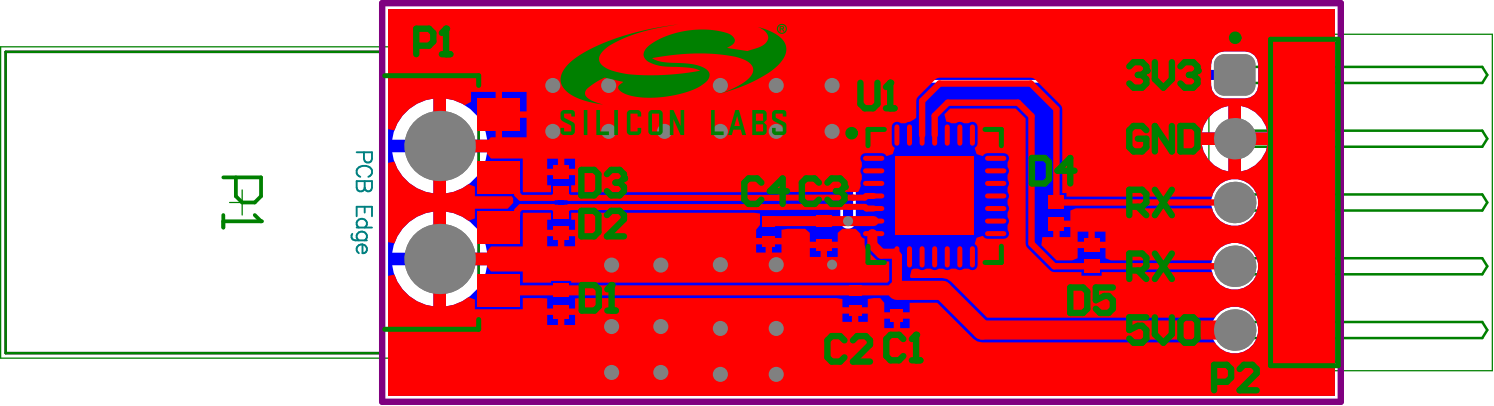
Realistic View

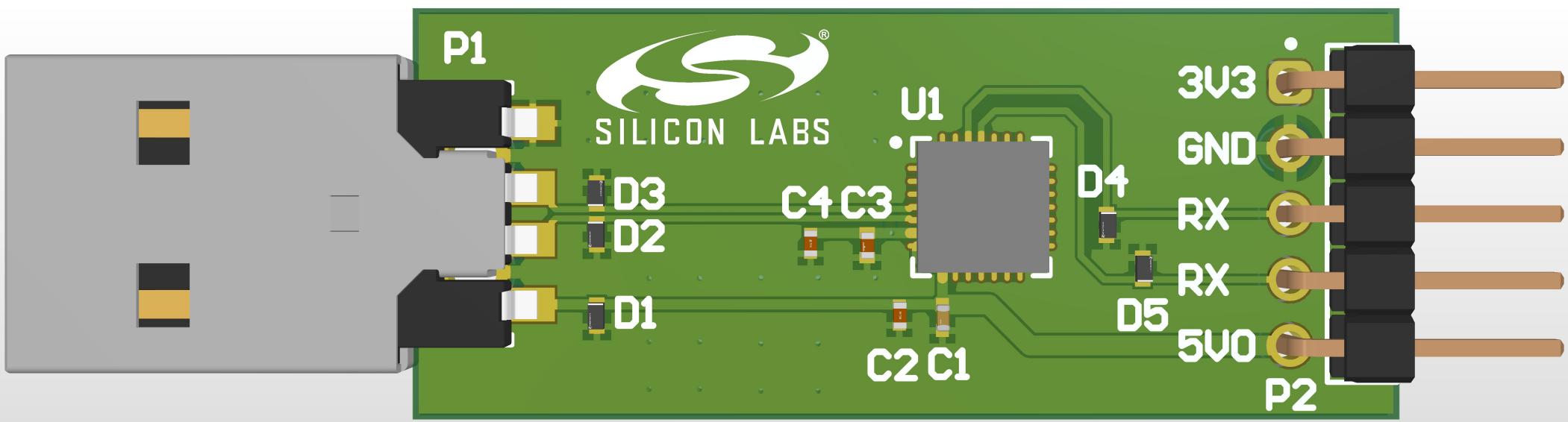


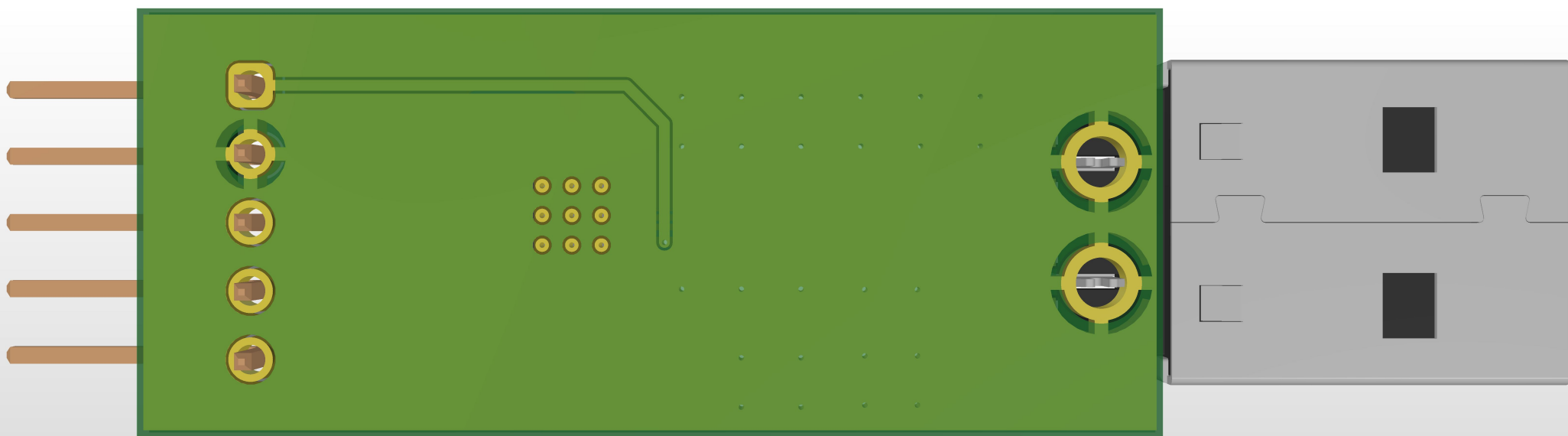
Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type
	Top Overlay			Legend
Surface Material	Top Solder	0.01mm	Solder Resist	Solder Mask
Copper	Top Layer	0.04mm		Signal
Core FR-4		1.50mm	FR-4	Dielectric
Copper	Bottom Layer	0.04mm		Signal
Surface Material	Bottom Solder	0.01mm	Solder Resist	Solder Mask
	Bottom Overlay			Legend

Total thickness: 1.59mm







## Design Rules Verification Report

Filename : D:\Altium Design Projects\CP2102\_USB\_To\_UART\CP2102\_USB\_To\_UART.Pcl

Warnings 0  
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=4mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( All )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=15.748mil) (Max=47.244mil) (Preferred=19.685mil) (InNet('VBUS'))	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=3.5mil) (All),(All)	0
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	0
Silk to Silk (Clearance=10mil) (All),(All)	0
Silk to Silk (Clearance=10mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)	0
Total	0