

# ASIC WiMax Phy: Phase 2

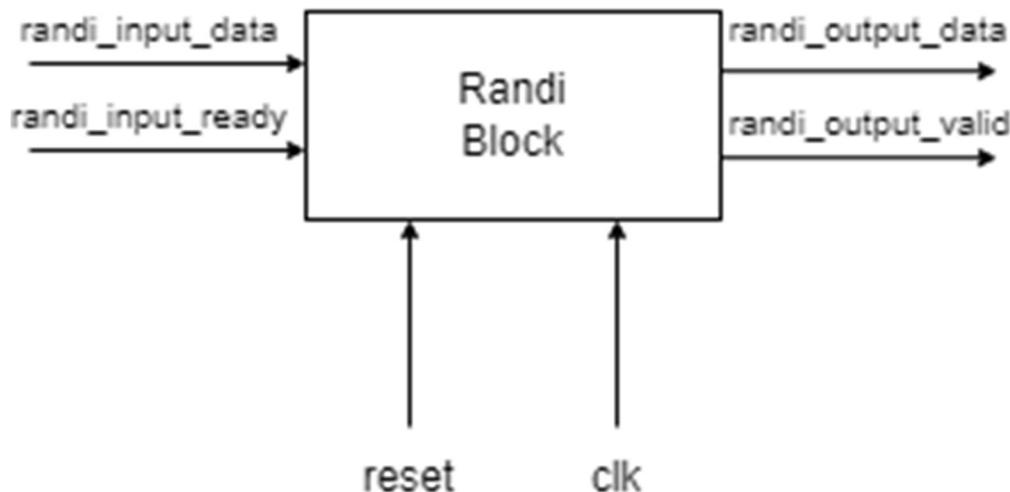
## Randomizer

Main File Name	Randi.vhd
Testbench File Name	Randi_tb.vhd

### Ports:

Signals	In/Out	Type	Width
Clk_50MHz	In	std_logic	1
Reset	In	std_logic	1
randi_input_data	In	std_logic	1
randi_input_ready	In	std_logic	1
randi_input_valid	In	std_logic	1
randi_output_valid	Out	std_logic	1
randi_output_data	Out	std_logic	1
randi_output_ready	Out	std_logic	1

### Block Diagram Sketch:

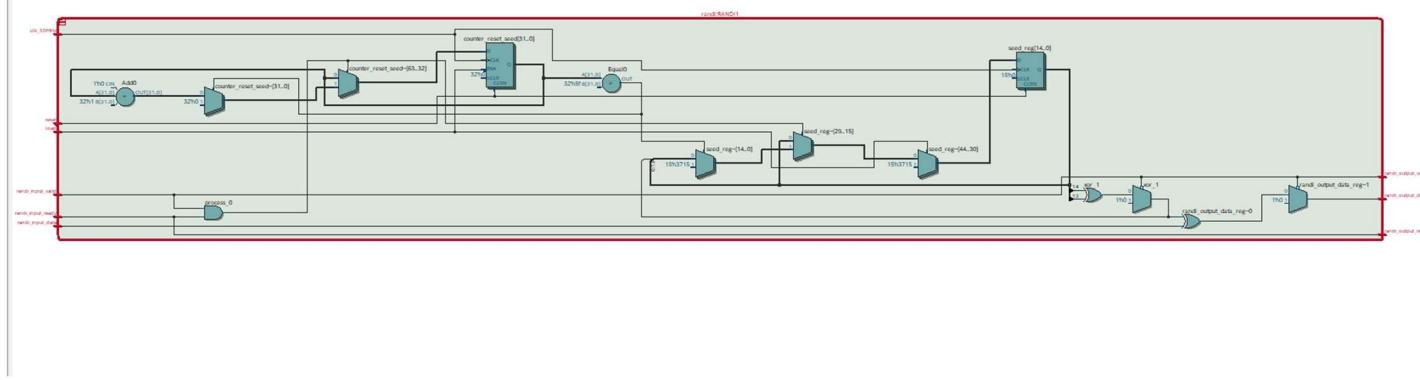


### Testing and Functionality

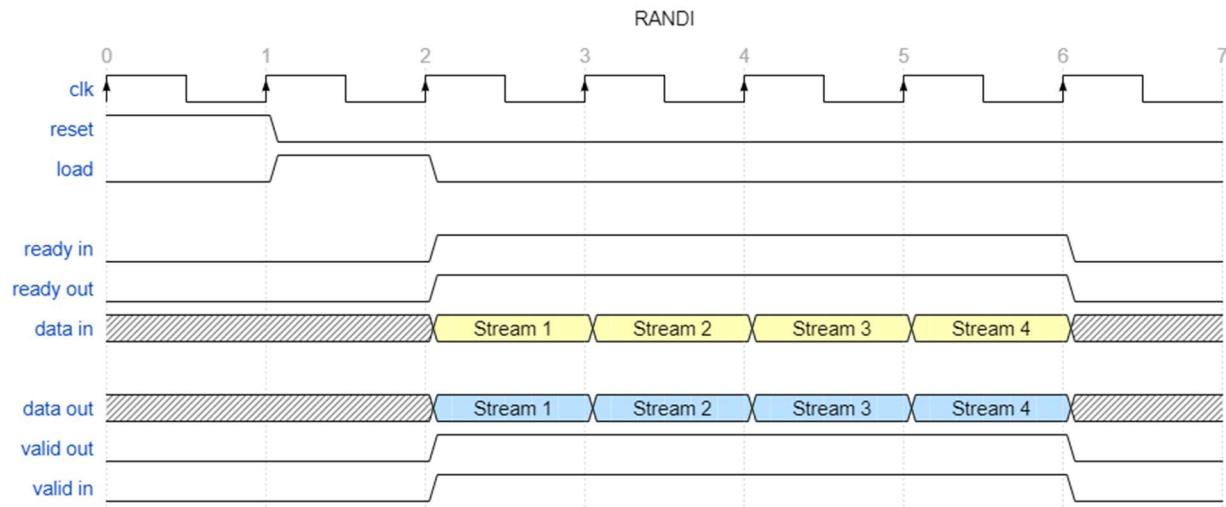
- We have tested on 2 Input streams
- We have 2x96 cycles, with a period of 20 ns = (3940 ns runtime in testbench).

- No Setup nor warm-up cycles
- Handshakes (ready and valid signals) are in phase with inputs/outputs.

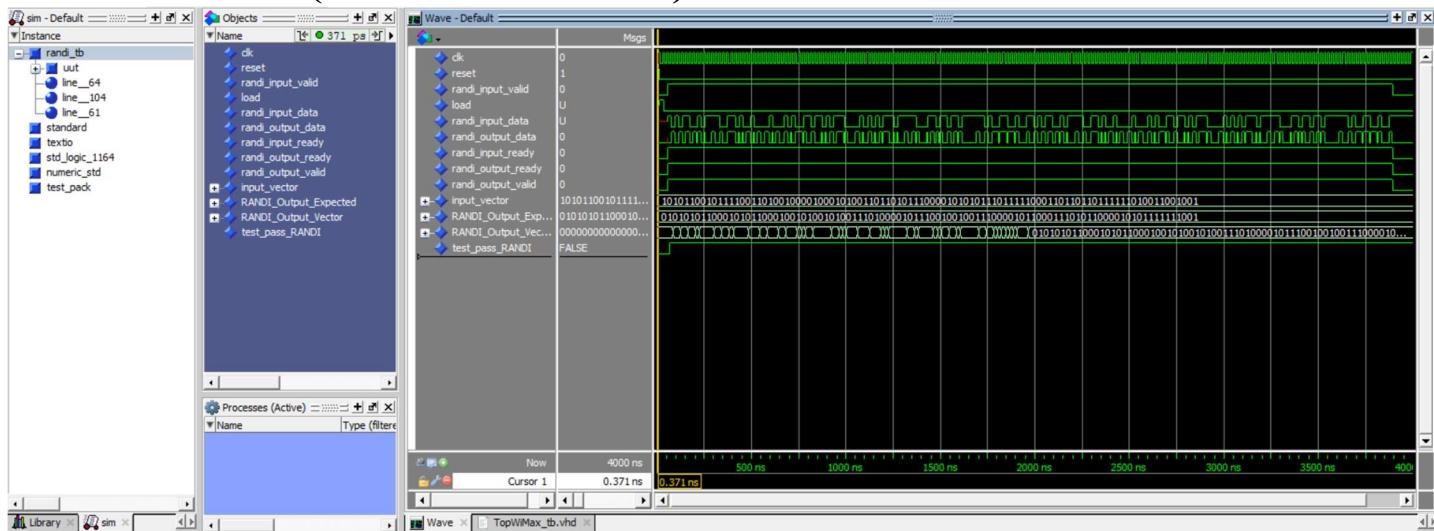
## RTL (Quartus)



## Waveform (Sketch Expect)



## Randi Results (ModelSim Altera)



## Randi Self-Check Transcript (ModelSim Altera)

```
** Note: ----- ## The Second Randomizer Input Stream
# Time: 1985 ns Iteration: 0 Instance: /randi_tb
** Note: ----- ## Done Inputting the Second stream:
# Time: 3895 ns Iteration: 0 Instance: /randi_tb
** Note: ----- Finished Inputting [2] Input Streams
# Time: 3895 ns Iteration: 0 Instance: /randi_tb
** Note: -----
# Time: 3895 ns Iteration: 0 Instance: /randi_tb
** Note: -----
# Time: 3905 ns Iteration: 0 Instance: /randi_tb
** Note: ----- ## Randomizer Second Input Stream test passed successfully
# Time: 3905 ns Iteration: 0 Instance: /randi_tb
** Note: -----
# Time: 3905 ns Iteration: 0 Instance: /randi_tb
** Note: -----
# Time: 3905 ns Iteration: 0 Instance: /randi_tb
** Note: -----
# Time: 3905 ns Iteration: 0 Instance: /randi_tb
** Note: -----
# Time: 3905 ns Iteration: 0 Instance: /randi_tb
** Note: -----Finished self checker for: RANDI Block-----
# Time: 3905 ns Iteration: 0 Instance: /randi_tb
** Note: -----
# Time: 3905 ns Iteration: 0 Instance: /randi_tb
** Note: -----
# Time: 3905 ns Iteration: 0 Instance: /randi_tb
** Note: -----
# Time: 3905 ns Iteration: 0 Instance: /randi_tb
** Note: ----- Simulation Finished
# Time: 3905 ns Iteration: 0 Instance: /randi_tb
** Note: -----
# Time: 3905 ns Iteration: 0 Instance: /randi_tb
```

VSIM 44>

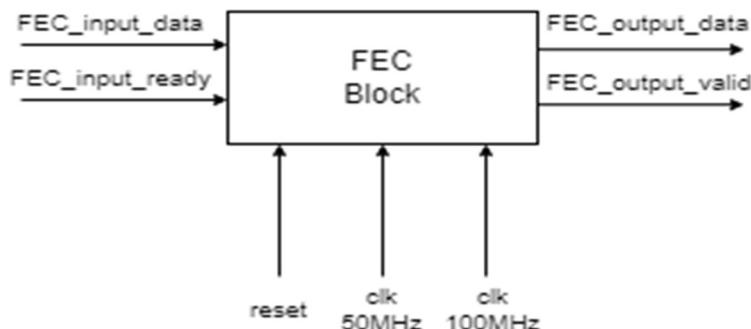
# FEC

Main File Name	FEC.vhd
Testbench File Name	FEC_tb.vhd
Extra File	FEC_RAM_2PORTS.vhd

## Ports:

Signals	In/Out	Type	Width
clk_50MHz	In	STD_LOGIC	1
clk_100MHz	In	STD_LOGIC	1
reset	In	STD_LOGIC	1
FEC_input_data	In	STD_LOGIC	1
FEC_input_ready	In	STD_LOGIC	1
FEC_input_valid	In	STD_LOGIC	1
FEC_output_ready	Out	STD_LOGIC	1
FEC_output_valid	Out	STD_LOGIC	1
FEC_output_data	Out	STD_LOGIC_VECTOR	1

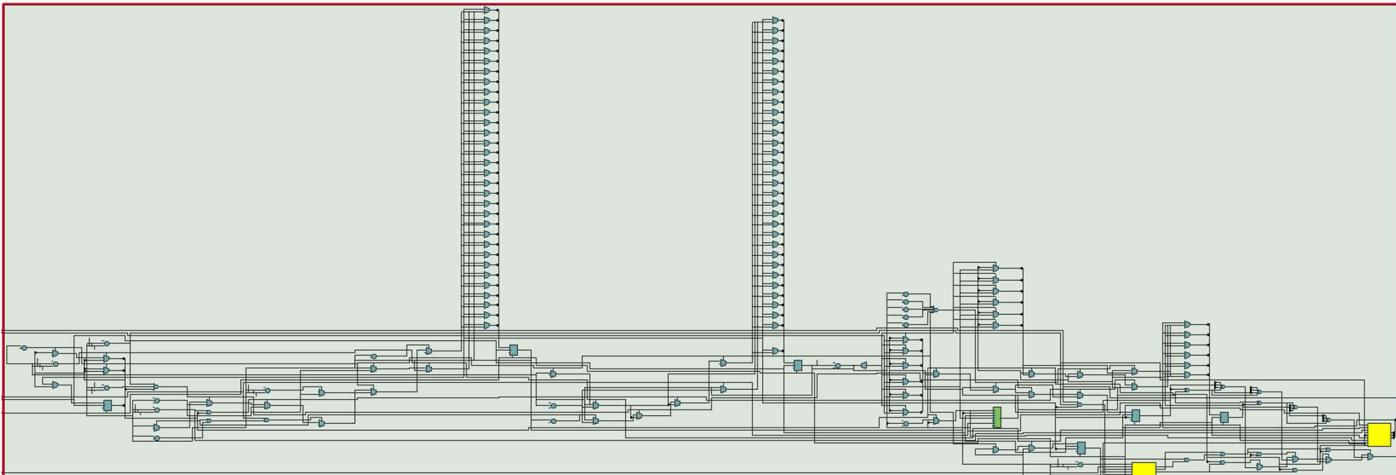
## Block Diagram Sketch:



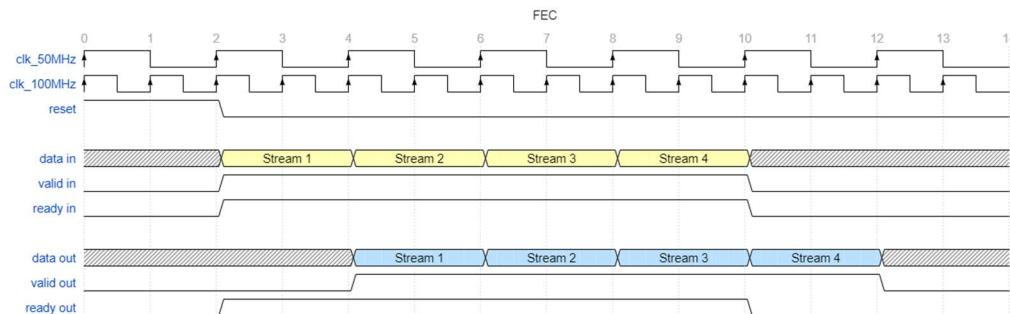
## Testing and Functionality

- 1- 5 streams of Data, around 10 us of inputting, and 10 us of outputting but delayed by 2 us. So total run time is a round 12 us.
- 2- We receive 96 data bits at 50 MHz, at period 20 ns. They are processed in parallel and sent to our PLL\_BLOCK (RAM).
- 3- Then we transmit 192 bits of data a faster rate of 100 MHz.
- 4- We need to either send or receive not both. And repeats the cycle again.

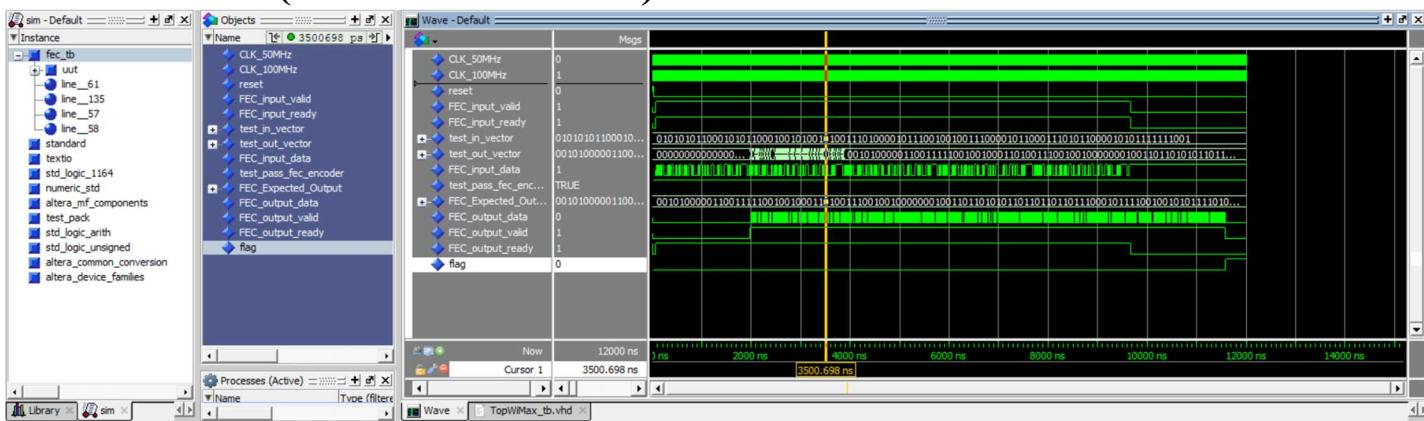
## RTL (Quartus)



## Waveform (Sketch Expect)



## FEC Results (ModelSim Altera)



## FEC Self Check (ModelSim Altera)

```
# ** Note: =====
#   Time: 7740 ns  Iteration: 0  Instance: /fec_tb
# ** Note: ----- ## The Fifth FEC Input Stream
#   Time: 7740 ns  Iteration: 0  Instance: /fec_tb
VSIM 39> run 2 us
# ** Note: =====
#   Time: 9652 ns  Iteration: 0  Instance: /fec_tb
# ** Note: ----- ## FEC Fourth Input Stream test passed Successfully
#   Time: 9652 ns  Iteration: 0  Instance: /fec_tb
# ** Note: ----- ## The Fifth FEC Input Stream
#   Time: 9652 ns  Iteration: 0  Instance: /fec_tb
# ** Note: ----- ## Done Inputting the Fifth stream:
#   Time: 9660 ns  Iteration: 0  Instance: /fec_tb
# ** Note: =====
#   Time: 9660 ns  Iteration: 0  Instance: /fec_tb
# ** Note: ----- Finishehd Inputting (5) Input Streams -----
#   Time: 9660 ns  Iteration: 0  Instance: /fec_tb
# ** Note: =====
#   Time: 9660 ns  Iteration: 0  Instance: /fec_tb
VSIM 40> run 2 us
# ** Note: =====
#   Time: 11572 ns  Iteration: 0  Instance: /fec_tb
# ** Note: ----- ## FEC Fifth Input Stream test passed Successfully
#   Time: 11572 ns  Iteration: 0  Instance: /fec_tb
# ** Note: =====
#   Time: 11572 ns  Iteration: 0  Instance: /fec_tb
# ** Note: -----Finished self checker for: FEC Block-----
#   Time: 11572 ns  Iteration: 0  Instance: /fec_tb
# ** Note: =====
#   Time: 11572 ns  Iteration: 0  Instance: /fec_tb
# ** Note: ----- Simulation Finished -----
#   Time: 11572 ns  Iteration: 0  Instance: /fec_tb
# ** Note: =====
#   Time: 11572 ns  Iteration: 0  Instance: /fec_tb
VSIM 40>
```

# Dual Port Memory

(We would change its name from PPL\_BLOCK to 2PORTSRAM in next phase).

Main File Name	PLL_main.vhd
Extra File	PLL_main_0002.v

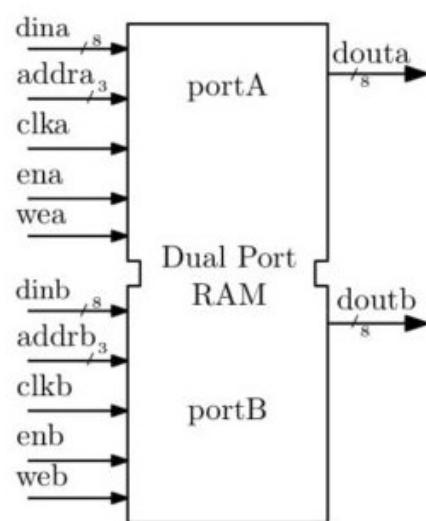
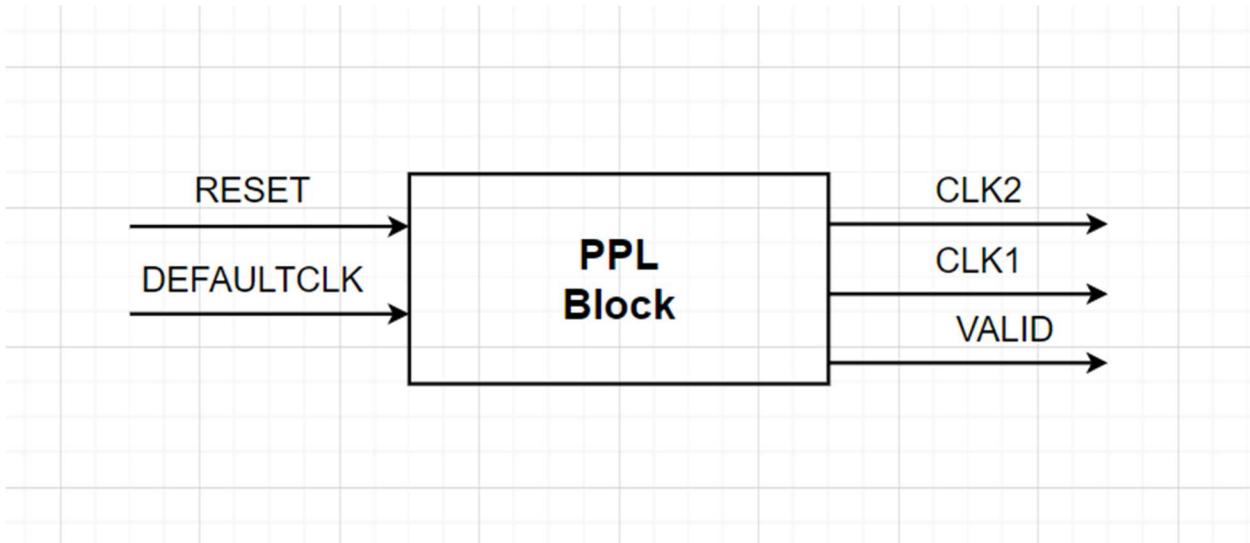


Fig.1

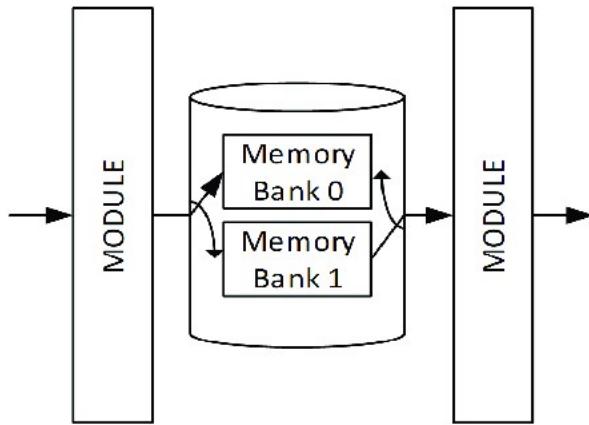


Fig 2.

Signals	In/Out	Type	Width
<b>refclk</b>	In	STD_LOGIC	1
<b>rst</b>	In	STD_LOGIC	1
<b>outclk_0</b>	Out	STD_LOGIC	1
<b>outclk_1</b>	Out	STD_LOGIC	1
<b>locked</b>	Out	STD_LOGIC	1

## Functionality

PLL take 50Mhz clock as reference, and output two clocks.

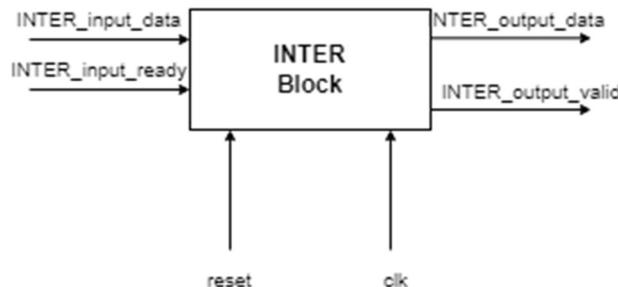
# Interleaver

Main File Name		INTER.vhd
Testbench File Name		INTER_tb.vhd
Extra File 1		INTER_RAM_2port

## Ports:

Signals	In/Out	Type	Width
INTER_Input_data	In	std_logic	1
INTER_Input_ready	In	std_logic	1
INTER_Input_valid	In	std_logic	1
Clk_100Mhz	In	std_logic	1
reset	In	std_logic	1
INTER_OUTPUT_data	Out	std_logic	1
INTER_OUTPUT_valid	out	std_logic	1
INTER_OUTPUT_ready	out	std_logic	1

## Block Diagram Sketch:

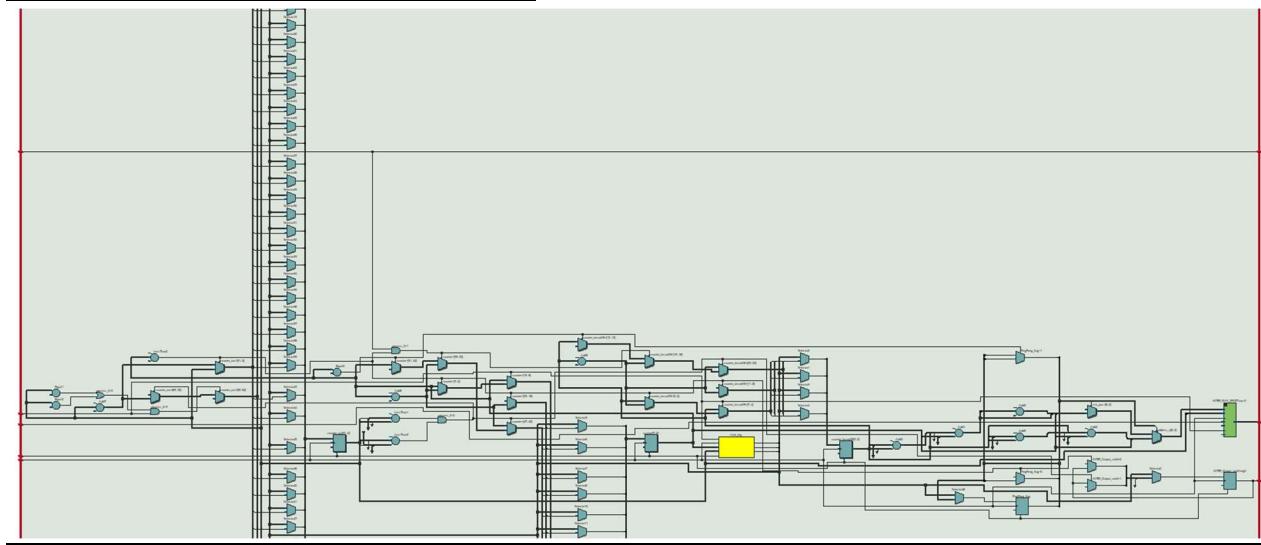


## Testing and Functionality

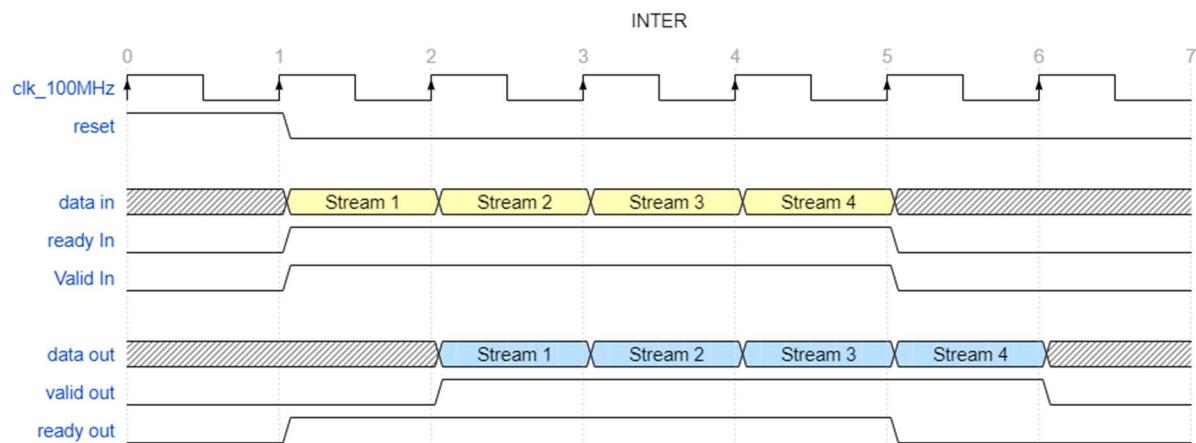
- 4 Input Streams, 2 us for each input. And 8 us for output streams, but shifted by 1 phase cycle. Thus total run time is 10 us.
- For INTER, input data is Parallel, then wires permeate the input, then output it serially
- Total delay of the block is  $n+2$  (where  $n$  is the number of cycles) ... and this two is mainly from shifting and loading.
-

# RTL (Quartus)

## 1- RTL OF INTER (MAIN BLOCK)

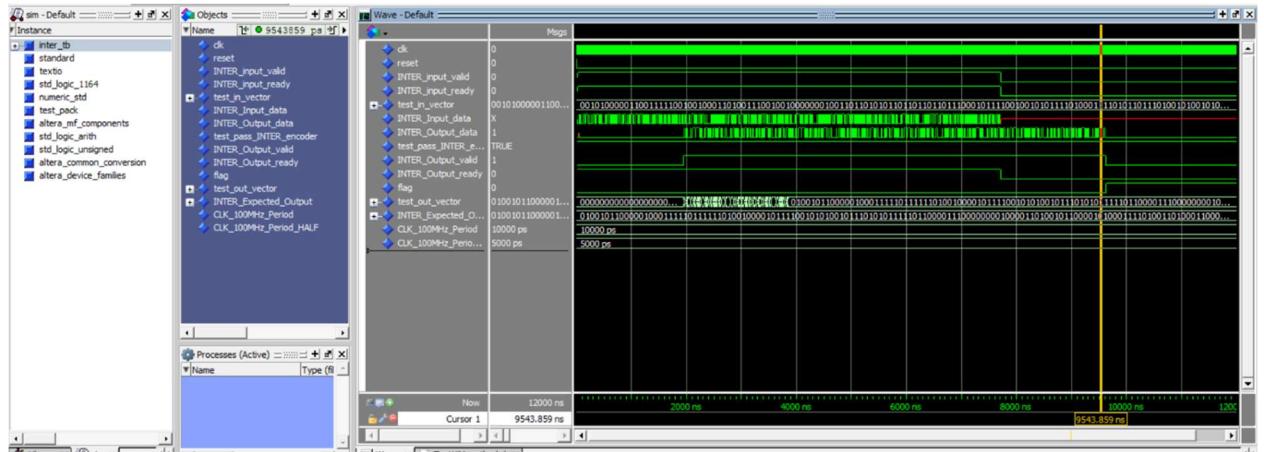


## WaveForm (Sketch Expect)



# Results (ModelSim Altera)

## 1- RESULTS INTER



## 2- INTER Self Check

```
Transcript
*** Note: ----- ## The Fourth INTER Input Stream
# Time: 5790 ns Iteration: 0 Instance: /inter_tb
*** Note: -----
# Time: 7707 ns Iteration: 0 Instance: /inter_tb
*** Note: ----- ## INTER Third Input Stream test passed Successfully
# Time: 7707 ns Iteration: 0 Instance: /inter_tb
*** Note: -----
# Time: 7707 ns Iteration: 0 Instance: /inter_tb
*** Note: ----- ## The Fourth INTER Input Stream
# Time: 7707 ns Iteration: 0 Instance: /inter_tb
*** Note: ----- ## Done Inputting the Fourth stream:
# Time: 7710 ns Iteration: 0 Instance: /inter_tb
*** Note: -----
# Time: 7710 ns Iteration: 0 Instance: /inter_tb
*** Note: ----- Finished Inputting (4) Input Streams
# Time: 7710 ns Iteration: 0 Instance: /inter_tb
*** Note: -----
# Time: 7710 ns Iteration: 0 Instance: /inter_tb
*** Note: -----
# Time: 9627 ns Iteration: 0 Instance: /inter_tb
*** Note: ----- ## INTER Fourth Input Stream test passed Successfully
# Time: 9627 ns Iteration: 0 Instance: /inter_tb
*** Note: -----
# Time: 9627 ns Iteration: 0 Instance: /inter_tb
*** Note: -----Finished self checker for: INTER Block
# Time: 9627 ns Iteration: 0 Instance: /inter_tb
*** Note: -----
# Time: 9627 ns Iteration: 0 Instance: /inter_tb
*** Note: -----
# Time: 9627 ns Iteration: 0 Instance: /inter_tb
*** Note: ----- Simulation Finished
# Time: 9627 ns Iteration: 0 Instance: /inter_tb
*** Note: -----
# Time: 9627 ns Iteration: 0 Instance: /inter_tb
*** Note: -----
```

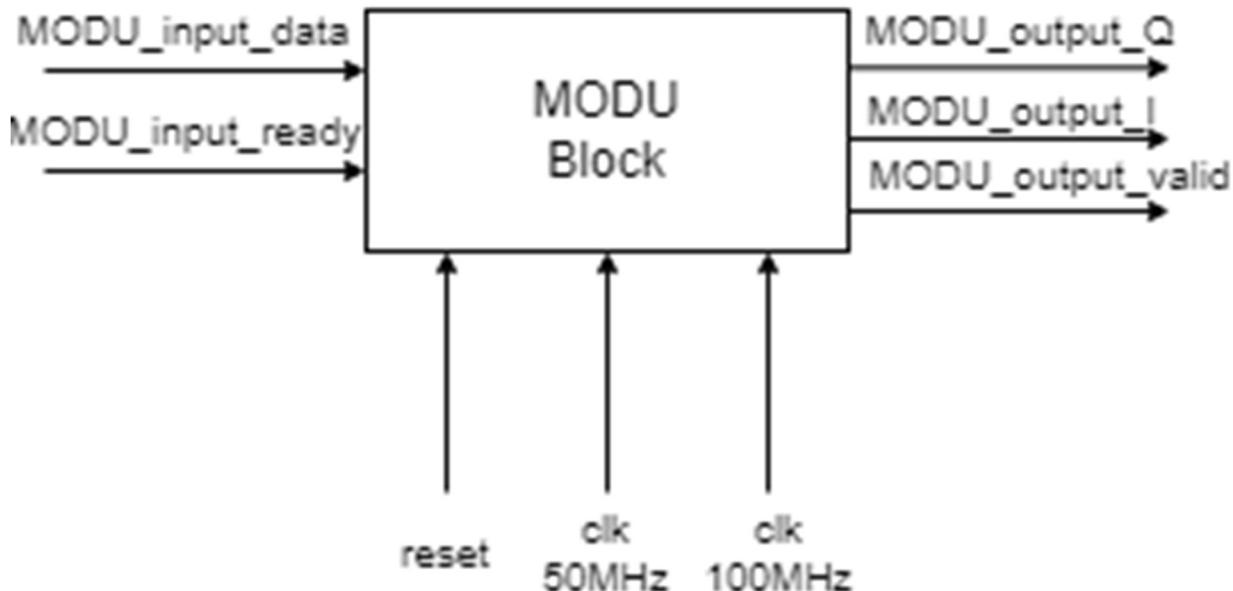
# Modulation

Main File Name	MODU.vhd
Testbench File Name	MODU_tb.vhd

## Ports:

Signals	In/Out	Type	Width
MODU_input_data	In	std_logic	1
MODU_input_ready	In	std_logic	1
MODU_input_valid	In	std_logic	1
clk_100MHz	In	std_logic	1
clk_50MHz	In	std_logic	1
reset	In	std_logic	1
MODU_output_valid	Out	std_logic	1
MODU_output_ready	Out	std_logic	1
MODU_output_Q	Out	std_logic_vector	16
MODU_output_I	Out	std_logic_vector	16

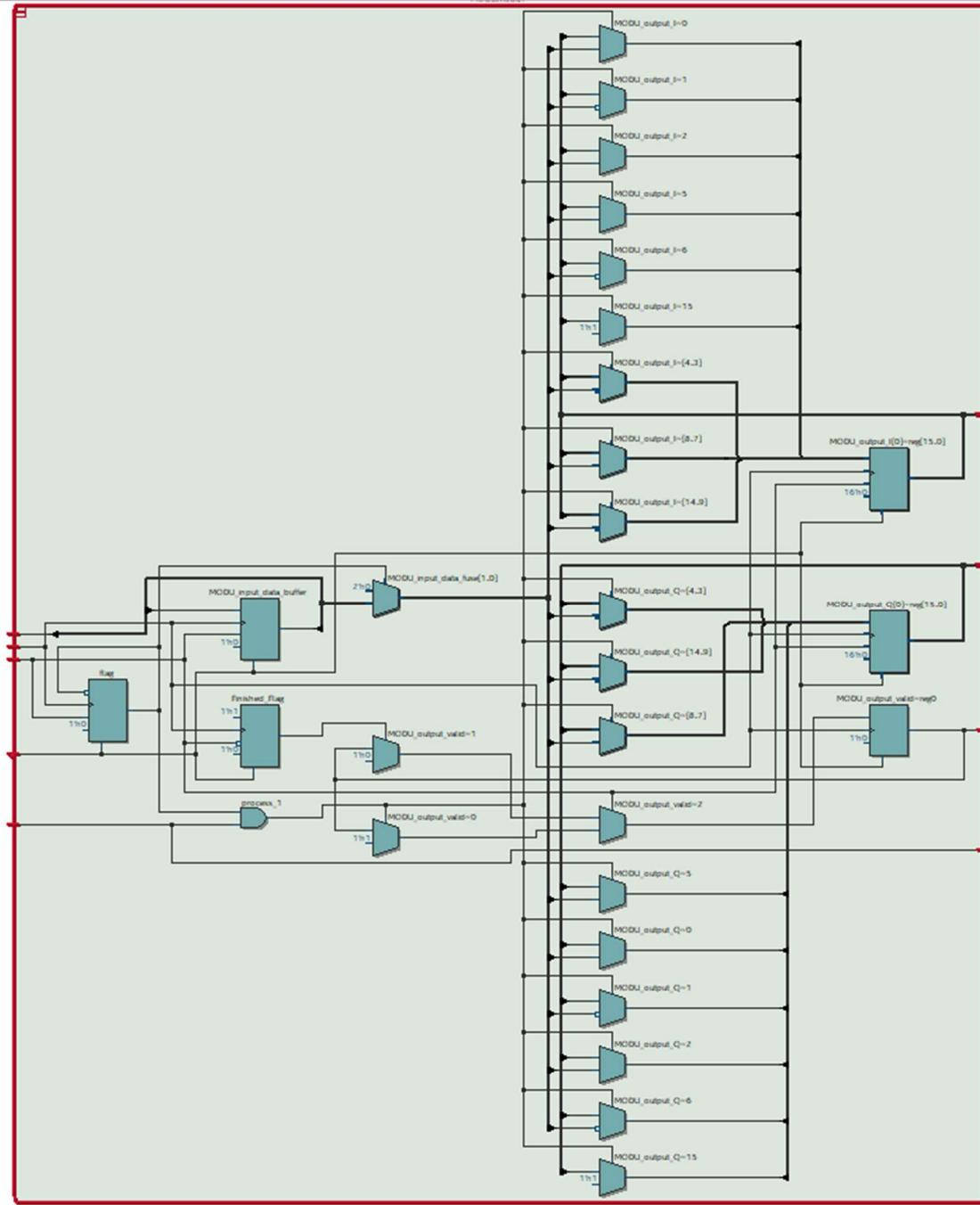
## Block Diagram Sketch:



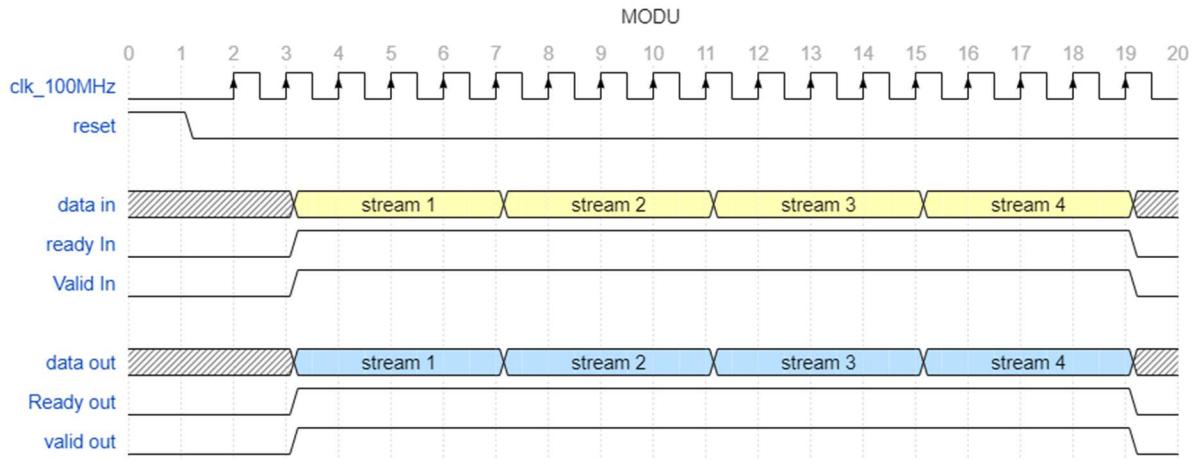
## **Testing and Functionality**

- 2 inputs streams. Total runtime of around 4 us.
- Again, we use 100MHz for output and 50MHz for inputs.
  - For handshaking, we have some delay to allow data to arrive as serial inputs (let's say late by x cycles).
  - The total time needed is  $n + x$  ( where n might be calculated as  $192 * 8$ ).

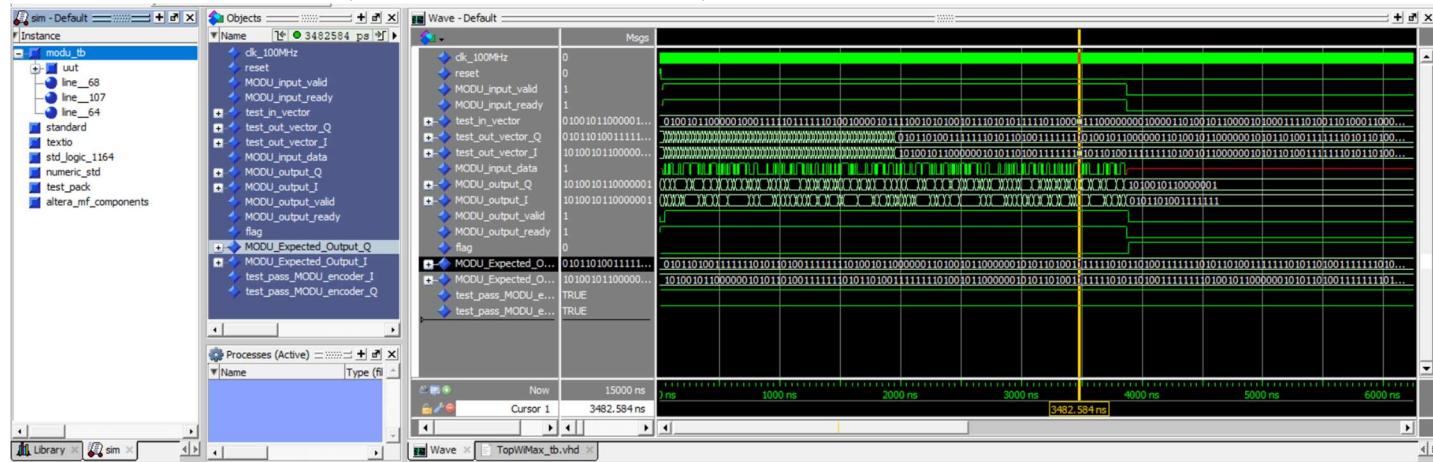
## RTL (Quartus)



## Waveform (Sketch Expect)



## MODU Results (ModelSim Altera)



# MODU Self Check (ModelSim Altera)

The screenshot shows the ModelSim Altera interface with the following details:

- Menu Bar:** File, Edit, View, Compile, Simulate, Add, Structure, Tools, Layout, Bookmarks, Window, Help.
- Toolbars:** Standard toolbar with icons for file operations, zoom, and simulation controls.
- Object Manager:** Shows "sim - Default" and "Objects - Default".
- Waveform Viewer:** Shows "Wave - Default" with a waveform for "TopWiMax\_tb.vhd".
- Script Editor:** Transcript window showing simulation log output.
- Log Output:** Transcript window content:

```
# ** Note: ----- ### Ended Checking MODU First Output stream
# Time: 1966536 ps Iteration: 0 Instance: /modu_tb
# ** Note: -----
# Time: 1966536 ps Iteration: 0 Instance: /modu_tb
# ** Note: ----- ### Started Checking MODU Second Output stream:
# Time: 1966536 ps Iteration: 0 Instance: /modu_tb
# ** Note: ----- ## Done Inputting MODU the Second stream:
# Time: 3870 ns Iteration: 0 Instance: /modu_tb
# ** Note: ----- Finishehd Inputting MODU (2) Input Streams -----
# Time: 3870 ns Iteration: 0 Instance: /modu_tb
# ** Note: -----
# Time: 3870 ns Iteration: 0 Instance: /modu_tb
# ** Note: ----- ## Second MODU Output Stream: 1536 Q Values Successed
# Time: 3888072 ps Iteration: 0 Instance: /modu_tb
# ** Note: -----
# Time: 3888072 ps Iteration: 0 Instance: /modu_tb
# ** Note: ----- ## Second MODU Output Stream: 1536 I Values Successed
# Time: 3888072 ps Iteration: 0 Instance: /modu_tb
# ** Note: -----
# Time: 3888072 ps Iteration: 0 Instance: /modu_tb
# ** Note: ----- ## Ended Checking MODU Second Output stream
# Time: 3888072 ps Iteration: 0 Instance: /modu_tb
# ** Note: -----
# Time: 3888072 ps Iteration: 0 Instance: /modu_tb
# ** Note: ----- Ended MODU Checking (Demodulating) (2) output streams -----
# Time: 3888072 ps Iteration: 0 Instance: /modu_tb
# ** Note: -----
# Time: 3888072 ps Iteration: 0 Instance: /modu_tb
# ** Note: ----- Simulation Finished -----
# Time: 3888072 ps Iteration: 0 Instance: /modu_tb
# ** Note: -----
# Time: 3888072 ps Iteration: 0 Instance: /modu_tb
```

VSIM 50>

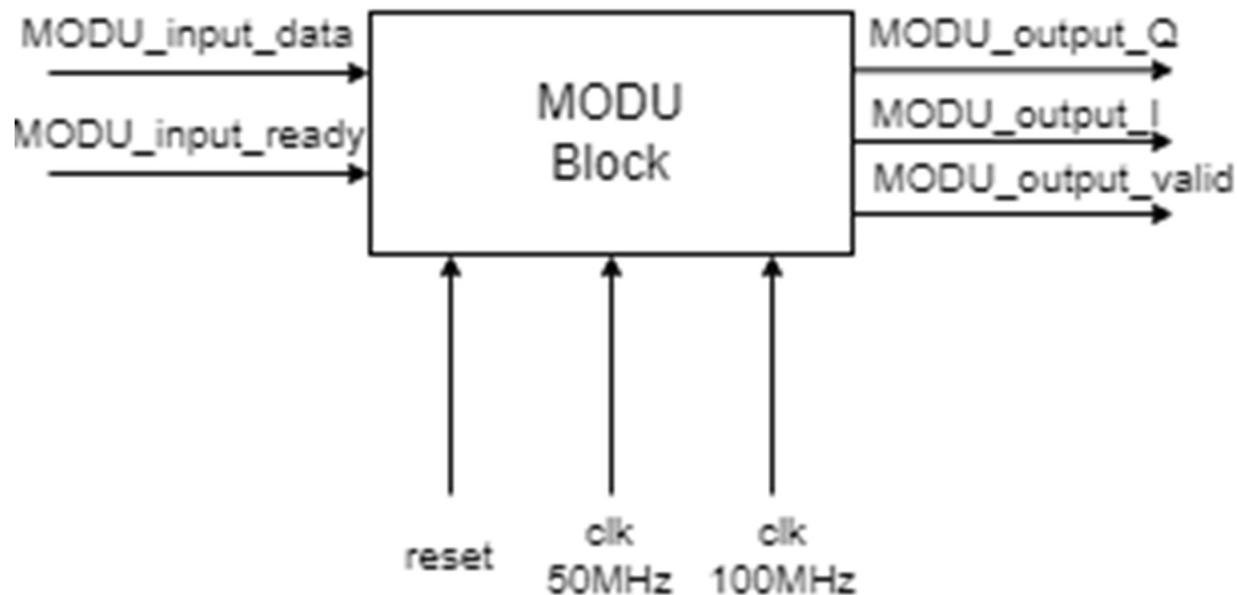
# TopWiMax

Main File Name	TopWiMax.vhd
Testbench File Name	TopWiMax_tb.vhd

## Ports:

Signals	In/Out	Type	Width
WiInput	In	std_logic	1
TopWiMax_in_ready	In	std_logic	1
TopWiMax_in_valid	In	std_logic	1
load	In	std_logic	1
clk_50MHz	In	std_logic	1
reset	In	std_logic	1
TopWiMax_out_valid	Out	std_logic	1
TopWiMax_out_ready	Out	std_logic	1
WiOutput1	Out	std_logic_vector	16
WiOutput2	Out	std_logic_vector	16

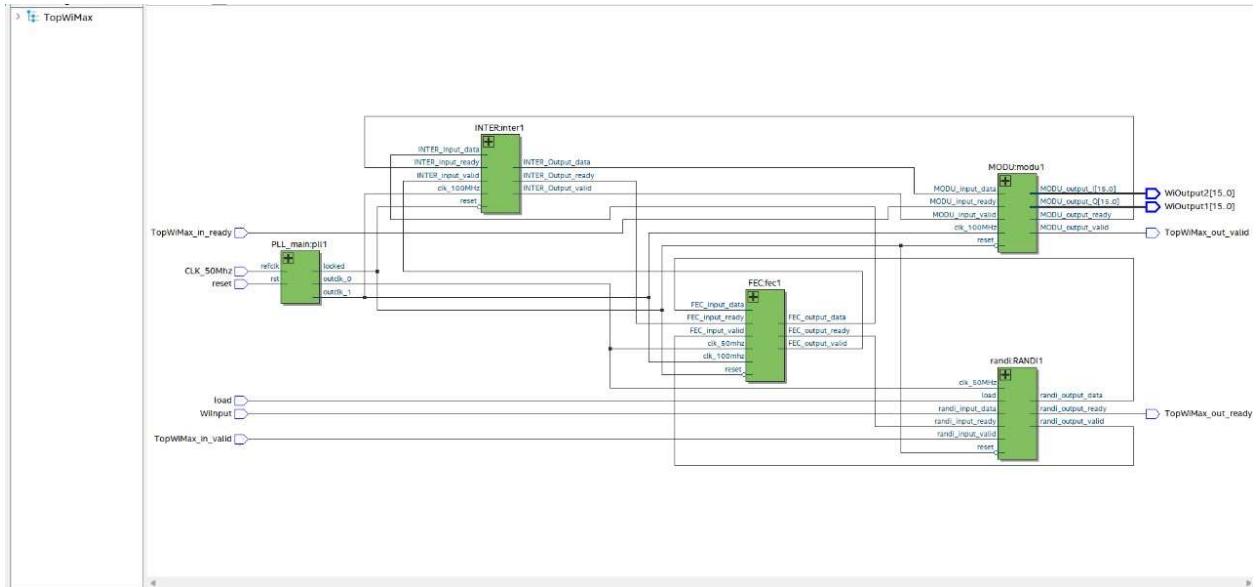
## Block Diagram Sketch:



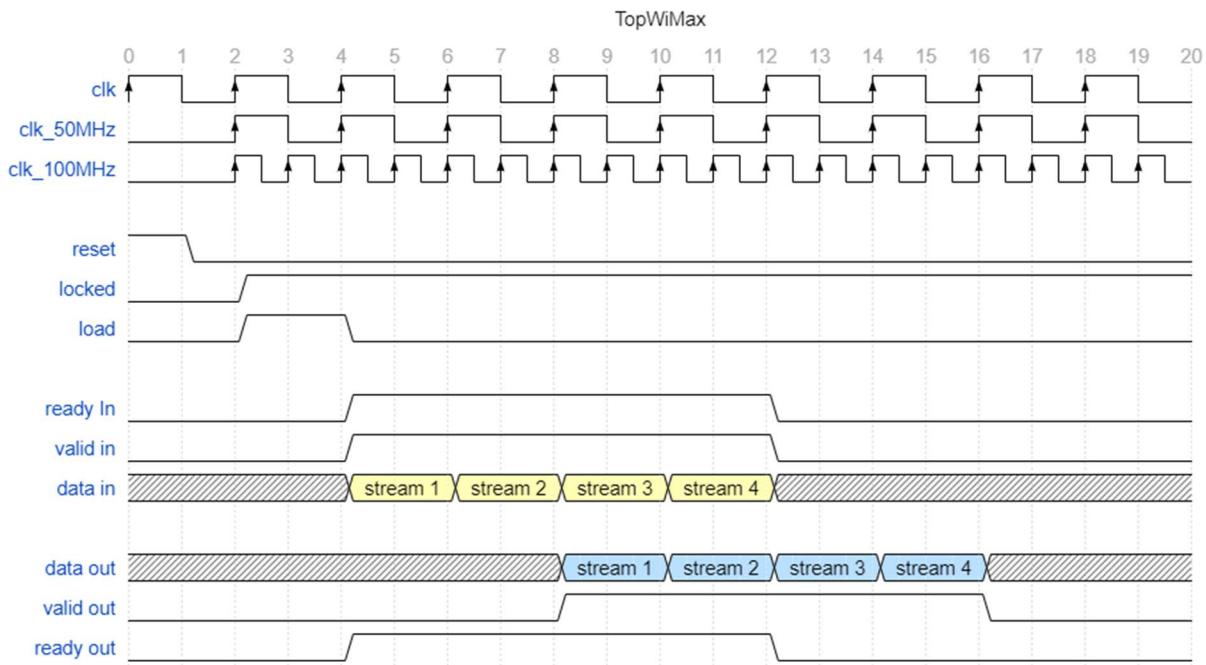
# Testing and Functionality

- 2 inputs streams. Total runtime of around 4 us.
- Again, we use 100MHz for output and 50MHz for inputs.
  - For handshaking, we have some delay to allow data to arrive as serial inputs (let's say late by x cycles).
  - The total time needed is n +x ( where n might be calculated as 192\*8).

## RTL (Quartus)



## Waveform (Sketch Expect)



# Top Module Results (ModelSim Altera)



# **MODU Self Check (ModelSim Altera)**

```
sim - Default ----- Objects ----- Wave - Default
Memory List sim How To? Wave TopWiMax_tb.vhd

Transcript
# Note: -----
# Time: 11595 ns Iteration: 0 Instance: /topwimax_tb
# Note: -----FINISHED SELF CHECKER-----
Time: 11595 ns Iteration: 0 Instance: /topwimax_tb
# Note: -----
# Time: 11595 ns Iteration: 0 Instance: /topwimax_tb
# Note: -----
# Time: 11595 ns Iteration: 0 Instance: /topwimax_tb
# Note: *** Fourth MDDU Output Stream: 1536 Q Values Successed
Time: 11618144 ps Iteration: 0 Instance: /topwimax_tb
# Note: -----
# Time: 11618144 ps Iteration: 0 Instance: /topwimax_tb
# Note: *** Fourth MDDU Output Stream: 1536 I Values Successed
Time: 11618144 ps Iteration: 0 Instance: /topwimax_tb
# Note: -----
# Time: 11618144 ps Iteration: 0 Instance: /topwimax_tb
# Note: *** Ended Checking MDDU Fourth Output stream
Time: 11618144 ps Iteration: 0 Instance: /topwimax_tb
# Note: -----
# Time: 11618144 ps Iteration: 0 Instance: /topwimax_tb
# Note: ----- Ended Checking (Demodulating) (4) output streams
Time: 11618144 ps Iteration: 0 Instance: /topwimax_tb
# Note: -----
# Time: 11618144 ps Iteration: 0 Instance: /topwimax_tb
# Note: ----- Stimulation of All Blocks Passed Successfully!!
Time: 11618144 ps Iteration: 0 Instance: /topwimax_tb
# Note: -----
# Time: 11618144 ps Iteration: 0 Instance: /topwimax_tb
# Note: ----- Simulation Finished
Time: 11618144 ps Iteration: 0 Instance: /topwimax_tb
# Note: -----
# Time: 11618144 ps Iteration: 0 Instance: /topwimax_tb
# Note: -----
# Time: 11618144 ps Iteration: 0 Instance: /topwimax_tb
```

# **MODU Self Check (ModelSim Altera) (With Error Injected)**

```
sim - Default ---+ Objects ---+ Wave - Default ---+  
Memory List sim | Now | Wave | TopWMax_tb.vhd |  
  
Transcript  
# ** Note:  
# Time: 11595 ns Iteration: 0 Instance: /topwmax_tb  
# ** Note: -----FINISHED SELF CHECKER-----  
# Time: 11595 ns Iteration: 0 Instance: /topwmax_tb  
# ** Note:  
# Time: 11595 ns Iteration: 0 Instance: /topwmax_tb  
# ** Note: ----- ## Fourth MODU Output Stream: 1536 Q Values Failed  
# Time: 11618144 ps Iteration: 0 Instance: /topwmax_tb  
# ** Note:  
# Time: 11618144 ps Iteration: 0 Instance: /topwmax_tb  
# ** Note: ----- ## Fourth MODU Output Stream: 1536 I Values failed  
# Time: 11618144 ps Iteration: 0 Instance: /topwmax_tb  
# ** Note:  
# Time: 11618144 ps Iteration: 0 Instance: /topwmax_tb  
# ** Note: ----- ## Ended Checking MODU Fourth Output stream  
# Time: 11618144 ps Iteration: 0 Instance: /topwmax_tb  
# ** Note:  
# Time: 11618144 ps Iteration: 0 Instance: /topwmax_tb  
# ** Note: ----- Ended Checking (Demodulating) (4) output streams -----  
# Time: 11618144 ps Iteration: 0 Instance: /topwmax_tb  
# ** Note:  
# Time: 11618144 ps Iteration: 0 Instance: /topwmax_tb  
# ** Note:  
# Time: 11618144 ps Iteration: 0 Instance: /topwmax_tb  
# ** Note: ----- Stimulation of one or more blocks failed!! -----  
# Time: 11618144 ps Iteration: 0 Instance: /topwmax_tb  
# ** Note:  
# Time: 11618144 ps Iteration: 0 Instance: /topwmax_tb  
# ** Note:  
# Time: 11618144 ps Iteration: 0 Instance: /topwmax_tb  
# ** Note: ----- Simulation Finished -----  
# Time: 11618144 ps Iteration: 0 Instance: /topwmax_tb  
# ** Note:  
# Time: 11618144 ps Iteration: 0 Instance: /topwmax_tb  
  
VSM3 74>
```

