## ASIC WiMax Phy: Phase 2

## Randomizer

|  |  |
| --- | --- |
| **Main File Name** | **Randi.vhd** |
| **Testbench File Name** | **Randi\_tb.vhd** |

### Ports:

|  |  |  |  |
| --- | --- | --- | --- |
| Signals | In/Out | Type | Width |
| Clk\_50MHz | In | std\_logic | 1 |
| Reset | In | std\_logic | 1 |
| randi\_input\_data | In | std\_logic | 1 |
| randi\_input\_ready | In | std\_logic | 1 |
| randi\_input\_valid | In | std\_logic | 1 |
| randi\_output\_valid | Out | std\_logic | 1 |
| randi\_output\_data | Out | std\_logic | 1 |
| randi\_output\_ready | Out | std\_logic | 1 |

### Block Diagram Sketch:

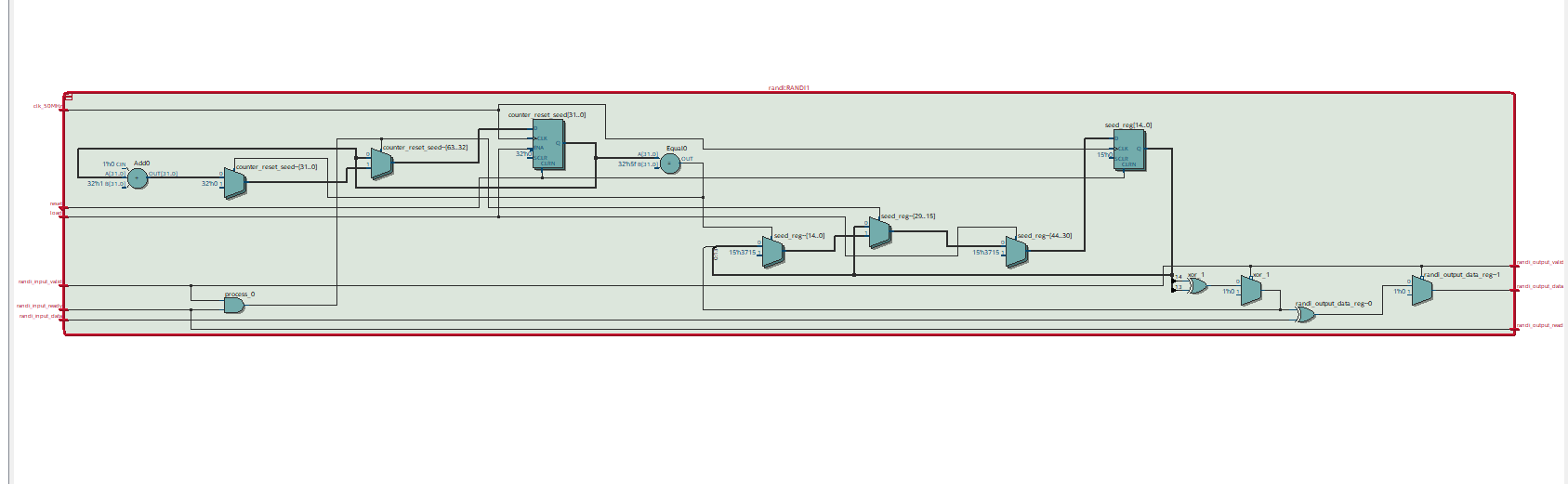
A black background with a black square

Description automatically generated with medium confidence

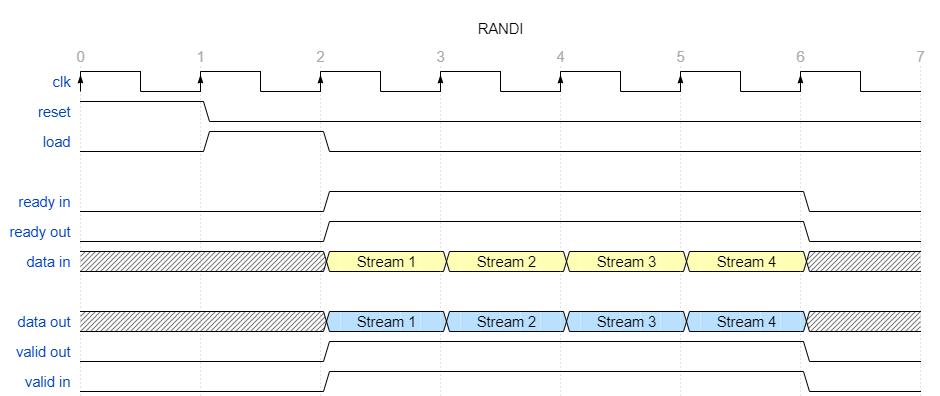
### Testing and Functionality

* We have tested on 2 Input streams
* We have 2x96 cycles, with a period of 20 ns = (3940 ns runtime in testbench).
* No Setup nor warm-up cycles
* Handshakes (ready and valid signals) are in phase with inputs/outputs.

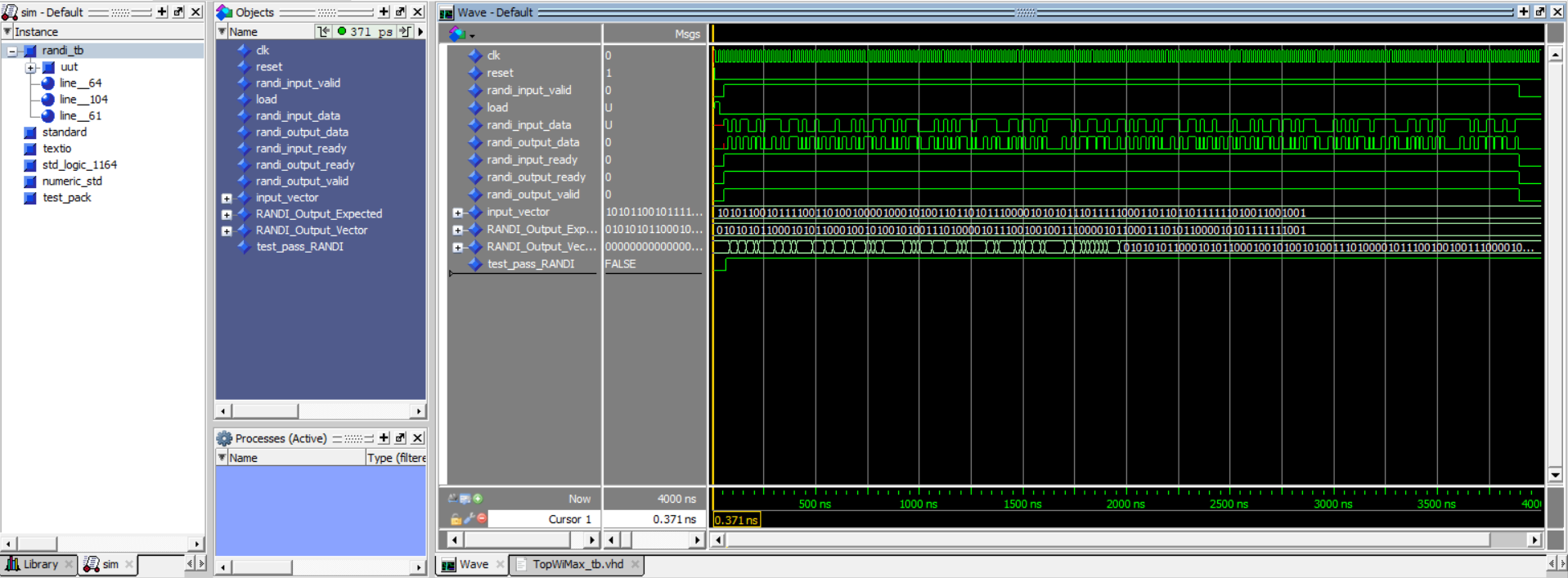
### RTL (Quartus)



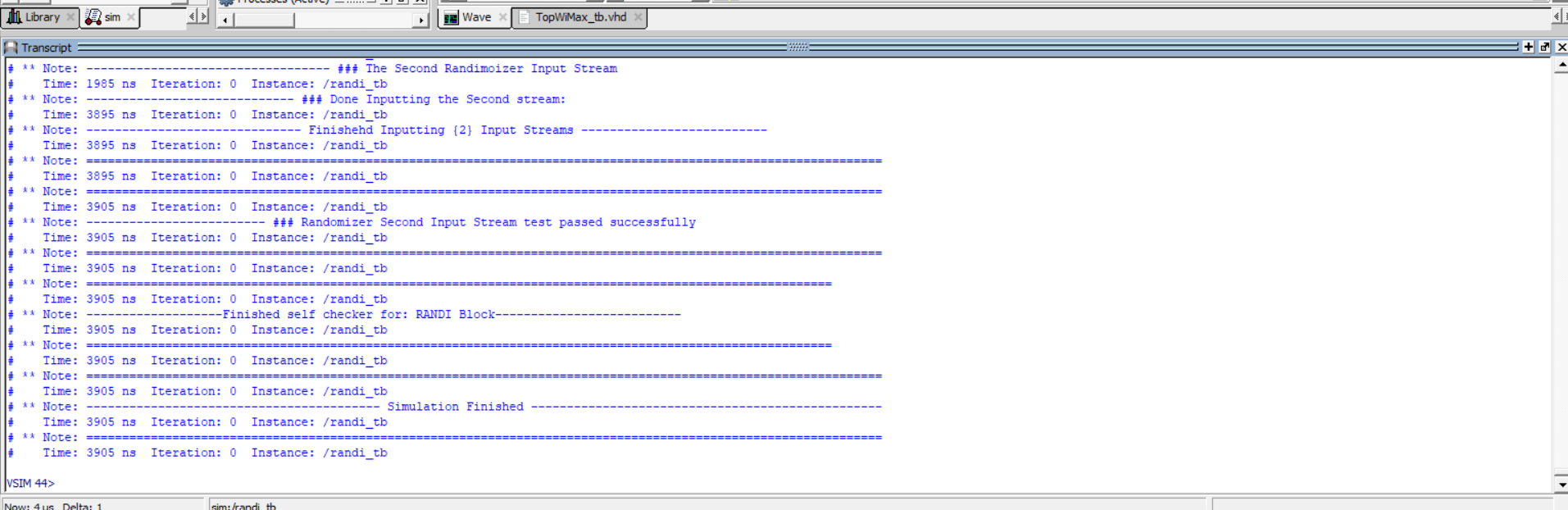
### Waveform (Sketch Expect)



### Randi Results (ModelSim Altera)



### Randi Self-Check Transcript (ModelSim Altera)



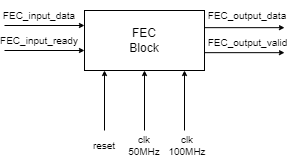
## FEC

|  |  |
| --- | --- |
| **Main File Name** | **FEC.vhd** |
| **Testbench File Name** | **FEC\_tb.vhd** |
| **Extra File** | **FEC\_RAM\_2PORTS.vhd** |

### Ports:

|  |  |  |  |
| --- | --- | --- | --- |
| Signals | In/Out | Type | Width |
| clk\_50MHz | In | STD\_LOGIC | 1 |
| clk\_100MHz | In | STD\_LOGIC | 1 |
| reset | In | STD\_LOGIC | 1 |
| FEC\_input\_data | In | STD\_LOGIC | 1 |
| FEC\_input\_ready | In | STD\_LOGIC | 1 |
| FEC\_input\_valid | In | STD\_LOGIC | 1 |
| FEC\_output\_ready | Out | STD\_LOGIC | 1 |
| FEC\_output\_valid | Out | STD\_LOGIC | 1 |
| FEC\_output\_data | Out | STD\_LOGIC\_VECTOR | 1 |

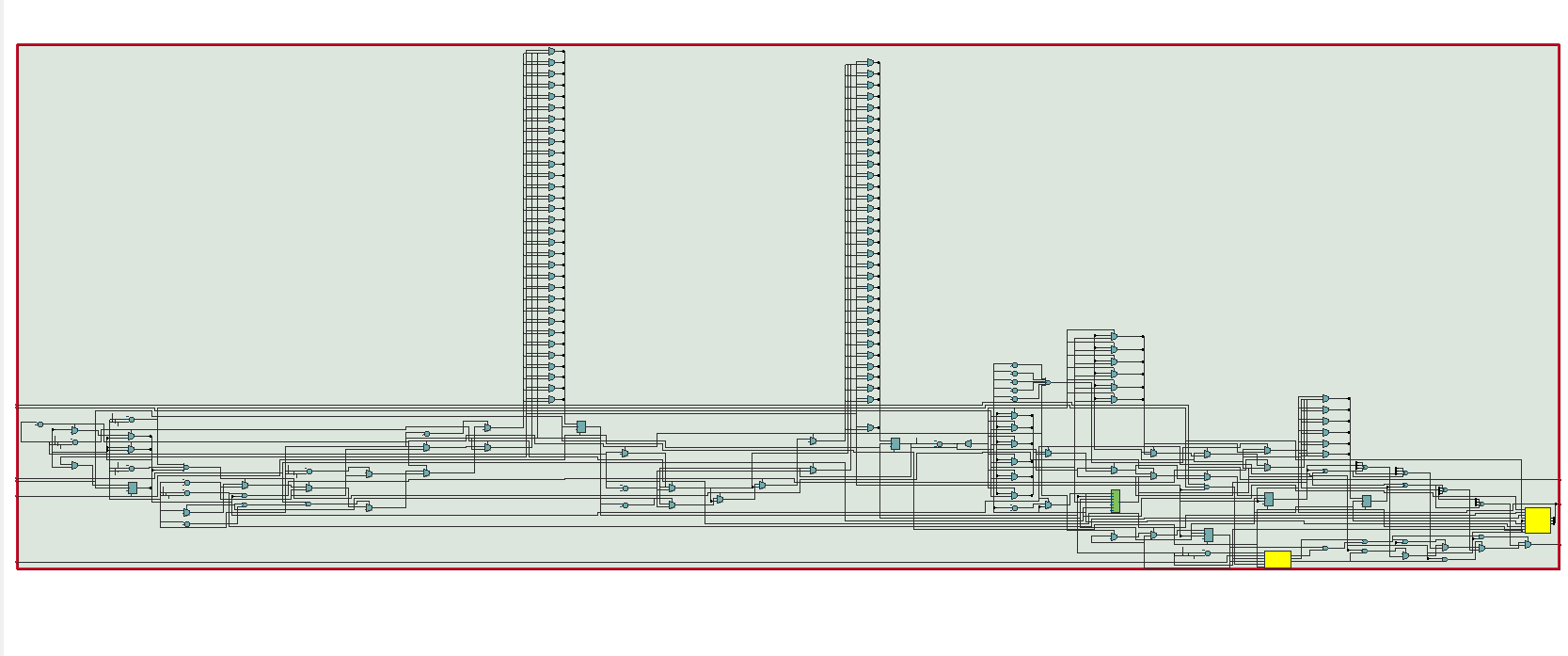
### Block Diagram Sketch:



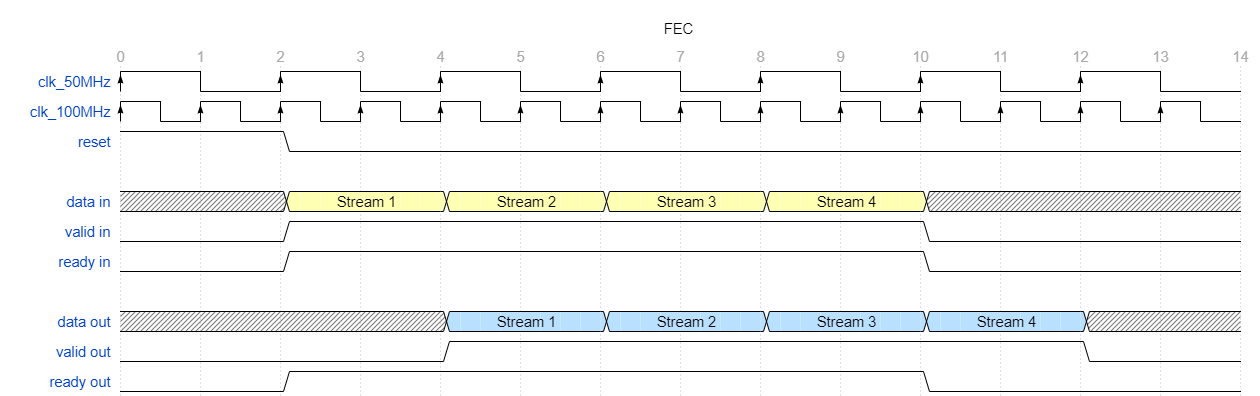
### Testing and Functionality

1. 5 streams of Data, around 10 us of inputting, and 10 us of outputting but delayed by 2 us. So total run time is a round 12 us.
2. We receive 96 data bits at 50 MHz, at period 20 ns. They are processed in parallel and sent to our PLL\_BLOCK (RAM).
3. Then we transmit 192 bits of data a faster rate of 100 MHz.
4. We need to either send or receive not both. And repeats the cycle again.

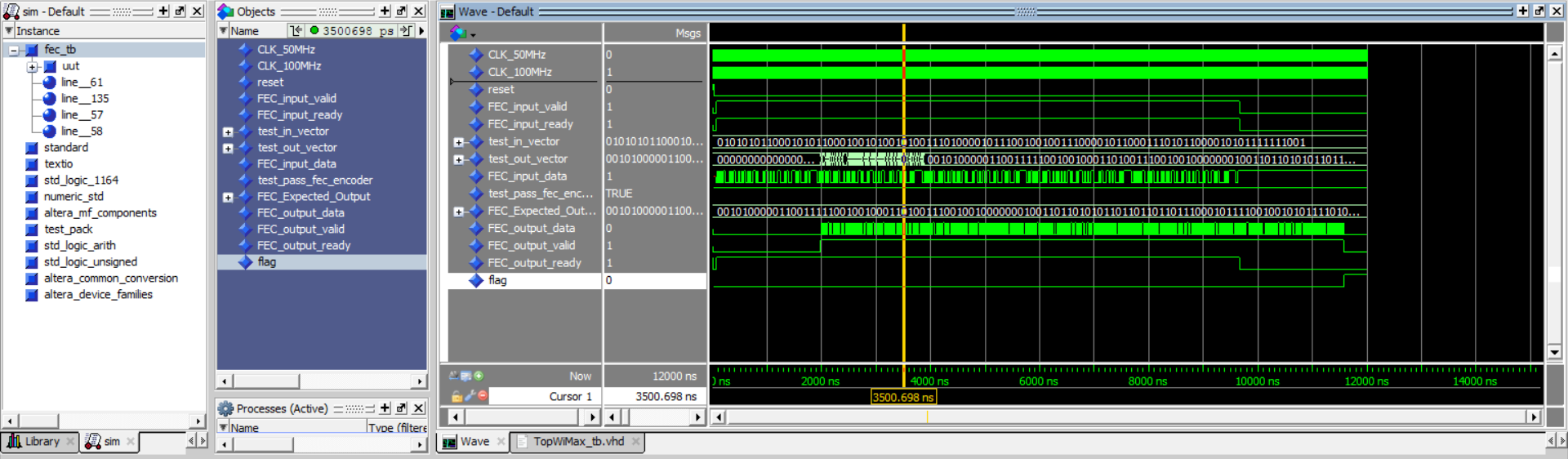
### RTL (Quartus)



### Waveform (Sketch Expect)



### FEC Results (ModelSim Altera)



### FEC Self Check (ModelSim Altera)



## Dual Port Memory

## (We would change its name from PPL\_BLOCK to 2PORTSRAM in next phase).

|  |  |
| --- | --- |
| **Main File Name** | **PLL\_main.vhd** |
| **Extra File** | **PLL\_main\_0002.v** |

A diagram of a block

Description automatically generated

## A diagram of a dual port ram Description automatically generated

Fig.1

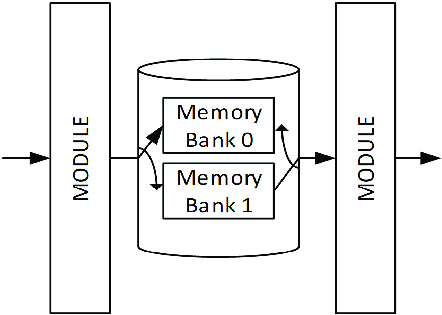


Fig 2.

|  |  |  |  |
| --- | --- | --- | --- |
| Signals | In/Out | Type | Width |
| refclk | In | STD\_LOGIC | 1 |
| rst | In | STD\_LOGIC | 1 |
| outclk\_0 | Out | STD\_LOGIC | 1 |
| outclk\_1 | Out | STD\_LOGIC | 1 |
| locked | Out | STD\_LOGIC | 1 |

**Functionality**

PLL take 50Mhz clock as reference, and output two clocks.

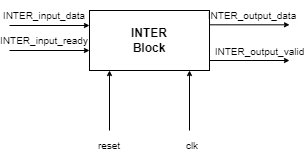
## Interleaver

|  |  |  |
| --- | --- | --- |
| **Main File Name** |  | **INTER.vhd** |
| **Testbench File Name** |  | **INTER\_tb.vhd** |
| **Extra File 1** |  | **INTER\_RAM\_2port** |

### Ports:

|  |  |  |  |
| --- | --- | --- | --- |
| Signals | In/Out | Type | Width |
| INTER\_INput\_data | **In** | std\_logic | 1 |
| INTER\_INput\_ready | **In** | std\_logic | 1 |
| INTER\_INput\_valid | **In** | std\_logic | 1 |
| Clk\_100Mhz | **In** | std\_logic | 1 |
| reset | **In** | std\_logic | 1 |
| INTER\_OUTput\_data | **Out** | std\_logic | 1 |
| INTER\_OUTput\_valid | **out** | std\_logic | 1 |
| INTER\_OUTput\_ready | **out** | std\_logic | 1 |

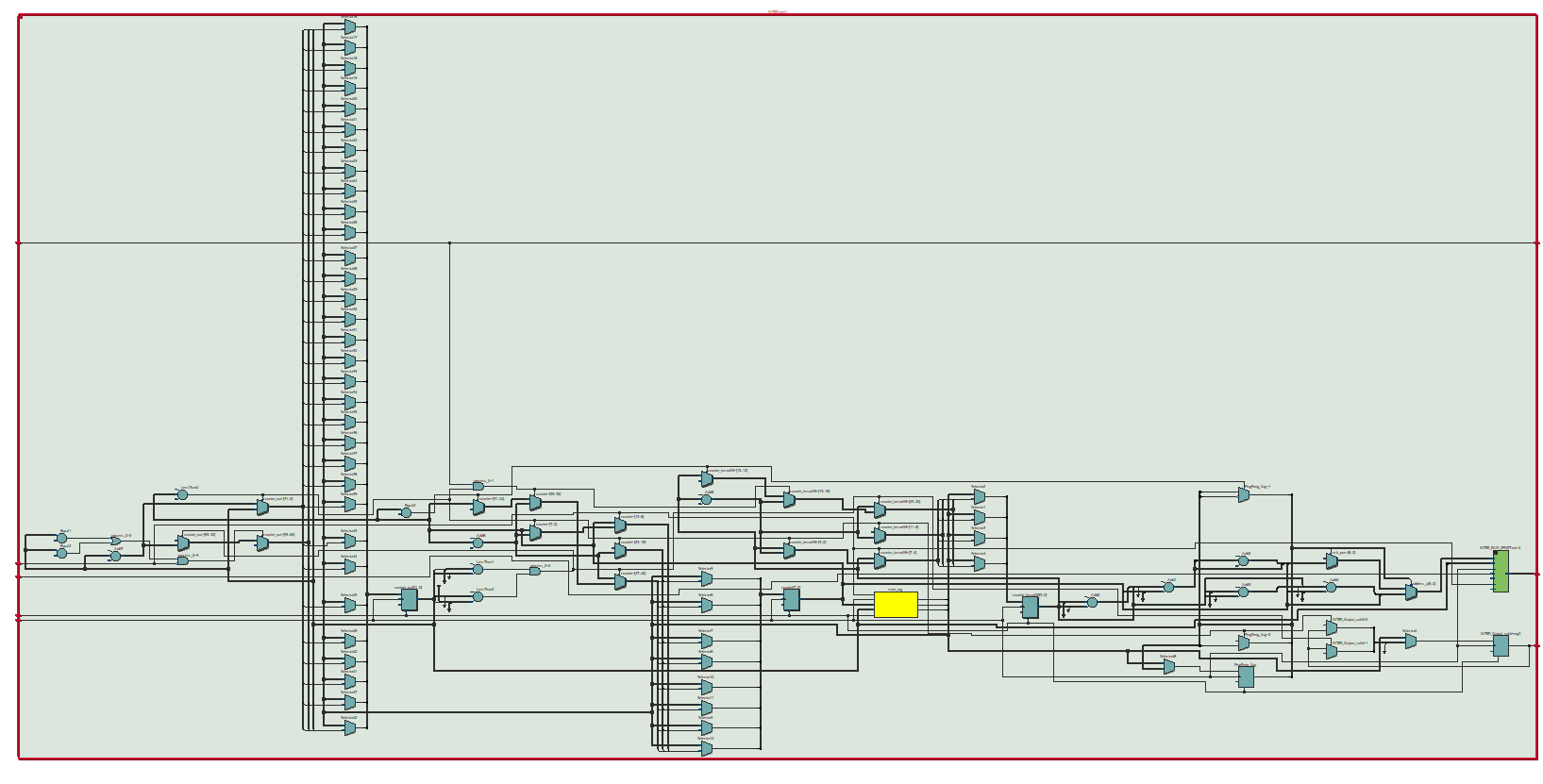
### Block Diagram Sketch:



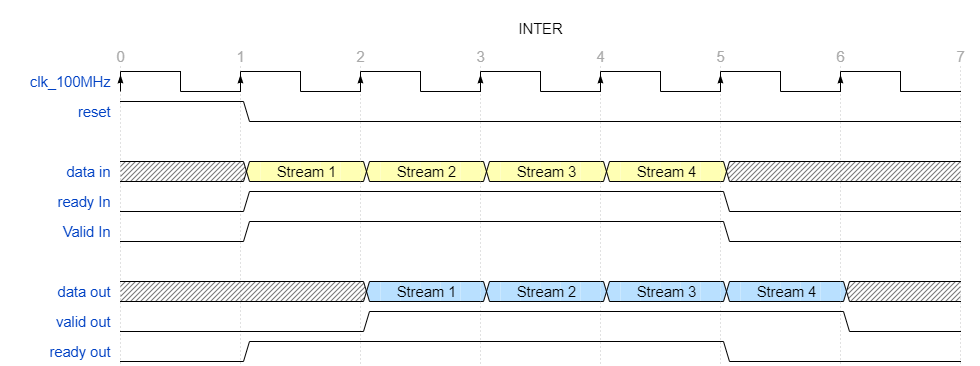
### Testing and Functionality

* 4 Input Streams, 2 us for each input. And 8 us for output streams, but shifted by 1 phase cycle. Thus total run time is 10 us.
* For INTER, input data is Parellel, then wires permeate the input, then output it serially
* Total delay of the block is n+2 (where n is the number of cycles) … and this two is mainly from shifting and loading.

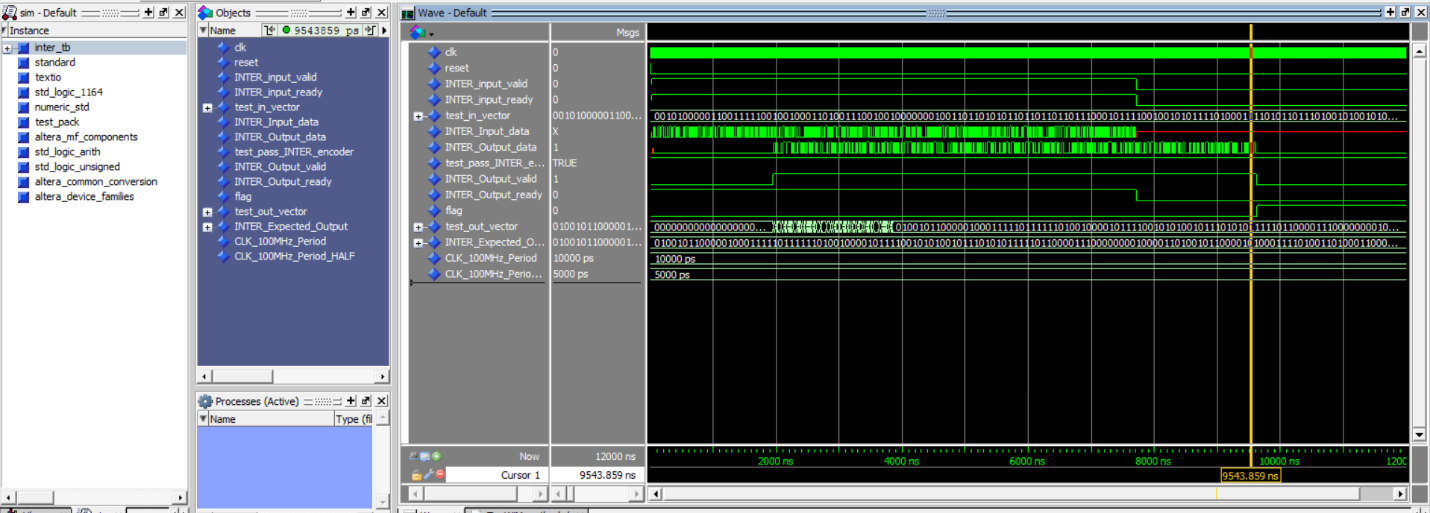
### RTL (Quartus)

1. **RTL OF INTER (MAIN BLOCK)  
   **

### WaveForm (Sketch Expect)



### Results (ModelSim Altera)

1. **RESULTS INTER** 
2. **INTER Self Check** 

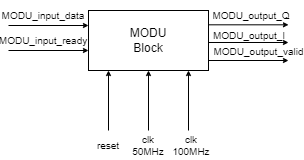
## Modulation

|  |  |
| --- | --- |
| **Main File Name** | **MODU.vhd** |
| **Testbench File Name** | **MODU\_tb.vhd** |

### Ports:

|  |  |  |  |
| --- | --- | --- | --- |
| Signals | In/Out | Type | Width |
| MODU\_input\_data | In | std\_logic | 1 |
| MODU\_input\_ready | In | std\_logic | 1 |
| MODU\_input\_valid | In | std\_logic | 1 |
| clk\_100MHz | In | std\_logic | 1 |
| clk\_50MHz | In | std\_logic | 1 |
| reset | In | std\_logic | 1 |
| MODU\_output\_valid | Out | std\_logic | 1 |
| MODU\_output\_ready | Out | std\_logic | 1 |
| MODU\_output\_Q | Out | std\_logic\_vector | 16 |
| MODU\_output\_I | Out | std\_logic\_vector | 16 |

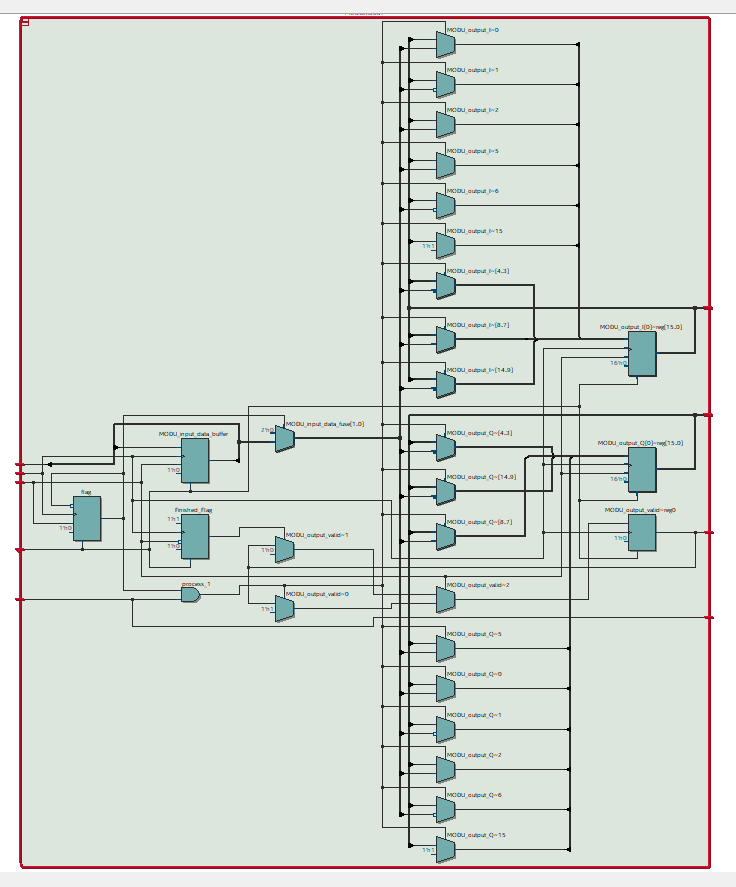
### Block Diagram Sketch:



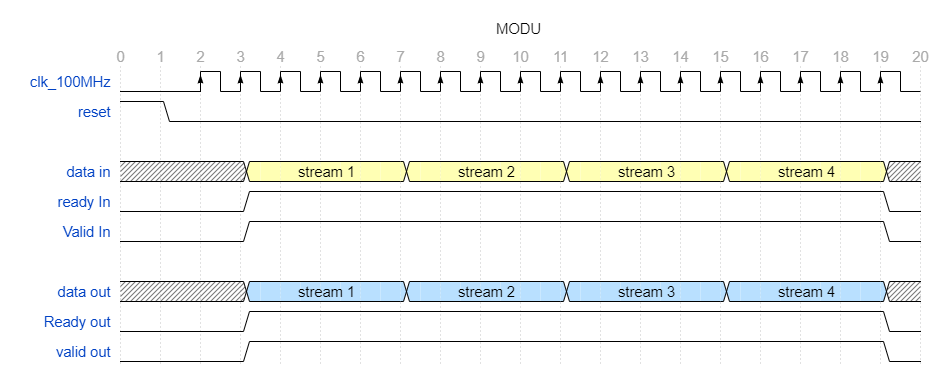
### Testing and Functionality

* ⁠2 inputs streams. Total runtime of around 4 us.
* Again, we use 100MHz for output and 50MHz for inputs.  
  - For handshaking, we have some delay to allow data to arrive as serial inputs (let’s say late by x cycles).   
  - The total time needed is n +x ( where n might be calculated as 192\*8).

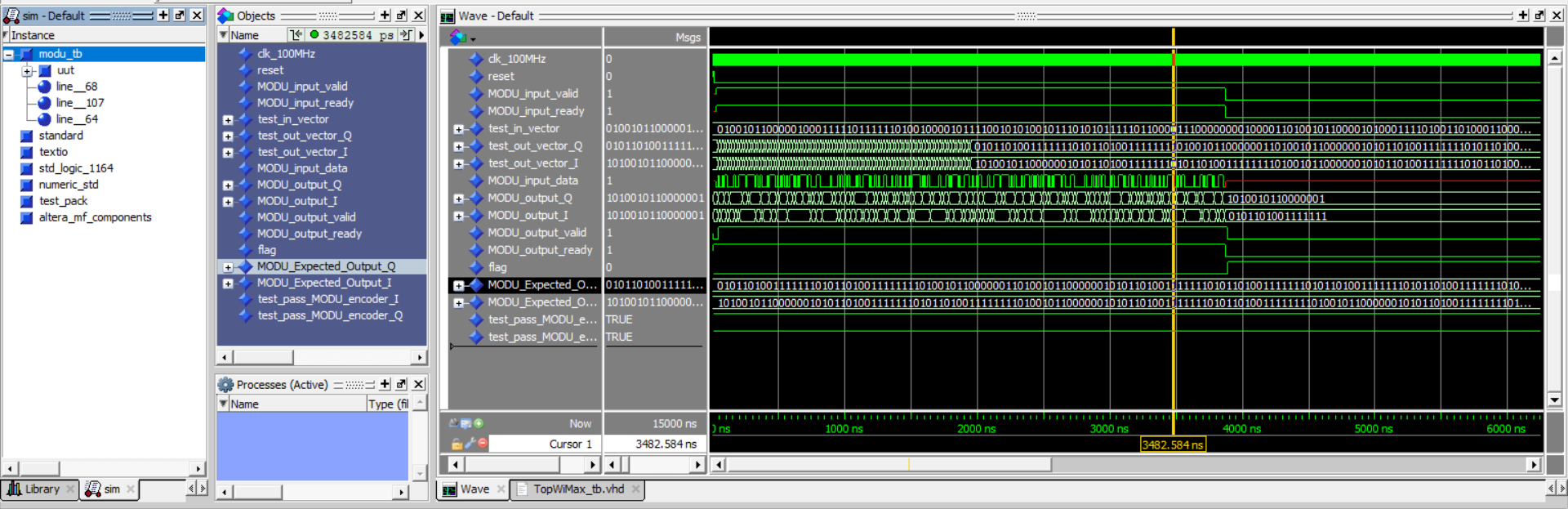
### RTL (Quartus)



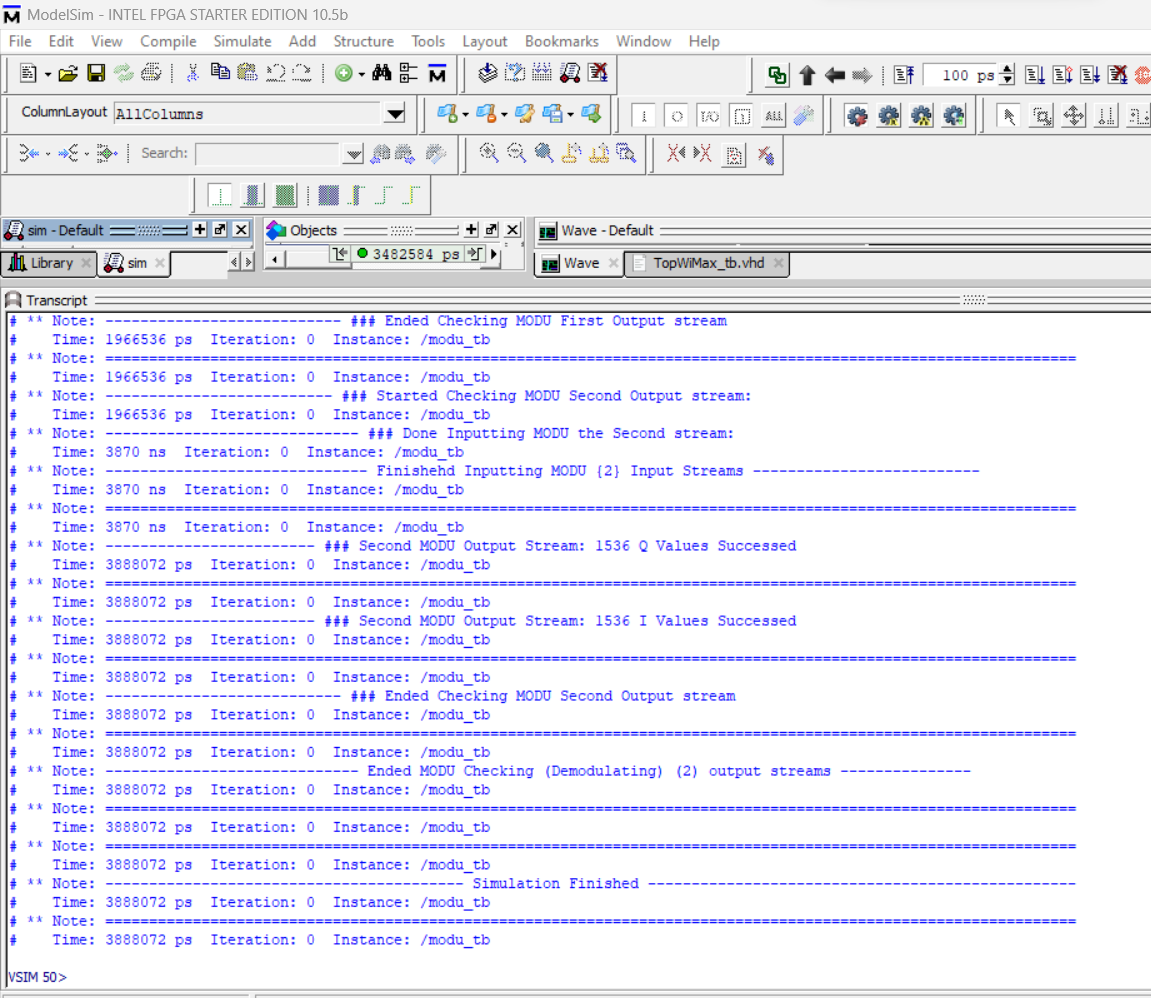
### Waveform (Sketch Expect)



### MODU Results (ModelSim Altera)



### Extra Fi MODU Self Chceck (ModelSim Altera)



## le

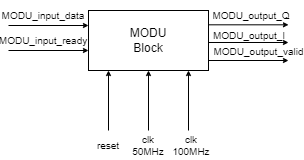
## 1 TopWiMax

|  |  |
| --- | --- |
| **Main File Name** | TopWiMax**.vhd** |
| **Testbench File Name** | TopWiMax **\_tb.vhd** |

### Ports:

|  |  |  |  |
| --- | --- | --- | --- |
| Signals | In/Out | Type | Width |
| WiInput | In | std\_logic | 1 |
| TopWiMax\_in\_ready | In | std\_logic | 1 |
| TopWiMax\_in\_valid | In | std\_logic | 1 |
| load | In | std\_logic | 1 |
| clk\_50MHz | In | std\_logic | 1 |
| reset | In | std\_logic | 1 |
| TopWiMax\_out\_valid | Out | std\_logic | 1 |
| TopWiMax\_out\_ready | Out | std\_logic | 1 |
| WiOutput1 | Out | std\_logic\_vector | 16 |
| WiOutput2 | Out | std\_logic\_vector | 16 |

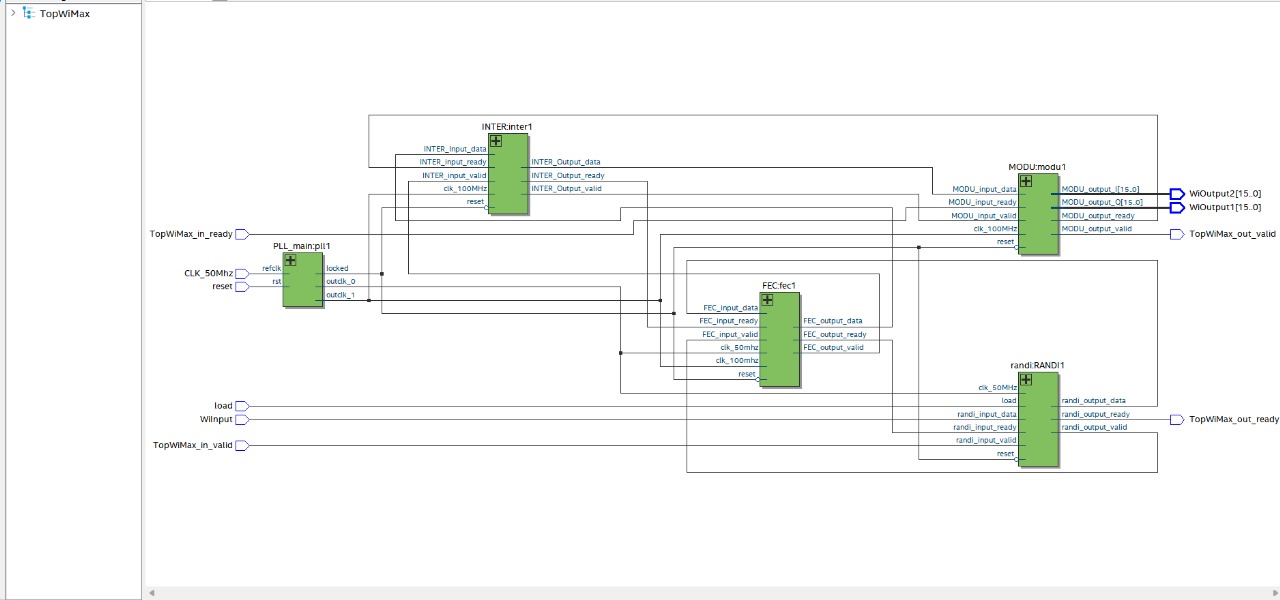
### Block Diagram Sketch:



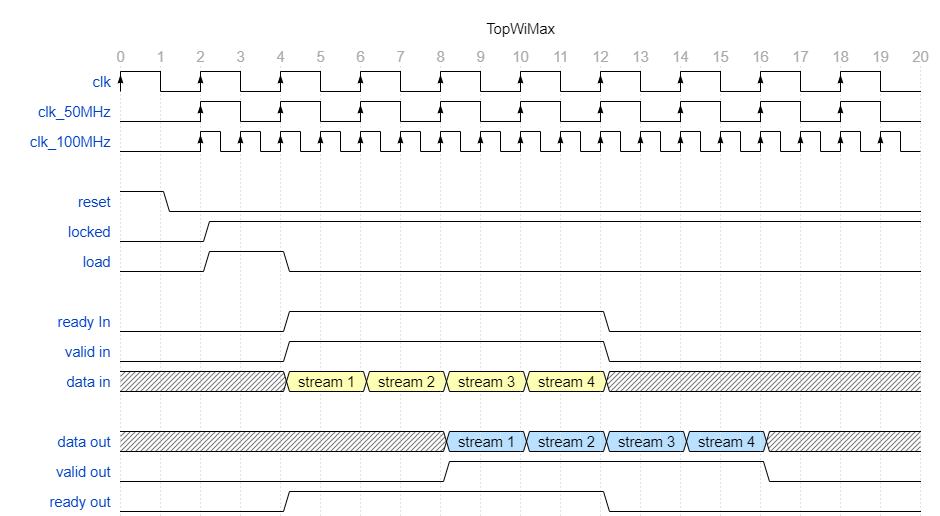
### Testing and Functionality

* ⁠2 inputs streams. Total runtime of around 4 us.
* Again, we use 100MHz for output and 50MHz for inputs.  
  - For handshaking, we have some delay to allow data to arrive as serial inputs (let’s say late by x cycles).   
  - The total time needed is n +x ( where n might be calculated as 192\*8).

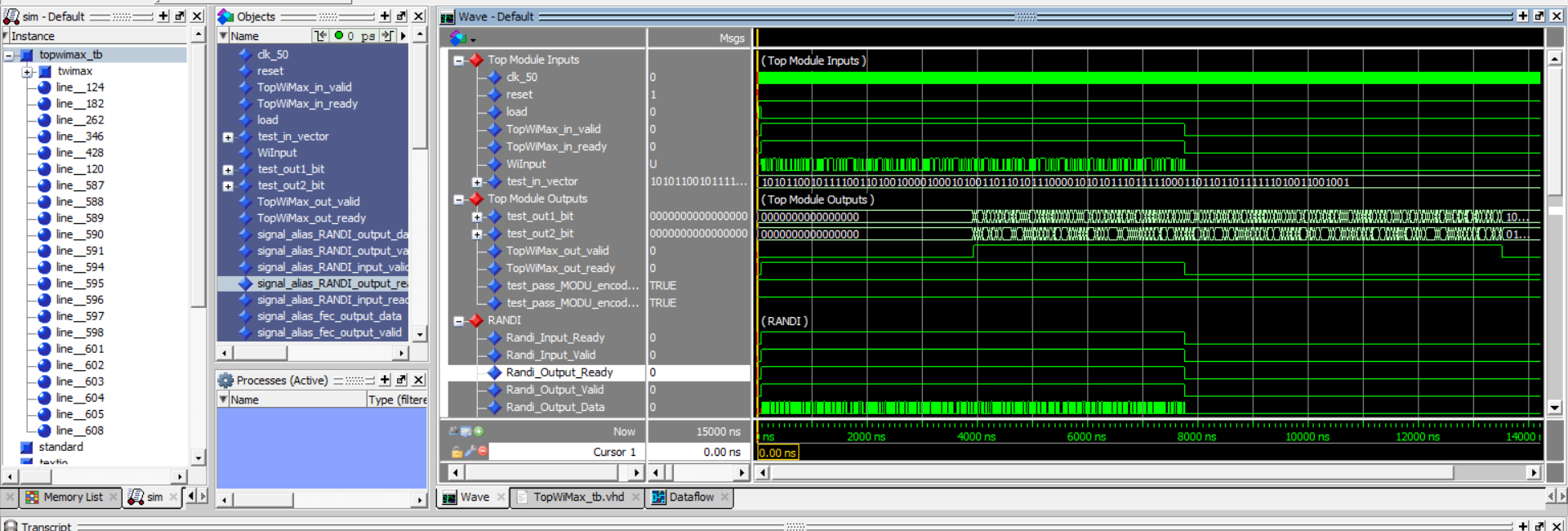
### RTL (Quartus)

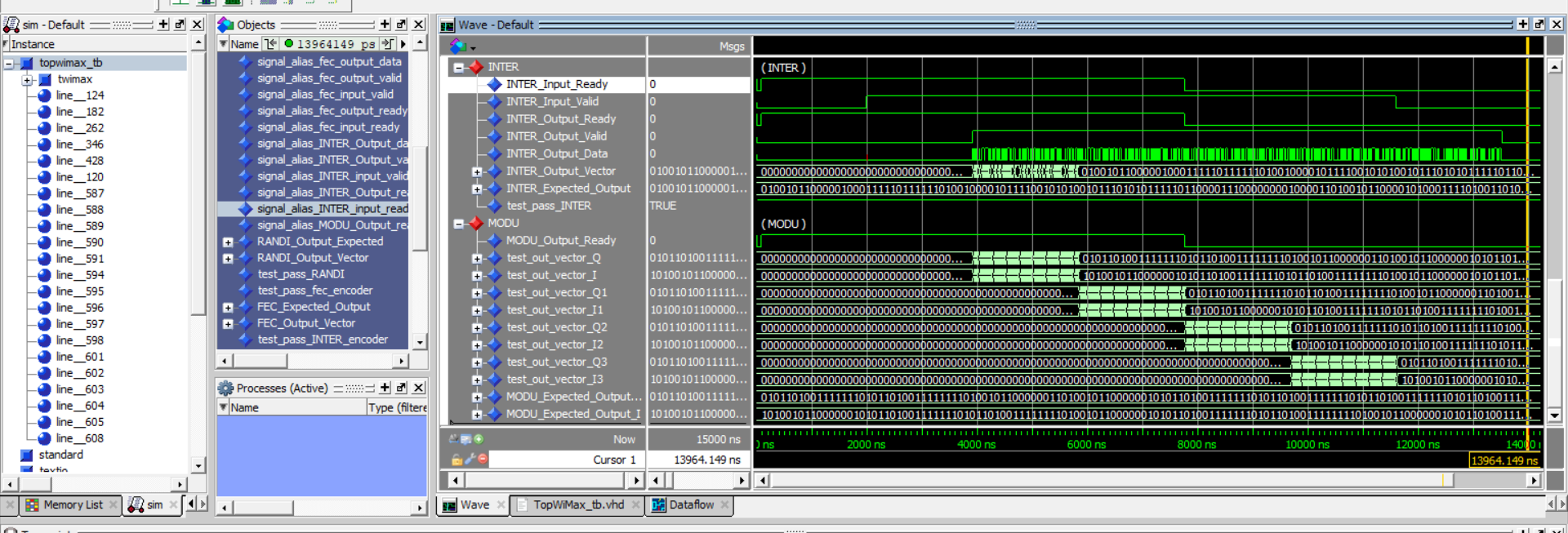
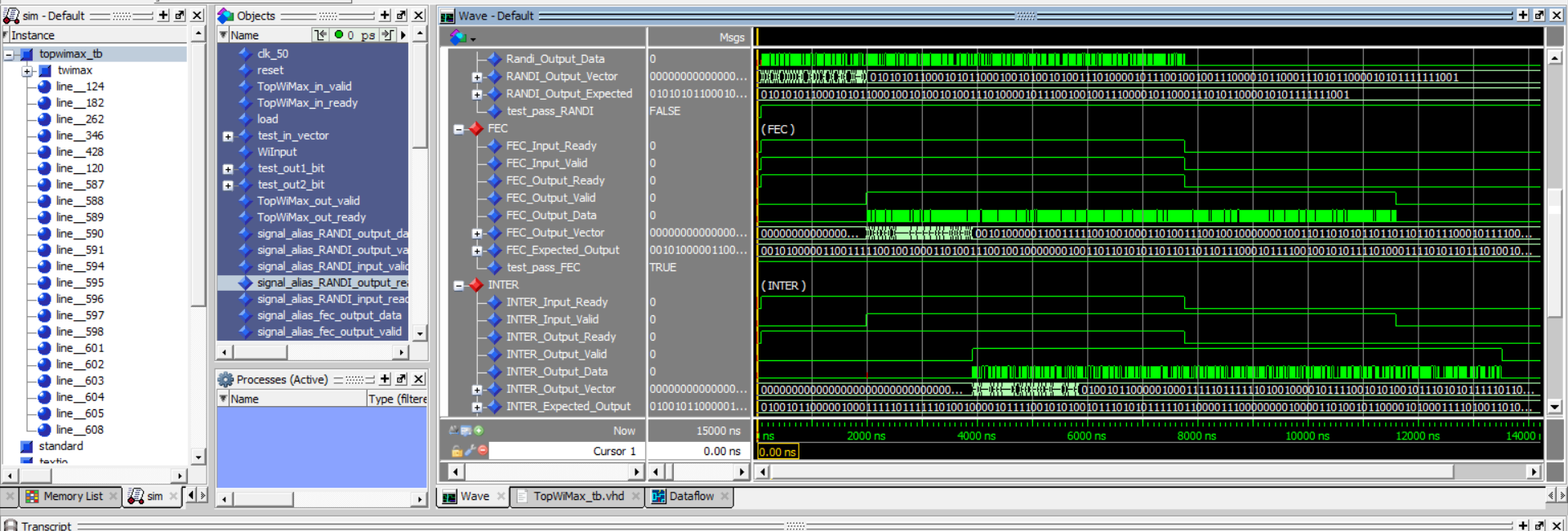


### Waveform (Sketch Expect)



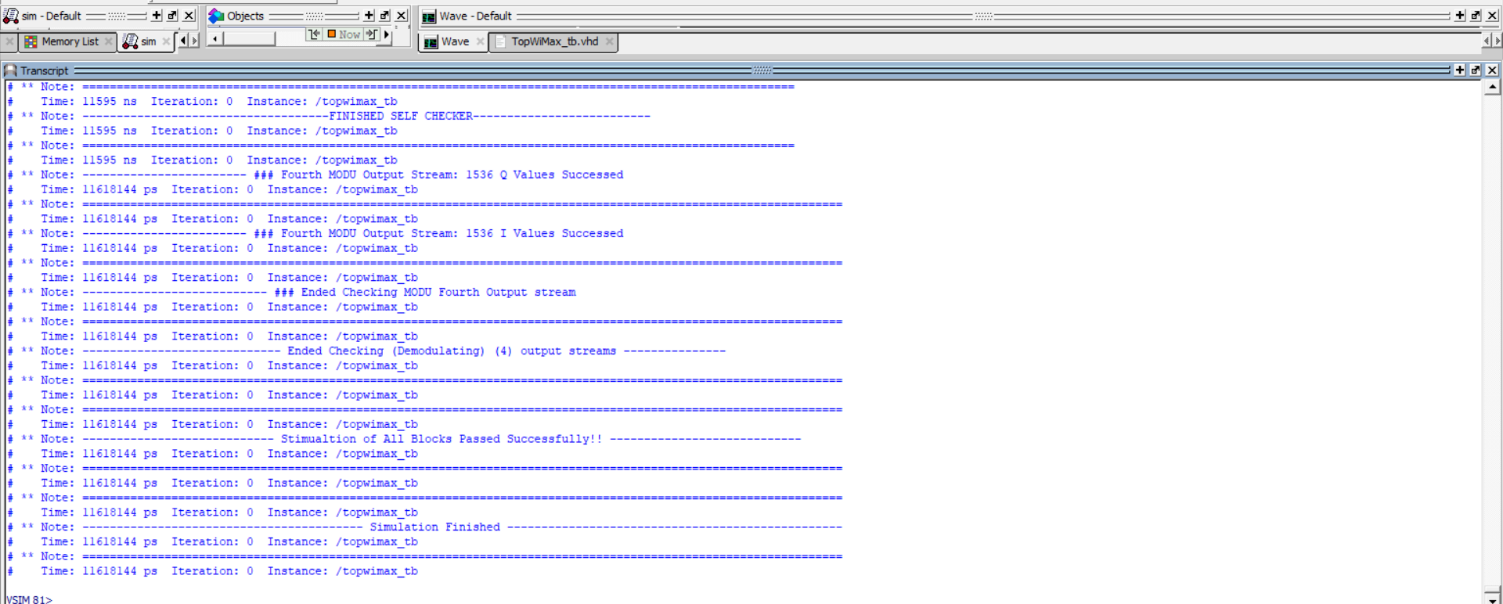
### Top Module Results (ModelSim Altera)





### Extra

### i MODU Self Chceck (ModelSim Altera)



### MODU Self Chceck (ModelSim Altera) (With Error Injected)

