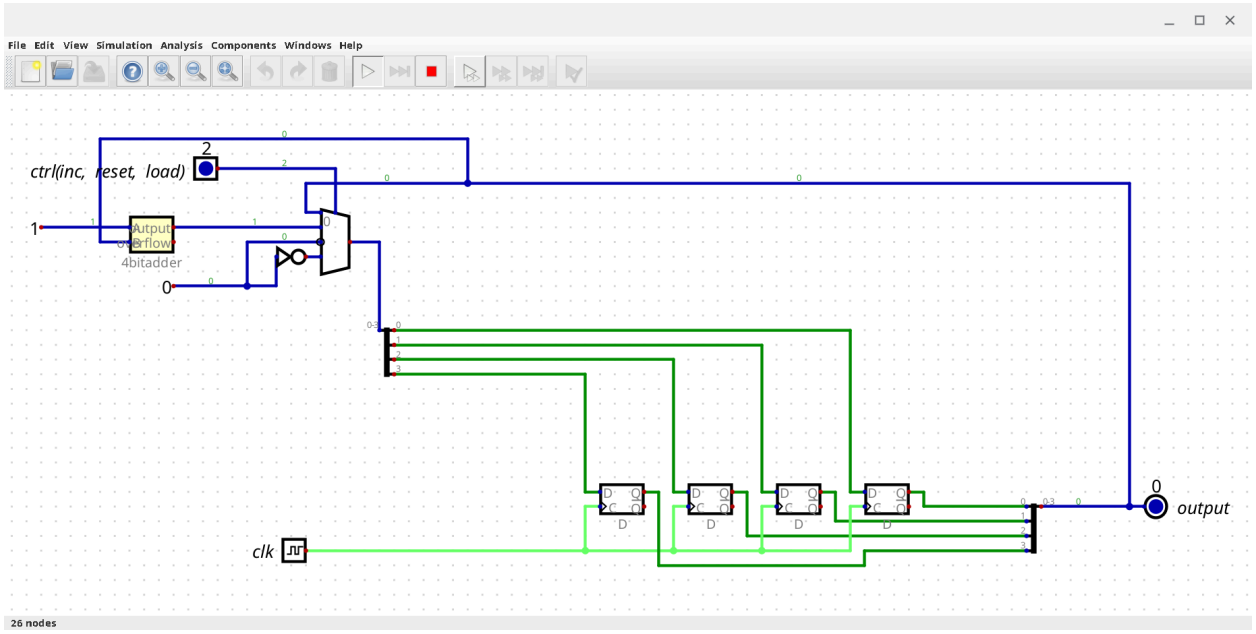
https://github.com/Alsheraa313/assignment-3-310

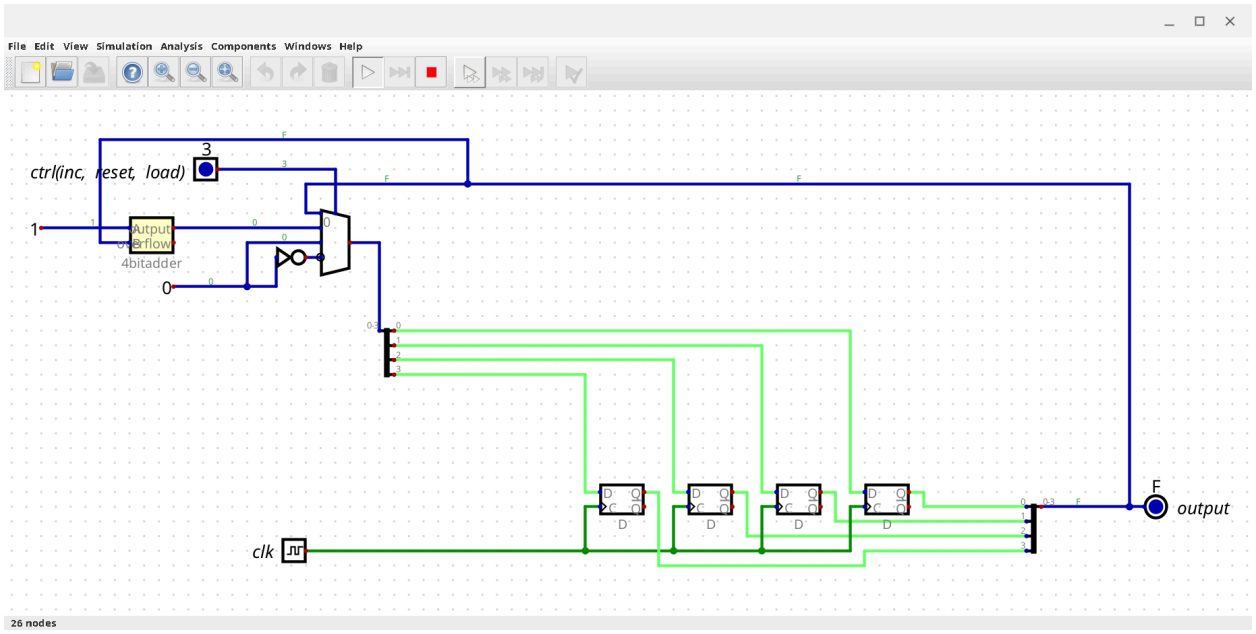
I worked individually

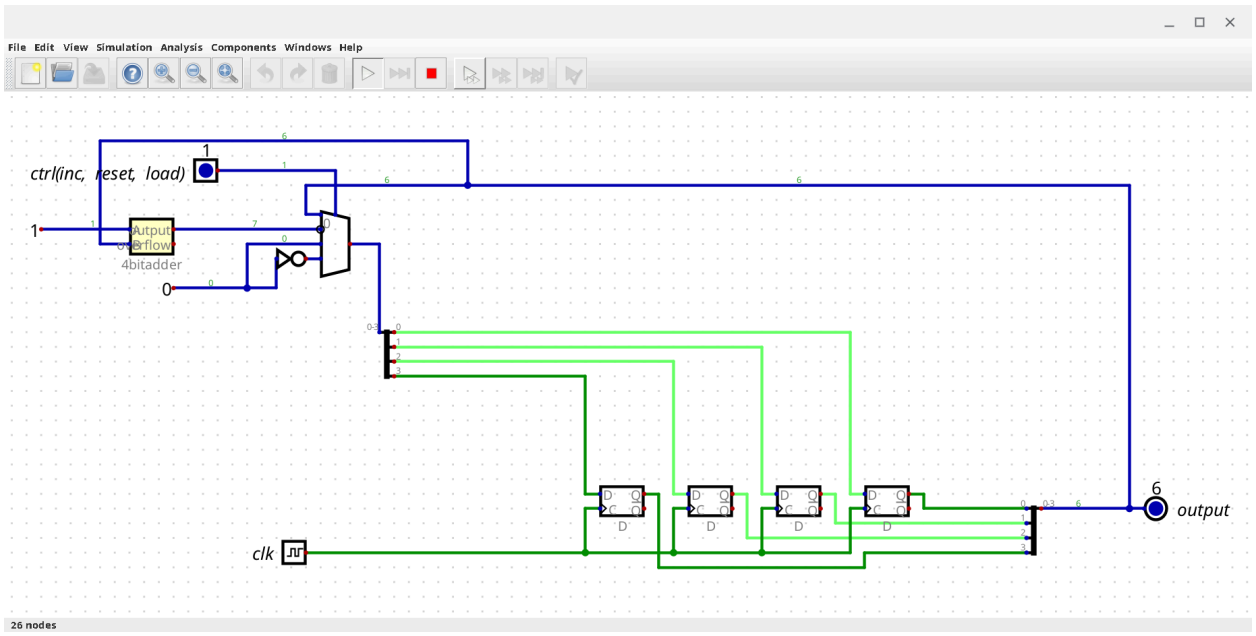
Design choices: the program counter feeds into the address input of the 16 address memory which then goes into a demultiplexer that selects the four 4 bit instruction registers. The output of the registers is then split up and taken into an instruction decoder which becomes the control signals for the register file. The register file's output become the A and B for the ALU and the extended instruction register becomes the selector pin for the ALU

Control signals: the control signals are generated by taking in the output of the extended instruction registers into the instruction decoder that takes a 2 bit input as the selector pin for a demultiplexer, and that output is split into one bit alongside a constant value zero. These two bits are then merged as an 8 bit output therefore generating a control signal for the register files

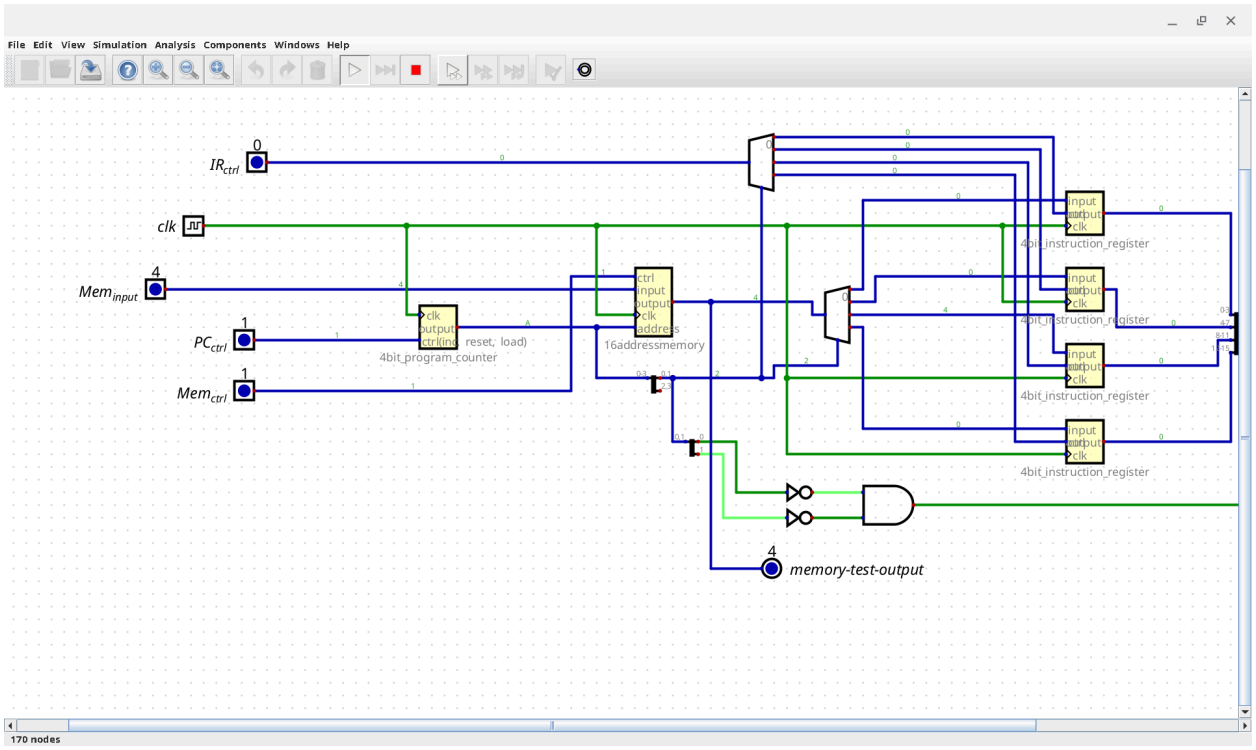
Program counter output

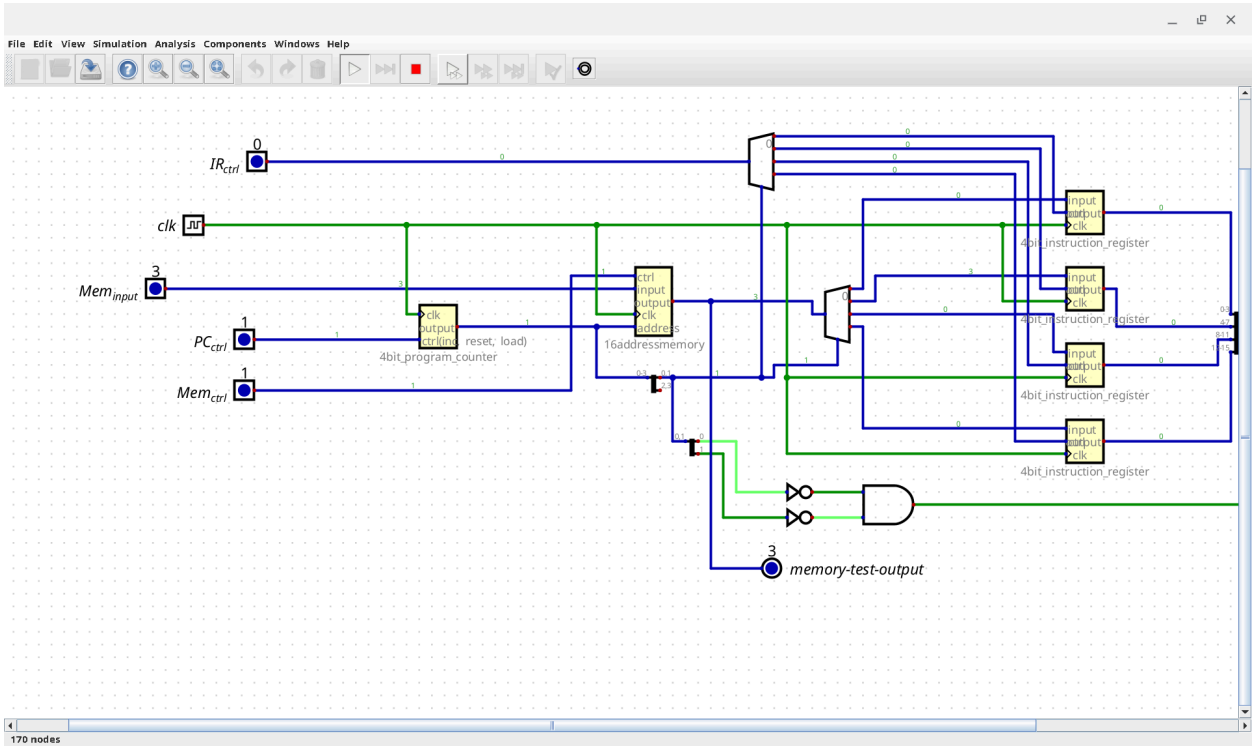


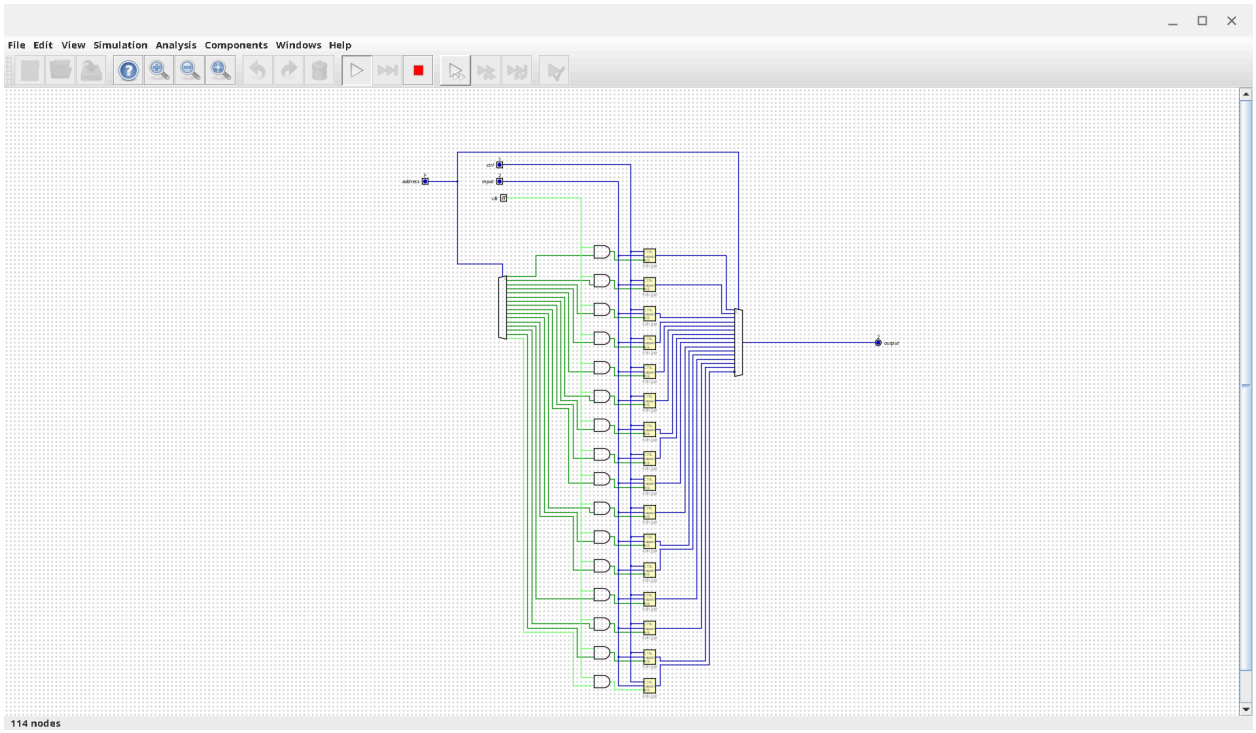




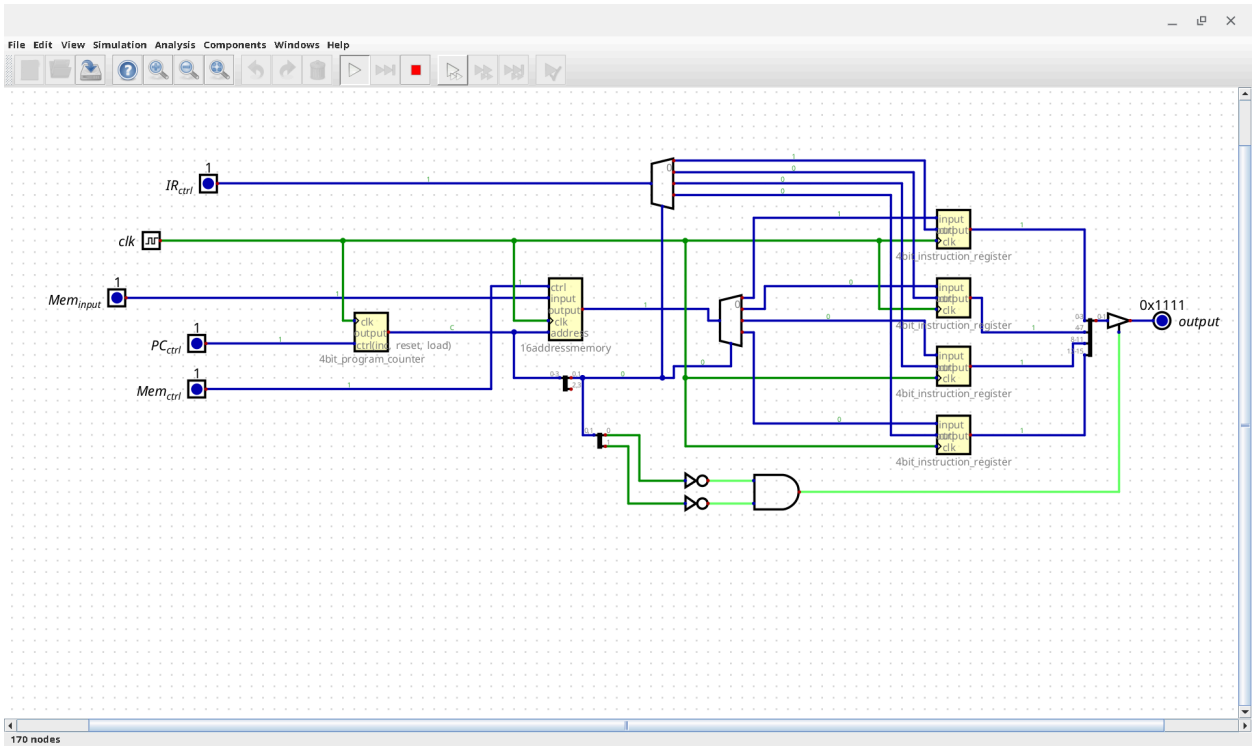
Instruction memory 16 address

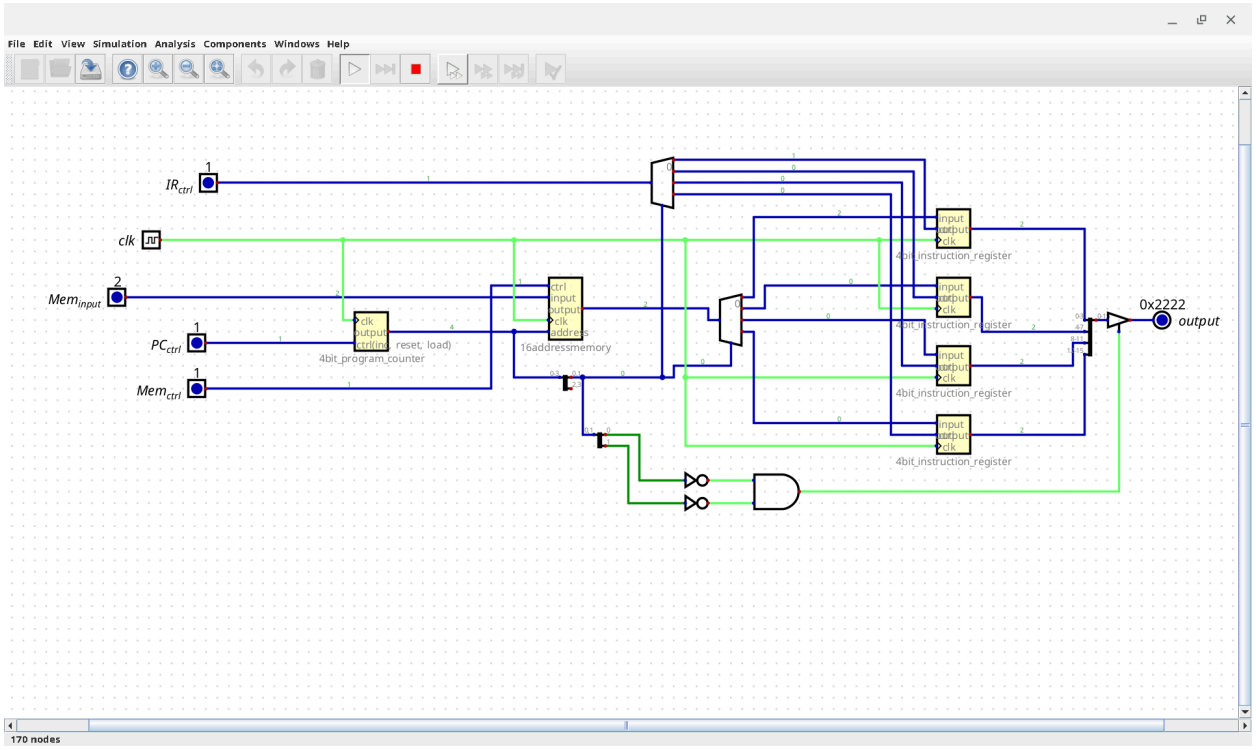

File Edit View Simulation Analysis Components Windows Help
IR_{ctrl}
0
clk
Mem_{input}
4
PC_{ctrl}
1
Mem_{ctrl}
1
4bit_program_counter
16addressmemory
4bit_instruction_register
4bit_instruction_register
4bit_instruction_register
4bit_instruction_register
4
memory-test-output
170 nodes

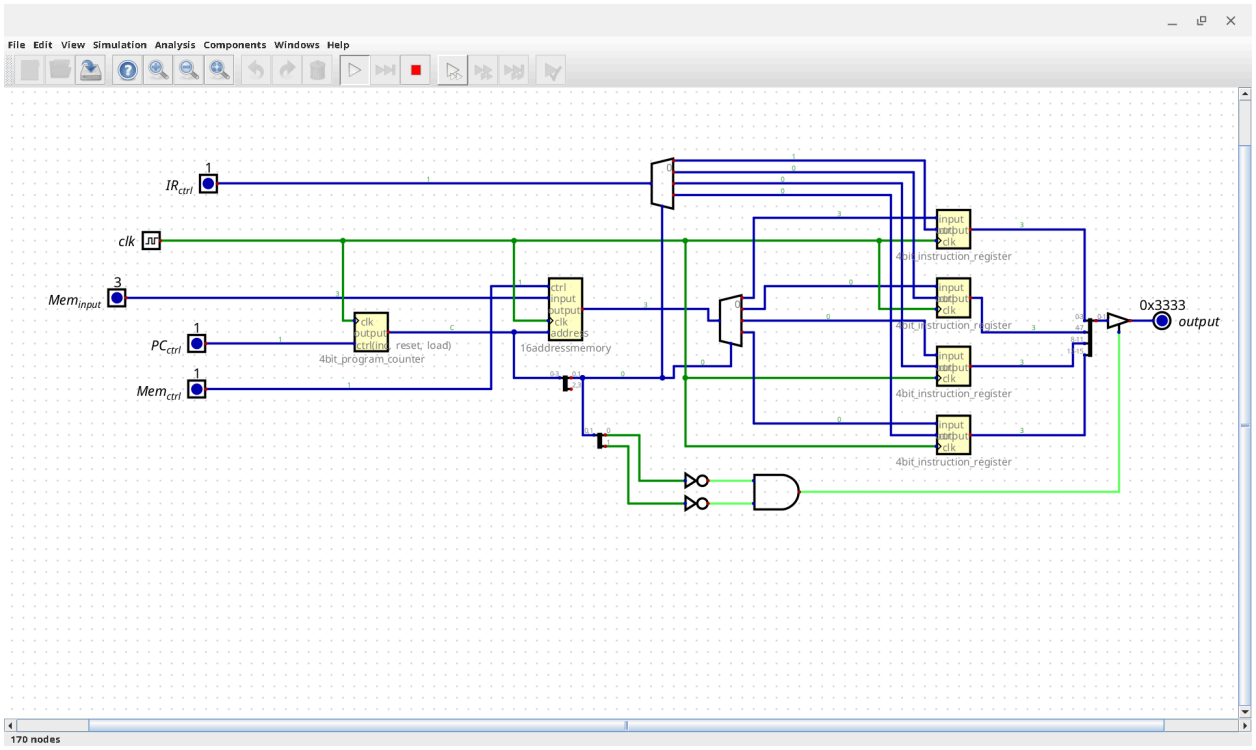

File Edit View Simulation Analysis Components Windows Help
IR_{ctrl}
0
clk
Mem_{input}
3
PC_{ctrl}
1
Mem_{ctrl}
1
4bit_program_counter
16addressmemory
4bit_instruction_register
4bit_instruction_register
4bit_instruction_register
4bit_instruction_register
3
memory-test-output
170 nodes

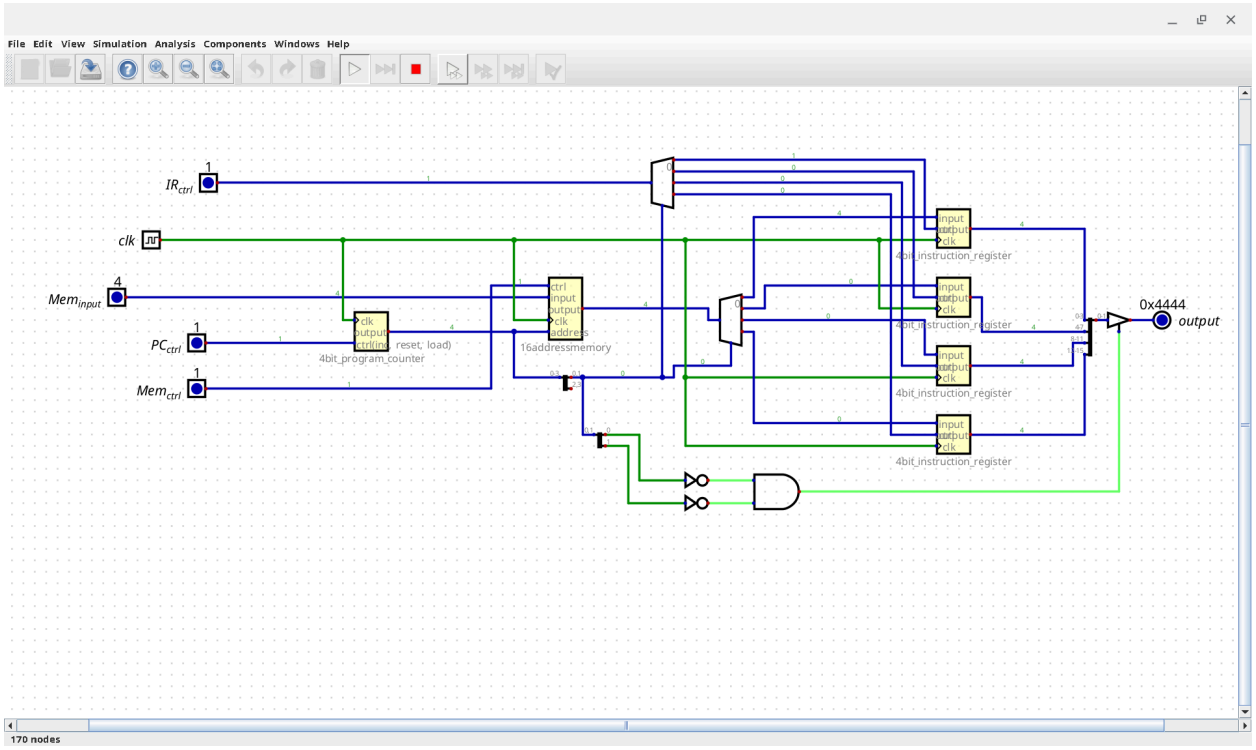


Extended IRs

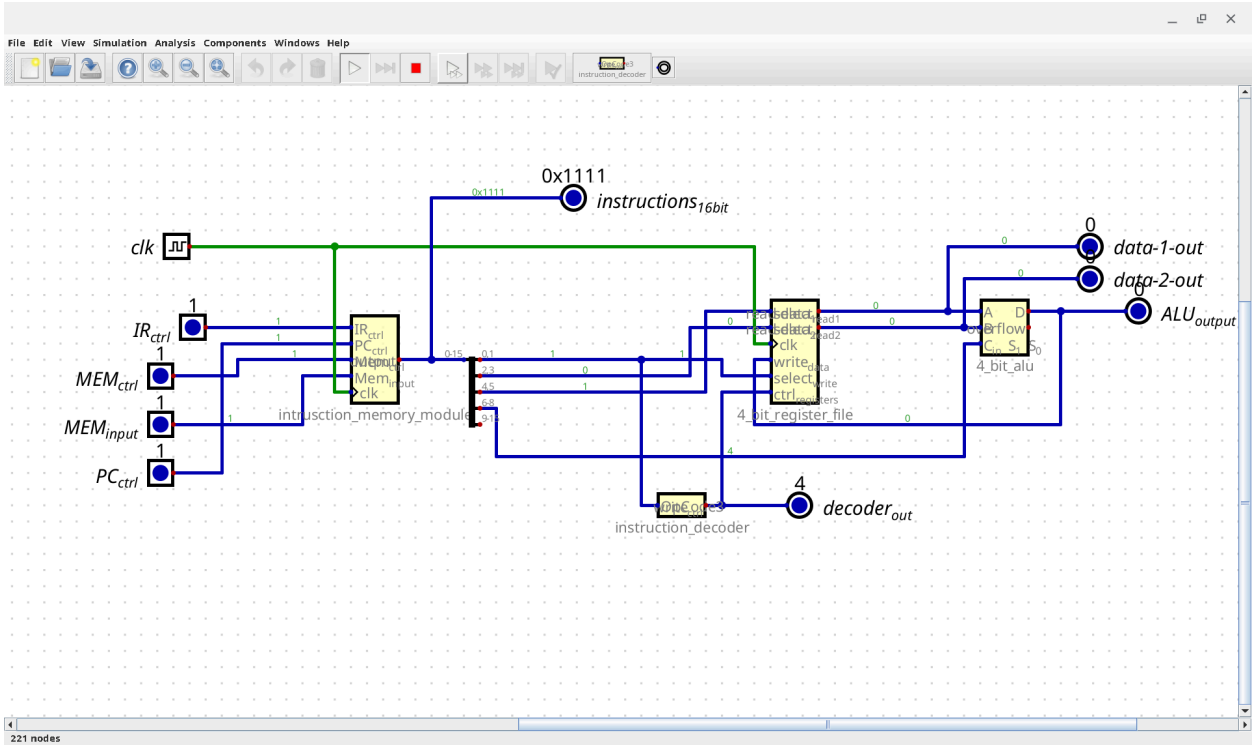

File Edit View Simulation Analysis Components Windows Help
IR_{ctrl}
clk
Mem_{input}
PC_{ctrl}
Mem_{ctrl}
4bit_program_counter
16addressmemory
4bit_instruction_register
0x1111
output
170 nodes

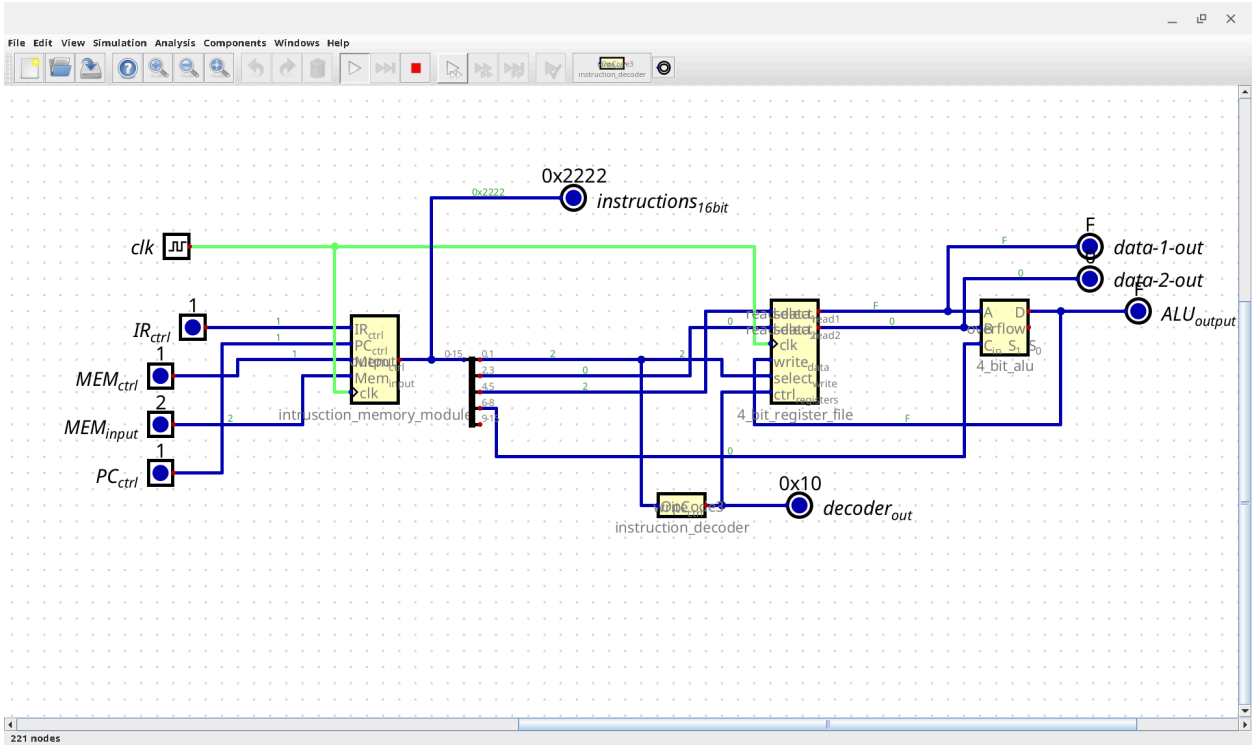

File Edit View Simulation Analysis Components Windows Help
IR_{ctrl}
clk
Mem_{input}
PC_{ctrl}
Mem_{ctrl}
4bit_program_counter
16addressmemory
4bit_instruction_register
0x2222
output
170 nodes





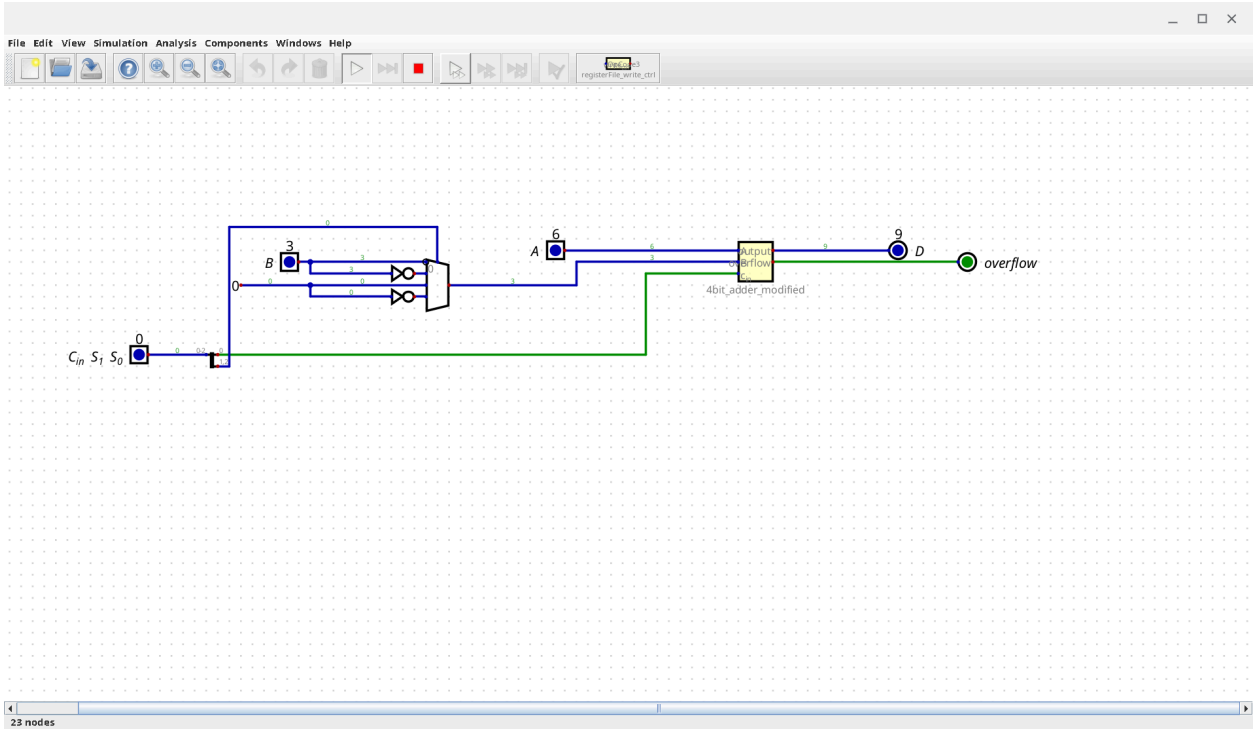
Instruction decoder / processor output



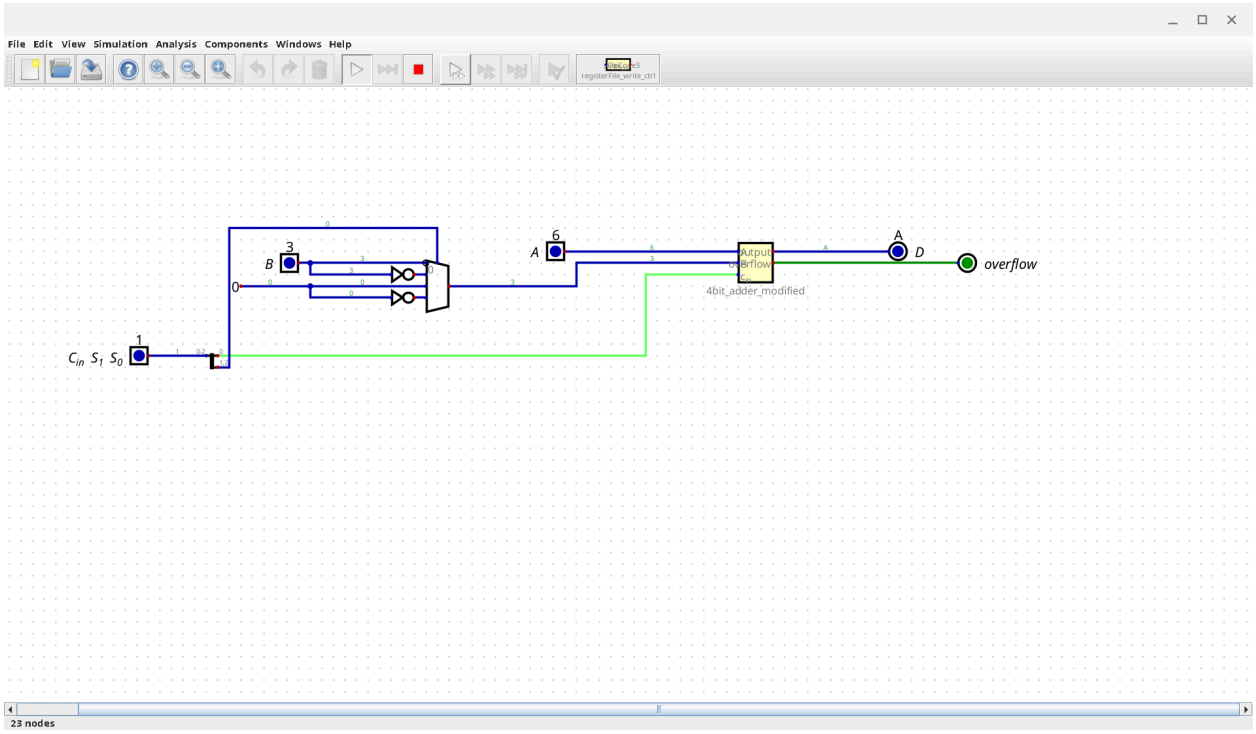


ALU operations

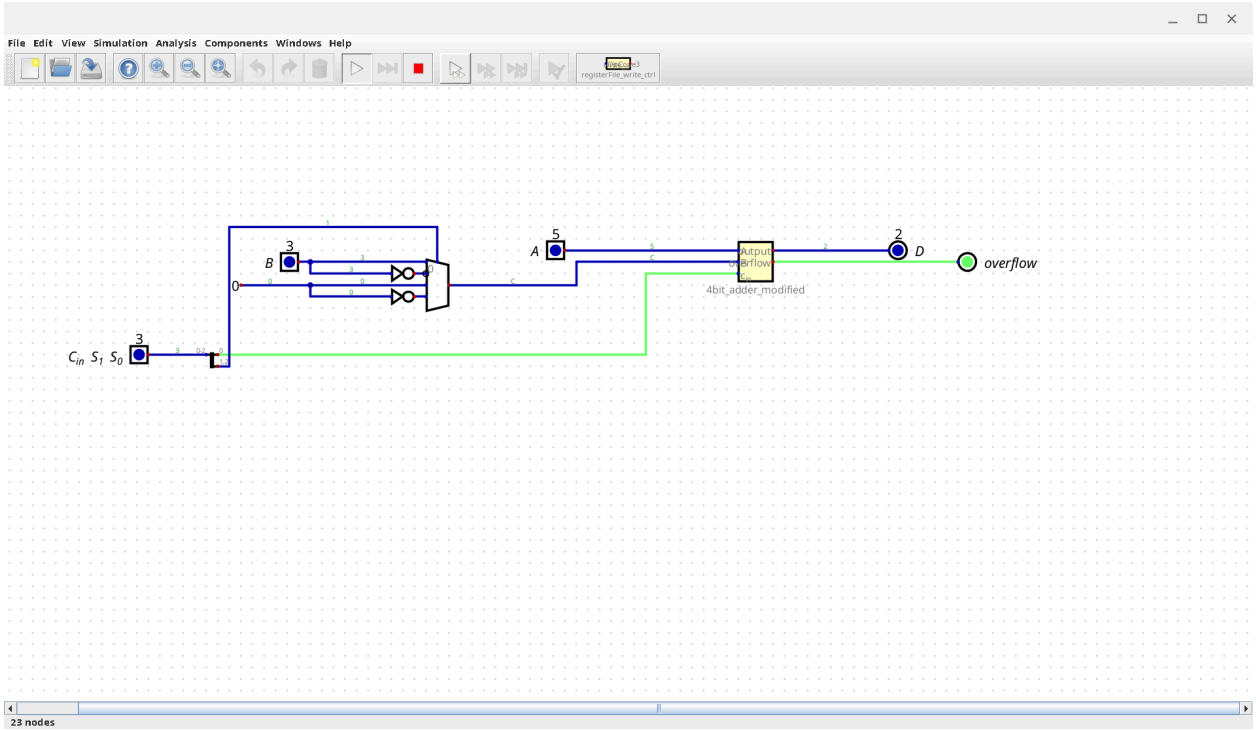
Add A + B



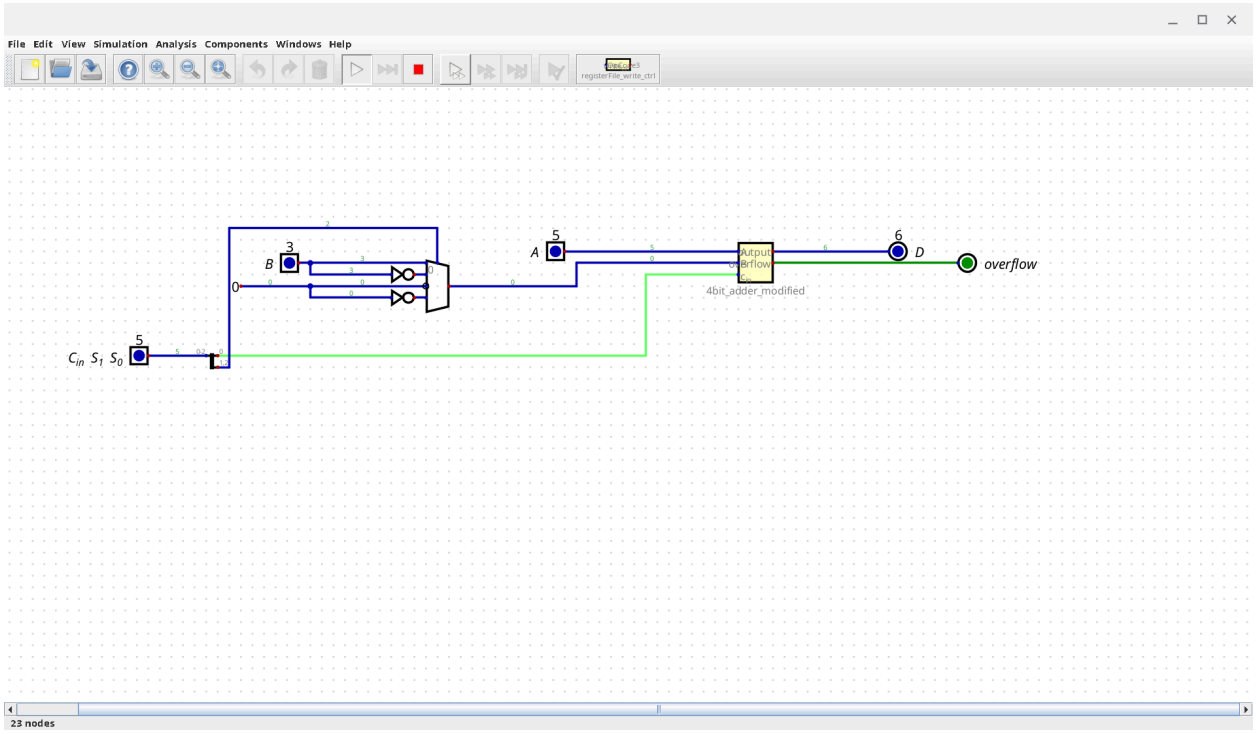
add with carry



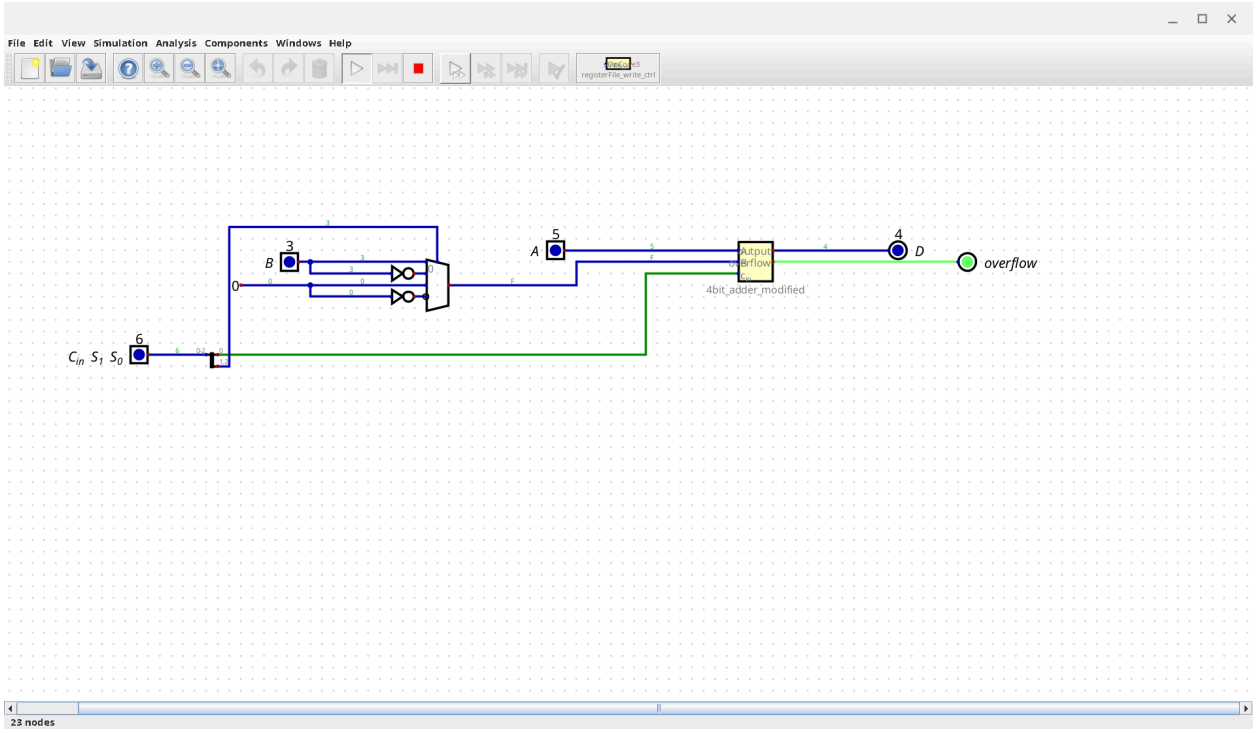
subtract A-B



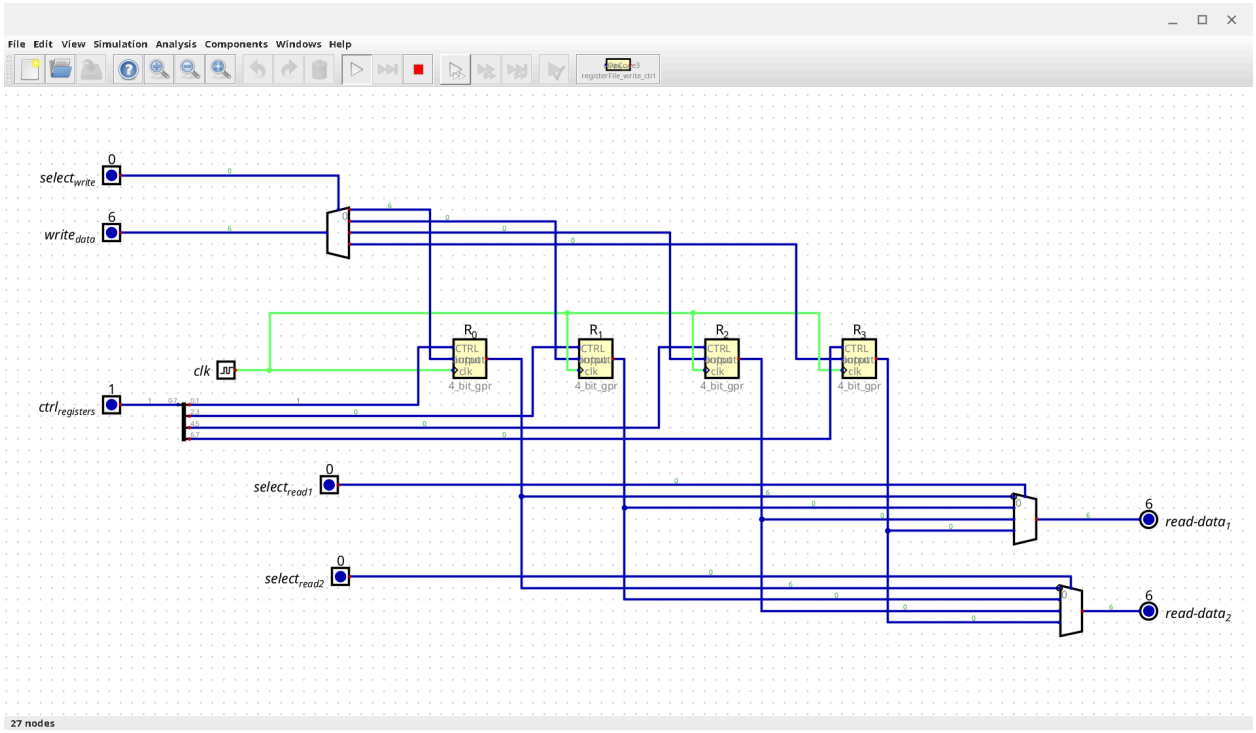
increment A

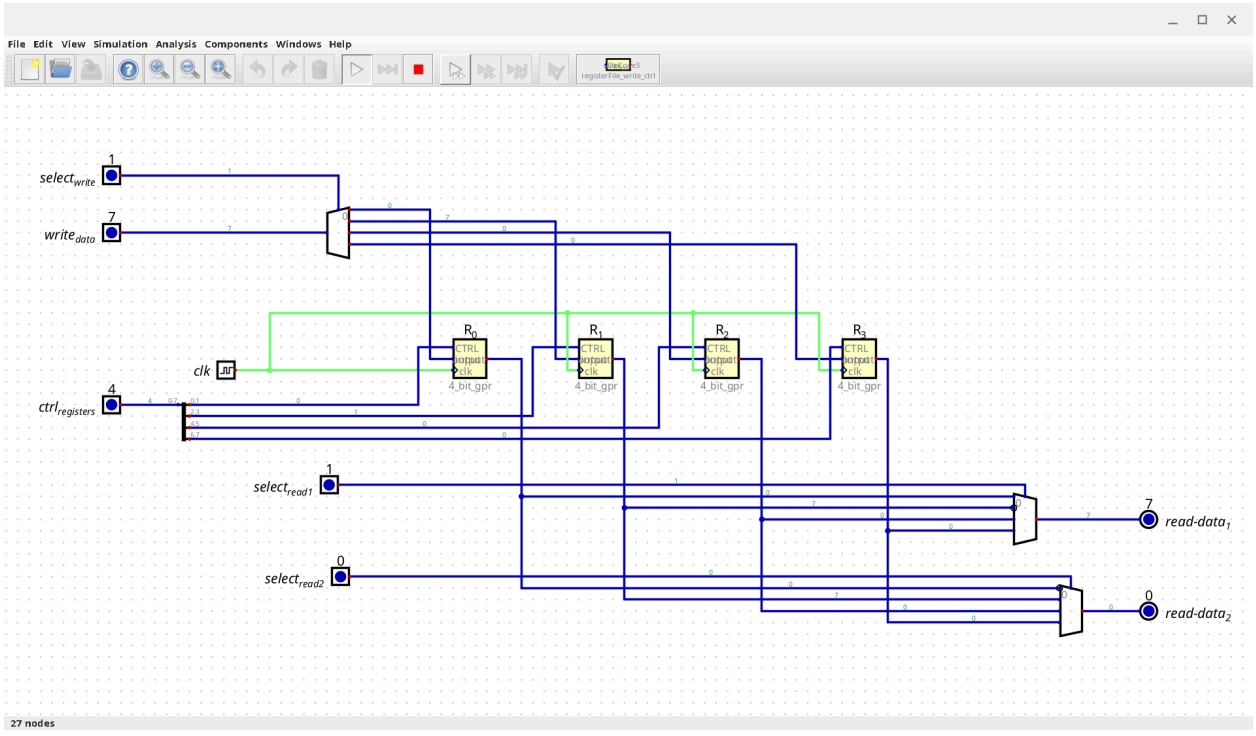


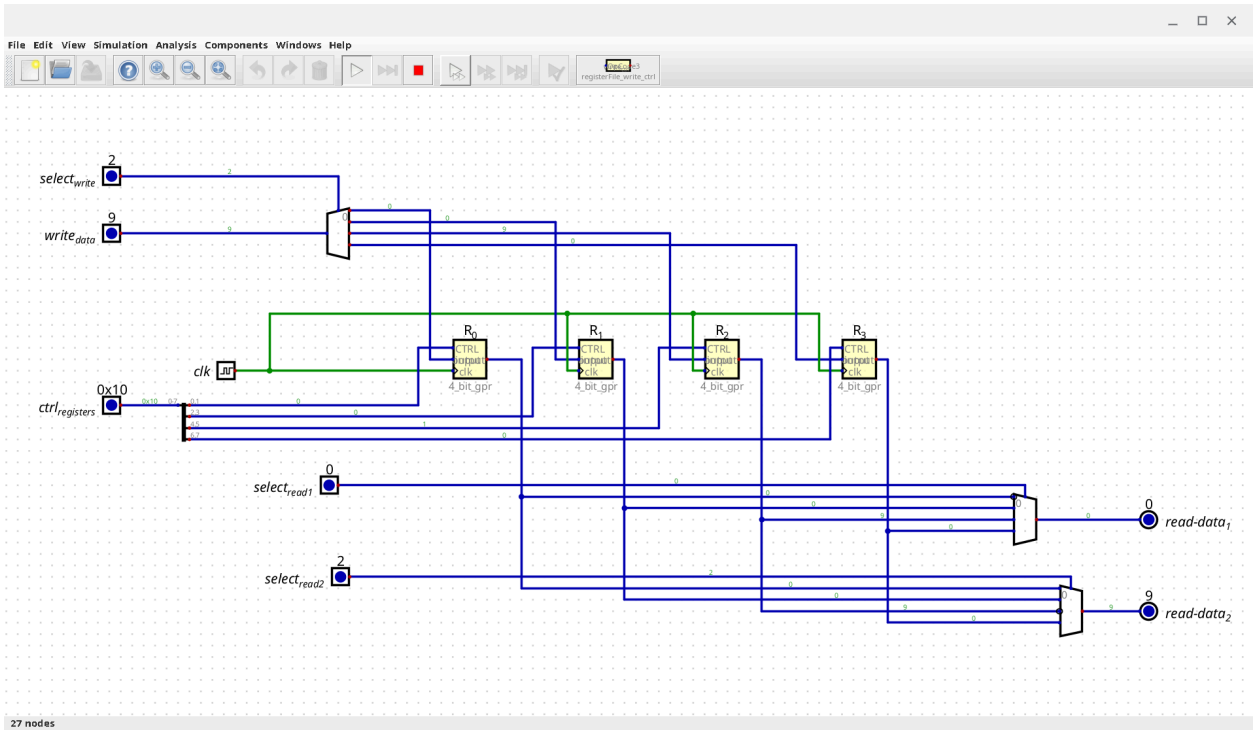
Decrement A

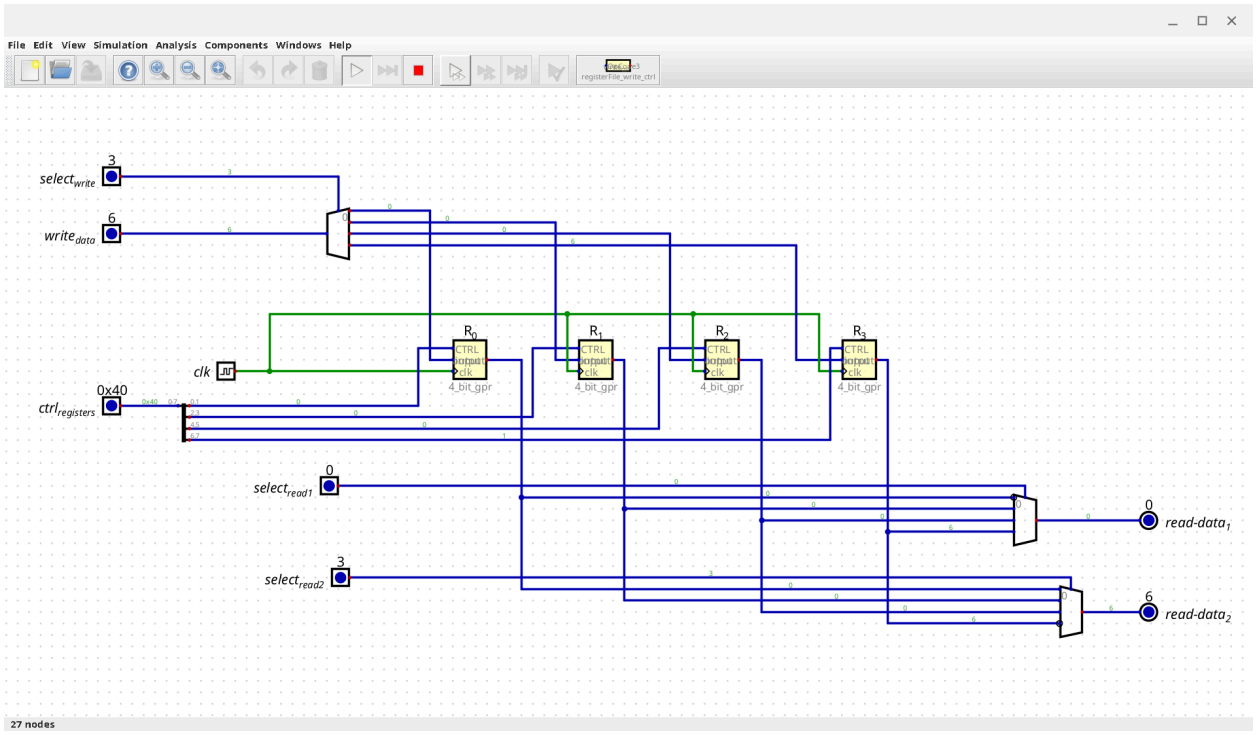

File Edit View Simulation Analysis Components Windows Help
B
3
0
A
5
4
D
overflow
C_{in} S_1 S_0
6
4bit_adder_modified
23 nodes

Register files






File Edit View Simulation Analysis Components Windows Help
registerFile_write_ctrl
select_write
2
write_data
9
clk
ctrl_registers
0x10
R0
R1
R2
R3
CTRL
clk
4_bit_gpr
select_read1
0
select_read2
2
read-data1
0
read-data2
9
27 nodes


File Edit View Simulation Analysis Components Windows Help
registerFile_write_ctrl
select_write
3
write_data
6
clk
ctrl_registers
0x40
R0
R1
R2
R3
CTRL
clk
4_bit_gpr
select_read1
0
select_read2
3
read-data1
0
read-data2
6
27 nodes