Pattern Stream&Capture block

By Alex Sukmanov

1. Introduction

This block is generic block that is integrated into FPGA that behaves as Tester for various ASICs. The FPGA in general is responsible of driving functional or scan pattern to the ASIC & check the pattern it gets back. This block, as part of the whole FPGA is responsible on the streaming & capturing of the pattern.



1. Requirements
   * High Level ( Interfaces )



* Clock & Reset
  + Clock –100 MHz system clock
  + Reset – Asynchronous system reset. Active low.
* Parameters
  + Nstream – Stream channel width parameter. Applied statically per synthesis.
  + Ncapture – Capture channel width parameter. Applied statically per synthesis.
  + Size – Size of test pattern. Can be modified dynamically. 0 to 4,294,967,296
  + Operation Mode – Operation mode selector [1:0]. 00 – Mode A. 01 – Mode B.   
    10 – Test Mode.
  + Go – Start operation pulse.
* Read port
  + Parallel data (128 bit) bus synchronous to 100 MHz system clock. Read transaction executed after handshake (Read request and Read valid) occurs.
* Write port
  + Parallel data (128 bit) bus synchronous to 100 MHz system clock. Write transaction executed after handshake (Write request and Write valid) occurs.  
    Write accept – second handshake for write approval.
* Status
  + Finish – Status flag bit. High when test vector streamed and data captured from ASIC.
  + Pass – Status flag bit for pattern check status. High – if expected data equals to captured data. Low – if expected data defers from captured data.
* Stream
  + Stream – parallel interface (GPIO) ASIC test input pins.
* Capture
  + Capture – parallel interface (GPIO) ASIC test output pins.

1. Principle of operation.

Test Pattern structure   
{Mask Vector [Ncapture-1:0], Expected Vector [Ncapture-1:0], Stream Vector [Nstream -1:0]} x Stream Pattern’s size.  
  
Block can operate in 3 modes.

* Mode A – Stream&Capture block reads from memory Test Pattern via **Read Port** and streams it to ASIC via **Stream** outputs. In parallel block captures data from ASIC via **Capture** inputs and writes it to memory via **Write Port**.
* Mode B – Stream&Capture block reads from memory Test Pattern via **Read Port.** Stream vector streamed to ASIC via **Stream** outputs. In parallel block captures data from ASIC via **Capture** inputs and compares it with Expected Vector. Mask vector used to compare only unmasked bits (not every cycle of captured vector contains relevant data).  
  The result is written to memory via **Write Port**.
* Test Mode – Stream&Capture block generates known default pattern and streams it to ASIC. Currently counter implemented as a default pattern.

1. Project Status.
   * Items done.  
     Project currently in pre-synthesis stage (RTL & Behavioral Simulation).  
     Mode A and Mode B have been implemented. Test Mode TBD.  
       
     Mode A approved by Behavioral simulation. DUT was tested with 1000 random test patterns with different pattern sizes. Simulation compared data transition on every stage with injected pattern from memory to ASIC and vice versa. 0 bit error rate.  
       
     Mode B approved by Behavioral simulation. DUT was tested with 1000 random test patterns with different pattern sizes. Simulation compared data transition on every stage with injected pattern from memory to ASIC and vice versa. 0 bit error rate.

Test mode implemented and approved by simulation. Block uses internal counter to stream pattern from 0 to Pattern\_Size-1 and write to memory captured data.

* + Items to be done.
    - Synthesis and debug signal definition
    - Static Timing Analysis
    - IP Creation
    - Implementation and bring up on Evaluation Board with ASIC mounted ( Out of course project’s scope)