Delft University of Technology

Faculty of Electrical Engineering, Mathematics and Computer Science
Computer Engineering Lab
2019-2020

Computer Architecture and Organization (CAO) EE3D11

Assignment 1

Deadline Feb 18, 2025 before 08:45!

Note:

- Upload a **single file** having the name "YourFirstName-LastName-HW-1" to the corresponding assignment in Brightspace.
- When needed, the answer should be **justified**. Show clearly which theory is used to find your final answer.

Exercise [2/2/2/2/2 pts]

Assume we have two different implementations P1 and P2 of the same ISA. The total instructions is $6*10^6$ and are divided into three classes A, B, and C as given in the next table

	Clock rate	CPI A	CPI B	CPI C
P1	2 GHz	2	3	2
P2	2.5 GHz	3	3	5

1. Assume instructions are divided into 30% of class A, 50% of Class B, and 20% of class C. Which implementation is slower?

P1: 7.5 *10^-3 s
P2: 8.16*10^-3 s → slower

2. What is the weighted/global CPI for each implementation?
   CPI= Clock cycles/ Instruction Count = CPU Time x Clock rate / Instruction count

Weighted:
- P1: 2.5
- P2: 3.4

Global:
- P1: 2.33
- P2: 3.4

3. Find the clock cycles required in both cases?

Clock cycles:
- P1: 1.62*10^7
- P2: 2.04*10^7

4. We would like to design a computer P3 to implement the same ISA and with the aim of CPU time of 5 ms. We can tune the design in order to increase the clock rate. However, this will lead to an increase of 1.2 x clock cycles of each of instruction classes of P1. How much should the clock rate of P3 be?

Clock rate P3: 3.888*10^9

5. We would like to design another computer P4 to implement the same ISA and with the aim of CPU time of 2 ms, and in a similar way as we did in question 4. Is this feasible if we assume that lead to an increase of 1.4 x clock cycles of each of instruction classes of P1?
   Justify your answer and explain the implications.

Assume we have two different processor implementations X and Y of the same ISA.
The total number of instructions is $7*10^6$ and these instructions are divided into three classes A, B, and C as given in the next table

	Clock rate	CPI A	CPI B	CPI C
X	2 GHz	2	3	2
Y	3 GHz	3	3	5

1. Assume instructions are divided into 30% of class A, 20% of Class B, and 50% of class C. Which implementation is slower?
   CPU Time = (Instruction Count x CPI) / Clock rate

   CPU Time (X) = $(2 * 30\% + 3 * 20\% + 2 * 50\%) * 7*10^6 / (2 * 10^9)$
   CPU Time (X) = $(.60 + .60 + 1.00) * 7*10^6 / 2*10^9 = 1540/2*10^5 = 7.70$ ms

   CPU Time (Y) = $(3 * 30\% + 3 * 20\% + 5 * 50\%) * 7*10^6 / (3 * 10^9)$
   CPU Time (Y) = $(.90 + .60 + 2.50) * 7*10^6 / (3 * 10^9) = 9.33$ ms

   Hence Y is slower than X

2. What is the weighted/global CPI for each implementation?
   Weighted CPI:
   CPI (X) = $2 * 30\% + 3 * 20\% + 2 * 50\% = 2.2$
   CPI (Y) = $3 * 30\% + 3 * 20\% + 5 * 50\% = 4$
   Global CPI:
   CPI (X) = $(2 + 3 + 2) / 3 = 2.33$
   CPI (Y) = $(3 + 3 + 5) / 3 = 3.67$

3. Find the clock cycles required in both cases.

   Clock cycles = Sum (CPI_i x IC_i)
   Clock cycles (X) = $2* 30\% IC + 3*20\% IC + 2*50\%*IC = (.60+.60+1.00)* 7 * 10^6 = 1.54*10^7$
   Clock cycles (Y) = $3* 30\% IC + 3*20\% IC + 5*50\%*IC = (.90+.60+2.50)* 7 * 10^6 = 2.8*10^7$

4. We would like to design a computer Z to implement the same ISA and with the aim of CPU time of 5 ms. We can tune the design in order to increase the clock rate. However, this will lead to an increase of 1.3 x clock cycles of each of instruction classes of X. How much should the clock rate of Z be?

   Clock rate(Z) = clock cycles(Z) / CPU time(Z)

   CPU time (Z) = 5 ms
   Clock cycles (Z) = 1.3 X Clock cycles (X) = $1.3 \times 1.54*10^7 = 20.02 *10^6$
   Clock rate (Z) = $20.02*10^6 / (5 *10^{-3}) = 4$ GHz

5. We would like to design another computer Z' to implement the same ISA and with the aim of CPU time of 2 ms, and in a similar way as we did in question 4. Is this feasible if we assume that it leads to an increase of 1.4 x clock cycles of each of instruction classes of X?
   Justify your answer and explain the implications.

   Applying the theory above will lead to a clock rate of more than 10.78 GHz.
   Realizing CPUs with higher speed than ~ 4 GHZ has been shown to be impossible due to power and thermal constrains. This is why Intel canceled the line of single core Pentium 4 around 2001.