2015-2016-CAO-Assignment 3 - Answers

Computer Architecture and Organisation (Technische Universiteit Delft)

Delft University of Technology
Faculty of Electrical Engineering, Mathematics and Computer Science
Computer Engineering Lab
2015-2016

Computer Architecture and Organization (CAO) EE3D11

Assignment 3

Deadline March 1, 2016 before 13:30!

Note:

- Send a **single file** having the name YourFirstName-LastName-Homework-1 to the following e-mails: H.A.DuNguyen@tudelft.nl, J.Yu-1@tudelft.nl , R.Nane@tudelft.nl
- When needed, the answer should be **justified**. Show clearly which theory is used to find you final answer.

Exercise 1 [5 pts]

This problem covers ***4-bit binary*** multiplication. Assume:

- Multiplier A= 10 (decimal)
- Multiplicand B = 11 (decimal)

Use the implementation of Figure 3.3 in the book (5th edition) to fill in the table below. Specify the iteration step, the contents of three registers as well as the description of the step. (see also Table 3.6 in the book). Give the value of the register in the binary format.

iteration	Description	Multiplier (MR)	Multiplicand (MD)	Product (P)
0	Initial values	1010	0000 1011	0000 0000
1	Multiplier bit =0, no add	1010	0000 1011	0000 0000
	Shift left MD	1010	0001 0110	0000 0000
	Shift right MR	0101	0001 0110	0000 0000
2	Multiplier bit =1, add MD to P	0101	0001 0110	0001 0110
	Shift left MD	0101	0010 1100	0001 0110
	Shift right MR	0010	0010 1100	0001 0110
3	Multiplier bit =0, no add	0010	0010 1100	0001 0110
	Shift left MD	0010	0101 1000	0001 0110
	Shift right MR	0001	0101 1000	0001 0110
4	Multiplier bit =1, add	0001	0101 1000	0110 1110
	Shift left MD	0001	1011 0000	0110 1110
	Shift right MR	0000	1011 0000	0110 1110
5	Multiplier bit =0, no add	0000	1011 0000	0110 1110
	Shift left MD	0000	0110 0000	0110 1110
	Shift right MR	0000	0110 0000	0110 1110

Optional: redo the same exercice above but now by using the hardware of Figure 3.5 of the (fifth edition of the book). No need to deliver the answer. However, we will be pleased to give you feedback if needed.; and it is strongly recommended to practice this question and compare the answers.

Exercise 2 [0.5/ 0.5 / 2 /2 pts]

In a Von Neumann architecture, groups of bits have no intrinsic meanings by themselves. What a bit pattern represents depends entirely on how it is used. The following table shows bit patterns expressed in **hexadecimal** notation: 0x0C300000

1. What decimal number does the bit pattern represent if it is an unsigned integer?
   - 0x0C300000 = 0000 1100 0011 0000 0000 0000 0000 0000 (binary)
     = 204472320

2. What decimal number does the bit pattern represent if it is a two's complement integer?
   - The same as in 1.

3. If this bit pattern is placed into the Instruction Register of a MIPS processor, what instruction will be executed?
   - **000011** 00 0011 0000 0000 0000 00 000000 **: it is jump and link instruction**
   - Format: op(6bits) address (26bits)
   - Hence: Jal 0x00300000

4. Assume now the IEEE 754 standard. What decimal number does the bit pattern represent if it is a floating point number?

   - 0x0C300000 = 0 00011000 01100000000000000000000 (binary)
     = sign-bit Exponent E (8bits) Fraction F(23bits)
   - Sign: positive
   - Exponent= 24-127=-103 (decimal). 127 is due to Bias notation
   - Fraction=1/4+1/8 =0.25+0.125=0.375
   - 1 is hidden
   - Answer is: $+1.375\ 2^{-103}$
   - …