```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity decoder_3x8 is
      Port(i: in std_logic_vector(2 downto 0); o: out std_logic_vector(7
downto 0));
end decoder_3x8;

architecture Behaviorial of decoder_3x8 is
begin
      o <= "00000001" when i="000" else "00000010" when i="001" else
"00000100" when i="010" else  "00001000" when i="011" else  "00010000"
when i="100" else  "00100000" when i="101" else  "01000000" when i="110"
else  "10000000";
end Behaviorial;
```