```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity mux_4x1 is
      Port(i: in std_logic_vector(3 downto 0); sel: in std_logic_vector(1
downto 0); o: out std_logic);
end mux_4x1;

architecture Behaviorial of mux_4x1 is
begin
      o <= i(0) when sel="00" else i(1) when sel="01" else i(2) when
sel="10" else i(3);
end Behaviorial;
```