```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity tri_state is
      Port(i: in std_logic; en: in std_logic; o: out std_logic);
end tri_state;

architecture Behaviorial of tri_state is
begin
      o <= i when en='1' else 'Z';
end Behaviorial;
```