```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity mux_4x1 is
      Port(d: in std_logic_vector(3 downto 0); sel: in std_logic_vector(1
downto 0); o: out std_logic);
end mux_4x1;

architecture Behaviorial of mux_4x1 is
begin
      p1: process(d,sel)
      begin
            if (sel="00") then o<= d(0);
            elsif (sel="01") then o <= d(1);
            elsif (sel="10") then o<= d(2);
            else o <= d(3);
            end if;
      end process p1;
end Behaviorial;
```