```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity demux_1x4 is
      Port(i: in std_logic; sel: in std_logic_vector(1 downto 0); o: out
std_logic_vector(3 downto 0));
end demux_1x4;

architecture Behaviorial of demux_1x4 is
begin
      o(0) <= (not sel(0)) and (not sel(1)) and i;
      o(1) <= (not sel(0)) and ( sel(1)) and i;
      o(2) <= ( sel(0)) and (not sel(1)) and i;
      o(3) <= ( sel(0)) and ( sel(1)) and i;
end Behaviorial;
```