```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity encoder_4x2 is
      Port(i: in std_logic_vector(3 downto 0); o: out std_logic_vector(1
downto 0));
end encoder_4x2;

architecture Behaviorial of encoder_4x2 is
begin
      o(0) <= (not i(0)) or (not i(1)) or i(2) or i(3);
      o(1) <= (not i(0)) or i(1) or (not i(2)) or i(3);
end Behaviorial;
```