```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity decoder_2x4 is
      Port(i: in std_logic_vector(1 downto 0); o: out std_logic_vector(3
downto 0));
end decoder_2x4;

architecture Behaviorial of decoder_2x4 is
begin
      p1: process(i)
      begin
            if (i="00") then o <= "0001";
            elsif (i="01") then o <= "0010";
            elsif (i="10") then o <= "0100";
            else o <= "1000";
            end if;
      end process p1;
end Behaviorial;
```