```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity mux_2x1 is
      Port(i: in std_logic_vector(1 downto 0); sel: in std_logic; o: out
std_logic);
end mux_2x1;

architecture Behaviorial of mux_2x1 is
begin
            o <= ((not sel) and i(0)) or (sel and i(1));
end Behaviorial;
```