```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity tri_state2 is
      Port(i: in std_logic; en: in std_logic; o: out std_logic);
end tri_state2;

architecture Behaviorial of tri_state2 is
begin
      with en select
      o <= i when '1', 'Z' when others;
end Behaviorial;
```