```
library IEEE;
use IEEE.std_logic_1164.all;

entity mag_comp is
      Port(a: in std_logic; b: in std_logic; eq: out std_logic; a_max: out
std_logic; b_max: out std_logic);
end mag_comp;

architecture Dataflow of mag_comp is
begin
      eq <= a xnor b;
      a_max <= a and (not b);
      b_max <= (not a) and b;
end Dataflow;
```