```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity mux_4x1 is
      Port(i: in std_logic_vector(3 downto 0); sel: in std_logic_vector(1
downto 0); o: out std_logic);
end mux_4x1;

architecture Behaviorial of mux_4x1 is
begin
      with sel select
      o <= i(0) when "00", i(1) when "01", i(2) when "10", i(3) when "11",
unaffected when others;
end Behaviorial;
```