```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity t_ff is
      Port(t_in : in std_logic; clk: in std_logic; rst: in std_logic;
t_out: out std_logic);
end t_ff;

architecture Behaviorial of t_ff is
begin
      p1: process(t_in,rst,clk)
      variable temp: std_logic:= '0';
      begin
            if(rst='1') then temp:='0';
            elsif(clk' event and clk='1') then
                  if(t_in='1') then temp:= not temp;
                  end if;
            end if;
      t_out <= temp;
      end process p1;
end Behaviorial;
```