```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity rom_8x8 is
      Generic(words: INTEGER:=8; bits: INTEGER:=8);
      Port(address: in INTEGER range 0 to (words-1);data: out
std_logic_vector((bits-1) downto 0));
end rom_8x8;

architecture Behaviorial of rom_8x8 is
type vector_array is array(0 to 7) of std_logic_vector(7 downto 0);
Constant memory:
vector_array:=("00000001","00000010","00000100","00001000","00010000","001
00000","01000000","10000000");
begin
      data <= memory(address);
end Behaviorial;
```