```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity sr_flipflop is
      Port(set: in std_logic; reset:in std_logic; clk: in std_logic; q:
inout std_logic);
end sr_flipflop;

architecture Behaviorial of sr_flipflop is
begin
      p1: process(set,reset,clk)
      begin
            if(set='0' and reset='0') then q<=q;
            elsif(set='1' and reset='0') then q<='1';
            elsif(set='0' and reset='1') then q<='0';
            else q <= 'U';
            end if;
      end process p1;
end Behaviorial;
```