```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity demux_1x4 is
      Port(i: in std_logic; sel: in std_logic_vector(1 downto 0); o: out
std_logic_vector(3 downto 0));
end demux_1x4;

architecture Behaviorial of demux_1x4 is
begin
      with sel select
      o <= "000" & i when "00", "00" & i & '0' when "01", '0' & i & "00"
when "10", i & "000" when "11", unaffected when others;
end Behaviorial;
```