

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity half_adder is
    Port(a: in std_logic; b: in std_logic; s: out std_logic; c: out
std_logic);
end half_adder;

architecture Behavioral of half_adder is
begin
    s <= a xor b;
    c <= a and b;
end Behavioral;
```