```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity siso_register is
      Port(r_in: in std_logic; clk: in std_logic; rst: in std_logic;
r_out: out std_logic);
end siso_register;

architecture Behaviorial of siso_register is
begin
      p1: process(r_in,clk,rst)
      variable s: std_logic_vector(3 downto 0);
      begin
            if(rst='1') then s := "0000";
            elsif(rising_edge(clk)) then s:= r_in & s(3 downto 1); r_out<=
s(0);
            end if;
      end process p1;
end Behaviorial;
```