```
library IEEE;
use IEEE.std_logic_1164.all;

entity and_gate_3in is
      Port(a: in std_logic; b: in std_logic; c: in std_logic; o: out
std_logic);
end and_gate_3in;

architecture Dataflow of and_gate_3in is
begin
      o <= a and b and c;
end Dataflow;
```