```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity lacg is
      Port(a: in std_logic_vector(7 downto 0);
      b: in std_logic_vector(7 downto 0);
      c_in: in std_logic;
      sum: out std_logic_vector(7 downto 0);
      c_out: out std_logic);
end lacg;

architecture Behaviorial of lacg is
begin
      p1: process(a,b,c_in)
      Variable in_carry: std_logic_vector(8 downto 1);
      begin
            sum(0) <= a(0) xor b(0) xor c_in;
            in_carry(1):= (a(0) and b(0)) xor c_in;
            l1: for i in 1 to 7 loop
                  sum(i) <= a(i) xor b(1) xor in_carry(i);
            end loop;
            c_out <= in_carry(8);
      end process p1;
end Behaviorial;
```