```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity ram_16x8 is
      Generic(words: INTEGER:=16; bits: INTEGER:=8);
      Port(en: in std_logic;clk: in std_logic;address: in INTEGER range 0
to (words-1);d_in: in std_logic_vector((bits-1) downto 0);d_out: out
std_logic_vector((bits-1) downto 0));
end ram_16x8;

architecture Behaviorial of ram_16x8 is
type vector_array is array(0 to (words-1))of std_logic_vector(0 to 7);
Signal memory: vector_array;
begin
      p1:process(en,clk)
      begin
            if(en='1') then
                  if(rising_edge(clk)) then
                        memory(address) <= d_in;
                  end if;
            end if;
            d_out <= memory(address);
      end process p1;
end Behaviorial;
```