```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity mux_4x1 is
      Port(i: in std_logic_vector(3 downto 0); sel: in std_logic_vector(1
downto 0); o: out std_logic);
end mux_4x1;

architecture Behaviorial of mux_4x1 is
begin
      o <=  (i(0) and (not sel(1)) and (not sel(0))) or (i(1) and (not
sel(1)) and ( sel(0))) or (i(2) and ( sel(1)) and (not sel(0))) or (i(3)
and ( sel(1)) and ( sel(0)));
end Behaviorial;
```