```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity decoder_4x16 is
      Port(a: in std_logic;b: in std_logic; c: in std_logic; d: in
std_logic; o: out std_logic_vector(15 downto 0));
end decoder_4x16;

architecture Behaviorial of decoder_4x16 is
begin
      o(0) <= (not a) and (not b) and (not c) and (not d);
      o(1) <= (not a) and (not b) and (not c) and ( d);
      o(2) <= (not a) and (not b) and ( c) and (not d);
      o(3) <= (not a) and (not b) and ( c) and ( d);
      o(4) <= (not a) and ( b) and (not c) and (not d);
      o(5) <= (not a) and ( b) and (not c) and ( d);
      o(6) <= (not a) and ( b) and ( c) and (not d);
      o(7) <= (not a) and ( b) and ( c) and ( d);
      o(8) <= ( a) and (not b) and (not c) and (not d);
      o(9) <= ( a) and (not b) and (not c) and ( d);
      o(10) <= ( a) and (not b) and ( c) and (not d);
      o(11) <= ( a) and (not b) and ( c) and ( d);
      o(12) <= ( a) and ( b) and (not c) and (not d);
      o(13) <= ( a) and ( b) and (not c) and ( d);
      o(14) <= ( a) and ( b) and ( c) and (not d);
      o(15) <= ( a) and ( b) and ( c) and ( d);
end Behaviorial;
```