```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;

entity full_subtractor is
      Port(a: in std_logic; b: in std_logic; c:in std_logic; diff: out
std_logic; bor: out std_logic);
end full_subtractor;

architecture Behaviorial of full_subtractor is
begin
      diff <= a xor b xor c;
      bor <= ((not a) and c) or ((not a) and b) or (b and c);
end Behaviorial;
```