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Velika cesta 41
Zagreb - Odra 10020
CROATIA

Mixed Signal Management Board

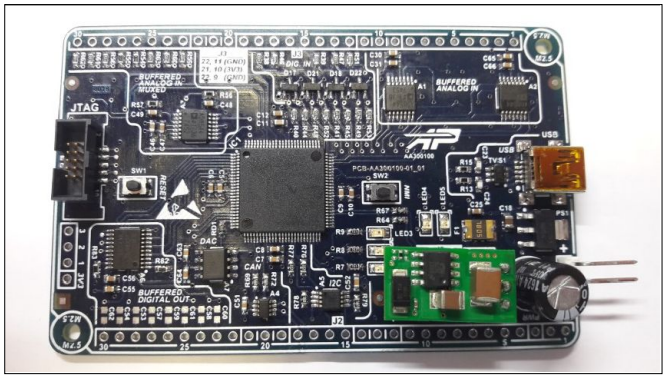
Catalogue number: AA300100
Document number: AA300100-020301010101

ALTIUM Project: MSMB10

Constructed by: 0113
Drawn by: M. Osonjacki - FER
Checked by: 0076
Approved by: 0113

Date: 03.10.2018.

PCB: PCB-AA300100-01_01



Rev.	Date	Author

PAGE 2
[02] Block diagram.SchDoc

PAGE 3
[03] Voltages - Contacts.SchDoc

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[05] Configurations.SchDoc

PAGE 6
[06] Mechanics.SchDoc

PAGE 6
[07] Interconnections.SchDoc

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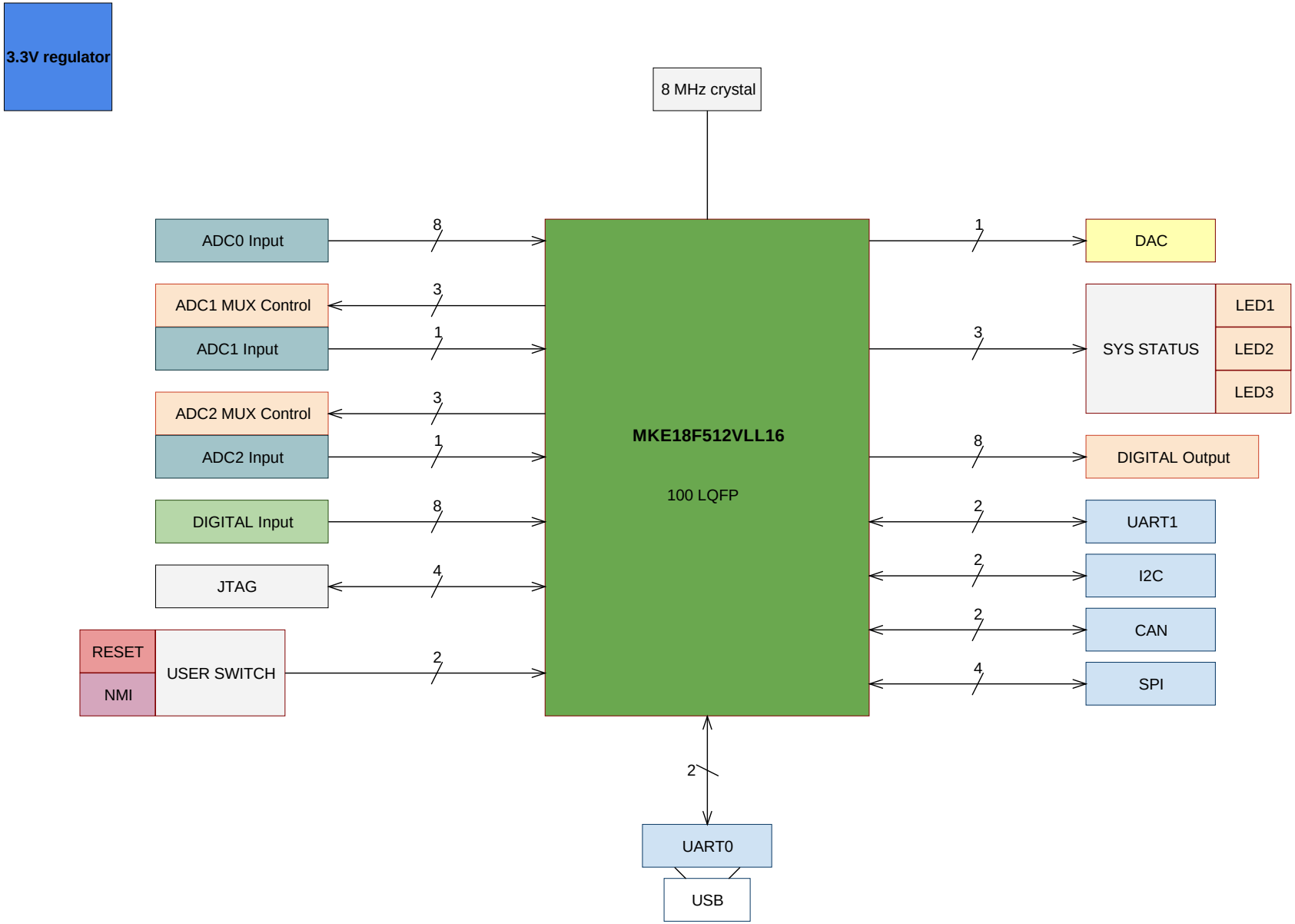
[99] Changes - Revisions.SchDoc



Measure: 1 : 1	Sheet: 2 / 16	Date	03.10.2018.	Document title: Mixed Signal Management Board Block diagram	
		Constructed by	0113		
		Drawn by	M. Osonjacki - FER		
		Checked by	0076		
		Approved by	0113		
		ALTPRO Velika cesta 41 10020 Zagreb CROATIA Made in Croatia	Catalogue number: AA300100	Document number: AA300100-020301010101	
Rev. Date	Name, surname	Int.mark: *		EXCHG. FOR: *	

[03] Voltages - Contacts.SchDoc

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Measure: 1 : 1	Sheet: 3 / 16	Date	03.10.2018.	Document title: Mixed Signal Management Board Voltage level list	
		Constructed by	0113		
		Drawn by	M. Osonjacki - FER		
		Checked by	0076		
		Approved by	0113		
		ALTPRO Velika cesta 41 10020 Zagreb CROATIA Made in Croatia	Catalogue number: AA300100	Document number: AA300100-020301010101	
Rev. Date	Name, surname	Int.mark: *		EXCHG. FOR: *	

08-B.12x1

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Measure: 1 : 1	Sheet: 4 / 16	Date	03.10.2018.	Document title: Mixed Signal Management Board Net list	
		Constructed by	0113		
		Drawn by	M. Osonjacki - FER		
		Checked by	0076		
		Approved by	0113		
		ALTPRO Velika cesta 41 10020 Zagreb CROATIA	Catalogue number: AA300100	Document number: AA300100-020301010101	
Rev. Date	Name, surname	Int.mark: *		EXCHG. FOR: *	

Made in Croatia

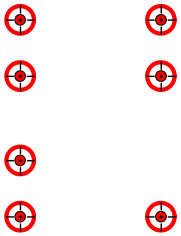
OR-B.12x1

MCU PIN CONFIGURATION

J2 PIN	NAZIV	J3 PIN	NAZIV	MCU PIN	NAZIV
1					
2					
3					
4					
5					
6	UART1 RX			56	PTC8/LPUART1_RX
7	UART1 TX			55	PTC9/LPUART1_TX
8	SPI SCK			48	PTB2/LPSPI0_SCK
9	SPI SIN			47	PTB3/ LPSPI0_SIN
10	SPI SOUT			28	PTB4/ LPSPI0_SOUT
11	SPI CS			27	PTB5/ LPSPI0_PCS1
12	GND				
13	3V3				
14	GND				
15	I2C SCL			41	PTD9/LPI2C_SCL
16	I2C SDA			42	PTD8/LPI2C_SDA
17	CAN H			29	PTC3/CAN0_TX
18	CAN L			30	PTC2/CAN0_RX
19	GND				
20	3V3				
21	GND				
22	DAC OUT			23	DAC0_OUT
23	PWM CH0			4	PTD0/FTM2_CH0
24	PWM CH1			3	PTD1/ FTM2_CH1
25	PWM CH2			9	PTE4/ FTM2_CH2
26	PWM CH3			8	PTE5/ FTM2_CH3
27	PWM CH4			6	PTE10/ FTM2_CH4
28	PWM CH5			5	PTE11/ FTM2_CH5
29	PWM CH6			2	PTE15/ FTM2_CH6
30	PWM CH7			1	PTE16/ FTM2_CH7
		1	ADC0 CH7	39	PTC1/ADC0_SE9
		2	ADC0 CH6	40	PTC0/ADC0_SE8
		3	ADC0 CH5	43	PTC17/ADC0_SE15
		4	ADC0 CH4	44	PTC16/ADC0_SE14
		5	ADC0 CH3	45	PTC15/ADC0_SE13
		6	ADC0 CH2	46	PTC14/ADC0_SE12
		7	ADC0 CH1	53	PTB1/ADC0_SE5
		8	ADC0 CH0	54	PTB0/ADC0_SE4
		9	GND		
		10	3V3		
		11	GND		
		12	DIN CH7	63	PTB17
		13	DIN CH6	64	PTB16
		14	DIN CH5	65	PTB15
		15	DIN CH4	66	PTB14
		16	DIN CH3	67	PTB13
		17	DIN CH2	68	PTB12
		18	DIN CH1	74	PTB11
		19	DIN CH0	75	PTB10
		20	GND		
		21	3V3		
		22	GND		
		23	ADC1 CTRL0	82	PTA16
		24	ADC1 CTRL1	83	PTA15
		25	ADC1 CTRL2	84	PTE6
		26	ADC1 CH2	85	PTE2/ADC1_SE10
		27	ADC2 CH2	89	PTA13/ADC2_SE4
		28	ADC2 CTRL0	90	PTA12
		29	ADC2 CTRL1	93	PTE1
		30	ADC2 CTRL2	94	PTE0

Mjerilo: 1 : 1	List: 5 / 16	Datum	03.10.2018.	Naziv dokumenta: Mixed Signal Management Board	
		Konstruirao/la	0113		
		Crtao/la	M. Osonjacki - FER	Configuration list	
		Kontrolirao/la	0076		
		Odobrio/la	0113		
		ALTPRO Made in Croatia, Velika cesta 41, 10020 Zagreb, CROATIA	Kataloški broj: AA300100	Broj dokumenta: AA300100-020301010101	
Rev. Datum	Ime i prezime	Int.ozn.: *		ZAMJ.ZA: *	

[06] Mechanics.SchDoc



Mjerilo: 1 : 1	List: 6 / 16	Datum	03.10.2018.	Naziv dokumenta: Mixed Signal Management Board Mechanics	
		Konstruirao/la	0113		
		Crtao/la	M. Osonjacki - FER		
		Kontrolirao/la	0076		
		Odobrio/la	0113		
		ALTPRO Velika cesta 41 10020 Zagreb CROATIA	Kataloški broj: AA300100	Broj dokumenta: AA300100-020301010101	
Rev. Datum	Ime i prezime	Int.ozn.: *		ZAMJ.ZA: *	

[07] Interconnections.SchDoc

D1 HSMS-BAT54S,215 — GND, 3V3, 3 JTAG_TMS
D2 HSMS-BAT54S,215 — GND, 3V3, 3 JTAG_TCLK
D3 HSMS-BAT54S,215 — GND, 3V3, 3 JTAG_TDO
D4 HSMS-BAT54S,215 — GND, 3V3, 3 JTAG_TDI
D5 HSMS-BAT54S,215 — GND, 3V3, 3 RST

[09] Power managment.SchDoc — V_DRV, 5V_USB

J3 H1x30: 30 ADC2_CTRL2_IN, 29 ADC2_CTRL1_IN, 28 ADC2_CTRL0_IN, 27 ADC2_CH2_IN, 26 ADC1_CH2_IN, 25 ADC1_CTRL2_IN, 24 ADC1_CTRL1_IN, 23 ADC1_CTRL0_IN, 22, 21, 20, 19 DIN_CH0_IN, 18 DIN_CH1_IN, 17 DIN_CH2_IN, 16 DIN_CH3_IN, 15 DIN_CH4_IN, 14 DIN_CH5_IN, 13 DIN_CH6_IN, 12 DIN_CH7_IN, 11, 10, 9, 8 ADC0_CH0_IN, 7 ADC0_CH1_IN, 6 ADC0_CH2_IN, 5 ADC0_CH3_IN, 4 ADC0_CH4_IN, 3 ADC0_CH5_IN, 2 ADC0_CH6_IN, 1 ADC0_CH7_IN

[12] Fast digital inputs.SchDoc: DIN_CH0_IN … DIN_CH7_IN → DIN_CH0 … DIN_CH7

[11] Fast analog inputs.SchDoc: ADC0_CH0_IN … ADC0_CH7_IN → ADC0_CH0 … ADC0_CH7

[13] Analog inputs.SchDoc: ADC1_CH2_IN, ADC1_CTRL0_IN, ADC1_CTRL1_IN, ADC1_CTRL2_IN, ADC2_CH2_IN, ADC2_CTRL0_IN, ADC2_CTRL1_IN, ADC2_CTRL2_IN

JTAG: R1 0R, R2 10k, R3 10k, R4 10k (3V3); 1 GND, 2 JTAG_TMS, 3 GND, 4 JTAG_TCLK, 5 GND, 6 JTAG_TDO, 7 GND, 8 JTAG_TDI, 9 GND, 10 RST — SHF-105-01-L-D-SM

[08] Chip.SchDoc: DIN_CH0 … DIN_CH7, ADC0_CH0 … ADC0_CH7, ADC1_CH2, ADC1_CTRL0 … ADC1_CTRL2, ADC2_CH2, ADC2_CTRL0 … ADC2_CTRL2, JTAG_TMS, JTAG_TCLK, JTAG_TDO, JTAG_TDI, RST, UART0_RX, UART0_TX, UART1_RX, UART1_TX, SPI_SCK, SPI_SOUT, SPI_CS, SPI_SIN, CAN_TX, CAN_RX, I2C_SCL, I2C_SDA, DAC_OUT, PWM_CH0 … PWM_CH7

[10] Mini USB.SchDoc: UART0_RX, UART0_TX

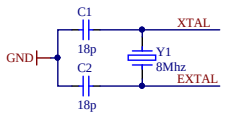
[14] Output communication.SchDoc: UART1_RX, UART1_TX, SPI_SCK, SPI_SOUT, SPI_CS, SPI_SIN, CAN_TX, CAN_RX, I2C_SCL, I2C_SDA → UART1_RX_IN, UART1_TX_OUT, SPI_SCK_SOUT, SPI_SOUT_OUT, SPI_CS_OUT, SPI_SIN_IN, CANH, CANL, I2C_SCL_OUT, I2C_SDA_OUT

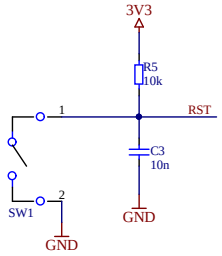
[15] Outputs.SchDoc: DAC_OUT, PWM_CH0 … PWM_CH7 → BUFF_DAC_OUT, PWM_BUFF_CH0 … PWM_BUFF_CH7

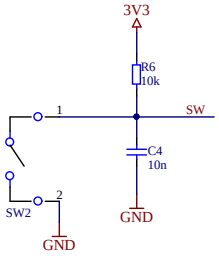
J2 H1x30: 1, 2, 3 BLANK, 4, 5, 6 UART1_RX_IN, 7 UART1_TX_OUT, 8 SPI_SCK_SOUT, 9 SPI_SIN_IN, 10 SPI_SOUT_OUT, 11 SPI_CS_OUT, 12, 13, 14, 15 I2C_SCL_OUT, 16 I2C_SDA_OUT, 17 CANH, 18 CANL, 19, 20, 21, 22 BUFF_DAC_OUT, 23 PWM_BUFF_CH0, 24 PWM_BUFF_CH1, 25 PWM_BUFF_CH2, 26 PWM_BUFF_CH3, 27 PWM_BUFF_CH4, 28 PWM_BUFF_CH5, 29 PWM_BUFF_CH6, 30 PWM_BUFF_CH7

MCU channels and periphery channels are NOT equal.
Please check pages 5 and 8.

Measure: 1 : 1	Sheet: 7 / 16	Date	03.10.2018.	Document title:	Mixed Signal Management Board
		Constructed by	0113		Interconnections
		Drawn by	M. Osonjacki - FER		
		Checked by	0076		
		Approved by	0113		
Rev. Date	Name, surname	ALTPRO Velika cesta 41 10020 Zagreb CROATIA Made in Croatia	Int.mark: *	Catalogue number: AA300100	Document number: AA300100-020301010101
				EXCHG. FOR: *	





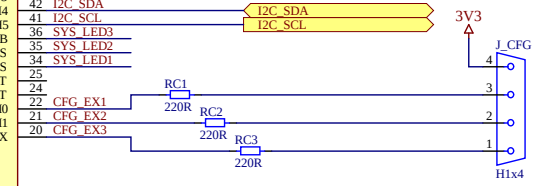


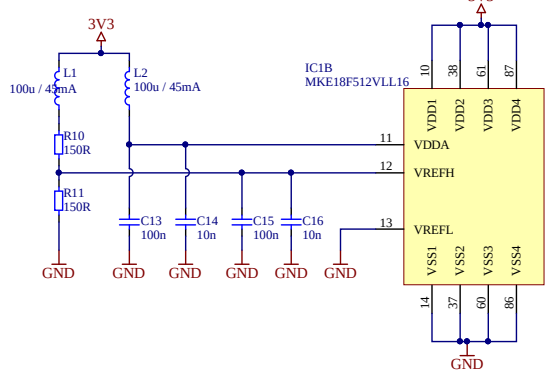
IC1A

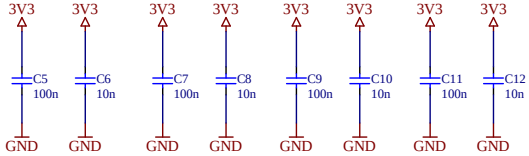
MKE18F512VLL16

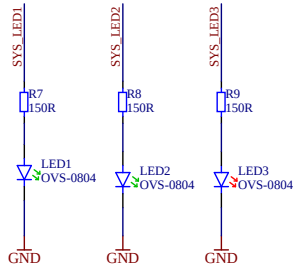
	79	PTA0/ADC0_SE0/ACMP0_IN0/TSI0_CH17/FTM2_CH1/LPI2C0_SCLS/FXIO_D2/FTM2_QD_PHA/LPUART0_CTS/TRGMUX_OUT3	
	78	PTA1/ADC0_SE1/ACMP0_IN1/FTM1_CH1/LPI2C0_SDAS/FXIO_D3/FTM1_QD_PHA/LPUART0_RTS/TRGMUX_OUT0	
UART0_RX	73	PTA2/ADC1_SE0/TSI0_CH13/FTM3_CH0/LPI2C0_SDA/EWM_OUT/LPUART0_RX	
UART0_TX	72	PTA3/ADC1_SE1/FTM3_CH1/LPI2C0_SCL/EWM_IN/LPUART0_TX	
JTAG_TMS	98	PTA4/JTAG_TMS/SWD_DIO/ACMP0_OUT/EWM_OUT	
RST	97	PTA5/RESET/TCLK1/JTAG_TRST	
	58	PTA6/ADC0_SE2/ACMP1_IN0/TSI0_CH10/FTM0_FLT1/LPSPI1_PCS1/EMVSIM_RST/LPUART1_CTS	
	57	PTA7/ADC0_SE3/ACMP1_IN1/TSI0_CH11/FTM0_FLT2/RTC_CLKIN/EMVSIM_CLK/LPUART1_RTS	PTD0/ADC2_SE0/TSI0_CH4/FTM0_CH2/LPSPI1_SCK/FTM2_CH0/EMVSIM_RST/FXIO_D0/TRGMUX_OUT1
	100	PTA8/LPUART3_RX/LPSPI2_SOUT/FXIO_D6/FTM3_FLT3	PTD1/ADC2_SE1/TSI0_CH5/FTM0_CH3/LPSPI1_SIN/FTM2_CH1/EMVSIM_CLK/FXIO_D1/TRGMUX_OUT2
	99	PTA9/LPUART3_TX/LPSPI2_PCS0/FXIO_D7/FTM3_FLT2/FTM1_FLT3	PTD2/ADC1_SE2/TSI0_CH18/FTM3_CH4/LPSPI1_SOUT/FXIO_D4/EMVSIM_IO/TRGMUX_IN5
JTAG_TDO	92	PTA10/JTAG_TDO/NOETM_TRACE_SWO/FTM1_CH4/FXIO_D0	PTD3/ADC1_SE3/TSI0_CH19/FTM3_CH5/LPSPI1_PCS0/FXIO_D5/EMVSIM_VCCEN/TRGMUX_IN4/NMI
	91	PTA11/FTM1_CH5/FXIO_D1	PTD4/ADC1_SE6/TSI0_CH20/FTM0_FLT3/FTM3_FLT3/EMVSIM_PD
ADC2_CTRL0	90	PTA12/ADC2_SE5/FTM1_CH6/CAN1_RX/LPI2C1_SDAS	PTD5/TSI0_CH21/FTM2_CH3/LPTMR0_ALT2/FTM2_FLT1/TRGMUX_IN7
ADC2_CH2	89	PTA13/ADC2_SE4/FTM1_CH7/CAN1_TX/LPI2C1_SCLS	PTD6/ACMP0_IN7/TSI0_CH22/LPUART2_RX/FTM2_FLT2
	88	PTA14/FTM0_FLT0/FTM3_FLT1/EWM_IN/FTM1_FLT0/BUSOUT	PTD7/ACMP0_IN6/TSI0_CH23/LPUART2_TX/FTM2_FLT3
ADC1_CTRL1	83	PTA15/ADC1_SE12/FTM1_CH2/LPSPI0_PCS3/LPSPI2_PCS3	PTD8/ACMP1_IN6/LPI2C1_SDA/FTM2_FLT2/FTM1_CH4
ADC1_CTRL0	82	PTA16/ADC1_SE13/FTM1_CH3/LPSPI1_PCS2	PTD9/ACMP1_IN5/LPI2C1_SCL/FTM2_FLT3/FTM1_CH5
	62	PTA17/FTM0_CH6/FTM3_FLT0/EWM_OUT	PTD10/FTM2_CH0/FTM2_QD_PHB
			PTD11/FTM2_CH1/FTM2_QD_PHA/LPUART2_CTS
ADC0_CH0	54	PTB0/ADC0_SE4/LPUART0_RX/LPSPI0_PCS0/LPTMR0_ALT3	PTD12/FTM2_CH2/LPI2C1_HREQ/LPUART2_RTS
ADC0_CH1	53	PTB1/ADC0_SE5/LPUART0_TX/LPSPI0_SOUT/TCLK0	PTD13/FTM2_CH4/LPUART3_RX/RTC_CLKOUT
SPI_SCK	48	PTB2/ADC0_SE6/FTM1_CH0/LPSPI0_SCK/FTM1_QD_PHB/TRGMUX_IN3	PTD14/FTM2_CH5/LPUART3_TX/CLKOUT
SPI_SIN	47	PTB3/ADC0_SE7/FTM1_CH1/LPSPI0_SIN/FTM1_QD_PHA/TRGMUX_IN2	PTD15/ACMP2_IN1/FTM0_CH0
SPI_SOUT	28	PTB4/ACMP1_IN2/TSI0_CH8/FTM0_CH4/LPSPI0_SOUT/TRGMUX_IN1	PTD16/ACMP2_IN0/FTM0_CH1
SPI_CS	27	PTB5/TSI0_CH9/FTM0_CH5/LPSPI0_PCS1/TRGMUX_IN0/ACMP1_OUT	PTD17/FTM0_FLT2/LPUART2_RX
XTAL	16	PTB6/XTAL/LPI2C0_SDA	
EXTAL	15	PTB7/EXTAL/LPI2C0_SCL	
	77	PTB8/ADC2_SE11/FTM3_CH0	
	76	PTB9/ADC2_SE10/FTM3_CH1/LPI2C0_SCLS	
DIN_CH0	75	PTB10/ADC2_SE9/FTM3_CH2/LPI2C0_SDAS	
DIN_CH1	74	PTB11/ADC2_SE8/FTM3_CH3/LPI2C0_HREQ	
DIN_CH2	68	PTB12/ADC1_SE7/FTM0_CH0/FTM3_FLT2/CAN2_RX	
DIN_CH3	67	PTB13/ADC1_SE8/FTM0_CH1/FTM3_FLT1/CAN2_TX	
DIN_CH4	66	PTB14/ADC1_SE9/FTM0_CH2/LPSPI1_SCK	
DIN_CH5	65	PTB15/ADC1_SE14/FTM0_CH3/LPSPI1_SIN	PTE0/ADC2_SE7/LPSPI0_SCK/TCLK1/LPI2C1_SDA/FTM1_FLT2
DIN_CH6	64	PTB16/ADC1_SE15/FTM0_CH4/LPSPI1_SOUT	PTE1/ADC2_SE6/LPSPI0_SIN/LPI2C0_HREQ/LPI2C1_SCL/FTM1_FLT1
DIN_CH7	63	PTB17/ADC2_SE3/ACMP2_IN7/FTM0_CH5/LPSPI1_PCS3	PTE2/ADC1_SE10/LPSPI0_SOUT/LPTMR0_ALT3/FTM3_CH6/LPUART1_CTS
			PTE3/TSI0_CH24/FTM0_FLT0/LPUART2_RTS/FTM2_FLT0/TRGMUX_IN6/ACMP2_OUT
			PTE4/TSI0_CH12/BUSOUT/FTM2_QD_PHB/FTM2_CH2/CAN0_RX/FXIO_D6/EWM_OUT
			PTE5/TSI0_CH0/TCLK2/FTM2_QD_PHA/FTM2_CH3/CAN0_TX/FXIO_D7/EWM_IN
ADC0_CH6	40	PTC0/ADC0_SE8/ACMP1_IN4/FTM0_CH0/FTM1_CH6	PTE6/ADC1_SE11/LPSPI0_PCS2/FTM3_CH7/LPUART1_RTS
ADC0_CH7	39	PTC1/ADC0_SE9/ACMP1_IN3/FTM0_CH1/FTM1_CH7	PTE7/ADC2_SE2/ACMP2_IN6/FTM0_CH7/FTM3_FLT0
CAN_RX	30	PTC2/ADC0_SE10/ACMP0_IN5/XTAL32/FTM0_CH2/CAN0_RX	PTE8/ACMP0_IN3/FTM0_CH6
CAN_TX	29	PTC3/ADC0_SE11/ACMP0_IN4/EXTAL32/FTM0_CH3/CAN0_TX	PTE9/ACMP2_IN2/DAC0_OUT/FTM0_CH7/LPUART2_CTS
JTAG_TCLK	96	PTC4/JTAG_TCLK/SWD_CLK/ACMP0_IN2/FTM1_CH0/RTC_CLKOUT/EWM_IN/FTM1_QD_PHB	PTE10/ADC2_SE12/TSI0_CH2/CLKOUT/LPSPI2_PCS1/FTM2_CH4/EMVSIM_IO/FXIO_D4/TRGMUX_OUT4
JTAG_TDI	95	PTC5/JTAG_TDI/TSI0_CH14/FTM2_CH0/RTC_CLKOUT/LPI2C1_HREQ/EMVSIM_PD/FTM2_QD_PHB	PTE11/ADC2_SE13/TSI0_CH3/LPTMR0_ALT1/FTM2_CH5/EMVSIM_VCCEN/FXIO_D5/TRGMUX_OUT5
	81	PTC6/ADC1_SE4/TSI0_CH15/LPUART1_RX/CAN1_RX/FTM3_CH2	PTE12/FTM0_FLT3/LPUART2_TX
	80	PTC7/ADC1_SE5/TSI0_CH16/LPUART1_TX/CAN1_TX/FTM3_CH3	PTE13/TSI0_CH1/LPSPI2_PCS2/FTM2_FLT0/EMVSIM_PD
UART1_RX	56	PTC8/ADC2_SE14/LPUART1_RX/FTM1_FLT0/LPUART0_CTS	PTE14/ACMP2_IN3/FTM0_FLT1/FTM2_FLT1
UART1_TX	55	PTC9/ADC2_SE15/LPUART1_TX/FTM1_FLT1/LPUART0_RTS	PTE15/TSI0_CH6/LPUART3_CTS/LPSPI2_SCK/FTM2_CH6/FXIO_D2/TRGMUX_OUT6
	52	PTC10/FTM3_CH4/TRGMUX_IN11	PTE16/TSI0_CH7/LPUART3_RTS/LPSPI2_SIN/FTM2_CH7/FXIO_D3/TRGMUX_OUT7
	51	PTC11/FTM3_CH5/TRGMUX_IN10	
	50	PTC12/FTM3_CH6/FTM2_CH6/LPUART3_CTS	
	49	PTC13/FTM3_CH7/FTM2_CH7/LPUART3_RTS	
ADC0_CH2	46	PTC14/ADC0_SE12/ACMP2_IN5/FTM1_CH2/TRGMUX_IN9	
ADC0_CH3	45	PTC15/ADC0_SE13/ACMP2_IN4/FTM1_CH3/TRGMUX_IN8	
ADC0_CH4	44	PTC16/ADC0_SE14/FTM1_FLT2/CAN2_RX/LPI2C1_SDAS	
ADC0_CH5	43	PTC17/ADC0_SE15/ACMP1_IN7/FTM1_FLT3/CAN2_TX/LPI2C1_SCLS	

PWM_CH0	4	PWM_CH0	PWM_CH0
PWM_CH1	3	PWM_CH1	PWM_CH1
	71		
SW	70	SW	
	69		
	33		
	32		
	31		
I2C_SDA	42	I2C_SDA	I2C_SDA
I2C_SCL	41	I2C_SCL	I2C_SCL
SYS_LED3	36	SYS_LED3	
SYS_LED2	35	SYS_LED2	
SYS_LED1	34	SYS_LED1	
	25		
	24		
CFG_EX1	22	CFG_EX1	
CFG_EX2	21	CFG_EX2	
CFG_EX3	20	CFG_EX3	
ADC2_CTRL2	94	ADC2_CTRL2	ADC2_CTRL2
ADC2_CTRL1	93	ADC2_CTRL1	ADC2_CTRL1
ADC1_CH2	85	ADC1_CH2	ADC1_CH2
	18		
PWM_CH2	9	PWM_CH2	PWM_CH2
PWM_CH3	8	PWM_CH3	PWM_CH3
ADC1_CTRL2	84	ADC1_CTRL2	ADC1_CTRL2
	59		
	26		
DAC_OUT	23	DAC_OUT	DAC_OUT
PWM_CH4	6	PWM_CH4	PWM_CH4
PWM_CH5	5	PWM_CH5	PWM_CH5
	19		
	7		
	17		
PWM_CH6	2	PWM_CH6	PWM_CH6
PWM_CH7	1	PWM_CH7	PWM_CH7









Measure: 1 : 1	Sheet: 8 / 16	Date	03.10.2018.
		Constructed by	0113
		Drawn by	M. Osonjacki - FER
		Checked by	0076
		Approved by	0113
Rev.	Date	Name, surname	Int.mark: *

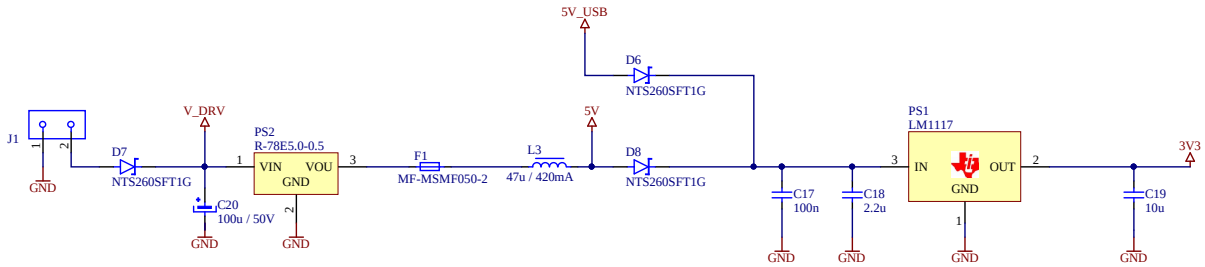
ALTPRO
Made in Croatia
Velika cesta 41
10020 Zagreb
CROATIA

Catalogue number:	AA300100
Document number:	AA300100-020301010101
EXCHG. FOR: *	

Document title: Mixed Signal Management Board
MCU

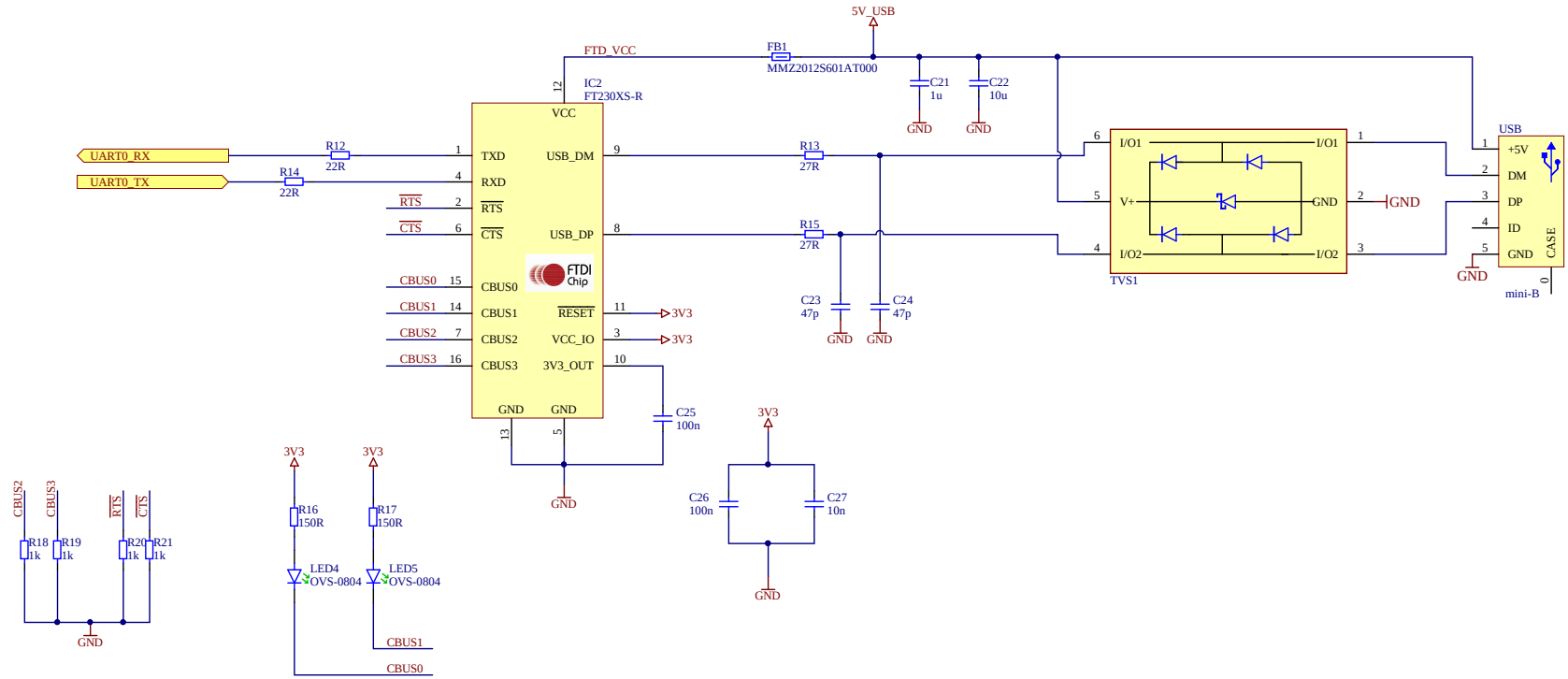
08-8-1201

Text



Measure: 1 : 1	Sheet: 9 / 16	Date	03.10.2018.		Document title: Mixed Signal Management Board	
		Constructed by	0113		Power block	
		Drawn by	M. Osonjacki - FER			
		Checked by	0076			
		Approved by	0113			
		ALTPRO Velika cesta 41 10020 Zagreb CROATIA Made in Croatia		Catalogue number: AA300100	Document number: AA300100-020301010101	
Rev. Date	Name, surname	Int.mark: *			EXCHG. FOR: *	

[10] Mini USB.SchDoc



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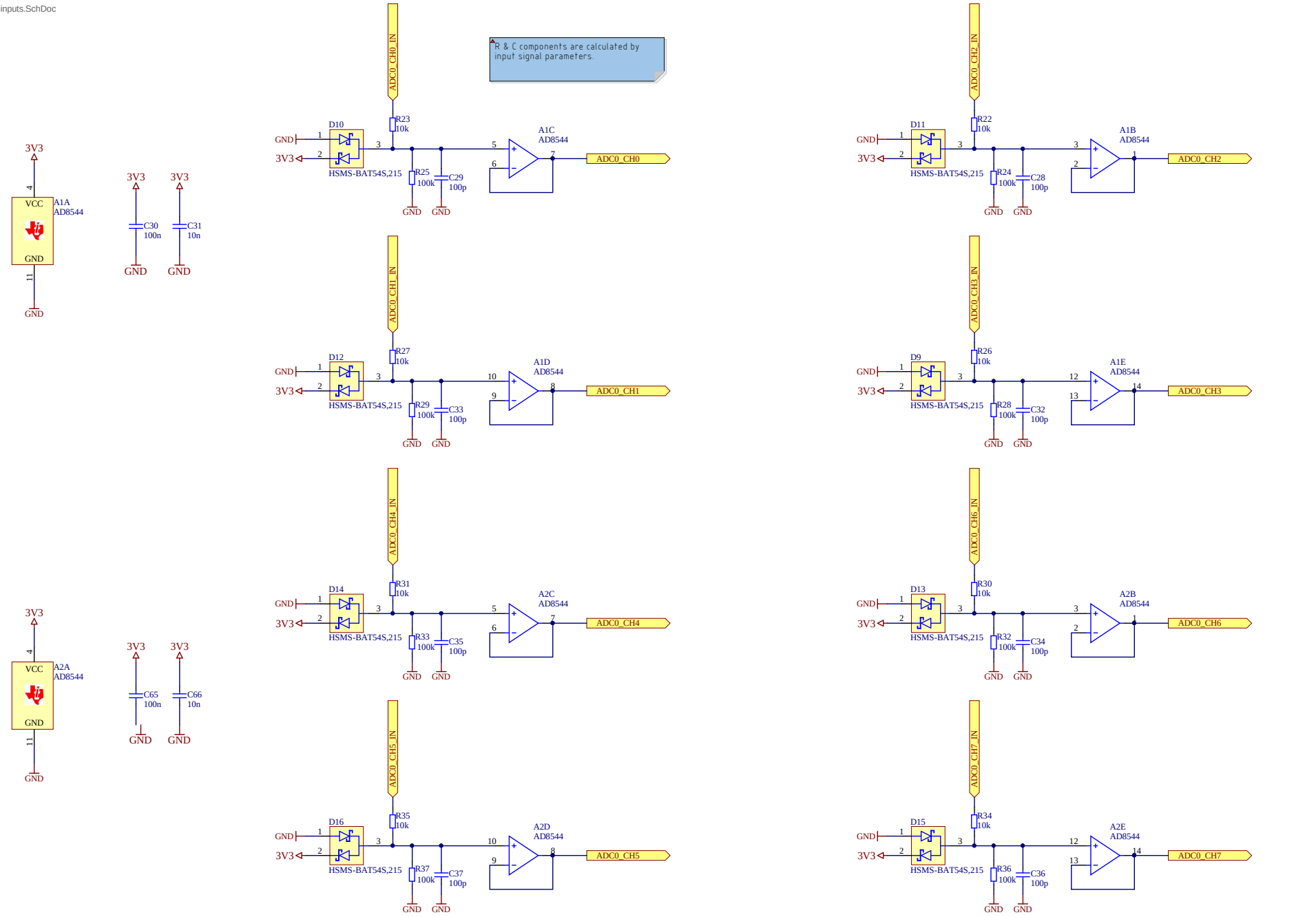
		Drawn by	M. Osonjacki - FER		
		Checked by	0076		
		Approved by	0113		
		ALTPRO Velika cesta 41 10020 Zagreb CROATIA Made in Croatia	Catalogue number: AA300100	Document number: AA300100-020301010101	
Rev. Date	Name, surname	Int.mark: *		EXCHG. FOR: *	



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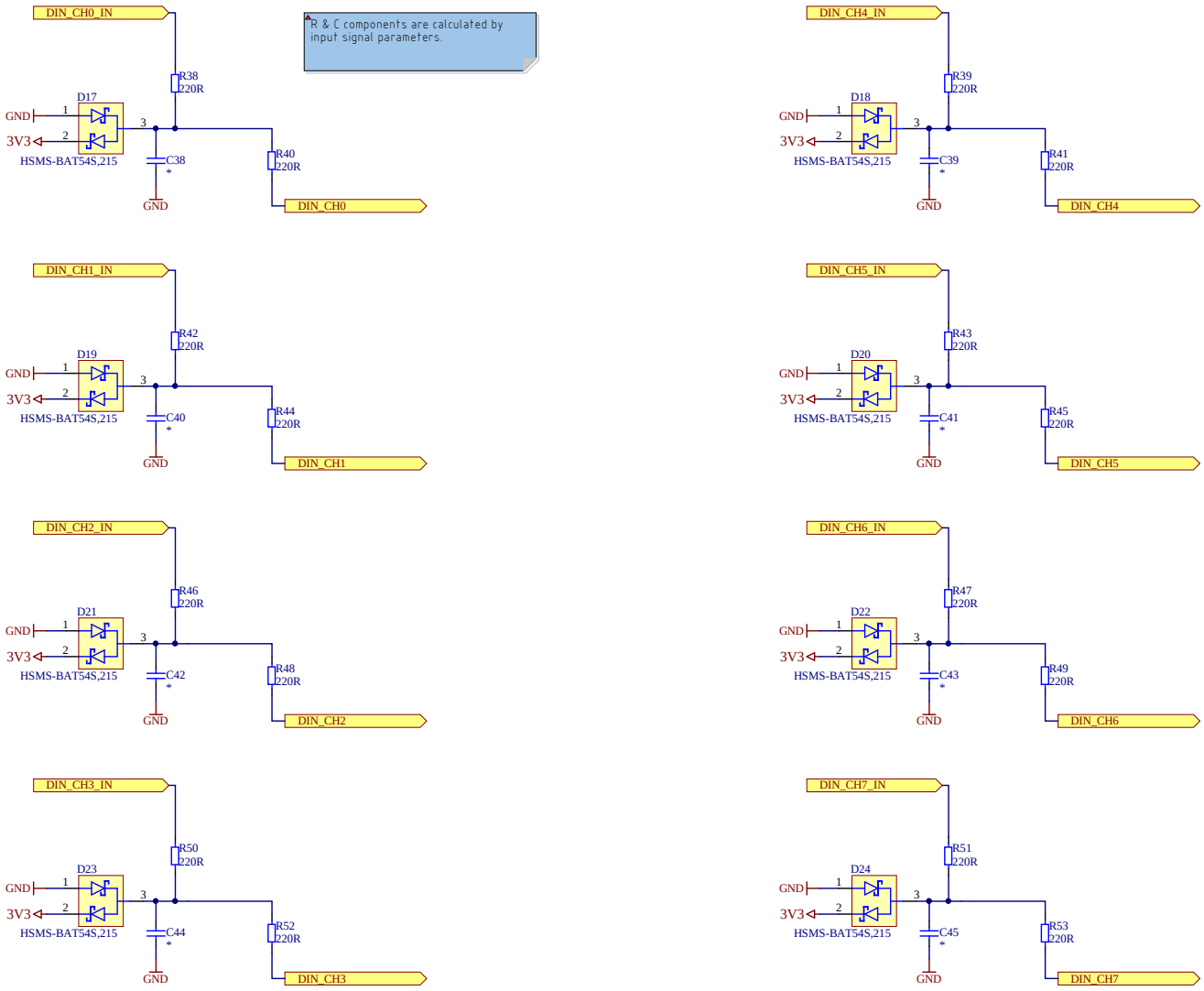
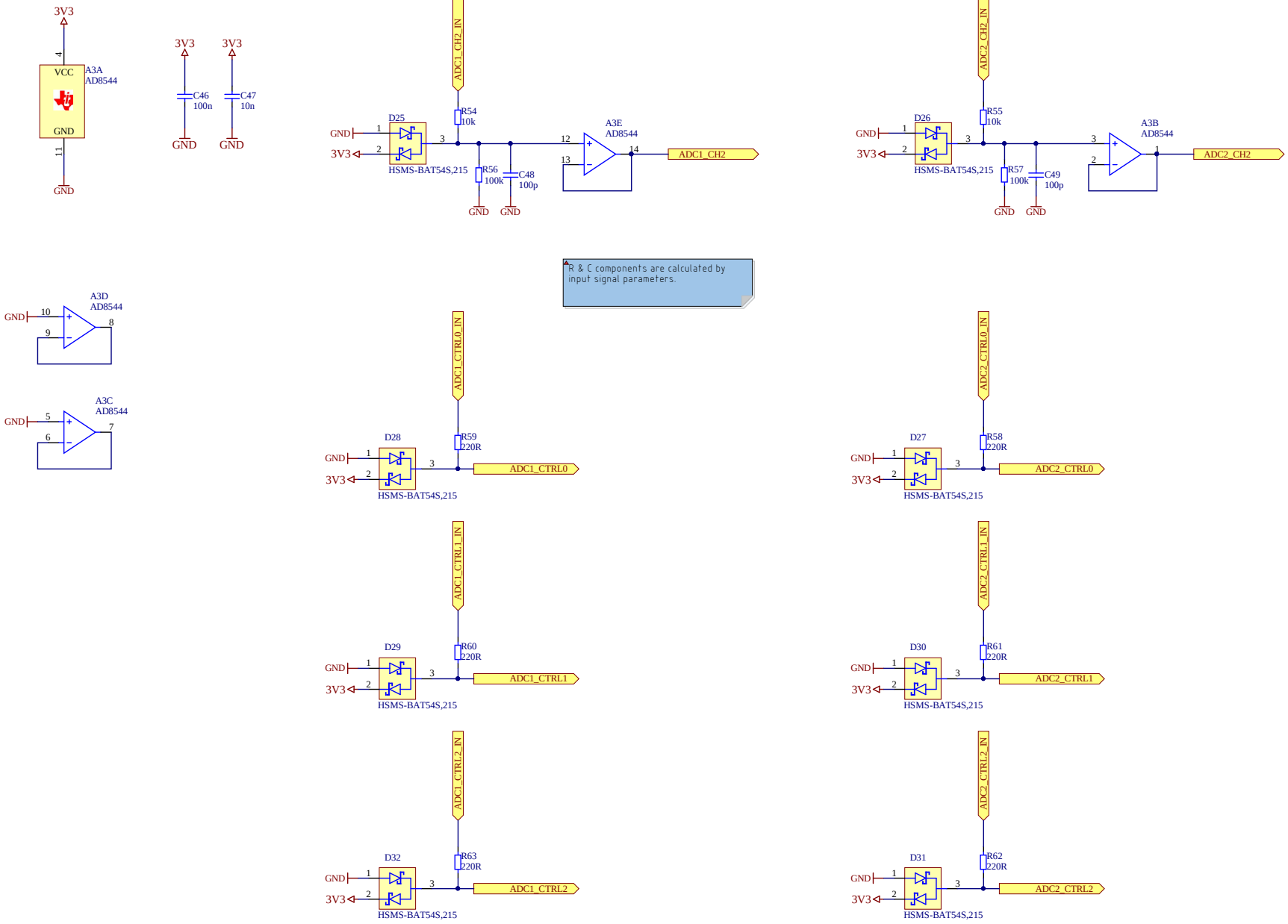
		Constructed by	0113		
		Drawn by	M. Osonjacki - FER		
		Checked by	0076		
		Approved by	0113		
		ALTPRO Velika cesta 41 10020 Zagreb CROATIA Made in Croatia	Catalogue number: AA300100	Document number: AA300100-020301010101	
Rev. Date	Name, surname	Int.mark: *		EXCHG. FOR: *	

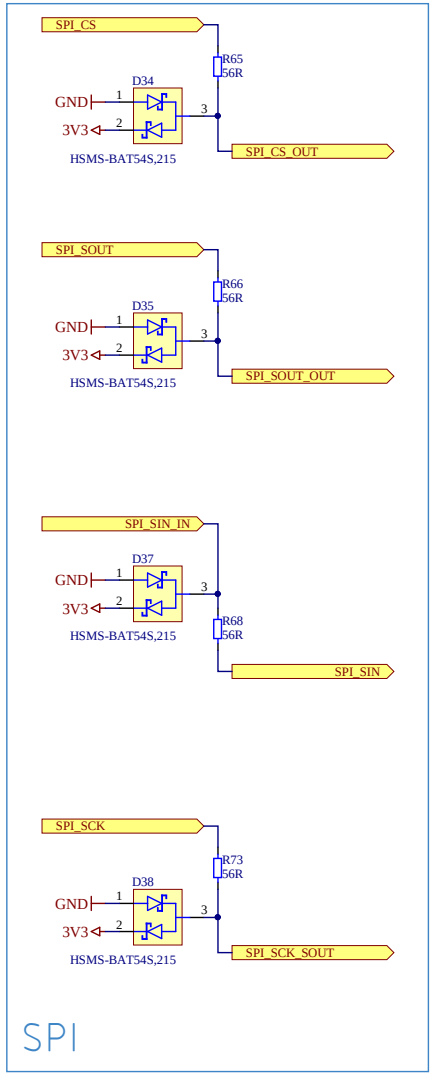


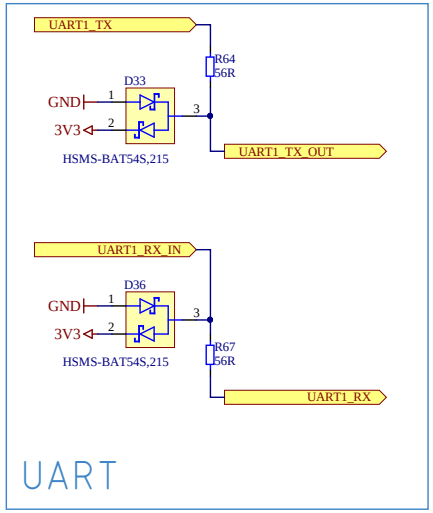
Measure: 1 : 1	Sheet: 12 / 16	Date	03.10.2018.	Document title: Mixed Signal Management Board Fast digital inputs (8 Ch)	
		Constructed by	0113		
		Drawn by	M. Osonjacki - FER		
		Checked by	0076		
		Approved by	0113		
		ALTPRO Velika cesta 41 10020 Zagreb CROATIA Made in Croatia	Catalogue number: AA300100	Document number: AA300100-020301010101	
Rev. Date	Name, surname	Int.mark: *		EXCHG. FOR: *	

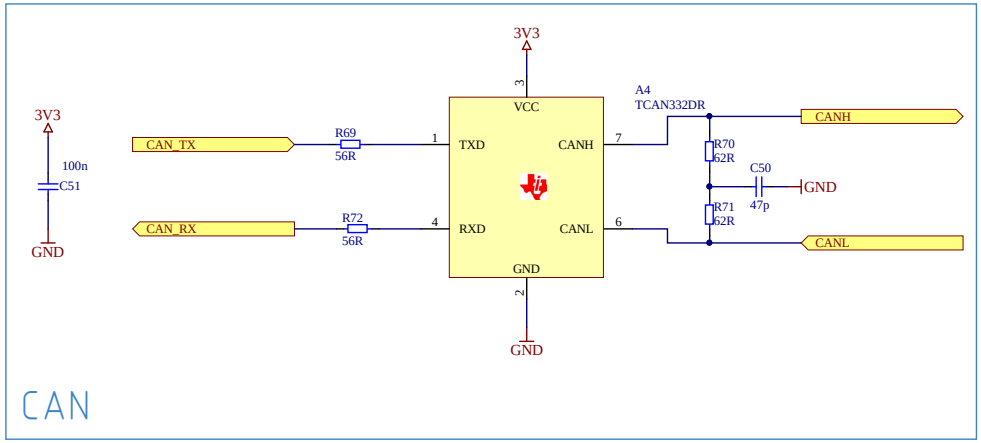
[13] Analog inputs.SchDoc

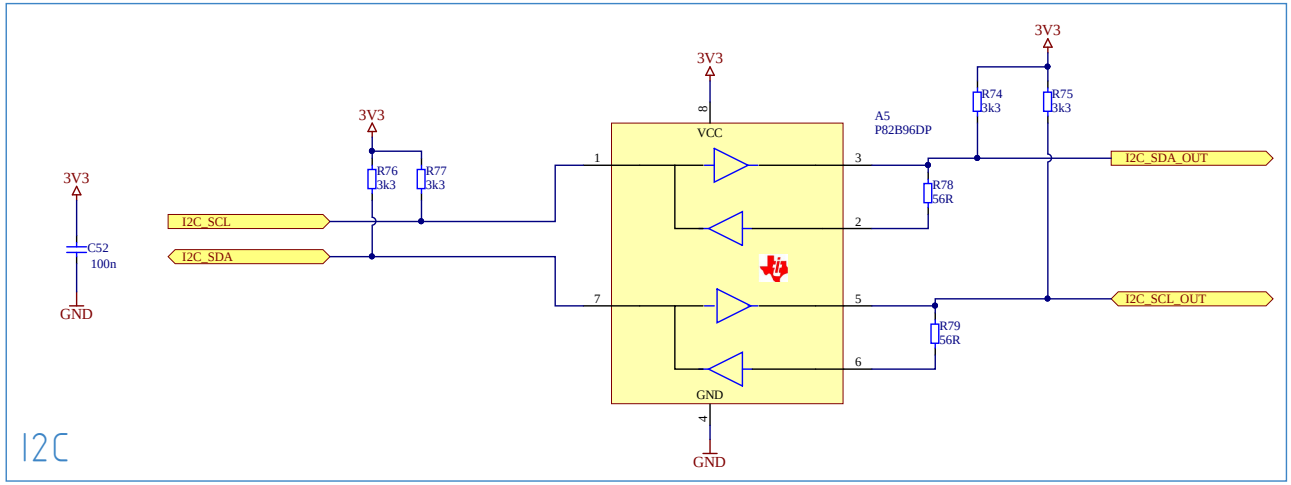


Measure: 1 : 1	Sheet: 13 / 16	Date	03.10.2018.	Document title: Mixed Signal Management Board	
		Constructed by	0113	Analog inputs (2 Ch) & controls	
		Drawn by	M. Osonjacki - FER		
		Checked by	0076		
		Approved by	0113		
		ALTPRO Velika cesta 41 10020 Zagreb CROATIA Made in Croatia		Catalogue number: AA300100	Document number: AA300100-020301010101
Rev.	Date / Name, surname	Int.mark: *			EXCHG. FOR: *

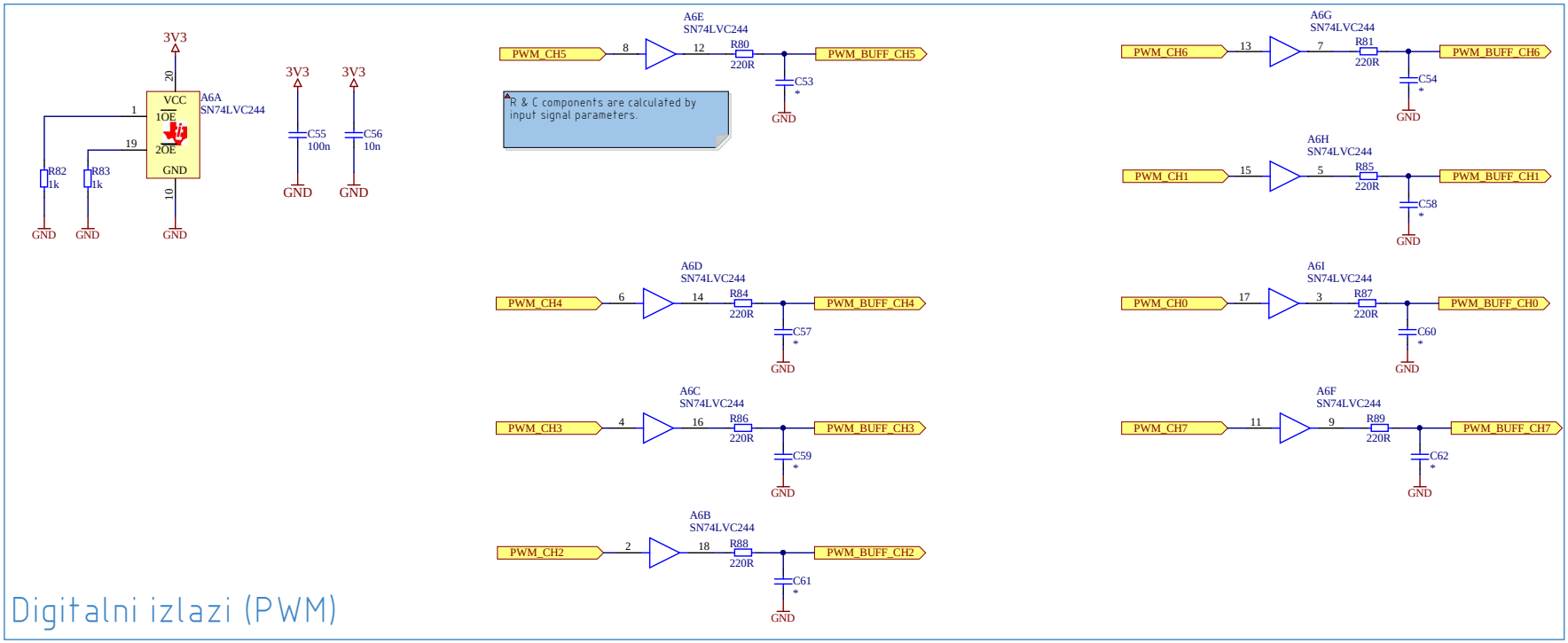


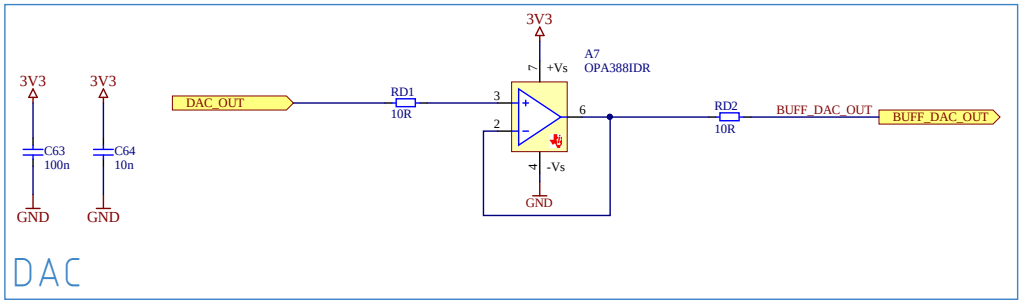






Measure: 1 : 1	Sheet: 14 / 16	Date	03.10.2018.	Document title: Mixed Signal Management Board	
		Constructed by	0113	Communication (SPI, UART, CAN, I2C)	
		Drawn by	M. Osonjacki - FER		
		Checked by	0076		
		Approved by	0113		
		ALTPRO Velika cesta 41 10020 Zagreb CROATIA Made in Croatia		Catalogue number: AA300100	Document number: AA300100-020301010101
Rev. Date	Name, surname	Int.mark: *			EXCHG. FOR: *





Measure: 1 : 1	Sheet: 15 / 16	Date	03.10.2018.	Document title: Mixed Signal Management Board			
		Constructed by	0113				
		Drawn by	M. Osonjacki - FER				
		Checked by	0076	Outputs (PWM 8 Ch, DAC)			
		Approved by	0113				
		ALTPRO Velika cesta 41 10020 Zagreb CROATIA Made in Croatia		Catalogue number: AA300100	Document number: AA300100-020301010101		
Rev.	Date	Name, surname	Int.mark: *		EXCHG. FOR: *		

[99] Changes - Revisions.SchDoc

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Measure: 1 : 1	Sheet: 16 / 16	Date	03.10.2018.		Document title: Mixed Signal Management Board Changes
		Constructed by	0113		
		Drawn by	M. Osonjacki - FER		
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		Approved by	0113		
		ALTPRO Velika cesta 41 10020 Zagreb CROATIA Made in Croatia	Catalogue number: AA300100		Document number: AA300100-020301010101
Rev. Date	Name, surname	Int.mark: *			EXCHG. FOR: *

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