ELEG 5765 Fundamentals of Automotive Integrated Circuits

Lecture 4

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Lecture 4: SPI & Project_1

Outline

- SPI
- Project_1

SPI Materials

- https://blog.csdn.net/u010632165/article/details/109460814
- https://blog.csdn.net/as480133937/article/details/105764119
- https://blog.csdn.net/Teminator_/article/details/141279117
- Infineon-TLE92466ED-DataSheet-v01_20-EN.pdf

VCS Materials

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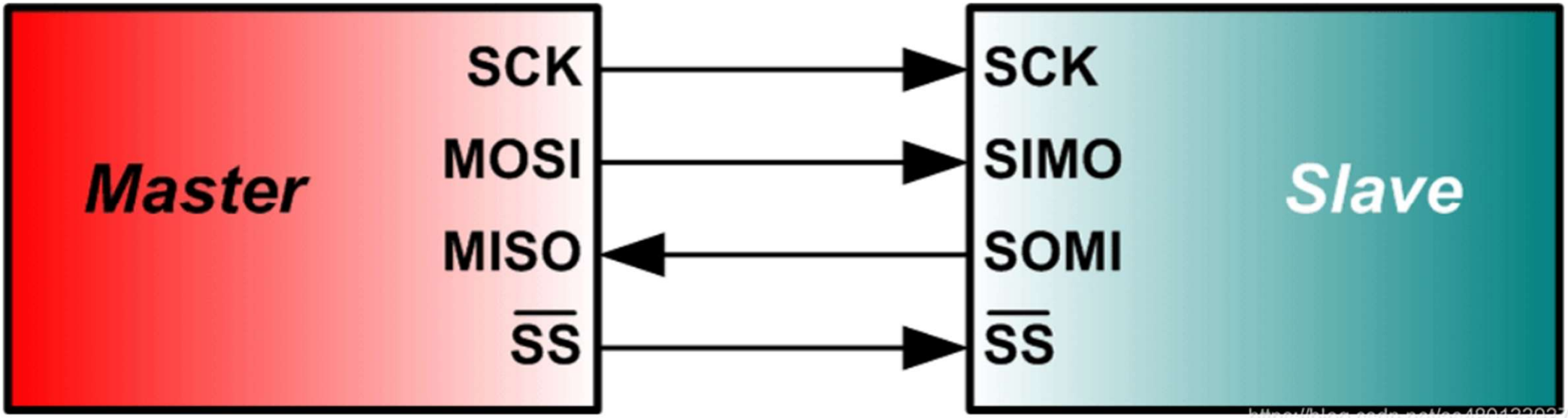
- VCS User Guide
- VCS命令详解(一):编译命令
  https://blog.csdn.net/burningCky/article/details/111558398
- VCS命令详解(二):仿真命令
  https://blog.csdn.net/burningCky/article/details/111743823
- VCS (1)~(7)
  https://blog.csdn.net/Tranquil_ovo/article/details/131797045
- VCS (一)~(四)
  https://zhuanlan.zhihu.com/p/127335447

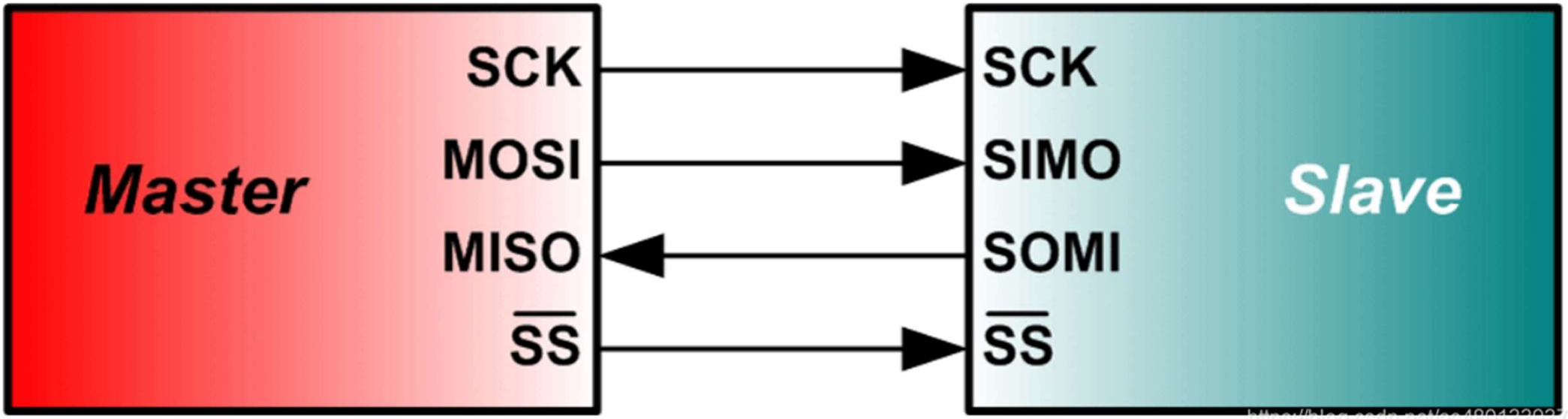
SPI Signals



SPI : Serial Peripheral Interface 串行外圍設備接口

- Clock
- MOSI
  - Master Output Slave Input
- MISO
  - Master Input Slave Output
- SS / CS
  - Slave Select / Chip Select

SPI Features



- Synchronous
  - All signals synchronous with clock whose frequency is determined by master
- Full duplex 全雙工
  - Can transmit data in both directions at the same time
  - Signals / Wires are with fixed direction
    - MOSI : Master → Slave
    - MISO : Slave → Master
- SS / CS : Slave Select / Chip Select
  - 1 master and multiple slaves
  - Master initiates operation

SPI Advantages and Disadvantages

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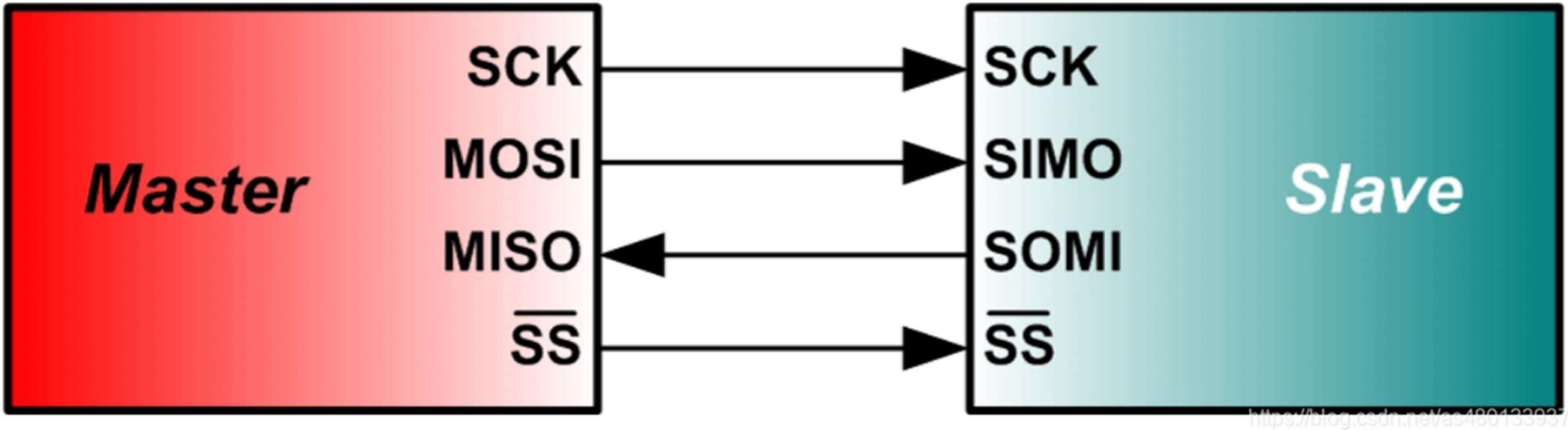


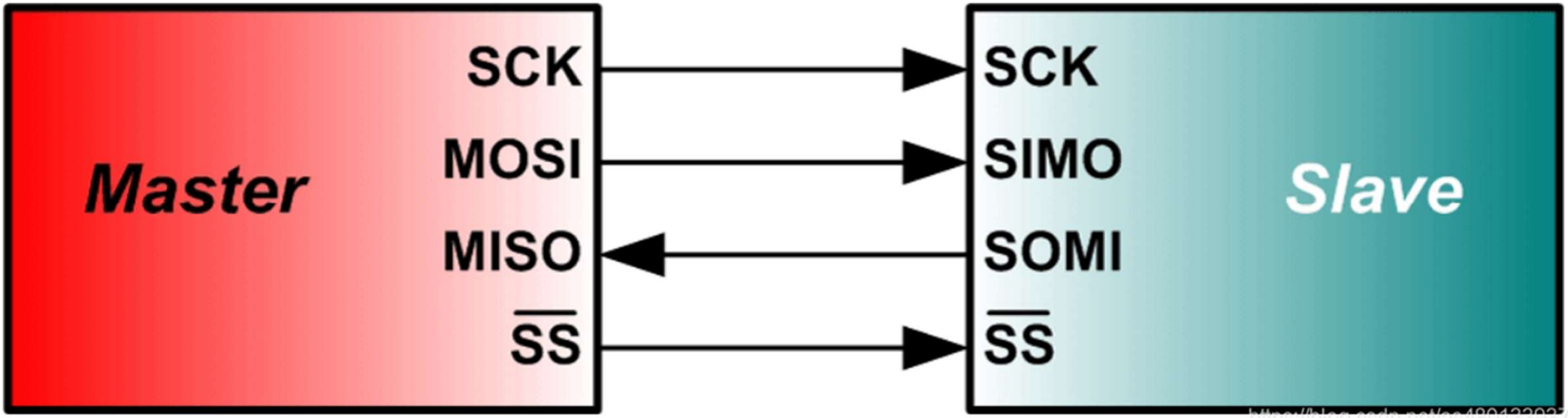
Advantages:

- Simple architecture and protocol
- Small number of wires (Minimum 4)
- Flexible length of data transmission
- No address needed

Disadvantages:

- No response from slave
- Possible waste of bandwidth in one direction

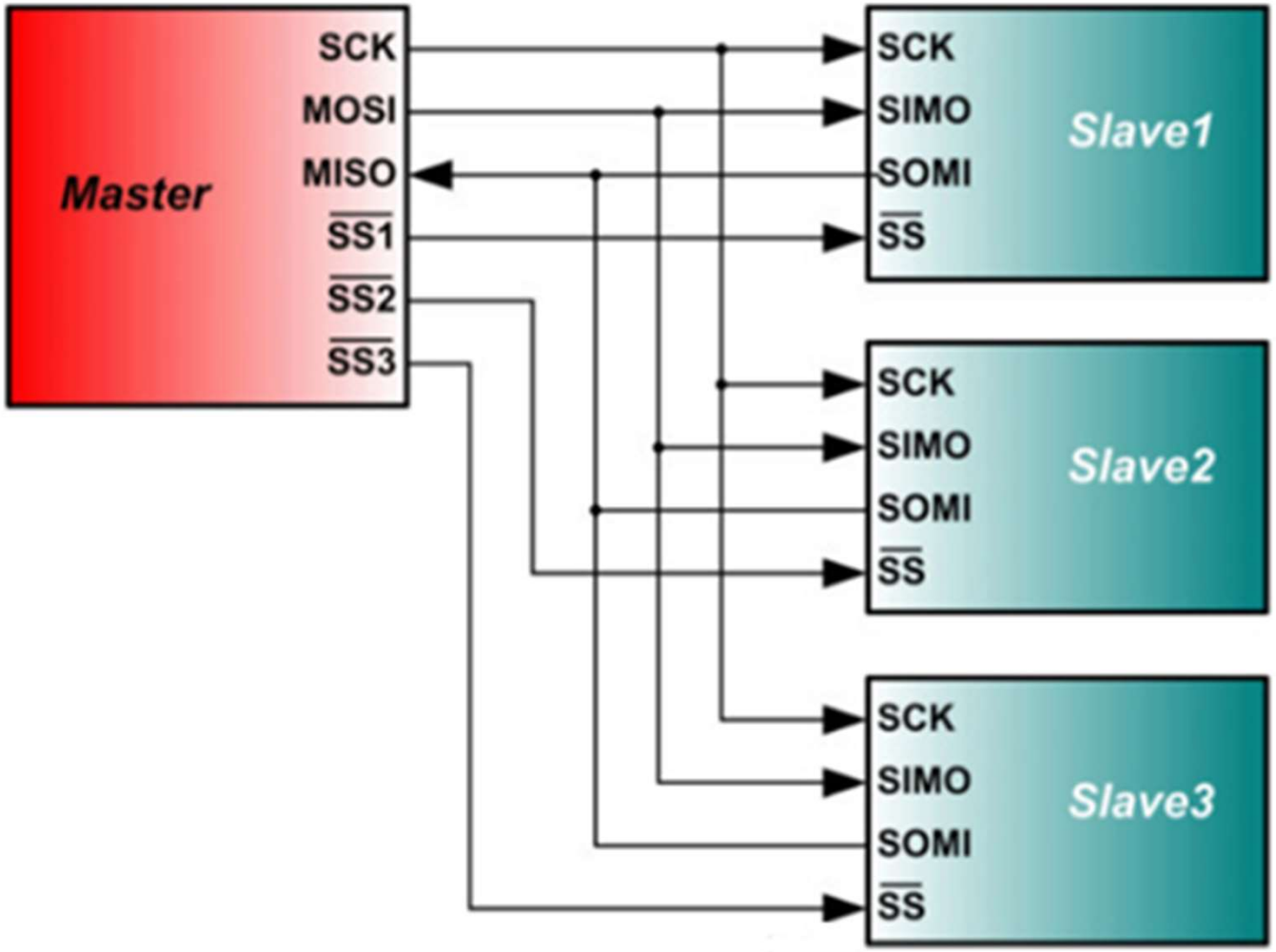
SPI Applications



Application

- Peripheral device with medium data throughput
- Flash, EEPROM, etc.
- Inter-chip
  - APB inner-chip

Architecture with Multiple Slaves 1: MUX



- Master select one slave from multiple slaves at a time
- Wire AND 線與 线与 (instead of MUX)

Archit. Multiple Slaves 2: Daisy Chain

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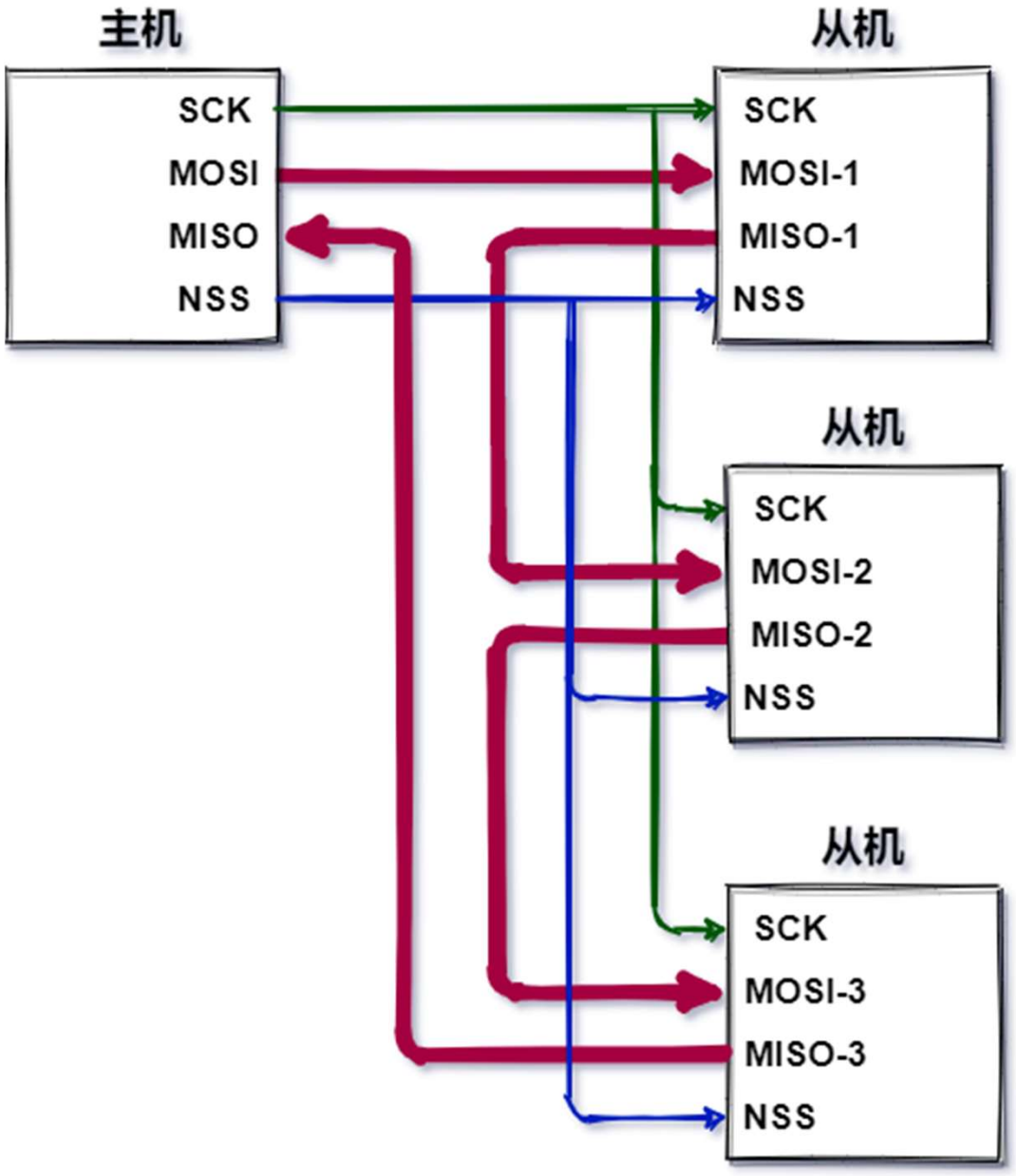
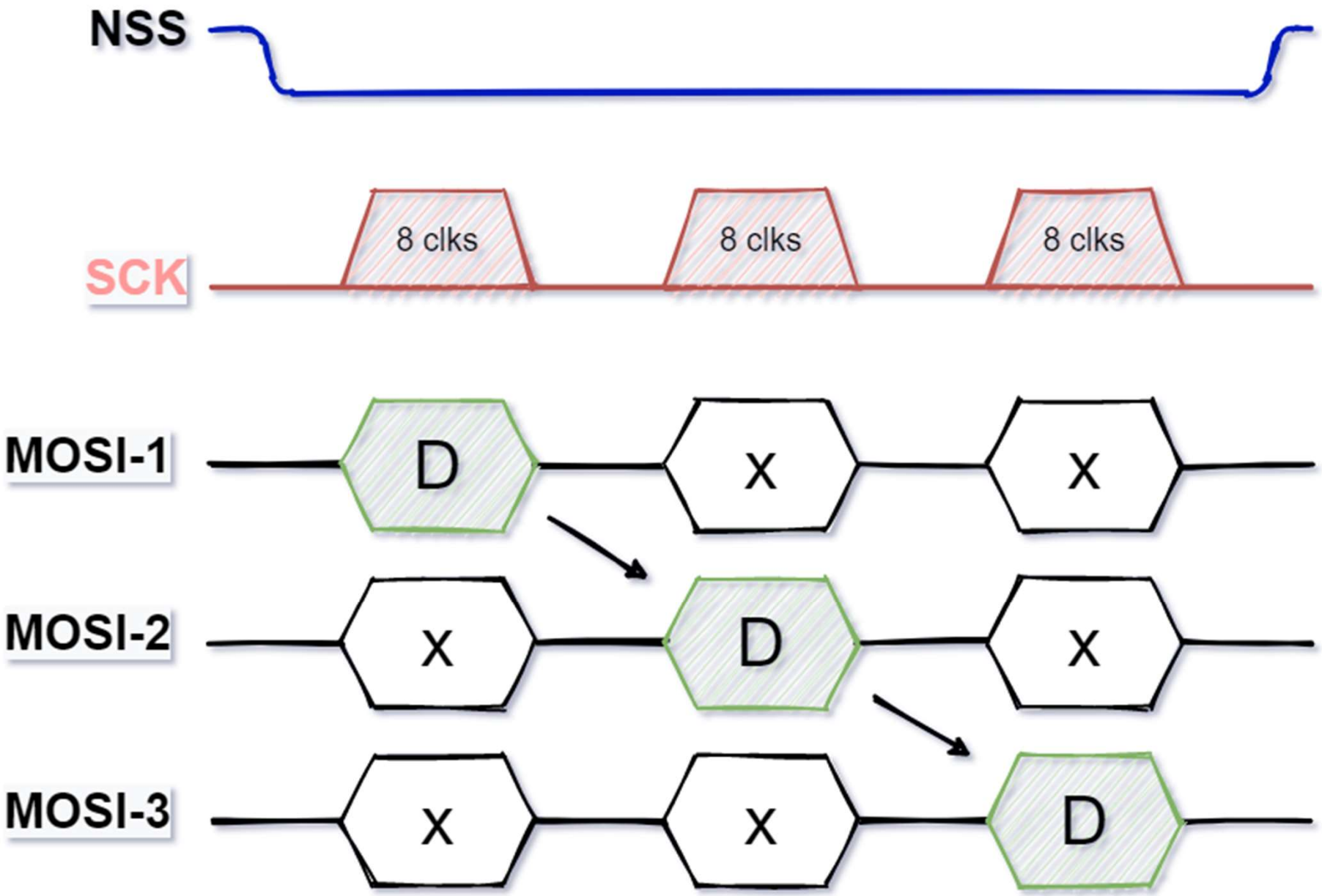


- Master and slave devices are connected in serial loop
- Data is transmitted from one device to its following device
- Advantage:
  - Long distance
  - Large number of devices
- Disadvantage:
  - Long delay
  - Disfunction in one device disable the whole system

Data Flow in Daisy Chain



D: Valid data; X: Invalid data

SPI Data Transmission: Overview

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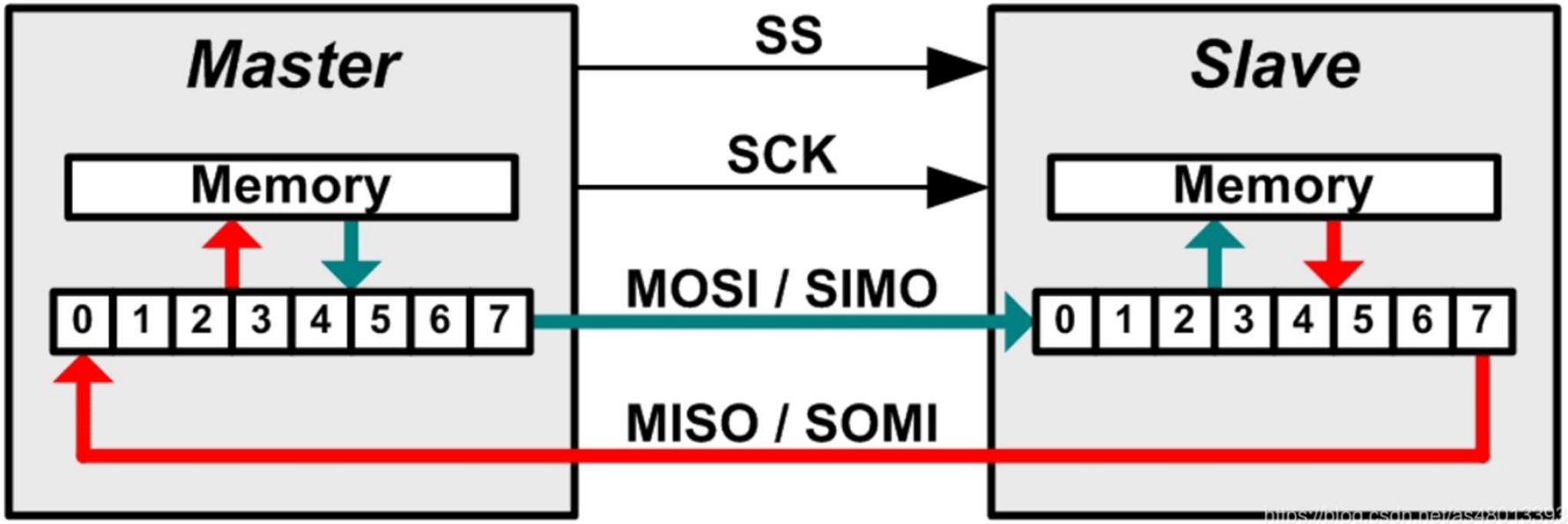

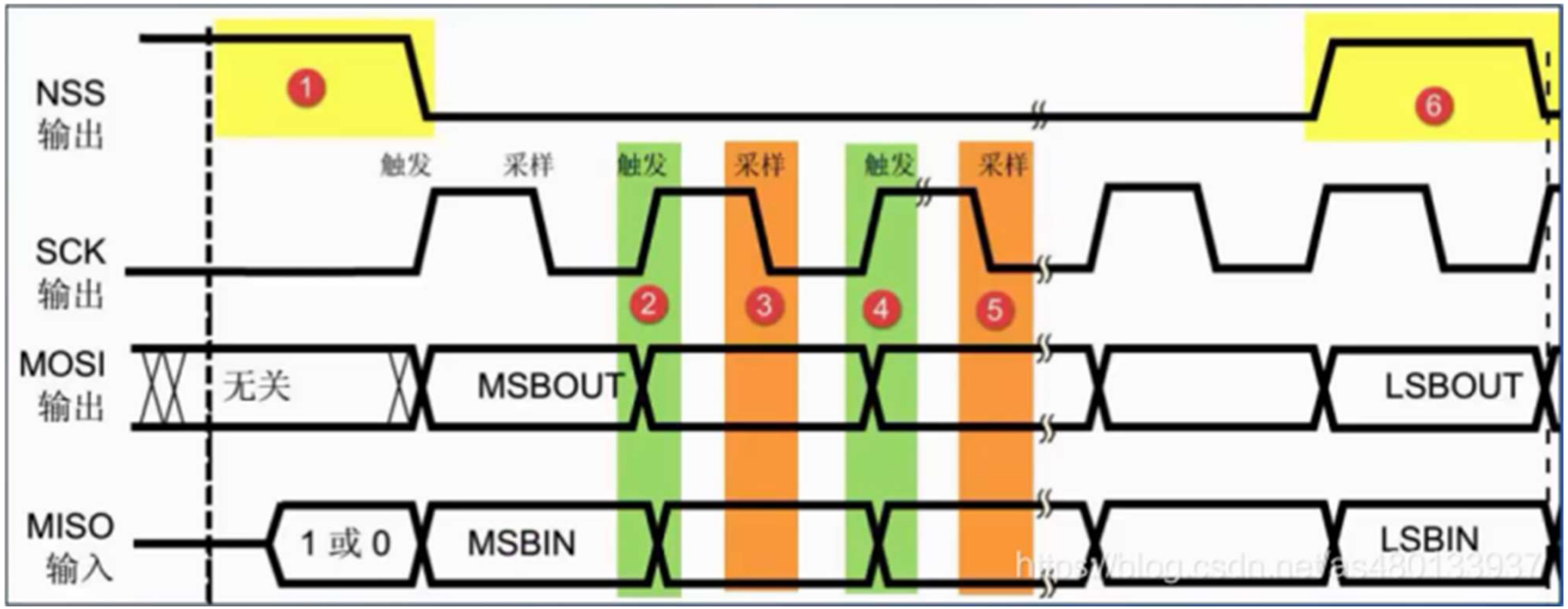

SPI Data Transmission

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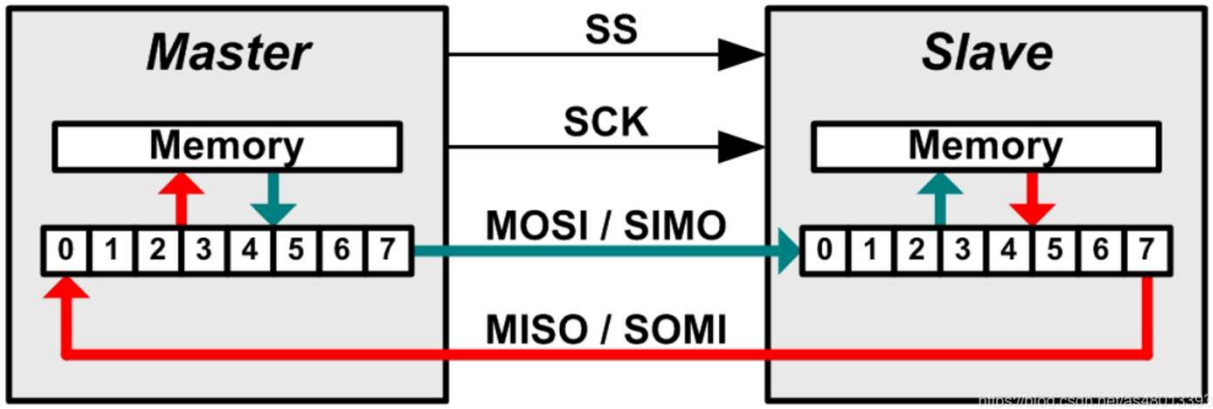
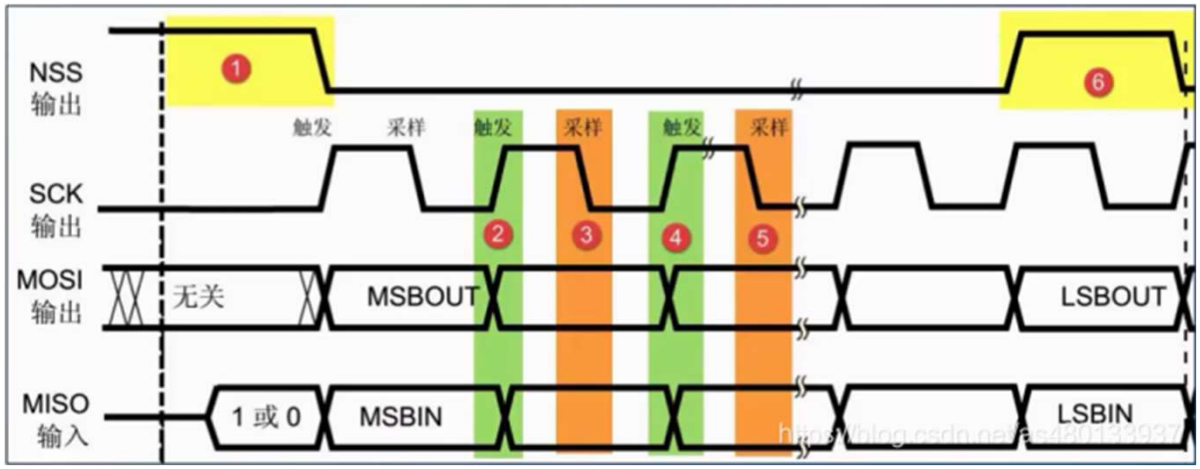
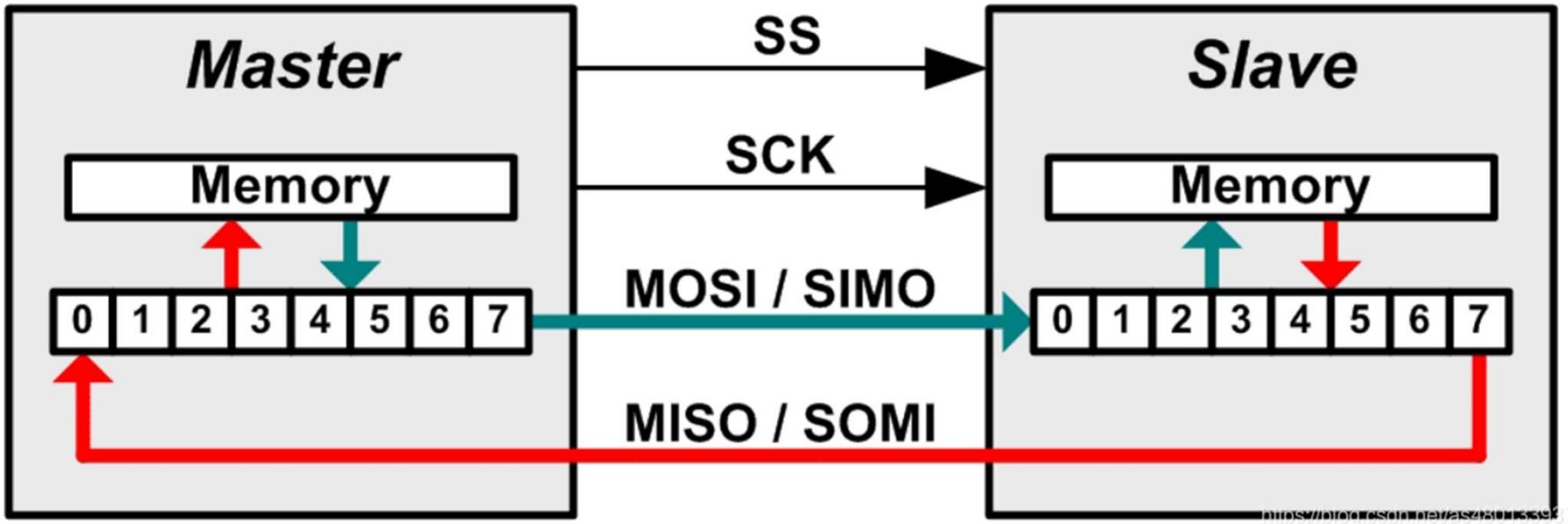




- Master assert the slave selection signal to inform the desired slave
- Master output clock signal which works as the synchronous reference for data output and input
- MOSI : Master outputs its data via MOSI while slave input the data
- MISO : Slave outputs its data via MISO while master input the data, at the same time as that of MOSI

SPI Hardware: Output and Input



- Output port (MO, SO)
  - Output the data bit one by one (serial)
  - Shift registers
- Input port (MI, SI)
  - Input the data bit one by one (serial)
  - Shift registers
  - Can share the same set of shift registers with output

Result: The shift registers in master and slave swap the data.

SPI Hardware: Data Memory and Flow

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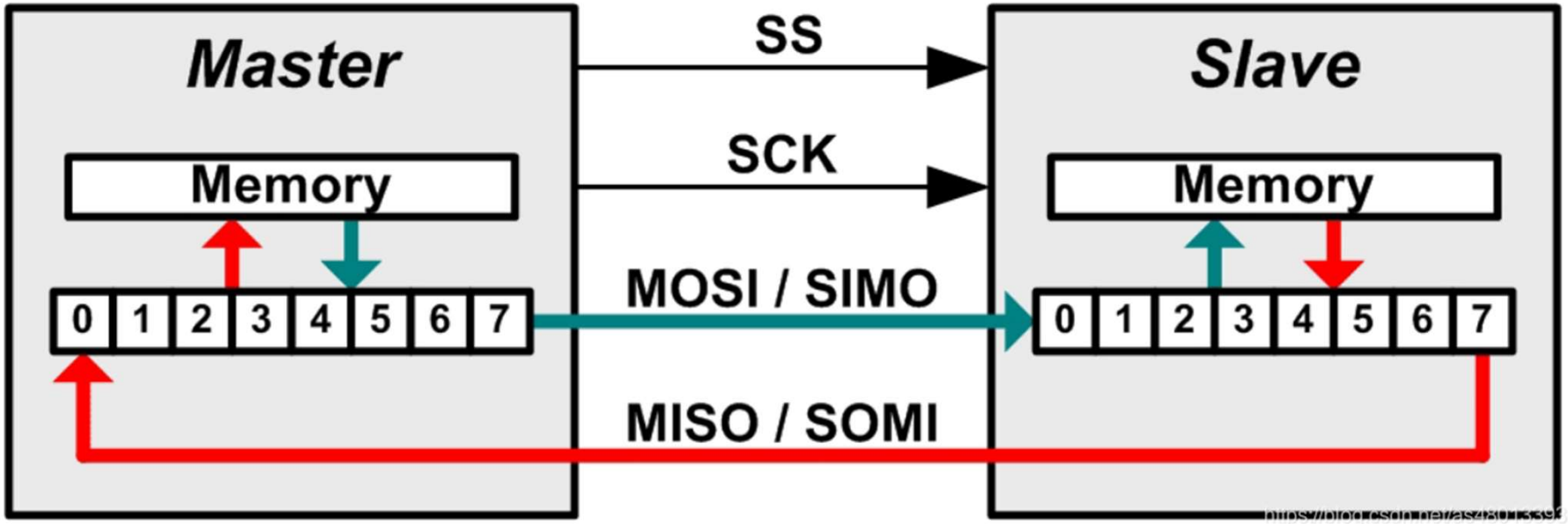
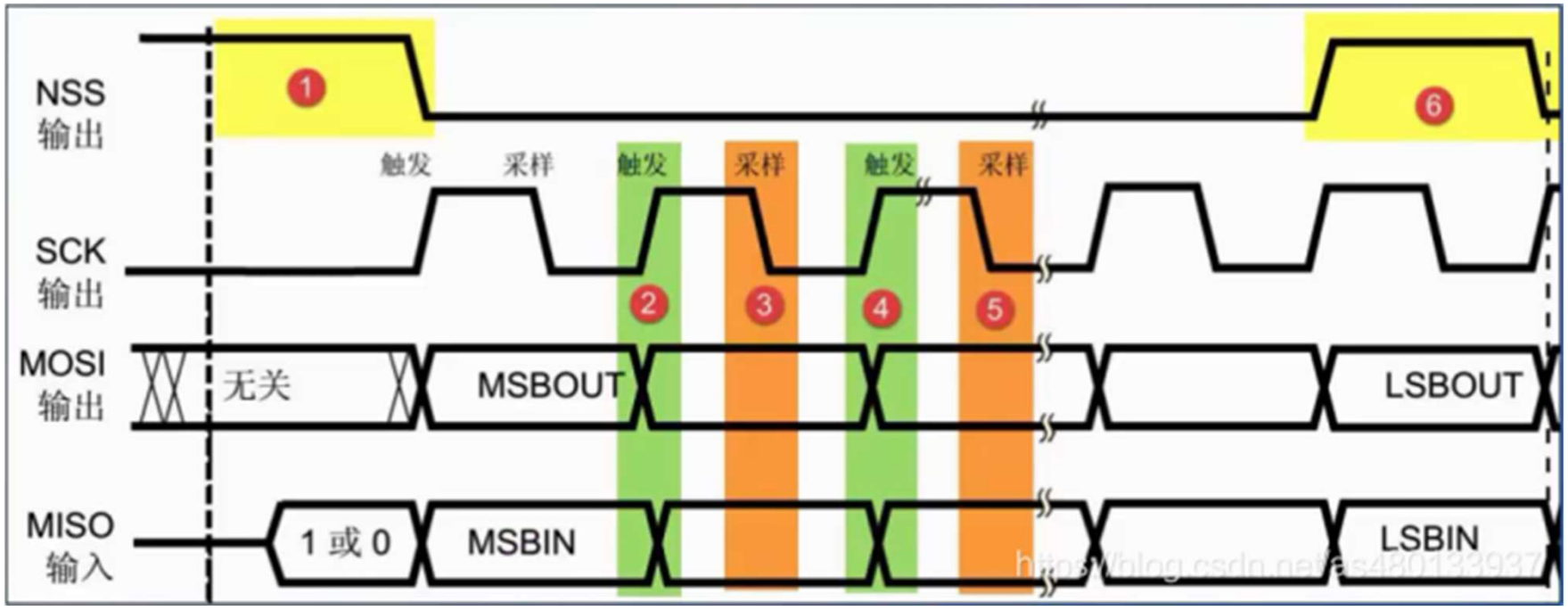


- Output circuit
  - Fetch data from memory and write into shift registers
  - Fetch data from shift registers and drive onto the output port
- Input circuit
  - Receive data from input port and write received data into shift registers
  - Store the data in shift registers into memory

SPI Timing



- When to start data transmission?
- When to end data transmission?

- When to output / drive data?
- When to input / receive data?

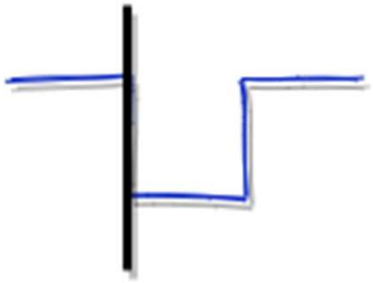
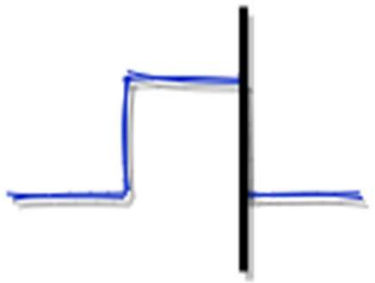
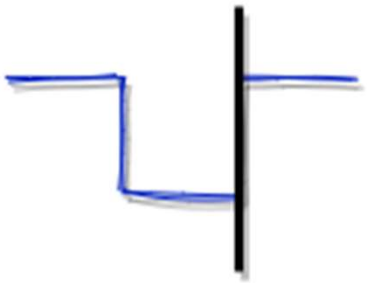
Clock Polarity

- CPOL = 0
  - Idle : clock = 0
  - Valid : clock = 1
- CPOL = 1
  - Idle : clock = 1
  - Valid : clock = 0

Clock Phase (Edge)

- CPHA = 0
  - Sampling the input data at the first switching edge of clock
- CPHA = 1
  - Sampling the input data at the second switching edge of clock

SPI Mode

Phase 相位 \ Polarity 极性	0	1
0		
1		

- Blue line:
  - clock
- Black line:
  - sampling time

SPI in Infineon TLE92466ED

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SPI in TLE92466ED: General Info.

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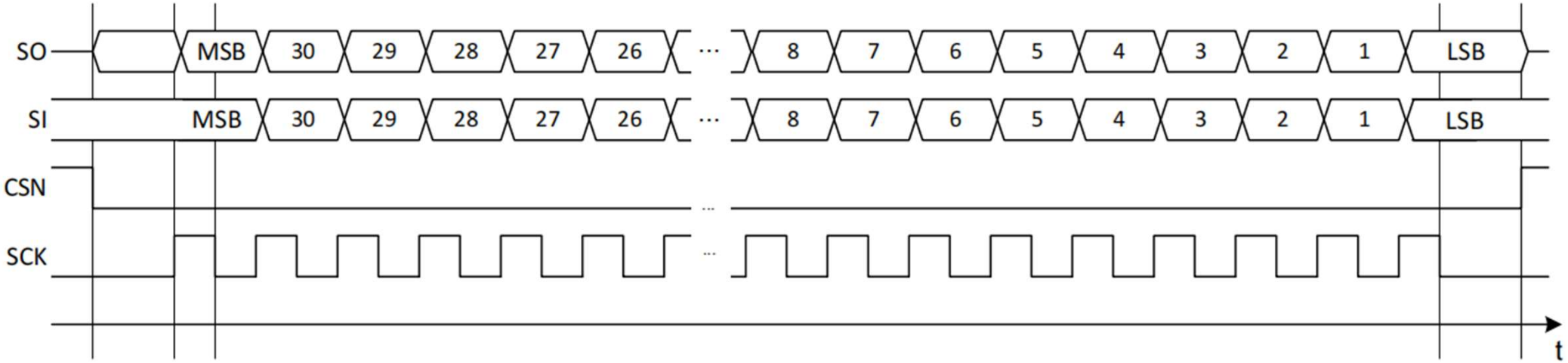
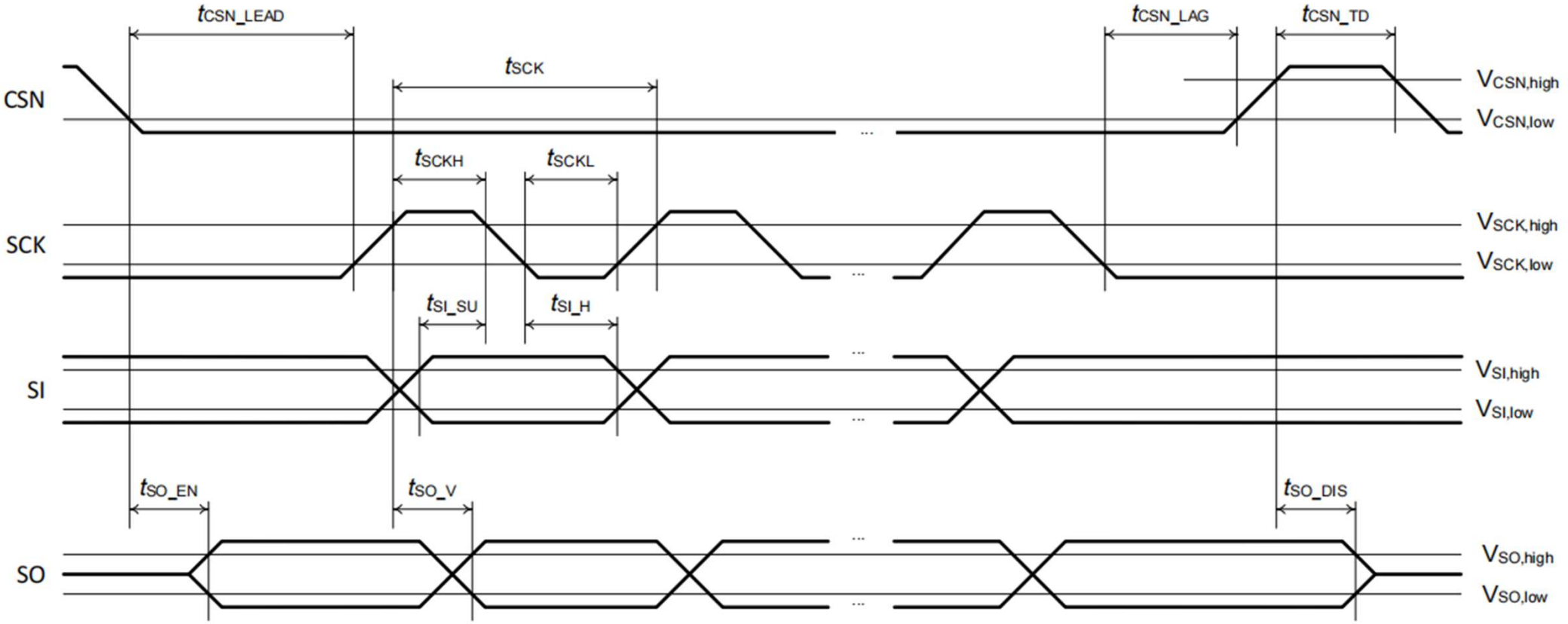
- The communication interface is based on a standard serial peripheral interface (SPI). The SPI is a full duplex synchronous serial slave interface.
- Four signal lines: SO, SI, SCK, and CSN.
- Data is transferred by the lines SI and SO at the data rate given by SCK.
- The falling edge of CSN indicates the beginning of a data access.
- Each access must be terminated by a rising edge of CSN.
- Data is sampled in on line SI at the falling edge of SCK and shifted out on line SO at the rising edge of SCK.
- A counter ensures that data is taken only when 32 bits have been transferred. If the number of bits transferred is not 32, the data frame is ignored.

SPI in TLE92466ED: Data Transmission



- The falling edge of CSN indicates the beginning of a data access.
- Each access must be terminated by a rising edge of CSN.
- Data is sampled in on line SI at the falling edge of SCK and shifted out on line SO at the rising edge of SCK.

SPI Timing Diagram



Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Serial clock high time	t_{SCKH}	50	–	–	ns	
Serial clock low time	t_{SCKL}	50	–	–	ns	
Enable lead time	t_{CSN_LEAD}	250	–	–	ns	falling CSN to rising SCK

CRC in TLE92466ED

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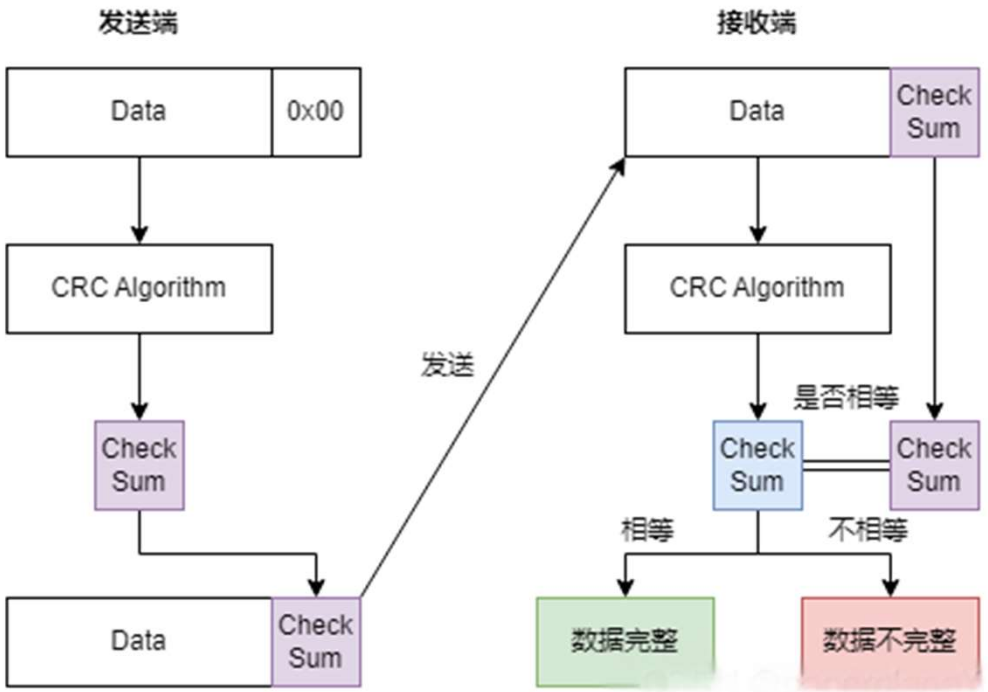
- An 8-bits cyclic redundancy code (CRC-8 SAE-J1850) is added to all SPI communication frames to detect corrupt data and to avoid wrong configuration of the IC. The CRC-8 SAE-J1850 polynomial is used for the calculation:

$$x^8 + x^4 + x^3 + x^2 + 1 \text{ or } 0x1D$$

- The initial value of the CRC-byte is 0xFF. The CRC result is XOR operated with 0xFF. The CRC-byte is located in the most significant byte of the SPI frame. The byte-sequence for the CRC calculation is as follows:

1st byte: SPI frame[7:0]
2nd byte: SPI frame[15:8]
3rd byte: SPI frame[23:16]

CRC



- CRC: A type of ECC (Error Check and Correct)
- By adding extra bits to the original data, ECC can detect a certain number of error bits and correct a certain number of error bits damaged in the transmission
- One extra parity bit
  - Can detect 1 error bit (cannot guarantee detect more than 1 error bits)
  - Can correct 0 error bit (cannot identify the location of error bit)

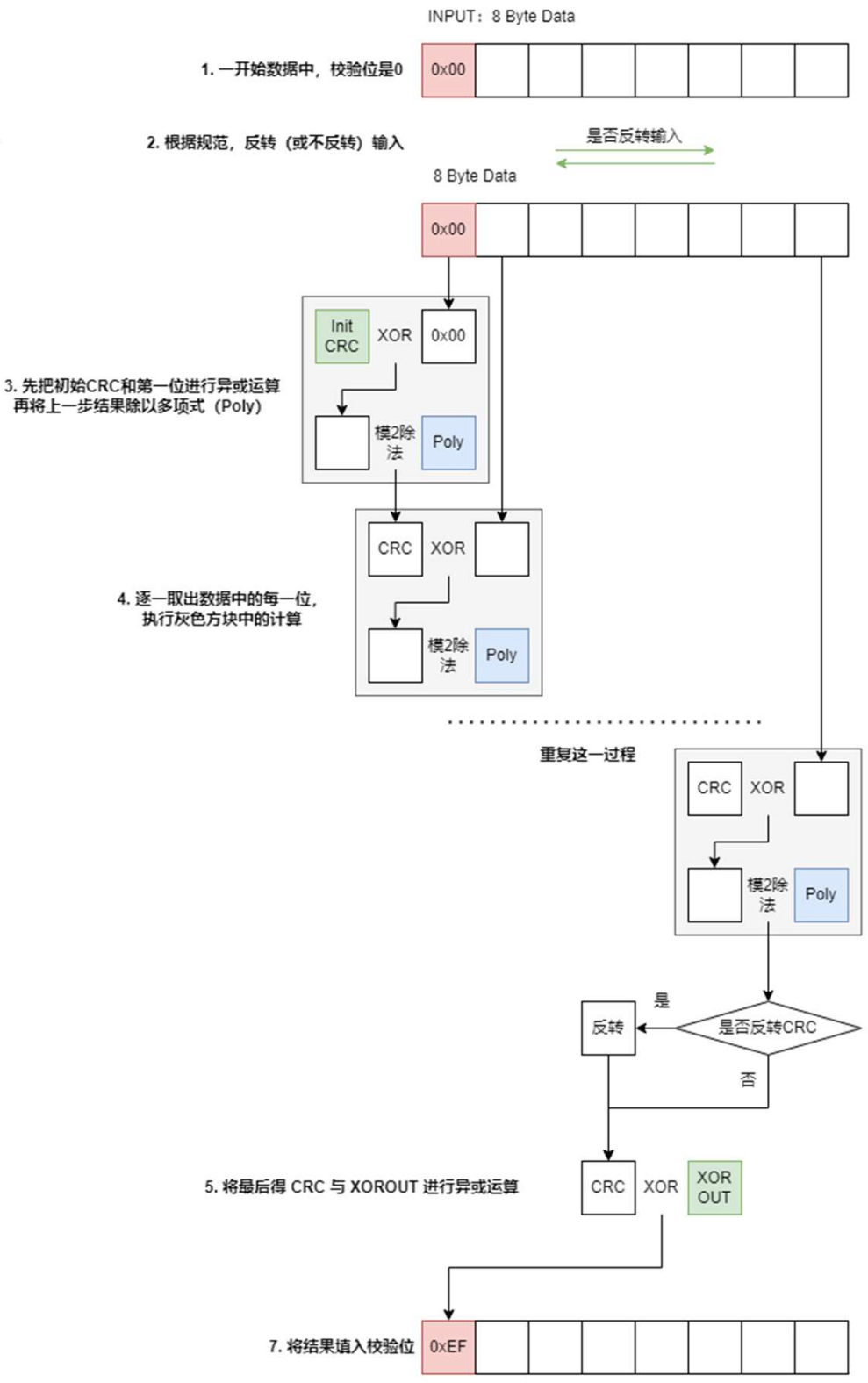
CRC-8 Generation

CRC algorithm

- CRC: The remainer of input data divided by polynomial
- Modulo 2 division

Parameters

- Initial CRC value
- Final XOR data
- Polynomial
- Input inversion or not
- Output inversion or not



Modulo 2 Calculation (+ - x /)

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Key

- XOR (same inputs → output 0) 異或（相同輸入產生0）
- No carry no borrow 沒有進位借位

Modulo 2 Add / Subtract

- 0＋0＝0　0＋1＝1　1＋0＝1　1＋1＝0
- 0－0＝0　0－1＝1　1－0＝1　1－1＝0

```
1      0 1 0 1
2  +   0 0 1 1
3  ---------
4      0 1 1 0
```

Modulo 2 Multiplication

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Modulo 2 multiplication

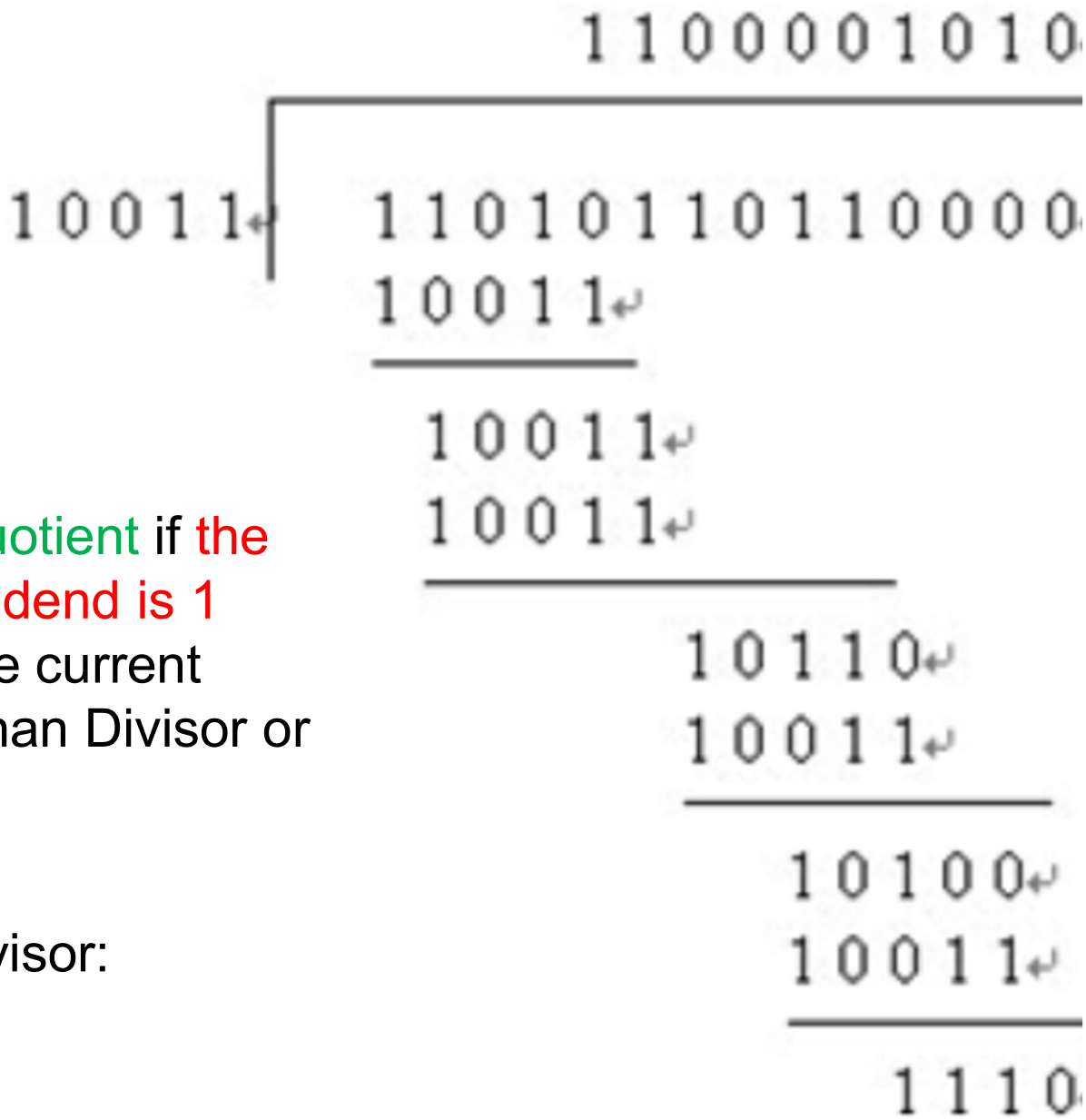
- Multiply: $0\times0=0$ $0\times1=0$ $1\times0=0$ $1\times1=1$
  - Same as general multiplication
- Accumulation: Modulo 2 add

```
1          1 0 1 1
2  ×         1 0 1
3  ---------------------
4          1 0 1 1
5        0 0 0 0
6  +   1 0 1 1
7  ---------------------
8      1 0 0 1 1 1
```

Modulo 2 Division

E / S = Q … R

- Get one bit of 1 in Quotient if the first bit of current Dividend is 1 no matter whether the current Dividend is smaller than Divisor or not
- Current dividend - divisor: Modulo 2 add



Modulo 2 Division: Example

E / S = Q … R

1111000 / 1101 = 1011 … 111

```
1     1 0 1 1     //商
2  --------------
3  1 1 1 1 0 0 0  //被除数,注意首位为1
4  1 1 0 1        //被除数首位为1,除以除数
5  ---------------
6    0 1 0 0 0 0  //余数去除首位,作为新的被除数
7    0 0 0 0      //被除数首位为0,除以0
8  ---------------
9      1 0 0 0 0  //余数去除首位,作为新的被除数
10     1 1 0 1    //被除数首位为1,除以除数
11 ---------------
12       1 0 1 0  //余数去除首位,作为新的被除数
13       1 1 0 1  //被除数首位为1,除以除数
14 ---------------
15         1 1 1  //余数,此时余数位数少于除数,不能继续除了
```

CRC Materials

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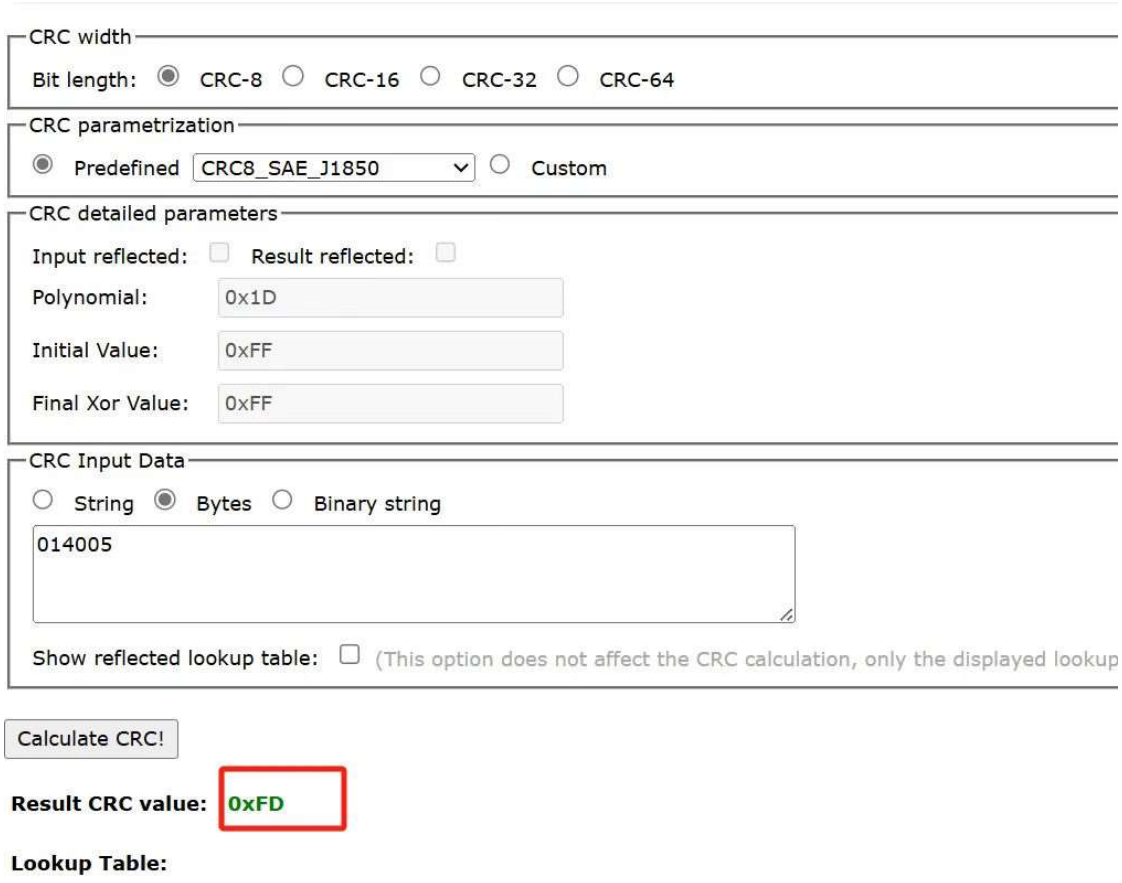
- https://blog.csdn.net/paperplaneY/article/details/131285130
- https://blog.csdn.net/m0_51487301/article/details/124270017
- https://blog.csdn.net/qq_33411687/article/details/82593466
- https://www.sunshine2k.de/coding/javascript/crc/crc_js.html



Data Flow (Command Protocol)

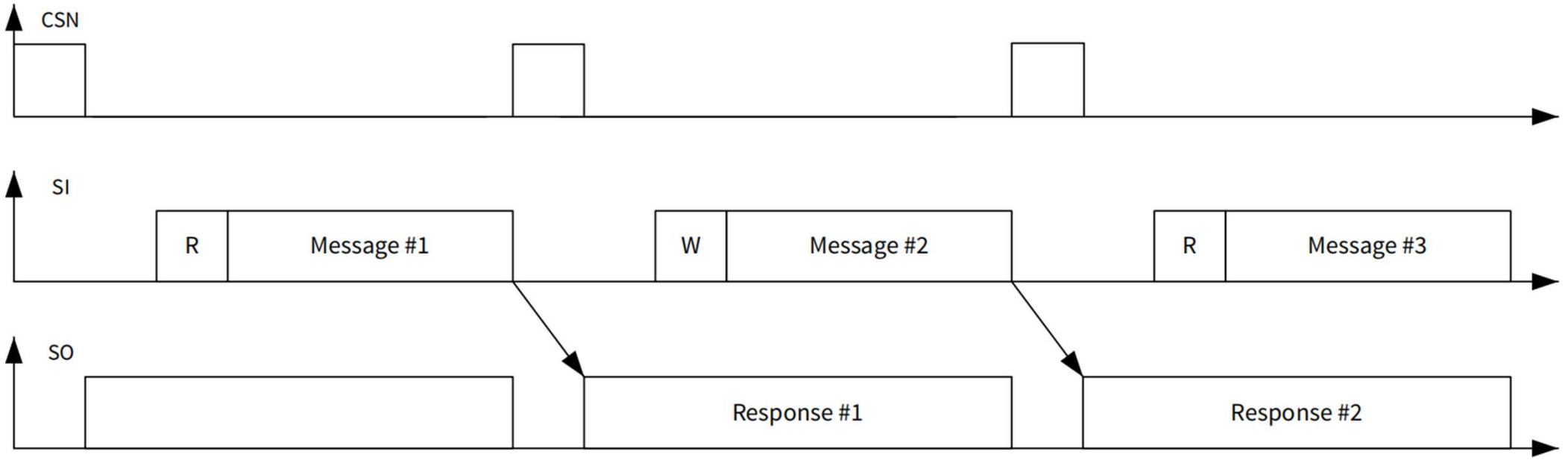
- The message from the microcontroller must be sent MSB first.
- The data from the SO pin is sent MSB first.

- For each command received at the SI pin of the SPI interface, a serial data stream is returned at the same time on the SO pin.

- The content of the SO data frame is dependent on the command which was received on the SI pin during the previous frame.

Data Flow (Command Protocol)

- A READ command (R/W = 0) returns the contents of the addressed register one SPI frame later. The data bits in the READ command are ignored.
- A WRITE command (R/W = 1) will write the data bits in the SPI word to the addressed register. The actual contents of addressed register will be returned to the SPI master (microcontroller) during the next SPI frame.



Project_1

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Design master and slave circuits of SPI interface according to the specification of Infineon TLE92466ED

- Data transmission as SPI protocol of Infineon TLE92466ED
- CRC-8 SAE-J1850
- [Optional] Implement command protocol