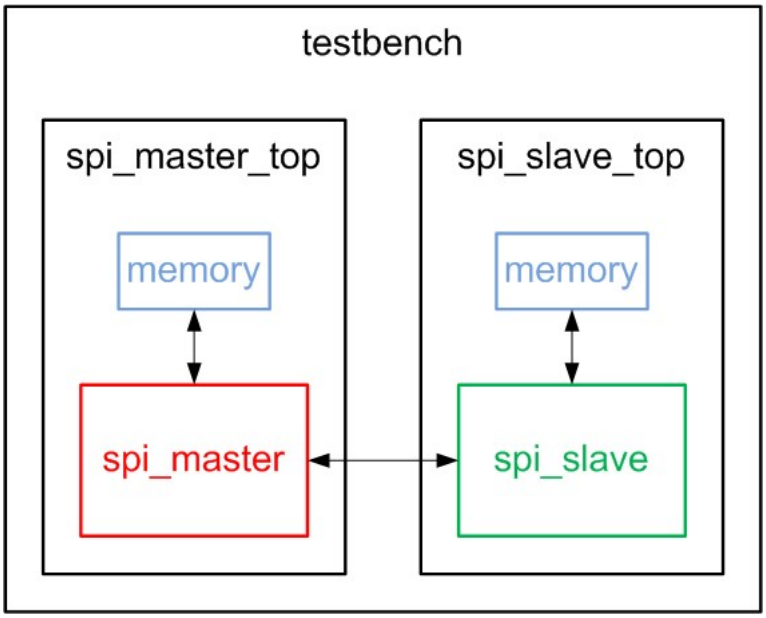
ELEG5765 Fundamental of Automotive IC

Spring Semester, 2025

Project 1

Due date: Feb. 28, 2025

Design master and slave circuits of SPI interface according to the specification of Infineon TLE92466ED.



1. Compose your design in three files. Pay attention to synthesizable design.
   a) spi_master_top.v for SPI master where the top module is spi_master_top;
   b) spi_slave_top.v for SPI slave where the top module is spi_slave_top;
   c) testbench.v for testing where the top module is testbench.
2. There may be multiple modules in each file.
3. These three files are located in the same directory, e.g. rtl.

4. Module spi_master_top is with the following interface:

Signal	I/O	Description
clk	I	Clock
rstn	I	Reset 0: Valid
sck	O	Clock to slave
csn	O	Chip select 0: Valid
mo	O	Data output
mi	I	Data input

5. Module spi_slave_top is with the following interface:

Signal	I/O	Description
clk	I	Clock
rstn	I	Reset 0: Valid
sck	I	Clock from master
csn	I	Chip select 0: Valid
so	O	Data output
si	I	Data input

6. Design requirement:
   a) Data transmission via SPI interface following SPI protocol of Infineon TLE92466ED;
   b) CRC-8 SAE-J1850 following SPI protocol of Infineon TLE92466ED;
   c) [Optional] Add memory to read/write data so that
      (1) output circuit read data from memory, generate CRC and drive onto output port;
      (2) input circuit receive data from input port, check CRC and write the correct payload data into memory.

   You may instance the following SRAM as memory:
   https://www.chipverify.com/verilog/verilog-single-port-ram
   You may instance the memory:

(1) data width 24 bits.

(2) depth 32.

d) [Optional] Implement command protocol following SPI protocol of Infineon TLE92466ED.

7. Submit
   a) Source codes of your three design files;
   b) Report showing
      1) your complement items;
      2) simulation waveforms;
      3) brief description of your designed circuit.