CUHK 香港中文大學 | Electronic Engineering 電子工程學系

ELEG 5765 Fundamentals of Automotive Integrated Circuits

Lecture 3

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Lecture 3: Solenoid Driver IC

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Outline

- Solenoid Driver IC
- IC Specification (PCB designer, Software designer, IC designer)
- Index Requirement

Classification of Automotive IC

From the point view of digital IC designer

- IC for Driving Automation / Assistance
  - similar to AI IC
  - high computing capability
  - dominantly digital
- IC for Smart Cockpit
  - similar to mobile phone CPU
  - powerful computing capability
  - dominantly digital + RF

Classification of Automotive IC

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- MCU
  - moderate to light computing capability
  - dominantly digital
- Dedicated Digital ASIC
  - for specific function
  - moderate to light computing capability
  - digital (majority) + analog (minority)
- Mixed Digital + Analog
  - mixed at circuit / module level
- Analog IC
  - e.g., sensor, ACDC, etc.
  - dominantly analog

Example of Automotive IC

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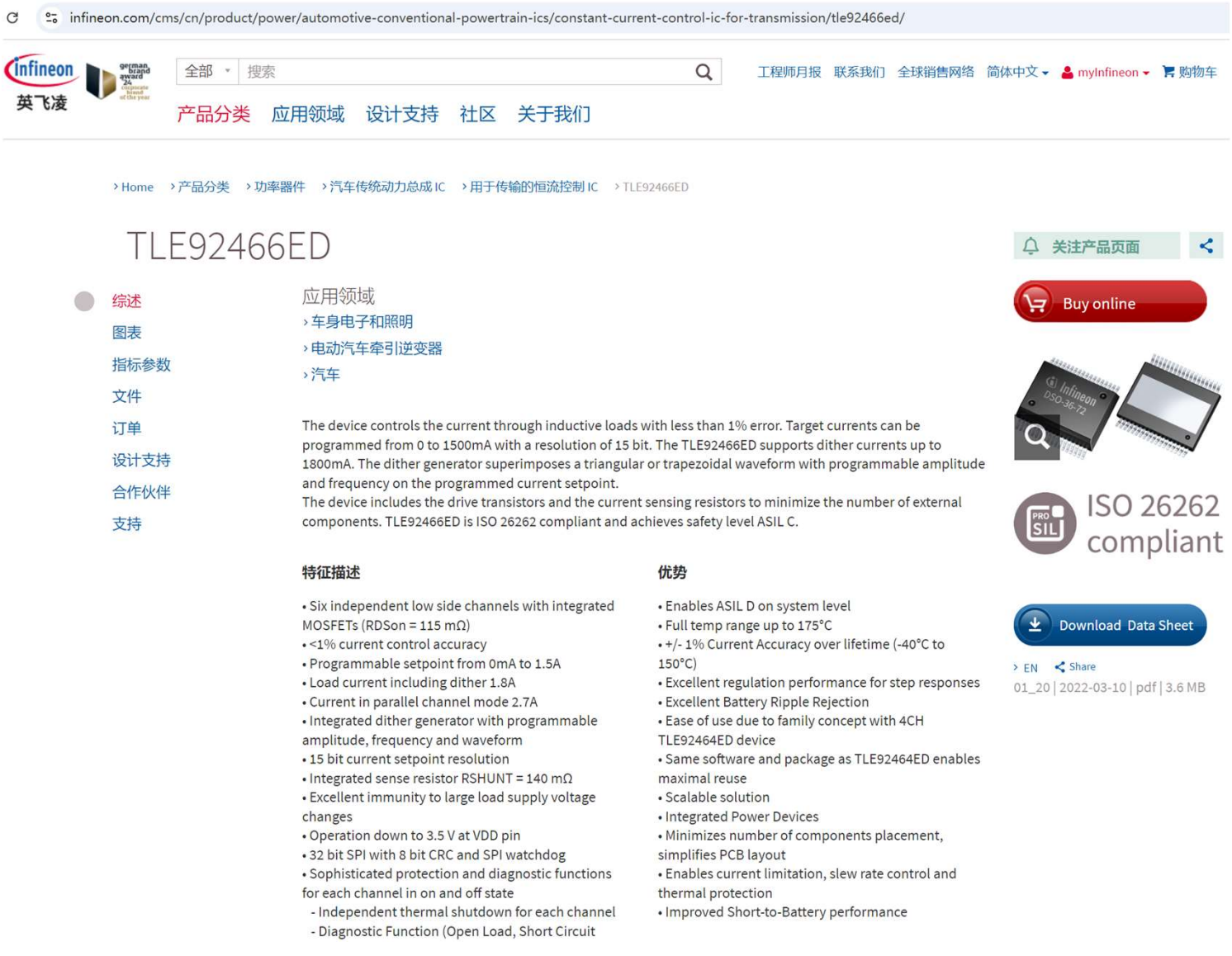
- Infineon TLE92466ED Six Channel Low-side solenoid driver IC
- https://www.infineon.com/cms/cn/product/power/automotive-conventional-powertrain-ics/constant-current-control-ic-for-transmission/tle92466ed/



infineon.com/cms/cn/product/power/automotive-conventional-powertrain-ics/constant-current-control-ic-for-transmission/tle92466ed/

Infineon 英飞凌

全部 搜索

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TLE92466ED

综述
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The device controls the current through inductive loads with less than 1% error. Target currents can be programmed from 0 to 1500mA with a resolution of 15 bit. The TLE92466ED supports dither currents up to 1800mA. The dither generator superimposes a triangular or trapezoidal waveform with programmable amplitude and frequency on the programmed current setpoint.
The device includes the drive transistors and the current sensing resistors to minimize the number of external components. TLE92466ED is ISO 26262 compliant and achieves safety level ASIL C.

ISO 26262 compliant

特征描述

- Six independent low side channels with integrated MOSFETs (RDSon = 115 mΩ)
- <1% current control accuracy
- Programmable setpoint from 0mA to 1.5A
- Load current including dither 1.8A
- Current in parallel channel mode 2.7A
- Integrated dither generator with programmable amplitude, frequency and waveform
- 15 bit current setpoint resolution
- Integrated sense resistor RSHUNT = 140 mΩ
- Excellent immunity to large load supply voltage changes
- Operation down to 3.5 V at VDD pin
- 32 bit SPI with 8 bit CRC and SPI watchdog
- Sophisticated protection and diagnostic functions for each channel in on and off state
  - Independent thermal shutdown for each channel
  - Diagnostic Function (Open Load, Short Circuit

优势

- Enables ASIL D on system level
- Full temp range up to 175°C
- +/- 1% Current Accuracy over lifetime (-40°C to 150°C)
- Excellent regulation performance for step responses
- Excellent Battery Ripple Rejection
- Ease of use due to family concept with 4CH TLE92464ED device
- Same software and package as TLE92464ED enables maximal reuse
- Scalable solution
- Integrated Power Devices
- Minimizes number of components placement, simplifies PCB layout
- Enables current limitation, slew rate control and thermal protection
- Improved Short-to-Battery performance

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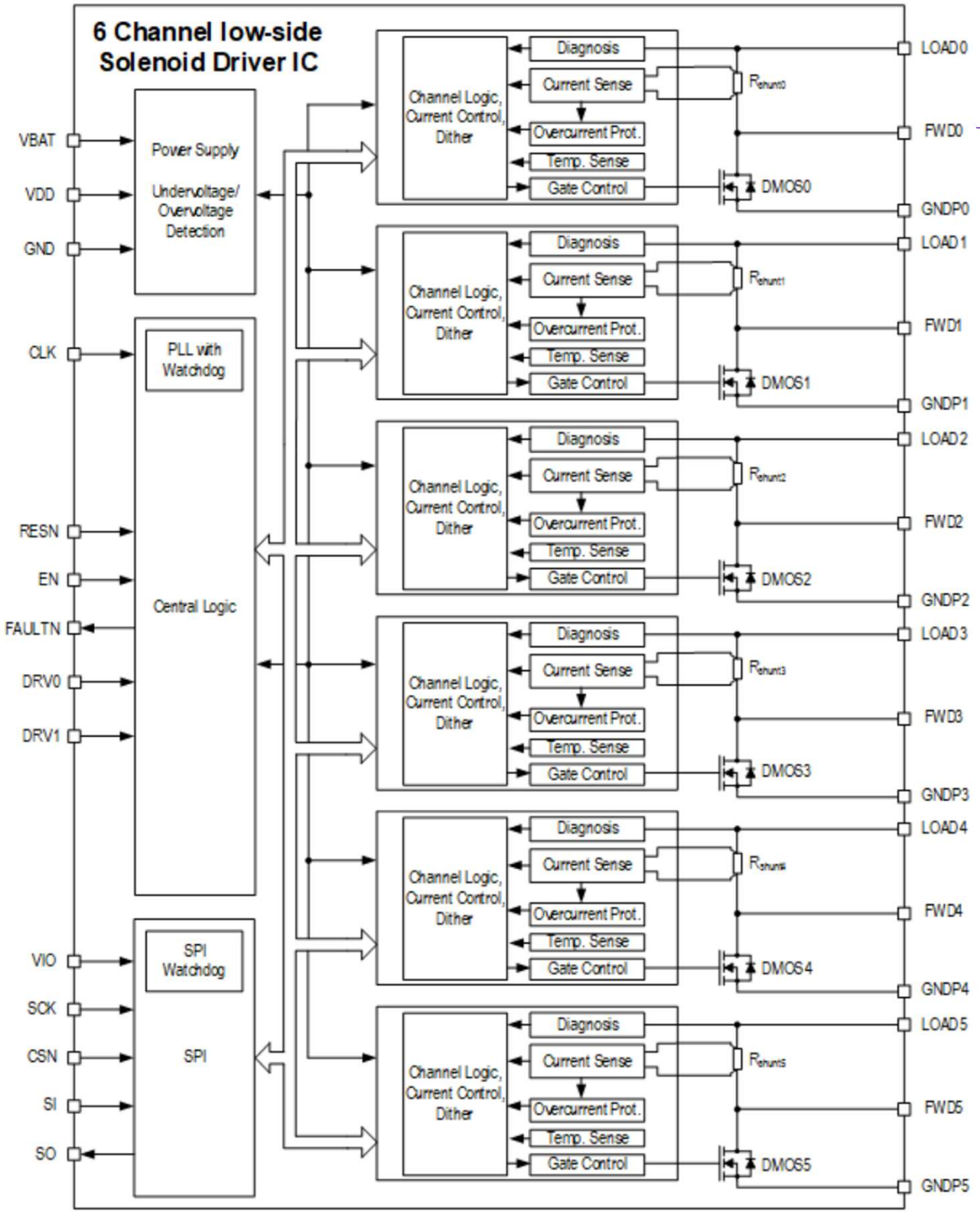
Block Diagram

- Six channels of driver
- Power supply
- Central logic
- SPI

Output current with desired strength by configuring via SPI interface.



Overview

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- The device controls the current through inductive loads with less than 1% error. Target currents can be programmed from 0 to 1500mA with a resolution of 15 bit.

- The TLE92466ED supports dither currents up to 1800mA. The dither generator superimposes a triangular or trapezoidal waveform with programmable amplitude and frequency on the programmed current setpoint.

- The device includes the drive transistors and the current sensing resistors to minimize the number of external components.

- TLE92466ED is ISO 26262 compliant and achieves safety level ASIL C.

Features

- Six independent low side channels with integrated MOSFETs (R_{DSon} = 115 mΩ)
- <1% current control accuracy
- Programmable setpoint from 0 mA to 1.5 A
- Load current including dither 1.8 A
- Current in parallel channel mode 2.7 A
- Integrated dither generator with programmable amplitude, frequency and waveform
- 15 bit current setpoint resolution
- Integrated sense resistor R_{SHUNT} = 140 mΩ
- Excellent immunity to large load supply voltage changes
- Operation down to 3.5 V at VDD pin
- 32 bit SPI with 8 bit CRC and SPI watchdog

Features

- Sophisticated protection and diagnostic functions for each channel in on and off state
  - Independent thermal shutdown for each channel
  - Diagnostic Function (Open Load, Short Circuit Ground, Overcurrent)
  - Voltage monitoring
  - Overtemperature protection
- Two independent current feedback paths with fast measurement option
- Integrated system clock with clock watchdog
- Temperature range -40°C to 175 °C
- Small power package PG-DSO-36-72
- Green Product (RoHS compliant)
- Pb-free (RoHS compliant) package
- AEC-Q100 Grade 0 qualified
- ISO 26262 Safety Element out of Context for safety requirements up to ASIL C

Advantage

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- Enables ASIL D on system level
- Full temp range up to 175°C
- +/- 1% Current Accuracy over lifetime (-40°C to 150°C)
- Excellent regulation performance for step responses
- Excellent Battery Ripple Rejection
- Ease of use due to family concept with 4CH TLE92464ED device
- Same software and package as TLE92464ED enables maximal reuse
- Scalable solution
- Integrated Power Devices
- Minimizes number of components placement, simplifies PCB layout
- Enables current limitation, slew rate control and thermal protection
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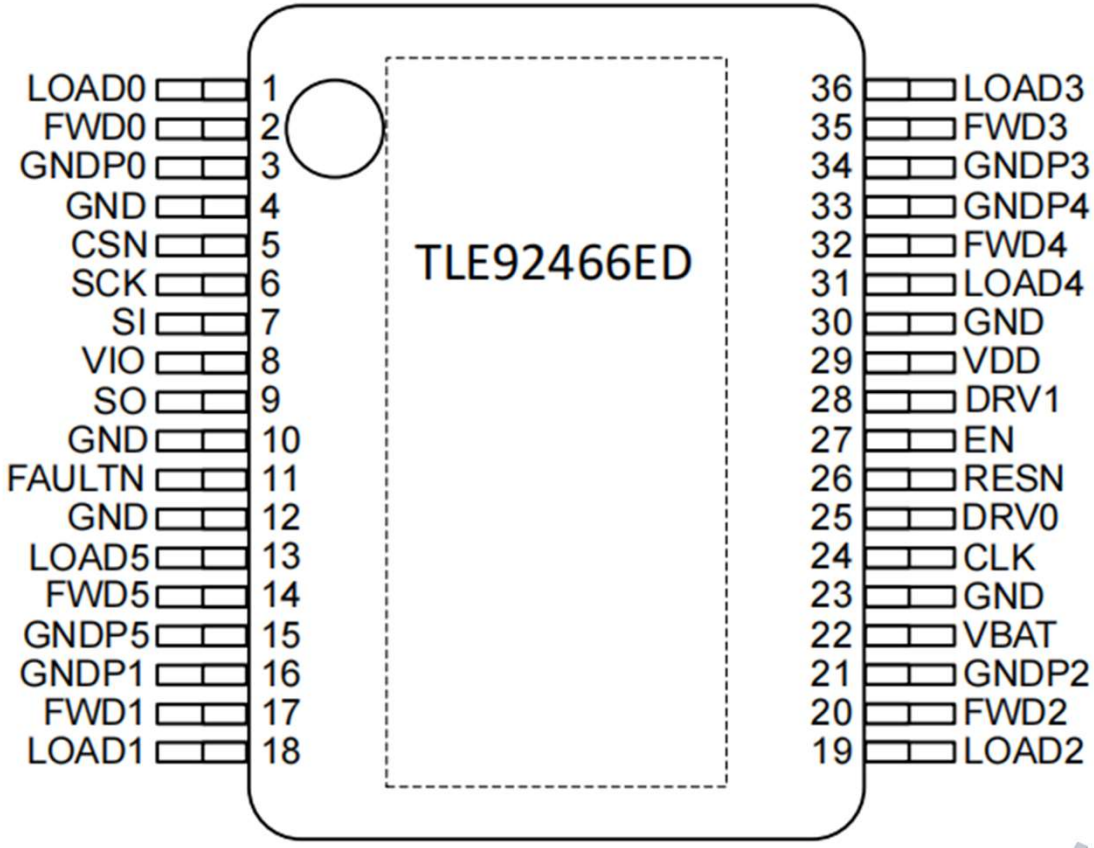
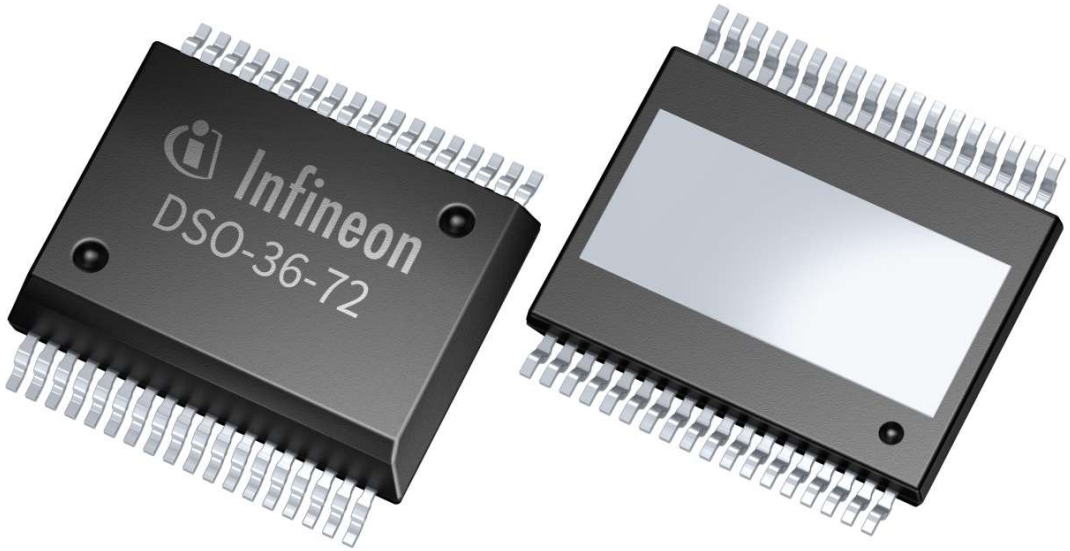
Pin


TLE92466ED
LOAD0 1
FWD0 2
GNDP0 3
GND 4
CSN 5
SCK 6
SI 7
VIO 8
SO 9
GND 10
FAULTN 11
GND 12
LOAD5 13
FWD5 14
GNDP5 15
GNDP1 16
FWD1 17
LOAD1 18
36 LOAD3
35 FWD3
34 GNDP3
33 GNDP4
32 FWD4
31 LOAD4
30 GND
29 VDD
28 DRV1
27 EN
26 RESN
25 DRV0
24 CLK
23 GND
22 VBAT
21 GNDP2
20 FWD2
19 LOAD2


Infineon
DSO-36-72

Pin

Table 1 Pin definition and functions

Pin	Symbol	Function
1	LOAD0	Output; for channel 0.
2	FWD0	Free wheeling diode; for channel 0.
3	GNDP0	Ground; for channel 0 power stage.
4	GND	Ground; connect to GND.
5	CSN	SPI chip select input; digital input: 3.3 V or 5.0 V logic levels.
6	SCK	SPI clock input; digital input: 3.3 V or 5.0 V logic levels.
7	SI	SPI input; digital input: 3.3 V or 5.0 V logic levels.
8	VIO	Supply SPI Slave Out (SO) pin; connected to 3.3 V or 5.0 V supply.
9	SO	SPI output; push pull output compatible to 3.3 V or 5.0 V logic levels.
10	GND	Ground; signal ground. Internally connected to cooling tab.
11	FAULTN	Status output; open drain output. In case not used, keep open.
12	GND	Ground; signal ground. Internally connected to cooling tab.
13	LOAD5	Output; for channel 5.
14	FWD5	Free wheeling diode; for channel 5.
15	GNDP5	Ground; ground connection for channel 5 power stage.
16	GNDP1	Ground; ground connection for channel 1 power stage.
17	FWD1	Free wheeling diode; for channel 1.

Pin	Symbol	Function
18	LOAD1	Output; for channel 1.
19	LOAD2	Output; for channel 2.
20	FWD2	Free wheeling diode; for channel 2.
21	GNDP2	Ground; ground connection for channel 2 power stage.
22	VBAT	Supply voltage; connected to battery voltage with reverse protection diode and filter against EMC.
23	GND	Ground; signal ground. Internally connected to cooling tab.
24	CLK	Clock input; Main system clock.
25	DRV0	Direct drive input: 3.3 V or 5.0 V logical levels.
26	RESN	Control input; digital input: 3.3 V or 5.0 V logic levels. Active low reset input.
27	EN	Control input; digital input: 3.3 V or 5.0 V logic levels. Active high enable input.
28	DRV1	Direct drive input: 3.3 V or 5.0 V logical levels.
29	VDD	Supply voltage; supplies digital circuits. Connected to 5.0 V supply voltage.
30	GND	Ground; signal ground. Internally connected to cooling tab.
31	LOAD4	Output; for channel 4.
32	FWD4	Free wheeling diode; for channel 4.
33	GNDP4	Ground; for channel 4 power stage.
34	GNDP3	Ground; for channel 3 power stage.
35	FWD3	Free wheeling diode; for channel 3.
36	LOAD3	Output; for channel 3.
37	Cooling Tap	Connect externally to GND and heat sink area

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