

EDA Study Material for Reference

<https://mp.weixin.qq.com/s/GpwRTelbjRWgXMhVu5cUSA>

<input type="checkbox"/> 文件名	修改时间	类型	大小
<input type="checkbox"/> IC_EDA_Lite.z01	2022-05-21 18:08	z01文件	4.38GB
<input type="checkbox"/> IC_EDA_Lite.z02	2022-05-21 18:08	z02文件	4.38GB
<input type="checkbox"/> IC_EDA_Lite.z03	2022-05-21 18:08	z03文件	4.38GB
<input type="checkbox"/> IC_EDA_Lite.zip	2022-05-21 18:08	zip文件	3.04GB
<input type="checkbox"/> Vmware激活密钥.txt	2022-05-21 18:08	txt文件	91B
<input type="checkbox"/> VMware-workstation-full-16.1.0-17198959.exe	2022-05-21 18:08	exe文件	621.55MB

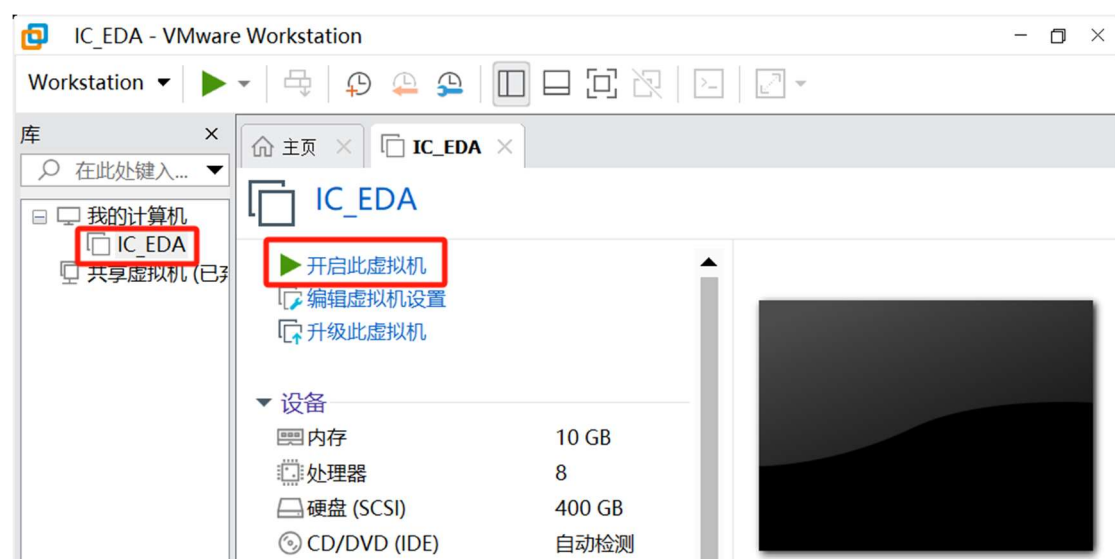
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Prepare the tools

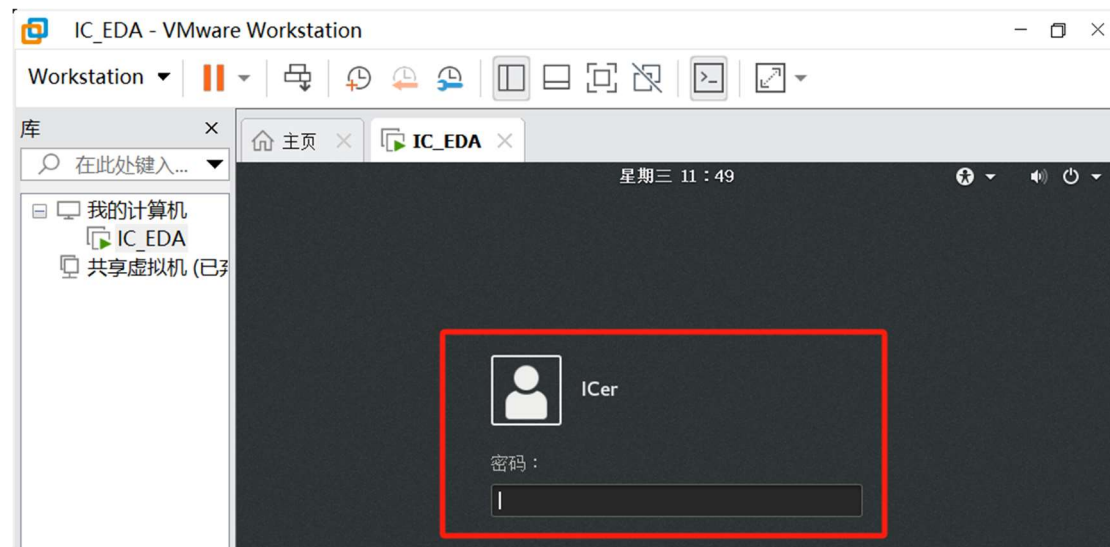
1. Install VMware and input the key
2. Extract the zip file.

Project breath_led

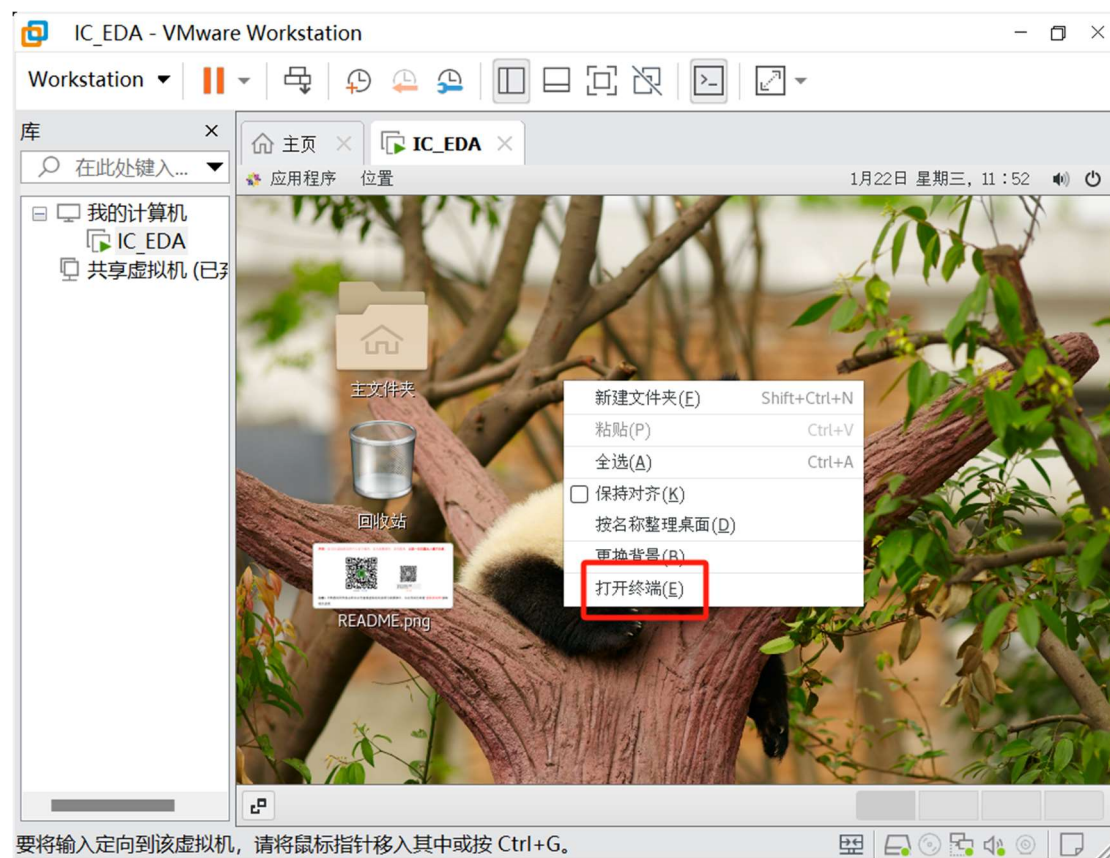
1. Run VMware and add/create virtual machine following the reference link.
2. Open virtual machine (Several minutes are needed to start the system)

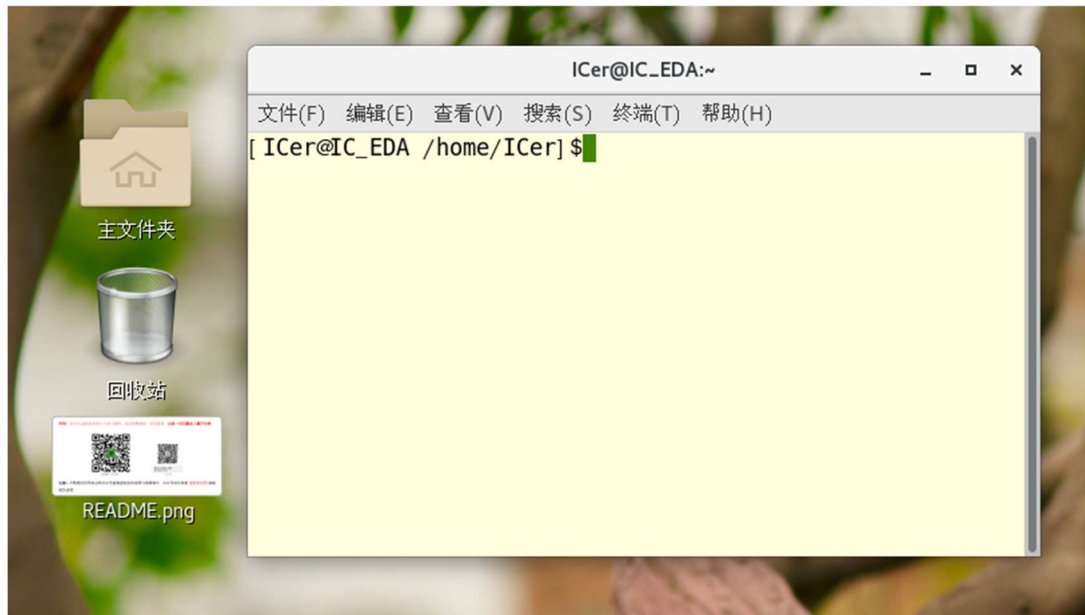


3. Login Linux with user ICer and password 2022



4. Right click on the Linux desktop to open terminal.





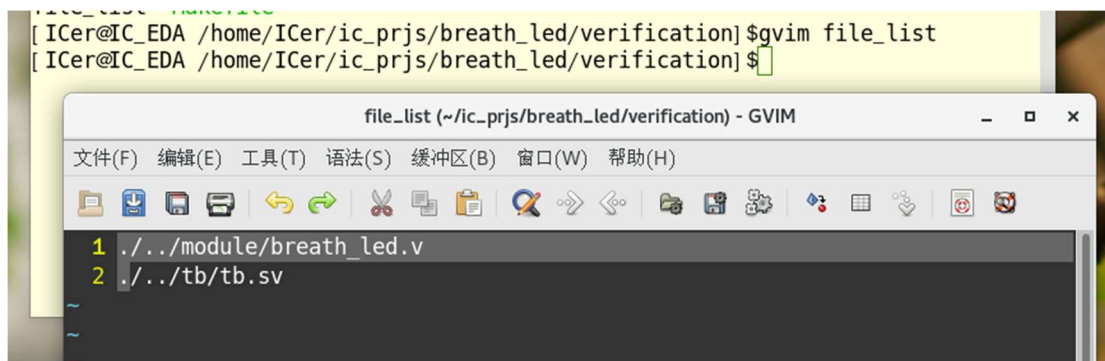
5. In terminal, go to `/home/ICer/ic_prjs/breath_led/verification`.



6. There are two files:

file_list list all the files needed for simulation. (In this project, `breath_led.v` is DUT while `tb.sv` is testbench.)

Makefile is the makefile to run command.



```
[ ICer@IC_EDA /home/ICer/ic_prjs/breath_led/verification]$gvim file_list
[ ICer@IC_EDA /home/ICer/ic_prjs/breath_led/verification]$gvim Makefile
[ ICer@IC_EDA /home/ICer/ic_prjs/breath_led/verification]$
```

```
1 #-----
2 all: \
3     vcs \
4     verdi
5 -----
6 #
7 # VCS
8 vcs: \
9     vcs \
10         -f file_list \
11         -timescale=1ns/1ns \
12         -full64 -R +vc +v2k -sverilog -debug_access+all \
13         |tee vcs.log
14 #-----
```

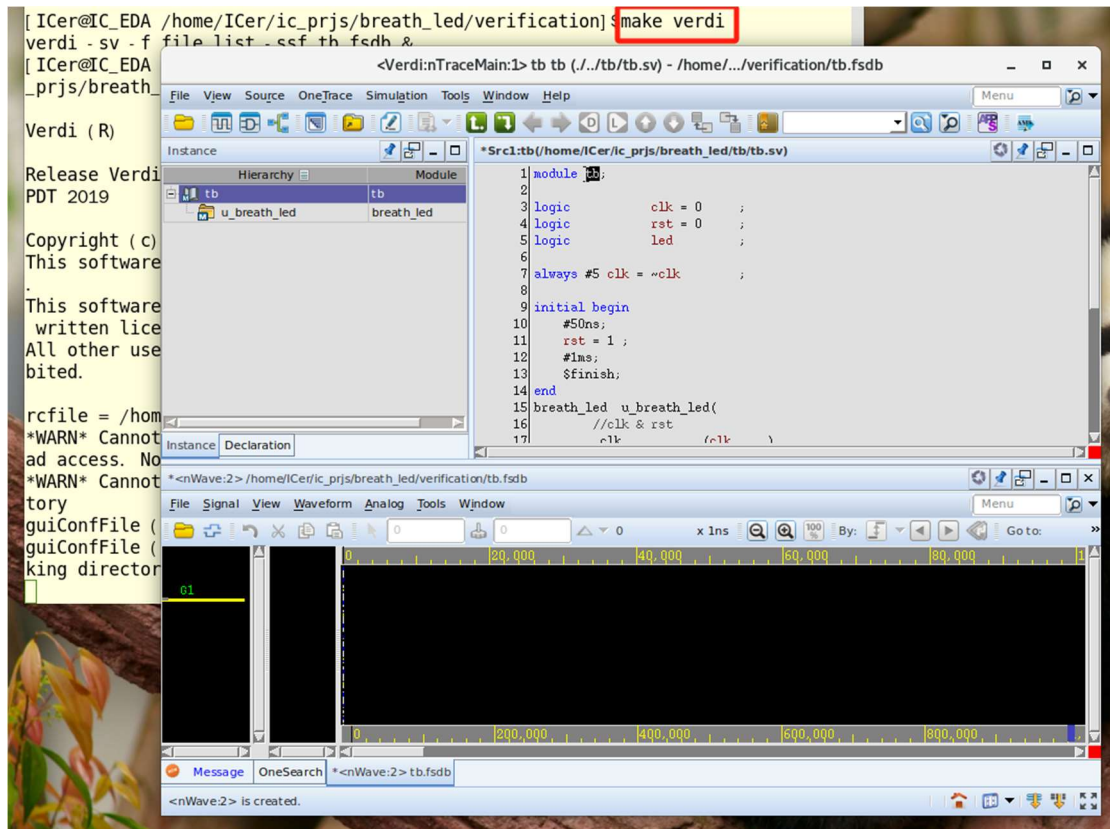
```
40 # verdi
41
42 verdi:
43     verdi -sv -f file_list -ssf tb.fsdb &
```

7. Run simulation by typing command “make vcs”

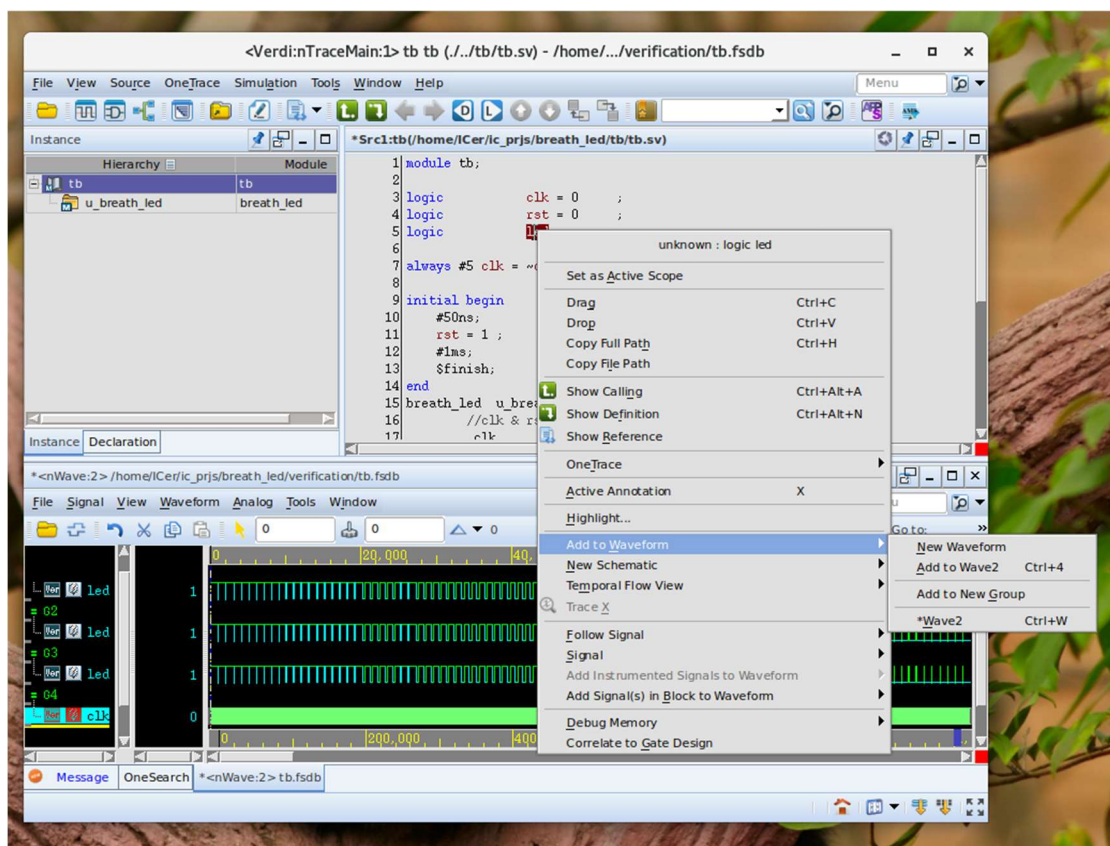
```
ICer@IC_EDA:~/ic_prjs/breath_led/verification
文件(F) 编辑(E) 查看(V) 搜索(S) 终端(T) 帮助(H)
ICer@IC_EDA /home/ICer/ic_prjs/breath_led/verification]$gvim Makefile
ICer@IC_EDA /home/ICer/ic_prjs/breath_led/verification]$make vcs
vcs \
    -f file_list \
    -timescale=1ns/1ns \
    -full64 -R +vc +v2k -sverilog -debug_access+all \
    |tee vcs.log
Chronologic VCS (TM)
Version 0-2018.09-1_Full64 -- Wed Jan 22 12:50:49 2025
Copyright (c) 1991-2018 by Synopsys Inc.
ALL RIGHTS RESERVED

This program is proprietary and confidential information of Synopsys Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.
```

8. Open Verdi to view waveform by typing command “make verdi”



9. In Verdi, add signal to waveform, or drag a signal to the waveform window, so that its waveform will appear.



Explanation of vcs options used in this project:

```
[ ICer@IC_EDA /home/ICer/ic_prjs/breath_led/verification]$gvim file_list
[ ICer@IC_EDA /home/ICer/ic_prjs/breath_led/verification]$gvim Makefile
[ ICer@IC_EDA /home/ICer/ic_prjs/breath_led/verification]$
```

```
1 #-----
2 all: \
3     vcs \
4     verdi
5 -----
6 #-----
7 # VCS
8 vcs :
9     vcs \
10         -f file_list \
11         -timescale=1ns/1ns \
12         -full64 -R +vc +v2k -sverilog -debug_access+all \
13         |tee vcs.log
14 #-----
```

-f *filename*

Specifies a file that contains a list of source files. You should specify the bottom most VHDL entity first, and then move up in order.

-f：指定一个文件，其中包含源文件的路径名列表和编译时选项。

-R

Runs the executable file immediately after VCS links it together.

-R：VCS 将可执行文件链接在一起后，立即运行可执行文件。

More options can be viewed in the following link:

<https://blog.csdn.net/burningCky/article/details/111558398>

<https://blog.csdn.net/burningCky/article/details/111743823>