

Electronics 315
Practical 3 Report
Class-AB power amplifier with preamplifier

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2 Circuit Diagram

See Figure 1 for the complete circuit diagram of the Power Amplifier together with the Pre-Amplifier.

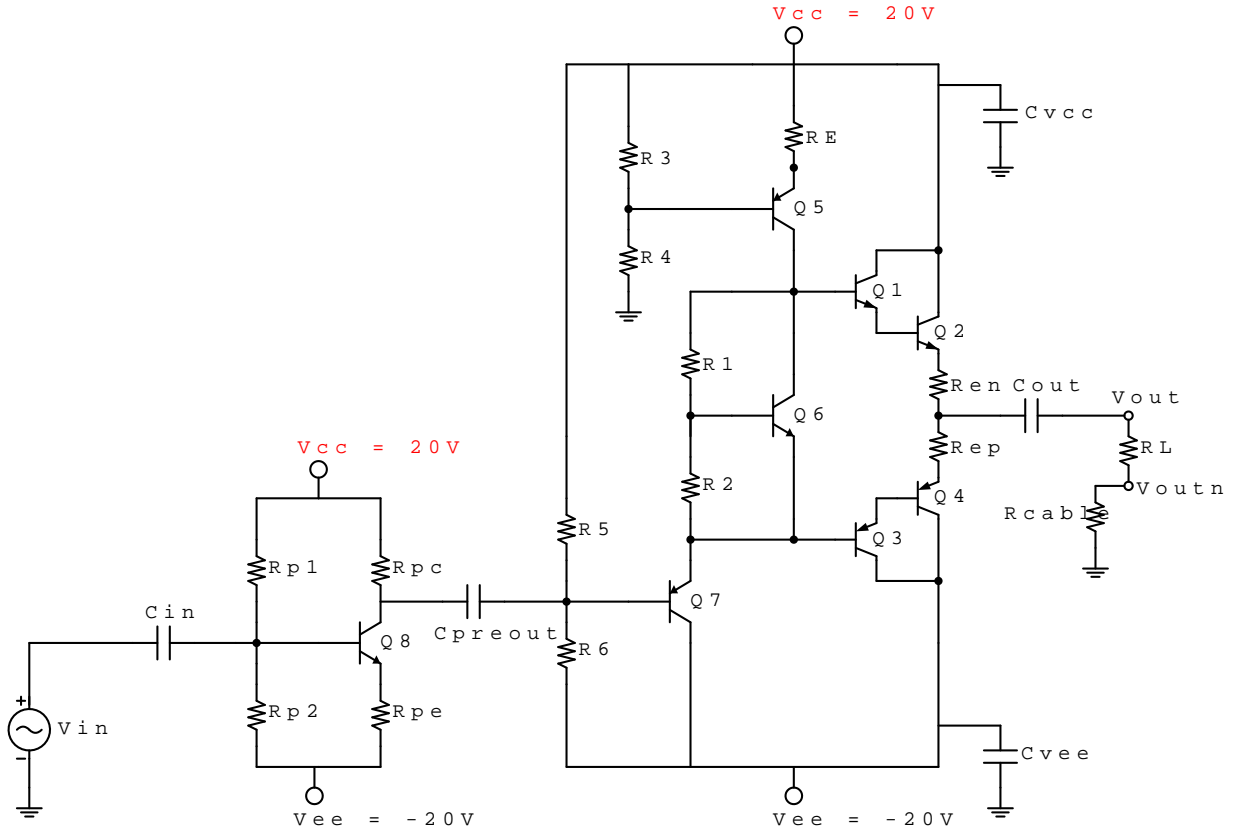


Figure 1: Complete Circuit Diagram of Power Amplifier with Pre-Amplifier

3 Power Amplifier Design

We are tasked to design a power amplifier that should deliver at least 8 W undistorted power into a $8\ \Omega$ resistive load. Design choices were made to select the appropriate transistors for this task, see table 1 for the list of transistors and their parameters.

COMPONENT	β (datasheet)	$V_{BE(on)}$	$V_{CE(sat)}$
Q1 2N2219A (npn)	100	0.7 V	0.3 V
Q2 TIP41C (npn)	50	0.6 V	0.2 V
Q3 2N2905A (pnp)	100	0.7 V	0.4 V
Q4 TIP42C (pnp)	50	0.6 V	0.3 V
Q5 2N2905A (pnp)	100	0.7 V	0.4 V
Q6 2N2219A (npn)	100	0.7 V	0.3 V
Q7 2N2905A (pnp)	100	0.7 V	0.4 V
Q8 2N2219A (npn)	100	0.7 V	0.3 V

Table 1: Datasheet Values for Transistors

Thus a design choice was made to design for 16 W undistorted power.

This results in:

$$\begin{aligned}\bar{P}_L &= \frac{V_{rms}^2}{R_L} = \frac{V_p^2}{2R_L} \\ 16 &= \frac{V_p^2}{2(8)} \\ V_p &= 16 \text{ V} \\ I_{L(max)} &= 2A\end{aligned}$$

Design choice: select $V_{RE} = 1V$ for ease of design.

Design Current Source:

$$\begin{aligned}I_{L(max)} &= 2A = I_{EQ(max)} \\ \text{When both transistors Q1 \& Q2 are on:} \\ I_{BQ(max)} &= \frac{I_{EQ(max)}}{\beta_1 \beta_2} \\ \text{See Table 1 } \beta_1 &= 100 \quad \beta_2 = 50 \\ I_{BQ(max)} &= \frac{2}{(100)(50)} = 400 \mu A\end{aligned}$$

Choose $I_{C6(min)} = 1mA$ to ensure that the VBE- multiplier stays on

$$\begin{aligned}I_{C6(max)} &= 1 \text{ mA} + 400 \text{ mA} \\ I_{C6(max)} &= 1.4 \text{ mA}\end{aligned}$$

Max base current at Q:

$$\begin{aligned}I_{B6(max)} &= \frac{I_{C6(max)}}{\beta_{6(min)}} = \frac{1.4 \times 10^{-3}}{100} \\ I_{B6(max)} &= 14 \text{ uA}\end{aligned}$$

Choose $I_{R1} \gg I_{B6(max)}$ such that we can ignore I_{B6} when designing

Choose I_{R1} as $0.5I_{C6(max)} = 0.7 \text{ mA}$

Current Source must supply at least:

$$\begin{aligned}I_{C5} &= I_{R1} + I_{C6(min)} + I_{B1(max)} \\ I_{C5} &= 2.1 \text{ mA}\end{aligned}$$

Choose $I_C = 2.5 \text{ mA}$, higher value chosen for a bit of headroom

$$\therefore R_E = \frac{V_{RE}}{I_C} = \frac{1}{2.5 \times 10^{-3}} = 400\Omega$$

Select R_B for bias stability

$$\begin{aligned}R_B &= 0.1\beta_5 \\ R_B &= 0.1(100)(400) \\ R_B &= 4k\Omega \\ \therefore I_{B5} &= \frac{I_{C5}}{\beta_5} = \frac{2.5 \times 10^{-3}}{100} = 25\mu A\end{aligned}$$

$$\begin{aligned}
\therefore 20 - V_{TH} &= V_{RE} + V_{EB_5(On)} + I_{\beta 5} R_B \\
\therefore V_{TH} &= 20 - 1 - 0.7 - (25\mu A)(4000) \\
\therefore V_{TH} &= 18.2 \text{ V}
\end{aligned}$$

$$\begin{aligned}
V_{TH} &= \frac{R_4}{R_3 + R_4} V_{CC} \dots (1) \quad \& \quad \frac{R_3 R_4}{R_3 + R_4} = R_B \dots (2) \\
\therefore \text{sub}(2) &\rightarrow (1) \\
\therefore V_{TH} &= \frac{R_B}{R_3} V_{CC} \\
\therefore R_3 &= \frac{4000(20)}{18.2} \\
R_3 &= 4.4\text{k}\Omega \\
\therefore R_4 &= 44.44\text{k}\Omega
\end{aligned}$$

Design VBE-Multiplier:

$$\begin{aligned}
\therefore V_{BB} &= V_{BE_2(On)} + V_{EB_4(On)} + V_{EB_3(On)} + V_{EB_1(On)} \\
\left(1 + \frac{R_1}{R_2}\right) V_{BE_6} &= 2.6 \text{ V} \\
\therefore V_{BE_6} + \frac{R_1}{R_2} V_{BE_6} &= 2.6 \\
\therefore \frac{R_1}{R_2} &= 2.71428
\end{aligned}$$

$$\begin{aligned}
I_{R_1} &= \frac{V_{BB}}{R_1 + R_2} \\
0.7 \times 10^{-3} &= \frac{2.6 \text{ V}}{R_1 + R_2} \\
\therefore R_1 + R_2 &= 3.714\text{k}\Omega \quad \& \quad \frac{R_1}{R_2} = 2.7143 \\
\therefore (2.714R_2) + R_2 &= 3.714\text{k}\Omega \\
R_2 &= 1000\Omega \\
\therefore R_1 &= 2.714\text{k}\Omega
\end{aligned}$$

Design Current Sink:

At $V_i = 0$, all of I_{C5} flows into Q7

For max output swing $V_o = 0$ if $V_i = 0$

$$\begin{aligned}
\therefore V_{B3} &= 0 - 0.6 \text{ V} - 0.7 \text{ V} \\
V_{B3} &= -1.3 \text{ V} \\
I_{Q7} = I_{C5} &= 2.5 \text{ mA}
\end{aligned}$$

$$V_{B3} = V_{BE_{7(on)}} + I_{B7}R_B + V_{TH} \quad ; \quad (I_{B7} = \frac{I_{C7}}{\beta})$$

$$\therefore V_{TH} = -1.3 - 0.7 - \frac{2.5 \times 10^{-3}}{100}(150000)$$

$$V_{TH} = -5.75 \text{ V}$$

$$V_{TH} = \frac{R_6}{R_5 + R_6} (V_{CC} - V_{EE}) + V_{EE} \quad \& \quad R_B = \frac{R_5 R_6}{R_5 + R_6}$$

$$\therefore V_{TH} = \frac{R_B}{R_5} (20 - (-20)) - 20$$

$$-5.75 + 20 = \frac{150000}{R_5} (40)$$

$$\therefore R_5 = 421.052 \text{ k}\Omega$$

$$\therefore R_6 = 233.010 \text{ k}\Omega$$

Input Resistance:

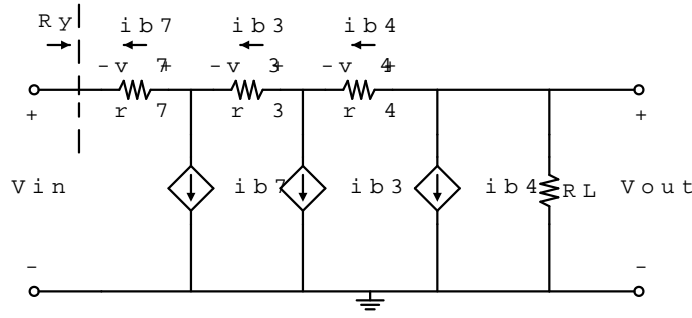


Figure 2: Power Amplifier Small Signal Equivalent

See figure 2 for visual representation of the small signal equivalent of the power amplifier when Q3 & Q4 are on.

$$R_y = r_{\pi 7} + (\beta_7 + 1) [r_{\pi 3} + (\beta_3 + 1) [r_{\pi 4} + (\beta_4 + 1) R_L]]$$

Using Spice the collector currents through Q3, Q4 and Q5 were found:

$$I_{C5} = 2.5 \text{ mA}$$

$$I_{C4} = 8.216 \text{ mA}$$

$$I_{C3} = 74.9 \text{ uA}$$

$$\begin{aligned}
r_{\pi_7} &= \frac{\beta_7 V_T}{I_{C6}} = \frac{100(0.026)}{2.5 \times 10^{-3}} \\
r_{\pi_7} &= 1040\Omega \\
r_{\pi_4} &= \frac{\beta_4 V_T}{I_{C4}} \\
r_{\pi_4} &= 158.228 \\
r_{\pi_3} &= \frac{\beta_3 V_T}{I_{C3}} = \frac{100(0.026)}{74.9 \times 10^6} \\
r_{\pi_3} &= 34.713\text{k}\Omega
\end{aligned}$$

$$\begin{aligned}
\therefore R_y &= r_{\pi_7} + (\beta_7 + 1) [r_{\pi_3} + (\beta_3 + 1) [r_{\pi_4} + (\beta_4 + 1) R_L]] \\
R_y &= 1040 + (101) [34.113 \times 10^3 + (101)[158.23 + (51) \times 8]] \\
R_y &= 9.28\text{M}\Omega
\end{aligned}$$

$$\begin{aligned}
\therefore R_{\text{in}} &= R_5 // R_6 // R_y \\
R_{\text{in}} &= (421.052 \times 10^3) // (233.010 \times 10^3 // (9.28 \times 10^6)) \\
R_{\text{in}} &= 147.614\text{k}\Omega
\end{aligned}$$

R2 was tuned down from 1000 Ω to 900 Ω in order to decrease Total Harmonic Distortion (THD).

4 Preamplifier Design

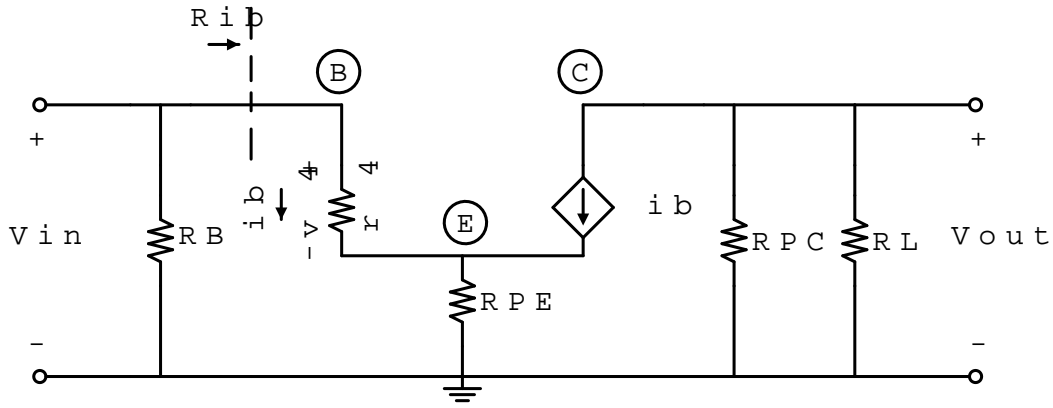


Figure 3: Pre-Amplifier Small Signal Equivalent

Design V_o of the Pre-Amplifier to be 16V, such that that gain $A_v = \frac{V_o}{V_i} = \frac{16}{0.5} = 32$ This is because the Power Amplifier needs an output voltage of 16V amplitude as per design choice, but the Power Amplifier has a gain

of approximately 1, so the gain stage needs to come from the Pre-Amplifier.

$$\begin{aligned}
 r_{\pi} &= \frac{100(0.026)}{5 \times 10^{-3}} \\
 r_{\pi} &= 520\Omega \\
 A_v &= \frac{V_o}{V_i} = \frac{16}{0.5} = 32 \\
 V_o &= -\beta i_b (R_{P_C} // R_L) \\
 V_i = V_x \quad &\& \quad V_x = i_b r_{\pi} + i_b (\beta + 1) R_{P_E} \\
 A_v &= \frac{V_o}{v_i} = \frac{-\beta i_b (R_{P_C} // R_L)}{i_b r_{\pi} + i_b (\beta + 1) R_{P_E}} = \frac{-\beta (R_{P_C} // R_L)}{r_{\pi} + (\beta + 1) R_{P_E}} \\
 R_L &= R_{in} \text{ (from power Amp)} = 147.614k\Omega \\
 \therefore |A_v| &= 32 = \left| \frac{-\beta (R_{P_C} // R_L)}{r_{\pi} + (101) R_{P_E}} \right| \dots (1) \text{ need 1 more Equation to solve}
 \end{aligned}$$

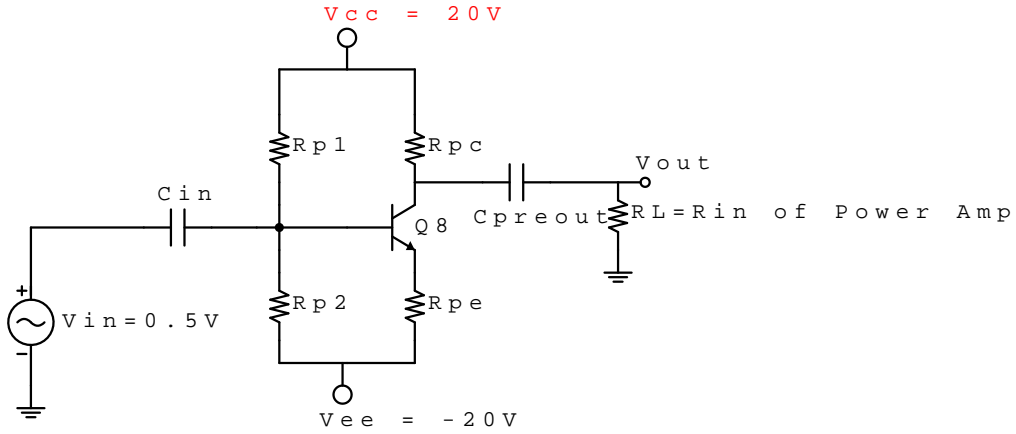


Figure 4: Pre-Amplifier Circuit

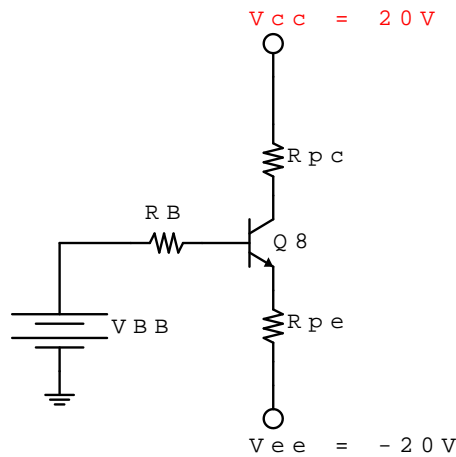


Figure 5: Thevenin Equivalent Of Pre-Amplifier Circuit

See figure 4 and figure 5 for visual reference to the calculations that follow:

For Max Output Swing:

$$V_{CEQ} = \frac{V_{CC} - V_{EE} - V_{CE(sat)}}{2}$$

$$V_{CEQ} = \frac{20 - (-20) - 0.3}{2}$$

$$V_{CEQ} = 19.85$$

From above choose $V_{CEQ} = 20V$ and $I_{CEQ} = 5mA$

$$R_B = R_{P_1} // R_{P_2}$$

KVL output loop: see figure 5

$$V_{CC} - V_{EE} = I_C R_{PC} + V_{CEQ} + I_E R_{PE}$$

$$\therefore R_{PE} = \frac{V_{CC} - V_{EE} - V_{CEQ} - I_C R_{PC}}{I_E}$$

$$R_{PE} = \frac{20 - (-20) - 20 - 5 \times 10^{-3} R_{PC}}{\frac{\beta+1}{\beta} (5 \times 10^{-3})} \dots (2)$$

$$\therefore \text{sub}(2) \rightarrow (1)$$

$$32 = \frac{+100 (R_{pc}/1147.815 \times 10^3)}{520 + (101) \left[\frac{20-5 \times 10^{-3} R_{pc}}{\frac{101}{100} 5 \times 10^{-3}} \right]}$$

$$\therefore 32 = \frac{100 \left(\frac{R_{PC} (147.614 \times 10^3)}{R_{PC} + 147.614 \times 10^3} \right)}{520 + 400000 - 100 R_{PC}}$$

$$\frac{12816640 - 3200 R_{PC}}{100} = \left(\frac{R_{PC} (147.614 \times 10^3)}{R_{PC} + 147.614 \times 10^3} \right)$$

$$\therefore R_{PC} = 3886.9\Omega$$

$$\therefore R_{PE} = 111.98\Omega$$

$$R_B = 0.1\beta R_{PF} = 0.1(100)(111.98) = 1119.8\Omega$$

KVL Input Loop: see figure 5

$$-V_{BB} + I_B R_B + V_{BE(on)} + I_E R_{PE} + V_{EE} = 0$$

$$V_{BB} = I_B R_B + V_{BE(on)} + I_E R_{PE} + V_{EE}$$

$$V_{BB} = \frac{5 \times 10^{-3}}{100} (1119.8) + 0.7 \text{ V} + \frac{101}{100} 5 \times 10^{-3} (111.98) - 20$$

$$V_{BB} = -18.6785V$$

$$V_{BB} = \frac{R_{P_2}}{R_{P_1} + R_{P_2}} (V_{CC} - V_{EE}) + V_{EE} \quad ; \quad R_B = \frac{R_{P_1} R_{P_2}}{R_{P_1} + R_{P_2}}$$

solving the above two equations simultaneously yields the following result:

$$-18.6785 = \frac{R_B}{R_{P_1}} (20 - (-20) + (-20))$$

$$\therefore R_{P_1} = 33.895 \text{ k}\Omega$$

$$\therefore R_{P_2} = 1.158 \text{ k}\Omega$$

No fine tuning was made to the Pre-Amplifier calculations.

5 Frequency Analysis and Capacitor Design

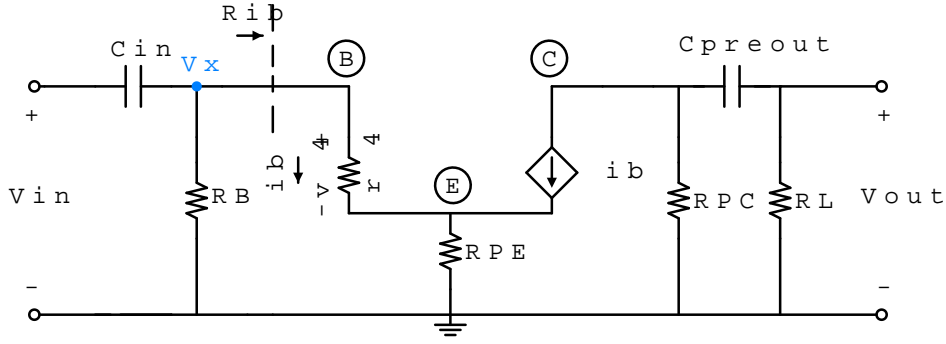


Figure 6: Pre-Amplifier Small Signal Equivalent with Capacitors

From Pre-Amplifier Design:

$$R_L = R_{in} = 147.614 \text{ k}\Omega \quad \& \quad R_B = R_{P_1} // R_{P_2} = 1119.8 \Omega$$

$$R_{R_C} = 3886.9 \Omega \quad ; \quad r_{\pi} = 520 \Omega$$

$$R_{P_E} = 111.98 \Omega \quad ; \quad R_{P_1} = 33.8948 \text{ k}\Omega$$

$$R_{P_2} = 1.158 \text{ k}\Omega$$

The audible hearing range of humans is around 20 Hz to 20 kHz, thus we will design our low cutoff frequency (f_L) for 20Hz.

To minimise the cost and size of capacitors, a good design strategy would be to design for the smallest possible capacitor values.

First the τ (time constant) for each capacitor is found, assuming that each capacitor is dominant.

C_{in} : (Short C_{preout})
(see figure 7)

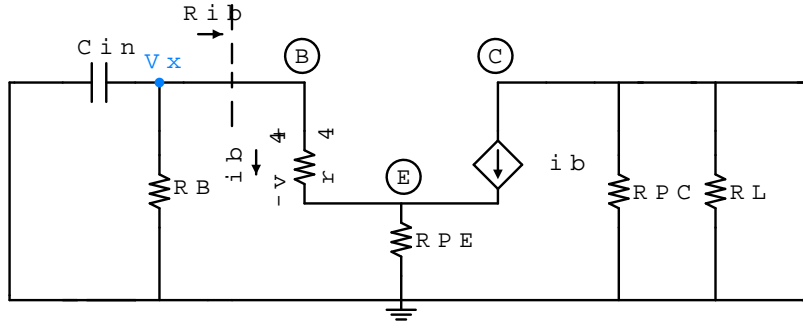


Figure 7: Equivalent Resistance for Cin

$$R_{ib} = \frac{V_x}{i_b} = \frac{i_b (r_\pi + (\beta + 1)R_{PE})}{i_b} = r_\pi + (\beta + 1)R_{PE}$$

$$\begin{aligned} R_{eq} &= R_B // R_{ib} \\ &= R_B / [r_\pi + (\beta + 1)R_{PE}] \\ &= 1119.8 / [520 + (101)(111.98)] \end{aligned}$$

$$R_{eq} = 1022.968 \Omega$$

$$\therefore \tau_{C_{in}} = R_{eq} C_{in}$$

$$\tau_{C_{in}} = 1022.968 C_{in}$$

C_{preout} : (Short C_{in})
(see figure 8)

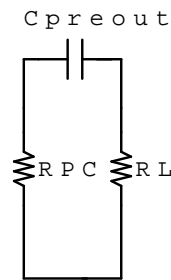


Figure 8: Equivalent Resistance for Cpreout

$$\begin{aligned} R_{eq} &= R_{PC} + R_L \\ &= 3886.9 + 147.614 \times 10^3 \end{aligned}$$

$$R_{eq} = 151.5 \text{ k}\Omega$$

$$\therefore \tau_{C_{preout}} = R_{eq} C_{preout}$$

$$\tau_{C_{preout}} = 151.5 \times 10^3 C_{preout}$$

C_{out} :
(see figure 9)

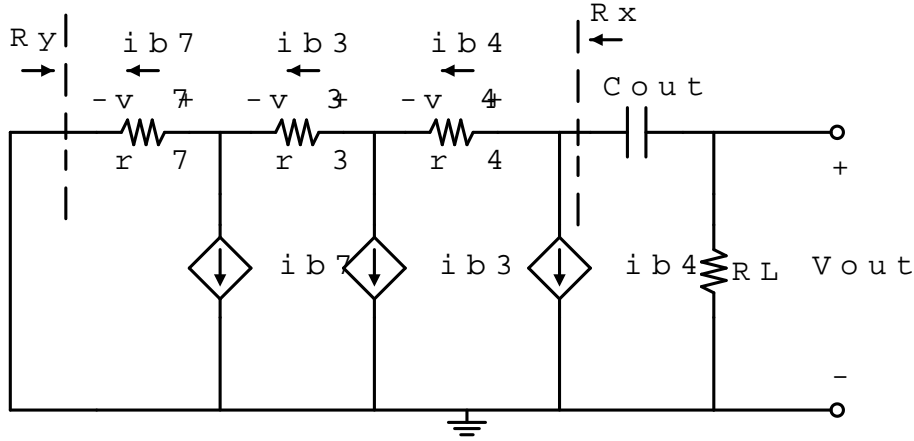


Figure 9: Equivalent Resistance for Cout (Q3 & Q4 on)

Using Spice $R_x = 8\Omega$

$$R_{eq} = R_L + R_x$$

$$R_{eq} = 8 + 8$$

$$R_{eq} = 16$$

$$\tau_{C_{out}} = 16C_{out}$$

Now we want to find the dominant capacitor, the capacitor with the smallest time constant will have the highest cutoff frequency and thus be the dominant capacitor.

$\therefore C_{out}$ is dominant ; $f_L = 20Hz$

$$\therefore \tau_{C_{out}} = \frac{1}{2\pi f}$$

$$\therefore 15.8C_{out} = \frac{1}{2\pi(20)}$$

$$\therefore C_{out} = 497.36\mu F$$

$$C_{out} = 500\mu F$$

Now select C_{in} & C_{preout} a decade lower: $f_L = \frac{20}{10} = 2Hz$ so as not to affect the required 20Hz cutoff frequency.

$$\therefore \tau_{in} = \frac{1}{2\pi f}$$

$$1022.968C_{in} = \frac{1}{2\pi(2)}$$

$$C_{in} = 77.79\mu F$$

$$\tau_{C_{preout}} = \frac{1}{2\pi f}$$

$$151.5 \times 10^3 C_{preout} = \frac{1}{2\pi(2)}$$

$$C_{preout} = 0.525\mu F$$

For the practical construction of the circuit, different capacitor values were used as they performed better and they were the values provided to us with our component packages.

$$C_{in} = 10\mu F$$

$$C_{preout} = 10\mu F$$

$$C_{out} = 4700\mu F$$

6 Gain Analysis

The Pre-Amplifier was designed to have a gain $A_v = 32$. Thus with an input voltage of 0.5V amplitude the output voltage should have an amplitude of 16V. Simulating the Pre-Amplifier in NGSpice yields the following graph (see figure 10)

As seen from figure 10 the output voltage is 15V, which is quite close to the designed value of 16V, thus giving a gain $A_v = 30$. The output voltage is nearly perfectly symmetrical thus providing maximum output voltage swing with no clipping.

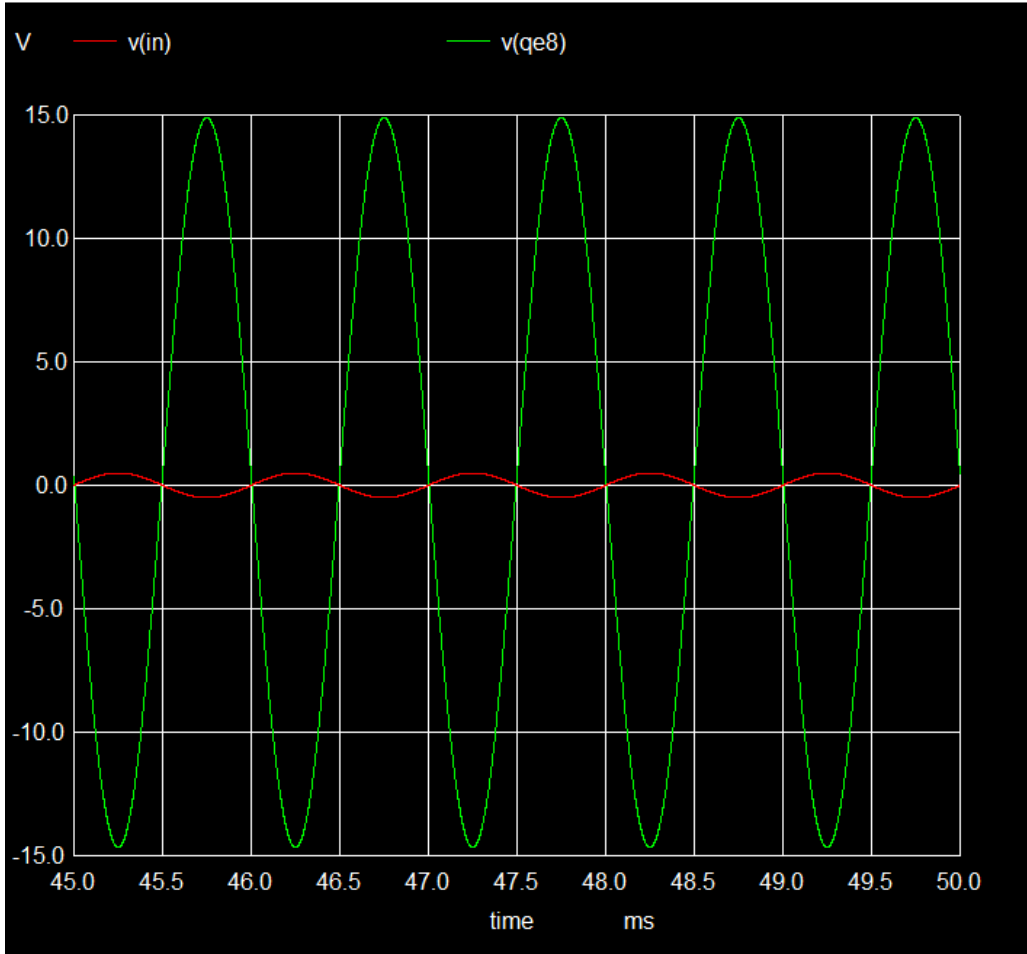


Figure 10: Pre-Amplifier Gain ($V_i=0.5$)

A power amplifier has a theoretical gain $A_v \approx 1$, thus when simulating the Power Amplifier in Spice we expect the output of the power amplifier to track the input from the pre-amplifier quite closely. As seen from figure 11 ($v(\text{out})$ is the output of the power amplifier and $v(\text{qe8})$ is the input from the pre-amplifier)

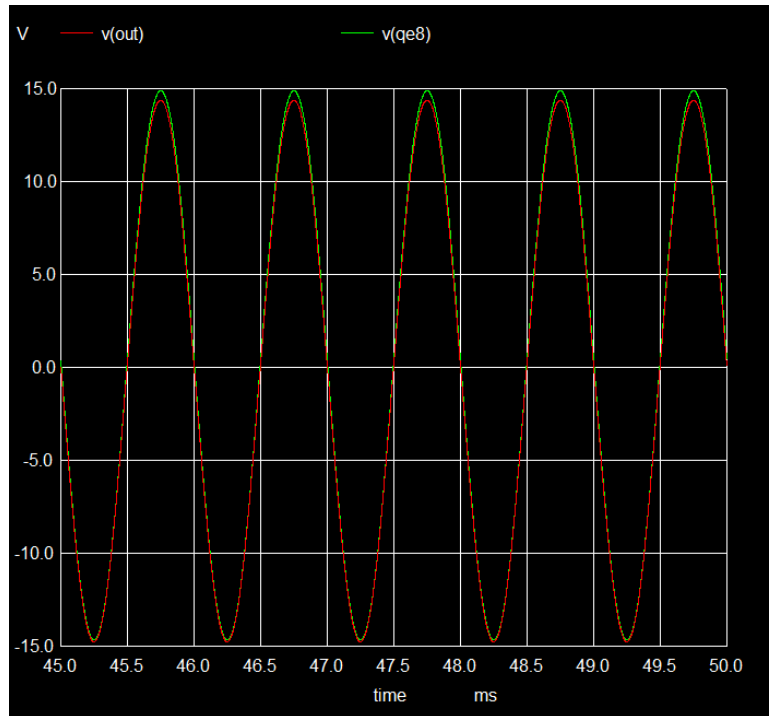


Figure 11: Power Amplifier Gain

Adding the pre-amplifier and the power amplifier together to form the complete audio amplifier yields the following graph when simulated in Spice using a 1kHz input signal with an amplitude of 0.5A. As seen from figure 12 the simulated gain $A_v = 30.24$ is slightly lower than the designed gain $A_v = 32$. This results in an output voltage amplitude of 15.2V, which is still enough to meet the minimum peak output voltage of 11.3V.

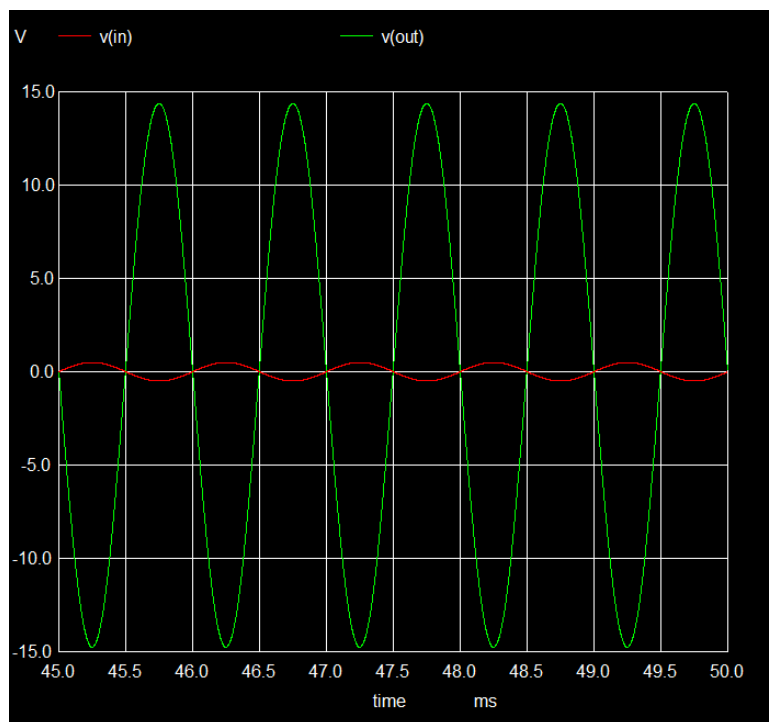


Figure 12: Complete Audio Amplifier Gain

7 Power and Thermal Analysis

Power Analysis:

NGSpice was used in order to calculate the power dissipated by all the components in the circuit, formulas 1 & 2 were used within spice to solve for these power dissipations.

To calculate the power dissipated through each transistor equation 1 was used.

$$P_Q = V_{CE}I_{CQ} \quad (1)$$

To calculate the power dissipated through each resistor equation 2 was used.

$$P_R = \frac{V^2}{R} \quad (2)$$

See table 2 for a complete list of the power dissipated in every component of the circuit.

COMPONENT	POWER DISSIPATION
Q1	54.73 mW
Q2	6.40 W
Q3	39.52 mW
Q4	3.72 W
Q5	51.64 mW
Q6	4.9 mW
Q7	41.24 mW
Q8	67.88 mW
R1	1.53 mW
R2	0.48 mW
R3	0.7 mW
R4	7.49 mW
R5	1.68 mW
R6	1.53 mW
Rpe	5.23 mW
Rpc	155.28 mW
Rp1	44.03 mW
Rp2	1.73 mW
RL	13.51 W
Rcable	1.69 mW

Table 2: Power dissipation of components.

As seen from table 2 all the resistors dissipate less than 0.25W and thus all the resistors can be small $\frac{1}{4}$ Watt carbon composites, except for R_L where a 25W load is used.

Thermal Analysis:

An ambient temperature of 30°C was chosen to account for operating temperatures slightly above normal room temperature.

A heatsink of 80x5x2mm was used to help dissipate heat and cool down the two power transistors.

For the Power Transistors Q2 and Q4, which use TIP41C and TIP42C packages formula 3 was used.

$$T_j = P_Q (\theta_{j-c} + \theta_{c-s} + \theta_{s-a}) + T_{ambient} \quad (3)$$

From the datasheets the following thermal resistances were obtained:

$$\theta_{j-c} = 1.92^\circ C$$

$$\theta_{c-s} = 1^\circ C$$

$$\theta_{s-a} = 10^\circ C$$

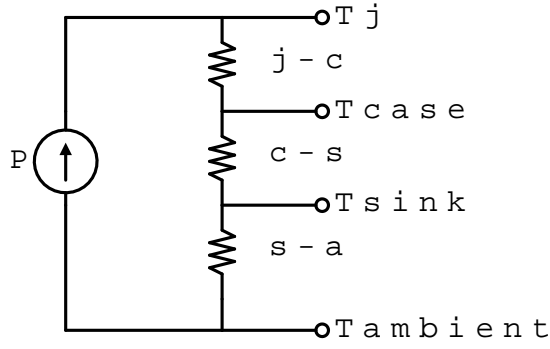


Figure 13: Thermal Equivalent Circuit for Transistors Q2 & Q4 (TIP41/2C packages)

TIP41C: Q_2 (T0-220 Package)

Using the power dissipated through each transistor calculated using Spice simulation: see Figure 13 and table 2

$$\begin{aligned}
 T_{j_2} &= P_{Q2}(\theta_{j-c} + \theta_{c-s} + \theta_{s-a}) + 30^\circ C \\
 T_{j_2} &= 6.39(1.92 + 1 + 10) + 30^\circ C \\
 T_{j_2} &= 112.56^\circ C
 \end{aligned}$$

TIP42C: Q_4 (T0-220 Package)

$$\begin{aligned}
 T_{j_4} &= P_{Q4}(\theta_{j-c} + \theta_{c-s} + \theta_{s-a}) + 30^\circ C \\
 T_{j_4} &= 3.429(1.92 + 1 + 10) + 30^\circ C \\
 T_{j_4} &= 78.06^\circ C
 \end{aligned}$$

For the other BJT transistors in TO-39 packages formula 4 was used.

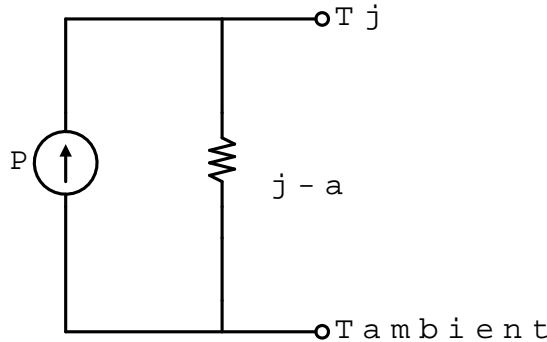


Figure 14: Thermal Equivalent Circuit for Transistors with T0-39 packages (Q1,Q3,Q5-Q8)

$$T_j = P_Q (\theta_{j-a}) + T_{ambient} \quad (4)$$

For 2N2219A Transistors: (T0-39 Package)

Using equation 4 and power dissipated through each transistor calculated using Spice simulation: see Figure 14 and table 2

$$\begin{aligned}
Q_1 : T_{j_1} &= P_{Q1}(\theta_{j-a}) + 30^\circ C \\
T_{j_1} &= 40.26^\circ C \\
Q_6 : T_{j_6} &= P_{Q6}(\theta_{j-a}) + 30^\circ C \\
T_{j_6} &= 30.91^\circ C \\
Q_8 : T_{j_8} &= P_{Q8}(\theta_{j-a}) + 30^\circ C \\
T_{j_8} &= 42.73^\circ C
\end{aligned}$$

For 2N905A Transistors: (T0-39 Package)

Using equation 4 and power dissipated through each transistor calculated using Spice simulation: see Figure 14 and table 2

$$\begin{aligned}
Q_3 : T_{j_3} &= P_{Q3}(\theta_{j-a}) + 30^\circ C \\
T_{j_3} &= 41.54^\circ C \\
Q_5 : T_{j_5} &= P_{Q5}(\theta_{j-a}) + 30^\circ C \\
T_{j_5} &= 45.08^\circ C \\
Q_7 : T_{j_7} &= P_{Q7}(\theta_{j-a}) + 30^\circ C \\
T_{j_7} &= 42.04^\circ C
\end{aligned}$$

These results are summarised in table 3 below.

COMPONENT	Temperature
Q1 2N2219A	40.26 °C
Q2 TIP41C	112.56 °C
Q3 2N2905A	41.54 °C
Q4 TIP42C	78.06 °C
Q5 2N2905A	45.084 °C
Q6 2N2219A	30.91 °C
Q7 2N2905A	42.04 °C
Q8 2N2219A	42.73 °C

Table 3: Thermal Analysis of Transistors.

8 Results and Conclusions

After all theoretical calculations and design choices were completed the results were simulated using NGSpice. Figure 15 shows the results obtained using the testbench with the theoretically calculated component values. However, most of these calculated resistor/capacitor values were not standard resistor/capacitor values, thus the closest possible resistor/capacitor was chosen that was available to us in the lab, or a series/parallel combination was made in order to get as close to the theoretically calculated values. Figure 16 shows the results obtained using the testbench with the chosen practical component values.

When comparing these two results, we can see that the power output dropped by around 2W with the practical values, the efficiency decreased by about 4%, but the THD was lower.

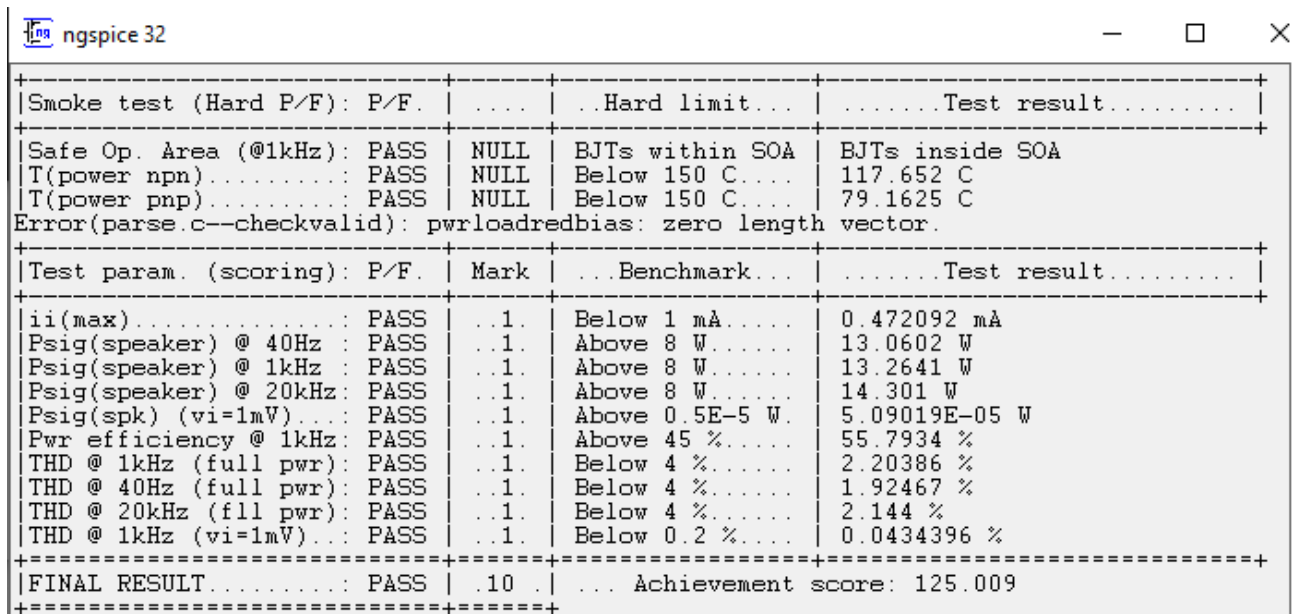
The efficiency of the audio amplifier is 51.49%, which is above the minimum requirement of 45%. The system has a output wattage of 11.21W at 1Khz and thus exceeds the minimum output wattage of 8W at 1kHz by 3.21W. The THD of the system is 1.92%, which is well below the required 4% and thus no audible distortion should occur.

Transistors Q2 & Q4 are both well below the safe operating temperature maximum of 150°C, with Q2 at 108.09°C and Q4 at 80.914°C. Hand calculated thermal results predicted temperatures of 112.56°C and 78.06°C for Q2 & Q4 respectively, thus the theory and simulated temperatures agree quite well.

As seen from figure 16, the circuit passes all the tests and meets all requirements and is ready to be physically constructed.

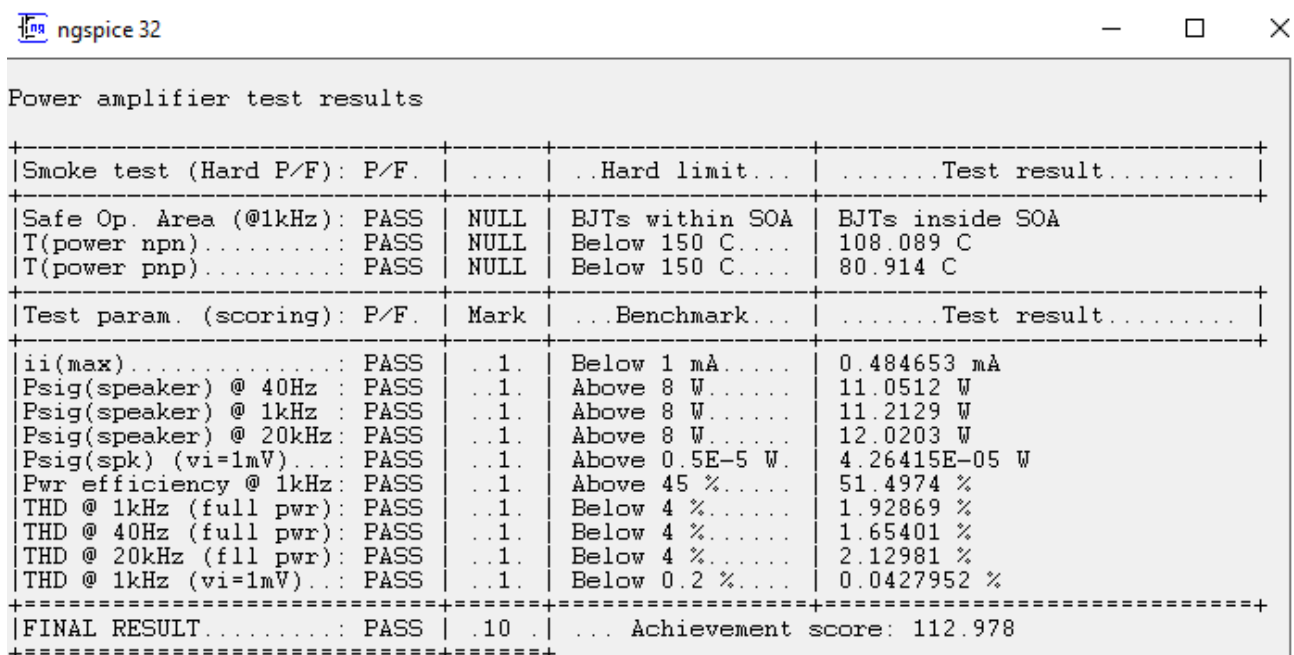
Figure 17 shows the gain of the physical circuit. The circuit failed to meet the minimum output voltage of 11.3V and only reached 9.6V, despite the simulation results showing that it should. This could be due to the resistors having too large tolerances that changed the biasing of the amplifiers.

Potential improvements to the circuit could be to use two transistors for the pre-amplifier in a cascade configuration which would provide a higher possible gain, which would increase the output wattage over the load. This would most likely require larger heatsinks with aluminum fins to help with heat dissipation in order to keep the power transistors cool to prevent them from overheating. Another potential improvement would be to use resistors that have lower tolerance %'s, however this would increase the total cost of the system.



ngspice 32				
Smoke test (Hard P/F): P/F. Hard limit... Test result.....				
Safe Op. Area (@1kHz): PASS NULL BJTs within SOA BJTs inside SOA				
T(power npn).....: PASS NULL Below 150 C.... 117.652 C				
T(power pnp).....: PASS NULL Below 150 C.... 79.1625 C				
Error(parse.c--checkvalid): pwrloadredbias: zero length vector.				
Test param. (scoring): P/F. Mark ...Benchmark... Test result.....				
ii(max).....: PASS ..1. Below 1 mA..... 0.472092 mA				
Psig(speaker) @ 40Hz : PASS ..1. Above 8 W..... 13.0602 W				
Psig(speaker) @ 1kHz : PASS ..1. Above 8 W..... 13.2641 W				
Psig(speaker) @ 20kHz: PASS ..1. Above 8 W..... 14.301 W				
Psig(spkr) (vi=1mV)...: PASS ..1. Above 0.5E-5 W. 5.09019E-05 W				
Pwr efficiency @ 1kHz: PASS ..1. Above 45 %..... 55.7934 %				
THD @ 1kHz (full pwr): PASS ..1. Below 4 %..... 2.20386 %				
THD @ 40Hz (full pwr): PASS ..1. Below 4 %..... 1.92467 %				
THD @ 20kHz (fll pwr): PASS ..1. Below 4 %..... 2.144 %				
THD @ 1kHz (vi=1mV)...: PASS ..1. Below 0.2 %.... 0.0434396 %				
=====				
FINAL RESULT.....: PASS .10 Achievement score: 125.009				
=====				

Figure 15: Spice Analysis Results from Test Bench using Theoretical Calculated Values



ngspice 32				
Power amplifier test results				
Smoke test (Hard P/F): P/F. Hard limit... Test result.....				
Safe Op. Area (@1kHz): PASS NULL BJTs within SOA BJTs inside SOA				
T(power npn).....: PASS NULL Below 150 C.... 108.089 C				
T(power pnp).....: PASS NULL Below 150 C.... 80.914 C				
Test param. (scoring): P/F. Mark ...Benchmark... Test result.....				
ii(max).....: PASS ..1. Below 1 mA..... 0.484653 mA				
Psig(speaker) @ 40Hz : PASS ..1. Above 8 W..... 11.0512 W				
Psig(speaker) @ 1kHz : PASS ..1. Above 8 W..... 11.2129 W				
Psig(speaker) @ 20kHz: PASS ..1. Above 8 W..... 12.0203 W				
Psig(spkr) (vi=1mV)...: PASS ..1. Above 0.5E-5 W. 4.26415E-05 W				
Pwr efficiency @ 1kHz: PASS ..1. Above 45 %..... 51.4974 %				
THD @ 1kHz (full pwr): PASS ..1. Below 4 %..... 1.92869 %				
THD @ 40Hz (full pwr): PASS ..1. Below 4 %..... 1.65401 %				
THD @ 20kHz (fll pwr): PASS ..1. Below 4 %..... 2.12981 %				
THD @ 1kHz (vi=1mV)...: PASS ..1. Below 0.2 %.... 0.0427952 %				
=====				
FINAL RESULT.....: PASS .10 Achievement score: 112.978				
=====				

Figure 16: Spice Analysis Results from Test Bench using Chosen Practical Values

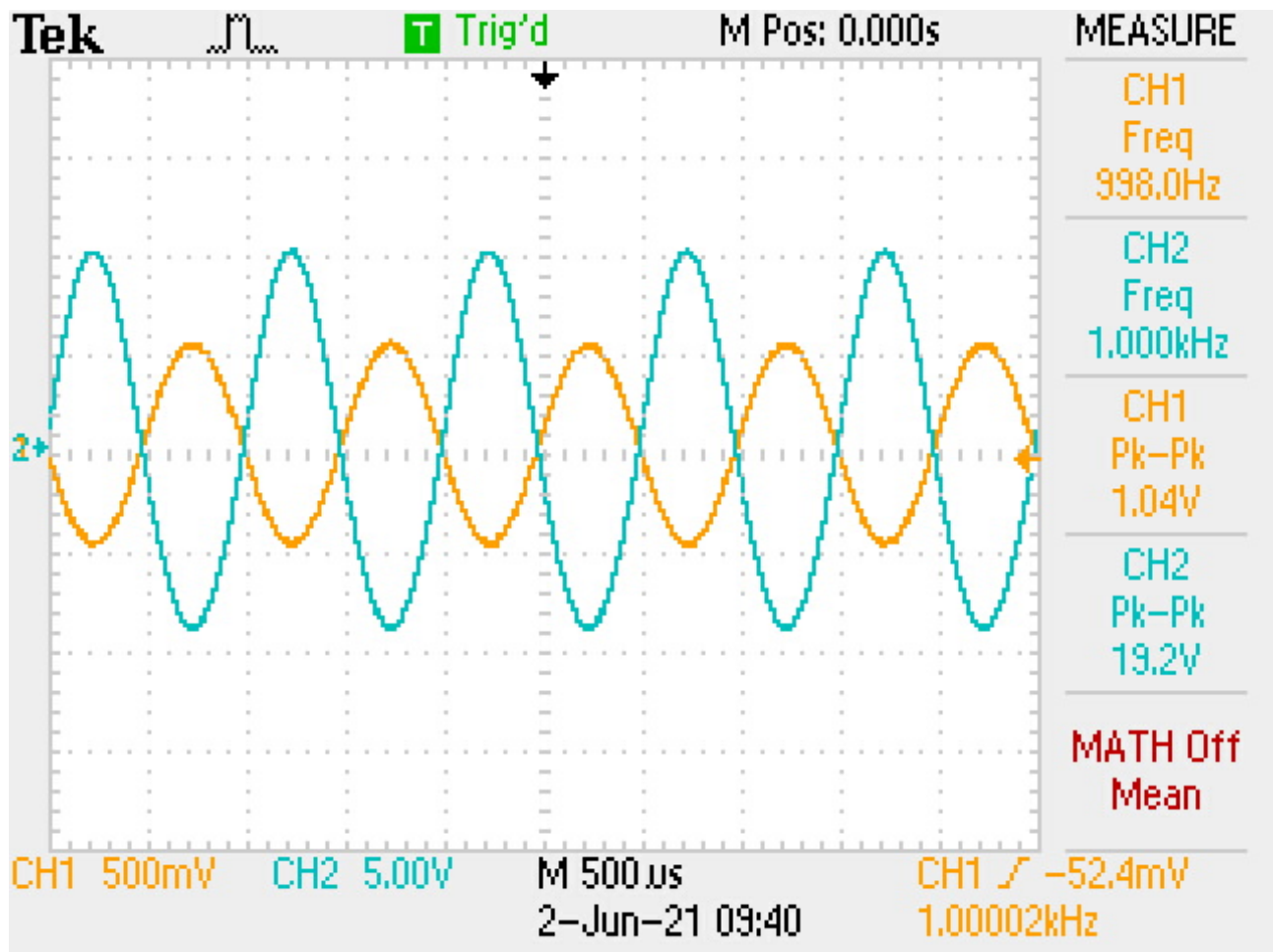


Figure 17: Gain of Physically Constructed Audio Amplifier