

N-Channel Logic Level Enhancement Mode Field Effect Transistor

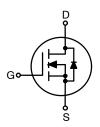
BSS138

General Description

These N-Channel enhancement mode field effect transistors are produced using **onsemi's** proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

Features

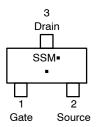
- 0.22 A, 50 V
 - $R_{DS(on)} = 3.5 \Omega @ V_{GS} = 10 V$
 - $R_{DS(on)} = 6.0 \Omega @ V_{GS} = 4.5 V$
- High Density Cell Design for Extremely Low R_{DS(on)}
- Rugged and Reliable
- Compact Industry Standard SOT-23 Surface Mount Package
- This Device is Pb-Free and Halogen Free





SOT-23-3 CASE 318-08

MARKING DIAGRAM



SS = Specific Device Code

M = Date Code*

= Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping [†]
BSS138,	SOT-23-3	3000 /
BSS138-G	(Pb-Free)	Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

BSS138

ABSOLUTE MAXIMUM RATINGS T_A = $25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Ratings	Unit	
V _{DSS}	Drain-Source Voltage	50	V	
V_{GSS}	Gate-Source Voltage	±20	1	
I _D	Drain Current – Continuous (Note 1)	0.22	Α	
	Drain Current – Pulsed (Note 1)	0.88	1	
P_{D}	Maximum Power Dissipation (Note 1)	0.36	W	
	Derate Above 25°C	2.8	mW/°C	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C	
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 s	300		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS $T_A = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Ratings	Unit
$R_{ heta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	350	°C/W

ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit			
OFF CHARACTERISTICS									
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	50	-	-	V			
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	-	72	_	mV/°C			
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 50 V, V _{GS} = 0 V	-	-	0.5	μΑ			
		$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V},$ $T_{J} = 125^{\circ}\text{C}$	-	-	5				
		V _{DS} = 30 V, V _{GS} = 0 V	_	-	100	nA			
I _{GSS}	Gate-Body Leakage	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	_	-	±100				
ON CHARAC	TERISTICS								
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 1 \text{ mA}$	0.8	1.3	1.5	V			
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C	-	-2	-	mV/°C			
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 0.22 A	-	0.7	3.5	Ω			
		V _{GS} = 4.5 V, I _D = 0.22 A	_	1.0	6.0	Ω			
		$V_{GS} = 10 \text{ V}, I_D = 0.22 \text{ A}, T_J = 125^{\circ}\text{C}$	_	1.1	5.8				
I _{D(on)}	On-State Drain Current	V _{GS} = 10 V, V _{DS} = 5 V	0.2	-	-	Α			
9FS	Forward Transconductance	V _{DS} = 10 V, I _D = 0.22 A	0.12	0.5	-	S			
DYNAMIC CH	IARACTERISTICS								
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V,	_	27	-	pF			
C _{oss}	Output Capacitance	f = 1.0 MHz	_	13	-	pF			
C _{rss}	Reverse Transfer Capacitance	7	_	6	-	pF			
R _G	Gate Resistance	V _{GS} = 15 mV, f = 1.0 MHz	_	9	-	Ω			

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted. (continued)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit		
SWITCHING CHARACTERISTICS								
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 30 \text{ V}, I_D = 0.29 \text{ A},$	-	2.5	5	ns		
t _r	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	_	9	18	ns		
t _{d(off)}	Turn-Off Delay Time		_	20	36	ns		
t _f	Turn-Off Fall Time		_	7	14	ns		
Qg	Total Gate Charge	$V_{DS} = 25 \text{ V}, I_D = 0.22 \text{ A},$	-	1.7	2.4	nC		
Q _{gs}	Gate-Source Charge	V _{GS} = 10 V	_	0.1	-	nC		
Q_{gd}	Gate-Drain Charge		-	0.4	-	nC		

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain-Source Diode Forward Current		İ	_	0.22	Α
V_{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.44 A (Note 2)	-	0.8	1.4	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

a) 350°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%

TYPICAL CHARACTERISTICS

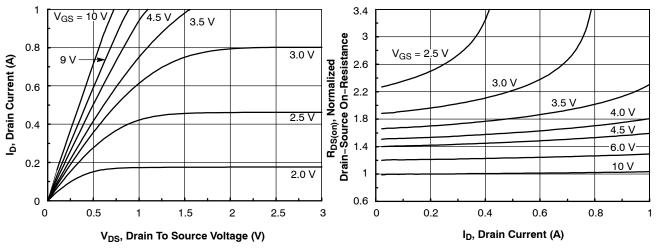


Figure 1. On-Region Characteristics

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

TYPICAL CHARACTERISTICS (continued)

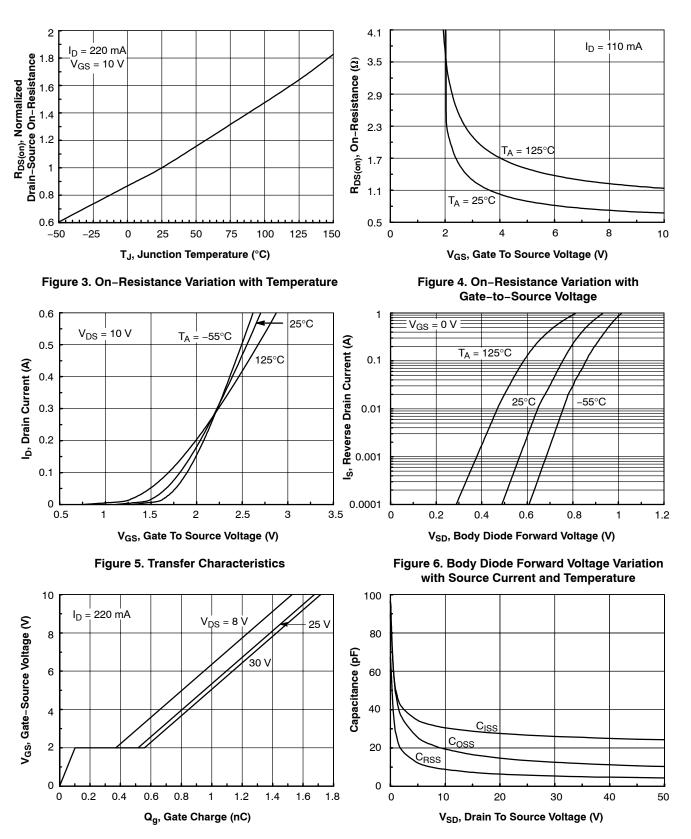


Figure 7. Gate Charge Characteristics

Figure 8. Capacitance Characteristics

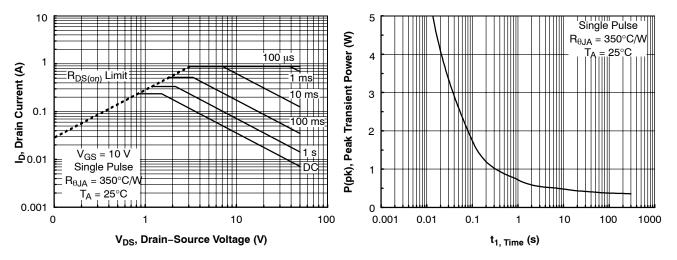


Figure 9. Maximum Safe Operating Area

Figure 10. Single Pulse Maximum Power Dissipation

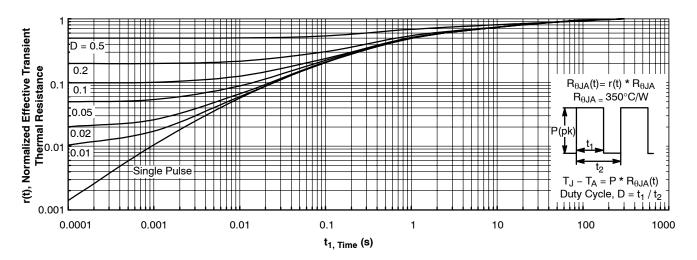


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1a. Transient thermal response will change depending on the circuit board design.



SOT-23 (TO-236) CASE 318-08 **ISSUE AS**

DATE 30 JAN 2018

SCALE 4:1 D - 3X b **TOP VIEW**







RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

3. ANODE

NOTES:

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH.
 MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL
- 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	М	ILLIMETE	RS		INCHES	
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
С	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
е	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
HE	2.10	2.40	2.64	0.083	0.094	0.104
Т	O٥		10°	O۰		10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code

= Date Code

= Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present.

STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE	ı	
STYLE 9:	STYLE 10:	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12:	STYLE 13:	STYLE 14:
PIN 1. ANODE	PIN 1. DRAIN		PIN 1. CATHODE	PIN 1. SOURCE	PIN 1. CATHODE
2. ANODE	2. SOURCE		2. CATHODE	2. DRAIN	2. GATE
3. CATHODE	3. GATE		3. ANODE	3. GATE	3. ANODE
STYLE 15:	STYLE 16:	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18:	STYLE 19:	STYLE 20:
PIN 1. GATE	PIN 1. ANODE		PIN 1. NO CONNECTION	I PIN 1. CATHODE	PIN 1. CATHODE
2. CATHODE	2. CATHODE		2. CATHODE	2. ANODE	2. ANODE
3. ANODE	3. CATHODE		3. ANODE	3. CATHODE-ANODE	3. GATE
STYLE 21:	STYLE 22:	STYLE 23:	STYLE 24:	STYLE 25:	STYLE 26:
PIN 1. GATE	PIN 1. RETURN	PIN 1. ANODE	PIN 1. GATE	PIN 1. ANODE	PIN 1. CATHODE
2. SOURCE	2. OUTPUT	2. ANODE	2. DRAIN	2. CATHODE	2. ANODE
3. DRAIN	3. INPUT	3. CATHODE	3. SOURCE	3. GATE	3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE				

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DESCRIPTION:	SOT-23 (TO-236)		PAGE 1 OF 1	

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3. CATHODE

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