Department of Computer Science and Information Engineering

National Cheng Kung University

數位系統實驗

LAB-11

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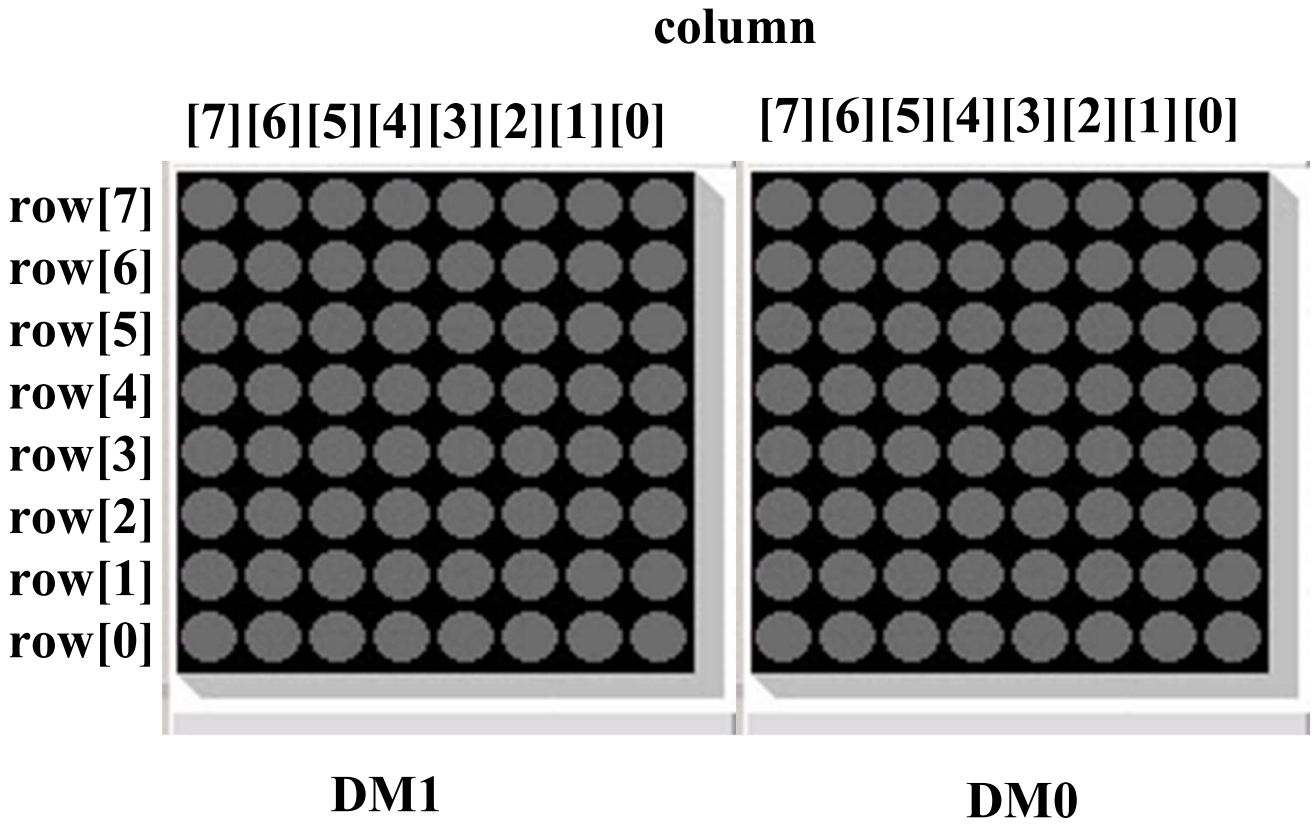
國立成功大學　資訊工程系

Outline

- 複習
  - Lab review
- Lab 說明
  - Lab Notice
  - Lab 11

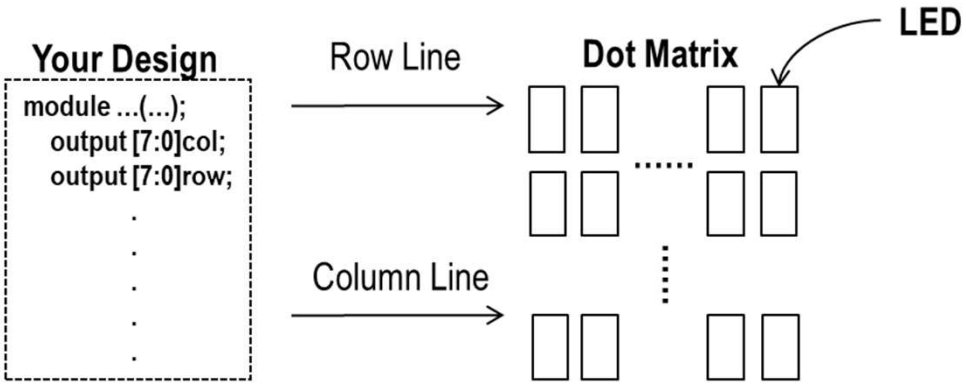
複習 - Lab Review

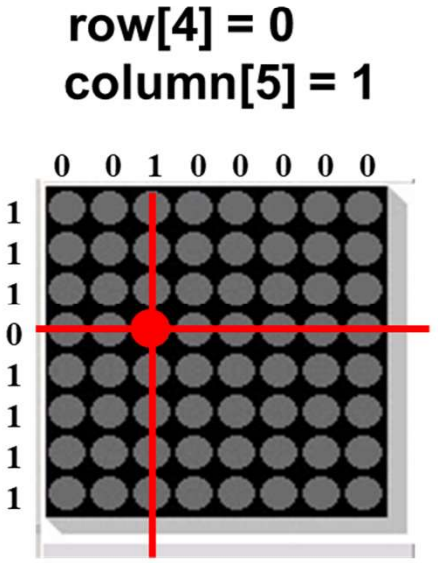
- **In DE0-CV external board**



複習 - **Lab Review**

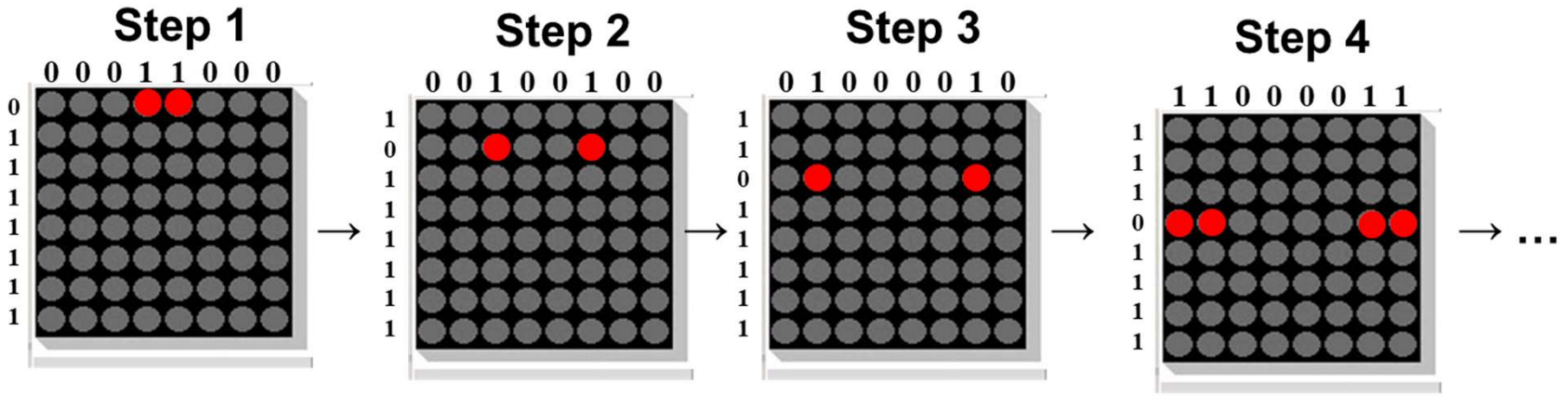
- 點矩陣由8 bits的row訊號及8 bits的column訊號控制
- 當row訊號第i個bit為0，column訊號的第j個bit為1，則第(i, j)個位置之點矩陣會被點亮





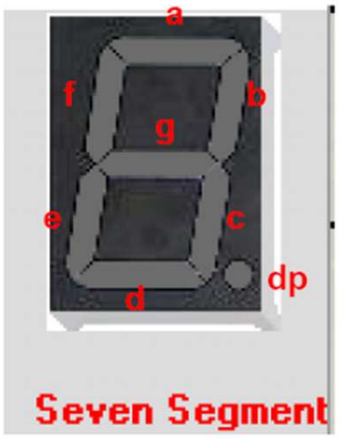
複習 - **Lab Review**

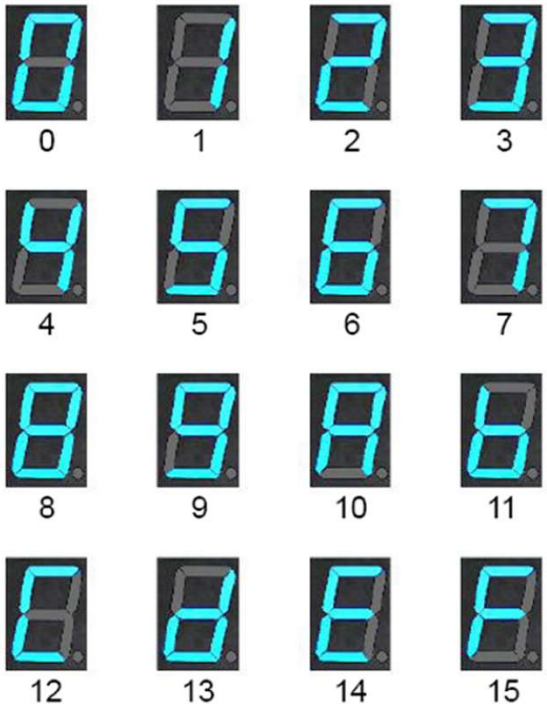
- 快速地將row控制訊號的每個bit輪流設為0
- 根據目前要顯示的row來判斷column訊號的哪些bits要設為0
- 藉由視覺暫留，達到一次顯示8列的視覺效果



Clock must be as 10000 Hz for display !!!

複習 - **Lab Review**





- 0 is on, 1 is off
- dp is useless in DE0-CV board
- Ex:  out=7'b1000000;
  g=1
- Ex:  out=7'b0010010;
  b=1, e=1

複習 - Lab Review

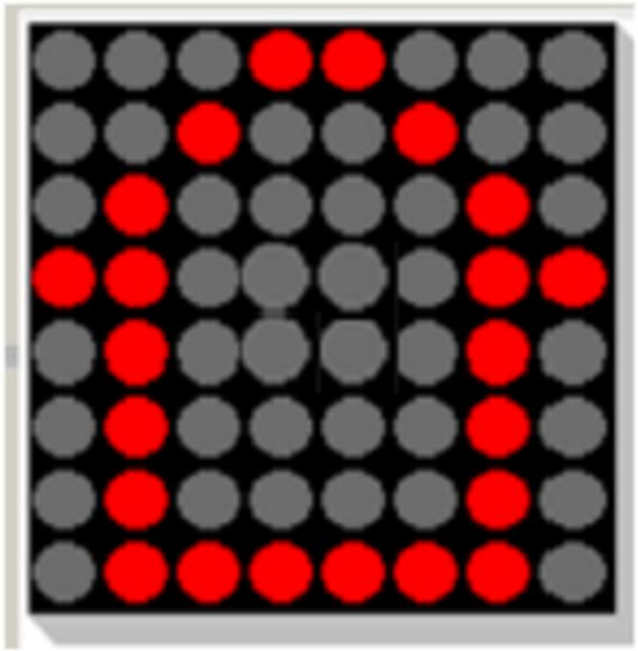
- Assign out to seven segment digit pin of FPGA
  - Take seven segment digit 0 as example

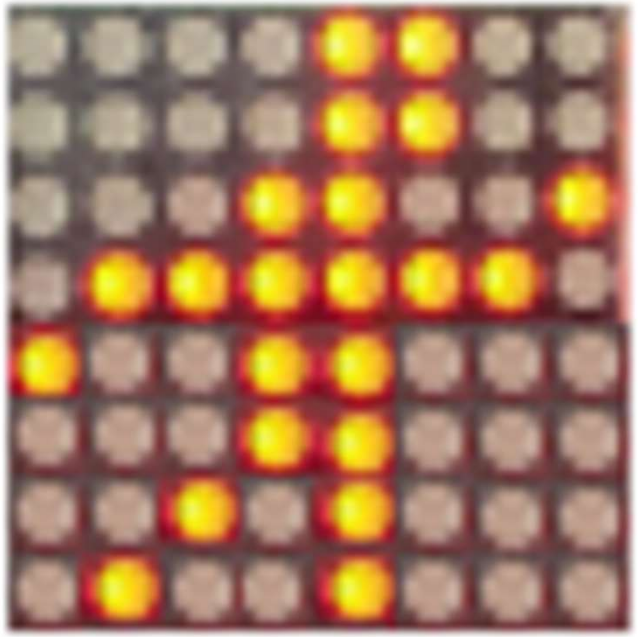
Signal Name	FPGA Pin No.	Description	Signal Assigned	
HEX00	PIN_C14	Seven Segment Digit 0[0]	out[0]	a
HEX01	PIN_E15	Seven Segment Digit 0[1]	out[1]	b
HEX02	PIN_C15	Seven Segment Digit 0[2]	out[2]	c
HEX03	PIN_C16	Seven Segment Digit 0[3]	out[3]	d
HEX04	PIN_E16	Seven Segment Digit 0[4]	out[4]	e
HEX05	PIN_D17	Seven Segment Digit 0[5]	out[5]	f
HEX06	PIN_C17	Seven Segment Digit 0[6]	out[6]	g

Lab 說明 - **Lab Notice**

- 請勿命名中文或數字開頭的資料夾
- Device family 請確認與 FPGA Chip 符合 (10M50DAF484C7G)
- Top module name & Project name 需要一致
- 在組合電路中，case、if…else…若沒有寫滿，合成後會產生latch

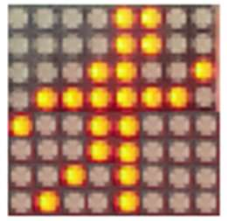
Lab 說明 - **Lab Notice**



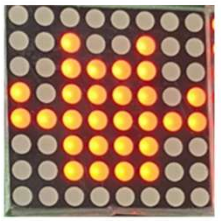


Lab 說明 - **Lab 11 Traffic Light System**

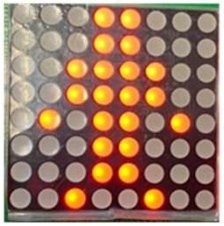
- 請設計一紅綠燈系統電路(變化順序: 綠 -> 黃 -> 紅)
- 電路腳位
  - **Input: clock(MAX10_CLK1_50)、Reset(KEY0)**
  - **Output: dot_row(8 bits)、dot_col(8 bits)、out(7 bits)**
- 使用七段顯示器根據燈號進行倒數(16進制)
  - 綠燈: 10數到0
  - 黃燈: 3數到0
  - 紅燈: 15數到0
- Reset按鈕控制:
  - 將系統設為初始狀態：燈號為綠燈，顯示綠燈圖像，計數器設為10



綠燈



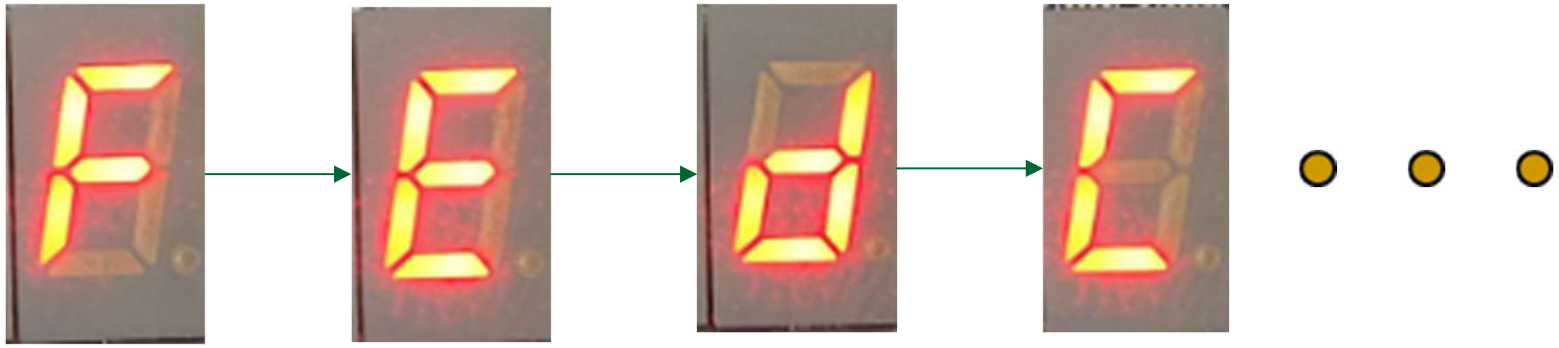
黃燈

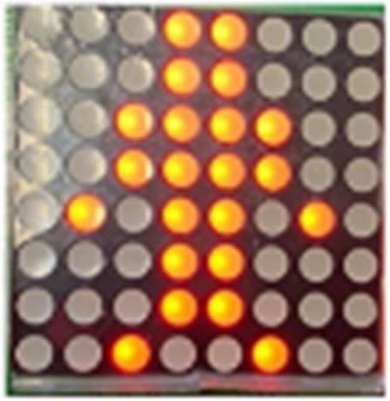


紅燈

Lab 說明 - **Lab 11 Traffic Light System**

七段顯示器 demo





Lab 說明 - Lab 11 Traffic Light System