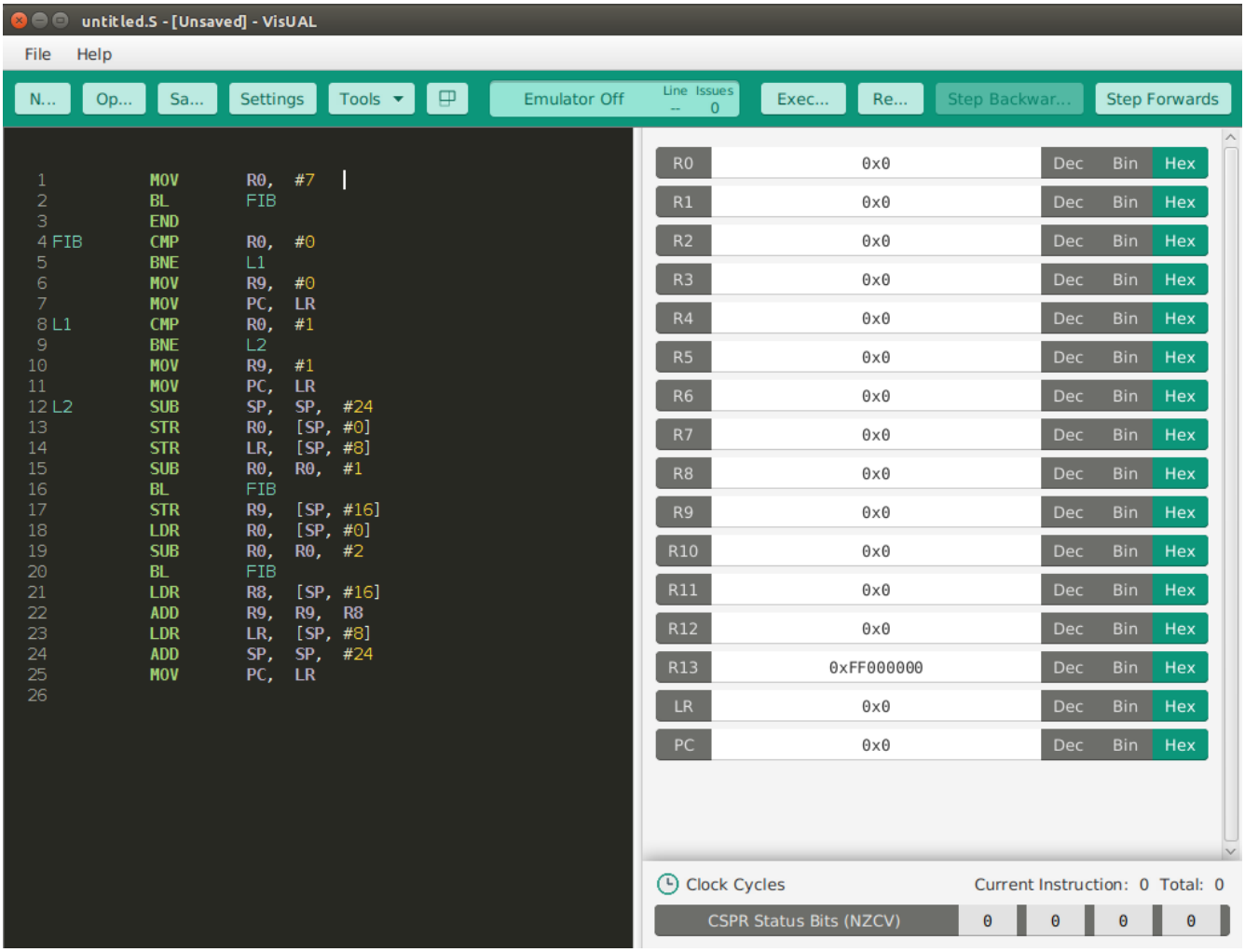
```
FIB:    SUBS    XZR,    X0,     XZR     //COMPARE INPUT WITH 0
        B.NE    L1                      //IF INPUT IS NOT ZERO, GO TO SECOND CHECK
        ADD     X19,    XZR,    XRZ     //PUT 0 IN RETURN VALUE REGISTER
        BR      LR                      //RETURN CONTROL TO CALLER
L1:     SUBIS   XZR,    X0,     #1      //COMPARE INPUT WITH 1
        B.NE    L2                      //IF INPUT IS NOT 1, GO TO THIRD CONDITION
        ADDI    X19,    XZR,    #1      //PUT 1 IN RETURN VALUE REGISTER
        BR      LR                      //RETURN CONTROL TO CALLER
L2:     SUBI    SP,     SP,     #24     //BEFORE PREPARING THE INPUT FOR CHILD
                                         // FUNCTION, PUT OWN COPY OF INPUT, RETURN
                                         //ADDRESS, AND FIRST RETURNED VALUE IN
                                         //STACK
        STUR    X0,     SP,     #0
        STUR    LR,     SP,     #8
        SUBS    X0,     X0,     #1      //NOW, X0 IS HOLDING n-1
        BL      FIB                     //FIRST SELF CALL OF FIBONACHI
        STUR    X19,    SP,     #16     //STORE THE RETURNED VALUE IN STACK
        LDUR    X0,     SP,     #0      //POP ORIGINAL VALUE OF INPUT
        SUBI    X0,     X0,     #2      //NOW, X0 IS HOLDING n-2
        BL      FIB                     //SECOND SELF CALL OF FIBONACHI
        LDUR    X18,    SP,     #16     //POP FIB(N-1)
        ADD     X19,    X19,    X18     //ADD THE TWO FIBONACHIS
        LDUR    LR,     SP,     #8      //POP RETURN ADDRESS
        ADDI    SP,     SP,     #24     //READJUST STACK POINTER
        BR      LR
```

Using visUAL simulator, with the corresponding ISA, and replacing X19 with R9, X18 with R8, you can test that the following works. The first line is the input n.


untitled.S - [Unsaved] - VisUAL
File
Help
N...
Op...
Sa...
Settings
Tools
Emulator Off
Line
--
Issues
0
Exec...
Re...
Step Backwar...
Step Forwards
1 MOV R0, #7
2 BL FIB
3 END
4 FIB CMP R0, #0
5 BNE L1
6 MOV R9, #0
7 MOV PC, LR
8 L1 CMP R0, #1
9 BNE L2
10 MOV R9, #1
11 MOV PC, LR
12 L2 SUB SP, SP, #24
13 STR R0, [SP, #0]
14 STR LR, [SP, #8]
15 SUB R0, R0, #1
16 BL FIB
17 STR R9, [SP, #16]
18 LDR R0, [SP, #0]
19 SUB R0, R0, #2
20 BL FIB
21 LDR R8, [SP, #16]
22 ADD R9, R9, R8
23 LDR LR, [SP, #8]
24 ADD SP, SP, #24
25 MOV PC, LR
26
R0 0x0 Dec Bin Hex
R1 0x0 Dec Bin Hex
R2 0x0 Dec Bin Hex
R3 0x0 Dec Bin Hex
R4 0x0 Dec Bin Hex
R5 0x0 Dec Bin Hex
R6 0x0 Dec Bin Hex
R7 0x0 Dec Bin Hex
R8 0x0 Dec Bin Hex
R9 0x0 Dec Bin Hex
R10 0x0 Dec Bin Hex
R11 0x0 Dec Bin Hex
R12 0x0 Dec Bin Hex
R13 0xFF000000 Dec Bin Hex
LR 0x0 Dec Bin Hex
PC 0x0 Dec Bin Hex
Clock Cycles
Current Instruction: 0 Total: 0
CSPR Status Bits (NZCV)
0
0
0
0