

计算机组成原理实验报告

一、CPU 设计方案综述

总体设计综述

本 CPU 为 Verilog 实现的流水线 CPU，支持指令集包含

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lb, lbu, lh, lhu, lw, sb, sh, sw, add, addu, sub, subu, mult, multu, div, divu, sll, srl, sra, , sllv,
srlv, srav, and, or, xor, nor, addi, addiu, andi, ori, xori, lui, slt, slti, sltiu, sltu, beq, bne,
blez, bgtz, bltz, bgez, j, jal, jalr, jr, mfhi, mflo, mthi, mtlo
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为了实现这些功能，CPU 主要包含了 ALU, Comp, Ctrl, Datapath, DM, Ext, GRF, Hazard, IFU, IM, LoadData, MDU, PC，这些模块并分成 5 级

关键模块定义

IFU

信号名	方向	信号描述
clk	I	时钟信号
reset	I	同步复位信号
stall	I	暂停信号
Branch	I	分支信号
Jump	I	跳转信号
PCBranch[31:0]	I	分支地址
PCJump[31:0]	I	跳转地址
Instr[31:0]	O	输出指令
PC[31:0]	O	输出地址

序号	功能名称	功能描述
1	取指令	根据 PC 地址将指令读出
2	复位	当复位信号有效时，将 PC 设置为 0x00003000
3	暂停	将 PC 暂停，输出指令不变
4	计算下一个 PC	若 Jump 有效，则 PC = JumpAddr 若 Branch 有效，则 PC = BranchAddr 否则，PC = PC + 4

IM

信号名	方向	信号描述
PC[31:0]	I	当前 PC 地址
Instr[31:0]	O	对应地址的指令

PC

信号名	方向	信号描述
clk	I	时钟信号
reset	I	同步复位信号
stall	I	暂停信号
NPC_Sel	I	控制下一个 PC 信号
NPC[31:0]	I	Branch 或 Jump 的 PC 信号
PC[31:0]	O	计算后的 PC

ALU

信号名	方向	信号描述
AluCtrl[3:0]	I	控制运算方式信号
A[31:0]	I	第一运算数
B[31:0]	I	第二运算数
S[4:0]	I	移位数
D[31:0]	O	运算结果数

序号	功能名称	功能描述
1	算术运算	将 A 和 B 进行算术运算
2	按位逻辑运算	将 A 和 B 按位进行逻辑运算
3	移位运算	将 B 按照 S 的移位数进行移位

MDU

信号名	方向	信号描述
clk	I	时钟信号
reset	I	复位信号
start	I	乘除指令信号
MDU_OP[3:0]	I	MDU 操作信号
A[31:0]	I	第一运算数
B[31:0]	I	第二运算数
Busy	O	繁忙信号
Hi[31:0]	O	Hi 寄存器值
Lo[31:0]	O	Lo 寄存器值

序号	功能名称	功能描述
1	复位	当复位信号有效时，将 Hi 和 Lo 清零
2	乘除	若进行乘法运算，高 32 位存入 Hi 寄存器，低 32 位存入 Lo 寄存器 若进行除法运算， $A \bmod B$ 存入 Hi 寄存器， $A \div B$ 存入 Lo 寄存器
3	取数	读取指定寄存器
4	存数	将 A 写入指定寄存器

Ctrl

信号名	方向	信号描述
Instr[31:0]	<i>I</i>	当前指令
RegDst[1:0]	<i>O</i>	选择 rd 、 rt 或 \$31 作为写入目标寄存器
Ext_Op[1:0]	<i>O</i>	控制扩展方式
Branch[2:0]	<i>O</i>	检测条件偏移指令
AluCtrl[3:0]	<i>O</i>	<i>ALU</i> 运算方式
MDU_OP[3:0]	<i>O</i>	<i>MDU</i> 运算方式
AluSrc	<i>O</i>	控制参与运算的数值
RegWrite	<i>O</i>	寄存器堆写入使能
MemToReg	<i>O</i>	控制 DM 数据写入寄存器堆
MemWrite	<i>O</i>	DM 写入使能
Jump	<i>O</i>	检测 J 指令信号
Link	<i>O</i>	将 PC + 4 写入寄存器信号
Return	<i>O</i>	将寄存器的地址写入 PC 信号
start	<i>O</i>	乘除指令信号
ifmfhi	<i>O</i>	mfhi 信号
ifmflo	<i>O</i>	mflo 信号
ifmdu	<i>O</i>	乘除槽信号
Zero	<i>O</i>	比较 0 信号
Tuse_rs[2:0]	<i>O</i>	使用 rs 的最大级数
Tuse_rt[2:0]	<i>O</i>	使用 rt 的最大级数
Tnew[2:0]	<i>O</i>	最新数据产生的级数
LoadType[2:0]	<i>O</i>	控制 Load 指令输出数据信号
MuxData[2:0]	<i>O</i>	<i>E</i> 级数据控制转发数据信号

Instr	RegDst	Ext_Op	Branch	AluCtrl	MDU_OP	AluSrc	RegWrite	MemToReg	Memwrite	Jump	Link	Return	start	ifmfhi	ifmflo	ifmdu	Zero	Tuse_rs	Tuse_rt	Tnew	LoadType
add	rd	x	x	add	x	0	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	<i>E</i>	<i>E</i>	x
addu	rd	x	x	add	x	0	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	<i>E</i>	<i>E</i>	x
and	rd	x	x	and	x	0	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	<i>E</i>	<i>E</i>	x
sub	rd	x	x	sub	x	0	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	<i>E</i>	<i>E</i>	x
subu	rd	x	x	sub	x	0	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	<i>E</i>	<i>E</i>	x
jr	x	x	x	x	x	0	0	0	0	1	0	1	0	0	0	0	0	<i>D</i>	x	x	x
jalr	rd	x	x	x	x	0	1	0	0	1	1	1	0	0	0	0	0	<i>D</i>	x	<i>F</i>	x
or	rd	x	x	or	x	0	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	<i>E</i>	<i>E</i>	x
xor	rd	x	x	xor	x	0	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	<i>E</i>	<i>E</i>	x
nor	rd	x	x	nor	x	0	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	<i>E</i>	<i>E</i>	x
sll	rd	x	x	sll	x	0	1	0	0	0	0	0	0	0	0	0	0	x	<i>E</i>	<i>E</i>	x
srl	rd	x	x	srl	x	0	1	0	0	0	0	0	0	0	0	0	0	x	<i>E</i>	<i>E</i>	x
sra	rd	x	x	sra	x	0	1	0	0	0	0	0	0	0	0	0	0	x	<i>E</i>	<i>E</i>	x
slt	rd	x	x	slt	x	0	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	<i>E</i>	<i>E</i>	x
sltu	rd	x	x	sltu	x	0	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	<i>E</i>	<i>E</i>	x
sllv	rd	x	x	sllv	x	0	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	<i>E</i>	<i>E</i>	x
srlv	rd	x	x	srlv	x	0	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	<i>E</i>	<i>E</i>	x
srav	rd	x	x	srav	x	0	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	<i>E</i>	<i>E</i>	x
mult	x	x	x	x	mult	0	0	0	0	0	0	0	1	0	0	1	0	<i>E</i>	<i>E</i>	x	x
multu	x	x	x	x	multu	0	0	0	0	0	0	0	1	0	0	1	0	<i>E</i>	<i>E</i>	x	x
div	x	x	x	x	div	0	0	0	0	0	0	0	1	0	0	1	0	<i>E</i>	<i>E</i>	x	x
divu	x	x	x	x	divu	0	0	0	0	0	0	0	1	0	0	1	0	<i>E</i>	<i>E</i>	x	x
mthi	x	x	x	x	mthi	0	0	0	0	0	0	0	0	0	0	1	0	<i>E</i>	x	x	x
mtlo	x	x	x	x	mtlo	0	0	0	0	0	0	0	0	0	0	1	0	<i>E</i>	x	x	x
mfhi	rd	x	x	x	x	0	1	0	0	0	0	0	0	1	0	1	0	x	x	<i>E</i>	x
mflo	rd	x	x	x	x	0	1	0	0	0	0	0	0	0	1	1	0	x	x	<i>E</i>	x
addi	rt	sign	x	add	x	1	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	x	<i>E</i>	x
addiu	rt	sign	x	add	x	1	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	x	<i>E</i>	x
andi	rt	zero	x	and	x	1	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	x	<i>E</i>	x
ori	rt	zero	x	or	x	1	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	x	<i>E</i>	x
xori	rt	zero	x	xor	x	1	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	x	<i>E</i>	x
lw	rt	sign	x	add	x	1	1	1	0	0	0	0	0	0	0	0	0	<i>E</i>	x	<i>M</i>	word
lb	rt	sign	x	add	x	1	1	1	0	0	0	0	0	0	0	0	0	<i>E</i>	x	<i>M</i>	sign_byte
lbu	rt	sign	x	add	x	1	1	1	0	0	0	0	0	0	0	0	0	<i>E</i>	x	<i>M</i>	byte
lh	rt	sign	x	add	x	1	1	1	0	0	0	0	0	0	0	0	0	<i>E</i>	x	<i>M</i>	sign_half
lhu	rt	sign	x	add	x	1	1	1	0	0	0	0	0	0	0	0	0	<i>E</i>	x	<i>M</i>	half
lui	rt	upper	x	add	x	1	1	0	0	0	0	0	0	0	0	0	0	x	x	<i>D</i>	x
sw	x	sign	x	add	x	1	0	0	0	1	0	0	0	0	0	0	0	<i>E</i>	<i>M</i>	x	x
sb	x	sign	x	add	x	1	0	0	0	1	0	0	0	0	0	0	0	<i>E</i>	<i>M</i>	x	x
sh	x	sign	x	add	x	1	0	0	0	1	0	0	0	0	0	0	0	<i>E</i>	<i>M</i>	x	x
j	x	x	x	x	x	0	0	0	0	1	0	0	0	0	0	0	0	x	x	x	x
jal	\$31	x	x	x	x	0	1	0	0	1	1	0	0	0	0	0	0	x	x	<i>F</i>	x
beq	x	sign	010	x	x	0	0	0	0	0	0	0	0	0	0	0	0	<i>D</i>	<i>D</i>	x	x
bne	x	sign	101	x	x	0	0	0	0	0	0	0	0	0	0	0	0	<i>D</i>	<i>D</i>	x	x
slti	rt	sign	x	slt	x	1	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	x	<i>E</i>	x
sltiu	rt	sign	x	sltu	x	1	1	0	0	0	0	0	0	0	0	0	0	<i>E</i>	x	<i>E</i>	x
bgez	x	sign	110	x	x	0	0	0	0	0	0	0	0	0	0	0	1	<i>D</i>	x	x	x
bgtz	x	sign	100	x	x	0	0	0	0	0	0	0	0	0	0	0	1	<i>D</i>	x	x	x
blez	x	sign	011	x	x	0	0	0	0	0	0	0	0	0	0	0	1	<i>D</i>	x	x	x
bltz	x	sign	001	x	x	0	0	0	0	0	0	0	0	0	0	0	1	<i>D</i>	x	x	x

Datapath

信号名	方向	信号描述
clk	<i>I</i>	时钟信号
reset	<i>I</i>	同步复位信号
stall_PC	<i>I</i>	PC 暂停信号
stall_FD	<i>I</i>	FD 寄存器暂停信号
stall_DE	<i>I</i>	DE 寄存器暂停信号
stall_EM	<i>I</i>	EM 寄存器暂停信号
stall_MW	<i>I</i>	MW 寄存器暂停信号
clr_FD	<i>I</i>	FD 寄存器清空信号
clr_DE	<i>I</i>	DE 寄存器清空信号
clr_EM	<i>I</i>	EM 寄存器清空信号
clr_MW	<i>I</i>	MW 寄存器清空信号
ForwardSel_D1[4:0]	<i>I</i>	D 级 RD1 转发信号
ForwardSel_D2[4:0]	<i>I</i>	D 级 RD2 转发信号
ForwardSel_EA[4:0]	<i>I</i>	E 级 A 转发信号
ForwardSel_EB[4:0]	<i>I</i>	E 级 B 转发信号
ForwardSel_MD[4:0]	<i>I</i>	M 级写入数据转发信号
Branch_D[2:0]	<i>I</i>	D 级 Branch 判断信号
ExtCtrl_D[1:0]	<i>I</i>	D 级扩展控制信号
RegDst[1:0]	<i>I</i>	D 级 A3 控制信号
Jump_D	<i>I</i>	D 级跳转信号
Return_D	<i>I</i>	D 级跳转寄存器信号
RegWrite_D	<i>I</i>	D 级写入使能信号
AluCtrl_E[3:0]	<i>I</i>	E 级 ALU 控制运算信号
MDU_OP_E[3:0]	<i>I</i>	E 级乘除槽控制运算信号
AluSrc_E	<i>I</i>	E 级控制运算数据信号
ifmfhi_E	<i>I</i>	E 级 mfhi 信号
ifmflo_E	<i>I</i>	E 级 mflo 信号
start_E	<i>I</i>	E 级乘除信号
MemWrite_M	<i>I</i>	M 级 DM 写入使能信号
StoreType_M[1:0]	<i>I</i>	M 级控制写入数据类型信号
MuxData_M[2:0]	<i>I</i>	M 级控制转发数据信号
MemToReg_W	<i>I</i>	W 级控制写入 DM 数据信号
Link_W	<i>I</i>	W 级写入 PC + 8 信号
RegWrite_W	<i>I</i>	W 级 GRF 写入使能信号
ifmfhi_W	<i>I</i>	W 级 mfhi 信号
ifmflo_W	<i>I</i>	W 级 mflo 信号
Instr_D[31:0]	<i>O</i>	D 级指令
Instr_E[31:0]	<i>O</i>	E 级指令
Instr_M[31:0]	<i>O</i>	M 级指令
Instr_W[31:0]	<i>O</i>	W 级指令
Pcplus4_D[31:0]	<i>O</i>	D 级 Pcplus4 信号
Pcplus4_E[31:0]	<i>O</i>	E 级 Pcplus4 信号
Pcplus4_M[31:0]	<i>O</i>	M 级 Pcplus4 信号
Pcplus4_W[31:0]	<i>O</i>	W 级 Pcplus4 信号

信号名	方向	信号描述
PCplus8_D[31:0]	<i>O</i>	<i>D</i> 级 PCplus 8 信号
PCplus8_E[31:0]	<i>O</i>	<i>E</i> 级 PCplus 8 信号
PCplus8_M[31:0]	<i>O</i>	<i>M</i> 级 PCplus 8 信号
PCplus8_W[31:0]	<i>O</i>	<i>W</i> 级 PCplus 8 信号
A3_E[4:0]	<i>O</i>	<i>E</i> 级 A3 地址
A3_M[4:0]	<i>O</i>	<i>M</i> 级 A3 地址
A3_W[4:0]	<i>O</i>	<i>W</i> 级 A3 地址
Busy_E	<i>O</i>	<i>E</i> 级乘除槽繁忙信号

DM

信号名	方向	信号描述
clk	I	时钟信号
reset	I	同步复位信号
MemWrite	I	写入使能信号
Addr[31:0]	I	数据存储器地址
writeData[31:0]	I	写入数据
PC[31:0]	I	当前 PC 地址
StoreType[1:0]	I	数据类型信号
DMOut[31:0]	O	对应输出数据

序号	功能名称	功能描述
1	复位	当 reset 信号有效则将 DM 数据清零
2	写数据	当 MemWrite 有效且时钟上升沿时，将 writeData 数据写入指定地址
3	读数据	从 Addr 读出数据

LoadData

信号名	方向	信号描述
LoadType[2:0]	I	控制数据类型信号
DataIn[31:0]	I	原始数据
Offset[1:0]	I	偏移量
DataOut[31:0]	O	根据类型定义后的数据

序号	功能名称	功能描述
1	转换数据	将数据转换成应有的数据类型

Ext

信号名	方向	信号描述
ExtCtrl[1:0]	I	控制扩展方式信号
imm16[15:0]	I	16 位立即数
imm[31:0]	O	扩展后的立即数

序号	功能名称	功能描述
1	扩展	按照 ExtCtrl 信号指定扩展数据和方式

GRF

信号名	方向	信号描述
clk	I	时钟信号
reset	I	同步复位信号
Regwrite	I	写入使能信号
A1[4:0]	I	指定 32 个寄存器中的一个，输出其中数据到 RD1
A2[4:0]	I	指定 32 个寄存器中的一个，输出其中数据到 RD2
A3[4:0]	I	指定 32 个寄存器中的一个，写入 writeData 数据
writeData[31:0]	I	输入数据
PC[31:0]	I	PC 地址
RD1[31:0]	O	A1 指定寄存器中的数据
RD2[31:0]	O	A2 指定寄存器中的数据

序号	功能名称	功能描述
1	复位	当复位信号有效时，寄存器清零
2	写数据	读出 A1,A2 的寄存器数据到 RD1,RD2
3	读数据	当 Regwrite 有效时且时钟上升沿时，将 writeData 写入指定寄存器内

Hazard

信号名	方向	信号描述
Instr_D[31:0]	I	D 级指令信号
Tuse_rs_D[2:0]	I	D 级 rs 使用数据信号
Tuse_rt_D[2:0]	I	D 级 rt 使用数据信号
ifmdu_D	I	D 级乘除槽指令
Instr_E[31:0]	I	E 级指令信号
Tnew_E[2:0]	I	E 级数据完成信号
A3_E[4:0]	I	E 级 A3 地址
start_E	I	E 级触发乘除槽信号
Busy_E	I	E 级乘除槽繁忙信号
Instr_M[31:0]	I	M 级指令信号
Tnew_M[2:0]	I	M 级数据完成信号
A3_M[4:0]	I	M 级 A3 地址
Instr_W[31:0]	I	W 级指令信号
Tnew_W[2:0]	I	W 级数据完成信号
A3_W[4:0]	I	W 级 A3 地址
ForwardSel_D1[4:0]	O	D 级 RD1 转发信号
ForwardSel_D2[4:0]	O	D 级 RD2 转发信号
ForwardSel_EA[4:0]	O	E 级 A 转发信号
ForwardSel_EB[4:0]	O	E 级 B 转发信号
ForwardSel_MD[4:0]	O	M 级 DM 写入数据转发信号
stall_PC	O	暂停 PC 信号
stall_FD	O	暂停 FD 寄存器信号
stall_DE	O	暂停 DE 寄存器信号
stall_EM	O	暂停 EM 寄存器信号
stall_MW	O	暂停 MW 寄存器信号
clr_FD	O	清除 FD 寄存器信号
clr_DE	O	清除 DE 寄存器信号
clr_EM	O	清除 EM 寄存器信号
clr_MW	O	清除 MW 寄存器信号

Forward

信号名	方向	信号描述
ForwardSel_D1[4:0]	I	D 级 RD1 转发信号
ForwardSel_D2[4:0]	I	D 级 RD2 转发信号
ForwardSel_EA[4:0]	I	E 级 A 转发信号
ForwardSel_EB[4:0]	I	E 级 B 转发信号
ForwardSel_MD[4:0]	I	M 级 DM 写入数据转发信号
RD1_D[31:0]	I	D 级 RD1 数据
RD2_D[31:0]	I	D 级 RD2 数据
Pcplus8_E[31:0]	I	E 级 Pcplus8 数据
imm_E[31:0]	I	E 级 imm 数据
RD1_E[31:0]	I	E 级 RD1 数据
RD2_E[31:0]	I	E 级 RD2 数据
MuxData_M[2:0]	I	M 级数据选择信号
Pcplus8_M[31:0]	I	M 级 Pcplus8 数据
imm_M[31:0]	I	M 级 imm 数据
RD2_M[31:0]	I	M 级 RD2 数据
AluOut_M[31:0]	I	M 级 ALU 数据
HI_M[31:0]	I	M 级 HI 数据
LO_M[31:0]	I	M 级 LO 数据
MuxData_w[2:0]	I	W 级数据选择信号
Pcplus8_w[31:0]	I	W 级 Pcplus8 数据
imm_w[31:0]	I	W 级 imm 数据
AluOut_w[31:0]	I	W 级 ALU 数据
DMOut_w[31:0]	I	W 级 DM 数据
HI_w[31:0]	I	W 级 HI 数据
LO_w[31:0]	I	W 级 LO 数据
MF_RD1_D[31:0]	O	D 级 RD1 转发数据
MF_RD2_D[31:0]	O	D 级 RD1 转发数据
MF_A_E[31:0]	O	E 级 A 转发数据
MF_B_E[31:0]	O	E 级 B 转发数据
MF_RD2_M[31:0]	O	M 级 RD2 转发数据

序号	功能名称	功能描述
1	转发	转发前几级的数据

Comp

信号名	方向	信号描述
zero	I	比较零信号
A[31:0]	I	RD1 信号
B[31:0]	I	RD2 信号
Comp_Out[2:0]	O	比较后输出信号

序号	功能名称	功能描述
1	数据比较	若 $A > B$ 则 Comp_Out = 100 若 $A = B$ 则 Comp_Out = 010 若 $A < B$ 则 Comp_Out = 001

重要机制实现方法

- 1. 跳转
利用 Branch 和 Jump 来判断下一个时钟沿写入的 PC 值
- 2. 转发
利用 $Tuse_{rs}$ 或 $Tuse_{rt} \geq$ 当前级数且 $Tnew \leq$ 当前级数，表示数据已经生成，可以直接转发
- 3. 暂停
若 $Tuse_{rs} > Tnew$ ，则将处理器暂停，直到数据生成为止

二、测试方案

典型测试样例

汇编代码

```
lui $t0, 0x7fff
ori $t0, 0xffff
mult $t0, $t0
mfhi $t1
mflo $t2
div $t1, $t2
mfhi $t1
mflo $t2
mthi $t0
mtlo $t0
mfhi $t1
mflo $t2

lui $t0, 0xffff
ori $t0, 0xffff
multu $t0, $t0
mfhi $t1
mflo $t2
divu $t1, $t2
mfhi $t1
mflo $t2
mthi $t0
mtlo $t0
mfhi $t1
mflo $t2

addi $t1, $0, 27
subi $t0, $0, 12
multu $t0, $t1
divu $t1, $t0
mfhi $t2
mflo $t3
mult $t0, $t1
mfhi $t2
mflo $t3
div $t0, $t1
mfhi $t2
mflo $t3
```

机器码

```
3c087fff
3508ffff
01080018
00004810
00005012
012a001a
00004810
00005012
01000011
01000013
00004810
00005012
3c08ffff
3508ffff
01080019
00004810
00005012
012a001b
00004810
00005012
01000011
01000013
00004810
00005012
2009001b
2001000c
00014022
01090019
0128001b
00005010
00005812
01090018
00005010
00005812
0109001a
00005010
```

00005812

期望结果

```
@00003000: $ 8 <= 7fff0000
@00003004: $ 8 <= 7fffffff
@0000300c: $ 9 <= 3fffffff
@00003010: $10 <= 00000001
@00003018: $ 9 <= 00000000
@0000301c: $10 <= 3fffffff
@00003028: $ 9 <= 7fffffff
@0000302c: $10 <= 7fffffff
@00003030: $ 8 <= ffff0000
@00003034: $ 8 <= ffffffff
@0000303c: $ 9 <= ffffffff
@00003040: $10 <= 00000001
@00003048: $ 9 <= 00000000
@0000304c: $10 <= ffffffff
@00003058: $ 9 <= ffffffff
@0000305c: $10 <= ffffffff
@00003060: $ 9 <= 0000001b
@00003064: $ 1 <= 0000000c
@00003068: $ 8 <= ffffffff4
@00003074: $10 <= 0000001b
@00003078: $11 <= 00000000
@00003080: $10 <= ffffffff
@00003084: $11 <= fffffebc
@0000308c: $10 <= ffffffff4
@00003090: $11 <= 00000000
```

汇编代码

```
li $t0, 0
li $s0, 256
for:
    beq $t0, $s0, for_end
    nop
    add $t0, $0, $t0
    sb $t0, ($t0)
    add $t0, $0, $t0
    j for
    addi $t0, $t0, 1
for_end:
add $t0, $0, $0
lb $a0, 0($t0)
lb $t1, 1($t0)
add $t0, $t1, $a0
lb $a0, 0($t0)
lb $t1, 1($t0)
add $t0, $t1, $a0
lb $a0, 0($t0)
lb $t1, 1($t0)
add $t0, $t1, $a0
lb $a0, 0($t0)
lb $t1, 1($t0)
add $t0, $t1, $a0
lb $a0, 0($t0)
lb $t1, 1($t0)
add $t0, $t1, $a0
lb $a0, 0($t0)
lb $t1, 1($t0)
add $t0, $t1, $a0
lb $a0, 0($t0)
lb $t1, 1($t0)
add $t0, $t1, $a0
```

机器码

```
24080000
24100100
11100006
00000000
00084020
a1080000
00084020
08000c02
21080001
00004020
81040000
81090001
01244020
81040000
81090001
01244020
81040000
81090001
01244020
81040000
81090001
01244020
81040000
81090001
01244020
81040000
81090001
01244020
81040000
81090001
01244020
```

期望结果

```
@00003000: $ 8 <= 00000000
@00003004: $16 <= 00000100
@00003010: $ 8 <= 00000000
@00003014: *00000000 <= 00000000
@00003018: $ 8 <= 00000000
@00003020: $ 8 <= 00000001
@00003010: $ 8 <= 00000001
@00003014: *00000000 <= 00000100
@00003018: $ 8 <= 00000001
@00003020: $ 8 <= 00000002
@00003010: $ 8 <= 00000002
@00003014: *00000000 <= 00020100
@00003018: $ 8 <= 00000002
@00003020: $ 8 <= 00000003
@00003010: $ 8 <= 00000003
@00003014: *00000000 <= 03020100
@00003018: $ 8 <= 00000003
```

@00003020: \$ 8 <= 00000004
@00003010: \$ 8 <= 00000004
@00003014: *00000004 <= 00000004
@00003018: \$ 8 <= 00000004
@00003020: \$ 8 <= 00000005
@00003010: \$ 8 <= 00000005
@00003014: *00000004 <= 00000504
@00003018: \$ 8 <= 00000005
@00003020: \$ 8 <= 00000006
@00003010: \$ 8 <= 00000006
@00003014: *00000004 <= 00060504
@00003018: \$ 8 <= 00000006
@00003020: \$ 8 <= 00000007
@00003010: \$ 8 <= 00000007
@00003014: *00000004 <= 07060504
@00003018: \$ 8 <= 00000007
@00003020: \$ 8 <= 00000008
@00003010: \$ 8 <= 00000008
@00003014: *00000008 <= 00000008
@00003018: \$ 8 <= 00000008
@00003020: \$ 8 <= 00000009
@00003010: \$ 8 <= 00000009
@00003014: *00000008 <= 00000908
@00003018: \$ 8 <= 00000009
@00003020: \$ 8 <= 0000000a
@00003010: \$ 8 <= 0000000a
@00003014: *00000008 <= 000a0908
@00003018: \$ 8 <= 0000000a
@00003020: \$ 8 <= 0000000b
@00003010: \$ 8 <= 0000000b
@00003014: *00000008 <= 0b0a0908
@00003018: \$ 8 <= 0000000b
@00003020: \$ 8 <= 0000000c
@00003010: \$ 8 <= 0000000c
@00003014: *0000000c <= 0000000c
@00003018: \$ 8 <= 0000000c
@00003020: \$ 8 <= 0000000d
@00003010: \$ 8 <= 0000000d
@00003014: *0000000c <= 00000d0c
@00003018: \$ 8 <= 0000000d
@00003020: \$ 8 <= 0000000e
@00003010: \$ 8 <= 0000000e
@00003014: *0000000c <= 000e0d0c
@00003018: \$ 8 <= 0000000e
@00003020: \$ 8 <= 0000000f
@00003010: \$ 8 <= 0000000f
@00003014: *0000000c <= 0f0e0d0c
@00003018: \$ 8 <= 0000000f
@00003020: \$ 8 <= 00000010
@00003010: \$ 8 <= 00000010
@00003014: *00000010 <= 00000010
@00003018: \$ 8 <= 00000010
@00003020: \$ 8 <= 00000011
@00003010: \$ 8 <= 00000011
@00003014: *00000010 <= 00001110
@00003018: \$ 8 <= 00000011
@00003020: \$ 8 <= 00000012
@00003010: \$ 8 <= 00000012
@00003014: *00000010 <= 00121110
@00003018: \$ 8 <= 00000012
@00003020: \$ 8 <= 00000013
@00003010: \$ 8 <= 00000013
@00003014: *00000010 <= 13121110
@00003018: \$ 8 <= 00000013
@00003020: \$ 8 <= 00000014
@00003010: \$ 8 <= 00000014
@00003014: *00000014 <= 00000014
@00003018: \$ 8 <= 00000014
@00003020: \$ 8 <= 00000015
@00003010: \$ 8 <= 00000015
@00003014: *00000014 <= 00001514
@00003018: \$ 8 <= 00000015
@00003020: \$ 8 <= 00000016
@00003010: \$ 8 <= 00000016
@00003014: *00000014 <= 00161514
@00003018: \$ 8 <= 00000016
@00003020: \$ 8 <= 00000017
@00003010: \$ 8 <= 00000017
@00003014: *00000014 <= 17161514
@00003018: \$ 8 <= 00000017
@00003020: \$ 8 <= 00000018
@00003010: \$ 8 <= 00000018
@00003014: *00000018 <= 00000018
@00003018: \$ 8 <= 00000018
@00003020: \$ 8 <= 00000019

@00003010: \$ 8 <= 00000019
@00003014: *00000018 <= 00001918
@00003018: \$ 8 <= 00000019
@00003020: \$ 8 <= 0000001a
@00003010: \$ 8 <= 0000001a
@00003014: *00000018 <= 001a1918
@00003018: \$ 8 <= 0000001a
@00003020: \$ 8 <= 0000001b
@00003010: \$ 8 <= 0000001b
@00003014: *00000018 <= 1b1a1918
@00003018: \$ 8 <= 0000001b
@00003020: \$ 8 <= 0000001c
@00003010: \$ 8 <= 0000001c
@00003014: *0000001c <= 0000001c
@00003018: \$ 8 <= 0000001c
@00003020: \$ 8 <= 0000001d
@00003010: \$ 8 <= 0000001d
@00003014: *0000001c <= 00001d1c
@00003018: \$ 8 <= 0000001d
@00003020: \$ 8 <= 0000001e
@00003010: \$ 8 <= 0000001e
@00003014: *0000001c <= 001e1d1c
@00003018: \$ 8 <= 0000001e
@00003020: \$ 8 <= 0000001f
@00003010: \$ 8 <= 0000001f
@00003014: *0000001c <= 1f1e1d1c
@00003018: \$ 8 <= 0000001f
@00003020: \$ 8 <= 00000020
@00003010: \$ 8 <= 00000020
@00003014: *00000020 <= 00000020
@00003018: \$ 8 <= 00000020
@00003020: \$ 8 <= 00000021
@00003010: \$ 8 <= 00000021
@00003014: *00000020 <= 00002120
@00003018: \$ 8 <= 00000021
@00003020: \$ 8 <= 00000022
@00003010: \$ 8 <= 00000022
@00003014: *00000020 <= 00222120
@00003018: \$ 8 <= 00000022
@00003020: \$ 8 <= 00000023
@00003010: \$ 8 <= 00000023
@00003014: *00000020 <= 23222120
@00003018: \$ 8 <= 00000023
@00003020: \$ 8 <= 00000024
@00003010: \$ 8 <= 00000024
@00003014: *00000024 <= 00000024
@00003018: \$ 8 <= 00000024
@00003020: \$ 8 <= 00000025
@00003010: \$ 8 <= 00000025
@00003014: *00000024 <= 00002524
@00003018: \$ 8 <= 00000025
@00003020: \$ 8 <= 00000026
@00003010: \$ 8 <= 00000026
@00003014: *00000024 <= 00262524
@00003018: \$ 8 <= 00000026
@00003020: \$ 8 <= 00000027
@00003010: \$ 8 <= 00000027
@00003014: *00000024 <= 27262524
@00003018: \$ 8 <= 00000027
@00003020: \$ 8 <= 00000028
@00003010: \$ 8 <= 00000028
@00003014: *00000028 <= 00000028
@00003018: \$ 8 <= 00000028
@00003020: \$ 8 <= 00000029
@00003010: \$ 8 <= 00000029
@00003014: *00000028 <= 00002928
@00003018: \$ 8 <= 00000029
@00003020: \$ 8 <= 0000002a
@00003010: \$ 8 <= 0000002a
@00003014: *00000028 <= 002a2928
@00003018: \$ 8 <= 0000002a
@00003020: \$ 8 <= 0000002b
@00003010: \$ 8 <= 0000002b
@00003014: *00000028 <= 2b2a2928
@00003018: \$ 8 <= 0000002b
@00003020: \$ 8 <= 0000002c
@00003010: \$ 8 <= 0000002c
@00003014: *0000002c <= 0000002c
@00003018: \$ 8 <= 0000002c
@00003020: \$ 8 <= 0000002d
@00003010: \$ 8 <= 0000002d
@00003014: *0000002c <= 00002d2c
@00003018: \$ 8 <= 0000002d
@00003020: \$ 8 <= 0000002e
@00003010: \$ 8 <= 0000002e

@00003014: *0000002c <= 002e2d2c
@00003018: \$ 8 <= 0000002e
@00003020: \$ 8 <= 0000002f
@00003010: \$ 8 <= 0000002f
@00003014: *0000002c <= 2f2e2d2c
@00003018: \$ 8 <= 0000002f
@00003020: \$ 8 <= 00000030
@00003010: \$ 8 <= 00000030
@00003014: *00000030 <= 00000030
@00003018: \$ 8 <= 00000030
@00003020: \$ 8 <= 00000031
@00003010: \$ 8 <= 00000031
@00003014: *00000030 <= 00003130
@00003018: \$ 8 <= 00000031
@00003020: \$ 8 <= 00000032
@00003010: \$ 8 <= 00000032
@00003014: *00000030 <= 00323130
@00003018: \$ 8 <= 00000032
@00003020: \$ 8 <= 00000033
@00003010: \$ 8 <= 00000033
@00003014: *00000030 <= 33323130
@00003018: \$ 8 <= 00000033
@00003020: \$ 8 <= 00000034
@00003010: \$ 8 <= 00000034
@00003014: *00000034 <= 00000034
@00003018: \$ 8 <= 00000034
@00003020: \$ 8 <= 00000035
@00003010: \$ 8 <= 00000035
@00003014: *00000034 <= 00003534
@00003018: \$ 8 <= 00000035
@00003020: \$ 8 <= 00000036
@00003010: \$ 8 <= 00000036
@00003014: *00000034 <= 00363534
@00003018: \$ 8 <= 00000036
@00003020: \$ 8 <= 00000037
@00003010: \$ 8 <= 00000037
@00003014: *00000034 <= 37363534
@00003018: \$ 8 <= 00000037
@00003020: \$ 8 <= 00000038
@00003010: \$ 8 <= 00000038
@00003014: *00000038 <= 00000038
@00003018: \$ 8 <= 00000038
@00003020: \$ 8 <= 00000039
@00003010: \$ 8 <= 00000039
@00003014: *00000038 <= 00003938
@00003018: \$ 8 <= 00000039
@00003020: \$ 8 <= 0000003a
@00003010: \$ 8 <= 0000003a
@00003014: *00000038 <= 003a3938
@00003018: \$ 8 <= 0000003a
@00003020: \$ 8 <= 0000003b
@00003010: \$ 8 <= 0000003b
@00003014: *00000038 <= 3b3a3938
@00003018: \$ 8 <= 0000003b
@00003020: \$ 8 <= 0000003c
@00003010: \$ 8 <= 0000003c
@00003014: *0000003c <= 0000003c
@00003018: \$ 8 <= 0000003c
@00003020: \$ 8 <= 0000003d
@00003010: \$ 8 <= 0000003d
@00003014: *0000003c <= 00003d3c
@00003018: \$ 8 <= 0000003d
@00003020: \$ 8 <= 0000003e
@00003010: \$ 8 <= 0000003e
@00003014: *0000003c <= 003e3d3c
@00003018: \$ 8 <= 0000003e
@00003020: \$ 8 <= 0000003f
@00003010: \$ 8 <= 0000003f
@00003014: *0000003c <= 3f3e3d3c
@00003018: \$ 8 <= 0000003f
@00003020: \$ 8 <= 00000040
@00003010: \$ 8 <= 00000040
@00003014: *00000040 <= 00000040
@00003018: \$ 8 <= 00000040
@00003020: \$ 8 <= 00000041
@00003010: \$ 8 <= 00000041
@00003014: *00000040 <= 00004140
@00003018: \$ 8 <= 00000041
@00003020: \$ 8 <= 00000042
@00003010: \$ 8 <= 00000042
@00003014: *00000040 <= 00424140
@00003018: \$ 8 <= 00000042
@00003020: \$ 8 <= 00000043
@00003010: \$ 8 <= 00000043
@00003014: *00000040 <= 43424140

@00003018: \$ 8 <= 00000043
@00003020: \$ 8 <= 00000044
@00003010: \$ 8 <= 00000044
@00003014: *00000044 <= 00000044
@00003018: \$ 8 <= 00000044
@00003020: \$ 8 <= 00000045
@00003010: \$ 8 <= 00000045
@00003014: *00000044 <= 00004544
@00003018: \$ 8 <= 00000045
@00003020: \$ 8 <= 00000046
@00003010: \$ 8 <= 00000046
@00003014: *00000044 <= 00464544
@00003018: \$ 8 <= 00000046
@00003020: \$ 8 <= 00000047
@00003010: \$ 8 <= 00000047
@00003014: *00000044 <= 47464544
@00003018: \$ 8 <= 00000047
@00003020: \$ 8 <= 00000048
@00003010: \$ 8 <= 00000048
@00003014: *00000048 <= 00000048
@00003018: \$ 8 <= 00000048
@00003020: \$ 8 <= 00000049
@00003010: \$ 8 <= 00000049
@00003014: *00000048 <= 00004948
@00003018: \$ 8 <= 00000049
@00003020: \$ 8 <= 0000004a
@00003010: \$ 8 <= 0000004a
@00003014: *00000048 <= 004a4948
@00003018: \$ 8 <= 0000004a
@00003020: \$ 8 <= 0000004b
@00003010: \$ 8 <= 0000004b
@00003014: *00000048 <= 4b4a4948
@00003018: \$ 8 <= 0000004b
@00003020: \$ 8 <= 0000004c
@00003010: \$ 8 <= 0000004c
@00003014: *0000004c <= 0000004c
@00003018: \$ 8 <= 0000004c
@00003020: \$ 8 <= 0000004d
@00003010: \$ 8 <= 0000004d
@00003014: *0000004c <= 00004d4c
@00003018: \$ 8 <= 0000004d
@00003020: \$ 8 <= 0000004e
@00003010: \$ 8 <= 0000004e
@00003014: *0000004c <= 004e4d4c
@00003018: \$ 8 <= 0000004e
@00003020: \$ 8 <= 0000004f
@00003010: \$ 8 <= 0000004f
@00003014: *0000004c <= 4f4e4d4c
@00003018: \$ 8 <= 0000004f
@00003020: \$ 8 <= 00000050
@00003010: \$ 8 <= 00000050
@00003014: *00000050 <= 00000050
@00003018: \$ 8 <= 00000050
@00003020: \$ 8 <= 00000051
@00003010: \$ 8 <= 00000051
@00003014: *00000050 <= 00005150
@00003018: \$ 8 <= 00000051
@00003020: \$ 8 <= 00000052
@00003010: \$ 8 <= 00000052
@00003014: *00000050 <= 00525150
@00003018: \$ 8 <= 00000052
@00003020: \$ 8 <= 00000053
@00003010: \$ 8 <= 00000053
@00003014: *00000050 <= 53525150
@00003018: \$ 8 <= 00000053
@00003020: \$ 8 <= 00000054
@00003010: \$ 8 <= 00000054
@00003014: *00000054 <= 00000054
@00003018: \$ 8 <= 00000054
@00003020: \$ 8 <= 00000055
@00003010: \$ 8 <= 00000055
@00003014: *00000054 <= 00005554
@00003018: \$ 8 <= 00000055
@00003020: \$ 8 <= 00000056
@00003010: \$ 8 <= 00000056
@00003014: *00000054 <= 00565554
@00003018: \$ 8 <= 00000056
@00003020: \$ 8 <= 00000057
@00003010: \$ 8 <= 00000057
@00003014: *00000054 <= 57565554
@00003018: \$ 8 <= 00000057
@00003020: \$ 8 <= 00000058
@00003010: \$ 8 <= 00000058
@00003014: *00000058 <= 00000058
@00003018: \$ 8 <= 00000058

@00003020: \$ 8 <= 00000059
@00003010: \$ 8 <= 00000059
@00003014: *00000058 <= 00005958
@00003018: \$ 8 <= 00000059
@00003020: \$ 8 <= 0000005a
@00003010: \$ 8 <= 0000005a
@00003014: *00000058 <= 005a5958
@00003018: \$ 8 <= 0000005a
@00003020: \$ 8 <= 0000005b
@00003010: \$ 8 <= 0000005b
@00003014: *00000058 <= 5b5a5958
@00003018: \$ 8 <= 0000005b
@00003020: \$ 8 <= 0000005c
@00003010: \$ 8 <= 0000005c
@00003014: *0000005c <= 0000005c
@00003018: \$ 8 <= 0000005c
@00003020: \$ 8 <= 0000005d
@00003010: \$ 8 <= 0000005d
@00003014: *0000005c <= 00005d5c
@00003018: \$ 8 <= 0000005d
@00003020: \$ 8 <= 0000005e
@00003010: \$ 8 <= 0000005e
@00003014: *0000005c <= 005e5d5c
@00003018: \$ 8 <= 0000005e
@00003020: \$ 8 <= 0000005f
@00003010: \$ 8 <= 0000005f
@00003014: *0000005c <= 5f5e5d5c
@00003018: \$ 8 <= 0000005f
@00003020: \$ 8 <= 00000060
@00003010: \$ 8 <= 00000060
@00003014: *00000060 <= 00000060
@00003018: \$ 8 <= 00000060
@00003020: \$ 8 <= 00000061
@00003010: \$ 8 <= 00000061
@00003014: *00000060 <= 00006160
@00003018: \$ 8 <= 00000061
@00003020: \$ 8 <= 00000062
@00003010: \$ 8 <= 00000062
@00003014: *00000060 <= 00626160
@00003018: \$ 8 <= 00000062
@00003020: \$ 8 <= 00000063
@00003010: \$ 8 <= 00000063
@00003014: *00000060 <= 63626160
@00003018: \$ 8 <= 00000063
@00003020: \$ 8 <= 00000064
@00003010: \$ 8 <= 00000064
@00003014: *00000064 <= 00000064
@00003018: \$ 8 <= 00000064
@00003020: \$ 8 <= 00000065
@00003010: \$ 8 <= 00000065
@00003014: *00000064 <= 00006564
@00003018: \$ 8 <= 00000065
@00003020: \$ 8 <= 00000066
@00003010: \$ 8 <= 00000066
@00003014: *00000064 <= 00666564
@00003018: \$ 8 <= 00000066
@00003020: \$ 8 <= 00000067
@00003010: \$ 8 <= 00000067
@00003014: *00000064 <= 67666564
@00003018: \$ 8 <= 00000067
@00003020: \$ 8 <= 00000068
@00003010: \$ 8 <= 00000068
@00003014: *00000068 <= 00000068
@00003018: \$ 8 <= 00000068
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@00003018: \$ 8 <= 000000f7
@00003020: \$ 8 <= 000000f8
@00003010: \$ 8 <= 000000f8
@00003014: *000000f8 <= 000000f8
@00003018: \$ 8 <= 000000f8
@00003020: \$ 8 <= 000000f9
@00003010: \$ 8 <= 000000f9
@00003014: *000000f8 <= 0000f9f8
@00003018: \$ 8 <= 000000f9
@00003020: \$ 8 <= 000000fa
@00003010: \$ 8 <= 000000fa
@00003014: *000000f8 <= 00faf9f8
@00003018: \$ 8 <= 000000fa
@00003020: \$ 8 <= 000000fb
@00003010: \$ 8 <= 000000fb
@00003014: *000000f8 <= fbfa9f8
@00003018: \$ 8 <= 000000fb
@00003020: \$ 8 <= 000000fc
@00003010: \$ 8 <= 000000fc
@00003014: *000000fc <= 000000fc
@00003018: \$ 8 <= 000000fc
@00003020: \$ 8 <= 000000fd
@00003010: \$ 8 <= 000000fd
@00003014: *000000fc <= 0000fdfc
@00003018: \$ 8 <= 000000fd
@00003020: \$ 8 <= 000000fe
@00003010: \$ 8 <= 000000fe
@00003014: *000000fc <= 00fefdfc
@00003018: \$ 8 <= 000000fe
@00003020: \$ 8 <= 000000ff
@00003010: \$ 8 <= 000000ff
@00003014: *000000fc <= fffefdfc
@00003018: \$ 8 <= 000000ff
@00003020: \$ 8 <= 00000100
@00003024: \$ 8 <= 00000000
@00003028: \$ 4 <= 00000000
@0000302c: \$ 9 <= 00000001
@00003030: \$ 8 <= 00000001
@00003034: \$ 4 <= 00000001
@00003038: \$ 9 <= 00000002
@0000303c: \$ 8 <= 00000003
@00003040: \$ 4 <= 00000003
@00003044: \$ 9 <= 00000004
@00003048: \$ 8 <= 00000007
@0000304c: \$ 4 <= 00000007

```
@00003050: $ 9 <= 00000008
@00003054: $ 8 <= 0000000f
@00003058: $ 4 <= 0000000f
@0000305c: $ 9 <= 00000010
@00003060: $ 8 <= 0000001f
@00003064: $ 4 <= 0000001f
@00003068: $ 9 <= 00000020
@0000306c: $ 8 <= 0000003f
```

思考题

1. 为什么需要有单独的乘除法部件而不是整合进 *ALU* ? 为何需要有独立的 `HI,LO` 寄存器?

因为 *ALU* 是一个 **32 位** 输出端口, 而乘除法是两个输出端口 `HI,LO`, 再加上乘除操作的延迟比较高, 所以作为独立模块能尽量不减少处理器的效能。

2. 参照你对延迟槽的理解, 试解释“乘除槽”。

与延迟槽相似的地方就是他们俩在 *D* 级检测到乘除指令就会产生 `start` 信号, 并且在下一周期产生 `busy` 信号, 若发生冲突就暂停, 直到 `busy` 信号无效为止, 若不暂停可理解位延迟槽的空指令。

3. 举例说明并分析何时按字节访问内存相对于按字访问内存性能上更有优势。

在 *C* 语言中的字符串处理会更为方便, 如果按字节访问就只需要直接读出一个字节, 若按字访问就需要判断 `offset` 并选择读取哪一个字节, 所以按字节访问相对会快许多。

4. 在本实验中你遇到了哪些不同指令类型组合产生的冲突? 你又是如何解决的? 相应的测试样例是什么样的?

如果你是手动构造的样例, 请说明构造策略, 说明你的测试程序如何保证覆盖了所有需要测试的情况; 如果你是完全随机生成的测试样例, 请思考完全随机的测试程序有何不足之处; 如果你在生成测试样例时采用了特殊的策略, 比如构造连续数据冒险序列, 请你描述一下你使用的策略如何结合了随机性达到强测的效果。

此思考题请同学们结合自己测试 *CPU* 使用的具体手段, 按照自己的实际情况进行回答

在 `lb, lbu, lh, lhu` 转发时遇到了一些问题, 因和 `p5` 不同在于他们转发的数据应为 `LoadType` 的输出数据, 而不是 `DM` 的输出数据, 所以在这里更改了转发端口即可解决。

在乘除槽的冲突指令利用了 `busy | start` 来判断 *D* 级指令该不该暂停, 以下为测试乘除指令暂停机制的测试代码。

```
mult $t0, $t1
mfhi $t0
div $t0, $t1
mthi $t1
multu $t0, $t1
mtlo $t0
divu $t1, $t0
mthi $t1
```

该测试代码将所有的乘除槽指令都集中在一起, 以便让暂停机制和转发机制能集中进行。

5. 为了对抗复杂性你采取了哪些抽象和规范手段? 这些手段在译码和处理数据冲突的时候有什么样的特点与帮助?

除了命名方面的改善, 还利用了 `Excel` 来将各个指令的 *Tuse* 和 *Tnew* 分析了一遍, 再写入程序。先把功能模块需要用的接口接线后, 先把模块放入数据通路, 再实现模块。若模块比较复杂, 可以先测一测模块再进一步搭建 *CPU*。最后就是代码风格, 代码能越简洁就越好, 最好是做到看第一眼就知道这一块是干什么的, 以便 `debug` 和修改代码。