一、填空题

1. 导通，截止
2. 关，高电平，开，低电平
3. 3.0，0.35
4. **ECL,TTL,CMOS，CMOS,TTL,ECL，CMOS,TTL,ECL**
5. $0,1$
6. $\overline{F}=(A+B)(\overline{C}+\overline{D})$ ， $F^{*}=(\overline{A}+\overline{B})(C+D)$
7. $F=A\overline{B}+AC+\overline{C}D$
8. 存储电路，反馈电路，输入信号
9. 编码
10. 译码，n ，2^{n}
11. 1111110111

二、选择题

1. ③
2. ④
3. ②
4. ④
5. ①

$$
\begin{aligned}
F &= AB + \overline{A}C + \overline{B}C + \overline{C}D + \overline{D} \\
&= AB + C(\overline{A} + \overline{B}) + \overline{C}D + \overline{D} \\
&= AB + \overline{AB}C + \overline{C}D + \overline{D} \\
&= AB + \overline{AB}C + \overline{C}D + AB\overline{D} + \overline{AB}\,\overline{D} \\
&= AB(1 + \overline{D}) + \overline{AB}(C + \overline{D}) + \overline{C}D \\
&= AB + \overline{AB}\,\overline{\overline{C}D} + \overline{C}D \\
&= AB + \overline{AB}\,\overline{\overline{C}D} + AB\overline{C}D + \overline{AB}\,\overline{C}D \\
&= AB(1 + \overline{C}D) + \overline{AB}(\overline{C}D + \overline{\overline{C}D}) \\
&= AB + \overline{AB} \\
&= 1
\end{aligned}
$$

6. ②

$$
\begin{gathered}
F = \overline{0 + 1 \cdot \overline{1}(0 + 1)} \\
F = \overline{0 + 0} \cdot 1 \\
F = 1 \cdot 1 = 1
\end{gathered}
$$

7. ③

$$
\begin{gathered}
A \oplus B = A\overline{B} + \overline{A}B \\
\overline{A} \oplus \overline{B} = \overline{A}B + A\overline{B} \\
\therefore A \oplus B = \overline{A} \oplus \overline{B}
\end{gathered}
$$

8. ③
9. ③
10. ②
11. ④

问答与计算题

1.

$$\begin{aligned} ABC+\overline{A}BD &= ABC(D+\overline{D})+\overline{A}BD(C+\overline{C}) \\ &= ABCD+ABC\overline{D}+\overline{A}BCD+\overline{A}B\overline{C}D \\ &= m_5+m_7+m_{14}+m_{15} \end{aligned}$$

2.

$$\begin{aligned} F &= \overline{AB+B\overline{C}}+A\overline{C} \\ &= \overline{AB}\cdot\overline{B\overline{C}}+A\overline{C} \\ &= (\overline{A}+\overline{B})(\overline{B}+\overline{C})+A\overline{C} \\ &= \overline{A}\cdot\overline{B}+\overline{A}\cdot\overline{C}+\overline{B}\cdot\overline{B}+\overline{B}\cdot\overline{C}+A\cdot\overline{C} \\ &= \overline{A}\cdot\overline{B}+\overline{C}(A+\overline{A})+\overline{B}(1+\overline{C}) \\ &= \overline{A}\cdot\overline{B}+\overline{C}+\overline{B} \\ &= \overline{B}(1+\overline{A})+\overline{C} \\ &= \overline{B}+\overline{C} \end{aligned}$$

3. 真值表如下

A	B	C	OUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$OUT = BC + AC + AB + ABC = AB + AC + BC$

Verilog HDL 程序

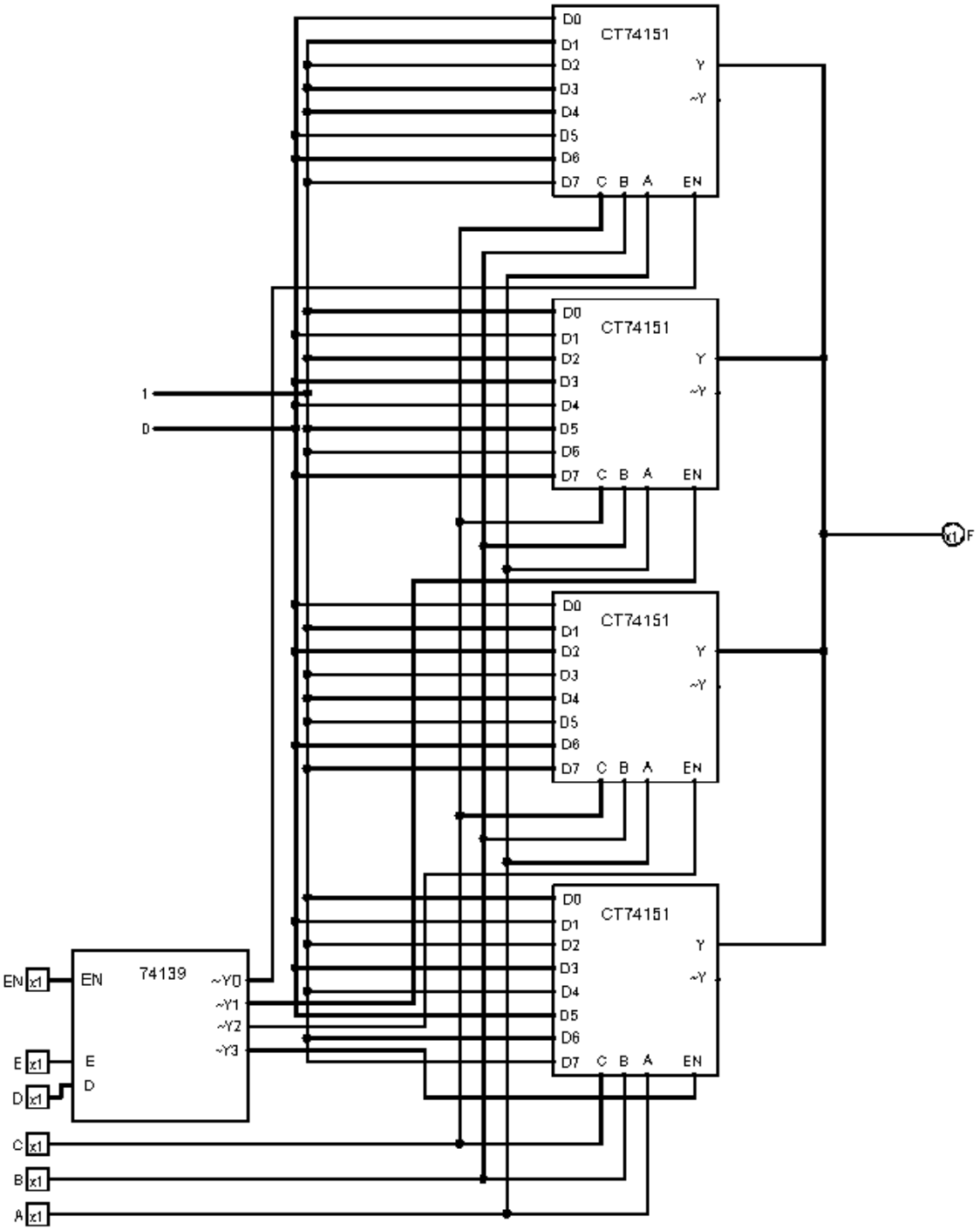
```
module temperature(A,B,C,OUT);
    input A, B, C;
    output OUT;

    assign OUT = A & B | B & C | A & C;

endmodule
```

4.

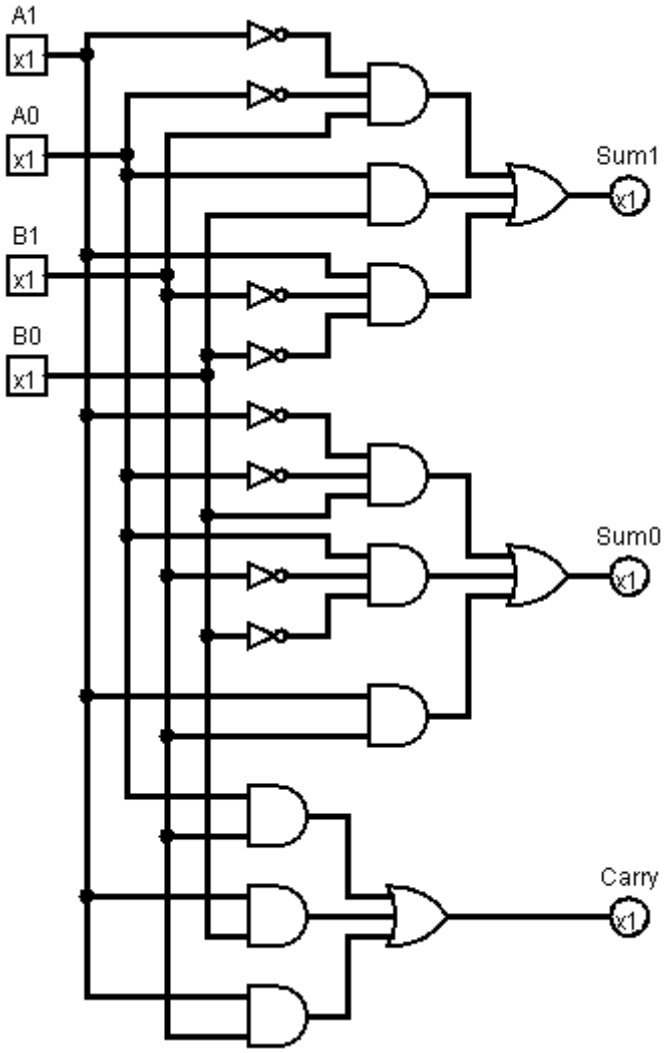
$$
\begin{aligned}
&\overline{B}C\overline{D} + B\overline{C}D + ACD + \overline{A}B\overline{CD} + \overline{AB}CD + B\overline{CD} + BCD \\
\implies &\overline{B}C\overline{D} + B\overline{C}D + \overline{A}B\overline{CD} + (A + \overline{AB})CD + B(\overline{CD} + CD) \\
\implies &\overline{B}C\overline{D} + B\overline{C}D + \overline{A}B\overline{CD} + (A + \overline{A} + \overline{B})CD + B \\
\implies &\overline{B}C\overline{D} + B\overline{C}D + \overline{A}B\overline{CD} + CD + B \\
\implies &C(\overline{BD} + D) + B(1 + \overline{C}D + \overline{A}\overline{CD}) \\
\implies &C(D + \overline{D})(D + \overline{B}) + B \\
\implies &C(D + \overline{B}) + B \\
\implies &CD + C\overline{B} + B \\
\implies &(B + \overline{B})(B + C) + CD \\
\implies &B + C + CD \\
\implies &B + C(1 + D) \\
\implies &B + C
\end{aligned}
$$

5. 利用4个**CT74151**多路选择器和**ABC**让各个多路选择器来按位输出，然后用**2**线**-4**线译码器(74139) 控制多路选择器的输出，就可以完成**32**位的多路选择器了。

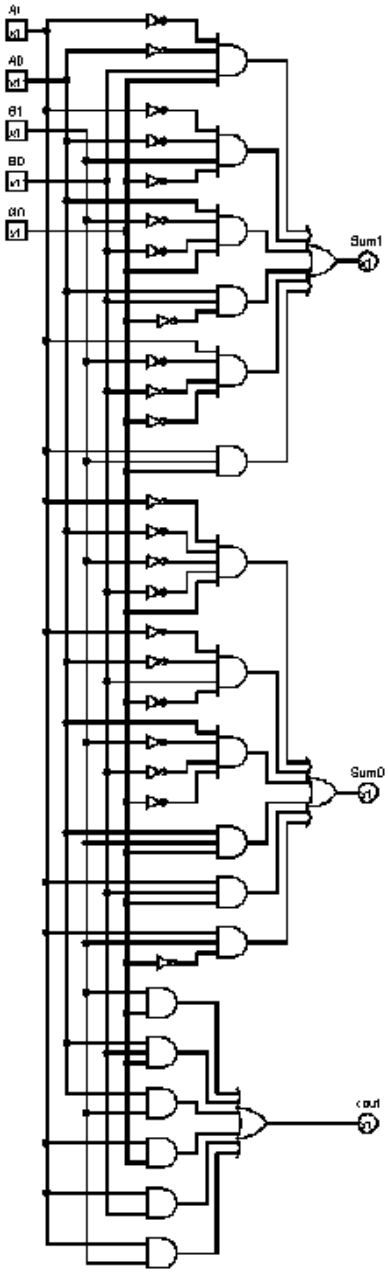
   实现方法如下图



6. **(1)** 三进制半加器



(2) 三进制全加器



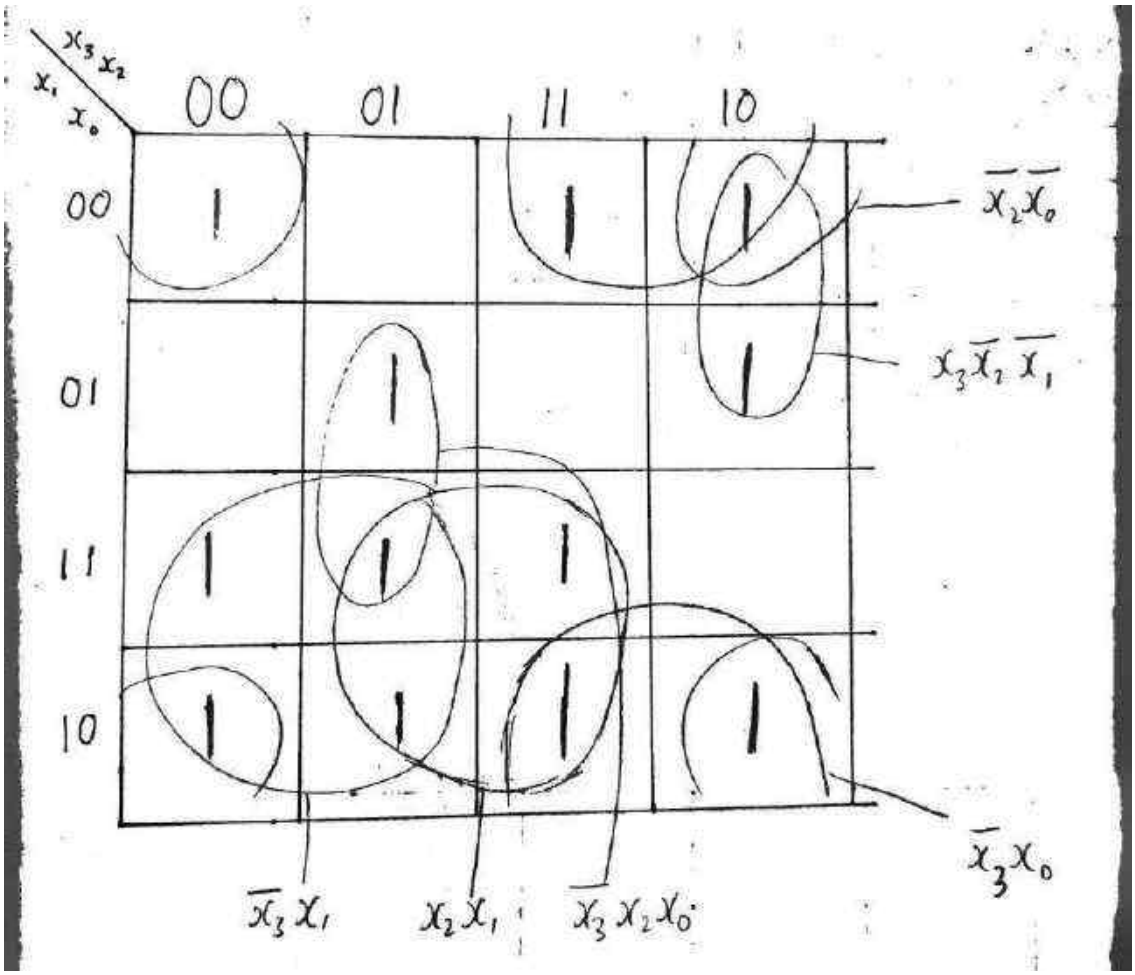
7. **(1)** 真值表如下

x_3	x_2	x_1	x_0	a	b	c	d	e	f	g	**out**
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	0	0	0	1	1	0	1
0	0	1	0	1	0	1	1	0	1	1	2
0	0	1	1	1	0	0	1	1	1	1	3
0	1	0	0	0	1	0	0	1	1	1	4
0	1	0	1	1	1	0	1	1	0	1	5
0	1	1	0	1	1	1	1	1	0	1	6
0	1	1	1	1	0	0	0	1	1	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	0	1	1	1	1	9
1	0	1	0	1	1	1	0	1	1	1	A
1	0	1	1	0	1	1	1	1	0	1	B
1	1	0	0	1	1	1	1	0	0	0	C
1	1	0	1	0	0	1	1	1	1	1	D
1	1	1	0	1	1	1	1	0	0	1	E
1	1	1	1	1	1	1	0	0	0	1	F

(2)

$$a = m_0 + m_2 + m_3 + m_5 + m_6 + m_7 + m_8 + m_9 + m_{10} + m_{12} + m_{14} + m_{15}$$

a的卡诺图

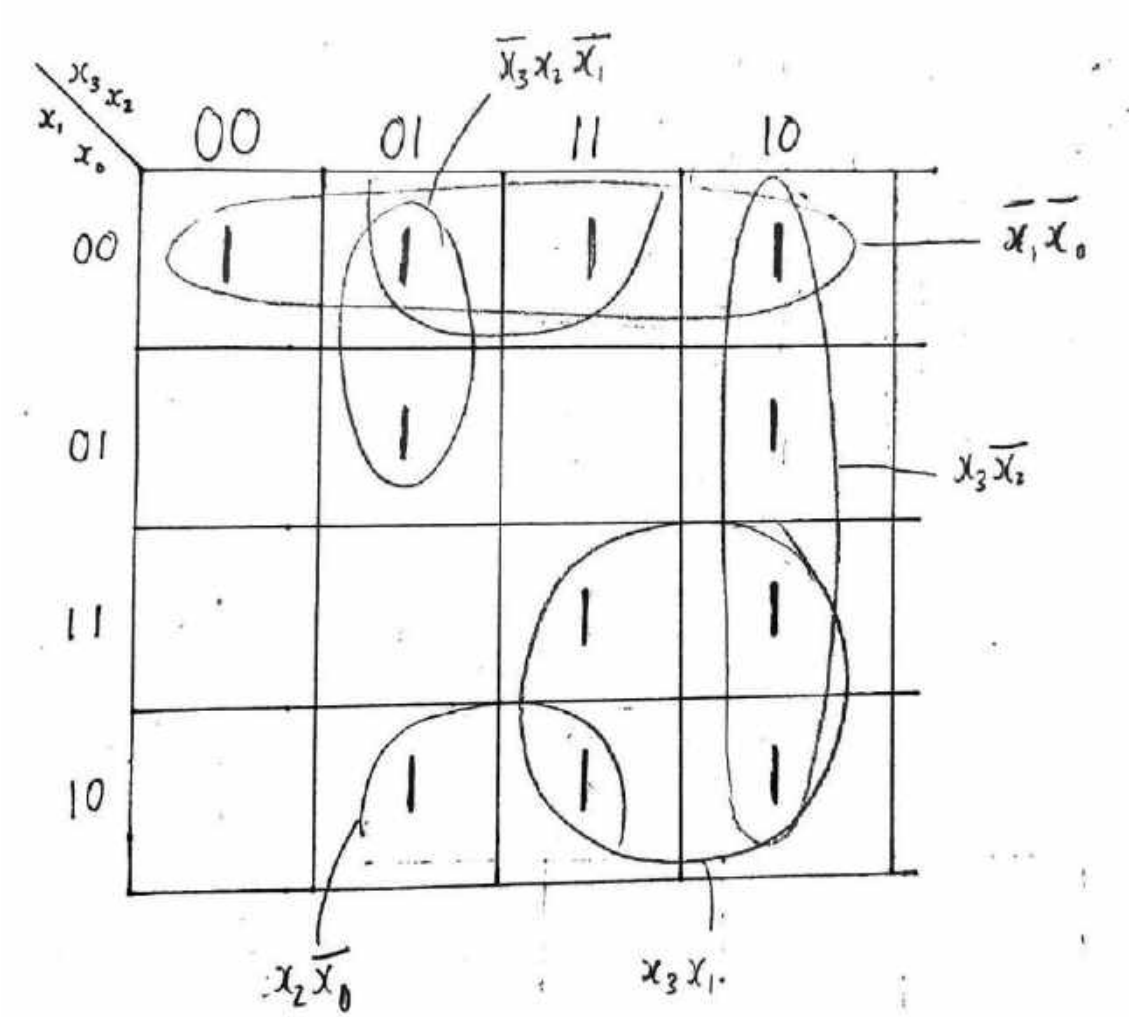


化简得

$$a = \overline{x}_2\overline{x}_0 + \overline{x}_3x_1 + \overline{x}_3x_2x_0 + x_2x_1 + x_3\overline{x}_2\overline{x}_1 + x_3\overline{x}_0$$

$$b = m_0 + m_4 + m_5 + m_6 + m_8 + m_9 + m_{10} + m_{11} + m_{12} + m_{14} + m_{15}$$

b的卡诺图

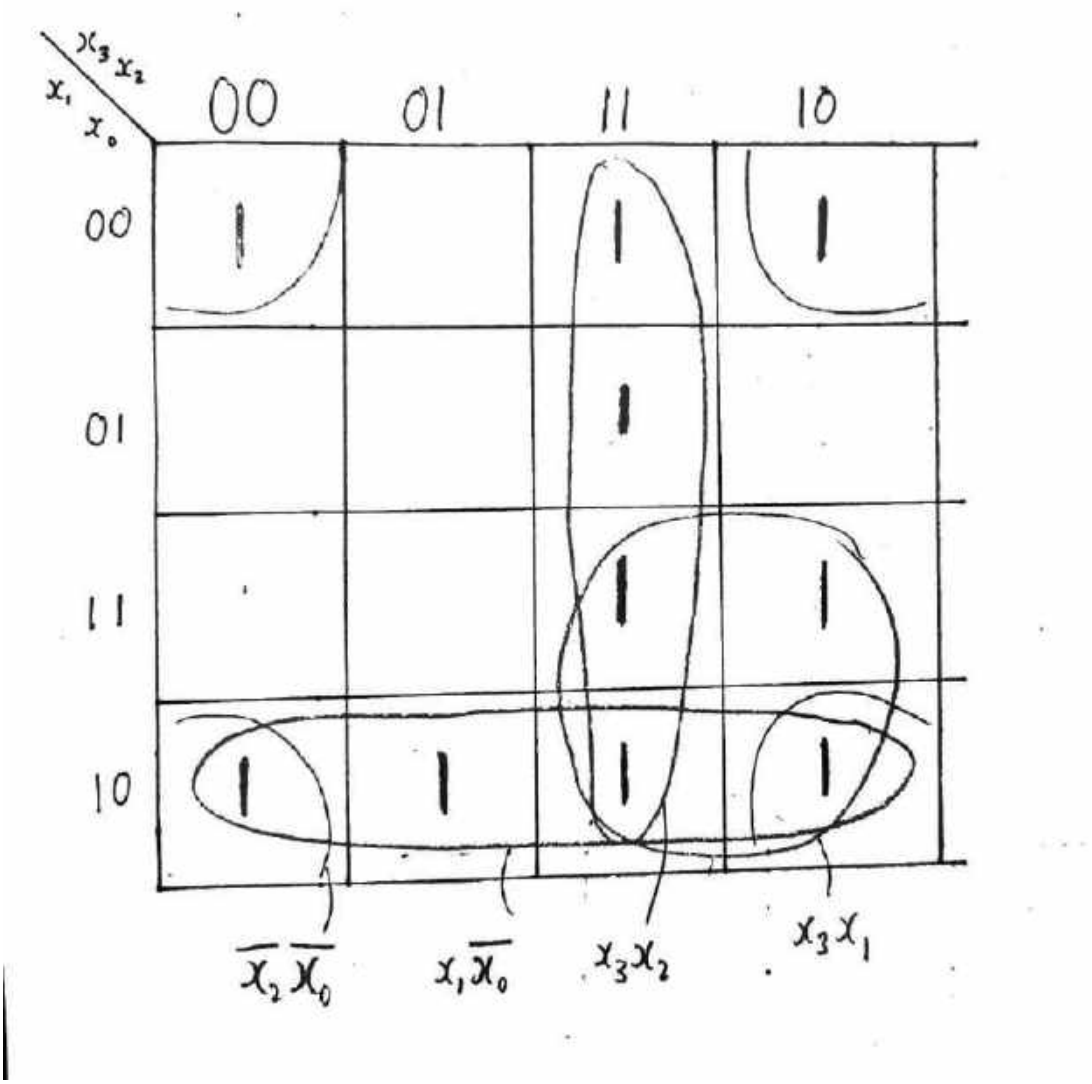


化简得

$$b = \overline{x}_1\overline{x}_0 + \overline{x}_3x_2\overline{x}_1 + x_2\overline{x}_0 + x_3\overline{x}_2 + x_3x_1$$

$$c = m_0 + m_2 + m_6 + m_8 + m_{10} + m_{11} + m_{12} + m_{13} + m_{14} + m_{15}$$

c的卡诺图

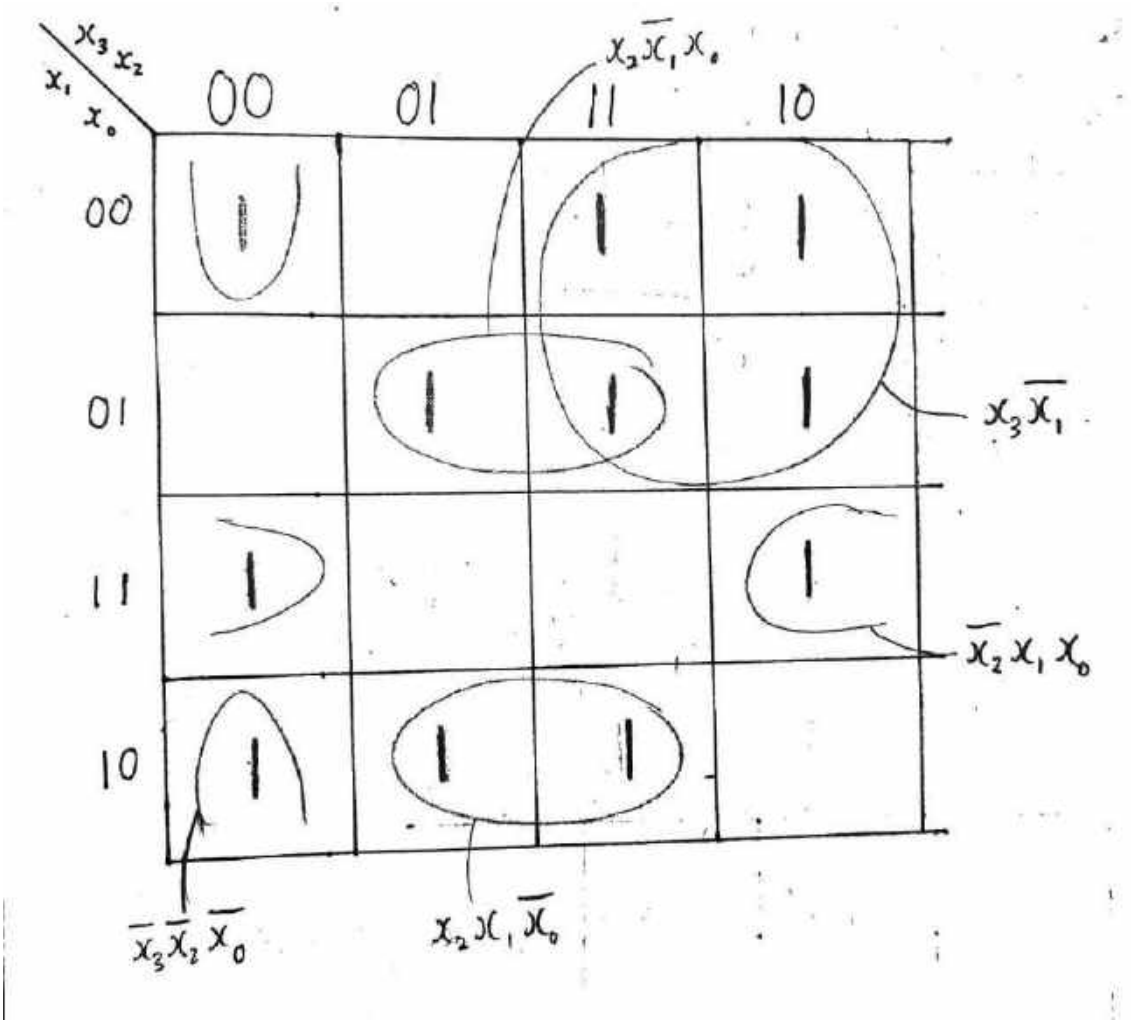


化简得

$$c = \overline{x}_2\overline{x}_0 + x_1\overline{x}_0 + x_3x_1 + x_3x_2$$

$$d = m_0 + m_2 + m_3 + m_5 + m_6 + m_8 + m_9 + m_{11} + m_{12} + m_{13} + m_{14}$$

d的卡诺图

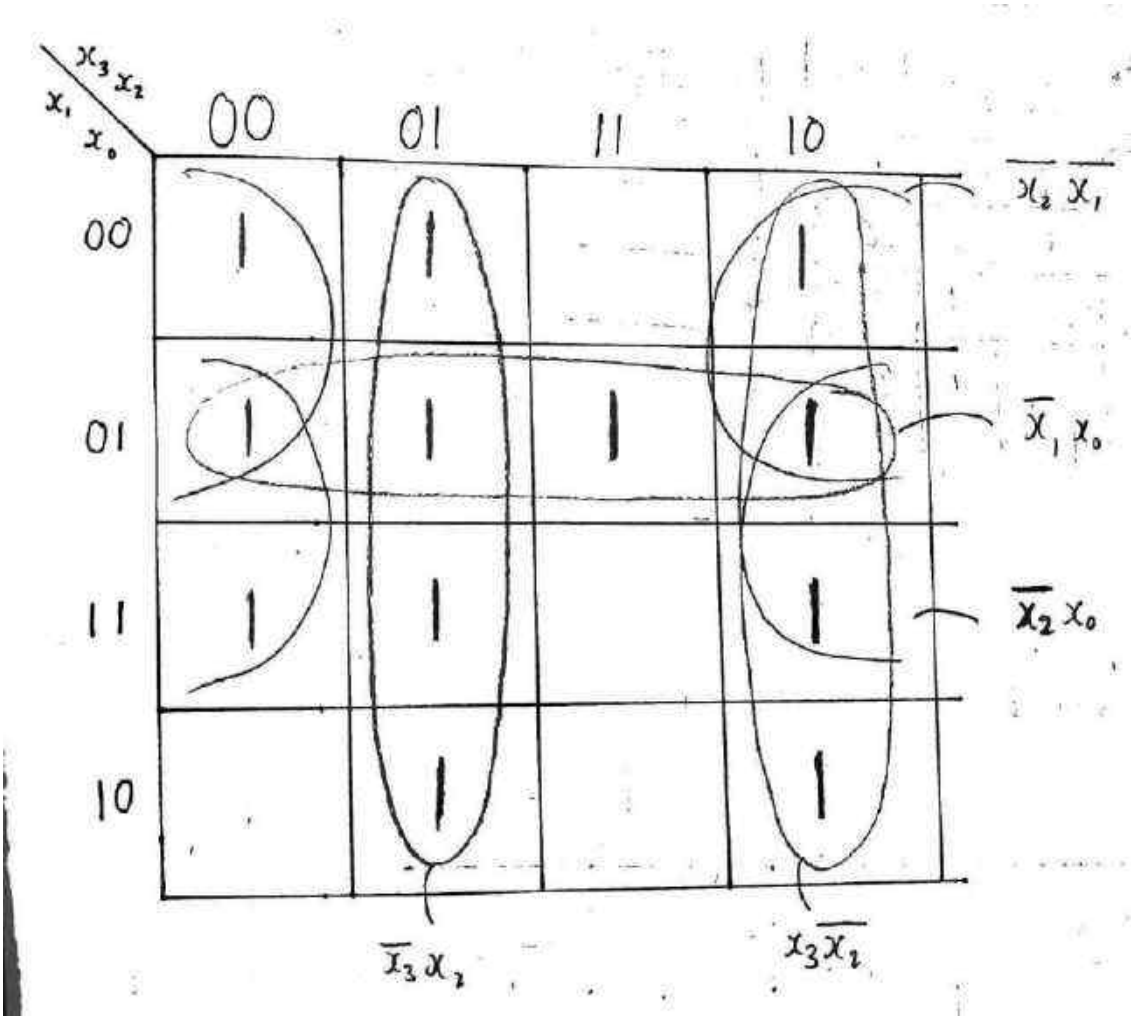


化简得

$$d = \overline{x}_3\overline{x}_2\overline{x}_0 + \overline{x}_2x_1x_0 + x_2\overline{x}_1x_0 + x_2x_1\overline{x}_0 + x_3\overline{x}_1$$

$$e = m_0 + m_1 + m_3 + m_4 + m_5 + m_6 + m_7 + m_8 + m_9 + m_{10} + m_{11} + m_{13}$$

e的卡诺图

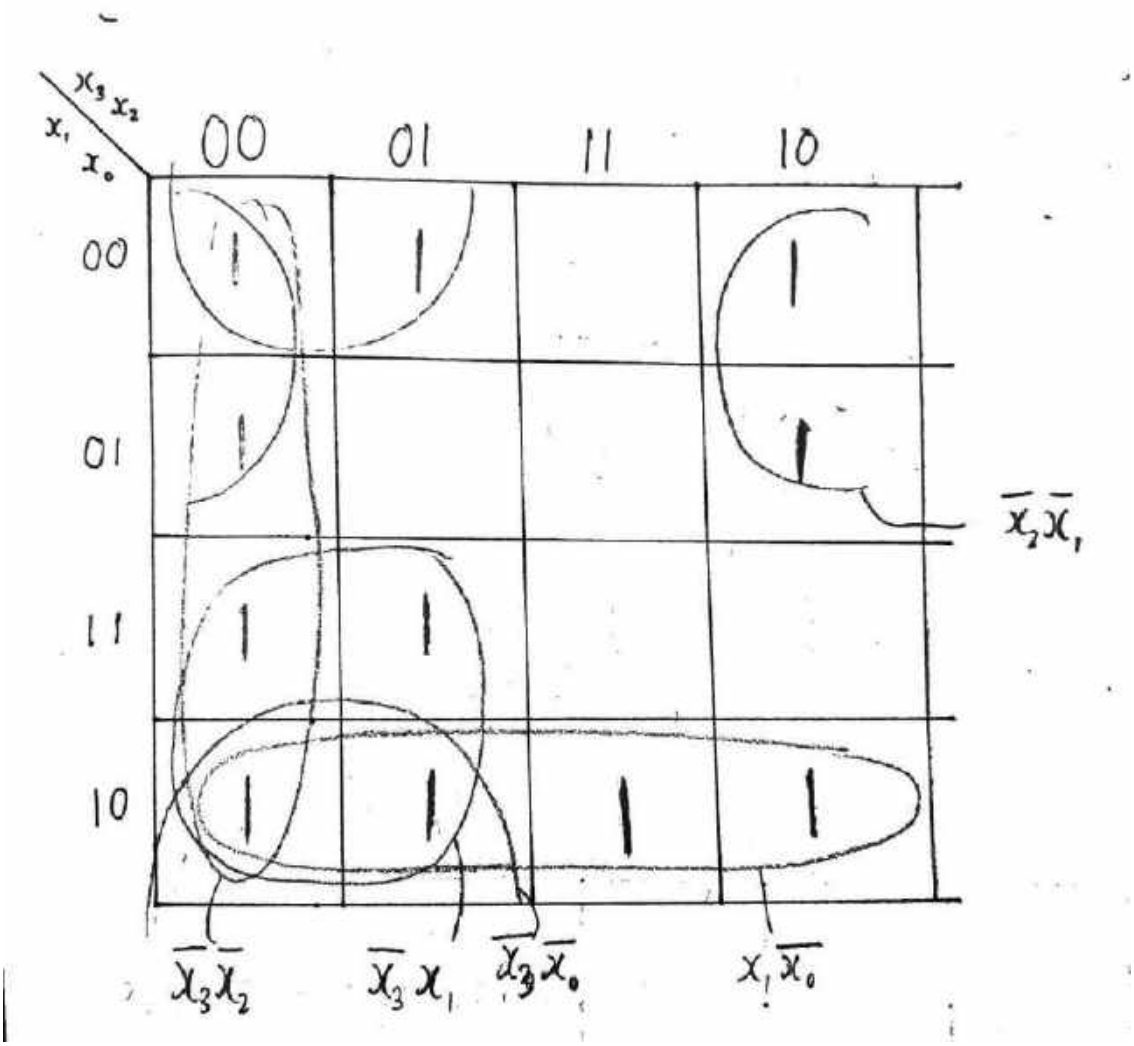


化简得

$$e = \overline{x}_2\overline{x}_1 + \overline{x}_2x_0 + \overline{x}_1x_0 + \overline{x}_3x_2 + x_3\overline{x}_2$$

$$f = m_0 + m_1 + m_2 + m_3 + m_4 + m_5 + m_7 + m_8 + m_9 + m_{10} + m_{13}$$

f的卡诺图

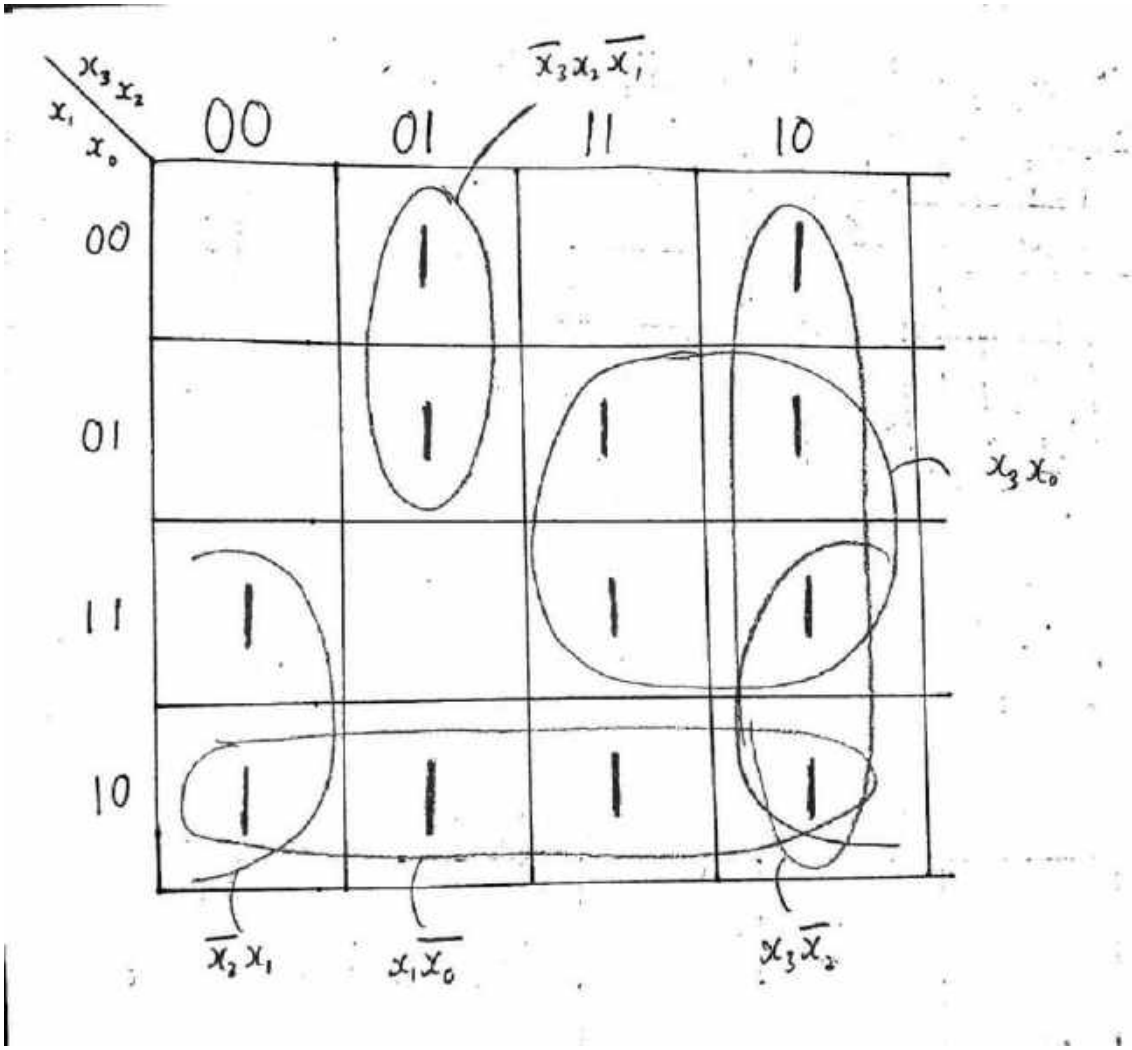


化简得

$$f = \overline{x}_3\overline{x}_2 + \overline{x}_3x_1 + \overline{x}_3\overline{x}_0 + x_1\overline{x}_0 + \overline{x}_2\overline{x}_1$$

$$g = m_2 + m_3 + m_4 + m_5 + m_6 + m_8 + m_9 + m_{10} + m_{11} + m_{13} + m_{14} + m_{15}$$

g的卡诺图



化简得

$$g = \overline{x}_2x_1 + x_1\overline{x}_0 + \overline{x}_3x_2\overline{x}_1 + x_3\overline{x}_2 + x_3x_0$$

(3) Verilog HDL 程序

```
module light(x,a,b,c,d,e,f,g);
    input [3:0] x;
    output a, b, c, d, e, f, g;

    assign a = ~x[2] & ~x[0] | ~x[3] & x[1] | ~x[3] & x[2] & x[0] | x[2] &
x[1] | x[3] & ~x[2] & ~x[1] | x[3] & ~x[0];
    assign b = ~x[1] & ~x[0] | ~x[3] & x[2] & ~x[1] | x[2] & ~x[0] | x[3] &
~x[2] | x[3] & x[1];
    assign c = ~x[2] & ~x[0] |  x[1] & x[0] |  x[3] & x[1] | x[3] & x[2];
    assign d = ~x[3] & ~x[2] & ~x[0] | ~x[2] & x[1] & x[0] | x[2] & ~x[1] &
x[0] | x[2] & ~x[1] & x[0] | x[2] & x[1] & ~x[0] | x[3] & ~x[1];
    assign e = ~x[2] & ~x[1] | ~x[2] & x[0] | ~x[1] & x[0] | ~x[3] & x[2] |
x[3] & ~x[2];
    assign f = ~x[3] & ~x[2] | ~x[3] & x[1] | ~x[3] & ~x[0] | x[1] & ~x[0] |
~x[2] & ~x[1];
    assign g = ~x[2] & x[1] | x[1] & ~x[0] | ~x[3] & x[2] & ~x[1] | x[3] &
~x[2] | x[3] & x[0];

endmodule
```