Please attach this cover sheet to your completed homework

ECE 324 Homework 4: Shift Register Simulation

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Exercise	Course outcome	Grade
Homework4	2.a, 7.b	/30

2.a. Define engineering problems from specified needs for digital systems including implementation on FPGAs using HDL programming.
7.b. Employ appropriate learning strategies such as communicating with an expert, using external resources, experimentation, simulation, etc.

Introduction: For this assignment we are called up on to implement a test bench for a sophisticated universal shift register. In an improvement to previous shift registers designed in this class this one possesses the ability to remember its state thanks to the procedural assign functionality of the always_comb syntax available in System Verilog. Our task is to implement a test bench capable of probing the functionality of Pong Chu's existing module and proving its functionality. Firstly, we will test its load functionality, its ability to shift left, right and to hold a memory state and finally we will force an asynchronous reset to bring it back to a ground state.

Implementation: Since we were only asked to design a test bench the unit under test will not be elaborated on here.

Test Bench: The test bench initializes a clock on lines 25-31 which is easily configurable through a local param N. As such if we need to speed up or slow down the period of machine, we can simply change this one local parameter.

After wards it resets the system and as soon as a system reset is complete begins to go through a series of tests for shifting left, right, holding and finally resets itself. All of this is managed in sync with the clock set up at the start of the program.

Proof of success:

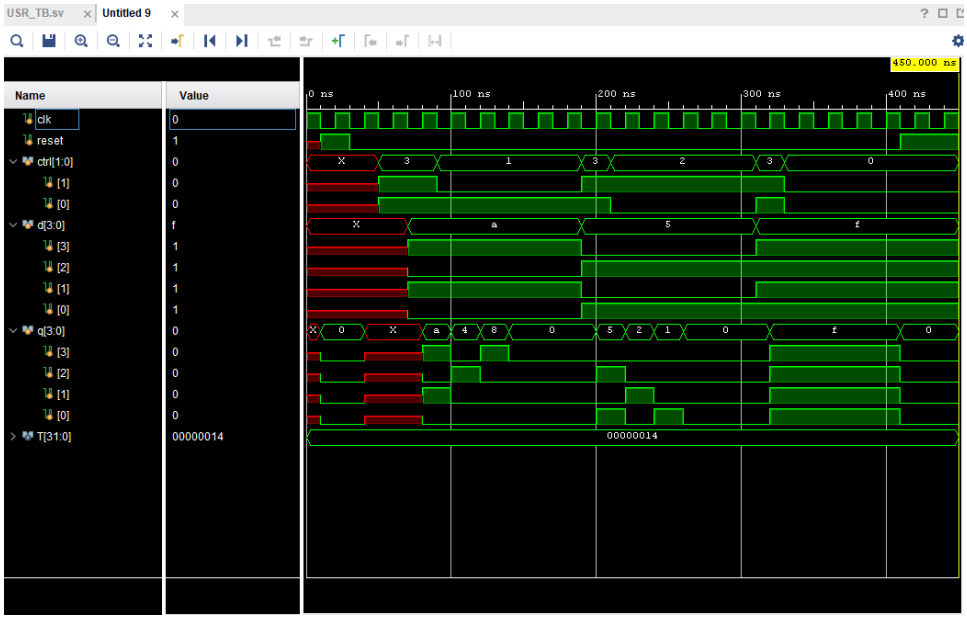

Figure 1: A wave diagram output by Vivado simulation.

The above wave diagram works through the functionality of Pong Chu's Universal shift register module. For example, this can be seen at time 210ns when the falling edge of the clock has ctrl at 2'b10 and the value of q is 4'b0010. Looking at the previous falling edge of the clock we can see the value of q is 4'b0101, meaning that it has been right shifted one space. As an additional check on functionality looking at time 410ns we can see that the reset pin goes high and the previously loaded value of 4'b1111 goes to 4'b0000 in the q output, showing that the module has been reset.

Summary: For this homework we were asked to write a test bench to evaluate the functionality of a universal shift register module that uses registers to store values as they are manipulated by its own internal functionality. The test bench as written demonstrates this functionality cleanly and proves its useful as a module for future projects.