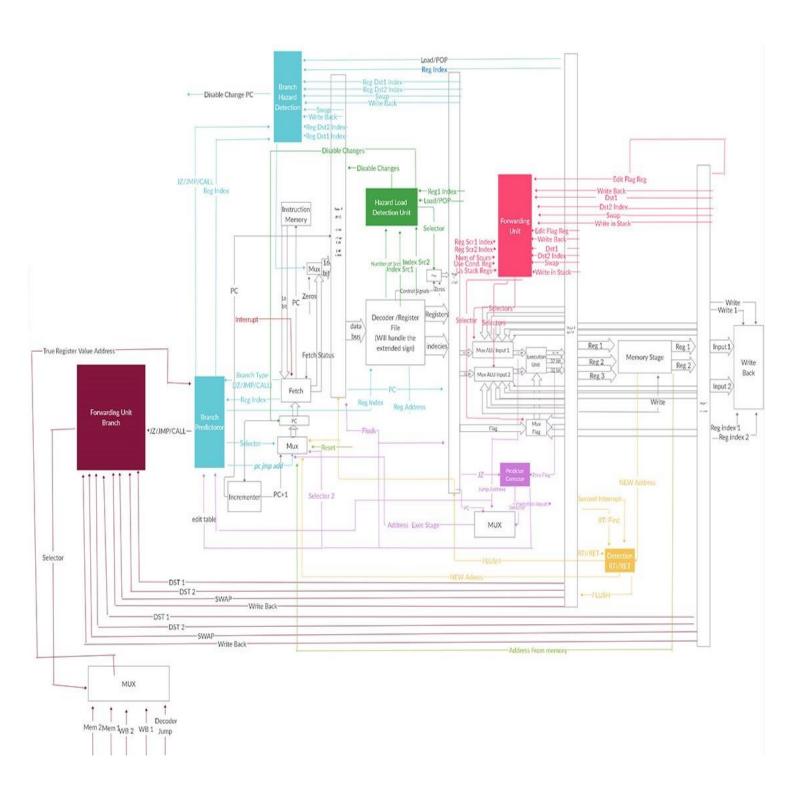




Project Arch Final delivery

Name	Section	B.N
Aly Ramzy Hassan	1	36
Mouhamed Khier	2	12
Nour Ahmed	2	31
Hager Ahmed	2	34

Full design:

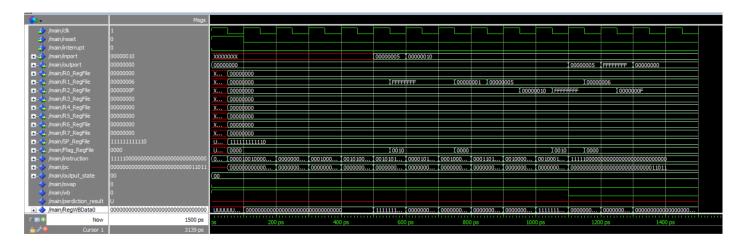


The unfinished parts of our processor:

- 1- Cash memory
- 2- Branch prediction

One operand file:

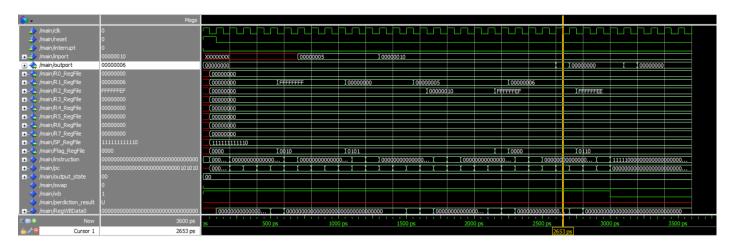
Before forwarding without no operation

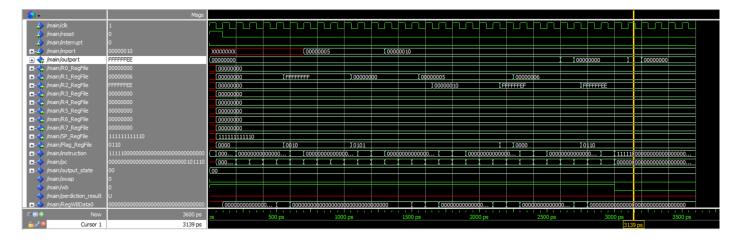


Hazards faced without forwarding:

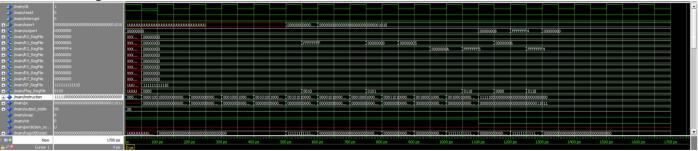
- 1- Inc R1 hazard is read after write.
- 2- Not R2 hazard is read after write.
- 3- Dec R2 hazard is read after write.
- 4- Out R1 hazard is read after write.
- 5- Out R2 hazard is read after write.

Before forwarding with no operation(solving the hazards with nop)



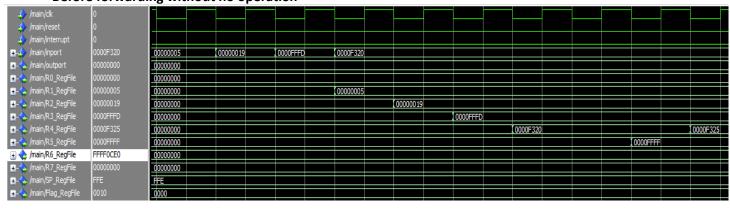


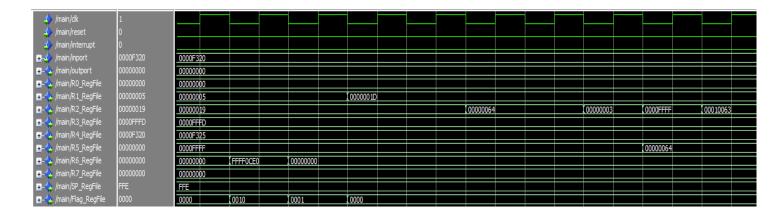
After forwarding:



Two operand file:

Before forwarding without no operation

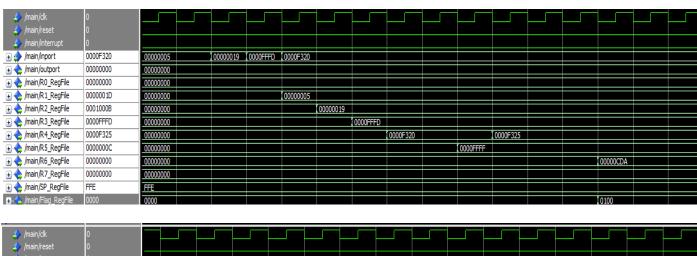


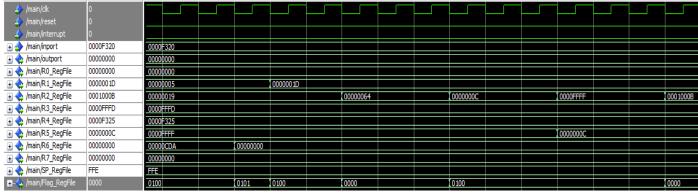


Hazards faced without forwarding:

- 1. SUB R5,R4,R6 hazard is read after write R4 & R5
- 2. AND R7,R6,R6 hazard is read after write R6
- 3. SHR R2,3 hazard is read after write R2
- 4. SWAP R2,R5 hazard is read after write R2
- 5. ADD R5,R2,R2 hazard is read after write R2 & R5

Before forwarding with no operation(solving the hazards with nop)





```
.ORG 2 #this is the interrupt address
100
.ORG 10
              #add 5 in R1
in
    R1
              #add 19 in R2
in
     R2
in
    R3
              #FFFD
    R4
              #F320
IADD R3,R5,2 #R5 = FFFF , flags no change
ADD R1,R4,R4
                #R4= F325 , C-->0, N-->0, Z-->0
NOP
NOP
               #R6= 0CDA , C-->1, N-->0,Z-->0
SUB R5,R4,R6
NOP
NOP
AND
    R7,R6,R6
                 #R6= 00000000 , C-->no change, N-->0, Z-->1
              #R1=1D , C--> no change, N-->0, Z--> 0
#R2=64 , C--> 0, N -->0 , Z -->0
OR
     R2,R1,R1
SHL
    R2,2
NOP
              #R2=0C , C -->1, N-->0 , Z-->0
SHR
    R2,3
NOP
NOP
SWAP R2,R5
              #R5=0C ,R2=FFFF ,no change for flags
NOP
ADD R5,R2,R2 #R2= 1000B (C,N,Z= 0)
```

After forwarding: / Imain/dk
/ Imain/dk
/ Imain/inset
/ Imain/interrupt
/ Imain/inte 00000005 00000019 0000FFFD 0000F320 00000000 00000000 00000005 0000001D 00000000 00000019 00000000 00000064 XXXXXXXXX XXXXXXXXXX 00000000 0000FFFD 00000000 0000FFFF 00000000 [00000CDA [00000000 → /main/R6_RegFile XXXXXXXX 00000000 , /main/R7_RegFile , /main/SP_RegFile XXXXXXXX 00000000 FFE 0100 0101 10000 0100 /main/clk /main/reset 0 /main/interrupt /main/inport **⊞**-4 0000F320 🛨 🔷 /main/outport 00000000 💶 👍 /main/R0_RegFile 00000000 🖢 /main/R1_RegFile 0000001D 💶 🔷 /main/R2_RegFile 00000019 00000064 0000000C 0000FFFF 0001000B 💶 🔷 /main/R3_RegFile 0000FFFD 💶 💠 /main/R4_RegFile 0000F325 🖕 /main/R5_RegFile 0000FFFF 0000000C 🛨 💠 /main/R6_RegFile XXXXXXXX 00000000

00000000

FFE

0100

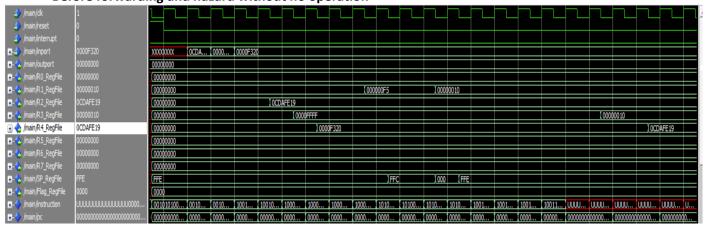
Memory file:

II-✓ /main/R7_RegFile

💶 🔷 /main/SP_RegFile

🔈 /main/Flag_RegFile

Before forwarding and hazard without no operation

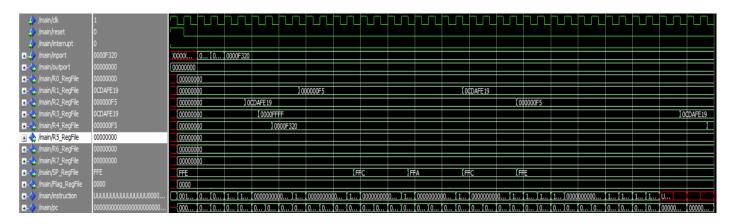


0000

0100

0000

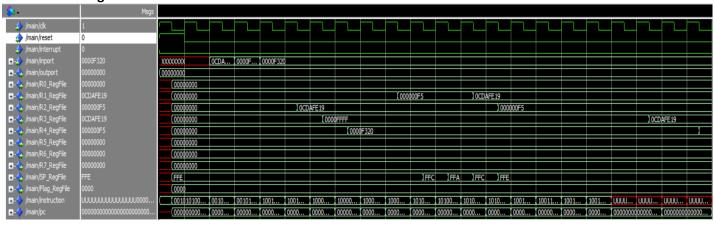
Before forwarding and hazard with no operation(solving the hazards with nop)



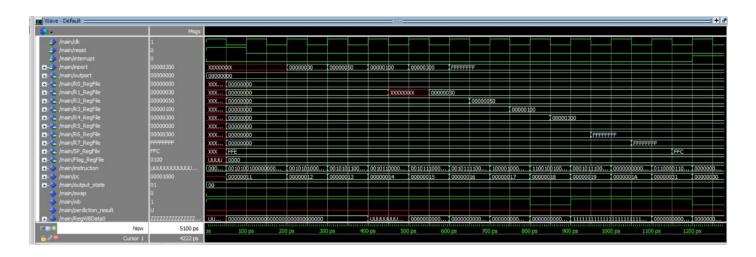
After only forwarding but no hazard:

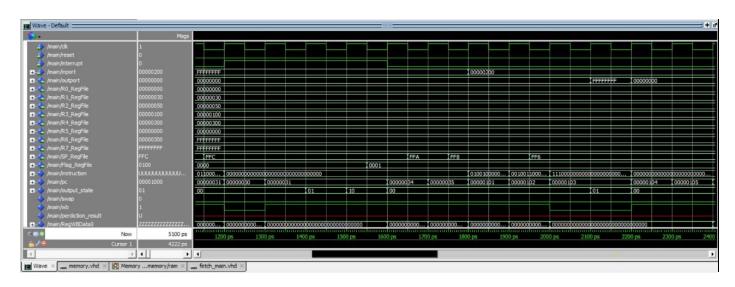
Aiter only i	After only forwarding but no nazard:																					
/main/dk /main/reset	1			╀			P-			┞	₽		P_		P_			┌				\Box
/main/interrupt	0																					
-/ /main/inport	0000F320	XXXXXXXX	OCDA	0000F	0000F320																	
	00000000	00000000																				
	00000000	00000000																				
	OCDAFE19	00000000								(000	000F5		(OCD	AFE19								
	000000F5	00000000				(OCD	AFE19							(000	000F5							
	OCDAFE19	00000000					(000	0FFFF												(OCD	AFE19	
	000000F5	00000000						(000	F320													
	00000000	00000000																				
	00000000	(00000000																				
	00000000	(00000000																				
	FFE	FFE									FFC	(FFA	(FFC	(FFE								
	0000	0000																				
<u>→</u> /main/instruction	UUUUUUUUUUUUUUUU0000	(001010100	0010	00101	1001	1001	1000	10000	1000	1000	1010	10100	1010	1010	1001	10011	1001	1001	UUUU	UUUU	UUUU	UUUU
. → /main/pc	000000000000000000000000000000000000000	000000000	0000	00000	0000	0000	0000	00000	0000	0000	0000	00000	0000	0000	0000	00000	0000	0000	00000000	00000	00000000	00000

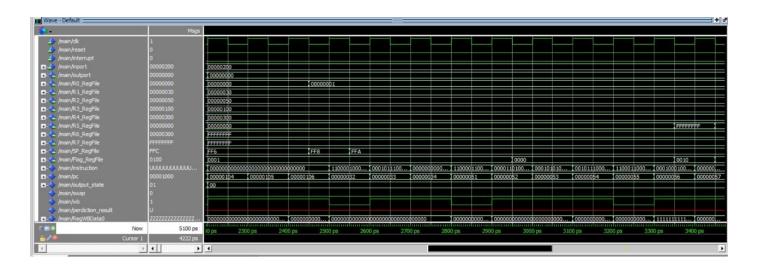
After forwarding and hazard:

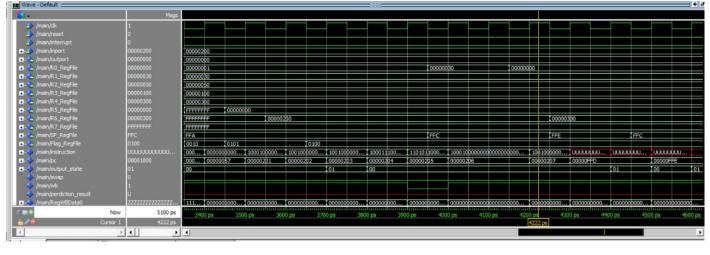


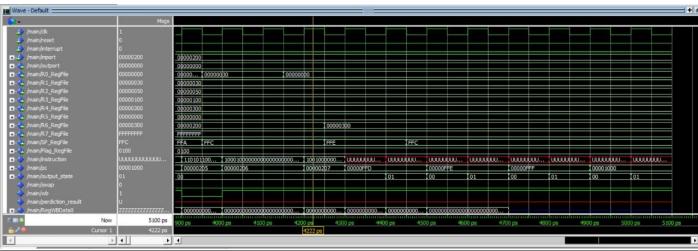
Branch file:











The following case show that the interrupt is working correctly.