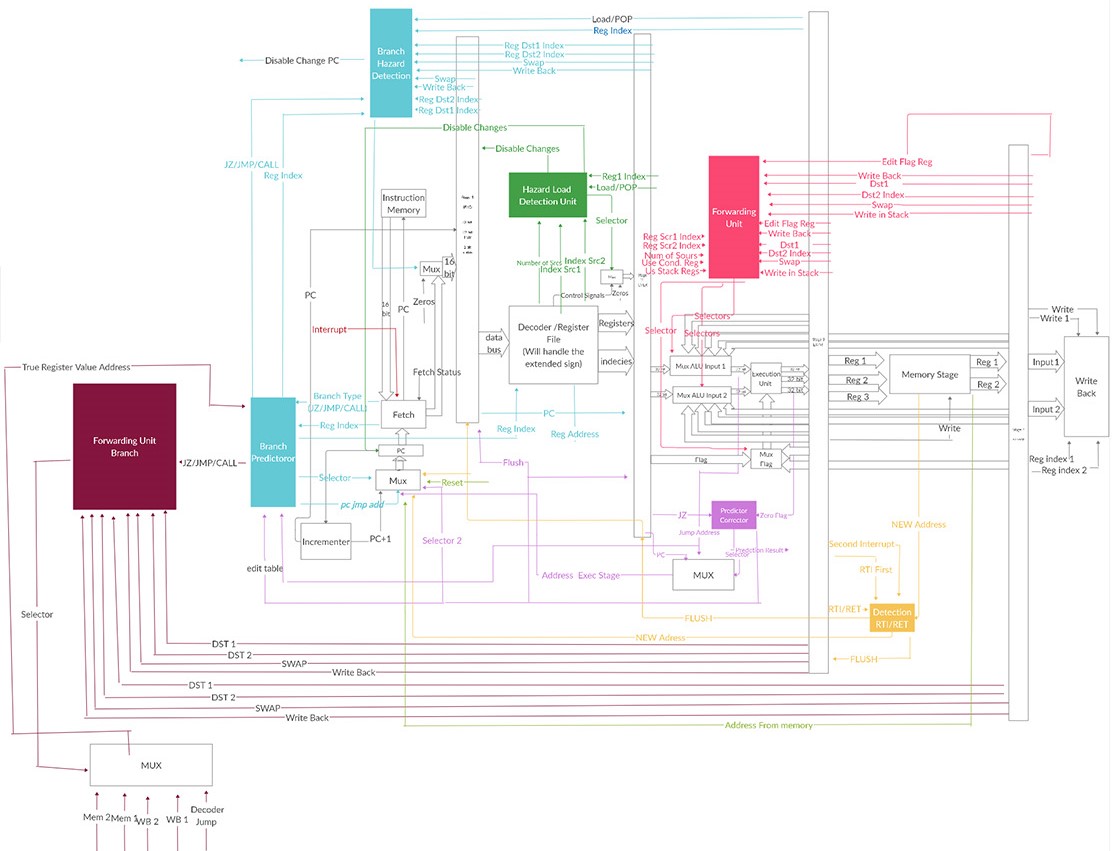
 **Cairo University**

**Faculty of Engineering**

**Project Arch**

**Final delivery**

|  |  |  |
| --- | --- | --- |
| Name | Section | B.N |
| Aly Ramzy Hassan | 1 | 36 |
| Mouhamed Khier | 2 | 12 |
| Nour Ahmed | 2 | 31 |
| Hager Ahmed | 2 | 34 |

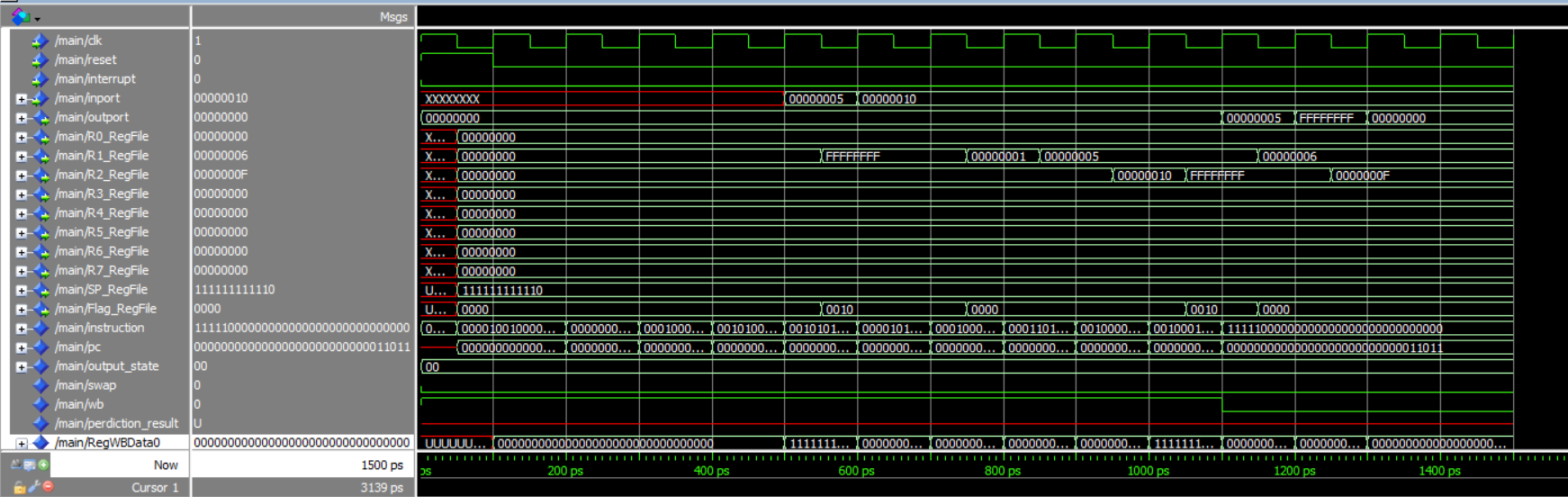
**Full design:**

**The unfinished parts of our processor:**

1. Cash memory
2. Branch prediction

**One operand file:**

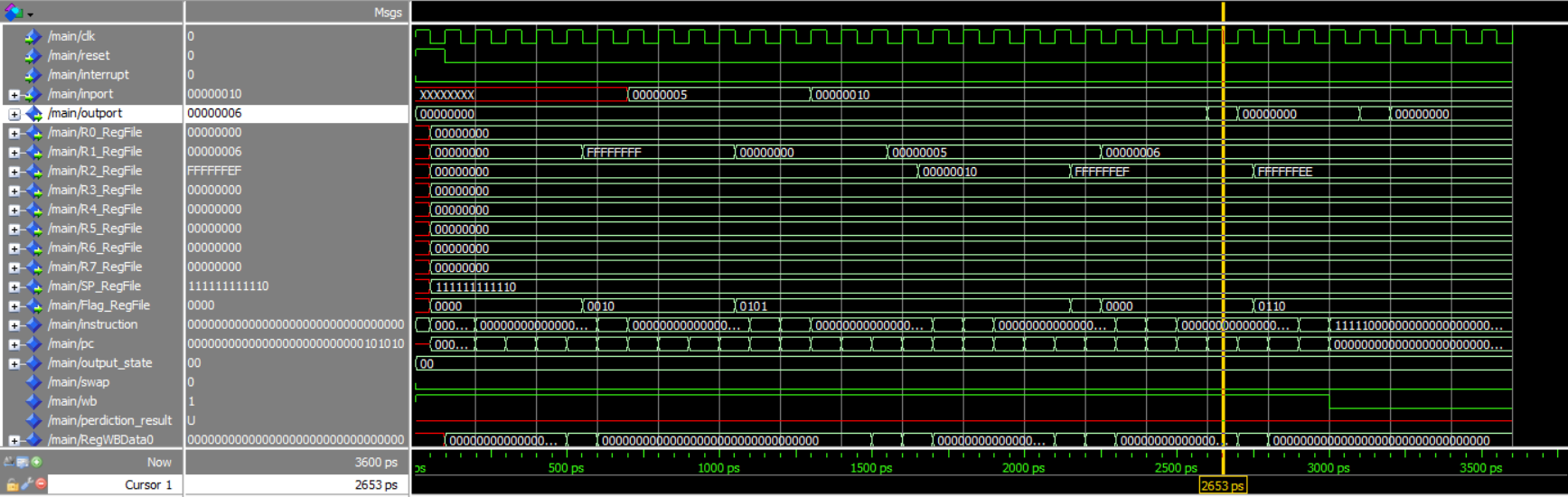
**Before forwarding without no operation**

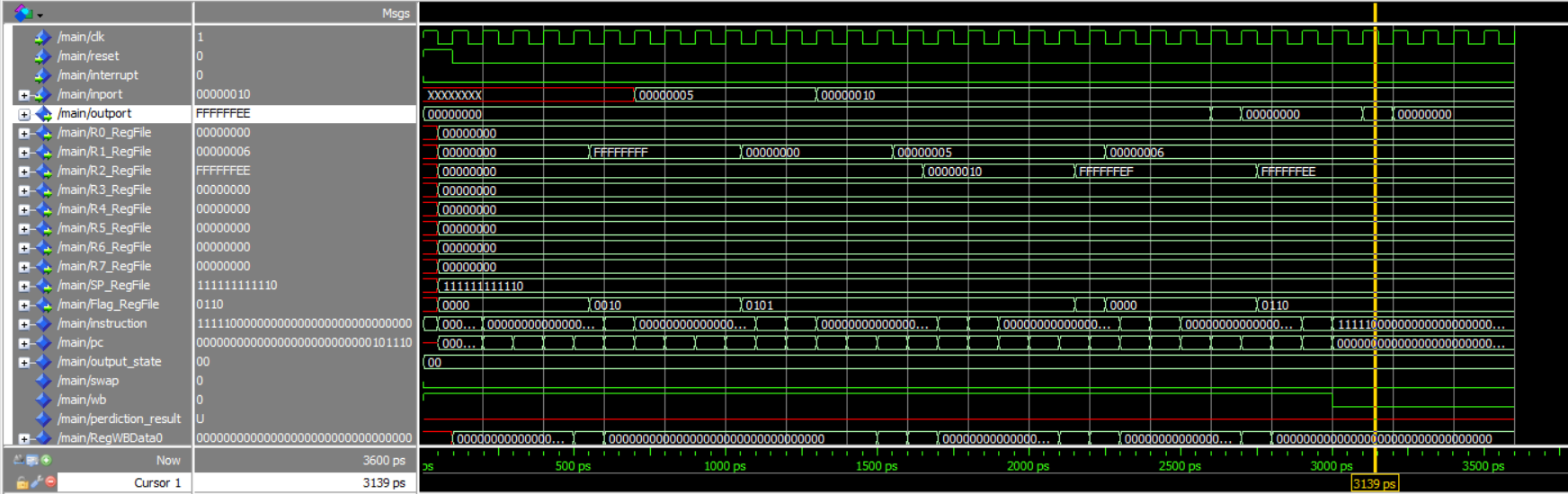
****

**Hazards faced without forwarding:**

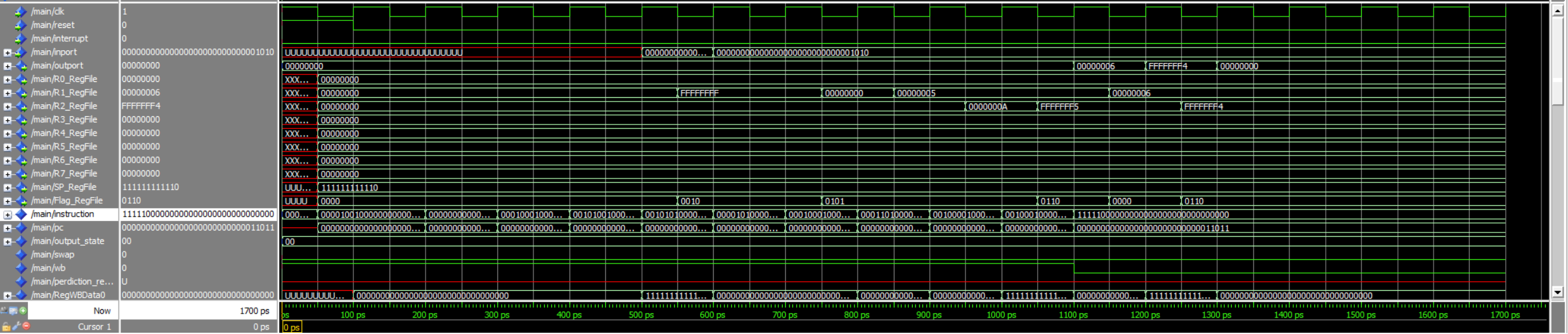
1. Inc R1 hazard is read after write.
2. Not R2 hazard is read after write.
3. Dec R2 hazard is read after write.
4. Out R1 hazard is read after write.
5. Out R2 hazard is read after write.

**Before forwarding with no operation(solving the hazards with nop)**

****

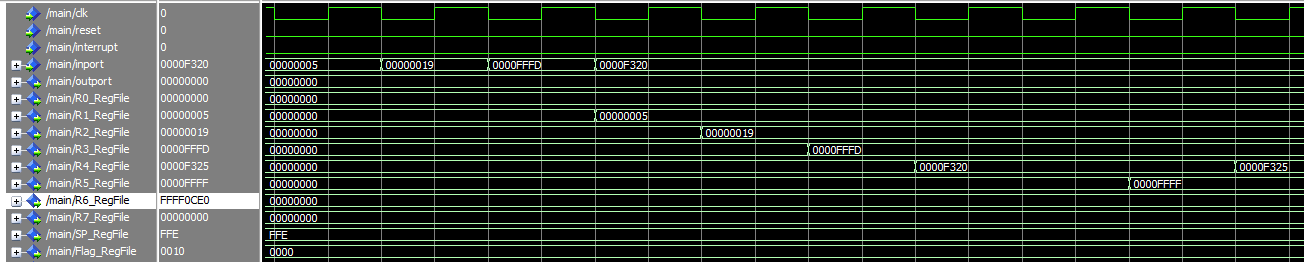
****

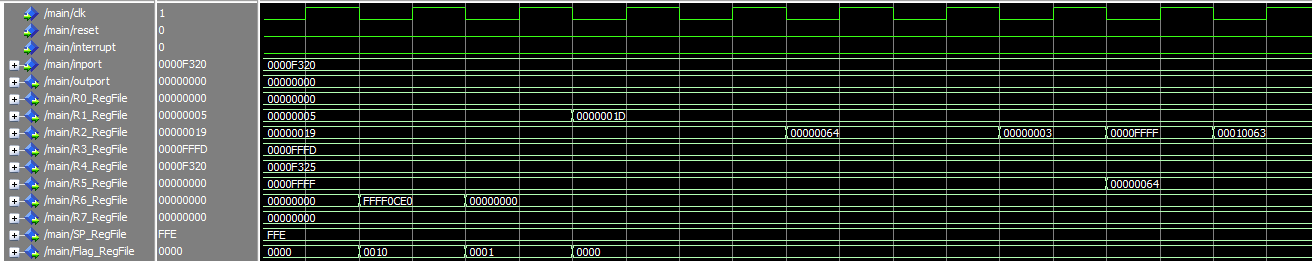
**After forwarding:**

****

**Two operand file:**

**Before forwarding without no operation**

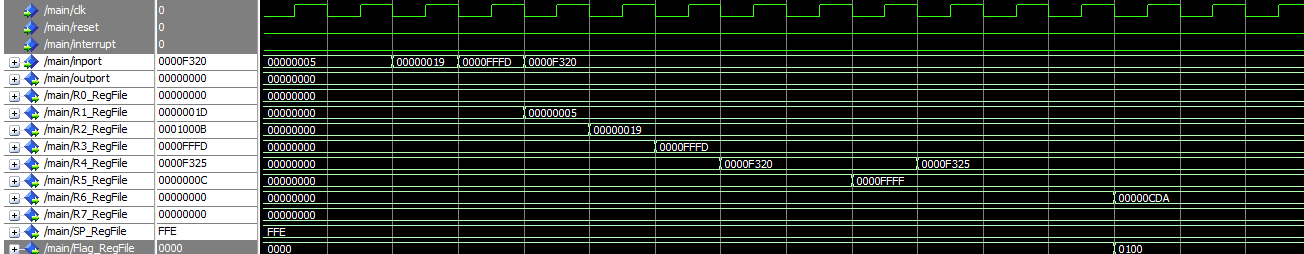
****

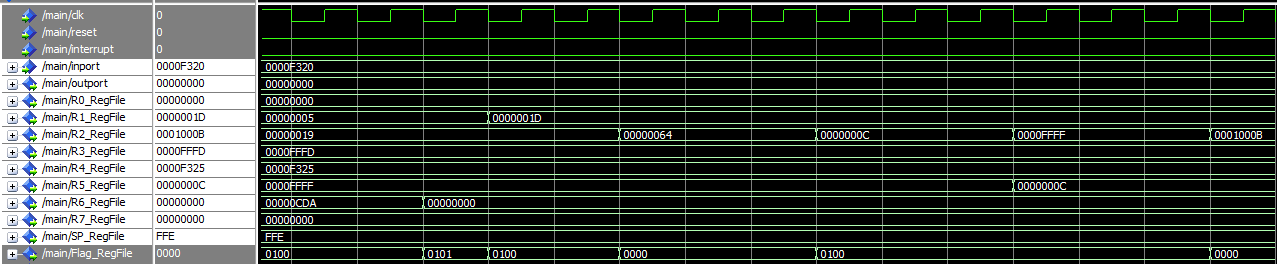
****

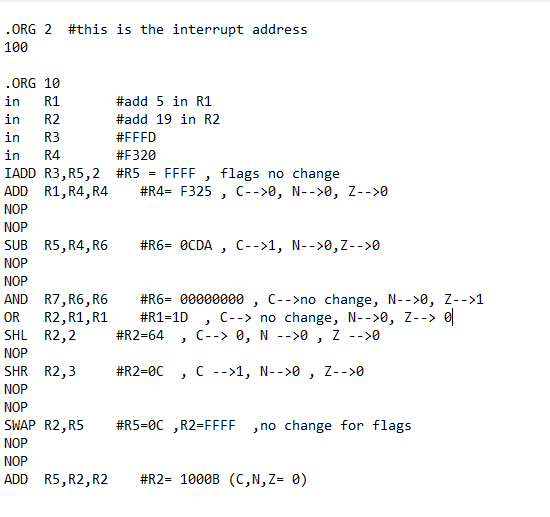
**Hazards faced without forwarding:**

1. SUB R5,R4,R6 hazard is read after write R4 & R5
2. AND R7,R6,R6 hazard is read after write R6
3. SHR R2,3 hazard is read after write R2
4. SWAP R2,R5 hazard is read after write R2
5. ADD R5,R2,R2 hazard is read after write R2 & R5

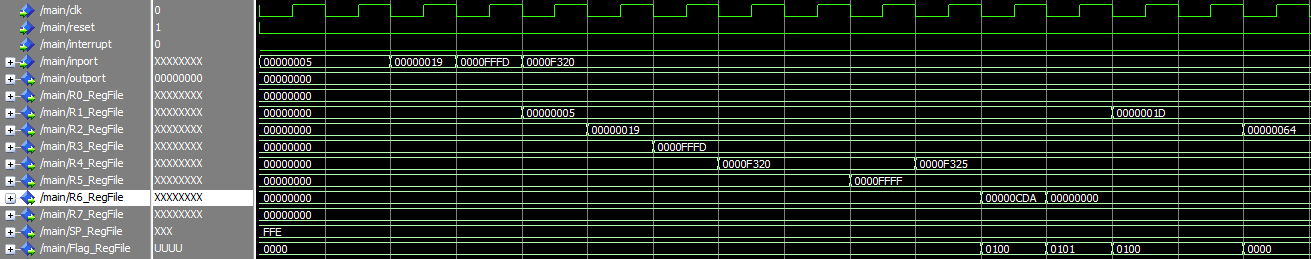
**Before forwarding with no operation(solving the hazards with nop)**

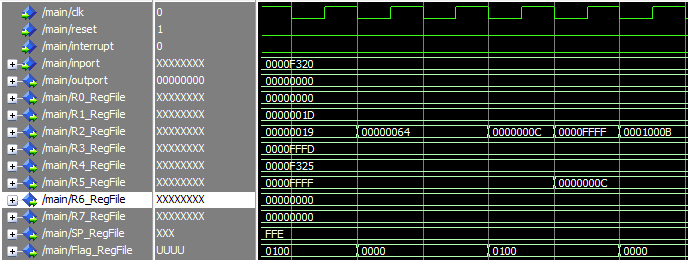
****

****

****

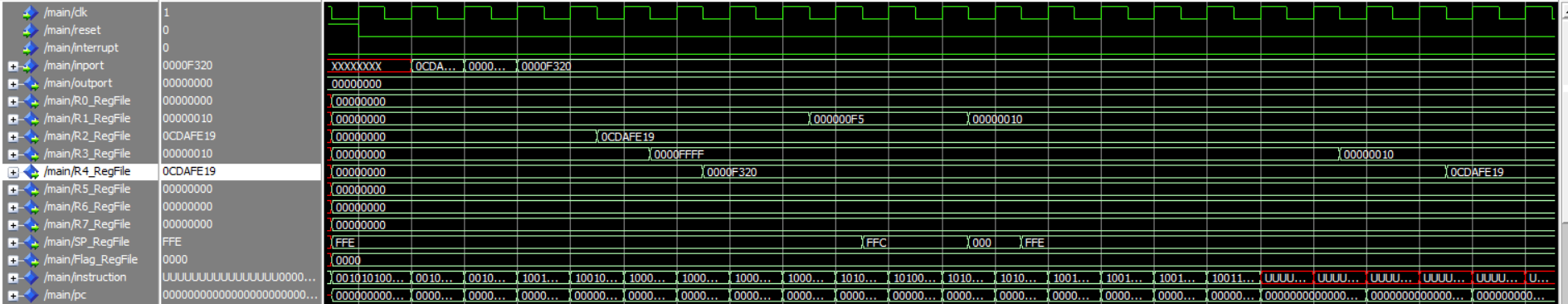
**After forwarding:**

****

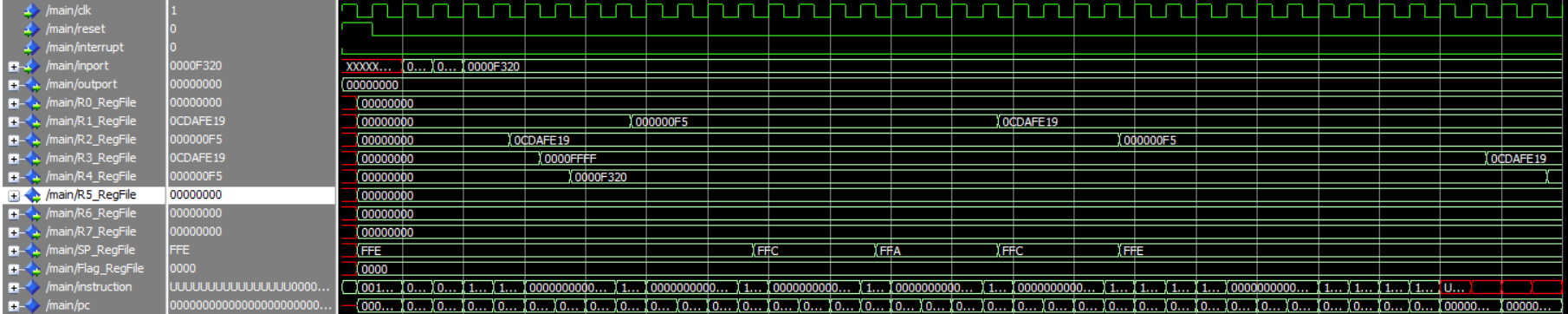
****

**Memory file:**

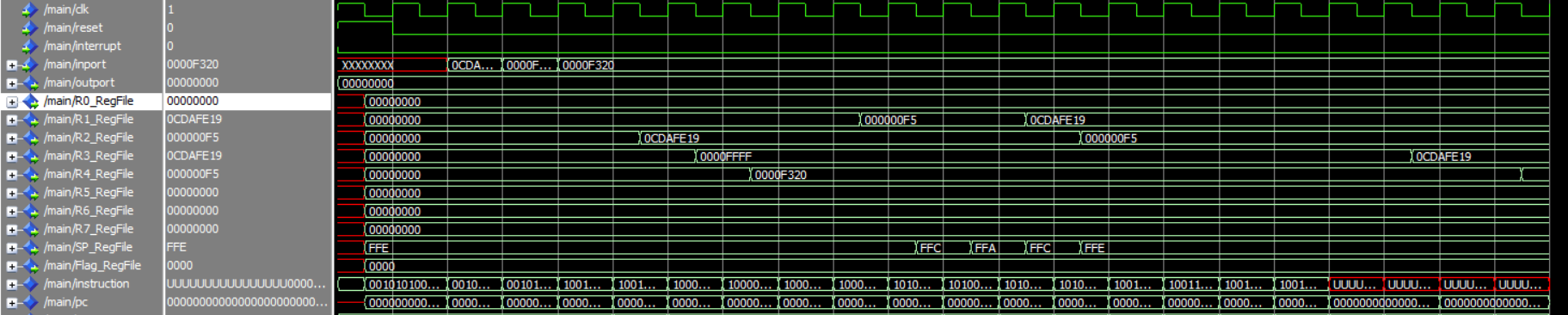
**Before forwarding and hazard without no operation**

****

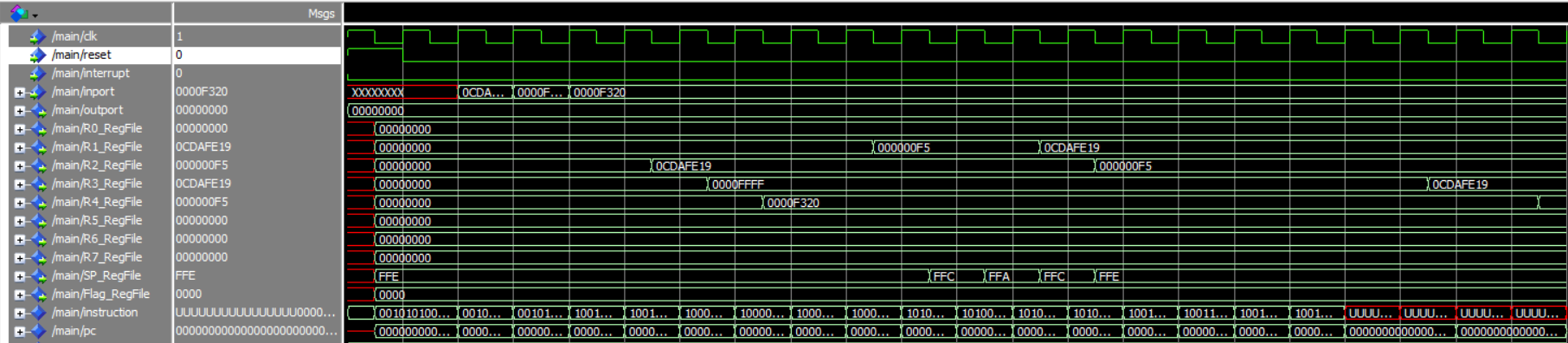
**Before forwarding and hazard with no operation(solving the hazards with nop)**

****

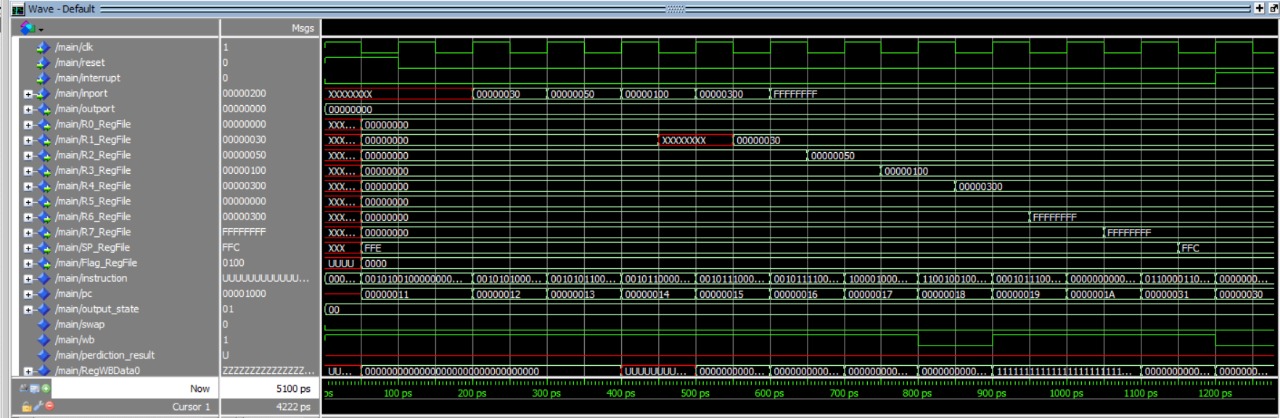
**After only forwarding but no hazard:**

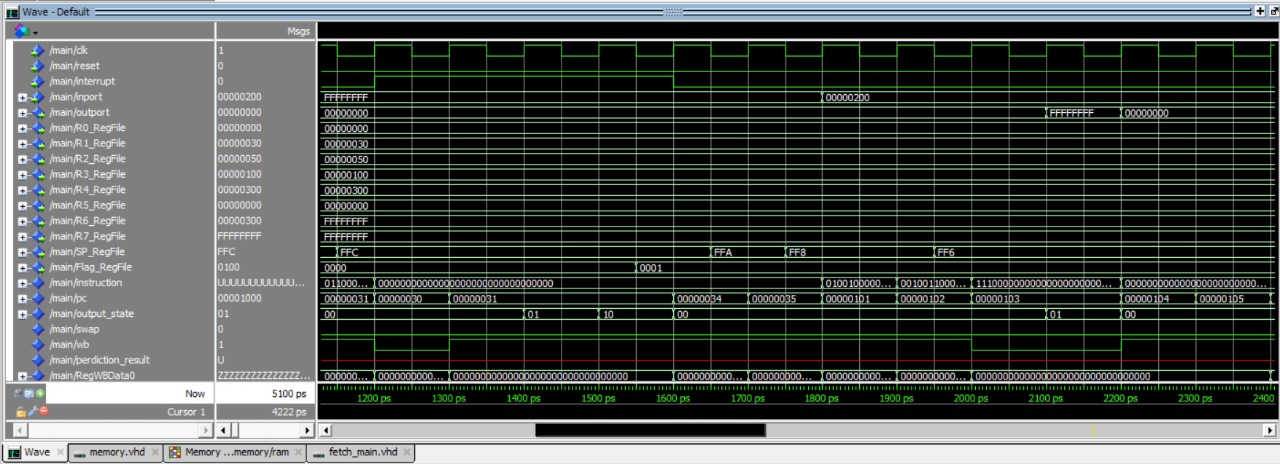
****

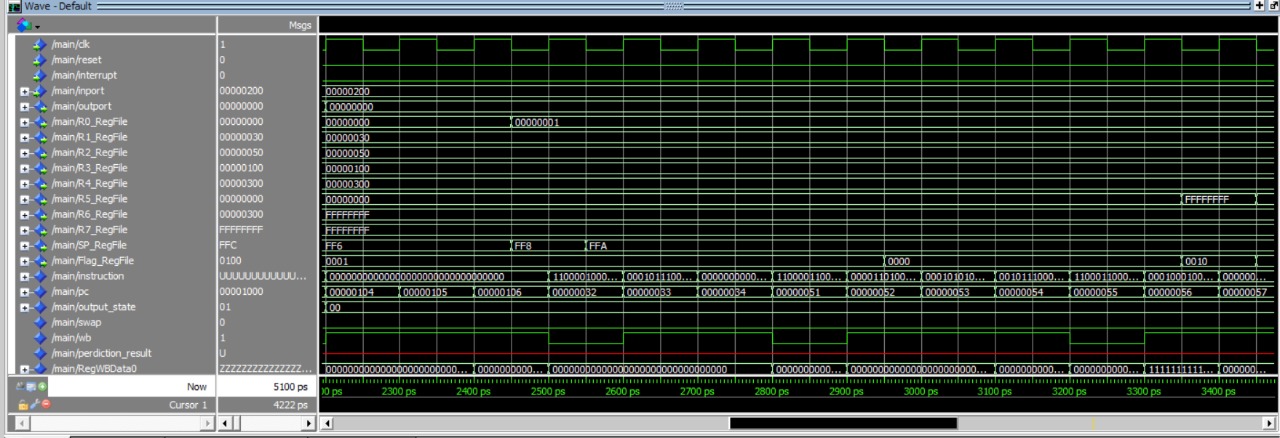
**After forwarding and hazard:**

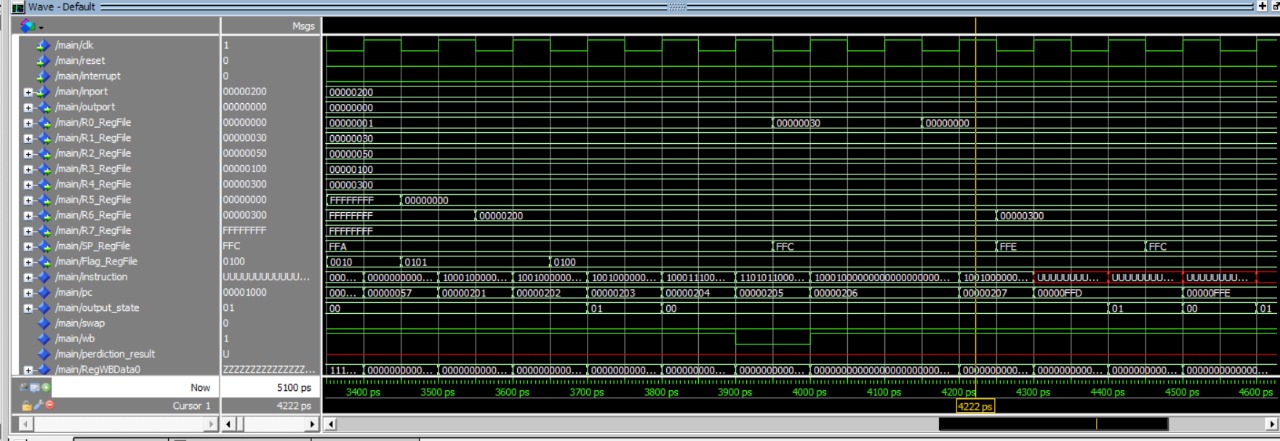
****

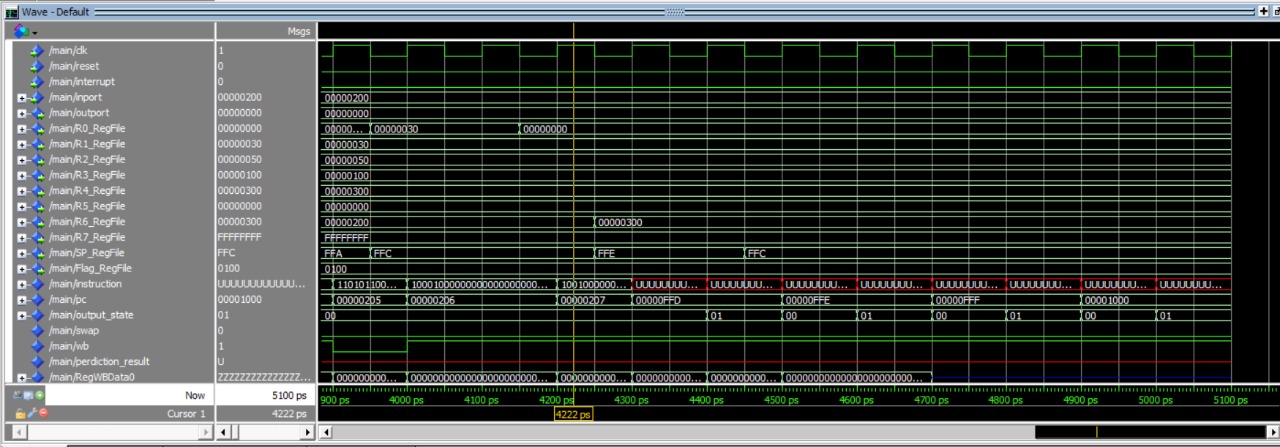
**Branch file:**









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**The following case show that the interrupt is working correctly.**