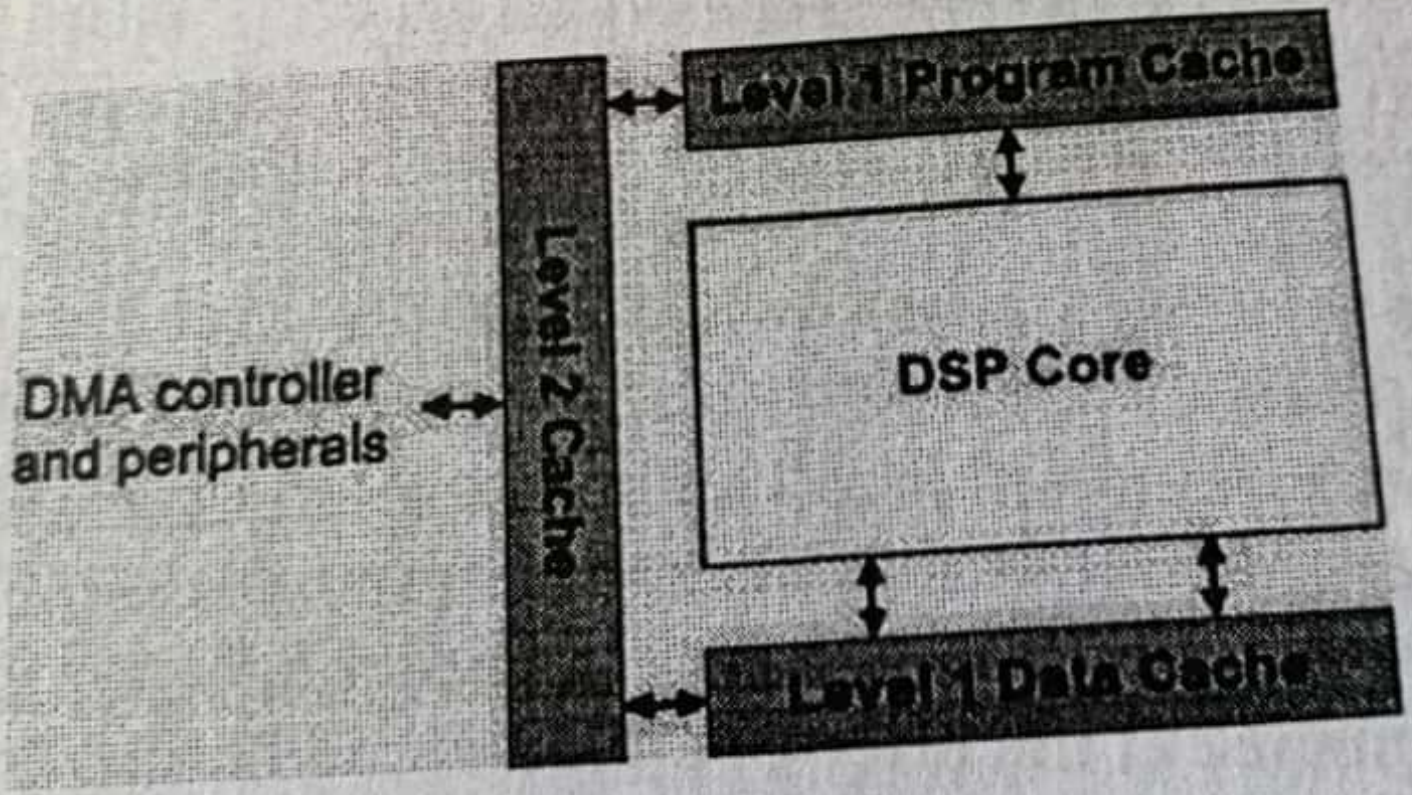
gram and data cache. There
L1 cache comprises 8 kbyte of memory divided into 4 kbyte of program
cache. The L2 cache comprises 256 kbyte of memory divided into 19
mory and 64 kbyte dual cache memory. The latter can be configured
combination of the two.



20C67xx family two-level cache architecture

he memories improve the average system performance. Howe
owing to the lack of

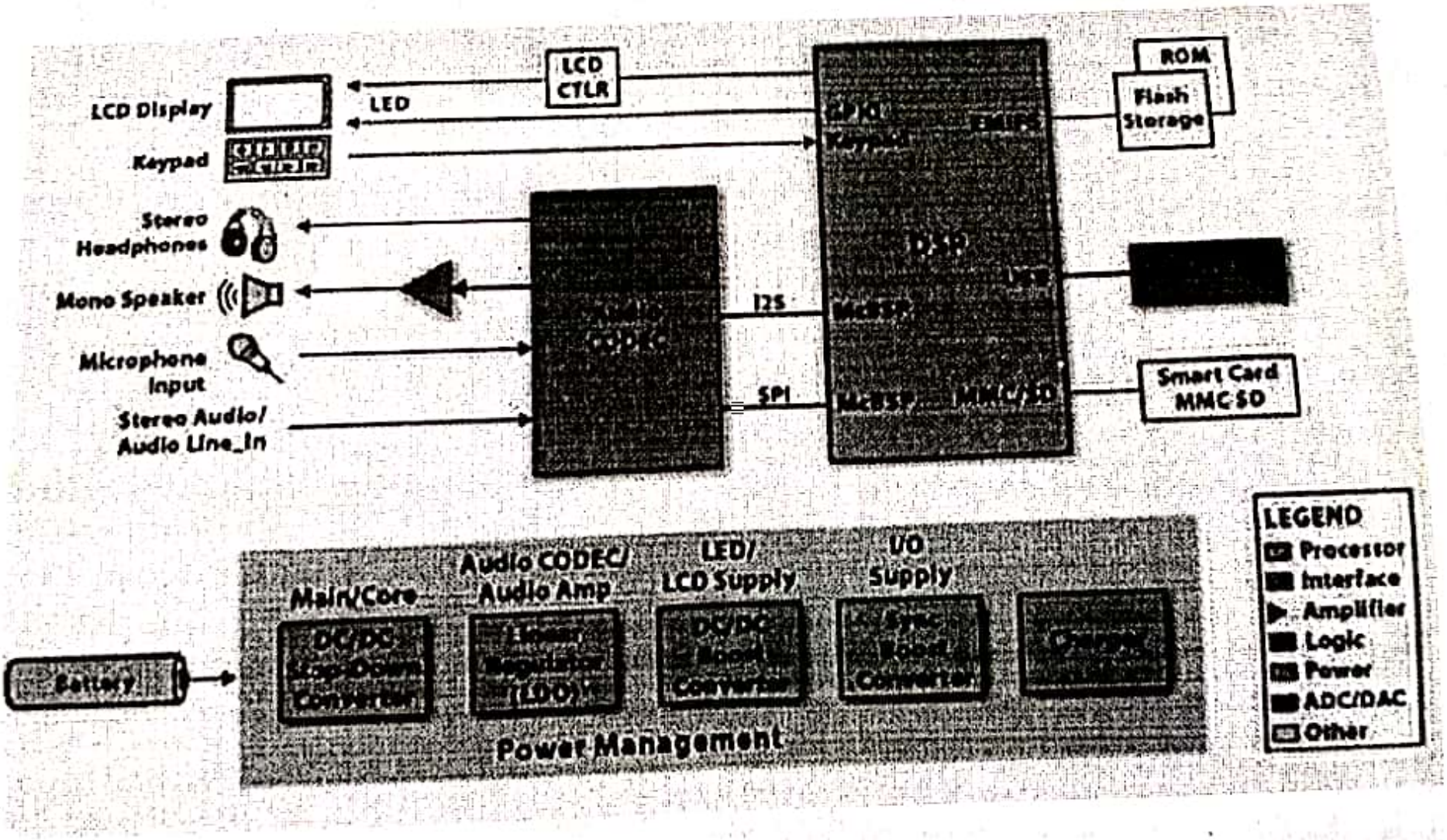


Fig. 2: Use of Texas Instruments DSP in a MP3 player/recorder system. Picture courtesy of Texas *Instruments.*

To illustrate this concept, the diagram above shows how a DSP is used in an MP3 player. During

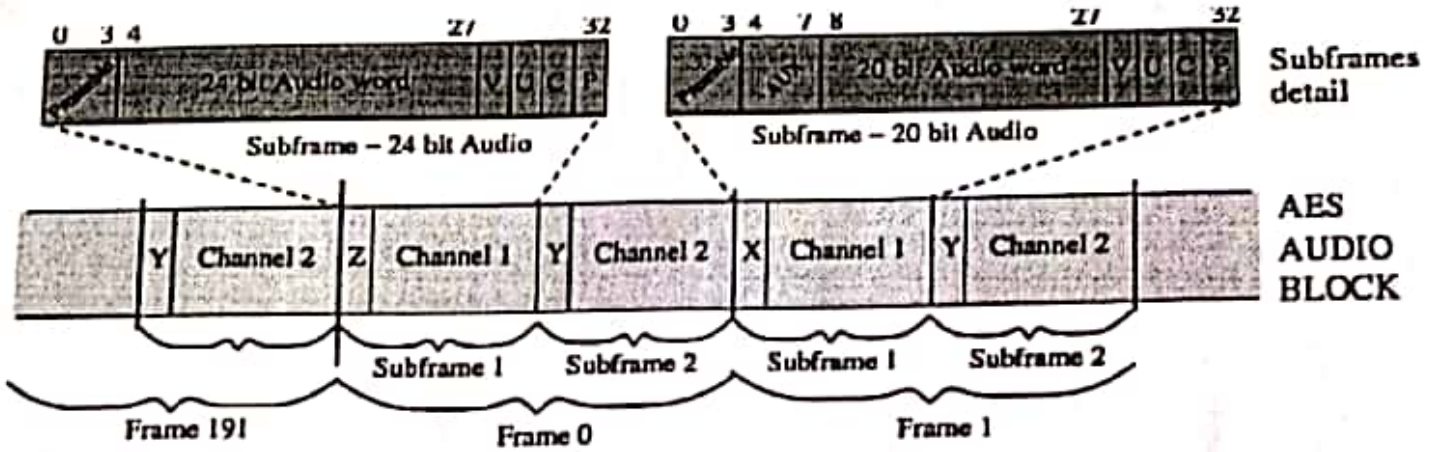


Fig.

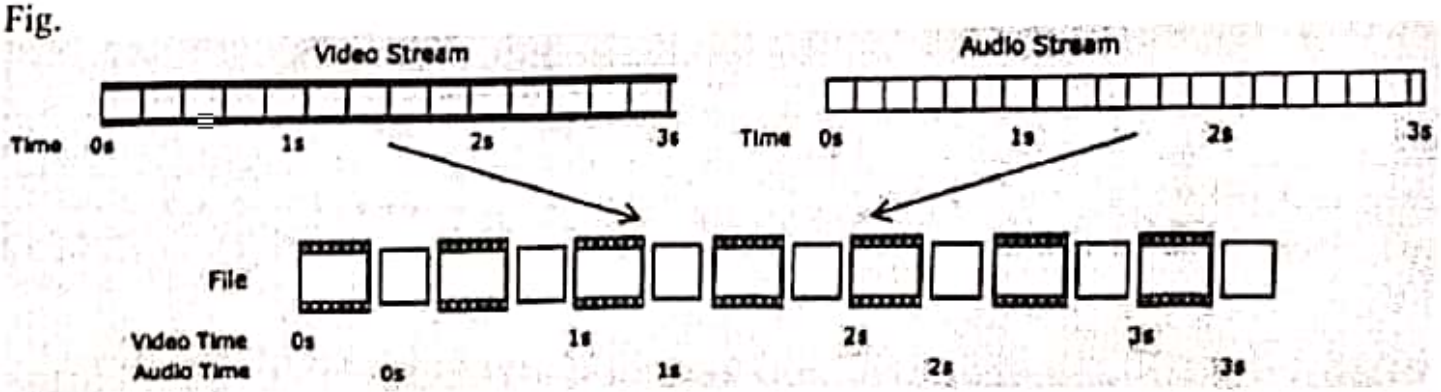


Fig.

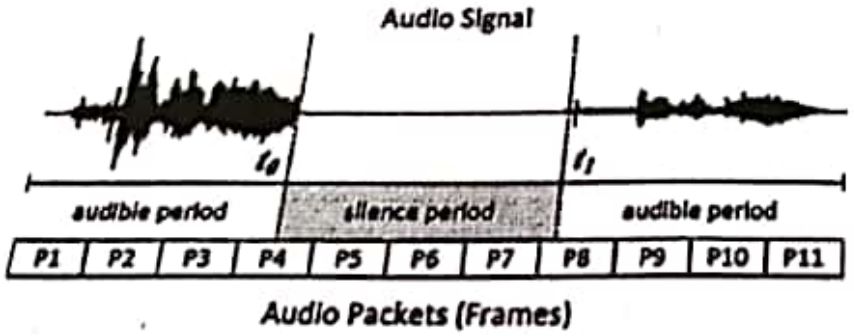


Fig.

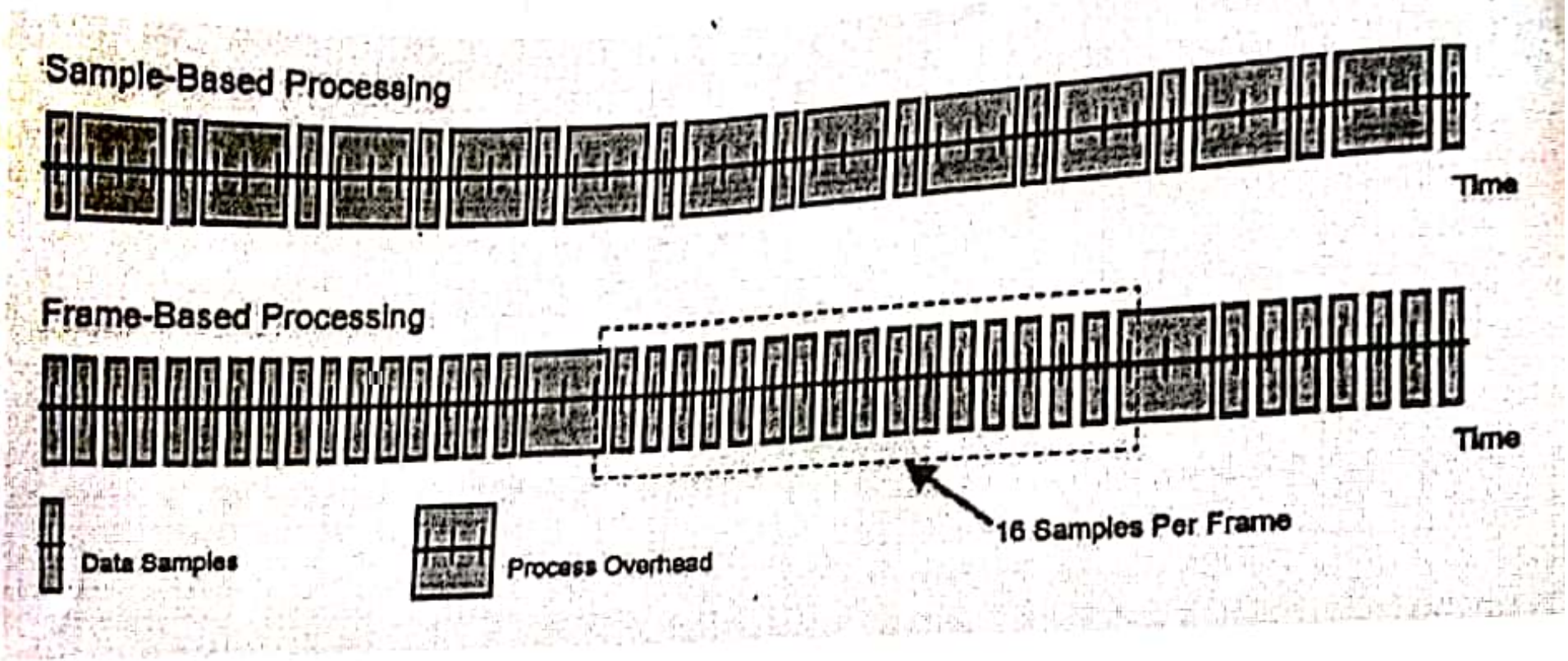


Fig.9

For an audio sampling rate of 48KHz, a processor working on a frame of 1042 samples have a frame acquisition interval of 21.22ms (ie 1024*20.833 microseconds). Here, the DSP has 21.33ms to complete all the required processing task for that frame of data. If the system handles signals in real time, it must not lose data; so, while the DSP is processing the first frame, it must also be acquiring the second frame.