

DEPARTMENT OF COMPUTER ENGINEERING,  
UNIVERSITY OF BENIN, BENIN CITY  
2017/2018 SESSION 2<sup>ND</sup> SEMESTER EXAMINATION

CPE522: SYSTEM PROGRAMMING  
ATTEMPT FIVE (5) QUESTIONS ONLY

Time: 3 hours

28/10/2018

- 1a. A full sub-tractor implements the arithmetic equation

$$D_i B_{out} = A - B - B_{in}$$

Where  $D_i$  and  $B_{out}$  denote the difference and borrow functions respectively. Derive a canonical sum-of-products Boolean equation for each output.

- i. Draw the logic circuit.  
ii. Write the entity declaration of the logic device.  
iii. Write the architecture behavioural description for the device.  
iv. Write the structural description for the device. (12marks)

- b. Write an entity declaration for a device with the following ports:

Port D is a 12-bit bus, input only  
Port OE and CLK are each input bits  
Port AD is a 12-bit, bi-directional bus  
Port A is a 12-bit bus, output only  
Port INT is a three-state output  
Port AS is an output only

(4marks)

Character statement definition

- c. State the general form of an object declaration and explain. (4marks)

- 2a. List and explain the major constructs in VHDL (12marks)

- b. A two-to-one multiplexer has three data inputs, a, b, and c and two select control inputs, X and Y. The multiplexer has a single output Z. If  $X = 1$ , Z is equal to a. If  $Y = 1$ , Z is equal to b otherwise Z is equal to c

- i. Write an entity declaration for the multiplexer named mux. Express the process statement for the multiplexer. (5marks)

- c. State the purposes that procedures serve in VHDL (3marks)

- 3a. List the characteristics of a process statement (4marks)

- b. Consider the process statement below

Signal S: Integer:=0;  
P1: PROCESS  
Begin  
S<= transport 1 after 1ns;  
S<= transport 1 after 1ns, 2 after 3ns, 4 after 4ns, 7 after 5ns;  
S<= transport 2 after 2ns;  
S<= transport 3 after 5ns, 4 after 4ns, 4 after 5ns, 6 after 10ns;  
Wait

End Process;

- i. What does this process statement do? (place four time/value pairs in the different for S)  
ii. What is the effect of the process statement on S? (6marks)

1 ns after 1 ns | 2 ns after 2 ns | 3 ns after 3 ns | 4 ns after 4 ns | 5 ns after 5 ns | 6 ns after 6 ns | 10 ns after 10 ns |

1 ns after 1 ns | 2 ns after 2 ns | 3 ns after 3 ns | 4 ns after 4 ns | 5 ns after 5 ns | 6 ns after 6 ns | 10 ns after 10 ns |

- A vhdl program controls a LED using a switch. When the switch is toggle to one (1) the reading (switch) will turn on when toggle to zero the reading (switch) will turn off.
- Briefly explain the behavior of the device described.
  - Sketch the device described
  - Write the architecture description of the device using concurrent signal assignment statement

(10marks)

- 4a. Consider the process statement of Qn4a

```

P1: Process
Variable B: Integer:= 1;
Begin
Loop1:
  For A in 1 to 12 loop
    B:= 400;
    Loop2: loop
      If B< (A * *2)
        Exit loop2;
      End if;
      B:= B/A;
    End loop loop2;
  End loop loop1;
  Wait;
End process.
  
```



```

Switch = 1
begin
  process
    if switch = 1 then
      LED = 1;
    else
      LED = 0;
    end process;
  end behavioral;
  
```

- i. Rewrite the process statement using the while statement.

- ii. Write the syntax for the while statement.

- iii. Write the general form of the process statement used

(10marks)

- b. Function and procedure are classified as subprograms in VHDL. Explain the features that differentiate them.

(3marks)

- c. Write the general form of a VHDL function

(3marks)

- i. Write a VHDL "function" description for a 3-input exclusive OR function

(4marks)

5ai. Design, using ROM, a square look up table for  $F(x) = \begin{cases} 2x^2, & \text{for } 0 \leq x \leq 5 \\ 0, & \text{Otherwise} \end{cases}$

- ii. What is a look up table?

(12marks)

- bi. Outline the advantages of PLDs.

(8marks)

- ii. Distinguish between a PAL, ROM and PLA.

- 6a. The state diagram of a service machine is as shown in Fig.Qn7a

- i. Generate a state table for the machine

(15marks)

- ii. Design a FSM for the service machine

- iii. What does this machine do?

- b. Outline the advantages and disadvantages of FSMs

(5marks)

7. Consider a door combination lock FSM in Fig. Q7 with the following specification:

fr

Fig. Q7. A door combination lock has three digits. The first digit is 3, the second digit is 6, and the third digit is 2. The lock is initially closed. It can be opened by entering the correct sequence of digits. The sequence must start with 3, followed by 6, and end with 2. The lock will open if the sequence is entered correctly. If an incorrect digit is entered, the lock will remain closed. If the correct sequence is entered, the lock will open. The lock will remain open until it is closed again.

- When a user punches in 3 values in sequence, the door should open; if there is an error the lock must be reset; once the door opens the lock must be reset
  - Inputs consist of sequence of input values, reset
  - Outputs consists of door open/close
  - Memory of the system must remember combination or always have it available as an input

(a) i. Identify the number of states

ii. Describe each of the states and the corresponding transitions

identify the input and output of the FSM

(5marks)

(b) Explain how you can come up with an optimal encoding scheme for the states

(5marks)

(c) Develop a state transition table for the FSM

(10marks)

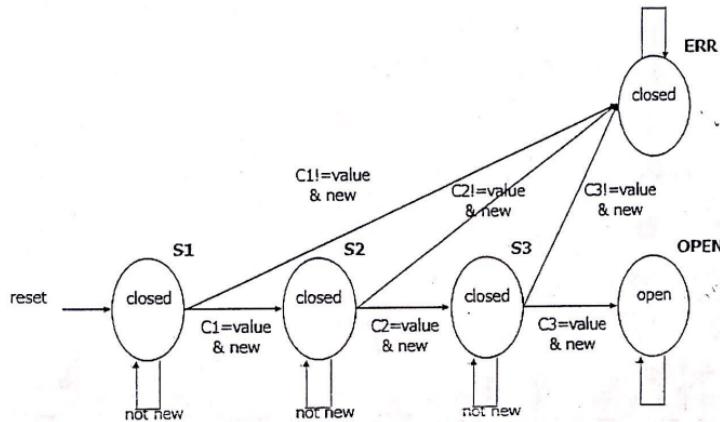


Fig. Q7

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 2<sup>nd</sup> SEMESTER EXAMINATIONS 2014/2015 SESSION

14<sup>TH</sup> September, 2015

CPE522: SYSTEM PROGRAMMING

Time: 3 Hours

INSTRUCTION: ATTEMPT QUESTION ONE (1) AND ANY OTHER FOUR (4)  
 QUESTIONS ONLY

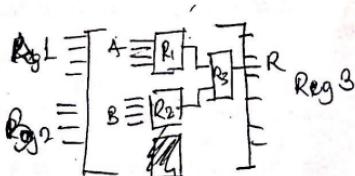
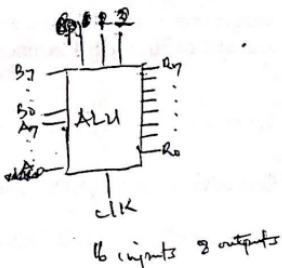
```

1. library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
entity simple_alu is
port( Clk : in std_logic; A,B : in signed(7 downto 0); Op : in unsigned(2 downto 0);
      R : out signed(7 downto 0) --output of ALU );
end simple_alu;

architecture Behavioral of simple_alu is
--temporary signal declaration,
signal Reg1,Reg2,Reg3 : signed(7 downto 0) := (others => '0');
begin
    Reg1 <= A;
    Reg2 <= B;
    Reg3 <= Reg3;
    process(Clk)
    begin
        if(rising_edge(Clk)) then
            case Op is
                when "000" =>
                    Reg3 <= Reg1 + Reg2;
                when "001" =>
                    Reg3 <= Reg1 - Reg2;
                when "010" =>
                    Reg3 <= not Reg1;
                when "011" =>
                    Reg3 <= Reg1 nand Reg2;
                when "100" =>
                    Reg3 <= Reg1 nor Reg2;
                when "101" =>
                    Reg3 <= Reg1 and Reg2;
                when "110" =>
                    Reg3 <= Reg1 or Reg2;
                when "111" =>
                    Reg3 <= Reg1 xor Reg2;
                when others =>
                    NULL;
            end case;
        end if;
    end process;
end Behavioral;

```

reset condition  
 regt ready  
 securt level;



end if;  
end process;  
end Behavioral;

- Sketch the entity block of the digital device described
- Explain how this digital device works
- Write the general form of the conditional control(s) used in the process statement (14Marks)

- 2a. Consider Fig.Qn2a.

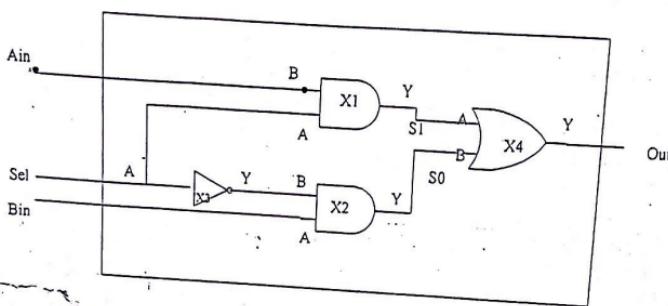


Fig.Qn2a

Write a structural description for Fig.Qn2a using named association for the component instantiation statement.(10 Marks)

- List and define the basic concepts of hardware structure.(4 Marks)
- Distinguish between component and entity declarations. (4 Marks)
- Write, with brief explanation, the general syntax of the architecture body. (7 Marks)
- One advantages of VHDL is Benchmarking capabilities.Explain.(3 Marks)

- 4a. List and define the conditions which can be set for process reactivation. (4 Marks)

- Write and briefly explain the syntax of the "Assertion statement".
- Outline the uses of assertion statement in VHDL description. (6 marks)
- Write and briefly explain the general forms of the VHDL's 'exit' statements. (4 Marks)

- 5ai. What is a VHDL identifier?  
ii. State the rules for defining VHDL identifiers.(5 Marks)  
b. Consider the description:

Architectural behavior of Device is

```
begin
  Process(x,y)
begin
```

④ exit loop label  
⑤ exit loop label, condition

Case expression  
when value  $\Rightarrow$   
out  $\leftarrow$

5. Convection  
time unit

```

If x = '1' and y = '1' then
Z <= transport '1' after delay;
Else
Z <= transport '0' after delay;
end if;
end process;
end architecture;

```

- i. Briefly explain the behaviour of the digital device described by the process statement.
- ii. Sketch the device described
- iii. Rewrite the architecture description of the device using concurrent signal assignment statement. (9Marks)

6. architecture Behavioral of JK\_Flipflop is

--signal declaration.

```

signal qtemp,qbartemp : std_logic := '0';
begin
    Q <= qtemp;
    Qbar <= qbartemp;

```

```

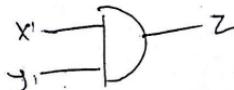
process(clk,reset)
begin
    if(reset = '1') then
        qtemp<= '0';
        qbartemp<= '1';
    elsif(rising_edge(clk)) then
        if(J='0' and K='0') then
            NULL;
        elsif(J='0' and K='1') then
            qtemp<= '0';
            qbartemp<= '1';
        elsif(J='1' and K='0') then
            qtemp<= '1';
            qbartemp<= '0';
        else
            qtemp<= not qtemp;
            qbartemp<= not qbartemp;
        end if;
    end if;
end process;
end Behavioral;

```

- i. Write the form of the process statement used in the behavioural description
- ii. Rewrite the description using the wait statement

X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

~~Ans~~



x,y: integer = 1

begin

z <= transport '1' after delay;

wait x,y

end architecture;

**DEPARTMENT OF COMPUTER ENGINEERING,  
UNIVERSITY OF BENIN, BENIN CITY  
2013/2014 SESSION 2<sup>ND</sup> SEMESTER EXAMINATIONS**

**CPE522: SYSTEM PROGRAMMING**

24/11/14

TIME : 3 HOURS

**INSTRUCTION: ANSWER QUESTION ONE (1) AND ANY OTHER FOUR QUESTIONS ONLY**

- 1a. Consider Fig.Qn1 below:

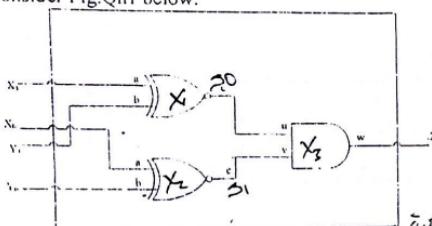


Fig.Qn1

- Write a VHDL description for the logic gate(s) used as (a) building block(s) for the digital device of Fig.Qn1
- Write a structural description for Fig.Qn1 using positional association for the component instantiation statement. (16 Marks)
- Write and briefly explain the syntax of the "Assertion statement". (6Marks) Pg 75
- Write, without any explanation, the general syntax of the architecture body. (2 Marks)
- Consider the process statement below:

Signal S:Integer:=0;

P1:

PROCESS

Begin:

S<=1 after 1ns, 3 after 3ns, 4 after 4ns, 5 after 5ns;  
S<=5 after 5ns, 4 after 5ns, 6 after 10ns;

Wait on level;  
End-process;

assert condition  
report message  
severity level;

Page 65

- What does this process statement do?
- What is the effect of the process statement on S? (5 Marks)
  - There are two levels in VHDL at which a designer must define the behavior of a discrete system. List and define these levels. (5 Marks) Pg 52

- 3a. Consider Fig.Qn3:

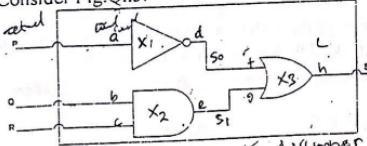


Fig.Qn3

- Write architecture body description for FigQn3 using named association for component instantiation statement.
- Write the general form of the entity declaration for a digital device with features of Fig.Qn3. (10 Marks) Pg 23
- VHDL is a strongly typed language. Explain (2 Marks) Pg 19.

- 4a. Define the following:
- Sensitivity channel Design entity (3 Marks) Pg 7
  - A signal S is assigned a logic 1 while a variable X is assigned a value 1. Write the VHDL representation for these assignments. (3 Marks)
  - Two advantages of VHDL are:  
 i. Device independent design  
 ii. Benchmarking capabilities. Explain why these are considered advantages. (6 Marks)
- (It does not enforce design methodology on design. It is compatible with VHDL as it is evaluated over time.)*

$S \leftarrow 1$

$X := 1$

- 5a. Consider Fig.Qn5

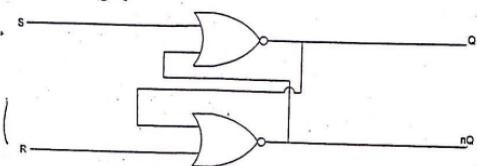


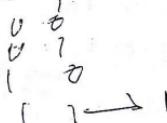
Fig.Qn5

- Write the VHDL description for the digital device Fig.Qn5 including an assertion statement for the condition that must not exist. (10 Marks)
- b. Write the general form of the process statement that is sensitive to the same set of signals. (2 Marks)
- 6a. Write the general form of the nested 'if' conditional control statement. (2 Marks)
- b. Consider the description:  
 Architectural behavior of D is -  
`begin`  
`Process(x,y)`  
`begin`  
 `If x = '1' and y = '1' then`  
 `Z <= transport '1' after delay;`  
 `Else`  
 `Z <= transport '0' after delay;`  
 `end if;`  
 `end process;`  
`end architecture;`
- i. Briefly explain the behaviour of the digital device described by the process statement.  
 ii. Sketch the device described (6 Marks)
- c. One of the shortcomings of VHDL is that the design Engineer gives up control of defining the gate-level implementation of circuits. Discuss. (4 Marks)
- 7a. Write and briefly explain the general forms of the VHDL's 'exit' statements. (4 1/2 Marks) Pg 73
- b. Outlines the uses of assertion statement in VHDL description. (3 marks)
- c. List and define the conditions which can be set for process reactivation. (4 1/2 Marks) Pg 53

`exit loop-label;`

Goodluck

`exit loop-label when condition;`



TH August, 2015

## CPE22: SYSTEM PROGRAMMING

Time: 1 1/2 hours

INSTRUCTION: ATTEMPT ALL QUESTIONS.

1. Consider Fig.Qn1.

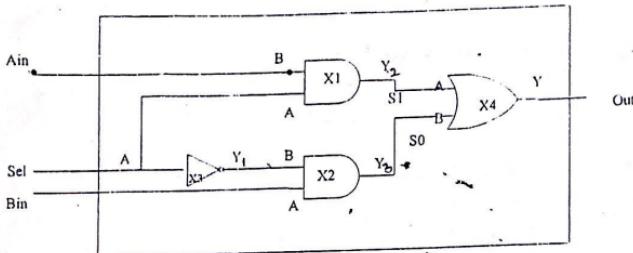


Fig.Qn1

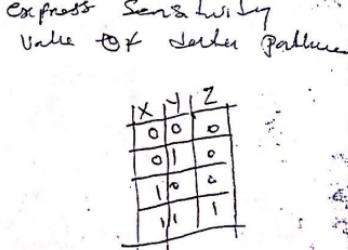
- a. Write a structural description for Fig.Qn1 using named association for the component instantiation statement. List and define the basic concepts of hardware structure.
2. Distinguish between component and entity declarations

~~2~~ One advantages of VHDL is Benchmarking capabilities. Explain why these are considered advantages

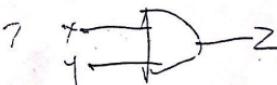
4. Define the following: i. Event ii. Sensitivity channel
- 5a. What is a VHDL identifier?  
b. State the rules for defining VHDL identifiers.)
- c. Consider the description:  
Architectural behavior of D is

```
begin
  Process(x,y)
    begin
      If x = '1' and y = '1' then
        Z <= transport '1' after delay;
      Else
        Z <= transport '0' after delay;
      end if;
    end process;
  end architecture;
```

- i. Briefly explain the behaviour of the digital device described by the process statement.  
ii. Sketch the device described (6 Marks)



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2016/2 E17

- ii. Write the entity declaration of the logic device  
 iii. Write the architecture behavioural description for the device using concurrent signal assignment. (14 Marks)
- b. Sketch and define the components of a finite state machine. (6 marks)
- 5a.i. Design using ROM, a square look up table for  $F(x) = \begin{cases} x^3, & \text{for } 0 \leq x \leq 5 \\ 0, & \text{Otherwise} \end{cases}$  (12 Marks)
- ii. What is a look up table? (12 Marks)
- bi. What is a programmable logic device?
- ii. Distinguish between a PAL, ROM and PLA. (8 Marks)
- 6a. Table Qn.6a below is the truth table of a code converter. Design a PAL logic implementation of the table. (14 Marks)
- b. Outline the advantages of PLDs. (6 Marks)
- 7a. The state diagram of a service machine is as shown in Fig. Qn7a
- i. Generate a state table for the machine
- ii. Design a FSM
- iii. What does this machine do? (15 Marks)
- b. Outline the advantages and disadvantages of FSMs (5 Marks)

Table Qn.6a: Code converter truth table

A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	1	1	1	0
0	1	1	0	1	0	1	0
0	1	1	1	1	0	1	1
1	0	0	0	1	0	0	1
1	0	0	1	1	0	0	0
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

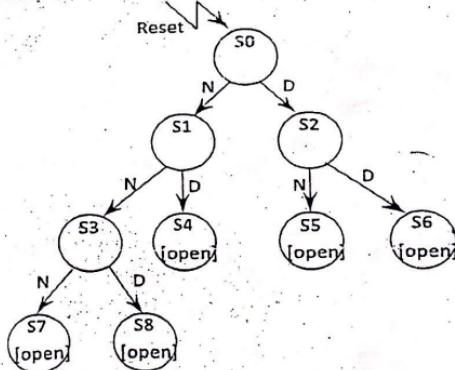


Fig. Qn.7a

N= Nickel = 5 Cents  
 D = Dime = 10 Cents

ii. Benchmarking capabilities.  
Explain why these are considered advantages. (5 Marks)

- b. Define the following:
- Event
  - Sensitivity channel (2 marks)
- c.i. What is the full meaning of the acronym VHDL?
- ii. What does the entity block of a VHDL code do?
- iii. What does the architecture block of a VHDL code do? (3 Marks)
- d.i. What is a VHDL identifier?
- ii. State the rules for defining VHDL identifiers. (4 Marks)
- 7a. List and define the types of delays associated with time/value pair assignment into the driver of a signal. (4 marks)
- b. One of the shortcomings of VHDL is that the design Engineer gives up control of defining the gate-level implementation of circuits. Discuss. (4 Marks)
- c. Consider the description:  
Architectural behavior of D is  
*begin*  
Process(x,y)  
*begin*  
    If x = '1' and y = '1' then  
        Z <= transport '1' after delay;  
    Else  
        Z <= transport '0' after delay;  
    end if;  
    end process;  
end architecture;
- Briefly explain the behaviour of the digital device described by the process statement.
  - Sketch the device described (6 Marks)

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- iii. Write and explain the form of the wait statement used
- iv. Rewrite the general form of the process statement for your answer to Qn6aii.
- v. What does the NULL statement, as used in the process statement, do?
- vi. Write the general form of the conditional control used in the process statement  
(14Marks)



- 7a. Consider Fig.Qn7.

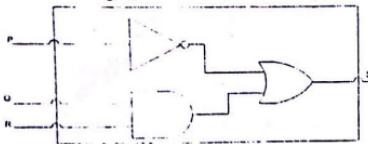


Fig.Qn7

- i. Write the entity declaration for the digital device of Fig.Qn7
- ii. Write the general form of the entity declaration for a digital device with features of Fig.Qn7.
- iii. Write the behavioural description for Fig.Qn7
- iv. Write the architecture behavior of Fig.Qn7 using concurrent signal assignment statement. (14 Marks)

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entity (name of entity)  
 Port (Signal name : mode type  
 );  
 end entity (name of entity);