DEPARTMENT OF COMPUTER ENGINEERING,
UNIVERSITY OF BENIN, BENIN CITY
2nd SEMESTER EXAMINATIONS 2014/2015 SESSION
TH August, 2015

CPE22: SYSTEM PROGRAMMING Time: 1 ½ hours

INSTRUCTION: ATTEMPT ALL QUESTIONS.

1. Consider Fig.Qn1.

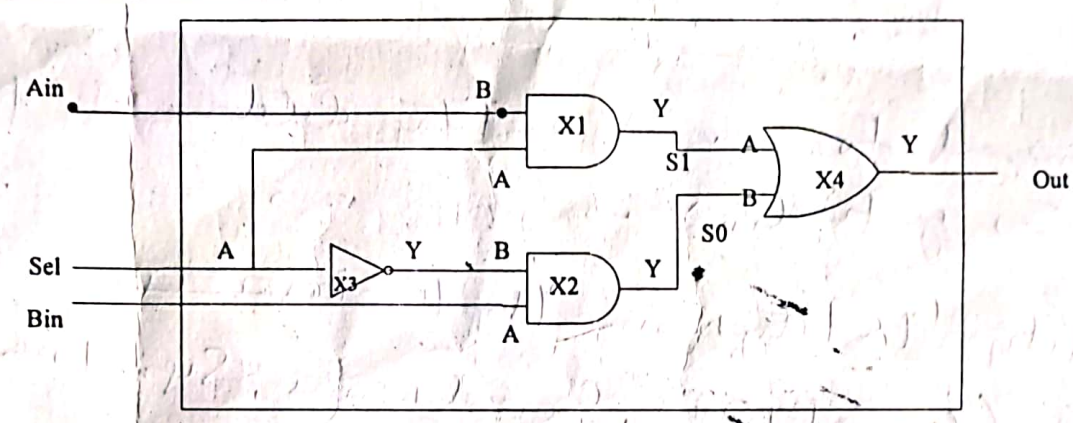

Fig.Qn1

a. Write a structural description for Fig.Qn1 using named association for the component instantiation statement. List and define the basic concepts of hardware structure.

2. Distinguish between component and entity declarations

3. One advantages of VHDL is Benchmarking capabilities. Explain why these are considered advantages

4. Define the following: i. Event ii. Sensitivity channel

5a. What is a VHDL identifier?

b. State the rules for defining VHDL identifiers.)

c. Consider the description:

```
Architectural behavior of D is
begin
    Process(x,y)
    begin
      If x = '1' and y = '1' then
      Z <= transport '1' after delay;
      Else
      Z <= transport '0' after delay;
      end if;
      end process;
end architecture;
```

i. Briefly explain the behaviour of the digital device described by the process statement.

ii. Sketch the device described *(6 Marks)*

GOODLUCK!!!

entity 'entity_name is
port (Signal_name, Signal name, Signal_name:
mode type;
Signal_name: mode type);
end entity_name;

The general form of a entity declaration for a digital device w features of fig Qn3 is given as

Entity 'Entity_name' is
port (Signal_name, Signal_name, Signal name;
mode type;
Signal_name, mode type;)
end entity

Entity 'entity_name' is
port (Signal name, Signal name; Signal name;
mode type;
Signal_name: mode type);
end entity_name.

VHDL is a strongly typed language because every object in a VHDL Construct has a type and can only hold values of that type. The type of an object is fixed in its declaration.

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The fundamental differences b/w the Entity declaration and Component declaration is

(1) Entity declaration as a Separately Compilable library unit can never occur in another library unit.

whereas the Component declaration can occur inside the library unit

2. An entity declaration declares something that really exist in the design library whereas a component declaration merely declares a template that does not really exist in the design library.

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procedures are also used to encapsulate behaviour code which can be used by different processes. The behaviour of the procedure is the same for all calls and even different parameters.

2c. Purpose that procedure serve in VHDL.

soln

procedure may serve as a purpose for isolating the complicated part/section of the process statement. This helps to add to the functional breakdown of the behaviour and makes the process statement easier to read.

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2. procedure may be used to encapsulate behaviour code, so that it can be used by different processes. The behaviour of the procedure is the same for all calls and different in parameters.

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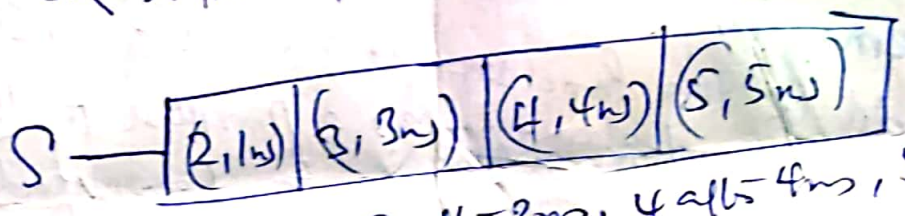
process statement assigns value/time pairs to signal drivers.

(ii) S <= 2 after 1ns, 3 after 3ns, 4 after 4ns, 5 after 5ns.



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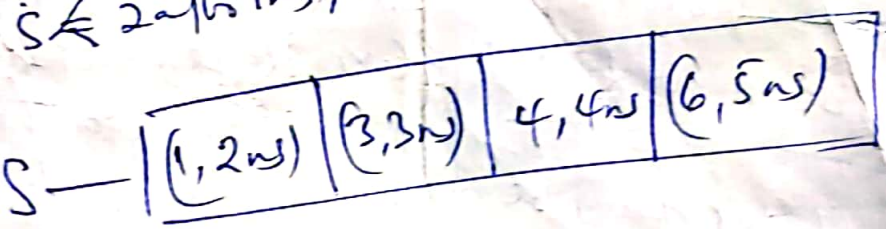
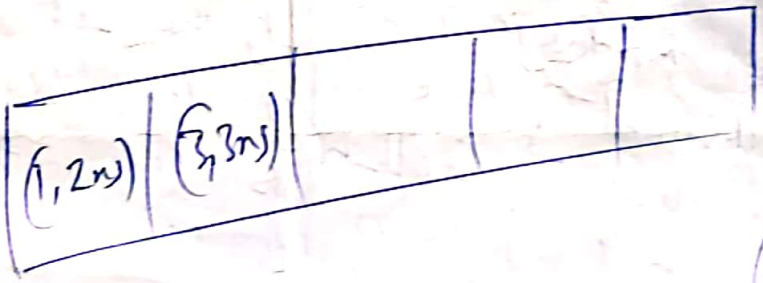
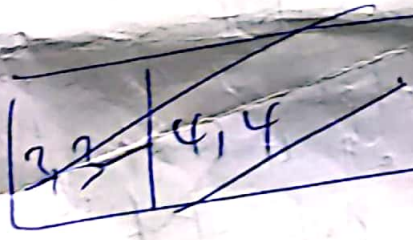
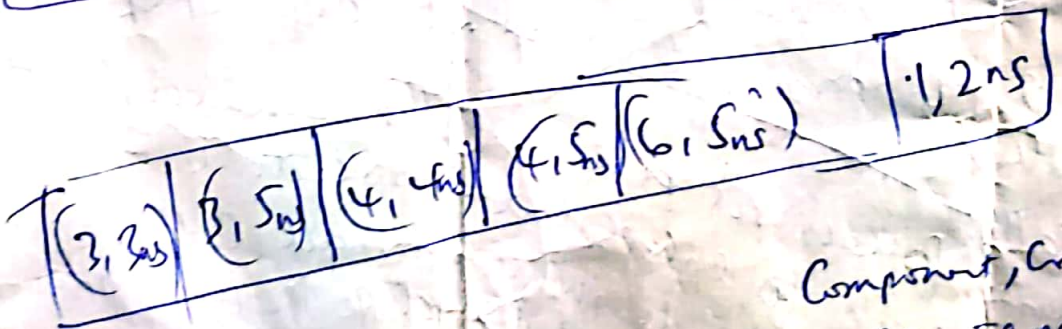




Component identifier is Declared (Port)
end component

Signal name, Signal name:
mode type;
Signal name: mode type
end component name





next statement

next — (condition) loop
statement;

Component, Compnet name
Port(Signal name, Signal name:
mode type;
Signal name, mode type));
end component name;

Variable <= Signal name <= value;