CPE522

Computer-aided design (CAD) of digital Circuits

* Computer-aided design is the use of computer to aid creation, modification, analysis, or optimization of a design such as a logic circuit
* It has a software to perform this task.
* The CAD software is used to increase the productivity of the designer, Improve the quality of the design, Improve communication through documentation, and to create a data base for manufacturing.
* CAD outputs is often in form of electronic files for print, machining or other manufacturing operations
* CAD tools used for a particular tasks are
  (i) design Entry
  (ii) Simulation
  (iii) Synthesis and Optimization
  (iv) physical design.

What is CAD tool in VHDL?

Tool - provides a collection of symbols that represent gates of various types with different inputs and outputs

A library in VHDL, a logic expression is called a simple assignment statement.

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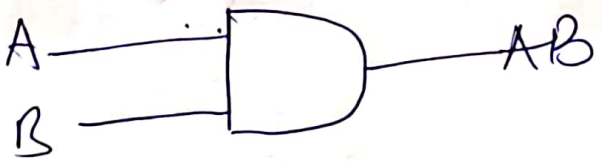
What is logic circuit design?

— These are basic organizing of the circuitry of a digital computer Per Calculations using components called logic gates, which are made up of integrated circuits that receive an input signal, process it, and change it into an output signal.

What is logic circuit in computer?

Computer often chain logic-gate together, by taking the output from one gate and using it as the input to another gate. We call that a logic circuit. Circuit enables computers to do more complex operations than they could accomplish with just a single gate. eg A diagram where two inputs A and B go into an AND gate as shown below



How is logic circuits used in the computer.

Computers uses logic gates to transform the 1s and 0s from input wires. A logic gate accepts inputs and outputs a result based on the state.

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What are constraints in VHDL?

Global constraints include period constraints for each clock (PERIOD), set up times for each input (OFFSET_IN), and clock-to clock constraints for each output (OFFSET_OUT). You can enter timing constraints using the Create Timing constraints process in project Navigator.

What is logic synthesis in VHDL?

— is a process in which a program is used to automatically convert a high-level textual representation of a design (specified using a HDL at the register transfer level (RTL) of abstract (in) into equivalent registers and Boolean equation

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Synthesis tools.

What is Synthesis tool?

The task of a synthesis tool is to analyze a VHDL description and infer what hardware elements are represented and how they are connected. A tool cannot infer hardware from any arbitrarily written VHDL model. Instead, we need to write models in a synthesis style that is recognized by the tool.

What is VHDL Synthesis?

Synthesis is a process where a VHDL is compiled and mapped into an implementation technology such as an FPGA or an ASIC. Not all constructs in VHDL are suitable for synthesis. For example, most constructs that explicitly deal with timing such as wait for 10 ns; are not synthesizable despite being valid for simulation.

How does a Synthesis tool work?

In computer engineering, logic synthesis is a process by which an abstract specification of desired circuit behavior, typically at register transfer level (RTL), is turned into a design implementation in terms of logic gates, typically by a computer program called a synthesis tool.

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Synthesis Optimization Using VHDL

Part 2

The Optimization can be performed at the code level or during the synthesis. The fully optimized design is that which has met the area and timing requirements. The optimization at the RTL level can be achieved by modifying the code to meet the intended functionality

Mapping in VHDL?

Modules communicate with the outside world through the entity. Port map is the part of the module instantiation where you declare which local signals the module's inputs and outputs shall be connected to.

A VHDL module created for running in a simulator usually has no input or output signals.

What are the libraries in VHDL?

VHDL libraries allow you to store commonly used packages and entities that you can use in VHDL files. (A VHDL package file contains common design elements that you can use in the VHDL file source files that make up your design.

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What is IEEE library in VHDL?

The IEEE1164 standard (Multivalue Logic System for VHDL Model Interoperability) is a technical standard published by the IEEE in 1993, it describes the definitions of logic values to be used in electronic design automation for

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What is VHDL design?

VHDL stands for very high-speed integrated circuit hardware description language. It is a programming language used to model a digital system by dataflow, behavioral and structural style of modelling. This language was first introduced in 1981 for the department of Defense (DOD) under the VHSIC program.

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What do you mean by top down design? (1)

Top down is a programming style, the main-stay of traditional procedural languages, in which design begins by specifying complex pieces and then dividing them into successively small pieces. In a bottom-up approach, the individual base elements of the system are first specified in great detail.

What is top-down and bottom-up approach in VHDL?

These traditional bottom-up designs are used to develop new structural, hierarchical design methods.

Top-Down Design: The desired design-style of all designs is the top-down design as it offers advantages like early testing, easy change of different technologies, a structured system design etc.

Top-down approach (also known as stepwise design) is essentially the breaking down of a system to gain insight into the subsystems that make it up. In a top-down approach an overview of the system is formulated, specifying but not detailing any first-level subsystems. Each subsystem is then refined in yet greater detail, sometimes in many additional subsystem levels, until the entire specification is reduced to base elements. Once these base elements are recognised then we can build these as component modules. Once they are built we can put them together, making the entire system from these individual components.

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A top-down approach (also known as stepwise design and stepwise refinement and in some cases used as a synonym of decomposition) is essentially the breaking down of a system to gain insight into its compositional sub-systems in a reverse engineering fashion. In a top-down approach an overview of the system is formulated specifying but not detailing, any first-level subsystems.

Each subsystem is then refined in yet greater detail, sometimes in many additional subsystem levels, until the entire specification is reduced to base elements. Once these base elements are recognised then we can build these as complete modules. Once they are built we can put them together, making the entire system from these modular components.

* Top-down design - in which design begins by specifying complex pieces and then dividing them into successively smaller pieces.

What is Simulation and why it is used?

Simulation Modeling solves real-world problems safely and efficiently. It provides an important method of analysis which is easily verified, communicated, and understood.
Unlike physical modeling such as making a scale copy of a building, simulation modeling is computer based and uses algorithms and equations.

What is Simulation example

A computer simulation (or "sim") is an attempt to model a real-life or hypothetical situation on a computer so that it can be studied to see how the system works.
A good example of the usefulness of using computers to simulate can be found in the field of network traffic simulation.

What is simulation and its types.

Simulator Types: A simulator is a device, computer program, or system that performs simulation.
A simulation is a method for implementing a model over time.

1. We are three (3) types of Commonly used Simulation
(1) Live: Simulation involving real people operating real Systems.
- Involve individuals or groups.
- May use actual equipment
- Should be close to replicating the actual activity
- Should provide a similar area of operations.

2. Virtual: Simulation involving real people operating Simulated Systems. Virtual simulations inject Humans-in-the loop in a central role by exercising
- Motor control skills (eg flying an airplane).
- Decision skills (eg committing fire control resources back)
- Communication skill (eg members of a C4I team).

3. Constructive: Simulation involving Simulated ~~Systems~~. ~~Real~~ people operating Simulated Systems. Real People can stimulate (make inputs) but are not involved in determining Outcomes. Constructive Simulations offers the ability to:
- Analyze Concepts
- Predict possible Outcomes
- Stress large Organizations.
- Make measurements
- Generate Statistics
- Perform analysis

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What are formal verification techniques?

Formal verification of software programs involves proving that a program satisfies a formal specification of its behavior. Subareas of formal verification include deductive verification, abstract interpretation, automated theorem proving, type systems, and lightweight formal methods.

Why formal verification is important?

Formal verification takes the guesswork out of this, and eliminates the risk of bugs in the silicon. These give the tools a formal basis to reason about the design, and to identify violations that signify problems or bugs.

What is meant by formal verification?

In the context of hardware and software systems, formal verification is the act of proving or disproving the correctness of intended algorithms underlying a system with respect to a certain formal specification or property, using formal methods of mathematics.

Formal verification is essentially concerned with identifying the correctness of hardware and software design operations. Because verification uses formal mathematical proofs, a suitable mathematical model of the design must be created.

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What is RTL Coding in VHDL?

RTL is an acronym for register transfer level. This implies that your VHDL code describes how data is transformed as it is passed from register to register. The transforming of data is performed by the combinational logic that exist between the registers.

What is RTL code example?

Module instances are also example of Synthesizable RTL statements.

How do you write RTL?

In a right-to-left, top-to-bottom script (commonly shortened to the right to left or abbreviated RTL), writing starts from the right of the page and continues to the left, proceeding from top to bottom for new lines.

How do we Code VHDL?

There are the following three ways

1) Entity: The Entity is used to specify the input and output ports of the Circuit.
2. Architecture: Architecture is the actual description of design, which is used to describe how the Circuit operates.
3. Configuration.

Ch 5 ①

The Simulation Speed (or the Simulation ratio) is how fast RoboDK simulates a real motion. A simulation ratio of 1 means that a movement that takes 1 second on a real robot will take 1 second to simulate. That means that a program that takes 5 seconds to execute on the real robot it will be simulated in 1 second.

What is Simulation run time?

The flow of time is only between events and is not continuous. Therefore, simulation time is not allowed to progress during an event, but only between events. In fact, the simulation time is always equal to the time at which the current event occurs.

Does time scale affect Simulation runtime?

The time scale compiler directive specifies the default time unit and precision to all design elements that follow this directive. It does not speed up the simulation time. So changing the timescale will have no effect on the simulation speed.

How do I run Simulation faster?

~~Start~~ tips to make your simulation run faster.

1. Vectorize the program.
2. Profile the program to identify the trouble spots.

3. Allocate arrays that are used in a loop.
4. Reduce the size of the parameter grid
5. Reduce the number of simulations.
6. Distribute independent computation.