DEPARTMENT OF COMPUTER ENGINEERING,
UNIVERSITY OF BENIN, BENIN CITY
2016/2017 SESSION 2ND SEMESTER EXAMINATION

28/07/2017

CPE522: SYSTEM PROGRAMMING Time: 3hours

ATTEMPT FIVE (5) QUESTIONS ONLY

1a

```
architecture Behavioural of JK_Flipflop is
--signal declaration.
signal qtemp, qbartemp : std_logic := '0';
begin
Q <= qtemp
Qbar <= qbartemp

process(clk,reset)
begin
if(reset = '1';) then
 qtemp <= '0';
 qbartemp <= '1';
elseif(rising_edge(clk) ) then
if(j= '0' and K = '0') then
 NULL;
else(J= '0' and k= '1') then
 qtemp <= '0';
 qbartemp <= '1';
elseif(J= '1' and k = '0') then
 qtemp <= '1';
 qbartemp <= '0';
else
 qtemp < not temp;
 qbartemp <= not qbartemp;
end if;
end if;
end process;
end Bebavioral;
```

i. Write the form of the process statement used in the behavioural description
ii. Rewrite the description using the wait statement
iii. Write and explain the form of the wait statement used
iv. Rewrite the general form of the process statement for your answer to Qn1aii
v. What does the NULL statement, as used in the process statement, do?
vi. Write the general form of the conditional control used in the process statement

(16marks)

b. function and procedure are classified as subprograms in VHDL. Explain features that differentiate them

(4marks)

2a. Discuss the special characteristics of VHDL data pathways.

b. Consider the process statement of Qn2b

```
P1: Process
Variable B: integer := 1;
Begin
Loop1:
For A in 1 to 12 loop
B:= 400;
Loop2: loop
If B< (A**2)
Exit loop2;
End if;
B:=B/A;
End loop loop2;
End loop loop1;
Wait;
End process
```

i. Rewrite the process statement using the next statement.

ii. Write the syntax for the next statement. (15 marks)

c. Briefly discuss the 'wait statement as used in VHDL. (5 marks)

3a. Write and explain the general syntax for a variable assignment (2 marks)

ai. List and define the basic concepts of hardware structure (3 marks)

b. Consider the device fig. Qn3b

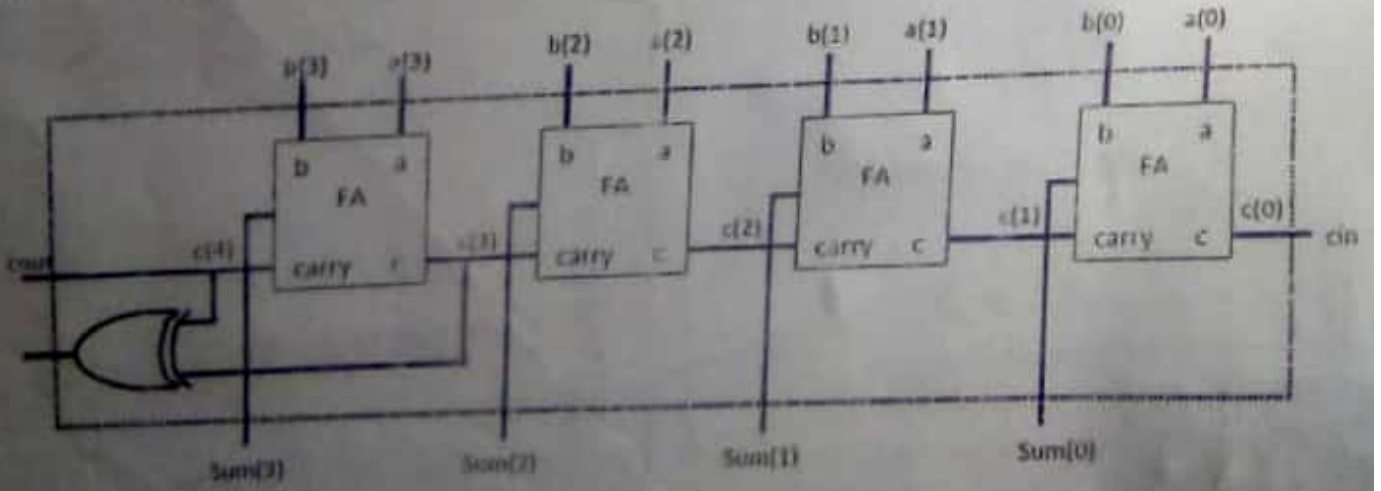


Fig. Qn3b

i. Write a VHDL description for the components used as (a) building block(s) for the digital device of fig.Qn3b using behavioural description for architecture body.

ii. Write a structural description for fig. Qn3b using positional association for the component instantiation statement

(15 marks)

4a. Given the function $f(X, Y, Z) = X\bar{Y}Z + \bar{X}Y\bar{Z} + \bar{X}YZ + XY\bar{Z}$

i Sketch the logic circuit represented by the logic function.

iii. the entity declaration of the logic device

b. Write the architecture behavioural description for the device using concurrent signal assignment. *(14 Marks)*

5a.i. Sketch and define the components of a finite state machine *(6 marks)*

ii. Design, using ROM, a square look up table for $F(x) = \begin{cases} x^3, & \text{for } 0 \le x \le 7 \\ 0, & \text{Otherwise} \end{cases}$

b. What is a look up table? *(12 Marks)*

ii. What is a programmable logic device?

Distinguish between a PAL, ROM and PLA. *(8 Marks)*

6a. Table Qn.6a below is the truth table of a code converter. Design a PAL logic implementation of the table. *(14 Marks)*

b. Outline the advantages of PLDs. *(6 Marks)*

7a. The state diagram of a service machine is as shown in Fig.Qn7a

i. Generate a state table for the machine

ii. Design a FSM

iii. What does this machine do? *(15 Marks)*

b. Outline the advantages and disadvantages of FSMs *(5 Marks)*

Table Qn.6a: Code converter truth table

A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	1	1	1	0
0	1	1	0	1	0	1	0
0	1	1	1	1	0	1	1
1	0	0	0	1	0	0	1
1	0	0	1	1	0	0	0
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

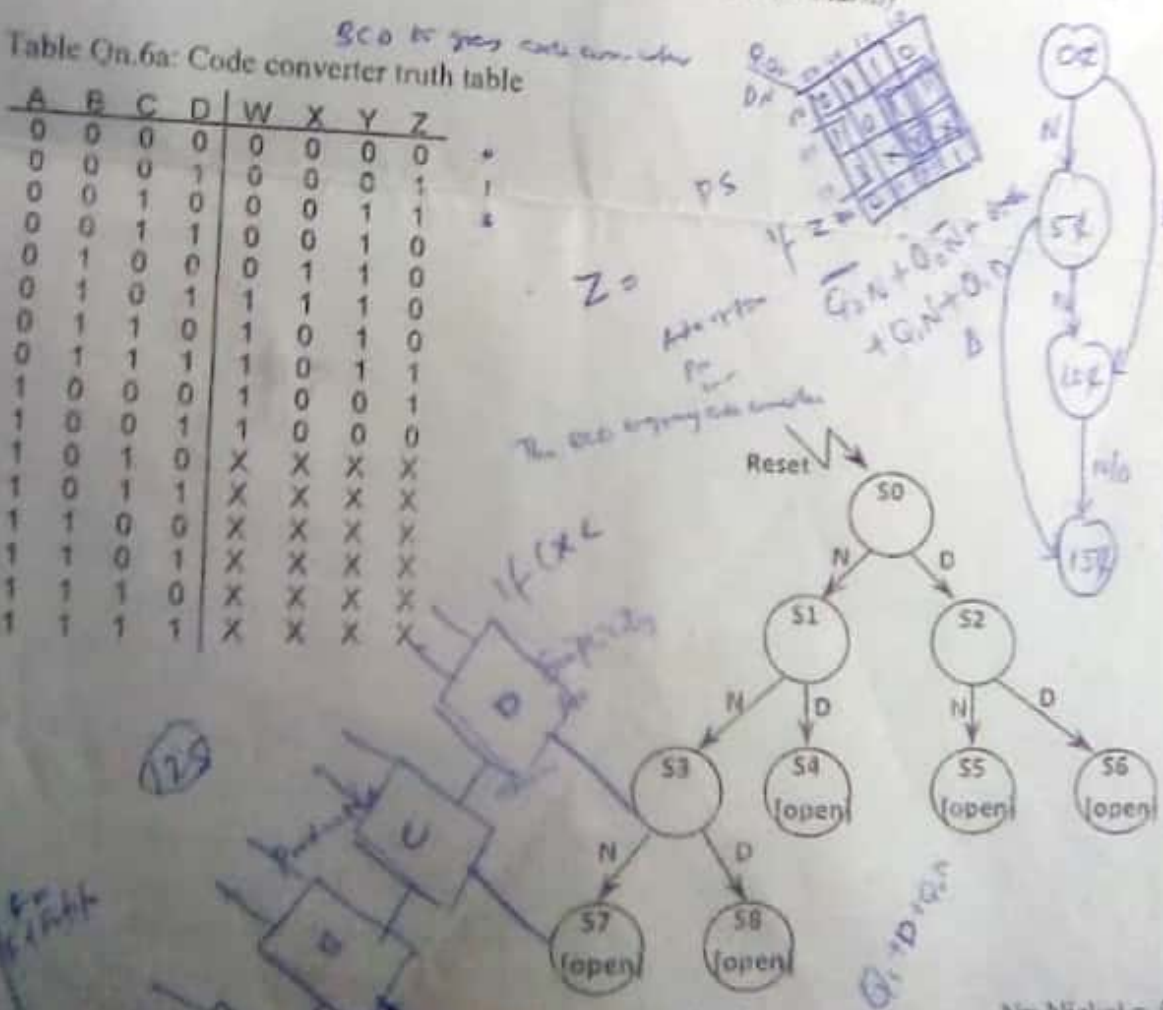


Fig.Qn.7a

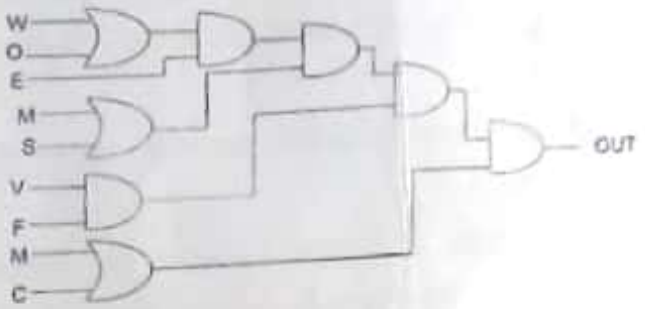
N= Nickel = 5 Cents

D = Dime = 10 Cents

DEPARTMENT OF COMPUTER ENGINEERING
FACULTY OF ENGINEERING
UNIVERSITY OF BENIN
SECOND SEMESTER EXAMINATION (2018/2019)
CPE522: DIGITAL SYSTEM DESIGN WITH VHDL 3HOURS

INSTRUCTIONS: ANSWER FIVE QUESTIONS IN ALL AND ATLEAST ONE FROM EACH SECTION

Q1. a) Consider the gate diagram below:

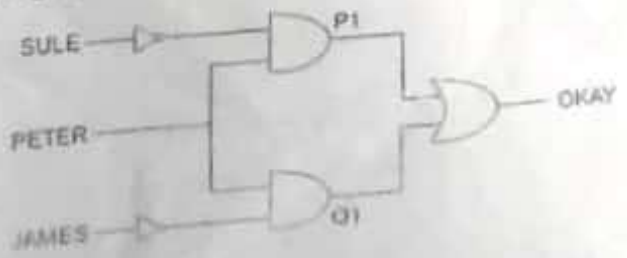


i) Write a HDL program for the above device.
ii) The output obtained from (i) above, should be convene to five different locations.

b) If given constants "true" and "false" which can be used as fixed buses for 1's or 0's.
i) Implement the HDL stub file for the constants in (b). Suppose we named the gate "WALLOP"
ii) Draw the gate-diagram.

(c) If a chip gate named "WIDGET" has a multiple outputs. Write an HDL stub file for defining the chip. (14marks)

Q2. Consider the logic circuit of fig Qn 2(a) below:



(i) Generate the truth table for the logic device
(ii) From the truth table, generate the logic function for the logic device
(iii) Write a HDL stub file for the device (14marks)

Q3. Explain briefly the following terms in relations to the structured design:

i) Schematic circuit capture
ii) Design process (simulation, synthesis)
iii) Structural design decomposition
iv) Design level (14marks)

SECTION B

a) Lists four VHDL capabilities that you know (2marks)

b) Write and explain the general syntax of the architecture body (4marks)

c) Write a VHDL description for a 4:1 multiplexer using structural modelling (5marks)

d) Write a VHDL program for an exclusive NOR gate using with-select statement (3marks)

a) Write a VHDL description for a full subtractor. Develop the sum of products of the Boolean equation (8marks)

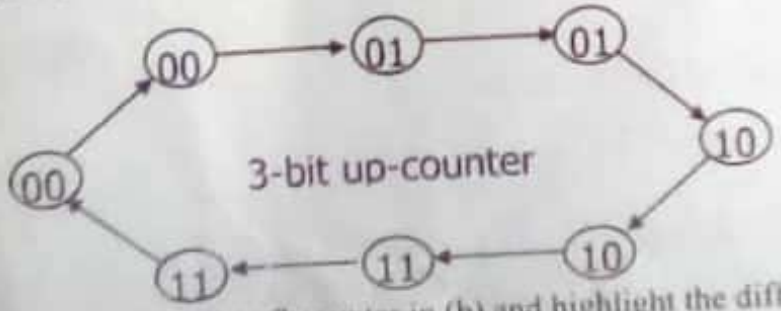
b) Write a VHDL description for an XOR gate using when-else statement (3marks)

c) Write a VHDL program for RS flip-flop using behavioural modelling (3marks)

SECTION C

a) With a suitable diagram describe the Mealy and Moore models of Finite State Machines (5marks)

b) Use the classical design method to design a 0-to-7 counter (Tip clearly show the state diagram, transition table etc] (7marks)



c) Use VHDL to redesign design the 0-to-7 counter in (b) and highlight the differences in the two design approaches (8marks)

Q7. a) An alternative to state diagram representation for FSMs is the algorithm state machine. Discuss (5marks)

b) Consider, the VHDL code below. Manually synthesize the digital system (7marks)

```
ARCHITECTURE a3 OF mux2_1 IS
    BEGIN
    OUT <= ((B AND NOT (SEL)) OR (AAND SEL));
END a3;
```

(8marks)

c) Consider, the VHDL code below
i. Sketch the state diagram
ii. Briefly describe the digital system

```
ARCHITECTURE a1 OF mux2_1 IS
        P1: PROCESS (sel, in0, in1)
BEGIN
IF (sel = '0') THEN
 yout <= in0;
 ELSE
 yout <= in1;
 END IF;
 END P1;
 END a1;
```

GOODLUCK

DEPARTMENT OF COMPUTER ENGINEERING,
UNIVERSITY OF BENIN, BENIN CITY
2017/2018 SESSION 2ND SEMESTER EXAMINATION

CPE522: SYSTEM PROGRAMMING Time: 3hours 28/10/2018

ATTEMPT FIVE (5) QUESTIONS ONLY

1a. A full sub-tractor implements the arithmetic equation

$D_iB_{out} = A - B - B_{in}$

Where D_i and Bout denote the difference and borrow functions respectively. Derive a canonical sum-of-products Boolean equation for each output.

i. Draw the logic circuit.
ii. Write the entity declaration of the logic device.
iii. Write the architecture behavioural description for the device.
iv. Write the structural description for the device. (12marks)

b. Write an entity declaration for a device with the following ports:

Port D is a 12-bit bus, input only
Port OE and CLK are each input bits
Port AD is a 12-bit, bi-directional bus
Port A is a 12-bit bus, output only
Port INT is a three-state output
Port AS is an output only (4marks)

c. State the general form of an object declaration and explain. (4marks)

2a. List and explain the major constructs in VHDL (12marks)

b. A two-to-one multiplexer has three data inputs, a, b, and c and two select control input, X and Y. The multiplexer has a single output Z. If X = 1, Z is equal to a. If Y = 1, Z is equal to b otherwise Z is equal to c

i. Write an entity declaration for the multiplexer named mux. Express the process statement for the multiplexer. (5marks)

c. State the purposes that procedures serve in VHDL (3marks)

3a. List the characteristics of a process statement (4marks)

b. Consider the process statement below

```
Signal S: Integer =0.
P1: PROCESS
Begin
S<= transport 1 after 1ns;
S<= transport 1 after 1ns, 2 after 3ns, 4 after 4ns, 7 after 5ns;
S<= transport 2 after 2ns;
S<= transport 3 after 5ns, 4 after 4ns, 4 after 5ns, 6 after 10ns;
Wait
End Process;
```

i. What does this process statement do?
ii. What is the effect of the process statement on S? (6marks)

A vhdl program controls a LED using a switch. When the switch is toggle to one (1) the reading (sw
will turn on when toggle to zero the reading (switch) will turn off.

i. Briefly explain the behavior of the device described.

ii. Sketch the device described

iii. Write the architecture description of the device using concurrent signal assignment statement

4a. Consider the process statement of Qn4a (10marks)

```
P1: Process
Variable B: Interger:= 1;
Begin
Loop1
For A in 1 to 12 loop
B:= 400;
Loop2: loop
If B< (A**2)
Exit loop2;
End if;
B:= B/A;
End loop loop2;
End loop loop1;
Wait;
End process;
```

i. Rewrite the process statement using the while statement.

ii. Write the syntax for the while statement.

iii. Write the general form of the process statement used (10marks)

b. Function and procedure are classified as subprograms in VHDL. Explain the features that differentiate them (3marks)

c. Write the general form of a VHDL function (3marks)

i. Write a VHDL "function" description for a 3-input exclusive OR function (4marks)

5ai. Design, using ROM, a square look up table for $F(x) = \begin{cases} 2x^2, & for\ 0 \le x \le 5 \\ 0, & Otherwise \end{cases}$ (12marks)

ii. What is a look up table?

bi. Outline the advantages of PLDs (8marks)

ii. Distinguish between a PAL, ROM and PLA

6a. The state diagram of a service machine is as shown in Fig Qn7a

i. Generate a state table for the machine

ii. Design a FSM for the service machine (15marks)

iii. What does this machine do? (5marks)

b. Outline the advantages and disadvantages of FSMs

7. Consider a door combination lock FSM in Fig. Q7 with the following specification:

- When a user punches in 3 values in sequence, the door should open; if there is an error the lock must be reset; once the door opens the lock must be reset
- Inputs consist of sequence of input values, reset
- Outputs consists of door open/close
- Memory of the system must remember combination or always have it available as an input

(a) i. Identify the number of states

ii. Describe each of the states and the corresponding transitions

identify the input and output of the FSM (5marks)

(b) Explain how you can come up with an optimal encoding scheme for the states (5marks)

(c) Develop a state transition table for the FSM (10marks)

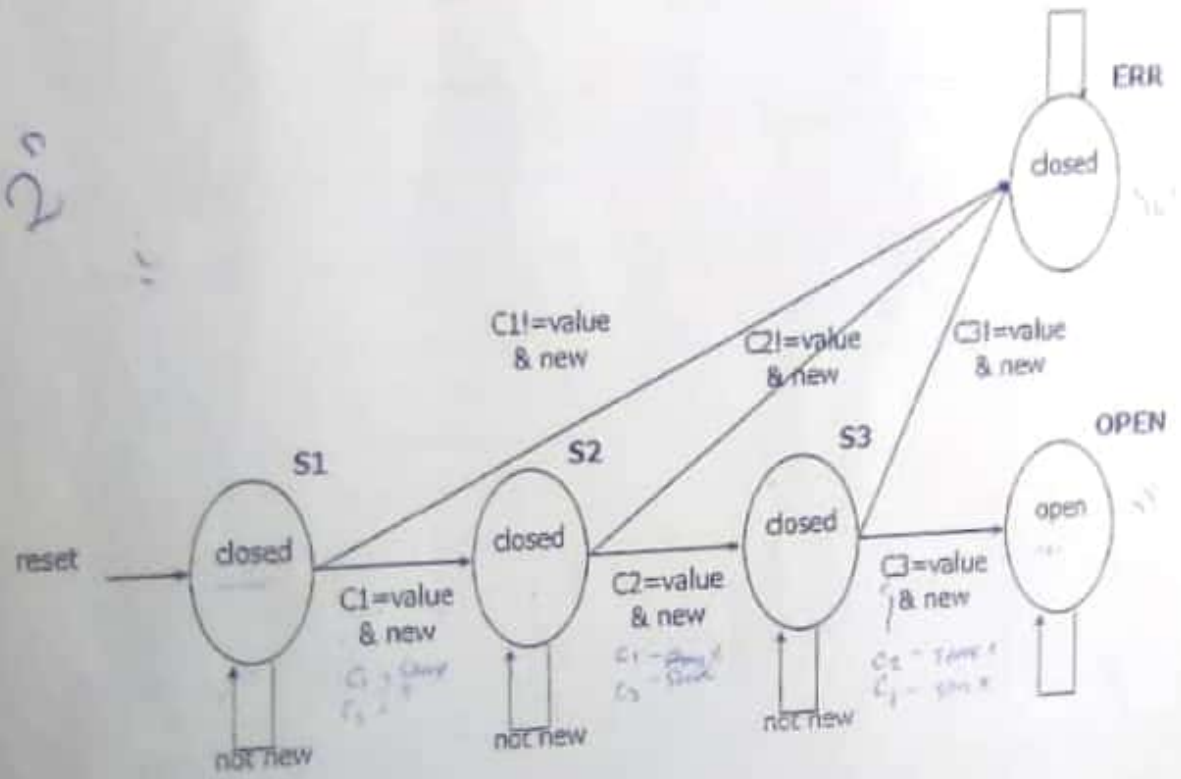


Fig. Q7