PUBLIC ENGAGEMENT ACTIVITY

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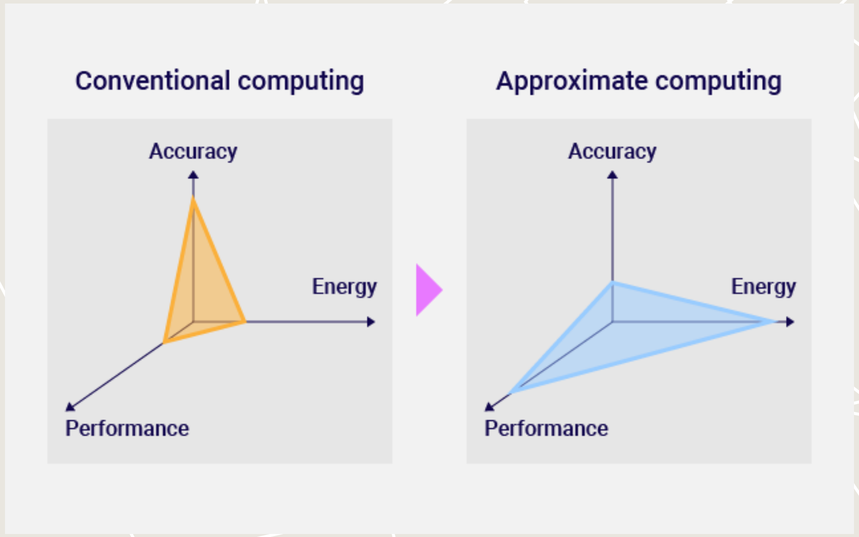
ABOUT THE PROJECT

- **Implement an Arithmetic Unit Utilizing Approximate Computing into RISC-V SoC.**
- **Supervisor: Mr. Neil Powell**



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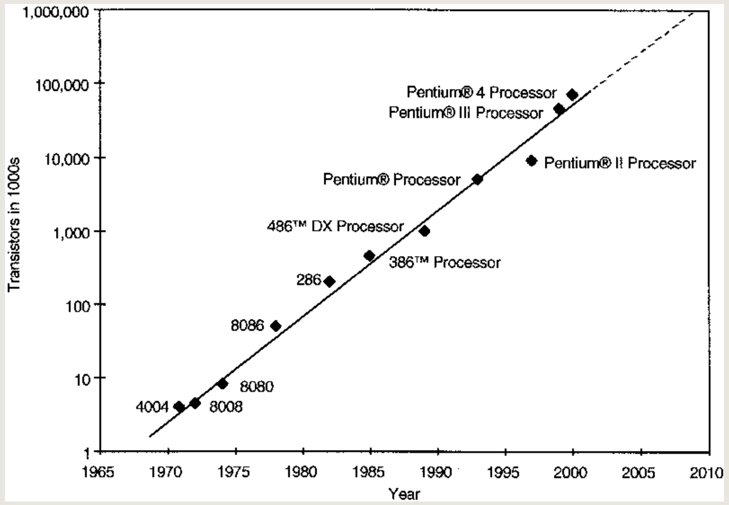
BACKGROUND & MOTIVATION

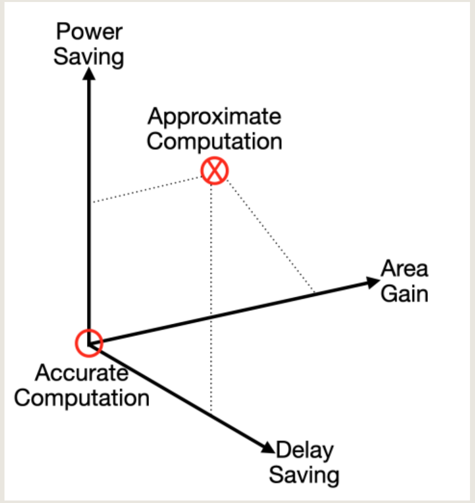
CONTEXT Growing demand for high-performance computing in machine learning, computer vision, and multimedia processing.

CHALLENGE Traditional computing approaches are limited by the slowing of Moore's Law.

OPPORTUNITY Approximate computing allows controlled errors for faster and energy-efficient computation.

IMPORTANCE Enables energy-efficient digital systems, suitable for error-tolerant applications like image processing.





ARCHITECTURE

8-bit Approximate MAC Unit

Input Fetch Stage

- **8-bit operands (A and B)** for multiplication
- Inputs are passed into the **fuzzy memoization block** to check for stored approximate results

Fuzzy Memoization Block

- **Caches previous computations** to avoid redundant calculations
- Uses **Hamming distance** to find a similar previously stored input-output pair.
- If a match is found, **cached result is used** instead of recalculating.

Approximate Multiplication Stage

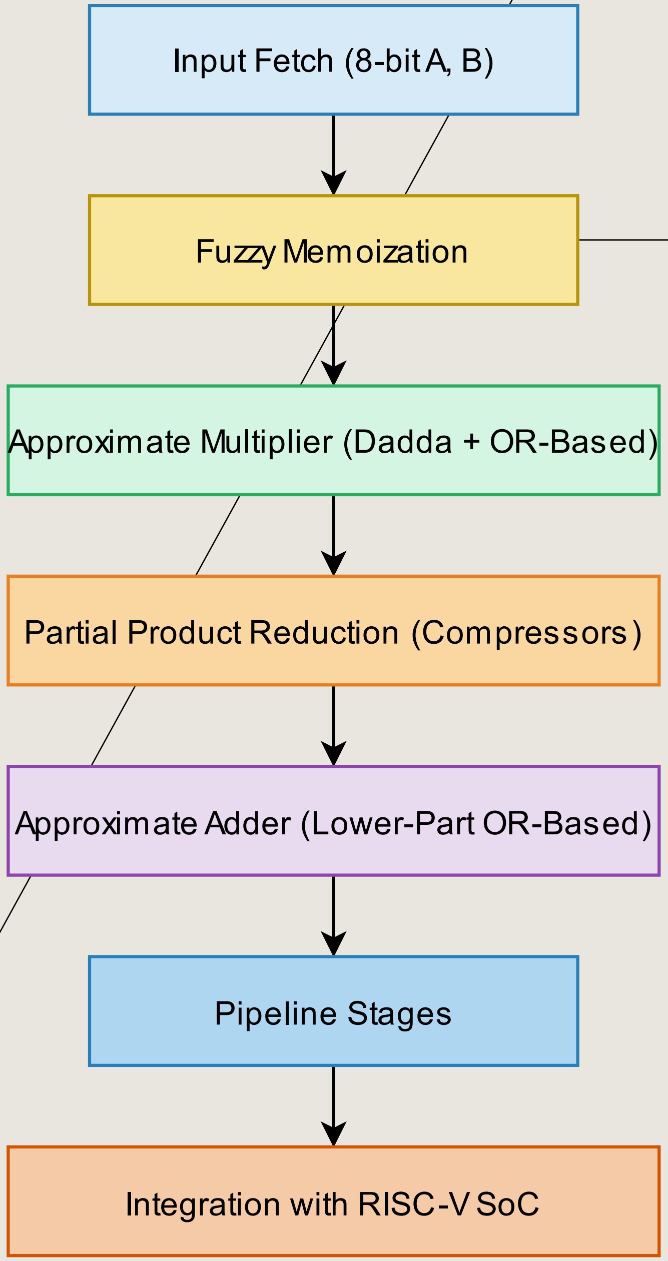
- Lower-Part OR-based Approximate Multiplier:
  - MSB (Most Significant Bits) handled with a Dadda Multiplier
  - LSB (Least Significant Bits) approximated using OR-based logic

Partial Product Reduction Stage

- Uses compressor-based approximate multipliers

Approximate Addition Stage

- Accumulation performed using Lower-Part OR-based Approximate Adders



Input Fetch (8-bit A, B)
Fuzzy Memoization
Approximate Multiplier (Dadda + OR-Based)
Partial Product Reduction (Compressors)
Approximate Adder (Lower-Part OR-Based)
Pipeline Stages
Integration with RISC-V SoC

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REAL-WORLD PROBLEM ADDRESSED

Energy-Efficiency

• Reduced power consumption by allowing controlled errors
• Lower energy requirements make it suitable for battery-powered devices

Traditional computation

• Precise arithmetic units consume more power and area
• High accuracy but less energy-efficient

Approximate computing

• Trades off accuracy for efficiency, reducing power and area
• Suitable for error-tolerant applications like image processing and AI

Ideal tasks

• Image processing (denoising, compression)
• Machine learning
• Signal processing in embedded systems

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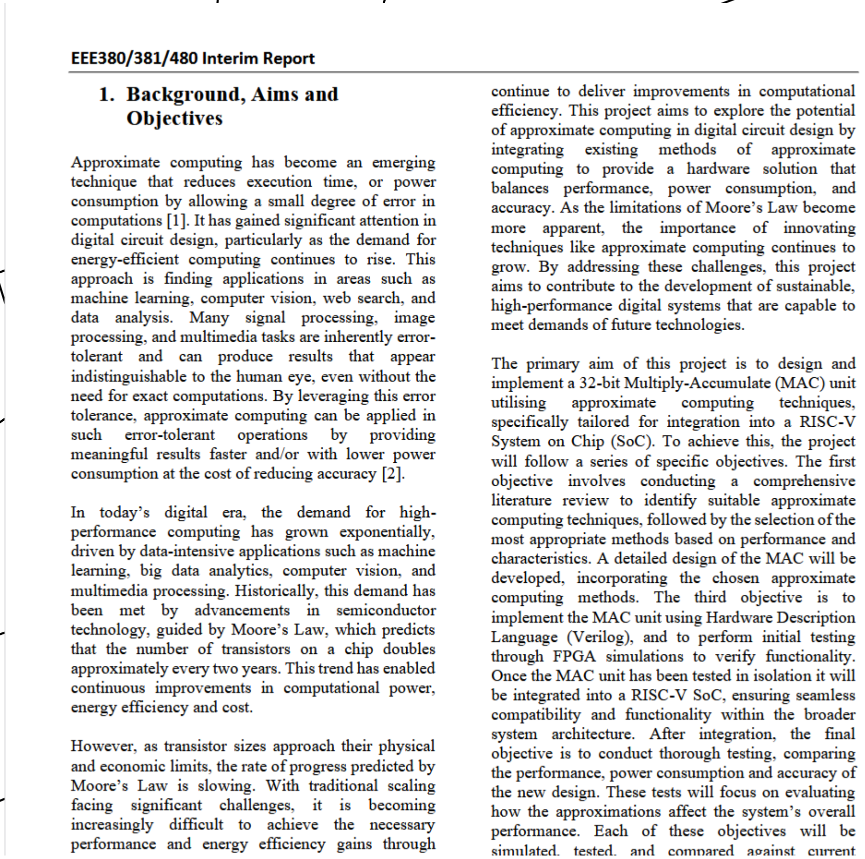
AIMS & OBJECTIVES



EEE380/381/480 Interim Report

1. Background, Aims and Objectives

Approximate computing has become an emerging technique that reduces execution time, or power consumption by allowing a small degree of error in computations [1]. It has gained significant attention in digital circuit design, particularly as the demand for energy-efficient computing continues to rise. This approach is finding applications in areas such as machine learning, computer vision, web search, and data analysis. Many signal processing, image processing, and multimedia tasks are inherently error-tolerant and can produce results that appear indistinguishable to the human eye, even without the need for exact computations. By leveraging this error tolerance, approximate computing can be applied in such error-tolerant operations by providing meaningful results faster and/or with lower power consumption at the cost of reducing accuracy [2].

In today's digital era, the demand for high-performance computing has grown exponentially, driven by data-intensive applications such as machine learning, big data analytics, computer vision, and multimedia processing. Historically, this demand has been met by advancements in semiconductor technology, guided by Moore's Law, which predicts that the number of transistors on a chip doubles approximately every two years. This trend has enabled continuous improvements in computational power, energy efficiency and cost.

However, as transistor sizes approach their physical and economic limits, the rate of progress predicted by Moore's Law is slowing. With traditional scaling facing significant challenges, it is becoming increasingly difficult to achieve the necessary performance and energy efficiency gains through continue to deliver improvements in computational efficiency. This project aims to explore the potential of approximate computing in digital circuit design by integrating existing methods of approximate computing to provide a hardware solution that balances performance, power consumption, and accuracy. As the limitations of Moore's Law become more apparent, the importance of innovating techniques like approximate computing continues to grow. By addressing these challenges, this project aims to contribute to the development of sustainable, high-performance digital systems that are capable to meet demands of future technologies.

The primary aim of this project is to design and implement a 32-bit Multiply-Accumulate (MAC) unit utilising approximate computing techniques, specifically tailored for integration into a RISC-V System on Chip (SoC). To achieve this, the project will follow a series of specific objectives. The first objective involves conducting a comprehensive literature review to identify suitable approximate computing techniques, followed by the selection of the most appropriate methods based on performance and characteristics. A detailed design of the MAC will be developed, incorporating the chosen approximate computing methods. The third objective is to implement the MAC unit using Hardware Description Language (Verilog), and to perform initial testing through FPGA simulations to verify functionality. Once the MAC unit has been tested in isolation it will be integrated into a RISC-V SoC, ensuring seamless compatibility and functionality within the broader system architecture. After integration, the final objective is to conduct thorough testing, comparing the performance, power consumption and accuracy of the new design. These tests will focus on evaluating how the approximations affect the system's overall performance. Each of these objectives will be simulated, tested, and compared against current

AIMS

- Design and implement an 8-bit Multiply-Accumulate (MAC) unit using approximate computing techniques
- Implement an arithmetic unit utilizing approximate computing into a RISC-V SoC
- Optimize the arithmetic unit for energy efficiency while maintaining acceptable computational accuracy.

OBJECTIVES

- Design and simulate the MAC unit using Verilog on FPGA
- Integrate the MAC unit into a RISC-V SoC
- Evaluate, analyze and compare performance, power consumption, and accuracy against traditional designs
- Validate the design using simulation tools
- Assess the impact of approximation on computational accuracy
- Evaluate the MAC unit's performance in a fuzzy memoized FIR filter for image processing

PROBLEM SPECIFICATION

Problem:

- Balancing accuracy, power consumption, and speed in arithmetic units

Expected Results:

- Enhanced computational efficiency with minimal accuracy loss
- Reduced power consumption and chip area

Methodology:

- Using Verilog for implementation and FPGA simulations
- Implementing Approximate Adders and Approximate Multipliers based on existing designs

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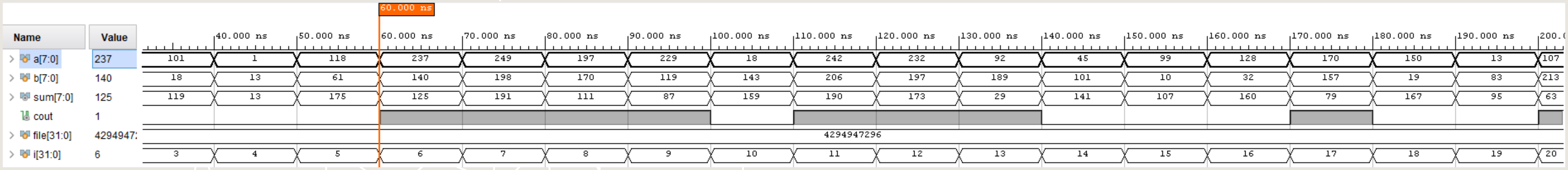
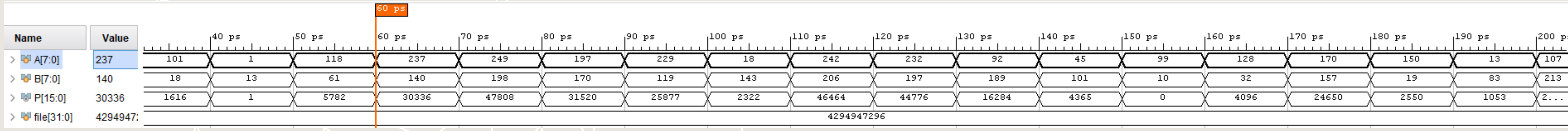


```
60.000 ns

Name        Value       40.000 ns  50.000 ns  60.000 ns  70.000 ns  80.000 ns  90.000 ns  100.000 ns  110.000 ns  120.000 ns  130.000 ns  140.000 ns  150.000 ns  160.000 ns  170.000 ns  180.000 ns  190.000 ns  200.0
a[7:0]      237         101  1    118  237  249  197  229  18   242  232  92   45   99   128  170  150  13   107
b[7:0]      140         18   13   61   140  198  170  119  143  206  197  189  101  10   32   157  19   83   213
sum[7:0]    125         119  13   175  125  191  111  87   159  190  173  29   141  107  160  79   167  95   63
cout        1
file[31:0]  4294947:    4294947296
i[31:0]     6           3    4    5    6    7    8    9    10   11   12   13   14   15   16   17   18   19   20
```

SIMULATION RESULTS - ADDER

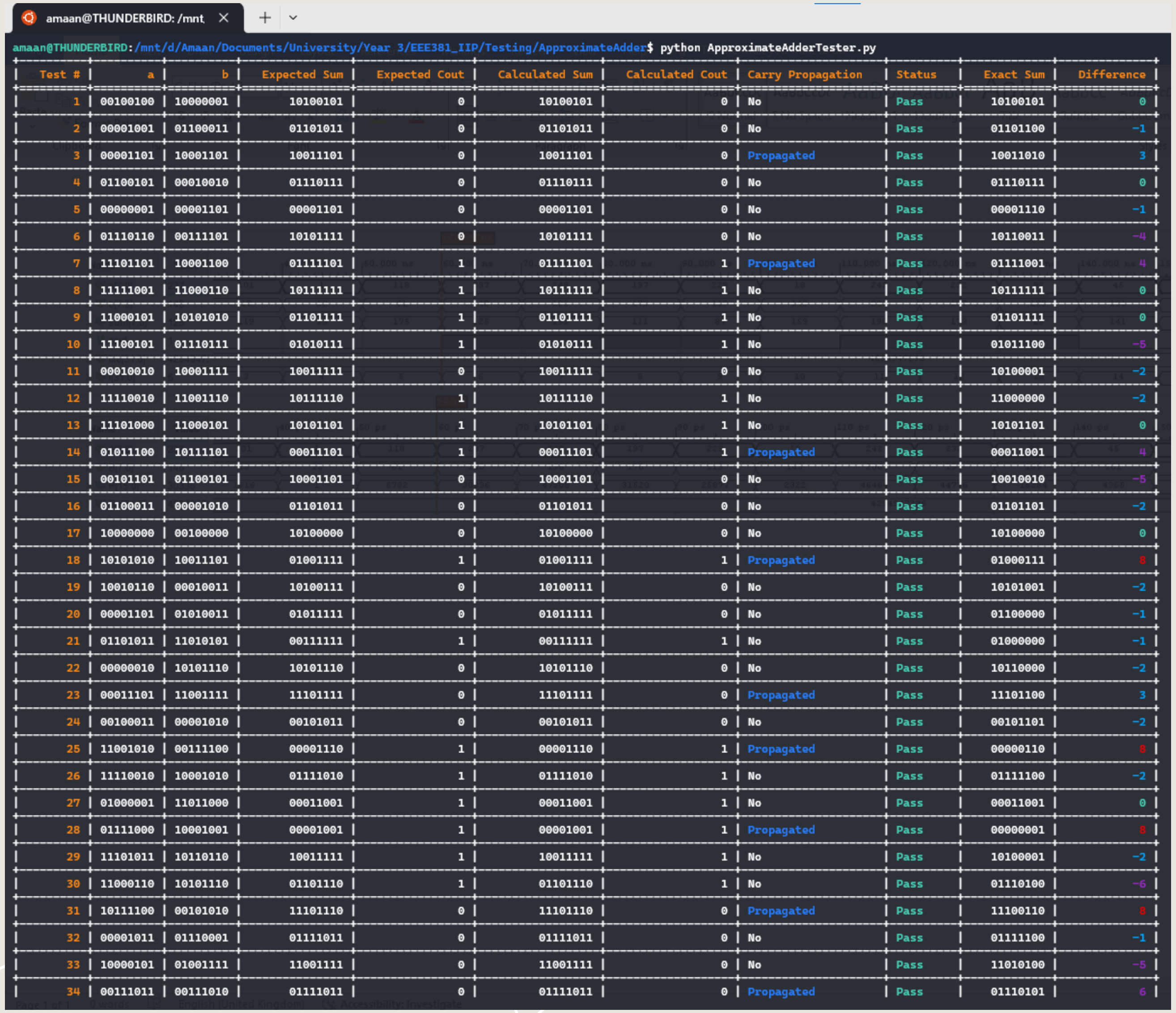


```
                              60 ps
Name        Value        |40 ps  |50 ps  |60 ps  |70 ps  |80 ps  |90 ps  |100 ps |110 ps |120 ps |130 ps |140 ps |150 ps |160 ps |170 ps |180 ps |190 ps |200 p
> A[7:0]    237       101     1     118    237    249    197    229    18     242    232    92     45     99     128    170    150    13     107
> B[7:0]    140       18      13    61     140    198    170    119    143    206    197    189    101    10     32     157    19     83     213
> P[15:0]   30336     1616    1     5782   30336  47808  31520  25877  2322   46464  44776  16284  4365   0      4096   24650  2550   1053   2...
> file[31:0] 4294947:                                                4294947296
```

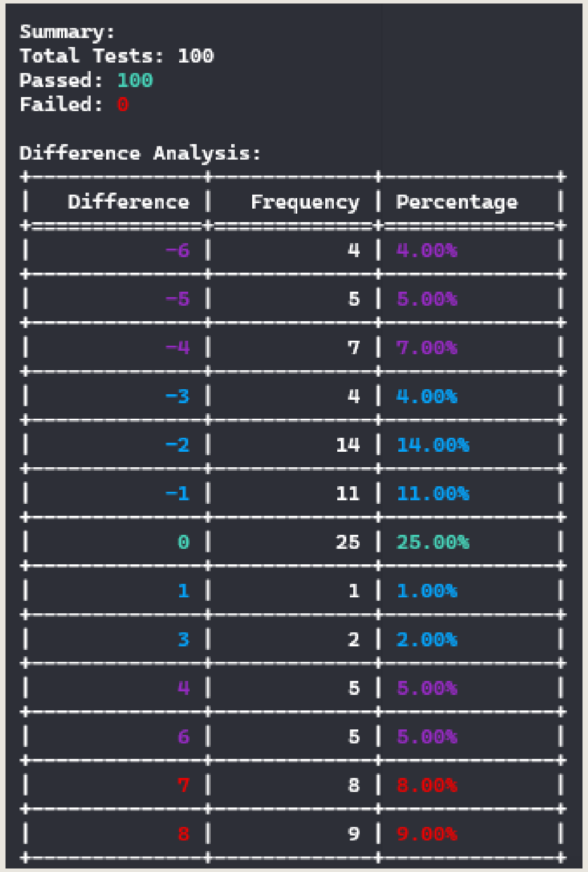
SIMULATION RESULTS - MULTIPLIER

ANALYSIS AND SIGNIFICANCE

UNIT TESTING - ADDER



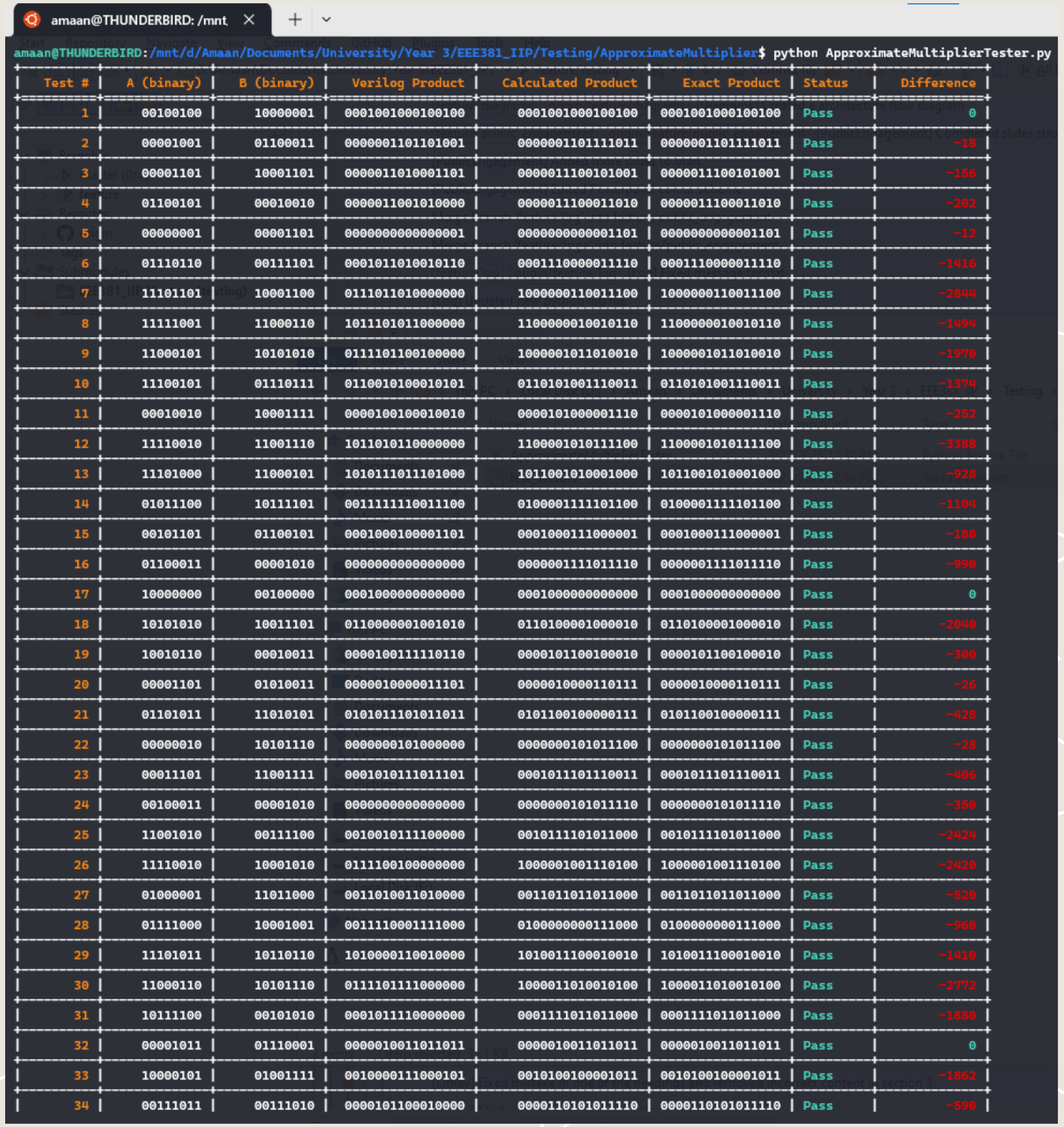
```
amaan@THUNDERBIRD: /mnt
amaan@THUNDERBIRD:/mnt/d/Amaan/Documents/University/Year 3/EEE381_IIP/Testing/ApproximateAdder$ python ApproximateAdderTester.py
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|  Test # |        a |        b |   Expected Sum |   Expected Cout |   Calculated Sum |   Calculated Cout | Carry Propagation  | Status   |   Exact Sum |   Difference |
+=========+==========+==========+================+=================+==================+===================+====================+==========+=============+==============+
|       1 | 00100100 | 10000001 |       10100101 |               0 |         10100101 |                 0 | No                 | Pass     |    10100101 |            0 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|       2 | 00001001 | 01100011 |       01101011 |               0 |         01101011 |                 0 | No                 | Pass     |    01101100 |           -1 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|       3 | 00001101 | 10001101 |       10011101 |               0 |         10011101 |                 0 | Propagated         | Pass     |    10011010 |            3 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|       4 | 01100101 | 00010010 |       01110111 |               0 |         01110111 |                 0 | No                 | Pass     |    01110111 |            0 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|       5 | 00000001 | 00001101 |       00001101 |               0 |         00001101 |                 0 | No                 | Pass     |    00001110 |           -1 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|       6 | 01110110 | 00111101 |       10101111 |               0 |         10101111 |                 0 | No                 | Pass     |    10110011 |           -4 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|       7 | 11101101 | 10001100 |       01111101 |               1 |         01111101 |                 1 | Propagated         | Pass     |    01111001 |            4 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|       8 | 11111001 | 11000110 |       10111111 |               1 |         10111111 |                 1 | No                 | Pass     |    10111111 |            0 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|       9 | 11000101 | 10101010 |       01101111 |               1 |         01101111 |                 1 | No                 | Pass     |    01101111 |            0 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      10 | 11100101 | 01110111 |       01010111 |               1 |         01010111 |                 1 | No                 | Pass     |    01011100 |           -5 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      11 | 00010010 | 10001111 |       10011111 |               0 |         10011111 |                 0 | No                 | Pass     |    10100001 |           -2 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      12 | 11110010 | 11001110 |       10111110 |               1 |         10111110 |                 1 | No                 | Pass     |    11000000 |           -2 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      13 | 11101000 | 11000101 |       10101101 |               1 |         10101101 |                 1 | No                 | Pass     |    10101101 |            0 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      14 | 01011100 | 10111101 |       00011101 |               1 |         00011101 |                 1 | Propagated         | Pass     |    00011001 |            4 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      15 | 00101101 | 01100101 |       10001101 |               0 |         10001101 |                 0 | No                 | Pass     |    10010010 |           -5 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      16 | 01100011 | 00001010 |       01101011 |               0 |         01101011 |                 0 | No                 | Pass     |    01101101 |           -2 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      17 | 10000000 | 00100000 |       10100000 |               0 |         10100000 |                 0 | No                 | Pass     |    10100000 |            0 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      18 | 10101010 | 10011101 |       01001111 |               1 |         01001111 |                 1 | Propagated         | Pass     |    01000111 |            8 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      19 | 10010110 | 00010011 |       10100111 |               0 |         10100111 |                 0 | No                 | Pass     |    10101001 |           -2 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      20 | 00001101 | 01010011 |       01011111 |               0 |         01011111 |                 0 | No                 | Pass     |    01100000 |           -1 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      21 | 01101011 | 11010101 |       00111111 |               1 |         00111111 |                 1 | No                 | Pass     |    01000000 |           -1 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      22 | 00000010 | 10101110 |       10101110 |               0 |         10101110 |                 0 | No                 | Pass     |    10110000 |           -2 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      23 | 00011101 | 11001111 |       11101111 |               0 |         11101111 |                 0 | Propagated         | Pass     |    11101100 |            3 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      24 | 00100011 | 00001010 |       00101011 |               0 |         00101011 |                 0 | No                 | Pass     |    00101101 |           -2 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      25 | 11001010 | 00111100 |       00001110 |               1 |         00001110 |                 1 | Propagated         | Pass     |    00000110 |            8 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      26 | 11110010 | 10001010 |       01111010 |               1 |         01111010 |                 1 | No                 | Pass     |    01111100 |           -2 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      27 | 01000001 | 11011000 |       00011001 |               1 |         00011001 |                 1 | No                 | Pass     |    00011001 |            0 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      28 | 01111000 | 10001001 |       00001001 |               1 |         00001001 |                 1 | Propagated         | Pass     |    00000001 |            8 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      29 | 11101011 | 10110110 |       10011111 |               1 |         10011111 |                 1 | No                 | Pass     |    10100001 |           -2 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      30 | 11000110 | 10101110 |       01101110 |               1 |         01101110 |                 1 | No                 | Pass     |    01110100 |           -6 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      31 | 10111100 | 00101010 |       11101110 |               0 |         11101110 |                 0 | Propagated         | Pass     |    11100110 |            8 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      32 | 00001011 | 01110001 |       01111011 |               0 |         01111011 |                 0 | No                 | Pass     |    01111100 |           -1 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      33 | 10000101 | 01001111 |       11001111 |               0 |         11001111 |                 0 | No                 | Pass     |    11010100 |           -5 |
+---------+----------+----------+----------------+-----------------+------------------+-------------------+--------------------+----------+-------------+--------------+
|      34 | 00111011 | 00111010 |       01111011 |               0 |         01111011 |                 0 | Propagated         | Pass     |    01110101 |            6 |
```



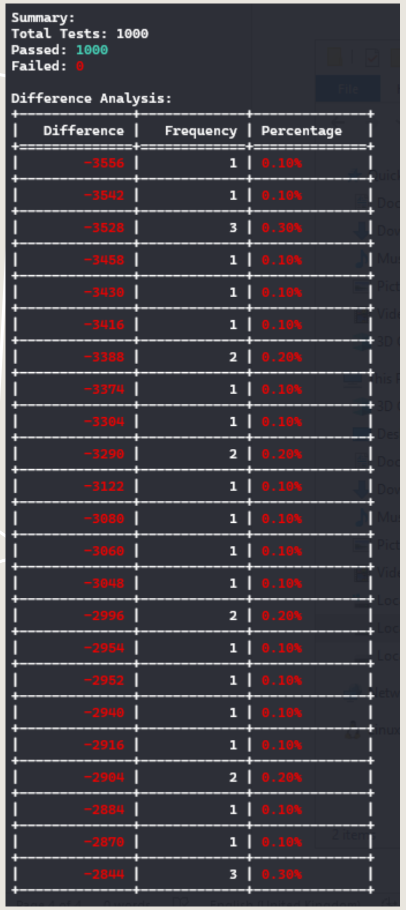
```
Summary:
Total Tests: 100
Passed: 100
Failed: 0

Difference Analysis:
+--------------+-------------+---------------+
|   Difference |   Frequency | Percentage    |
+==============+=============+===============+
|           -6 |           4 | 4.00%         |
+--------------+-------------+---------------+
|           -5 |           5 | 5.00%         |
+--------------+-------------+---------------+
|           -4 |           7 | 7.00%         |
+--------------+-------------+---------------+
|           -3 |           4 | 4.00%         |
+--------------+-------------+---------------+
|           -2 |          14 | 14.00%        |
+--------------+-------------+---------------+
|           -1 |          11 | 11.00%        |
+--------------+-------------+---------------+
|            0 |          25 | 25.00%        |
+--------------+-------------+---------------+
|            1 |           1 | 1.00%         |
+--------------+-------------+---------------+
|            3 |           2 | 2.00%         |
+--------------+-------------+---------------+
|            4 |           5 | 5.00%         |
+--------------+-------------+---------------+
|            6 |           5 | 5.00%         |
+--------------+-------------+---------------+
|            7 |           8 | 8.00%         |
+--------------+-------------+---------------+
|            8 |           9 | 9.00%         |
+--------------+-------------+---------------+
```

UNIT TESTING – MULTIPLIER



```
amaan@THUNDERBIRD:/mnt/d/Amaan/Documents/University/Year 3/EEE381_IIP/Testing/ApproximateMultiplier$ python ApproximateMultiplierTester.py
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
| Test #  | A (binary) | B (binary) | Verilog Product  | Calculated Product  | Exact Product    | Status | Difference |
+=========+============+============+==================+=====================+==================+========+============+
|       1 |   00100100 |   10000001 | 0001001000100100 |    0001001000100100 | 0001001000100100 | Pass   |          0 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|       2 |   00001001 |   01100011 | 0000001101101001 |    0000001101111011 | 0000001101111011 | Pass   |        -18 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|       3 |   00001101 |   10001101 | 0000011010001101 |    0000011100101001 | 0000011100101001 | Pass   |       -156 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|       4 |   01100101 |   00010010 | 0000011001010000 |    0000011100011010 | 0000011100011010 | Pass   |       -202 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|       5 |   00000001 |   00001101 | 0000000000000001 |    0000000000001101 | 0000000000001101 | Pass   |        -12 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|       6 |   01110110 |   00111101 | 0001011010010110 |    0001110000011110 | 0001110000011110 | Pass   |      -1416 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|       7 |   11101101 |   10001100 | 0111011010000000 |    1000000110011100 | 1000000110011100 | Pass   |      -2844 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|       8 |   11111001 |   11000110 | 1011101011000000 |    1100000010010110 | 1100000010010110 | Pass   |      -1494 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|       9 |   11000101 |   10101010 | 0111101100100000 |    1000001011010010 | 1000001011010010 | Pass   |      -1970 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      10 |   11100101 |   01110111 | 0110010100010101 |    0110101001110011 | 0110101001110011 | Pass   |      -1374 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      11 |   00010010 |   10001111 | 0000100100010010 |    0000101000001110 | 0000101000001110 | Pass   |       -252 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      12 |   11110010 |   11001110 | 1011010110000000 |    1100001010111100 | 1100001010111100 | Pass   |      -3388 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      13 |   11101000 |   11000101 | 1010111011101000 |    1011001010001000 | 1011001010001000 | Pass   |       -928 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      14 |   01011100 |   10111101 | 0011111110011100 |    0100001111101100 | 0100001111101100 | Pass   |      -1104 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      15 |   00101101 |   01100101 | 0001000100001101 |    0001000111000001 | 0001000111000001 | Pass   |       -180 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      16 |   01100011 |   00001010 | 0000000000000000 |    0000001111011110 | 0000001111011110 | Pass   |       -990 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      17 |   10000000 |   00100000 | 0001000000000000 |    0001000000000000 | 0001000000000000 | Pass   |          0 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      18 |   10101010 |   10011101 | 0110000001001010 |    0110100001000010 | 0110100001000010 | Pass   |      -2040 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      19 |   10010110 |   00010011 | 0000100111110110 |    0000101100100010 | 0000101100100010 | Pass   |       -300 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      20 |   00001101 |   01010011 | 0000010000011101 |    0000010000110111 | 0000010000110111 | Pass   |        -26 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      21 |   01101011 |   11010101 | 0101011101011011 |    0101100100000111 | 0101100100000111 | Pass   |       -428 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      22 |   00000010 |   10101110 | 0000000101000000 |    0000000101011100 | 0000000101011100 | Pass   |        -28 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      23 |   00011101 |   11001111 | 0001010111011101 |    0001011101110011 | 0001011101110011 | Pass   |       -406 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      24 |   00100011 |   00001010 | 0000000000000000 |    0000000101011110 | 0000000101011110 | Pass   |       -350 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      25 |   11001010 |   00111100 | 0010010111100000 |    0010111101011000 | 0010111101011000 | Pass   |      -2424 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      26 |   11110010 |   10001010 | 0111100100000000 |    1000001001110100 | 1000001001110100 | Pass   |      -2420 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      27 |   01000001 |   11011000 | 0011010011010000 |    0011011011011000 | 0011011011011000 | Pass   |       -520 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      28 |   01111000 |   10001001 | 0011110001111000 |    0100000000111000 | 0100000000111000 | Pass   |       -960 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      29 |   11101011 |   10110110 | 1010000110010000 |    1010011100010010 | 1010011100010010 | Pass   |      -1410 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      30 |   11000110 |   10101110 | 0111101111000000 |    1000011010010100 | 1000011010010100 | Pass   |      -2772 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      31 |   10111100 |   00101010 | 0001011110000000 |    0001111011011000 | 0001111011011000 | Pass   |      -1880 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      32 |   00001011 |   01110001 | 0000010011011011 |    0000010011011011 | 0000010011011011 | Pass   |          0 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      33 |   10000101 |   01001111 | 0010000111000101 |    0010100100001011 | 0010100100001011 | Pass   |      -1862 |
+---------+------------+------------+------------------+---------------------+------------------+--------+------------+
|      34 |   00111011 |   00111010 | 0000101100010000 |    0000110101011110 | 0000110101011110 | Pass   |       -590 |
```



```
Summary:
Total Tests: 1000
Passed: 1000
Failed: 0

Difference Analysis:
+--------------+--------------+---------------+
|   Difference |    Frequency | Percentage    |
+==============+==============+===============+
|        -3556 |            1 | 0.10%         |
+--------------+--------------+---------------+
|        -3542 |            1 | 0.10%         |
+--------------+--------------+---------------+
|        -3528 |            3 | 0.30%         |
+--------------+--------------+---------------+
|        -3458 |            1 | 0.10%         |
+--------------+--------------+---------------+
|        -3430 |            1 | 0.10%         |
+--------------+--------------+---------------+
|        -3416 |            1 | 0.10%         |
+--------------+--------------+---------------+
|        -3388 |            2 | 0.20%         |
+--------------+--------------+---------------+
|        -3374 |            1 | 0.10%         |
+--------------+--------------+---------------+
|        -3304 |            1 | 0.10%         |
+--------------+--------------+---------------+
|        -3290 |            2 | 0.20%         |
+--------------+--------------+---------------+
|        -3122 |            1 | 0.10%         |
+--------------+--------------+---------------+
|        -3080 |            1 | 0.10%         |
+--------------+--------------+---------------+
|        -3060 |            1 | 0.10%         |
+--------------+--------------+---------------+
|        -3048 |            1 | 0.10%         |
+--------------+--------------+---------------+
|        -2996 |            2 | 0.20%         |
+--------------+--------------+---------------+
|        -2954 |            1 | 0.10%         |
+--------------+--------------+---------------+
|        -2952 |            1 | 0.10%         |
+--------------+--------------+---------------+
|        -2940 |            1 | 0.10%         |
+--------------+--------------+---------------+
|        -2916 |            1 | 0.10%         |
+--------------+--------------+---------------+
|        -2904 |            2 | 0.20%         |
+--------------+--------------+---------------+
|        -2884 |            1 | 0.10%         |
+--------------+--------------+---------------+
|        -2870 |            1 | 0.10%         |
+--------------+--------------+---------------+
|        -2844 |            3 | 0.30%         |
+--------------+--------------+---------------+
```

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COMPARISON: AIMS AND MILESTONES

ACHIEVEMENTS

- Established a benchmark with a pipelined MAC unit
- Conceptual and partial implementation of AAUD architecture
- Implemented Approximate Adder and Approximate Multiplier
- Unit testing completed and modules validated

PENDING TASKS

- Complete integration of approximate multipliers and adders
- Explore Fuzzy memoization implementation
- Conduct comprehensive testing for power, speed, and accuracy
- Compare against other approximation units to evaluate performance

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FUTURE WORK PLAN

NEXT STEPS

Complete implementation of approximate arithmetic units

Integrate AAUD into RISC-V SoC and conduct full system testing

Evaluate performance against traditional MAC units

LONG-TERM

Explore further optimizations with different approximation methods

Investigate potential applications in other error-tolerant domains, such as machine learning

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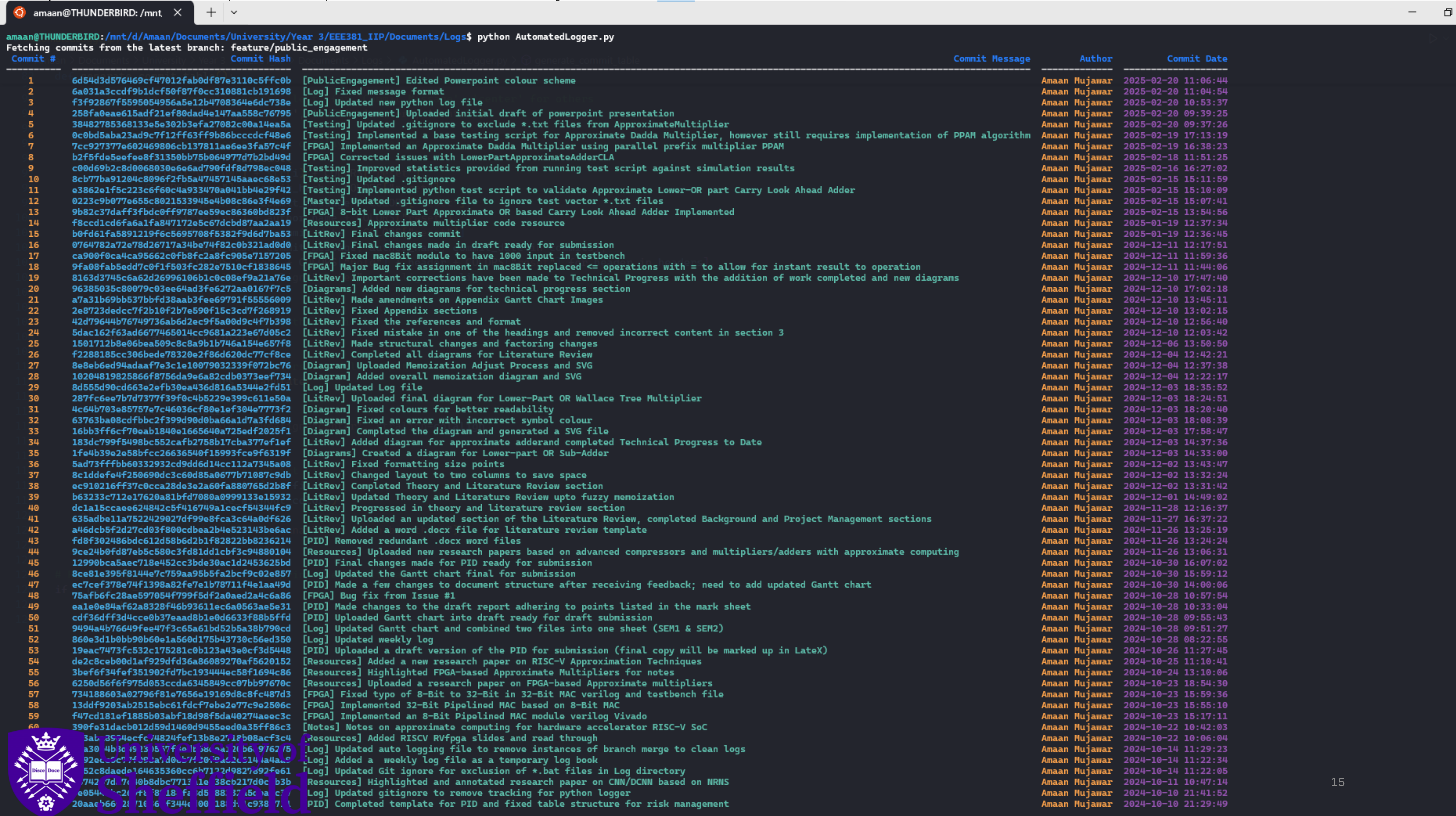

```
amaan@THUNDERBIRD:/mnt/d/Amaan/Documents/University/Year 3/EEE381_IIP/Documents/Logs$ python AutomatedLogger.py
Fetching commits from the latest branch: feature/public_engagement
 Commit #           Commit Hash                                                                                                          Commit Message        Author          Commit Date
----------  ----------------------------------------  ----------------------------------------------------------------------------------------------------------  ---------------  -------------------
    1       6d54d3d576469cf47012fab0df87e3110c5ffc0b  [PublicEngagement] Edited Powerpoint colour scheme                                                          Amaan Mujawar    2025-02-20 11:06:44
    2       6a031a3ccdf9b1dcf50f87f0cc310881cb191698  [Log] Fixed message format                                                                                  Amaan Mujawar    2025-02-20 11:04:54
    3       f3f92867f5595054956a5e12b4708364e6dc738e  [Log] Updated new python log file                                                                           Amaan Mujawar    2025-02-20 10:53:37
    4       258fa0eae615adf21ef80dad4e147aa558c76795  [PublicEngagement] Uploaded initial draft of powerpoint presentation                                        Amaan Mujawar    2025-02-20 09:39:25
    5       38482785368133e5e302b3efa27082c00a14ea5a  [Testing] Updated .gitignore to exclude *.txt files from ApproximateMultiplier                              Amaan Mujawar    2025-02-20 09:37:26
    6       0c0bd5aba23ad9c7f12ff63ff9b86bcccdcf48e6  [Testing] Implemented a base testing script for Approximate Dadda Multiplier, however still requires implementation of PPAM algorithm  Amaan Mujawar    2025-02-19 17:13:19
    7       7cc927377e602469806cb137811ae6ee3fa57c4f  [FPGA] Implemented an Approximate Dadda Multiplier using parallel prefix multiplier PPAM                     Amaan Mujawar    2025-02-19 16:38:23
    8       b2f5fde5eefee8f31350bb75b064977d7b2bd49d  [FPGA] Corrected issues with LowerPartApproximateAdderCLA                                                   Amaan Mujawar    2025-02-18 11:51:25
    9       c00d69b2c8d0068030e6e6ad790fdf8d798ec048  [Testing] Improved statistics provided from running test script against simulation results                  Amaan Mujawar    2025-02-16 16:27:02
   10       8cb77ba91204c8096f2fb5a47457145aaec68e53  [Testing] Updated .gitignore                                                                                Amaan Mujawar    2025-02-15 15:11:59
   11       e3862e1f5c223c6f60c4a933470a041bb4e29f42  [Testing] Implemented python test script to validate Approximate Lower-OR part Carry Look Ahead Adder       Amaan Mujawar    2025-02-15 15:10:09
   12       0223c9b077e655c8021533945e4b08c86e3f4e69  [Master] Updated .gitignore file to ignore test vector *.txt files                                          Amaan Mujawar    2025-02-15 15:07:41
   13       9b82c37daff3fbdc0ff9787ee59ec86360bd823f  [FPGA] 8-bit Lower Part Approximate OR based Carry Look Ahead Adder Implemented                             Amaan Mujawar    2025-02-15 13:54:56
   14       f8ccd1cd6fa6a1fa847172e5c67dcbd87aa2aa19  [Resources] Approximate multiplier code resource                                                            Amaan Mujawar    2025-01-19 12:37:34
   15       b0fd61fa5891219f6c5695708f5382f9d6d7ba53  [LitRev] Final changes commit                                                                               Amaan Mujawar    2025-01-19 12:36:45
   16       0764782a72e78d26717a34be74f82c0b321ad0d0  [LitRev] Final changes made in draft ready for submission                                                   Amaan Mujawar    2024-12-11 12:17:51
   17       ca900f0ca4ca95662c0fb8fc2a8fc905e7157205  [FPGA] Fixed mac8Bit module to have 1000 input in testbench                                                 Amaan Mujawar    2024-12-11 11:59:36
   18       9fa08fab5edd7c0f1f503fc282e7510cf1838645  [FPGA] Major Bug fix assignment in mac8Bit replaced <= operations with = to allow for instant result to operation  Amaan Mujawar    2024-12-11 11:44:06
   19       8163d3745c6a62d26996106b1c0c08ef9a21a76e  [LitRev] Important corrections have been made to Technical Progress with the addition of work completed and new diagrams  Amaan Mujawar    2024-12-10 17:47:40
   20       96385035c80079c03ee64ad3fe6272aa0167f7c5  [Diagrams] Added new diagrams for technical progress section                                                Amaan Mujawar    2024-12-10 17:02:18
   21       a7a31b69bb537bbfd38aab3fee69791f55556009  [LitRev] Made amendments on Appendix Gantt Chart Images                                                     Amaan Mujawar    2024-12-10 13:45:11
   22       2e8723dedcc7f2b10f2b7e590f15c3cd7f268919  [LitRev] Fixed Appendix sections                                                                            Amaan Mujawar    2024-12-10 13:02:15
   23       42d79644b76749736ab6d2ec9f5a00d9c4f7b398  [LitRev] Fixed the references and format                                                                    Amaan Mujawar    2024-12-10 12:56:40
   24       5dac162f63ad6677465014cc9681a223e67d05c2  [LitRev] Fixed mistake in one of the headings and removed incorrect content in section 3                    Amaan Mujawar    2024-12-10 12:03:42
   25       1501712b8e06bea509c8c8a9b1b746a154e657f8  [LitRev] Made structural changes and factoring changes                                                      Amaan Mujawar    2024-12-06 13:50:50
   26       f2288185cc306bede78320e2f86d620dc77cf8ce  [LitRev] Completed all diagrams for Literature Review                                                       Amaan Mujawar    2024-12-04 12:42:21
   27       8e8eb6ed94adaaf7e3c1e10079032339f072bc76  [Diagram] Uploaded Memoization Adjust Process and SVG                                                        Amaan Mujawar    2024-12-04 12:37:38
   28       10204819825866f8756da9e6a82cdb0373eef734  [Diagram] Added overall memoization diagram and SVG                                                         Amaan Mujawar    2024-12-04 12:22:17
   29       8d555d90cd663e2efb30ea436d816a5344e2fd51  [Log] Updated Log file                                                                                      Amaan Mujawar    2024-12-03 18:35:52
   30       287fc6ee7b7d7377f39f0c4b5229e399c611e50a  [LitRev] Uploaded final diagram for Lower-Part OR Wallace Tree Multiplier                                   Amaan Mujawar    2024-12-03 18:24:51
   31       4c64b703e85757e7c46036cf80e1ef304e7773f2  [Diagram] Fixed colours for better readability                                                              Amaan Mujawar    2024-12-03 18:20:40
   32       63763ba08cdfbbc2f399d90d0ba66a1d7a3fd684  [Diagram] Fixed an error with incorrect symbol colour                                                       Amaan Mujawar    2024-12-03 18:08:39
   33       16bb3ff6cf70eab1840e1665640a725edf2025f1  [Diagram] Completed the diagram and generated a SVG file                                                    Amaan Mujawar    2024-12-03 17:58:47
   34       183dc799f5498bc552cafb2758b17cba377ef1ef  [LitRev] Added diagram for approximate adderand completed Technical Progress to Date                        Amaan Mujawar    2024-12-03 14:37:36
   35       1fe4b39e2e58bfcc26636540f15993fce9f6319f  [Diagrams] Created a diagram for Lower-part OR Sub-Adder                                                    Amaan Mujawar    2024-12-03 14:33:00
   36       5ad73fffbb60332932cd9dd6d14cc112a7345a08  [LitRev] Fixed formatting size points                                                                       Amaan Mujawar    2024-12-02 13:43:47
   37       8c1ddefe4f250690dc3c60d85a0677b71087c9db  [LitRev] Changed layout to two columns to save space                                                        Amaan Mujawar    2024-12-02 13:32:24
   38       ec910216ff37c0cca28de3e2a60fa880765d2b8f  [LitRev] Completed Theory and Literature Review section                                                      Amaan Mujawar    2024-12-02 13:31:42
   39       b63233c712e17620a81bfd7080a0999133e15932  [LitRev] Updated Theory and Literature Review upto fuzzy memoization                                        Amaan Mujawar    2024-12-01 14:49:02
   40       dc1a15ccaee624842c5f416749a1cecf54344fc9  [LitRev] Progressed in theory and literature review section                                                 Amaan Mujawar    2024-11-28 12:16:37
   41       635adbe11a7522429027df99e8fca3c64a0df626  [LitRev] Uploaded an updated section of the Literature Review, completed Background and Project Management sections  Amaan Mujawar    2024-11-27 16:37:22
   42       a46dcb5f2d27cd03f800cdbea2b4e523143be6ac  [LitRev] Added a word .docx file for literature review template                                             Amaan Mujawar    2024-11-26 13:25:19
   43       fd8f302486bdc612d58b6d2b1f82822bb8236214  [PID] Removed redundant .docx word files                                                                    Amaan Mujawar    2024-11-26 13:24:24
   44       9ce24b0fd87eb5c580c3fd81dd1cbf3c94880104  [Resources] Uploaded new research papers based on advanced compressors and multipliers/adders with approximate computing  Amaan Mujawar    2024-11-26 13:06:31
   45       12990bca5aec718e452cc3bde30ac1d2453625bd  [PID] Final changes made for PID ready for submission                                                       Amaan Mujawar    2024-10-30 16:07:02
   46       8ce81e395f8144e7c759aa95b5fa2bcf9c02e857  [Log] Updated the Gantt chart final for submission                                                          Amaan Mujawar    2024-10-30 15:59:12
   47       ec7cef378e74f1398a82fe7e1b78711f4e1aa49d  [PID] Made a few changes to document structure after receiving feedback; need to add updated Gantt chart    Amaan Mujawar    2024-10-30 14:00:06
   48       75afb6fc28ae597054f799f5df2a0aed2a4c6a86  [FPGA] Bug fix from Issue #1                                                                                Amaan Mujawar    2024-10-28 10:57:54
   49       ea1e0e84af62a8328f46b93611ec6a0563ae5e31  [PID] Made changes to the draft report adhering to points listed in the mark sheet                          Amaan Mujawar    2024-10-28 10:33:04
   50       cdf36dff3d4cce0b37eaad8b1e0d6633f88b5ffd  [PID] Uploaded Gantt chart into draft ready for draft submission                                            Amaan Mujawar    2024-10-28 09:55:43
   51       9494a4b76649fee47f3c65a61bd52b5a38b790cd  [Log] Updated Gantt chart and combined two files into one sheet (SEM1 & SEM2)                               Amaan Mujawar    2024-10-28 09:51:27
   52       860e3d1b0bb90b60e1a560d175b43730c56ed350  [Log] Updated weekly log                                                                                    Amaan Mujawar    2024-10-28 08:22:55
   53       19eac7473fc532c175281c0b123a43e0cf3d5448  [PID] Uploaded a draft version of the PID for submission (final copy will be marked up in LateX)            Amaan Mujawar    2024-10-26 11:27:45
   54       de2c8ceb00d1af929dfd36a86089270af5620152  [Resources] Added a new research paper on RISC-V Approximation Techniques                                   Amaan Mujawar    2024-10-25 11:10:41
   55       3bef6f34fef351902fd7bc193444ec58f1694c86  [Resources] Highlighted FPGA-based Approximate Multipliers for notes                                        Amaan Mujawar    2024-10-24 13:10:06
   56       6250d56f6f975d053ccda6345849cc07bb97670c  [Resources] Uploaded a research paper on FPGA-based Approximate multipliers                                 Amaan Mujawar    2024-10-23 18:54:30
   57       734188603a02796f81e7656e19169d8c8fc487d3  [FPGA] Fixed typo of 8-Bit to 32-Bit in 32-Bit MAC verilog and testbench file                               Amaan Mujawar    2024-10-23 15:59:36
   58       13ddf9203ab2515ebc61fdcf7ebe2e77c9e2506c  [FPGA] Implemented 32-Bit Pipelined MAC based on 8-Bit MAC                                                  Amaan Mujawar    2024-10-23 15:55:10
   59       f47cd181ef1885b03abf18d98f5da40274aeec3c  [FPGA] Implemented an 8-Bit Pipelined MAC module verilog Vivado                                             Amaan Mujawar    2024-10-23 15:17:11
   60       390fe31dacb012d59d1460d9455eed0a35ff86c3  [Notes] Notes on approximate computing for hardware accelerator RISC-V SoC                                  Amaan Mujawar    2024-10-22 10:42:03
 [illegible] [illegible]3ab[illegible]4824fef13b8e2[illegible]8b08acf3c4  [Resources] Added RISCV RVfpga slides and read through                      Amaan Mujawar    2024-10-22 10:06:04
 [illegible] [illegible]a30[illegible]4b3[illegible]  [Log] Updated auto logging file to remove instances of branch merge to clean logs                  Amaan Mujawar    2024-10-14 11:29:23
 [illegible] [illegible]92e[illegible]  [Log] Added a  weekly log file as a temporary log book                                                           Amaan Mujawar    2024-10-14 11:22:34
 [illegible] [illegible]52c8daede164635360cc6b7122d9827892fe61  [Log] Updated Git ignore for exclusion of *.bat files in Log directory                 Amaan Mujawar    2024-10-14 11:22:05
 [illegible] [illegible]742[illegible]0b8dbc7713[illegible]38cb217d0c[illegible]b3b  [Resources] Highlighted and annotated research paper on CNN/DCNN based on NRNS  Amaan Mujawar    2024-10-11 10:47:14
 [illegible] [illegible]e054[illegible]  [Log] Updated gitignore to remove tracking for python logger                                                    Amaan Mujawar    2024-10-10 21:41:52
 [illegible] 20aa[illegible]66[illegible]f344[illegible]c938[illegible]  [PID] Completed template for PID and fixed table structure for risk management  Amaan Mujawar    2024-10-10 21:29:49
```

THANK YOU

Amaan Mujawar

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