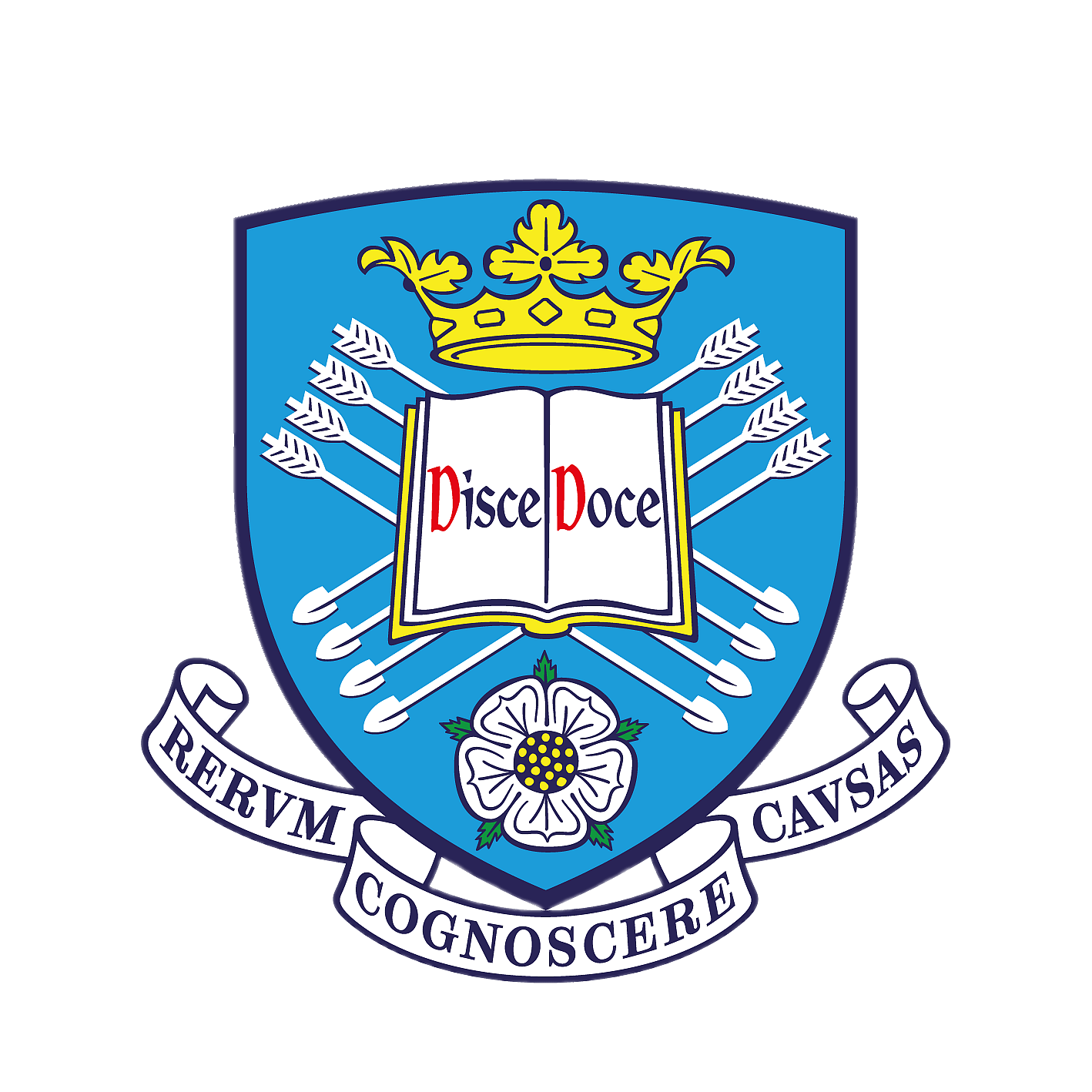
**Design of an Approximate Computing-based 32-bit MAC Unit: A Step Towards RISC-V SoC Integration**

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**Abstract**

The increasing volume of data generated by modern applications, such as image processing, video streaming, and machine learning, has illustrated the need for more energy-efficient and faster computing solutions. Traditional computing methods often fall short in addressing the challenges of high energy consumption and extended processing times. This dissertation explores the integration of Approximate Computing (AC) into the design of a 32-bit Multiply-Accumulate (MAC) unit within a Reduced Instruction Set Computer (RISC-V) System on Chip (SoC) to overcome these limitations. The approach leverages Approximate Computing, which allows for reduced accuracy in non-critical operations, leading to significant gains in speed and energy efficiency.

The primary goal of this project is to design and implement a MAC unit that seamlessly integrates with the RISC-V processor architecture while achieving performance improvements, such as lower power consumption, faster processing speeds, and acceptable accuracy levels. The project utilizes the Xilinx Vivado Design Suite for design, simulation, and synthesis, and the implementation is carried out on the Artix Nexus 7 FPGA platform. Detailed performance metrics, including power consumption, speed benchmarks, and accuracy, are measured and evaluated to ensure the success of the design.

**Introduction**

The rapid advancement of digital technologies has led to a significant increase in the demand for high-performance computing systems capable of handling large, complex datasets. As applications such as machine learning, big data analytics, computer vision, and multimedia processing become more ubiquitous, the need for efficient and energy-conscious computing solutions has never been more pressing. Traditional approaches to computation have largely relied on continually shrinking transistor sizes, guided by Moore's Law, to achieve improvements in performance, energy efficiency, and cost. However, as transistor sizes approach their physical limits, the rate of progress predicted by Moore's Law has slowed, necessitating the exploration of new approaches that can complement traditional scaling.

One such innovative approach is approximate computing, which offers a paradigm shift in how computations are performed. Unlike conventional computing, which strives for exact results, approximate computing allows for controlled errors in computation to achieve significant reductions in execution time, power consumption, and resource utilization. This approach is particularly well-suited for applications in which small errors are tolerable, such as signal processing, image processing, and multimedia tasks. By exploiting the inherent error tolerance in many real-world applications, approximate computing enables systems to deliver faster results and consume less power without perceptibly compromising the quality of the output.

The growing interest in approximate computing is driven by the increasing demand for energy-efficient and high-performance computing solutions, particularly in contexts where perfect accuracy is not critical. As the limitations of Moore's Law become more evident, the need for alternative techniques to continue achieving performance and energy gains is becoming increasingly urgent. Approximate computing, by enabling systems to deliver optimized performance at the expense of slight inaccuracies, represents a promising solution to the challenges of modern computing.

**Background and Motivation**

The motivation behind this dissertation lies in the urgent need for efficient computing architectures capable of handling the growing demands of data-intensive applications while minimizing energy consumption and reducing execution time. Traditional computing methods are increasingly inadequate for meeting the performance and energy requirements of modern systems. The ever-growing volume of data generated by applications such as image processing, video streaming, and machine learning necessitates the development of more efficient computing solutions that can handle these data demands without compromising system performance.

This dissertation explores the integration of approximate computing techniques within the context of a Reduced Instruction Set Computing (RISC-V) System on Chip (SoC), with a specific focus on designing a 32-bit Multiply-Accumulate (MAC) unit. By leveraging approximate computing methods, the project aims to develop an arithmetic unit that reduces power consumption and processing time, particularly in applications where minor inaccuracies are acceptable. The integration of approximate computing into a RISC-V SoC architecture aims to enhance overall system efficiency, enabling better handling of large volumes of data while reducing resource consumption.

**Aims and Objectives**

The primary aim of this dissertation is to design and implement a 32-bit Multiply-Accumulate (MAC) unit that utilizes approximate computing techniques for integration into a RISC-V SoC. The project will pursue the following objectives:

1. **Literature Review**: Conduct an in-depth literature review to explore various approximate computing techniques, identifying the most suitable methods for integration into the MAC unit based on their performance, characteristics, and potential for reducing power consumption and execution time.
2. **Design**: Develop a detailed architectural design for the MAC unit, incorporating the chosen approximate computing methods. The design will focus on optimizing the trade-off between performance, power consumption, and accuracy.
3. **Implementation**: Implement the MAC unit using Hardware Description Language (HDL), specifically Verilog, and conduct initial testing and simulation through FPGA platforms to verify the functionality of the design.
4. **Integration**: Integrate the MAC unit into a RISC-V SoC architecture, ensuring compatibility with the system and performing integration testing to assess its functionality within the broader system context.
5. **Evaluation**: Conduct comprehensive evaluations to assess the impact of the approximate computing methods on the system’s performance. This will include analyzing power consumption, processing speed, and accuracy metrics, comparing the results with industry standards to determine the effectiveness of the proposed solution.

**Project Significance**

This project is of particular significance in light of the increasing demand for energy-efficient computing systems capable of handling large datasets and complex computations. As traditional approaches to computation face diminishing returns in terms of performance and energy efficiency, approximate computing presents an opportunity to optimize computational resources by allowing a controlled level of error in specific tasks. The integration of approximate computing into a RISC-V SoC offers a novel approach to achieving high-performance, energy-efficient computing, making it suitable for a wide range of modern applications. By contributing to the development of efficient hardware solutions, this research has the potential to drive advancements in the design of sustainable digital systems for future technologies.