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|  | **THE UNIVERSITY OF SHEFFIELD School of Electrical and Electronic Engineering**  **3rd Year Individual Project — Project Initialisation Document** | | | |  |
| **Student Name** | | Amaan Mujawar | | | |
| **Project Title** | | Implement an Arithmetic Unit utilising Approximate Computing into RISC-V SoC | | | |
| **Supervisor** | | Mr Neil Powell | **Second Marker** |  | |

**Project motivation:**

The rapid increase in data generated by applications such as image processing, video streaming, and machine learning has created a need for efficient computing solutions. Traditional computing methods often lead to high energy consumption and prolonged processing times, making them inadequate for modern data-intensive tasks.

This project aims to develop an Arithmetic Unit that utilises Approximate Computing, which allows for less precise calculations in scenarios where perfect accuracy is not critical. This approach can significantly enhance processing speed and reduce energy usage, making it particularly suitable for applications that can tolerate minor inaccuracies.

The motivation for this work to integrate Approximate Computing into a Reduced Instruction Set Computer (RISC-V) System on Chip (SoC). By focusing on these objectives, we aim to improve overall system efficiency, enabling better handling of large data volumes while minimising resource consumption.

**Project Specification:**

The objective of this project is to design and implement an Arithmetic Unit using Approximate Computing techniques for integration into a RISC-V SoC. The development will utilise the Artix Nexus 7 FPGA and the Xilinx Vivado Design Suite as primary tools.

The project will consist of several key tasks. First, a literature review will be conducted to identify relevant Approximate Computing techniques. Following this, the design phase will involve creating architectural designs and schematic diagrams to outline the functionality of the Arithmetic Unit and its interactions with the RISC-V SoC.

In the implementation phase, the Arithmetic Unit will be coded using Hardware Description Languages (HDLs), and the FPGA will be synthesized, simulated, and programmed using Vivado. Testing and verification will include the development of test cases to evaluate performance and accuracy, ensuring proper integration with the RISC-V SoC.

Throughout the project, comprehensive documentation will be maintained to capture design choices, implementation processes, and testing outcomes. The expected outcome is a fully functional Arithmetic Unit that demonstrates the advantages of Approximate Computing in terms of performance and energy efficiency, along with detailed documentation that provides insights into the design and implementation process.

**Project Schedule:**

The objective of this project is to design and implement an Arithmetic Unit using Approximate Computing techniques for integration into a RISC-V SoC. Development will utilise the Artix Nexus 7 FPGA and the Xilinx Vivado Design Suite as primary tools.

The project’s first Milestone 1, involves the completion of a final process initiation document for submission. Following this, a literature review will be conducted to identify relevant Approximate Computing techniques. In Milestone 2, a detailed project specification will be planned and drafted for referencing and setting the foundation whilst proceeding with the design phase.

During the design phase, architectural designs and schematic diagrams will be created to outline the functionality of the Arithmetic Unit and its interactions with the RISC-V SoC. After the design is established, Milestone 3 will focus on selecting an appropriate approximation method to be implemented in the project.

In the implementation phase, the Arithmetic Unit will be coded using Hardware Description Languages (HDLs). Milestone 4 will be reached when the chosen approximation method is implemented on the FPGA, followed by synthesis, simulation, and programming using the Vivado Design Suite. Rigorous testing and verification will ensue, including the development of comprehensive test cases to evaluate performance and accuracy, ensuring proper integration with the RISC-V SoC.

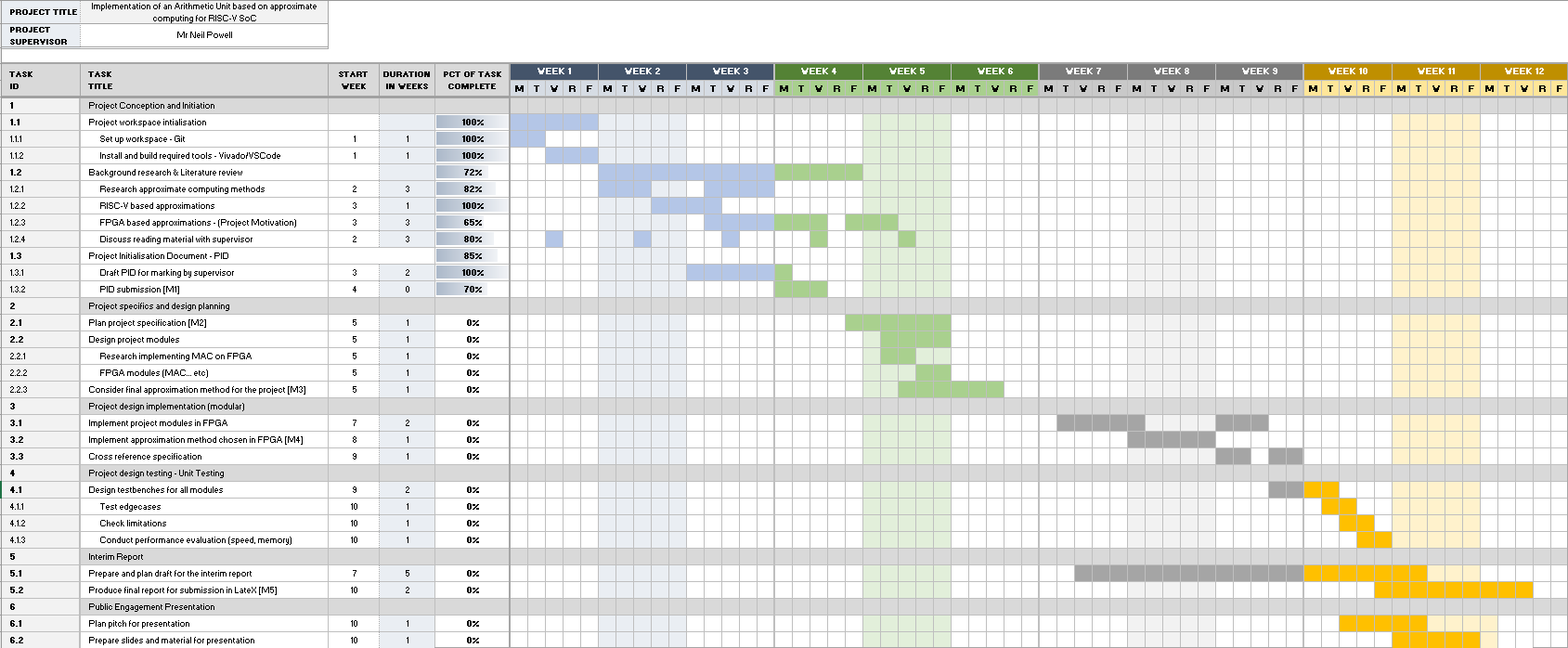
Finally, in Milestone 5, a final interim report will be produced to document progress and outcomes. Throughout the project, comprehensive documentation will capture design choices, implementation processes, and testing results. The expected outcome is a fully functional Arithmetic Unit that demonstrates the advantages of Approximate Computing in terms of performance and energy efficiency, along with detailed documentation that provides insights into the design and implementation process.

**Risk Register:**

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| --- | --- | --- | --- | --- |
|  | **Description of Risk** | **Risk evaluation (L/M/H)** | **Chance of risk (L/M/H)** | **Mitigation of Risk** |
| **1** | Loss of data (USB key) | M | L | Multiple back-ups, GitHub. |
| **2** | Delays in literature review affecting subsequent phases | M | M | |  | | --- | |  |   Implement peer reviews and consult supervisor regularly. |
| **3** | Incomplete or inaccurate design documentation | M | M | Consult with supervisor to ensure documentation is thorough and accurate. |
| **4** | Technical difficulties with FPGA programming | H | M | Seek support from resources and experienced colleagues. |
| **5** | Issues during testing leading to inaccurate results | H | M | Develop detailed test cases and conduct iterative testing. |
| **6** | Hardware failures (e.g., FPGA malfunctions) | H | L | Keep backup hardware available and conduct regular checks. |
| **7** | Resource availability (e.g., tools, software licenses) | M | L | Secure necessary tools and licenses early in the project. |
| **8** | Changes in project scope or requirements | M | M | Establish clear specifications. |
| **9** | Staff member availability (e.g., illness, other commitments) | M | M | Have tasks that can be carried on in parallel, so workflow is not interrupted. |
| **10** | Time management issues affecting project timeline | M | M | Conduct regular status meetings with supervisor. |

**Appendix:**

**Gantt chart:**



M1 – Milestone 1 for producing a final process initiation document for submission

M2 – Milestone 2 for planning a detailed project specification

M3 – Milestone 3 for choosing an approximation method to be implemented for the project

M4 – Milestone 4 for implementing the chosen approximation method in FPGA

M5 – Milestone 5 for producing a final interim report

**References: (Still need to be added)**

*Reference should be IEEE referencing style. Web references should be kept to a minimum as they are usually not peer-reviewed.*