The Operation of Real Mode Interrupt

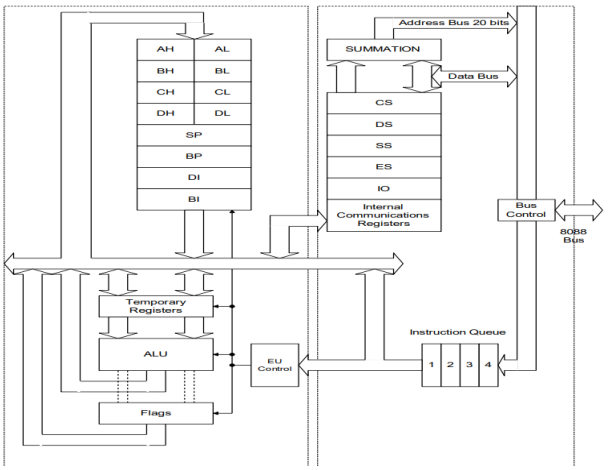
1. The contents of the flag registers are pushed onto the stack.
2. Both the interrupt (IF) and (TF) flags are cleared. This disables the INTR pin and the trap or single-step feature.
3. The contents of the code segment register (CS) is pushed onto the stack.
4. The contents of the instruction pointer (IP) is pushed onto the stack.
5. The interrupt vector contents are fetched, and then placed into both IP and CS so that the next instruction executes at the interrupt service procedure addressed by the interrupt vector.
6. While returning from the interrupt-service routine by the ins. IRET, flags return to their state prior to the interrupt and and operation restarts at the prior IP address. The return address (CS and IP) is not always the next instruction, with some interrupt types it is the current instruction.

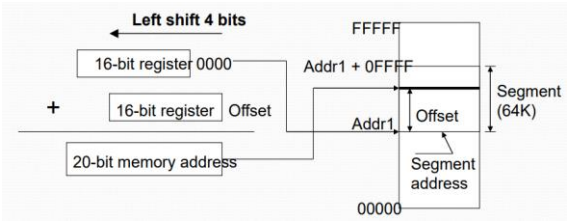
Interrupt Vector Table

- Interrupt vector table consists of 256 entries each containing 4 bytes.
- Each entry contains the offset and the segment address of the interrupt vector each 2 bytes long.
- Table starts at the memory address 00000F.
- First 32 vectors are spared for various microprocessor families.
- The rest 224 vectors are user definable.
- **The lower the vector number, the higher the priority.**

Interrupt Vector Table

INT Number	Physical Address
INT 00	00000
INT 01	00004
INT 02	00008
:	:
:	:
INT FF	003FC





Interrupt instructions

- Interrupt enable flag (IF) causes external interrupts to be enabled.
- INT n initiates a vectored call of a subroutine.
- INTO instruction should be used after each arithmethic instruction where there is a possibility of an overflow.
- HLT waits for an interrupt to occur.
- WAIT waits for $\overline{TEST}$ input to go high.