Linear decoding :

- This technique uses the unused address lines of the microprocessor as chip selects for the memory chips.
- This method is used for small systems.
- A simple way to connect an 8 bit microprocessor to a 6k RAM system using linear decoding is shown as follows.
- In this approach, the address lines A9 though A0 of the microprocessor are used as a common input to each 1K x 8 RAM chip.
- The remaining 6 high – order lines are use to select one of the 6 RAM chips

Address Map realized by the system:

Binary address pattern A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0	Device Selected	Address arranged in Hex
0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1	RAM Chip 0	0400 To 07FF
0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 1 1 1 1 1 1 1 1	RAM Chip 1	0800 To 0BFF
0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 1 1 1 1 1 1 1 1 1	RAM Chip 2	1000 To 13FF
0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 1 1 1 1 1 1 1 1	RAM Chip 3	2000 To 23FF
	RAM Chip 4	
	RAM Chip 5	

Advantages: does not require decoding hardware

Disadvantages:

- 64K bytes of RAM space, interface only 6 K
- Address map is not contiguous, it is sparsely distributed.
- If both A11 & A12 high at the same time, bus conflict occurs.
- If all unused address lines are not utilized as CS for memory Then unused pins don’t care

Full-partial decoding:

- Here 2- to- 4 decoder is used and interface the
- 8 bit microprocessor with 4K bytes of RAM
- Also observe that this hardware makes sure that the memory
- system is enabled only when the lines A15 through A12 are Zero.
- •The complete address map corresponding to this organization is
- summarized below

Binary address pattern A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0	Device Selected	Address arranged in Hex
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1	RAM Chip 0	0000 To 03FF
0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1	RAM Chip 1	0400 To 07FF
0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 1 1 1 1 1 1 1 1	RAM Chip 2	0800 To 0BFF
0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1	RAM Chip 3	0C00 To 0FFF

Memory management Unit:

The MMU translates logical addresses to physical addresses provided by the memory chips

The memory can perform address translation in one of two ways:

Using Substitution technique

By adding an offset to each logical address to obtain the corresponding physical address

The MMU reduces the burden of the memory management function of O/S

The basic function provided by MMU are

Address translation

Protection