LD Lab (CS2091D)-ASSIGNMENT NO.: I(b)

Submission Date: 09-09-2021(THURSDAY) 11:59 PM.

Implement the following logic function using ***Verilog*** with each of the three modeling techniques (Gate-level modeling, Dataflow modeling, and Behavioral modeling). Subsequently, Simulate and verify all the given logic functions using ***ModelSim*** integrated with ***Quartus Prime Lite Edition Software*.**

Please note that the only building blocks you can use are primitive **NAND gates** and the composite gates you will gradually build on top of them. Verilog code for initiating the basic NAND Gate in ModelSim is ***nand nand_1 (out, in0, in1);*** As the assignment progresses, students have to call/use the basic logical functions already implemented to build other logical functions.

1. Basic MULTIPLEXER
2. Basic DE MULTIPLEXER
3. 16-BIT MULTIPLEXER
4. 16-BIT / 4-WAY MULTIPLEXER
5. 16-BIT / 8-WAY MULTIPLEXER
6. 4-WAY DEMULTIPLEXER
7. 8-WAY DEMULTIPLEXER