Faculty of Engineering & Technology – Electrical & Computer Engineering Department

Second Semester 2022 – 2023

Integrated Circuits

ENCS3330

Assignment #3

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Section: 2

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Part I

Design, layout, and simulation of CMOS NAND gate:

Solution

The nand circuit schematic and layout are shown below after DRC and LVS were verified correctly. Note that a 180nm process file was used, as agreed by the instructor. Since there was difficulty in obtaining that 35u model available, and 180n is better (smaller).

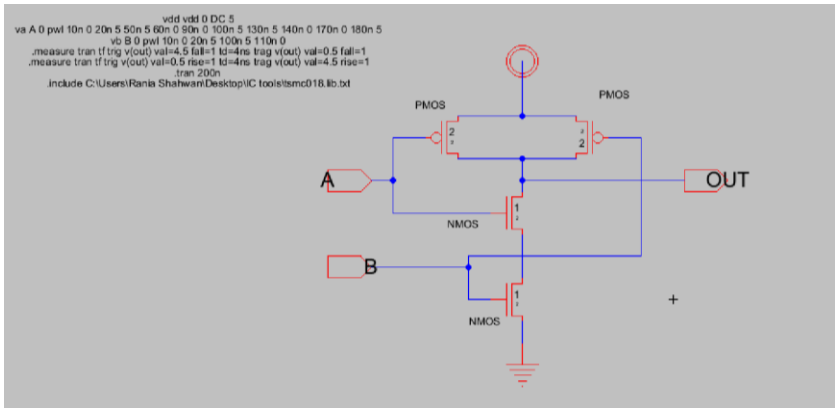

Figure 1: Nand gate schematic

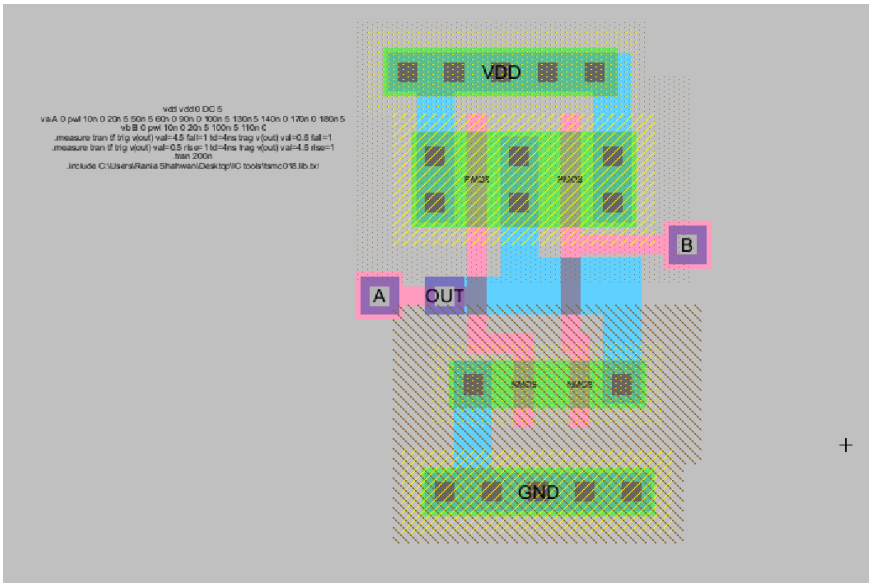

Figure 2: Nand gate layout

Simulation Results

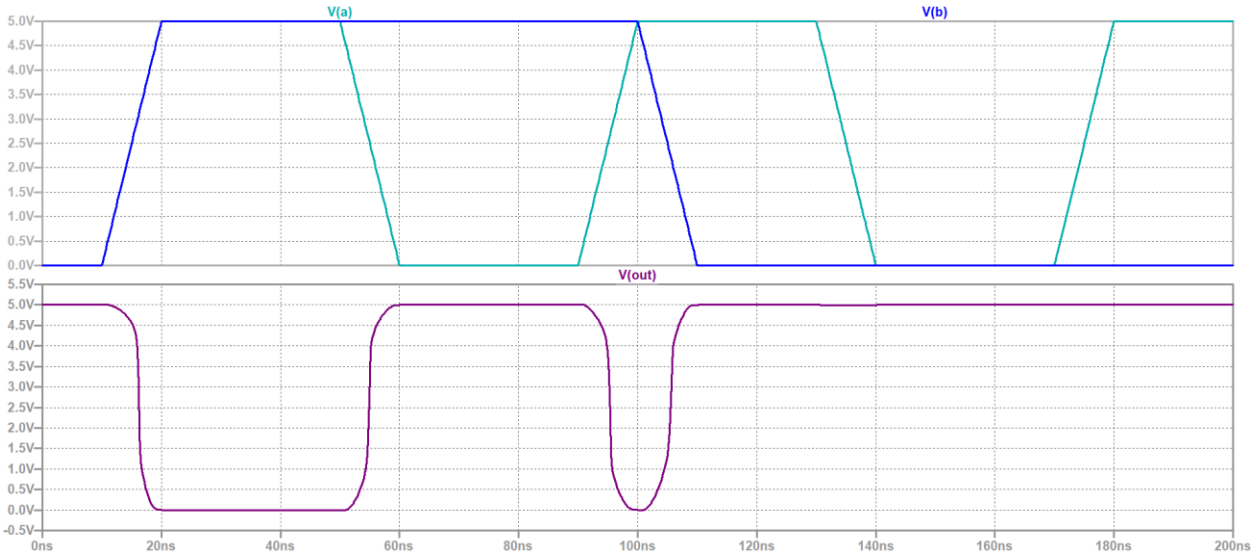

Figure 3: Nand gate simulation

10% rise = 17.42ns

90% rise = 14.31ns

T rise= 3.11ns

10% fall = 56.52ns

90% fall= 53.31ns

T fall = 3.21 ns

Approximately accepted.

- 22nm technology implies that the smallest length of a transistor that you can make with that technology is 22nm. The lengths can be larger than that - but that is the smallest.

Part II

Design, layout, and simulation of CMOS XOR gate

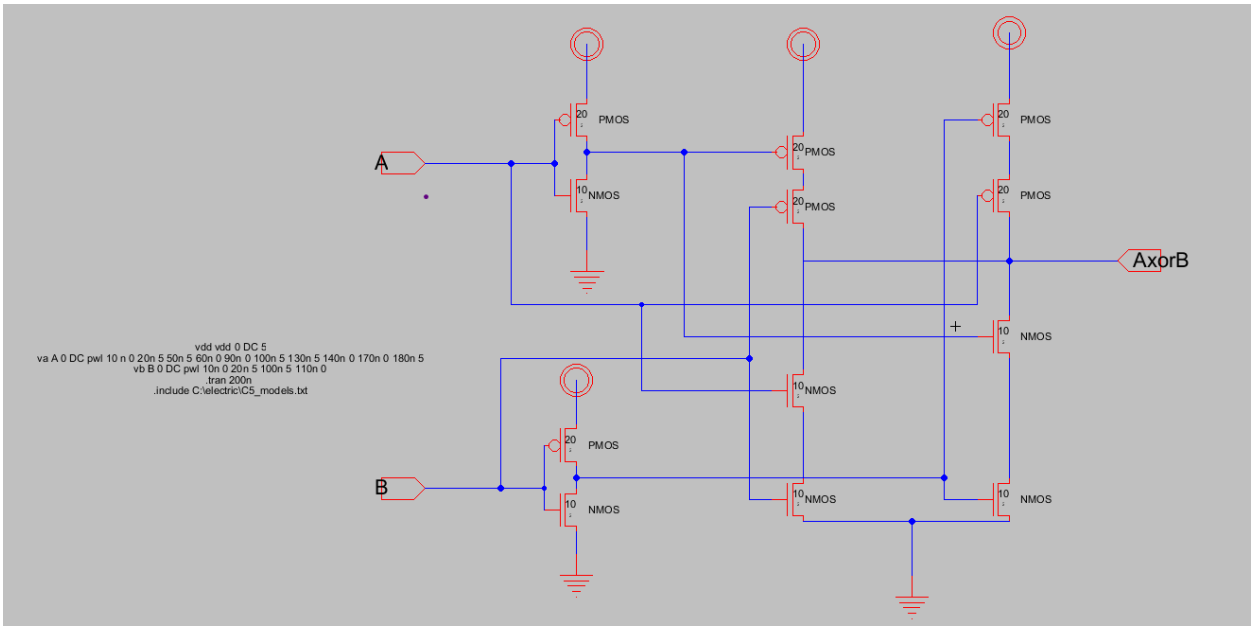

Figure 4: XOR gate schematic

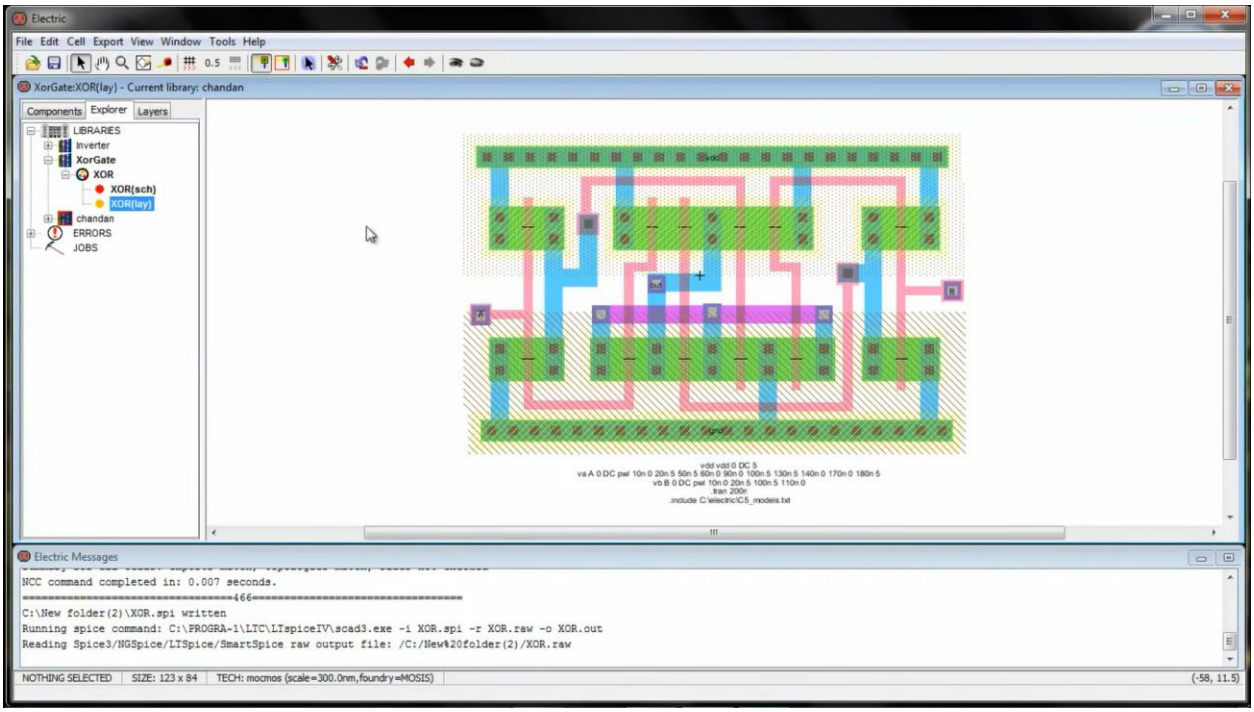

Figure 5: XOR gate layout

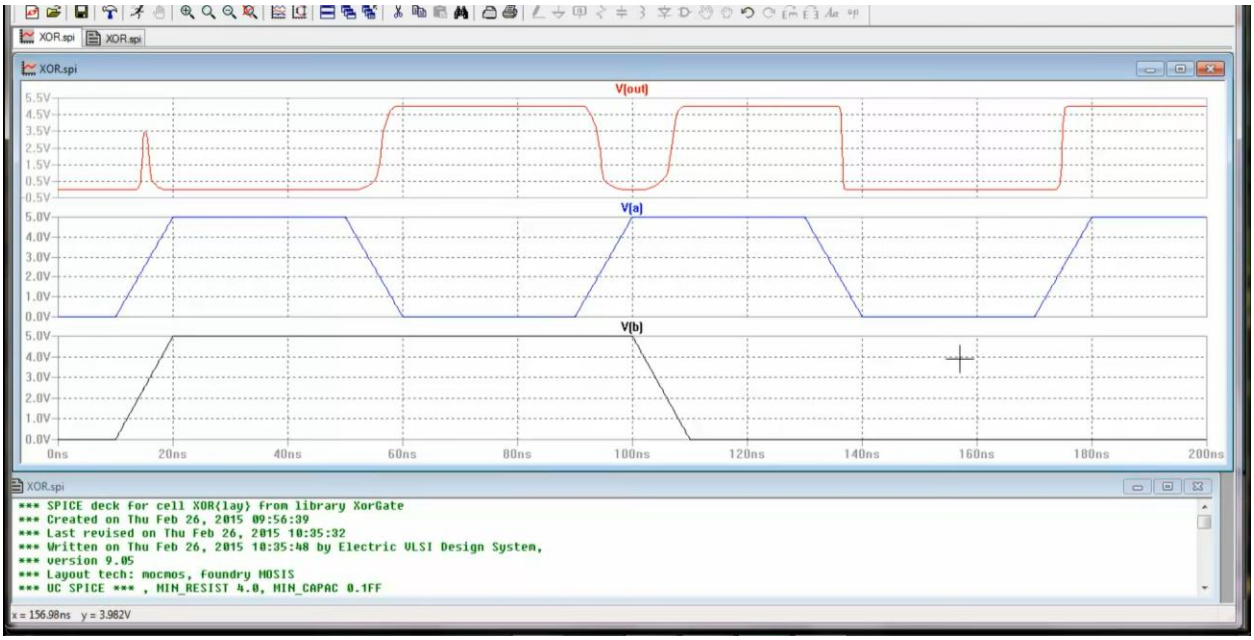

Figure 6: Xor gate simulation

Part III

Design a 2-bit full adder, including design from truth table up to transistor and simulation (spice and layout).

Solution

Schematic Design

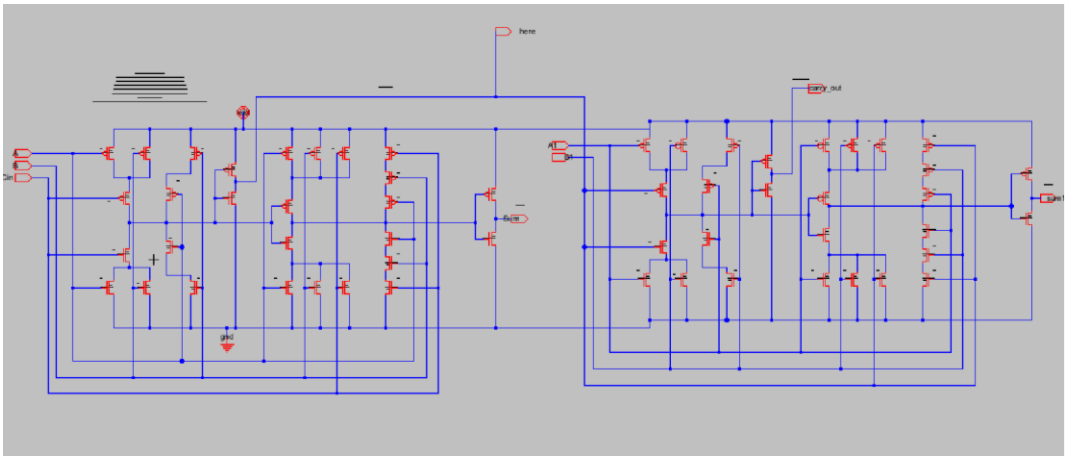

Figure7: 2-bit Full Adder Schematic

Spice Code:

vdd vdd 0 dc 1.8

va A 0 pulse (1.8 0 0 10p 10p 10n 20n)

vb B 0 pulse (1.8 0 0 10p 10p 40n 80n)

vaa A1 0 pulse (1.8 0 0 10p 10p 20n 40n)

vbb B1 0 pulse (1.8 0 0 10p 10p 80n 160n)

vc Cin 0 pulse (1.8 0 0 10p 10p 160n 320n)

.tran 1n 400n

.include C:\Users\Rania Shahwan\Desktop\IC tools\tsmc018.lib.txt

- Tsmc 180 nm process file was included.

The first part of the circuit:

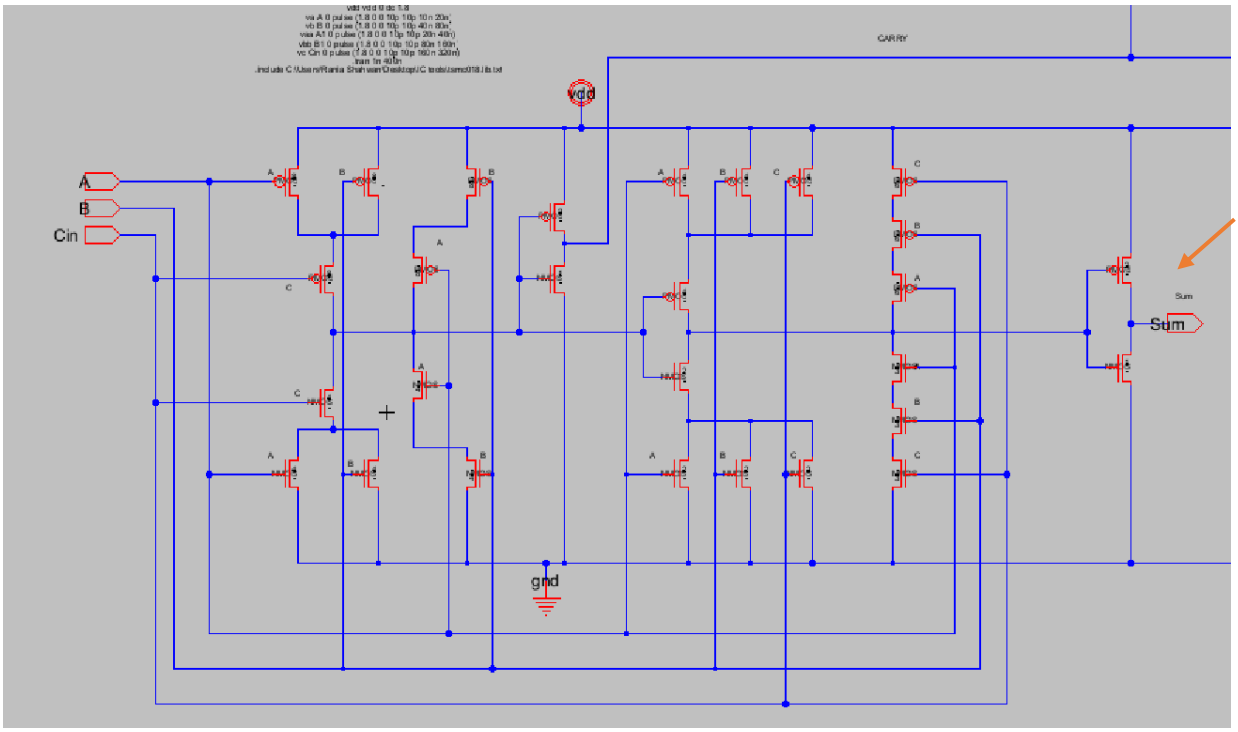

Figure 8: Full adder schematic -first part-

Carry out from the first stage is the input carry for the second stage, the least significant bit of the sum is also generated here.

Cout = (A+B)Cin + AB.

Sum = (Cout)' (A+B+C) + ABC

Each output is followed by an inverter, since CMOS is a not logic.

Second part gives the most significant bit of the sum and the carry out.

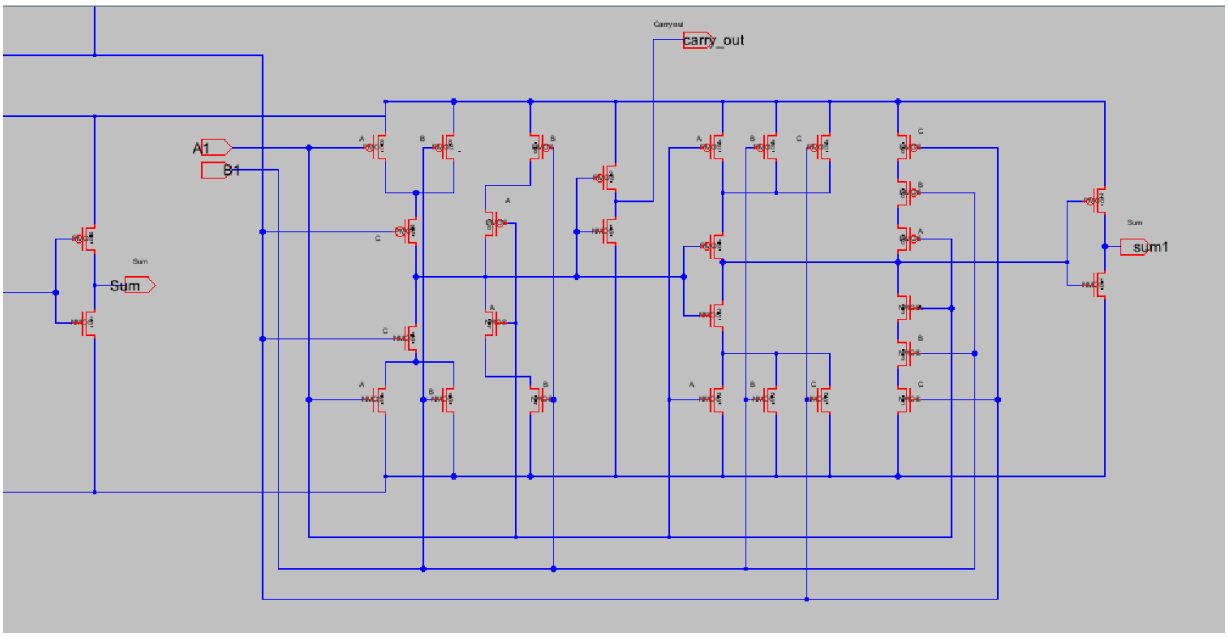

Figure9: Full adder schematic -second part-

Layout Design

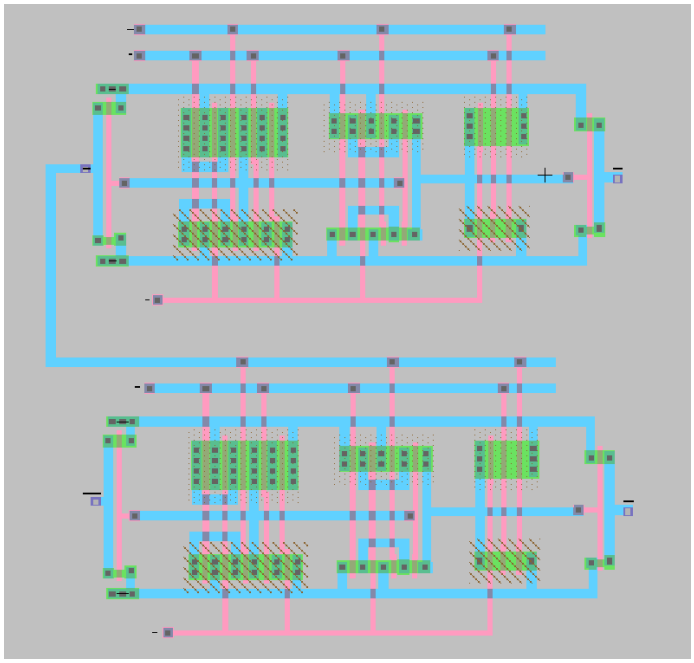

Figure10: Full adder layout

The same topology implemented in schematic was implemented in layout design, the figure below shows the first part of the adder, note that sizing was taken into consideration.

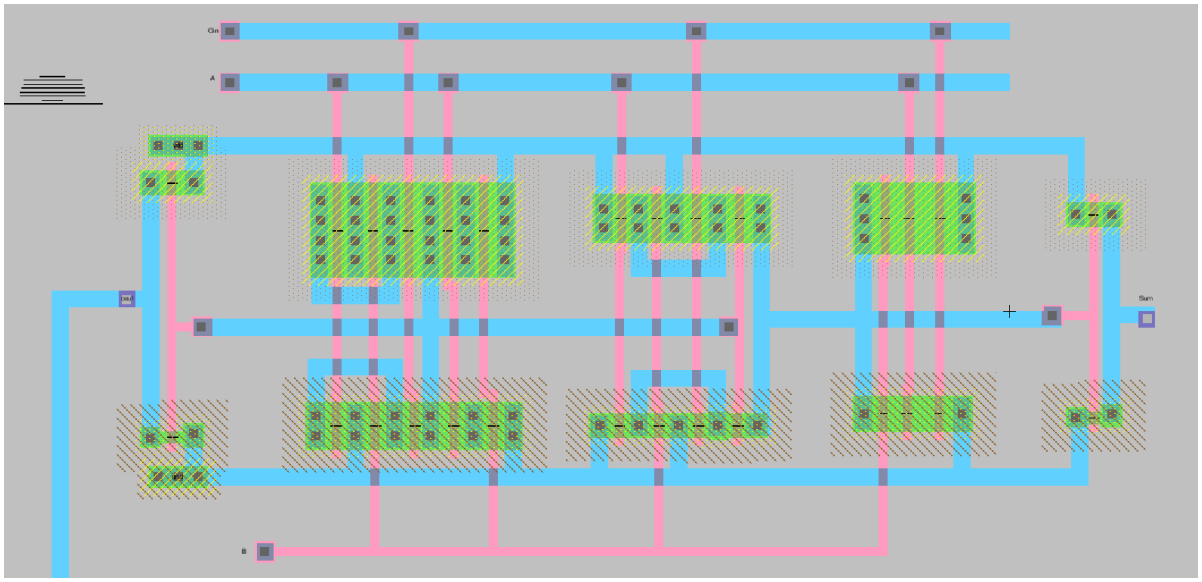

Figure11: Larger view

Simulation Results

After DRC and LVS rules were checked, and the functionally of the circuits were also tested, simulation results can be seen below.

Note that #1 is the most significant bit → (a1 a) + (b1 b) + cin = carry out, (sum1 sum).

For example, at 40ns we have 00+01+0 = 01 and the carry out =0.

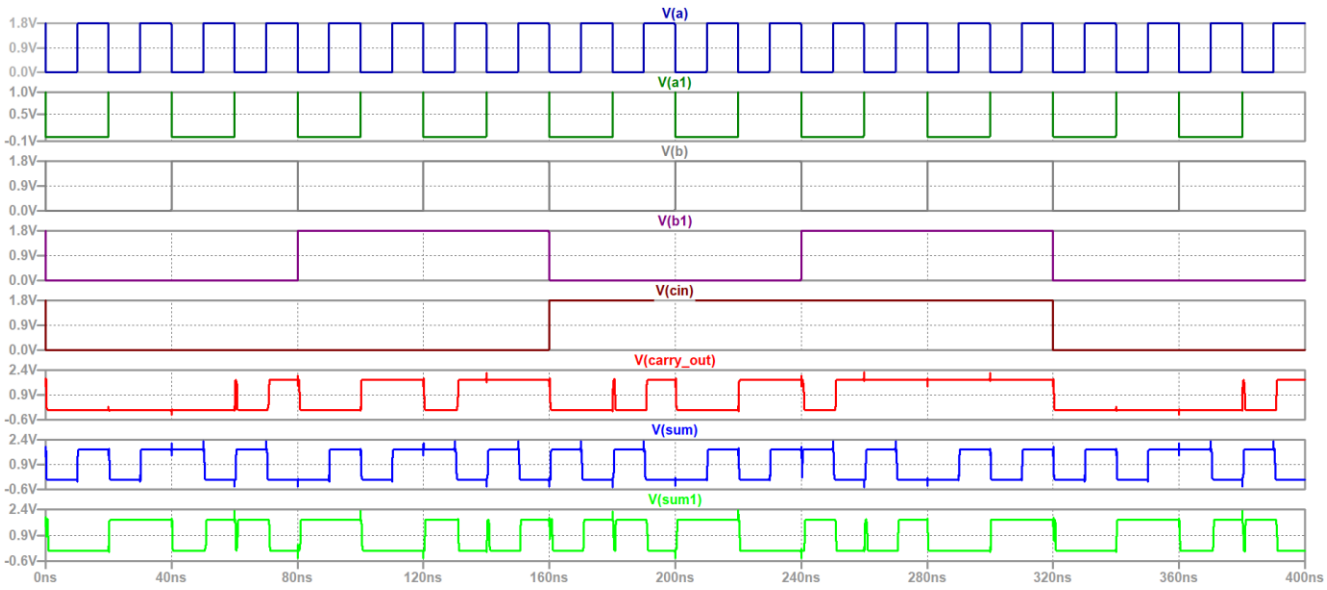

Figure12: Full adder simulation