

# **Major Report**

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ELE 504: Electronic Circuits II

# Abstract

The goal of this project was to design, simulate, implement, and experimentally verify a fully analog, linear VCFG capable of producing symmetrical triangular and square waveforms over two frequency ranges of 100-4400 Hz or 20-880 Hz, with gain and control voltage adjustability. Using OP AMPS and discrete components from  $\pm 12$  V supplies, we designed and built a bistable comparator, an integrator, a voltage-controlled DC-to- $\pm$ DC converter, a frequency-range-selection network, and an amplitude-control subsystem.

The project was executed according to a milestone-based, progressive approach in which subsystems were analyzed theoretically, simulated in MultiSIM, and then verified experimentally on a breadboard. The observations from each milestone showed good correlation between theoretical analysis and experimental measurements, with variances primarily due to op-amp non-idealities, offset voltages, and breadboard parasitics.

In general, the completed system effectively generated triangular and square waveforms with frequency varying linearly with the input control voltage, satisfying the required frequency ranges, voltage limits, and amplitude-control specifications.

# Objectives

The objective of this project was to design and build a fully analog Voltage-Controlled Function Generator (VCFG) capable of producing square and triangular waveforms with the following specifications:

- **Waveform Types:** Symmetrical square and triangular waves.
- **Control Voltage Range:** 0.1 V to 5 V.
- **Frequency Output:**
  - **Range 1:** 100 Hz to  $f_x$  ( $\approx 4400$  Hz for this project).
  - **Range 2:** 20 Hz to  $f_x/5$ .
- **Linear Transfer Function:**  $f_o = K \cdot V_c$
- **Amplitude Control:** 0–8 V peak-to-peak for both waveforms.
- **Power Supply:**  $\pm 12$  V only.
- **Design Constraints:** OP-AMPS and discrete components only; no IC waveform generators.

The final report integrates all milestone work and presents the full theory, design, implementation procedure, and conclusions for the entire VCFG system.

# Introduction

Voltage-controlled waveform generation is essential in measurement systems, analog synthesizers, communication circuits, and automatic control. A triangular/square  $V_o$  (Voltage-Controlled Function Generator) can be built using the combination of:

1. A **bistable comparator** (Schmitt trigger) to generate switching limits.
2. An **integrator** that charges and discharges between these limits.
3. A **control-voltage-dependent current source** to vary the slope of the triangle, and therefore its frequency.

In order to make sure each component of the Voltage Controlled Function Generator, we must design and test each component separately. In this project, the fundamental building blocks were developed incrementally across four milestones:

- **Milestone 1 – Fixed-frequency waveform generator**
- **Milestone 2 – Limiter integration and DC-to- $\pm$ DC converter design**
- **Milestone 3 – Full voltage-controlled triangular/square  $V_{co}$**
- **Milestone 4 – Frequency-range switching and amplitude control**

This systematic approach enabled thorough verification of every subsystem individually before integrating them into the complete VCFG product.

# Theory

## The Inverting Integrator

The key purpose of the Inverting Integrator is to convert the square wave into a triangular wave. Similar to taking a step function and taking integration to get a line with a slope this part of the circuit operates the same way. There is also another special function of this component and that being that it generates a frequency due to the capacitor in the component.

The integrator produces a linear ramp whose slope is determined by:  $\frac{dV}{dt} = \frac{V_{in}}{RC}$

Whenever the integrator output reaches  $V_{TH}$  or  $V_{TL}$ , the bistable comparator toggles, and the integrator begins ramping in the opposite direction.

The current that goes through R is  $i(t) = \frac{V_i(t)}{R}$

Due to the special properties of the capacitor, it can store the charge that goes through and has memory. The voltage across C can be given as:

$$V_C = \frac{1}{C} \int i(t) dt + V_C(t=0)$$

The voltage across the output can be given as:

$$V_{out} = -V_C = -\frac{1}{C} \int i(t) dt + V_C(t=0)$$

Thus, by manipulating the various equations we can find the frequency as the integration is from 0 to t:

$$T = \frac{2(V_{TH} - V_{TL})RC}{L^+} \quad \text{Which gives: } f = \frac{1}{T} = \frac{L^+}{2(V_{TH} - V_{TL})RC}$$

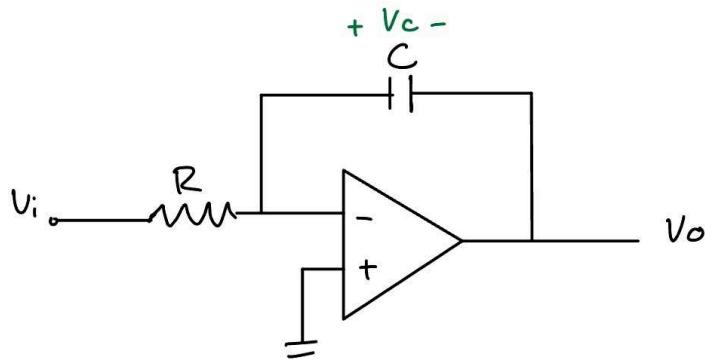


Figure 1.0 - Circuit Diagram of Inverting Integrator

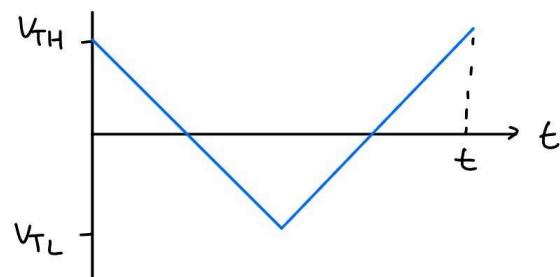


Figure 1.1 Output of Integrator

## The Inverting Bistable Comparator

A Schmitt trigger produces a square waveform that switches at two threshold voltages,  $V_{TH}$  and  $V_{TL}$ . The bistable only has two possible values  $L^+$  and  $L^-$  depending on input voltage. These voltages depend on the feedback resistors and the supply-limited saturation voltages of the op-amp:

$$V_{TH} = \left( \frac{R_1}{R_2} \right) L^+ \quad \text{and} \quad V_{TL} = \left( \frac{R_1}{R_2} \right) L^-$$

The output square wave acts as the driving signal for the integrator.

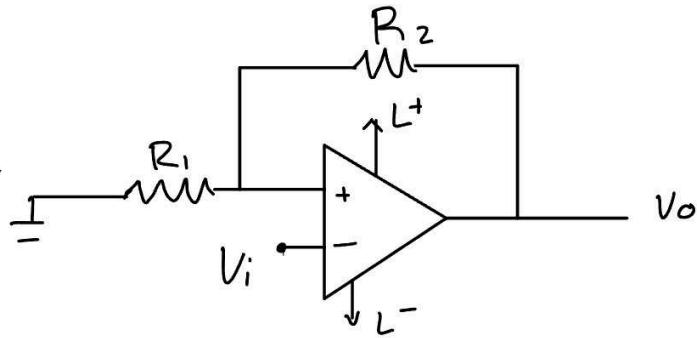


Figure 2.0 - Circuit diagram of an inverting Bistable

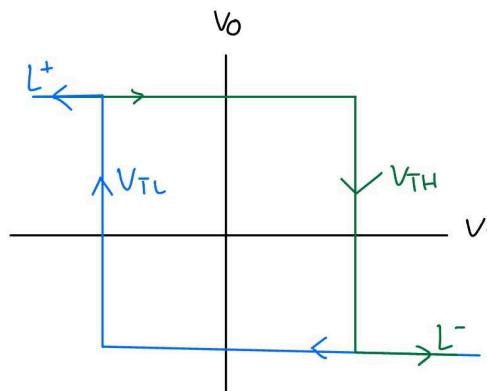


Figure 2.1 - Input and Output Relationship for an inverting Bistable

## The DC to ± Dc Convertor

To achieve linear frequency control with the input control voltage  $V_c$ , a digital-switch-based converter generates a symmetrical  $\pm V_c$  waveform. This waveform is applied to the integrator input so that:

$$f \propto V_c$$

The converter uses:

- A 6.3 V peak square wave to toggle MOSFET/BJT switches.
- Diodes to steer the control voltage into positive or negative polarity.
- A capacitor smoothing network.

As a result, the integrator receives  $+ V_c$  during one half-cycle and  $- V_c$  during the other.

### Digital Switch

The DC to ± Dc Convertor has a gain of 1 and the phase of the output depends on the digital switch if its open or closed. If the switch is closed then it will output with a phase change of 180°/flipped. If the switch is open then there is change in the phase and the output is simply the input. The switch is created using a NPN BJT, a diode and two resistors. The switch will be active (closed) when  $V_{BE} > 0.7$  V and the switch is off (open) when  $V_{BE} < 0.7$  V.

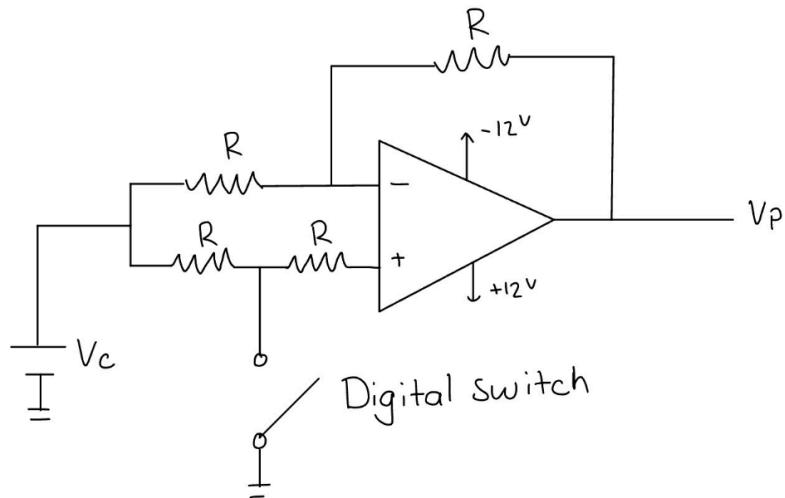


Figure 3.0 - Circuit diagram for DC to ± Dc Convertor

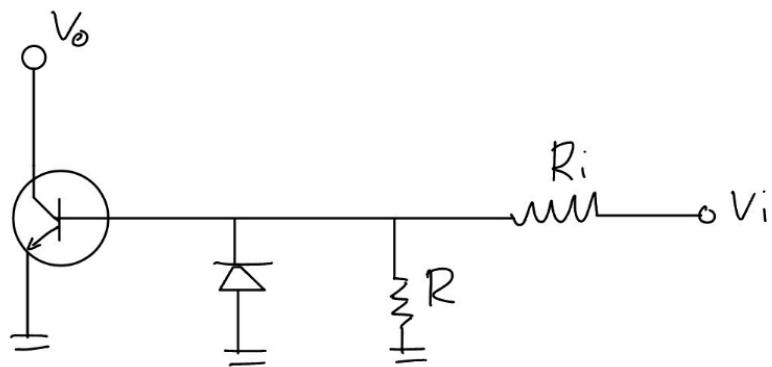


Figure 3.1 - Circuit diagram for digital switch using an NPN BJT

### Frequency Range Control

Because the frequency is inversely proportional to the input resistance of the integrator:

$$f \propto \frac{1}{R_{in}}$$

Changing a single resistor allows switching between Range 1 and Range 2:

- **Range 1:**  $R = R_o$
- **Range 2:**  $R = 5R_o$   
(reduces frequency by a factor of 5)

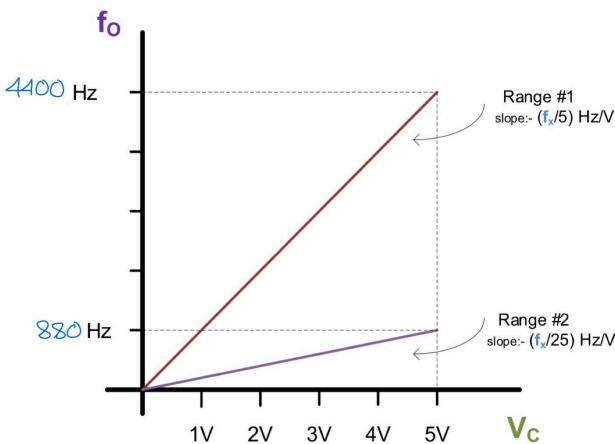


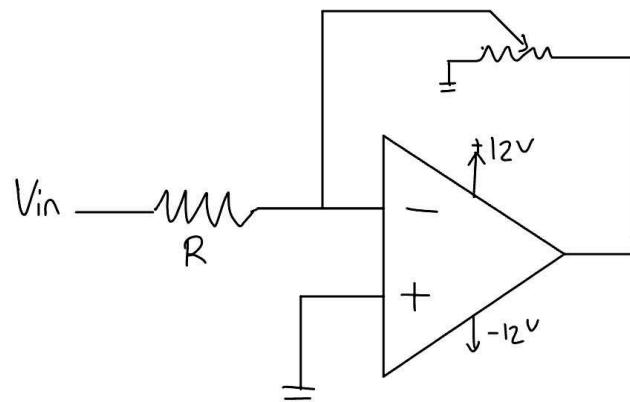
Figure 4.0 frequency depending on  $V_c$

## Amplitude Control Output Stage

To obtain controlled amplitude from 0–8 V<sub>pp</sub>, a non-inverting amplifier with a potentiometer-adjustable gain is used by keeping  $R_{in}$  fixed using a potentiometer as  $R_f$  we can control the gain:

$$V_{out} = \left(1 + \frac{R_f}{R_{in}}\right) V_{signal}$$

This amplification is applied independently to the triangular and square outputs.



*Figure 5.0 circuit diagram of Amplitude control circuit*

# Design Analysis

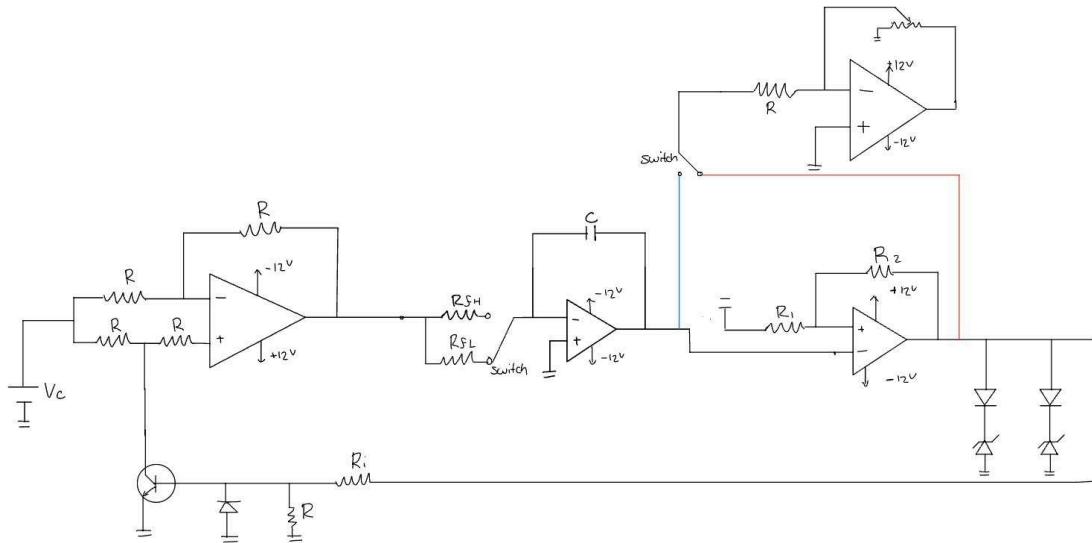


Figure 6.0 Complete circuit diagram of VCFG

## The Inverting Integrator

The inverting integrator controls the frequency throughout the entire circuit. Changing the resistor gives a different frequency. The value of the resistor can be found by rearranging the frequency equation for R since it has all the values needed such as the frequency (4400Hz), V<sub>c</sub> (5v) and capacitance of C = 0.01μF. We get a resistor value of 7.1 kΩ which we don't have in the lab so we used a 6.8 kΩ which gives a frequency of about 4700 kΩ. To get a maximum frequency of 880 Hz (f/5) we can just simply multiply the resistor value by 5 to get 35.5 kΩ. We can easily choose between the 2 frequencies by simply switching between the two resistors.

## Bistable Design

The values of R<sub>1</sub> and R<sub>2</sub> are determined by using the equation of the Bistable by plugging in V<sub>o</sub>=6.3v and V<sup>+</sup>=4v, by using 27 kΩ we are able to solve for R<sub>2</sub> which gives 47 kΩ. To ensure the output of the bistable is limited to only 6.3V we use two 1N4148 diodes and two 1N4734A Zener diodes. Zener diodes (5.6 V) and diodes (0.7V) were added in the feedback loop of the bistable to clamp output to ±6.3 V, ensuring consistent threshold voltages independent of op-amp saturation characteristics.

## The DC to ± Dc Convertor

Since the Convertor has a gain of one, all resistors should be the same, while the resistor closest to the positive terminal should be set to a lower resistor to block unwanted feedback. The resistor we used in the design is 10 kΩ, as they are abundant in the lab kit, along with a 1 kΩ in the positive terminal.

Along with the Convertor, there is a digital switch which we designed using available components in the lab kit, 2N3904 NPN BJT, a 100 Ω in series, and a 1kΩ and a 1N4148 diode connected in parallel to the base and the ground.

## Amplitude Control Output Stage

A potentiometer-controlled non-inverting amplifier was added to allow:

- 0–100% amplitude
- Independent adjustment for triangular and square outputs

Simulations confirmed proper operation across all  $V_c$  values and both frequency ranges. The potentiometer was in the feedback connection.

## Experiment Procedure

### Simulation Procedure

For each milestone:

1. Circuits were captured in MultiSIM.
2. Threshold voltages, saturation values, and waveforms were measured.
3.  $V_c$  was swept from 1 V to 5 V.
4. Frequency measurements were made for both triangular and square wave outputs.
5. The gain-control stage was tested at multiple potentiometer settings.
6. Frequency-range switching was verified.

### Breadboard Procedure

1. ±12 V rails provided using lab bench supplies.
2. Each subsystem was wired independently before full integration.

3. Oscilloscope measurements were taken for:

- $V_{TH}$  and  $V_{TL}$
- Square wave amplitude
- Triangular wave symmetry
- Full frequency sweep
- Both gain and range switching

4. Component values were adjusted as needed to compensate for:

- Op-amp offset
- Breadboard parasitics
- Slew-rate limitations

5. Final integrated system testing verified full compliance with specifications.

## Milestone Procedure:

### **Milestone 1 – Fixed-Frequency Generator**

The first milestone established the core topology:

1. A bistable comparator generating a stable square wave at  $f_x$ .
2. An integrator producing the corresponding triangular wave.
3. Component values selected to achieve the assigned frequency (approximately 4400 Hz).
4. Use of  $\pm 12$  V supplies and a realistic output swing of  $\pm 10.5$  V was considered for design.

Theoretical thresholds, expected waveforms, and component sizing were calculated using the hysteresis and integrator equations. The circuit was simulated for verification before physical implementation.

### **Milestone 2 – Precise Limiter and DC-to- $\pm$ DC Converter**

This milestone introduced two essential subsystems:

#### A. Limiter-Enhanced Fixed Frequency Generator

Zener diodes (5.6 V) were added in the feedback loop of the bistable to clamp output to  $\pm 6.3$  V, ensuring consistent threshold voltages independent of op-amp saturation characteristics.

#### B. DC-to- $\pm$ DC Converter

Designed around:

- A switching network driven by an external  $\pm 6.3$  V square wave
- Steering diodes
- A controlled  $V_c$  input

This subsystem outputs  $+ V_c$  during one half cycle and  $- V_c$  during the next, creating the necessary polarity-reversing control input for linear frequency modulation.

Simulations demonstrated proper polarity inversion and proportional output levels.

### **Milestone 3&4 – Integrated Linear VCFG**

In this milestone, the bistable/integrator from Milestone 1–2 was integrated with the DC-to- $\pm$ DC converter. Key considerations:

- The integrator input resistor was modified ( $\sim 6.8\text{--}7.1$  k $\Omega$ ) to achieve the correct  $f_x \approx 4400\text{Hz}$ .
- Linear dependence between frequency and control voltage was demonstrated across  $V_c = 1 - 5V$ .

The triangular and square waveforms scaled correctly in frequency while maintaining symmetry.

### **Milestone 5 – Frequency Range and Gain Control**

This milestone added two final features:

#### A. Frequency Range Switch

- Range 1:  $R = 12$  k $\Omega$
- Range 2:  $R = 60$  k $\Omega$  (approx  $5\times$  greater  $\rightarrow 1/5$  frequency)

This meets project specifications for required frequency ranges.

#### B. Output Gain Control

A potentiometer-controlled non-inverting amplifier was added to allow:

- 0–100% amplitude
- Independent adjustment for triangular and square outputs

Simulations confirmed proper operation across all  $V_c$  values and both frequency ranges.

## Results and Observations

- The fixed-frequency generator produced clean triangular and square waveforms.
- Adding Zener limiters ensured precise and repeatable threshold voltages.
- The DC-to- $\pm$ DC converter behaved as expected, though improper diode orientation initially caused clipping in the negative half-cycle before being corrected.
- When integrated, the VCFG demonstrated a linear increase in frequency with increasing  $V_c$ , consistent with the theoretical  $f_o = K \cdot V_c$  relation.
- The full system achieved:
  - Proper operation over both frequency ranges
  - Stable triangular and square outputs
  - Smooth amplitude control
- Minor discrepancies between simulation and hardware were attributed to:
  - Op-amp input offset voltages
  - Slew-rate limitations (especially LM741)
  - Tolerance differences in resistors
  - Measurement inaccuracies in lab oscilloscopes

Despite these, the system met all required specifications.

### Milestone 1:

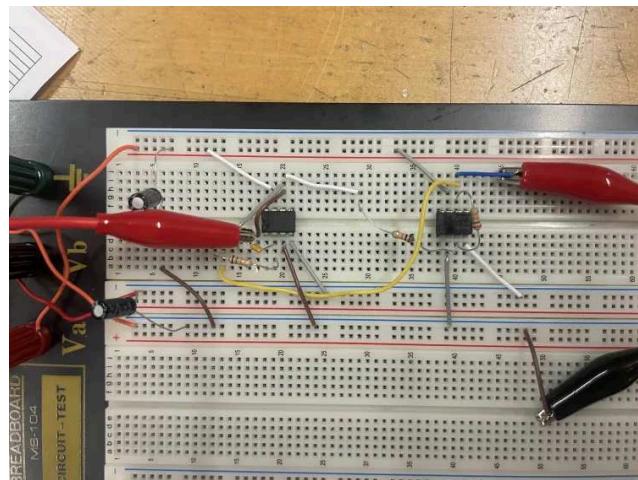


Figure 1.A In lab Circuit for Integrator and Bistable

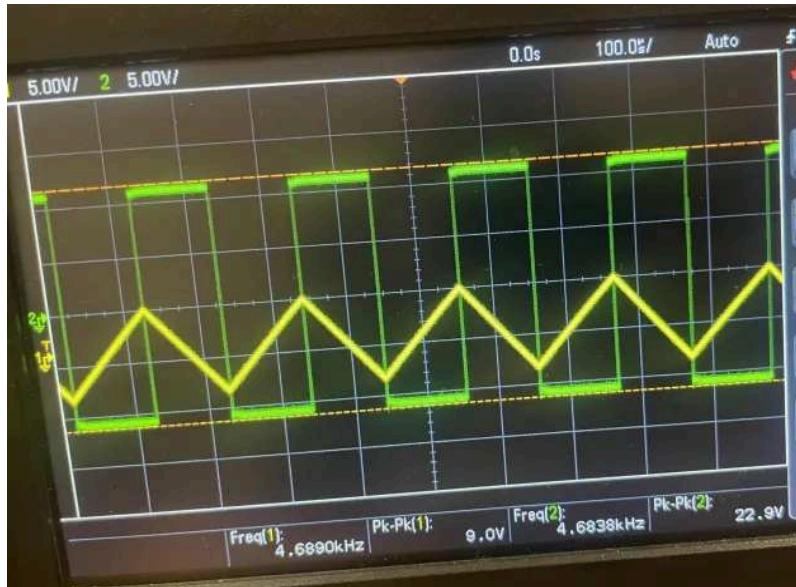


Figure 1.B.1 Waveform for Integrator and Bistable

|           | $R$            | $R_1$        | $R_2$        | $V_{TH}$ | $V_{TL}$ | $L^+$  | $L^-$   | $T$             | $f$    |
|-----------|----------------|--------------|--------------|----------|----------|--------|---------|-----------------|--------|
| Pre-Lab   | 11.4k $\Omega$ | 10k $\Omega$ | 20k $\Omega$ | 3.261    | -3.74    | 9.915  | -8.951  | 230.932 $\mu$ s | 4330Hz |
| In-Lab    | 15k $\Omega$   | 10k $\Omega$ | 27k $\Omega$ | 4.208V   | -4.792V  | 11.65V | -11.25V | 213.265 $\mu$ s | 4689Hz |
| corrected | 14.7k $\Omega$ | 10k $\Omega$ | 27k $\Omega$ | 4.208V   | -4.729V  | 11.65V | -11.25  | 227.273 $\mu$ s | 4400Hz |

Figure 1.C Results for Integrator and Bistable

### Milestone 2:

#### Part A: Implementing clamping diodes

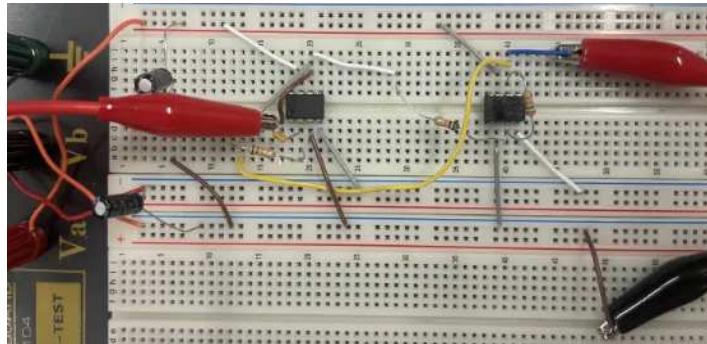


Figure 2.A In lab Circuit for Integrator and Bistable with clamping diodes

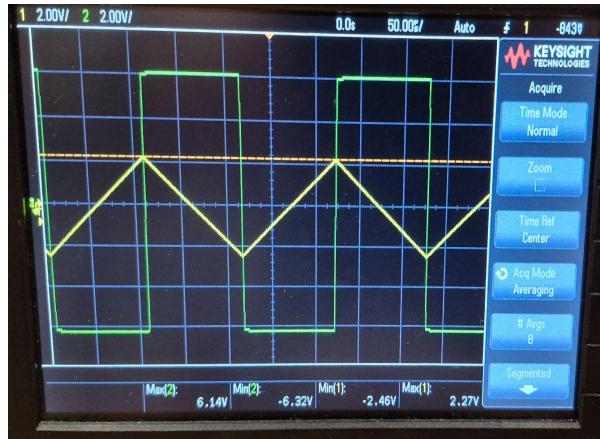


Figure 2.B.0 Waveform Showing  $V_{TH}$  &  $L^+$

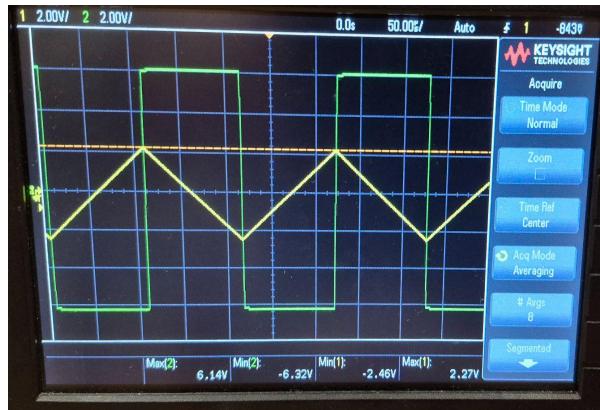


Figure 2.B.1 Waveform Showing  $V_{TL}$  &  $L^-$

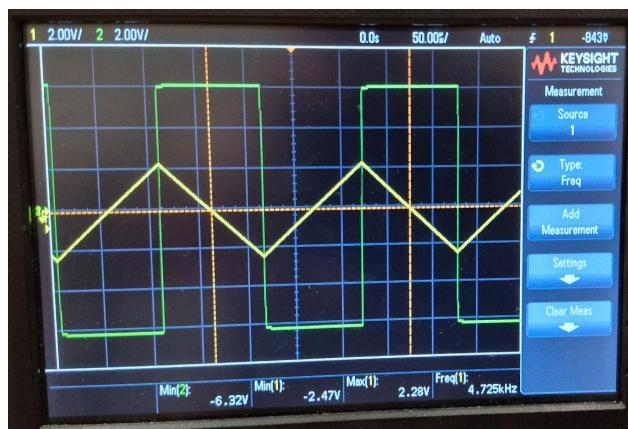


Figure 2.B.2 Waveform Showing frequency

|         | $R$  | $R_1$ | $R_2$ | $V_{TH}$ | $V_{TL}$ | $L^+$  | $L^-$   | $T$       | $f$    |
|---------|------|-------|-------|----------|----------|--------|---------|-----------|--------|
| Pre-Lab | 15kΩ | 10kΩ  | 27kΩ  | 2.016V   | -2.027V  | 6.160V | -6.160V | 224.194μs | 4460Hz |
| In-Lab  | 15kΩ | 10kΩ  | 27kΩ  | 2.27V    | -2.46V   | 6.14V  | -6.32V  | 211.640μs | 4725Hz |

Figure 2.C Results for Integrator and Bistable with clamping diodes

### Part B: Implementing DC to ± Dc Convertor with digital switch

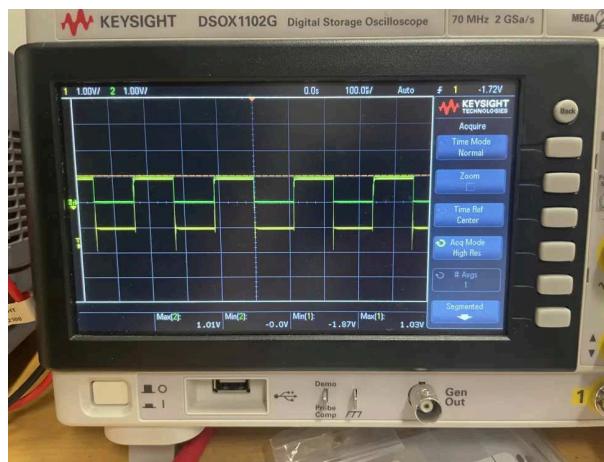


Figure 2.C.1 Waveform DC to ± DC Convertor at 1V

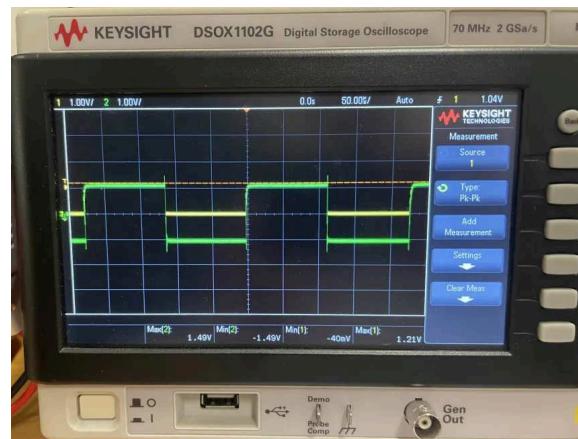


Figure 2.C.2 DC to ± DC Convertor at 2V

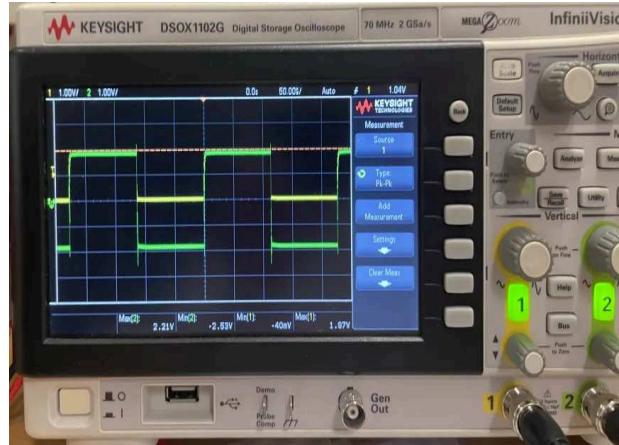


Figure 2.C.3 DC to ± DC Convertor at 3V

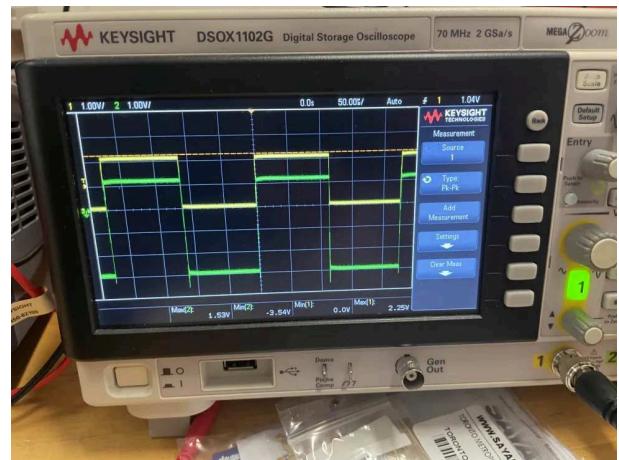


Figure 2.C.4 DC to ± DC Convertor at 4V

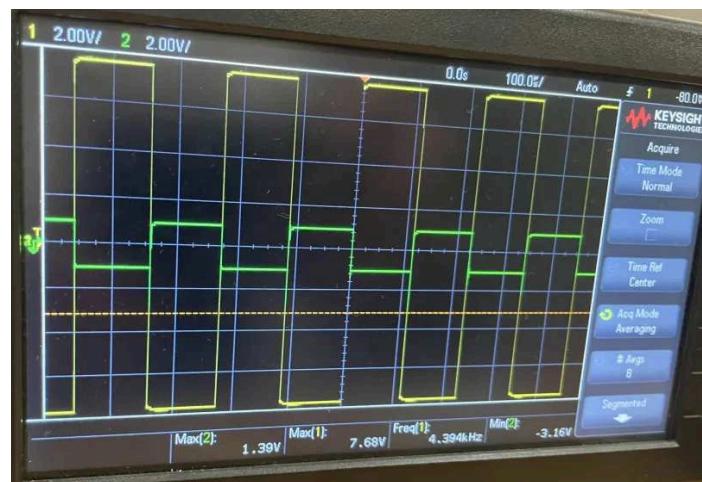


Figure 2.C.5 DC to ± DC Convertor at 5V

### Milestone 3-4:

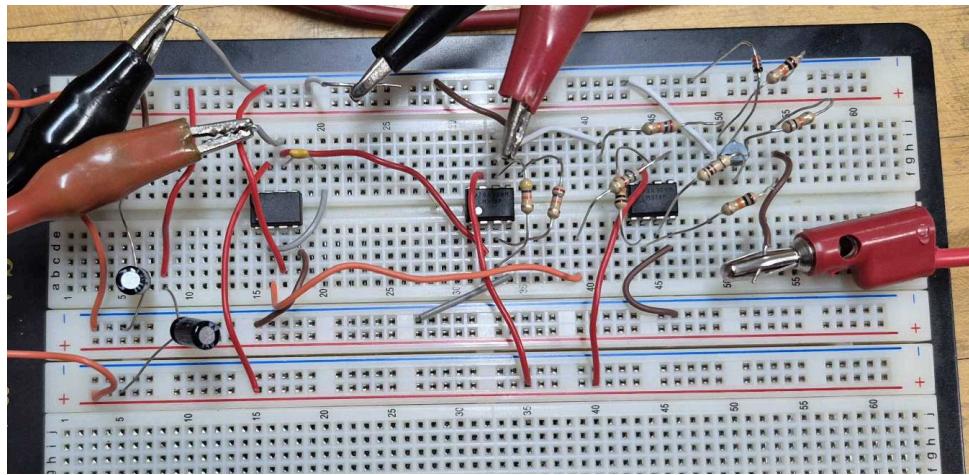


Figure 3.A In lab Circuit for Integrator and Bistable and DC to  $\pm$  DC Convertor



Figure 3.B.1 Waveform for Integrator and Bistable and DC to  $\pm$  DC Convertor at 1V

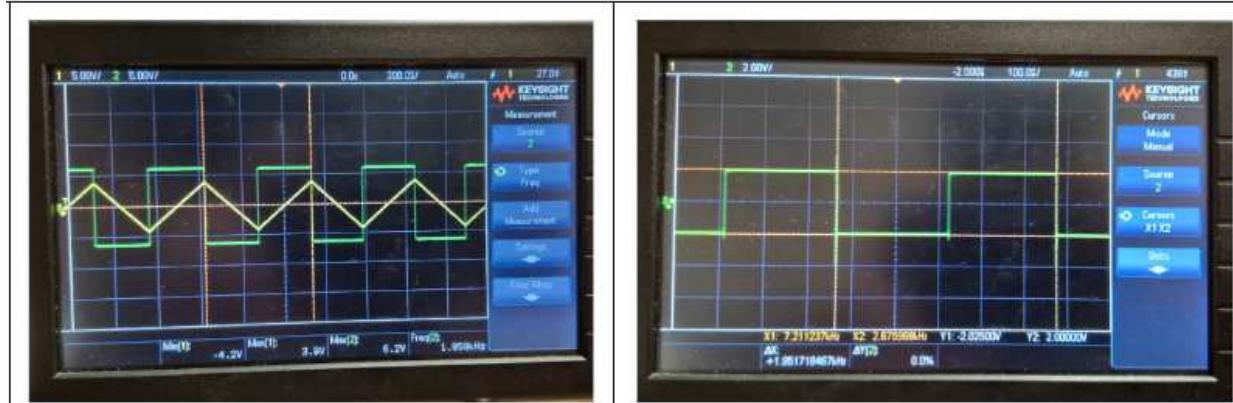


Figure 3.B.2 Waveform for Integrator and Bistable and DC to  $\pm$  DC Convertor at 2V

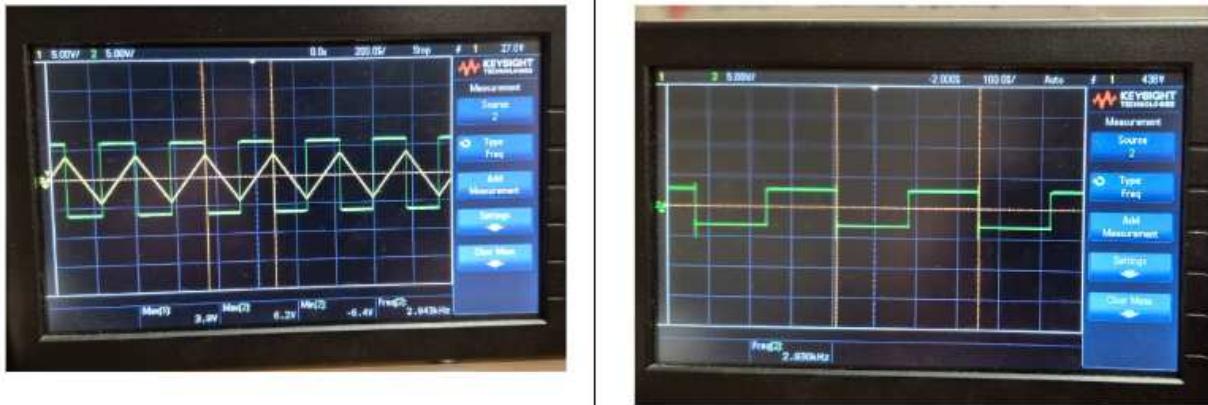


Figure 3.B.3 Waveform for Integrator and Bistable and DC to  $\pm$  DC Convertor at 3V

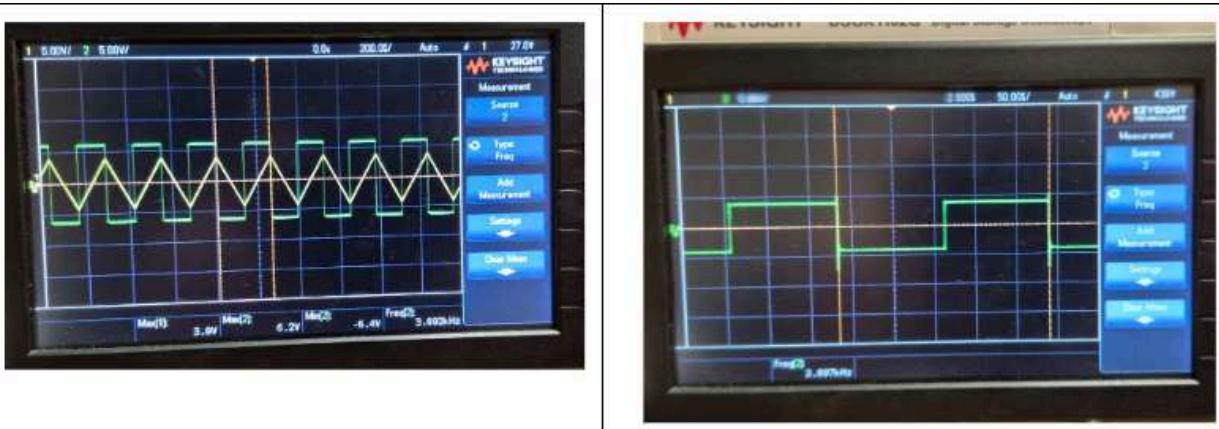


Figure 3.B.4 Waveform for Integrator and Bistable and DC to  $\pm$  DC Convertor at 4V

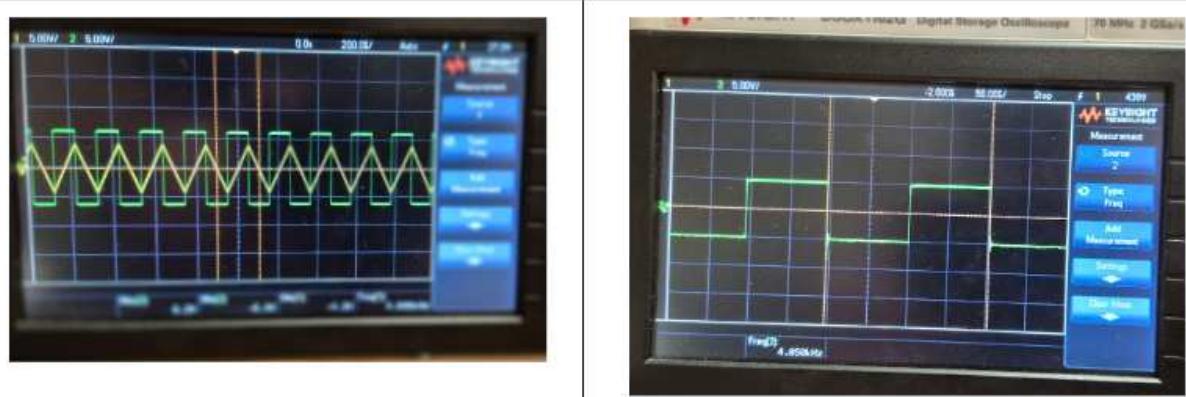


Figure 3.B.5 Waveform for Integrator and Bistable and DC to  $\pm$  DC Convertor at 5V

| $V_c$ | $R$  | $R_1$ | $R_2$ | $V_{TH}$ | $V_{TL}$ | $L^+$ | $L^-$ | $T$                   | $f$      |
|-------|------|-------|-------|----------|----------|-------|-------|-----------------------|----------|
| 1v    | 6.8K | 27k   | 47K   | 3.8V     | -4.1V    | 6.2v  | -6.4v | $1.03 \times 10^{-3}$ | 971.3Hz  |
| 2v    | 6.8K | 27k   | 47K   | 3.9V     | -4.2V    | 6.2v  | -6.4v | $5.1 \times 10^{-4}$  | 1.959Khz |
| 3v    | 6.8K | 27k   | 47K   | 3.9V     | -4.2v    | 6.2v  | -6.4v | $3.40 \times 10^{-4}$ | 2.943Khz |
| 4v    | 6.8K | 27k   | 47K   | 3.9V     | -4.3V    | 6.2v  | -6.4v | $2.57 \times 10^{-4}$ | 3.892Khz |
| 5v    | 6.8K | 27k   | 47K   | 4V       | -4.3V    | 6.2v  | -6.4v | $2.13 \times 10^{-4}$ | 4.859kHz |

Figure 3.C *Waveform Recorded Results for Integrator and Bistable and DC to  $\pm$  DC Convertor Circuit*

#### Milestone 5:

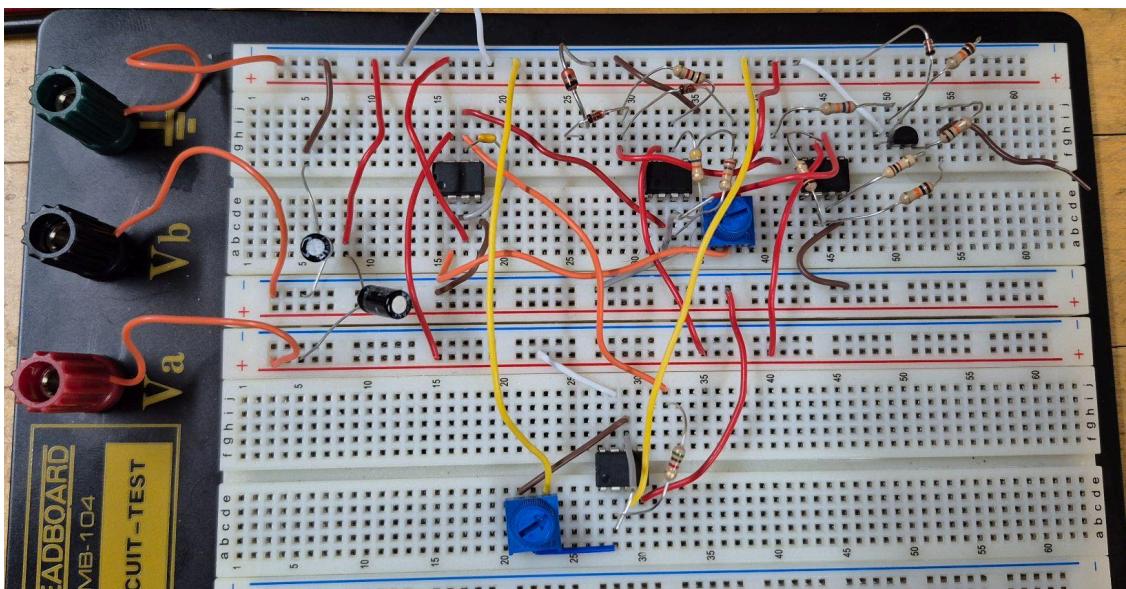


Figure 4.A Complete physical circuit used in lab

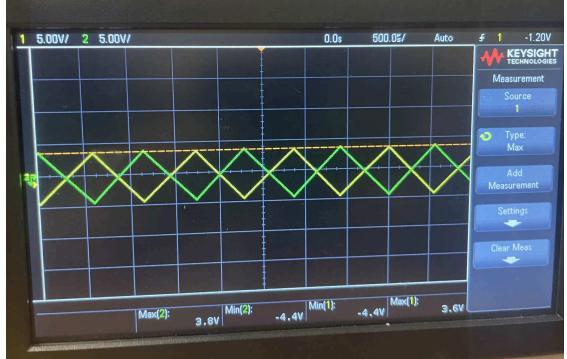
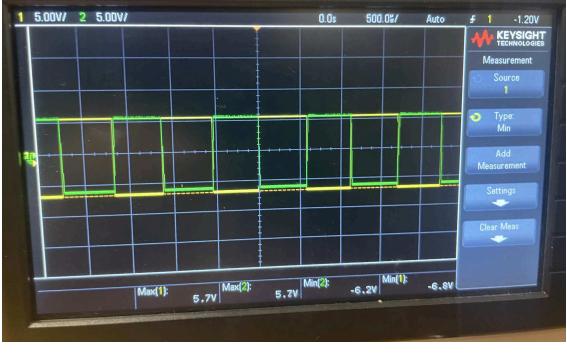
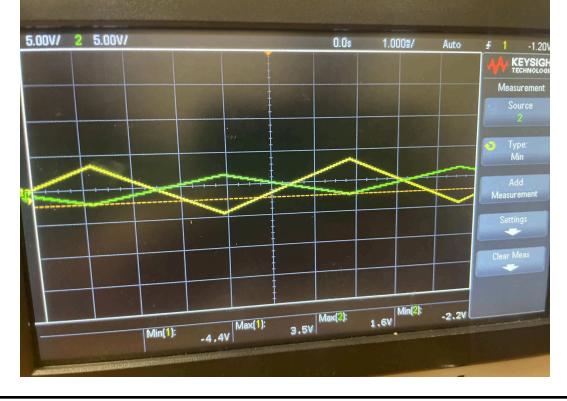
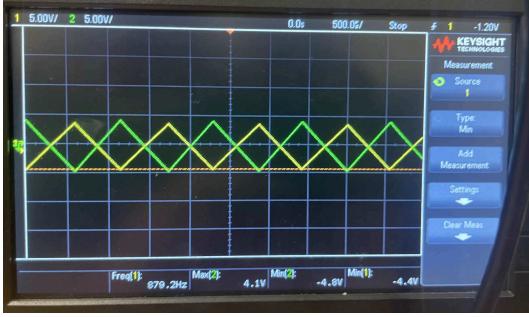
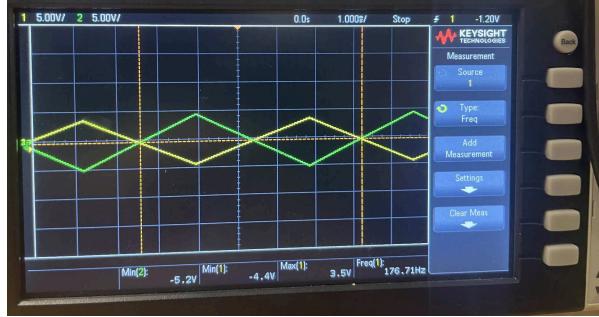
| Vc = 1                          |  |  |
|---------------------------------|--|--|
| Gain                            | Triangle   | Square   |
| 100%                            |   |    |
| 50%                             |  |   |
| Frequency - range 1<br>12k Ohms |  |  |
| Frequency - range 2<br>60k Ohms |  |  |

Figure 4.B.1 Complete circuit at 1V

$V_C = 3$

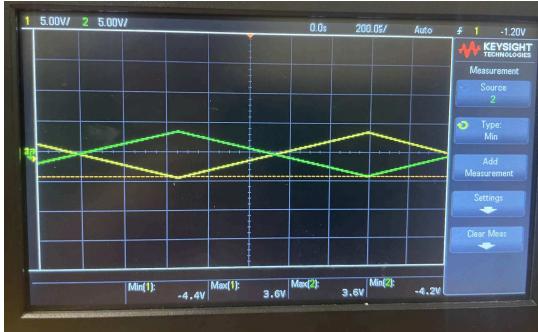
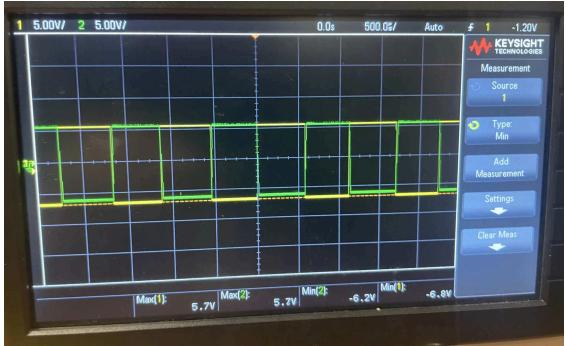
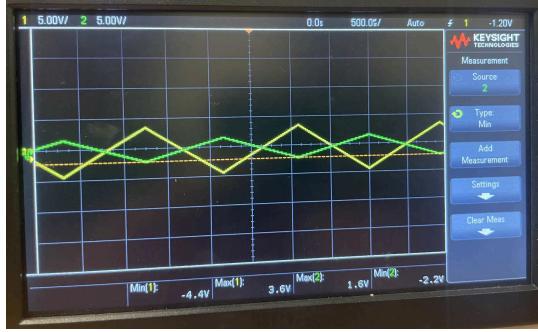
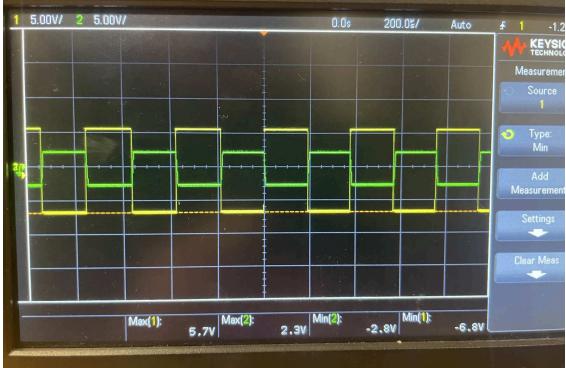
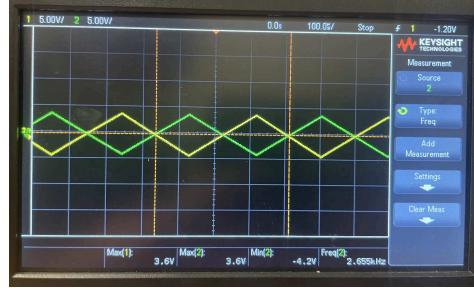
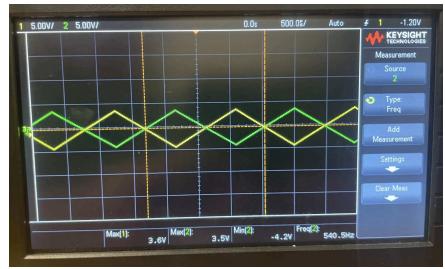
| Gain                            | Triangle   | Square   |
|---------------------------------|--|--|
| 100%                            |   |    |
| 50%                             |  |   |
| Frequency - range 1<br>12k Ohms |  |  |
| Frequency - range 2<br>60k Ohms |  |  |

Figure 4.B.2 Complete circuit at 3V

$V_C = 5$

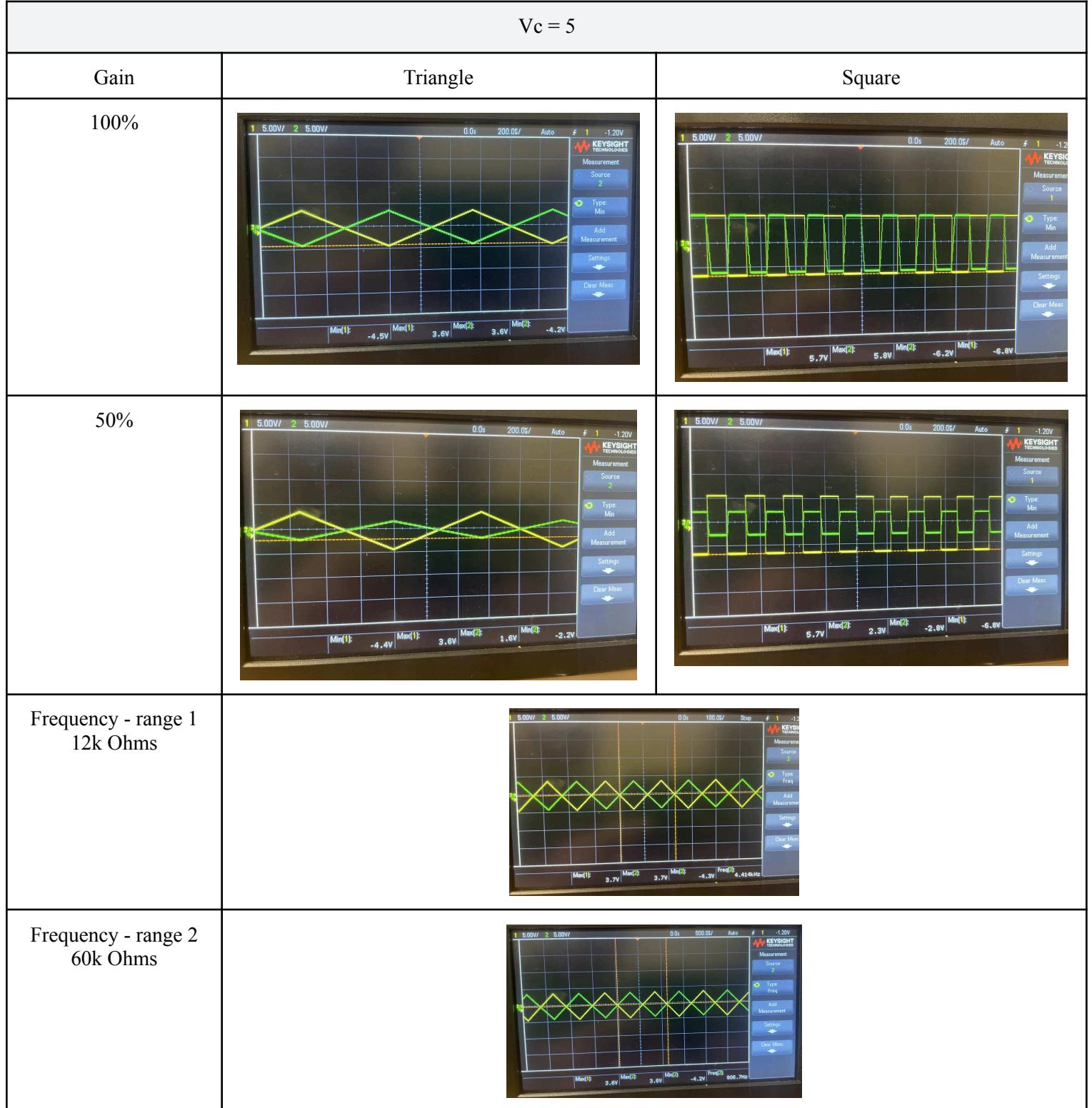


Figure 4.B.2 Complete circuit at 5V

| Vc = 1V                    |                 |                 |                |                |
|----------------------------|-----------------|-----------------|----------------|----------------|
| Gain                       | V <sub>TH</sub> | V <sub>TL</sub> | L <sup>+</sup> | L <sup>-</sup> |
| 100%                       | 4.2v            | -4.8v           | 5.7v           | -6.2v          |
| 75%                        | 2.7v            | -3.3v           | 4.3v           | -4.7v          |
| 50%                        | 1.6v            | -2.2v           | 2.3v           | -2.8v          |
| 25%                        | 600mv           | -1.1v           | 1.4v           | -1.9v          |
| Frequency - range 1 (12kΩ) | 880Hz           |                 |                |                |
| Frequency - range 2 (60kΩ) | 176Hz           |                 |                |                |

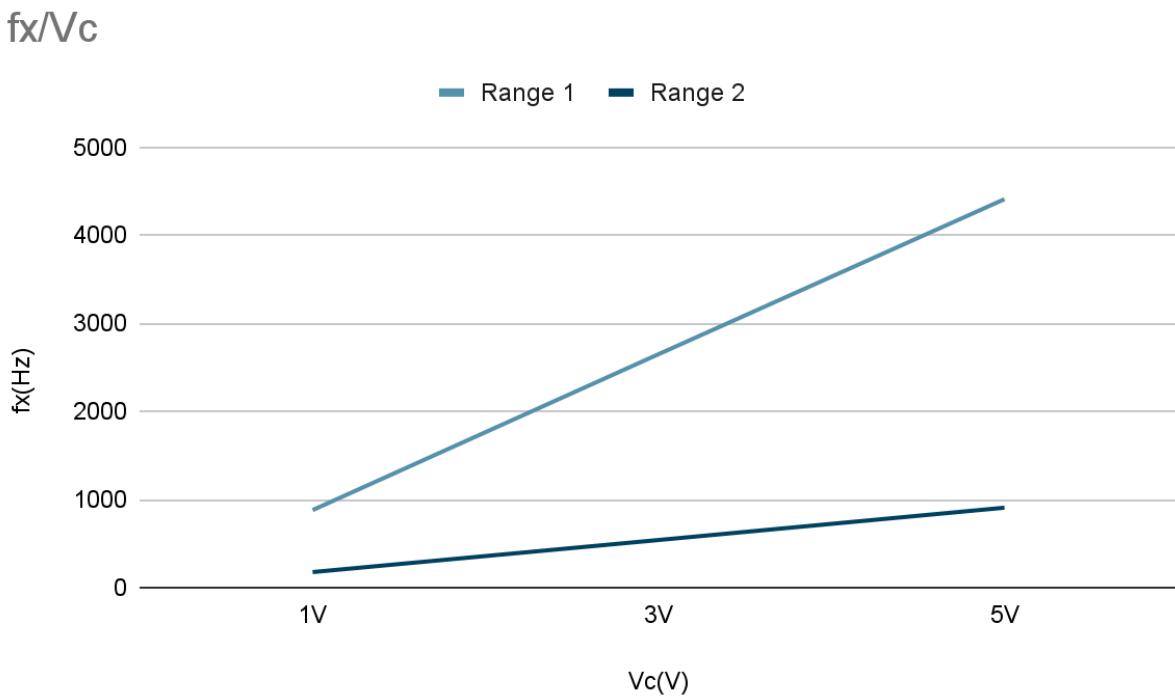
Figure 4.C.1 Complete circuit at 1V

| Vc = 3V                    |                 |                 |                |                |
|----------------------------|-----------------|-----------------|----------------|----------------|
| Gain                       | V <sub>TH</sub> | V <sub>TL</sub> | L <sup>+</sup> | L <sup>-</sup> |
| 100%                       | 3.6v            | -4.2v           | 5.8v           | -6.2v          |
| 50%                        | 1.6v            | -2.2v           | 2.3v           | -2.8v          |
| Frequency - range 1 (12kΩ) | 2.65KHz         |                 |                |                |
| Frequency - range 2 (60kΩ) | 540Hz           |                 |                |                |

Figure 4.C.2 Complete circuit at 3V

| Vc = 5V                    |                 |                 |                |                |
|----------------------------|-----------------|-----------------|----------------|----------------|
| Gain                       | V <sub>TH</sub> | V <sub>TL</sub> | L <sup>+</sup> | L <sup>-</sup> |
| 100%                       | 3.6v            | -4.2v           | 5.8v           | -6.2v          |
| 50%                        | 1.6v            | -2.2v           | 2.3v           | -2.8v          |
| Frequency - range 1 (12kΩ) | 4.41KHz         |                 |                |                |
| Frequency - range 2 (60kΩ) | 907Hz           |                 |                |                |

Figure 4.C.3 Complete circuit at 5V



*Figure 4.D.1 Relationship between frequencies and voltages*

## Conclusion and Recommendations

Based on the results throughout this project and seen above, this design project was a success and met all requirements. The output waveforms of the final Voltage-controlled function Generator meet all the specifications and limitations presented throughout the lab, with high accuracy and similarity with the simulations and very low distortions. All the minor discrepancies can be attributed to the resistor allowances and the non-ideal characteristics of the Op Amp.

If we were required to reattempt the project and the design, there are several things we would keep in mind.

1. Always use capacitors in parallel with the voltage sources to minimize distortion and disturbances.
2. Make sure all pins of the Op amp are connected correctly prior to starting the testing. This ensures that the Op amps do not burn out
3. Make sure resistor values are high enough to prevent unwanted current to flow throughout the circuit, causing incorrect readings and the Op Amp overheating.
4. When debugging the circuit, use the oscilloscope to make sure you're getting the correct readings, and always make sure the Op Amp is not fried and functions as it should be.
5. Make sure the circuit is neat and organized. This ensures that the circuit is easier to build upon in the future and is easier to debug.

# Appendix

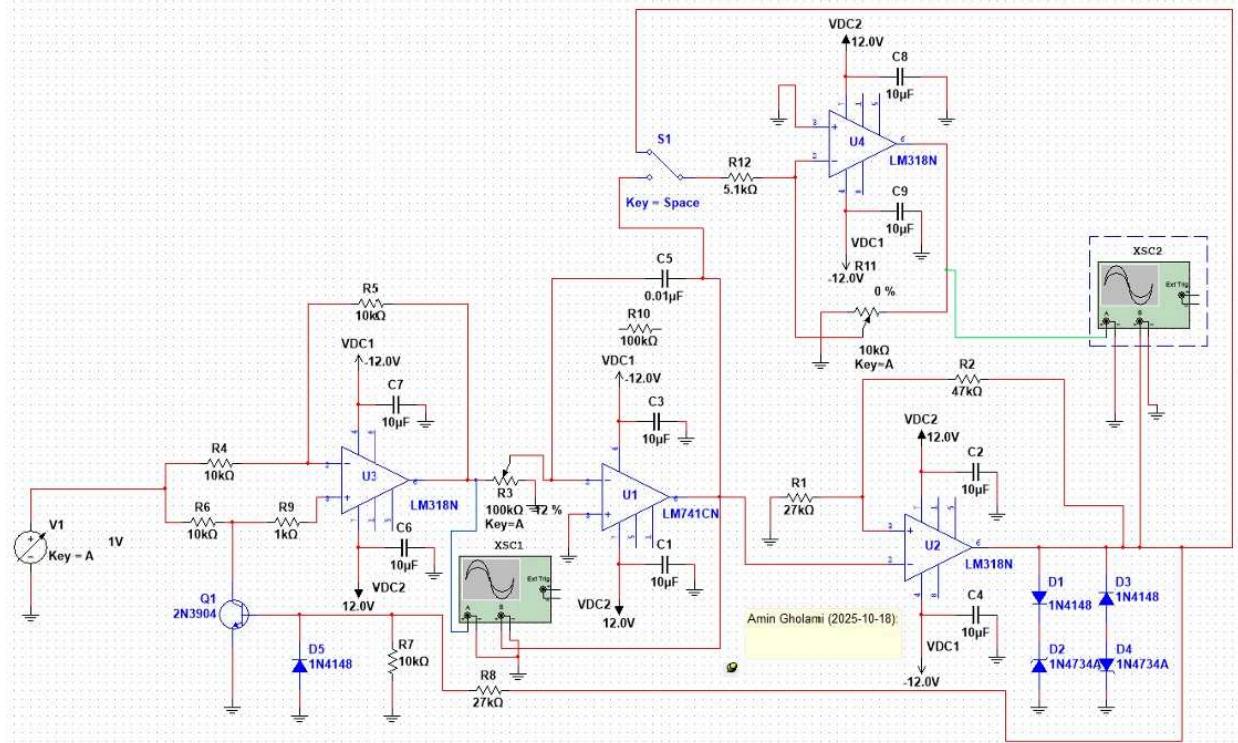


Figure 5.0 Schematic of the complete circuit on MultiSim

## Part list:

1.  $10\text{k}\Omega$
2.  $1\text{k}\Omega$
3.  $27\text{k}\Omega$
4.  $47\text{k}\Omega$
5.  $5.1\text{k}\Omega$
6.  $10\text{k}\Omega$  Potenameter
7.  $100\text{k}\Omega$  Poternameter
8.  $0.01 \mu\text{F}$  capacitor
9. 1N4148 0.7V diode
10. 1N4734A 5.6V Zener diode
11. 2N3904 NPN BJT transistor
12. LM741CN Operational amplifier
13. LM318N Operational amplifier

## Required tools for this experiment:

1.  $\pm 12\text{V}$  Power supply
2. 0V- 5V DC source
3. Oscilloscope