****

**Format No. QSP/7.1/01.F01 (B) Issue No.05 Rev. No 5 Dated: July 22, 2018**

**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**UNIVERSITY OF PETROLEUM & ENERGY STUDIES**

**College of Engineering Studies**

**Dehradun**

**COURSE PLAN**

Program : B. Tech – CS - (CCVT)

Course : Computer System Architecture.

Course Code : CSEG 2004

No. of credits : 3 (2-Offline, 1-Online)

Semester : III

Session : 2018-19

Batch : 2017-21

Prepared by : Ms. Avita Katal

Email : akatal@ddn.upes.ac.in

**Approved By**

HOD/ Prog. Head

UPES Campus Tel : +91-135-2770137

“Energy Acres” Fax : +91 135- 27760904

P.O. Bidholi, , Dehradun

**COURSE PLAN**

1. **PREREQUISITE:**
   1. Basic Knowledge of Computers.
2. **PROGRAM OUTCOMES (POs) and PROGRAM SPECIFIC OUTCOMES (PSOs) for Cloud Computing and Virtualization Technologies:**

**B1. PROGRAM OUTCOMES (POs)**

**PO1 Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

**PO2 Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

**PO3 Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

**PO4 Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

**PO5 Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

**PO6 The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

**PO7 Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

**PO8 Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

**PO9 Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

**PO10 Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

**P11 Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one’s own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

**P12 Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

**B2. Program Specific Outcomes (PSOs)**

**PSO 13** Perform system and application programming using computer system concepts, concepts of Data Structures, algorithm development, problem solving and optimizing techniques

**PSO 14** Apply software development and project management methodologies using concepts of front-end and back-end development and emerging technologies and platforms.

**PSO 15** Ability to understand and apply Cloud Computing architecture for scalable, secure and dynamically provisioned business oriented environment with optimized performance tuning and data reliability.

1. **COURSE OUTCOMES FOR COMPUTER SYSTEM ARCHITECTURE: At the end of this course student should be able to**

CO1: Identify Functional Units, Bus Structure and Addressing Modes.

CO2: Design the Digital Components including – Decoder, Multiplexer and Arithmetic Circuits.

CO3: Learn the Design of Arithmetic Unit, Logic Unit and Control Unit.

CO4: Understand the Design of Hardwired & Microprogrammed Control Unit.

CO5: Identify the Memory Hierarchy mapping and its Performance, and Understanding the Interface of ALU with I/O devices.

**Table: Correlation of POs and PSOs v/s COs**

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| PO/CO | PO  1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO  9 | PO  10 | PO  11 | PO  12 | PSO  1 | PSO  2 | PSO  3 |
| CO1 | 2 | 2 | 2 |  | 3 | 3 |  |  | 2 |  |  | 1 |  | 1 |  |
| CO2 | 2 | 3 | 1 |  | 2 | 3 |  |  | 2 |  |  | 2 |  | 1 |  |
| CO3 | 2 | 2 | 3 |  | 2 | 3 |  |  | 2 |  |  | 2 |  | 1 |  |
| CO4 | 3 | 3 | 2 |  | 3 | 3 |  |  | 2 |  |  | 1 |  | 1 |  |
| CO5 | 2 | 2 | 2 |  | 2 | 3 |  |  | 2 |  |  | 3 |  | 1 |  |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | Engineering Knowledge | Problem analysis | Design/development of solutions | Conduct investigations of complex problems | Modern tool usage | The engineer and society | Environment and sustainability | Ethics | Individual or team work | Communication | Project management and finance | Life-long Learning | Perform system and application programming using computer system concepts, concepts of Data Structures, algorithm development, problem solving and optimizing techniques | Apply software development and project management methodologies using concepts of front-end and back-end development and emerging technologies and platforms. | Ability to understand and apply Cloud Computing architecture for scalable, secure and dynamically provisioned business oriented environment with optimized performance tuning and data reliability. | |
| Course Code | Course Title | PO1 | PO2 | PO3 | PO 4 | PO 5 | PO6 | PO 7 | PO8 | PO9 | PO 10 | PO 11 | PO12 | PSO13 | PSO14 | | PSO15 |
|  | CSA | 2 | 2 | 2 |  | 2 | 3 | 1 |  | 2 |  |  | 2 |  | **1** | |  |

1=weakly mapped

2= moderately mapped

3=strongly mapped

1. **COURSE OUTLINE**

* Introduction
* ALU Design
* Control Unit Design
* Memory Unit Organization
* Input Output Organization

1. **PEDAGOGY**

* Presentation
* flipped classroom session
* think-pair and share
* YouTube videos as a startup

1. **COURSE COMPLETION PLAN**

|  |  |
| --- | --- |
| **Total Class room sessions** | 24(Offline) &12(Online) |
| **Total Quizzes** | 02 |
| **Total Test** | 01 |
| **Total Assignment** | 02 |

One Session =60 minutes

1. **EVALUATION & GRADING**

Students will be evaluated based on the following 3 stages.

* 1. Internal Assessment - 30%

5.2 Mid-term Examination - 20%

* 1. End term Examination - 50%

**G1. INTERNAL ASSESSMENT: WEIGHTAGE – 30%**

Internal Assessment shall be done based on the following:

|  |  |  |
| --- | --- | --- |
| S. No. | Description | % of Weightage out of 30% |
| 1 | Test(1) + Quizzes (2) | 50% |
| 2 | Assignments (2) | 40% |
| 3 | Attendance | 10% |

**G2*. Internal Assessment Record Sheet (including Mid Term Examination marks)*** *will be displayed online at the end of semester i.e. last week of regular classroom teaching.*

**G3. CLASS TESTS/QUIZZES:** One Class Test based on descriptive type theoretical & numerical questions and Two Quizzes based on objective type questions will be held; one quiz one test at least ten days before the Mid Term Examination and and second quiz at least ten days before the End Term Examination. Those who do not appear in quiz examinations shall lose their marks.

*The marks obtained by the students will be displayed on LMS a week before the start of Mid Term and End Term Examinations respectively.*

**G4. ASSIGNMENTS:** Two assignments based on theory and numerical problems; one before mid-term and one before end term examination would be taken. Those who fail to submit the assignments by the due date shall lose their marks.

**G5. GENERAL DISCIPLINE:** Based on student’s regularity, punctuality, sincerity and participation in the interactions.

*The marks obtained by the students will be displayed on LMS at the end of semester.*

**G6. MID TERM EXAMINATION: WEIGHTAGE – 20%**

Mid Term examination shall be of Two Hours duration and will consist of 50 Objective type questions and would be conducted through blackboard.

**G7. END TERM EXAMINATION: WEIGHTAGE – 50%**

End Term Examination shall be Three Hours duration and shall be a combination of Short and Long theory/numerical Questions.

**G8. GRADING:**

The overall marks obtained at the end of the semester comprising all the above three mentioned shall be converted to a grade.

1. **COURSE DELIVERY PLAN (online sessions are highlighted in yellow)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Module / Session** | **Big Ideas / Topics** | **Course Outcomes Addressed** | **Required Learning Resources**  **(including media)** | **Pedagogy / Discussion(s) / Postings** | **Assignment(s)** |
| **Unit-1**  **Introduction (11 Hours)** | **Evolution of Computer Systems,** Von Neumann Architecture**,** Moore’s Law, Computer Types, Functional Units, **Devices (Input, Output, Storage & Communication Devices),** **Memory System (RAM, ROM, Cache, VM, etc.),** Introduction to Logic Gates, Truth Table, K-Map, Latch Flip Flops (J, K & D), Encoder & Decoder, MUX & DEMUX, **Registers & Counters,** Binary Number system, Overview of RISC/CISC, **RISC vs. CISC.** | CO1, CO2 | T1, R1, R2, R3, OL2, OL3, OL4 | **Lecture, Discussion and**  **Blackboard** | **As per the schedule mentioned below** |
| **L1** | Introduction to blended Course for CSA, Importance of CSA |  | PPT | **Discussion** |  |
| **L2** | Von Neumann Architecture, Functional units, Moore’s Law, Computer Types, Binary Number System |  | T1 [67 - 85], R2 [22 - 69] | **Lecture and Discussion** |  |
| **L3** | **Evolution of Computer System, Devices( Input, Output, Storage & Communication Devices)** |  | **Resources on blackboard** | **Online via blackboard** |  |
| **L4** | Binary Number System with numerical |  | T1 [67 - 85], R2 [22 - 69] | **Lecture and Discussion** |  |
| **L5** | Introduction to Logic Gates, Truth Table. |  | T1 [1 - 12], R2 [108 - 138] | **Lecture and Discussion** |  |
| **L6** | **Memory System (RAM, ROM, Cache, VM, etc.) Overview of RISC/CISC, RISC vs. CISC** |  | **Resources on blackboard** | **Online via blackboard** |  |
| **L7** | K-Map and its numerical |  | T1 [447 - 471, 284 - 286]  T1 [12 - 18], R2 [196 - 212] | **Lecture and Discussion** |  |
| **L8** | Adder & Subtractor, Latch |  | T1 [20 - 22], R2 [282 - 289] | **Lecture and Discussion** |  |
| **L9** | **Registers & Counters** |  | **Resources on blackboard**  **T1 [41 - 47, 47 - 48, 50 - 58], R2 [511 - 526, 527 - 541]** | **Online via blackboard** |  |
| **L10** | Flip-Flops (RS, J, K, D) |  | T1 [24 - 28], R2 [459 - 479] | **Lecture and Discussion** |  |
| **L11** | DEMUX, MUX, Encoder & Decoder | T1 [47 - 49, 43 - 49], R2 [345 -356, 330 - 343 ] | **Lecture and Discussion** |  |
|  | Doubt Clearance Session/Pending Topics |  |  |  |  |
| **Unit II**  **ALU Design**  **(8 Hours)** | Computer Organization and Design, Instruction Codes, Op-Code, Computer registers, Computer Instructions, CPU stack Organization, Instruction Formats, **Instruction types**, Timing and control, Instruction and Instruction sequencing, Instruction Cycle, Memory Reference Instructions, **Addressing modes,** Program Control, **Types of Interrupts**, Design computer ,performance and metrics, **Introduction to Parallelism,** **Flynn’s classification of computers, Feng’s classification,** **Parallel architecture**, Pipeline Hazards Condition for Stalls Requirements | CO1, CO3 | T1, R1, OL5, OL6, OL7 | **Lecture, Discussion and**  **Blackboard** | **As per the schedule mentioned below** |
| **L12** | Computer Organization and Design, Instruction Codes, Op-Code, Computer Registers. |  | T1[125 - 131] | **Lecture and Discussion** |  |
| **L13** | Computer Instructions, CPU stack organization. |  | T1[134 - 136, 249 - 255] | **Lecture and Discussion** |  |
| **L14** | **Instruction types**, **Addressing mode**, **Interrupts**, **Types of Interrupts**, **Priority Interrupts**, **Daisy chaining Priority.** |  | **Resources on blackboard** | **Online via blackboard** |  |
| **L15** | Instruction formats, Timing and control, Instruction Sequencing & Instruction Cycles, Memory Reference Instructions, Program Control, Design computer, performance and metrics. |  | T1[257 - 261, 137,141 – 145, 147- 151, 275 - 280] | **Lecture and Discussion** |  |
| **L16** | CLASS TEST-1 (Offline) |  |  |  |  |
| **L17** | Introduction to Pipelining (arithmetic & instruction pipeline), Basic performance issues in pipelining, Limitations on practical depth of a pipeline. |  | T1[301 - 312] | **Lecture and Discussion** |  |
| **L18** | **Introduction to parallelism, Flynn’s classification of computers**, **Feng’s Classification**, **Parallel architecture.** |  | **Resources on blackboard** | **Online via blackboard** |  |
| **L19** | Pipeline Hazards, Conditions for Stall. |  | T1 [301 - 312] | **Lecture and Discussion** |  |
|  | Doubt Clearance Session/Pending Topics |  |  |  |  |
| **Unit III**  **Control Unit Design**  **(8 Hours)** | Introduction, Instruction Interpretation & Execution, Control Transfer, **Fetch Cycle**, Micro programmed Control, Control Memory, **Micro programmed vs. Hardwired Control Unit,** Nano Programming, Superscalar processing. | CO1, CO4 | T1, R1, OL1 | **Lecture, Discussion and**  **Blackboard** | **As per the schedule mentioned below** |
| **L20** | Introduction, Instruction Interpretation & Execution |  | R1 [577 - 583] | **Lecture and Discussion** |  |
| **L21** | Control Transfer |  | R1 [538 - 587] | **Lecture and Discussion** |  |
| **L22** | **Fetch Cycle** |  | **R1 [578 - 580]** | **Online via blackboard** |  |
| **L23** | Micro programmed Control |  | R1 [603 - 605] | **Lecture and Discussion** |  |
| **L24** | Control Memory |  | OL1 | **Lecture and Discussion** |  |
| **L25** | **Micro programmed vs. Hardwired Control Unit** |  | **Resources on Blackboard** | **Online via blackboard** |  |
| **L26** | Nano Programming |  | T1[328 – 330] | **Lecture and Discussion** |  |
| **L27** | Superscalar Programming |  | Resources on blackboard | **Online via blackboard** |  |
|  | Doubt Clearance Session/Pending Topics |  |  |  |  |
| **Unit IV**  **Memory Unit Organization**  **(4 Hours)** | **Memory Locations & Addresses,** **Semiconductor Memory**, Static and Dynamic Memory, Main Memory, **Auxiliary Memory,** Associative Memory, Cache Memory, **Secondary Memories: Optical Magnetic Tape, Magnetic Disk and Controllers** | CO1, CO5 | T1 | **Lecture, Discussion and**  **Blackboard** | **As per the schedule mentioned below** |
| **L28** | **Memory Locations**  **& Addresses, Semiconductor Memory.** |  | **Resources on blackboard**  **T1[452 – 454, 447 - 449]** | **Online via blackboard** |  |
| **L29** | Static and Dynamic Memory, Main Memory. |  | T1[447 - 451] | **Lecture and Discussion** |  |
| **L30** | Associative Memory, Cache Memory |  | T1[458 – 464, 464 - 471] | **Lecture and Discussion** |  |
| **L31** | **Auxiliary Memory, Secondary Memory: Optical Magnetic Tape, Magnetic Disk and Controllers** |  | **Resources on blackboard**  **T1[454 - 458]** | **Online via blackboard** |  |
|  | Doubt Clearance Session/Pending Topics |  |  |  |  |
| **Unit V**  **I/O**  **Organization**  **(5 Hours)** | I/O and their brief description, Bus Interface, **Bus arbitration,** **Data Transfer**, Types of Interrupts, I/O Interrupts, Channels, Direct Memory Access, I/O processing | CO1, CO6 | T1 | **Lecture, Discussion and**  **Blackboard** | **As per the schedule mentioned below** |
| **L32** | I/O and their brief description, Bus Interface |  | T1[383 - 392] | **Lecture and Discussion** |  |
| **L33** | **Data Transfer Techniques** |  | **Resources on blackboard**  **T1[393 – 416]** | **Online via blackboard** |  |
| **L34** | Types of I/O Interrupts, Channels |  | T1[404 – 416, 422 - 429] | **Lecture and Discussion** |  |
| **L35** | **Bus arbitration** |  | **Resources on blackboard**  **T1[383 – 390]** | **Online via blackboard** |  |
| **L36** | Direct Memory Access, I/O processing |  | T1[417-421, 422 - 430] | **Lecture and Discussion** |  |
|  | Doubt Clearance Session/Pending Topics |  |  |  |  |

1. **SUGGESTED READINGS:**

**H1. TEXT BOOK:**

1. “Computer System Architecture”, 3rd edition, M. Morris Mano, Pearson Publications.

**H2. REFERRENCE BOOKS:**

1. “Computer Organization and Architecture”, Sixth Edition, William Stallings, Pearson Publications.

2. “Fundamental of Digital electronics", second edition, A. Anand Kumar, PHI publications

3. “Computer Organization and Architecture”, Third Edition, John P. Hayes, TATA McGraw HILL

**H3. OTHER RESOURCES**

**H4. VIDEO RESOURCES:**

1. NPTEL Lectures VIDEO
2. **RESOURCES: - PPT & VIDEO - Black Board**

**H5. WEB RESOURCES:**

1. **http://www.laureateiit.com/projects/bacii2014/projects/coa\_anil/control\_memory.html**
2. **http://www.ni.com/example/14493/en/**
3. **https://www.youtube.com/watch?v=2ecMG\_OciLo**
4. **https://www.youtube.com/watch?v=Sf\_Yx2z1fRk**
5. **http://www.cs.uwm.edu/classes/cs458/Lecture/HTML/ch05.html**
6. **https://www.youtube.com/watch?v=CDO28Esqmcg**
7. **http://nptel.ac.in/courses/106106092/12#**
8. **GUIDELINES**

***Cell Phones and other Electronic Communication Devices*:** Cell phones and other electronic communication devices (such as Blackberries/Laptops) are not permitted in classes during Tests or the Mid/Final Examination. Such devices MUST be turned off in the class room.

***E-Mail and online learning tool:*** Each student in the class should have an e-mail id and a pass word to access the LMS system regularly. Regularly, important information – Date of conducting class tests, guest lectures, via online learning tool. The best way to arrange meetings with us or ask specific questions is by email and prior appointment. All the assignments preferably should be uploaded on online learning tool. Various research papers/reference material will be mailed/uploaded on online learning platform time to time.

***Attendance:*** Students are required to have **minimum attendance of 75%** in each subject. Students with less than said percentage shall **NOT** be allowed to appear in the end semester examination.

***Passing criterion:*** Student has to secure minimum 30%/40% marks of the “highest marks in the class scored by a student in that subject (in that class/group class)” individually in both the ‘End-Semester examination’ and ‘Total Marks’ in order to pass in that paper.

* Passing Criterion for B. Tech: Minimum 30% and 40% of the highest marks in the class applicable to the students admitted before July 2015 and onwards July 2015 respectively.
* Passing Criterion for M. Tech: minimum 40% of the highest marks in the class

1. **Course outcome assessment**

To assess the fulfilment of course outcomes two different approaches have been decided. Degree of fulfillment of course outcomes will be assessed in different ways through direct assessment and indirect assessment. In Direct Assessment, it is measured through quizzes, tests, assignment, Mid-term and/or End-term examinations. It is suggested that each examination is designed in such a way that it can address one or two outcomes (depending upon the course completion). Indirect assessment is done through the student survey which needs to be designed by the faculty (sample format is given below) and it shall be conducted towards the end of course completion. The evaluation of the achievement of the Course Outcomes shall be done by analyzing the inputs received through Direct and Indirect Assessments and then corrective actions suggested for further improvement.

**Sample format for Indirect Assessment of Course outcomes**

|  |
| --- |
| NAME: |
| ENROLLMENT NO: |
| SAP ID: |
| COURSE: Computer System Architecture. |
| PROGRAM: B.Tech CS CCVT |

Please rate the following aspects of course outcomes of Computer System Architecture.

Use the scale 1-4\*

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Sl. No. |  | 1 | 2 | 3 | 4 |
| 1 | CO1. Identify Functional Units, Bus Structure and Addressing Modes. |  |  |  |  |
| 2 | CO2: Design Digital Components including – Decoder, Multiplexer and Arithmetic Circuits and Design Arithmetic and Control Unit. |  |  |  |  |
| 3 | CO3: Learn the Design of Arithmetic Unit, Logic Unit and Control Unit. |  |  |  |  |
| 4 | CO4: Understand the Design of Hardwired & Microprogrammed Control Unit. |  |  |  |  |
| 5 | CO5: Identify the Memory Hierarchy and its Performance. |  |  |  |  |
| 6 | CO5: Identify the Memory Hierarchy mapping and its Performance, and Understanding the Interface of ALU with I/O devices. |  |  |  |  |

3

Below Average

Good

1

**\***

Very Good

Average

4

2