|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1. | | Answer :       (c)  Reason : The AND, and OR functions are only two of a total of 16 possible functions formed with two binary variables. Therefore, for two variables n=2, and the number of possible Boolean functions is 16. | | |
| 2. | | Answer :       (a)  Reason : This means that it is not practical for use in systems requiring high-speed operations. The characteristic parameters for the CMOS gate depend on the power supply voltage VDD that is used. The power dissipation increases with increase in voltage supply. The propagation delay decreases with increase in voltage supply and the noise margin is estimated to be about 40% of the voltage supply value. | | |
| 3. | | Answer :       (a)  Reason : Consider the 20-bit logical address. The 4-bit segment number specifies one of 16 possible segments. The 8-bit page number can specify up to 256 pages, and the 8-bit word field implies a page size of 256 words. This configuration allows each segment to have any number of pages up to 256. the smallest possible segment will have one page of 256 words. The largest possible segment will have 256 pages, for a total of 256\*256 = 65,536 which means 64K words. | | |
| 4. | | Answer :       (b)  Reason : Associative memories are expensive compared to random-access memories because of the added logic associated with each cell. Therefore, the simplest way to determine cache locations in which to store memory blocks is the Direct Mapping. | | |
| 5. | | Answer :       (d)  Reason : 2’s complement of -6  =  11111010  2’s complement of -13 = 11110011  Add the two numbers in their 2’s complement form, including their sign bits and discard any carry out of the sign (leftmost) bit position. So the answer is 11101101 (-19).  -6    11111010  -13  11110011  ----------------------  -19  11101101 | | |
| 6. | | Answer :       (e)  Reason : Program Counter (PC) keeps track of the instruction of the program stored in memory. | | |
| 7. | | Answer :       (a)  Reason :   The major components of CPU are Control Unit, Register Set, and Arithmetic Logic Unit. | | |
| 8. | | Answer :       (d)  Reason :   The next state is a complement state. | | |
| 9. | | Answer :       (e)  Reason : When R = 1 and S = 1, race will always end with Master Latch in the logic 1 state, but this will not be certain with real components. | | |
| 10. | | Answer :       (c)  Reason : Toggle flip-flop as it changes its output on each clock edge. | | |
| 11. | | Answer :       (b)  Reason : To SR flip-flop two new connections from Q and Q’ outputs back to original input gates eliminate the indeterminate condition. | | |
| 12. | | Answer :       (c)  Reason : The operation part of an instruction code specifies the operation to be performed. This operation must be executed on some data stored in memory and/or processor registers. An instruction code, therefore, must specify not only the operation, but also the register or memory words where the operands are to be found, as well as the register or memory words where the result is to be stored. For this reason, the bulk of binary information in a digital computer is stored in memory, but all computations are done in Processor Registers. | | |
| 13. | | Answer :       (d)  Reason : A replacement operator consisting of the information transfer from one register to another, is designated in symbolic form. | | |
| 14. | | Answer :       (a)  Reason : Registers found in processor are called operational registers and in memory unit are called storage registers. | | |
| 15. | | Answer :       (c)  Reason : A virtual memory system provides a mechanism for translating program-generated addresses into correct main memory locations. This is done dynamically, while programs are being executed in the CPU. The translation or mapping is handled automatically by the hardware by means of a mapping table. | | |
| 16. | | Answer :       (a)  Reason : Excess-3code generation takes 3 as excess to the binary code. | | |
| 17. | | Answer :       (a)  Reason : The Bus master is allowed to initiate data transfer on the bus. | | |
| 18. | | Answer :       (c)  Reason : Debugger is a program, which finds errors in program. | | |
| 19. | | Answer :       (a)  Reason : Multiplexer is called as Data Selector in computers where Dynamic memory uses the same address lines for both row and column addressing and a set of multiplexers is used to first select row address and then switch to column address. | | |
| 20. | | Answer :       (b)  Reason : A full-adder is simply a connection of two half-adders joined by a OR gate, and other half-adder simplify the AND gate also. | | |
| 21. | | Answer :       (a)  Reason : Decoder uses address inputs as binary numbers and produces an output signal. | | |
| 22. | | Answer :       (a)  Reason : The correspondence between the main memory blocks and those in the cache is specified by a mapping function, because the basic characteristic of cache memory is fast access time. Therefore, very little or no time must be wasted when searching for words in the cache. | | |
| 23. | | Answer :       (c)  Reason : A technique called cycle stealing allows the DMA controller to transfer one data word at a time, after which it must return control of buses to the CPU. | | |
| 24. | | Answer :       (c)  Reason : The control condition is terminated with a colon. | | |
| 25. | | Answer :       (c)  Reason :   When x = 0, y = 0 the corresponding carry and sum are 0,0. | | |
| 26. | | Answer :       (b)  Reason : Logical gates are building blocks of combinational circuits whereas, flipflops are combination of logic gates, registers are memory storages. | | |
| 27. | | Answer :       (d)  Reason :   Absorption law :- x + xy = x = x (1+y)  = x . 1  = x. | | |
| 28. | | Answer :       (a)  Reason : The binary number 011 111 000 represents the octal digits 3, 7, 0 from left to right distrubution by three bits. | | |
| 29. | | Answer :       (b)  Reason : Boolean functions expressed as a sum (ORing of terms) of minterms or maxterms (ANDing of terms) are said to be in canonical form. | | |
| 30. | | Answer :       (d)  Reason : All the options are used to handle data transfer to and from peripherals. | | |
| 31. | | Answer :   (c)  Reason:    The gray code of 1001 is 1101 | | |
| 32. | | Answer :   (d)  Reason:    Unsigned binary representation occupies less space to store the number +255. | | |
| 33. | | Answer :   (c)  Reason:    The AND, and OR functions are only two of a total of 16 possible functions formed with two binary variables. Therefore, for two variables n=2, and the number of possible Boolean functions is 16. | | |
| 34. | | Answer :   (b)  Reason:    This means that it is not practical for use in systems requiring high-speed operations. The characteristic parameters for the CMOS gate depend on the power supply voltage VDD that is used. The power dissipation increases with increase in voltage supply. The propagation delay decreases with increase in voltage supply and the noise margin is estimated to be about 40% of the voltage supply value. | | |
| 35. | | Answer :   (a)  Reason:    Consider the 20-bit logical address. The 4-bit segment number specifies one of 16 possible segments. The 8-bit page number can specify up to 256 pages, and the 8-bit word field implies a page size of 256 words. This configuration allows each segment to have any number of pages up to 256. the smallest possible segment will have one page of 256 words. The largest possible segment will have 256 pages, for a total of 256\*256 = 65,536 which means 64K words. | | |
| 36. | | Answer :   (b)  Reason:    Associative memories are expensive compared to random-access memories because of the added logic associated with each cell. Therefore, the simplest way to determine cache locations in which to store memory blocks is the Direct Mapping. | | |
| 37. | | Answer :   (d)  Reason:    2’s complement of -6  =  11111010  2’s complement of -13 = 11110011  Add the two numbers in their 2’s complement form, including their sign bits and discard any carry out of the sign (leftmost) bit position. So the answer is 11101101 (-19).  -6      11111010  -13   11110011  ------------------  -19   11101101 | | |
| 38. | | Answer :   (e)  Reason:    Program Counter (PC) keeps track of the instruction of the program stored in memory. | | |
| 39. | | Answer :   (a)  Reason:    The major components of CPU are Control Unit, Register Set, and Arithmetic Logic Unit. | | |
| 40. | | Answer :   (d)  Reason: | | |
| 41. | | Answer :   (e)  Reason:    When R = 1 and S = 1, race will always end with Master Latch in the logic 1 state, but this will not be certain with real components. | | |
| 42. | | Answer :   (c)  Reason:    Toggle flip-flop as it changes its output on each clock edge. | | |
| 43. | | Answer :   (b)  Reason:    To SR flip-flop two new connections from Q and Q’ outputs back to original input gates eliminate the indeterminate condition. | | |
| 44. | | Answer :   (c)  Reason:    The operation part of an instruction code specifies the operation to be performed. This operation must be executed on some data stored in memory and/or processor registers. An instruction code, therefore, must specify not only the operation, but also the register or memory words where the operands are to be found, as well as the register or memory words where the result is to be stored. For this reason, the bulk of binary information in a digital computer is stored in memory, but all computations are done in Processor Registers. | | |
| 45. | | Answer :   (d)  Reason:    A replacement operator consisting of the information transfer from one register to another, is designated in symbolic form. | | |
| 46. | | Answer :   (a)  Reason:    Registers found in processor are called operational registers and in memory unit are called storage registers. | | |
| 47. | | Answer :   (c)  Reason:    A virtual memory system provides a mechanism for translating program-generated addresses into correct main memory locations. This is done dynamically, while programs are being executed in the CPU. The translation or mapping is handled automatically by the hardware by means of a mapping table | | |
| 48. | | Answer :   (b)  Reason:    The octal number and their binary coded equivalent BCD is a straight assignment of binary equivalent. It is possible to assign weights to the binary bits according to their position as per conversion of octal number to binary number. | | |
| 49. | | Answer :   (a)  Reason:    The processor, cache memory and I/O devices are interconnected by means of a common bus. | | |
| 50. | | Answer :   (c)  Reason:    Debugger is a program, which finds errors in program. | | |
| 51. | | Answer :   (a)  Reason:    Decoder. | | |
| 52. | | Answer :   (b)  Reason:    A full-adder is simply a connection of two half-adders joined by a OR gate, and other half-adder simplify the AND gate also. | | |
| 53. | | Answer :   (e)  Reason:    The corresponding  between the main memory blocks and those in the cache is specified by a mapping function, because the basic characteristic of cache memory is fast access time. Therefore, very little or no time must be wasted when searching for words in the cache. | | |
| 54. | | Answer :   (d)  Reason:    16 RAM chips of size 256\*4 are needed to construct a CACHE of size 2KB | | |
| 55. | | Answer :   (b)  Reason:    The collection of address spaces in a physical memory is called address space. | | |
| 56. | | Answer :   (a)  Reason:    The Bus master is allowed to initiate data transfer on the bus. | | |
| 57. | | Answer :   (a)  Reason:    Transfer of one word data at a time using DMA transfer technique is called Cycle Stealing. | | |
| 58. | | Answer :   (b)  Reason:    Serial interface transfers one bit at a time, whereas others can handle more than one bit. | | |
| 59. | | Answer :   (b)  Reason:    In a  based Logical gates are building blocks of combinational circuits whereas, flipflops are combination of logic gates, registers are memory storages. | | |
| 60. | | Answer :   (b)  Reason:    Entering new information into a register is called loading. | | |
| 61. | | Answer :   (b)  Reason  :  Divide the given number 888 by 5 and write all the remainder terms from the bottom to up and finally we will get (12023) to the base 5 | | |
| 62. | | Answer :   (a)  Reason  :  C’ + A | | |
| 63. | | Answer :   (d)  Reason  :  3CD | | |
| 64. | | Answer :   (b)  Reason  :  8086 is a 16 bit processor. | | |
| 65. | | Answer :   (a)  Reason  :  The data inside a computer is represented in Binary form i.e (0’s and 1’s). | | |
| 66. | | Answer :   (b)  Reason  :  A parity bit is used to detect errors. | | |
| 67. | | Answer :   (b)  Reason  :  The minimum number of bits required to store a Hexadecimal number FF is 4. | | |
| 68. | | Answer :   (d)  Reason  :  Makes some arithmetic calculations faster. | | |
| 69. | | Answer :   (b)  Reason  :  Motorola 8086 is not a processor. | | |
| 70. | | Answer :   (b)  Reason  :  Cycle Stealing concept is used in DMA . | | |
| 71. | | Answer :   (a)  Reason  :  optical storage has faster access time than disk storage. | | |
| 72. | | Answer :   (c)  Reason  :  It increases the disk storage capacity and availability. | | |
| 73. | | Answer :   (c)  Reason  :  It is used for accessing stack. | | |
| 74. | | Answer :   (a)  Reason  :  Combinational circuits has memory. | | |
| 75. | | Answer :   (e)  Reason  :  Data Bus is not involved in memory write operation. | | |
| 76. | | Answer :   (b)  Reason  :  Arithmetic-logic unit is responsible for coordinating various operations using timing signals | | |
| 77. | | Answer :   (c)  Reason  :  pages out pages that have been least used recently | | |
| 78. | | Answer :   (b)  Reason  :  ROM is a non-volatile memory. | | |
| 79. | | Answer :   (b)  Reason  :  Cache memory enhances memory access time. | | |
| 80. | | Answer :   (c)  Reason  :  When all of its inputs are low and high. | | |
| 81. | | Answer :   (c)  Reason  :  A machine cycle refers to Fetching, decoding and executing  an instruction. | | |
| 82. | | Answer :   (d)  Reason  :  System bus consists of a Control bus, Data bus and a Address bus. | | |
| 83. | | Answer :   (b)  Reason  :  The bootable code is stored in ROM. | | |
| 84. | | Answer :   (e)  Reason  :  Access time. | | |
| 85. | | Answer :   (d)  Reason  :  System bus is not a part of a cpu . | | |
| 86. | | Answer :   (e)  Reason  :  Memory mapped I/O involves transferring information between I/O devices and CPU . | | |
| 87. | | Answer :   (d)  Reason  :  EEPROM is the type of memory whose contents is erased with the passage of electiricity. | | |
| 88. | | Answer :   (c)  Reason  :  CPU performance is measured in MHz | | |
| 89. | | Answer :   (c)  Reason  :  The read / write line belongs to the address bus.a | | |
| 90. | | Answer :   (a)  Reason  :  Busy waiting is to allow the CPU wait for a busy device. | | |
| 91. | | Answer :       (c)  Reason:  Addressing mode that specifies a register which contains the memory address of the operand is  Register Indirect Addressing Mode. | | |
| 92. | | Answer :       (c)  Reason:  Address space indicate a set of Logical Addresses. | | |
| 93. | | Answer :       (c)  Reason:  Stack does not Implement FIFO but implements LIFO. | | |
| 94. | | Answer :       (e)  Reason:  Handshaking is the method in which the unit receiving the data responds with another control signal. | | |
| 95. | | Answer :       (c)  Reason:  The page replacement algorithm in which there is a replacement of a page, which will not be used for the longest period of time is OPT. | | |
| 96. | | Answer :       (e)  Reason:  The input device for which finger shows the cursor movement is Glide pad. | | |
| 97. | | Answer :       (b)  Reason:  6543- 4444= 2099 | | |
| 98. | | Answer :       (b)  Reason:  The octal equivalent of  011001 =31. | | |
| 99. | | Answer :       (b)  Reason:  SPA stands for Skip If (Accumulator) Positive | | |
| 100. | | Answer :       (c)  Reason:  Combinational circuit is an interconnection of logic gates. | | |
| 101. | | Answer :       (d)  Reason:  ROM is  the memory usually written by the manufacturer. | | |
| 102. | | Answer :       (e)  Reason:  D stands in D-flip flop stands for Data. | | |
| 103. | | Answer :       (b)  Reason:  The program is executed from main memory until it attempts to reference a page that is still in auxiliary memory called Page Fault. | | |
| 104. | | Answer :       (c)  Reason:  DMA stands for Direct Memory Access. | | |
| 105. | | Answer :       (b)  Reason:  The symbol to represent a state in the state diagram is | | |
| 106. | | Answer :       (d)  Reason:  DR ← M [AR] is Memory Read. | | |
| 107. | | Answer :       (d)  Reason:  A computer has memory of 256k words of 32 bits each, 18 bits  are required to specify the address part. | | |
| 108. | | Answer :       (c)  Reason:  Speakers can be called as a peripheral. | | |
| 109. | | Answer :       (c)  Reason:  is a symbol for AND. | | |
| 110. | | Answer :       (c)  Reason:  Selective Set is the operation sets to 1 the bits in one register where there are corresponding 1’s in the second register. | | |
| 111. | | Answer :       (a)  Reason:  D7I'T  in the instruction cycle represents Register –reference instructions. | | |
| 112. | | Answer :       (d)  Reason:  (r-1)’s complement of 345 in octal number system is 432. | | |
| 113. | | Answer :       (e)  Reason:  SHRA  stands for Arithmetic shift right. | | |
| 114. | | Answer :       (d)  Reason:  Temporal Locality describe that the information which will be used in near future is likely to be in use already. | | |
| 115. | | Answer :       (c)  Reason:  CISC stands for Complex Instruction Set Computer. | | |
| 116. | | Answer :       (e)  Reason:  The three state gates in a digital circuit Logic 0, logic 1, high impedance | | |
| 117. | | Answer :       (d)  Reason:  The table that lists the required inputs for a given change of state is Excitation Table. | | |
| 118. | | Answer :       (c)  Reason:  Microphone is a Input device. | | |
| 119. | | Answer :       (b)  Reason:  Execution is the phase in which the programs must reside in the main memory. | | |
| 120. | | Answer :       (d)  Reason:  (x')' = x. | | |
|  | | **Answer** | **Reason** | |
| **121.** | | d | Is the input device for which finger shows the cursor movement | |
| **122.** | | a | SPA stands for Skip If (Accumulator) Positive | |
| **123.** | | b | ROM is the memory usually written by the manufacturer. | |
| **124.** | | B | The program is executed from main memory until it attempts to reference a page that is still in auxiliary memory called Page Fault. | |
| **125.** | | B | is the symbol which represent a state in the state diagram | |
| **126.** | | A | A computer has memory of 256k words of 32 bits each, 18 bits are required to specify the address part. | |
| **127.** | | A | **V**  is a symbol for **OR** | |
| **128.** | | B | D7I’T  in the instruction cycle represents Register –reference instructions | |
| **129.** | | D | SHRA stands for Arithmetic shift right | |
| **130.** | | B | CISC stands for complex instruction set computer. | |
| **131.** | | C | Is the phase in which the programs must reside in the main memory. | |
| **132.** | | E | Is the three state gates in a digital circuit | |
| **133.** | | C | Stack does not Implement FIFO but implements LIFO | |
| **134.** | | E | Hand shaking is the method in which the unit receiving the data responds with another control signal | |
| **135.** | | B | 6543- 4444= 2099 | |
| **136.** | | D | (x’)’ = x | |
| **137.** | | C | Register indirect addressing mode. Is the addressing mode that specifies a register which contains the memory address of the operand | |
| **138.** | | B | The octal equivalent of 011001 =31 | |
| **139.** | | C | Combinational circuit is an interconnection of logic gates. | |
| **140.** | | E | D stands in D-flip flop stands for Data | |

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| --- | --- | --- | --- | --- | --- |
| **141.** | | C | | Address spaces  Indicate a set of Logical Addresses. | |
| **142.** | | C | | DMA stands for Direct Memory Access | |
| **143.** | | D | | DR ← M [AR] is Memory Read | |
| **144.** | | E | | (r-1)’s complement of 345 in octal number system is 432 | |
| **145.** | | D | | Temporal Locality describe that the information which will be used in near future is likely to be in use already. | |
| **146.** | | D | | Excitation table is the table that lists the required inputs for a given change of state | |
| **147.** | | C | | Microphone is a Input device | |
| **148.** | | C | | Selective Set is the operation sets to 1 the bits in one register where there are corresponding 1’s in the second register | |
| **149.** | | B | | Speakers can be called as a peripheral. | |
| **150.** | | b | | Bar code reader. | |
| **151.** | | Answer :   (a)  Reason  :  10100 is the binary number which is equivalent to 20. | |
| **152.** | | Answer :   (d)  Reason  :  The Hexadecimal number system has a radix of 16. | |
| **153.** | | Answer :   (c)  Reason  :  The equivalent of -3510 in 8-bit 2’s complement representation is 11011101. | |
| **154.** | | Answer :   (a)  Reason  :  The BCD equivalent of decimal number 32.94 is  0011 0010 .1001 0100. | |
| **155.** | | Answer :   (d)  Reason  :  The code which can represent numbers, characters, and special characters are called Alphanumeric code. | |
| **156.** | | Answer :   (c)  Reason  :  In a Hamming code for transmitting a data of 4-bit, three parity bits are used. | |
| **157.** | | Answer :   (b)  Reason  :  The Boolean expression F = AB’C’D + AB’CD’ + A’BCD can be written as F = ∑m (7, 9, 10). | |
| **158.** | | Answer :   (a)  Reason  :  The Boolean expression F(A,B,C,D) =∑m(0, 3) is  (A + B + C’ + D’) (A + B + C + D) | |
| **159.** | | Answer :   (a)  Reason  :  In a Karnaugh map the adjacent minterms can be combined only if the configuration of 2. | |
| **160.** | | Answer :   (c)  Reason  :  For realizing the Boolean expression AC + AD + BC + BD the  number of inputs needed are 12. | |
| **161.** | | Answer :   (c)  Reason  :  Using Karnaugh map SOP form of the expression  (B + C + D) (B’ + C + D’) (A’ + B + C’ + D’) (A + B’ + E’) (A + B’ + D’) will be B’C’D + A’B’C + ABC + BD’E’ + ACD’ + ABD’. | |
| **162.** | | Answer :   (a)  Reason  :  The number of input variables which a NOT gate can have is One. | |
| **163.** | | Answer :   (b)  Reason  :  The unique output for a NAND logic gate is a 0 when all the inputs are 1. | |
| **164.** | | Answer :   (e)  Reason  :  States of bus may be  Logic 0,logic 1 and high impedence | |
| **165.** | | Answer :   (c)  Reason  :  The binary pattern   101110   is an answer received after adding two numbers in a 6-bit two’s complement system. The answer in decimal system is – 18. | |
| **166.** | | Answer :   (a)  Reason  :  The answer results in Range overflow when a 4-bit ALU which is based on 1’complement arithmetic is used to the addition   1101 + 1011. | |
| **167.** | | Answer :   (b)  Reason  :  The function AB’C + ABC can be realized by using 3 gates. | |
| **168.** | | Answer :   (a)  Reason  :  The equivalent binary number of 11.812510 is 1011.1101. | |
| **169.** | | Answer :   (b)  Reason  :  The decimal equivalent of 110010 based on Two’s complement arithmetic is –13. | |
| **170.** | | Answer :   (a)  Reason  :  Combinational circuits has memory. | |
| **171.** | | Answer :   (b)  Reason  :  Arithmetic-logic unit is responsible for coordinating various operations using timing signals. | |
| **172.** | | Answer :   (a)  Reason  :  The data inside a computer is represented in Binary form i.e (0’s and 1’s). | |
| **173.** | | Answer :   (b)  Reason  :  A parity bit is used to detect errors. | |
| **174.** | | Answer :   (d)  Reason  :  only (I) and (II) are correct. | |
| **175.** | | Answer :   (a)  Reason  :  The most compact form of Boolean expression which corresponds to the map is | |
| **176.** | | Answer :   (d)  Reason  :  The information which will be used in near future is likely to be in use already is Temporal Locality | |
| **177.** | | Answer :   (c)  Reason  :  The page replacement algorithm where thee is a replacement of a page ,which will not be used for the longest period of time is OPT | |
| **178.** | | Answer :   (a)  Reason  :  A Strobe pulse is supplied by one unit to indicate the other unit when the transfer has to occur | |
| **179.** | | Answer :   (c)  Reason  :  A Set of Logical Addresses is called Address Space. | |
| **180.** | | Answer :   (c)  Reason  :  CRC is used for checking errors in transmission. | |
| **181.** | | Answer :   (b)  Reason :            The first computer architecture having stored program is Von-Neumann | |
| **182.** | | Answer :   (c)  Reason :            Large-scale integrated and very large-scale integrated circuits are used  in the IV generation. | |
| **183.** | | Answer :   (a)  Reason :            The x value is 01000011 | |
| **184.** | | Answer :   (c)  Reason :            The gray code of 1001 is 1101 | |
| **185.** | | Answer :   (a)  Reason :            Over –flow flag will be set . | |
| **186.** | | Answer :   (a)  Reason :            The binary adder is used to add binary numbers of any length | |
| **187.** | | Answer :   (d)  Reason :            Unsigned binary representation occupies less space to store the number +255. | |
| **188.** | | Answer :   (e)  Reason :            If 2n data inputs lines are connected to a MUX then there will be n Selection lines.                   For  8-to -1 MUX 23 input lines and 3 selection lines are possible | |
| **189.** | | Answer :   (d)  Reason :            The complement of AB’ +C’D is ( A’+B ) ( C+D’ ) | |
| **190.** | | Answer :   (b)  Reason :            Shift registers are used for serial to parallel data. Conversion. | |