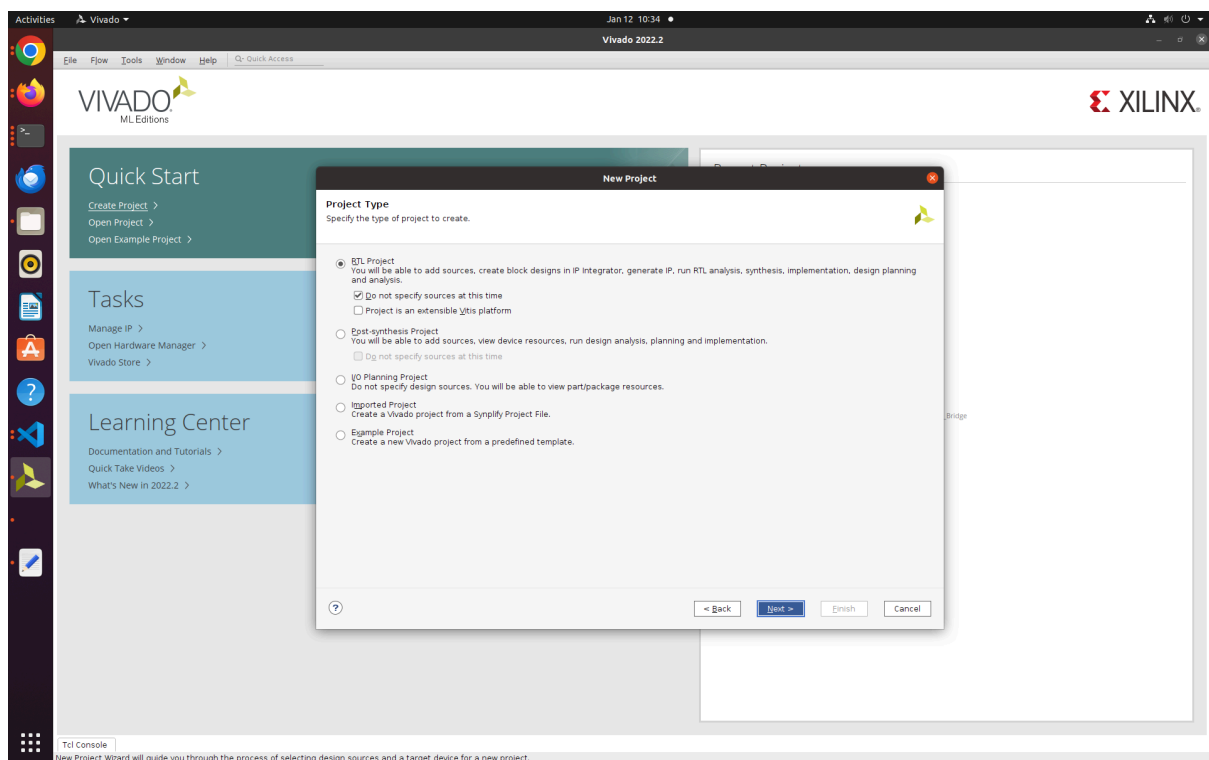
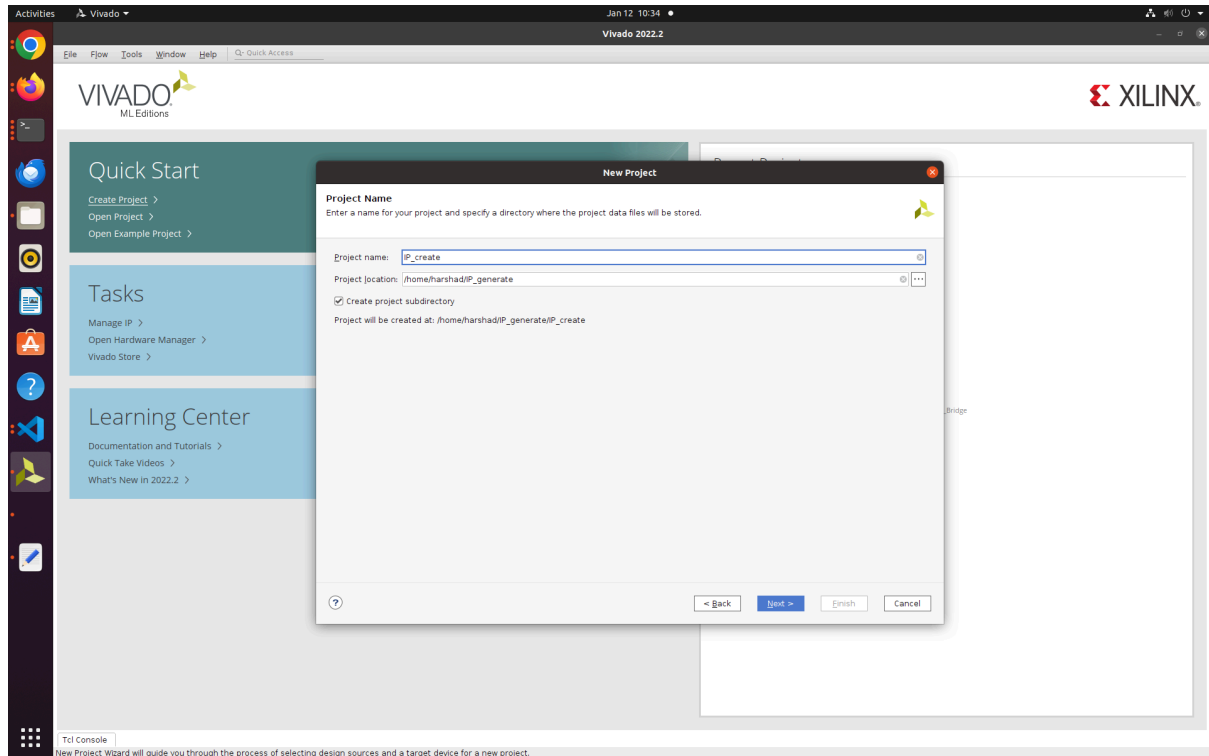


Clock wizard Generation Guide

Step 1 : Create an empty vivado project or use an existing one. Following snips show steps to create a new project.



The screenshot shows the Vivado 2017.1 IDE interface. The main window displays the 'Quick Start' and 'Learning Center' sections. A 'New Project' dialog box is open in the foreground, showing the 'Default Part' selection screen. The dialog includes a search bar, a list of parts, and a table of board connections. The 'Kintex-7 KC705 Evaluation Platform' is selected. The 'Board Connections' table shows FMC_HPC and FMC_LPC connections.

Quick Start

- Create Project >
- Open Project >
- Open Example Project >

Tasks

- Manage IP >
- Open Hardware Manager >
- Xilinx Tcl Store >

Learning Center

- Documentation and Tutorials >
- Quick Take Videos >
- Release Notes Guide >

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: ☐ Parts ☒ Boards

Filter/Preview

Vegdon: All

Display Name: All

Board Rev: Latest

Search:

Display Name	Vendor	Board Rev	Part
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	@xc7z020cig484-1
Artix-7 AC701 Evaluation Platform	xilinx.com	1.1	@xc7a200tbg676
Kintex-7 KC705 Evaluation Platform	xilinx.com	1.1	@xc7k325tfg900
Kintex-UltraScale KCUI05 Evaluation Platform	xilinx.com	1.0	@xccku040-fvwl15
Kintex UltraScale+ KCUI16 Evaluation Platform	xilinx.com	1.0	@xccku5p-fvb676-2
Kintex UltraScale KCUI500 Acceleration Development Board	xilinx.com	1.0	@xccku115-fvb210

Board Connectors

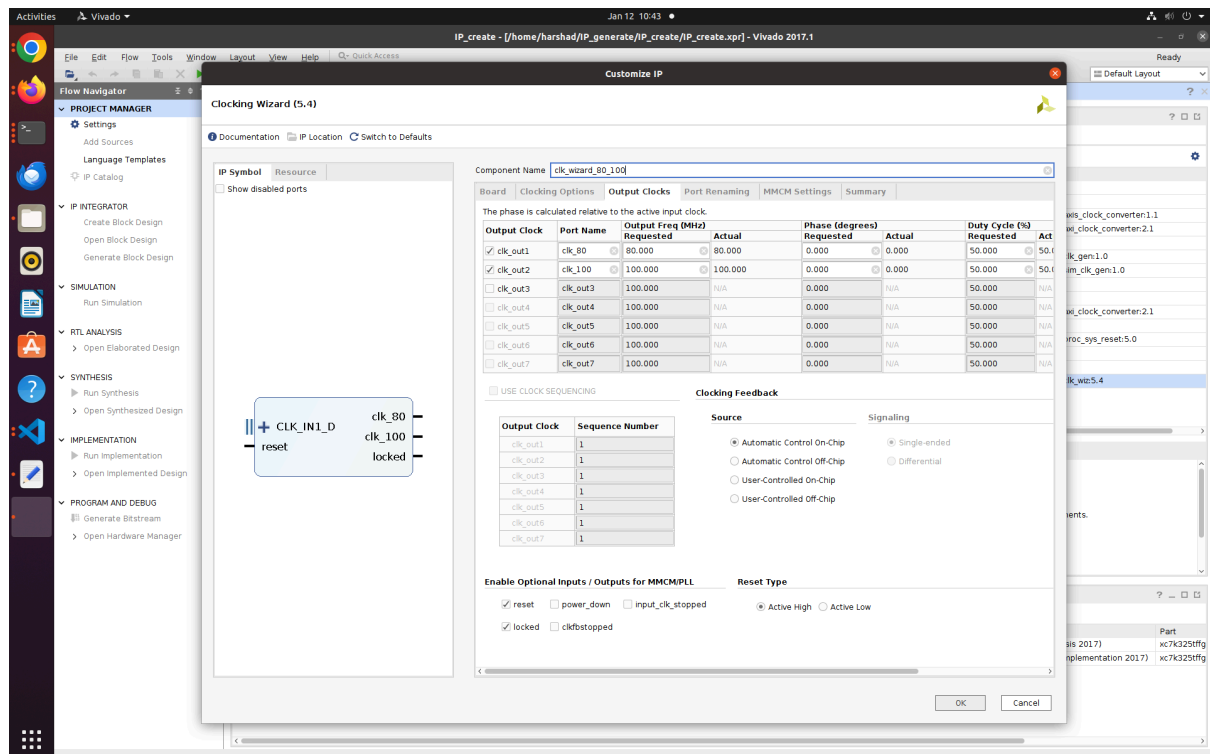
FMC_HPC

FMC_LPC

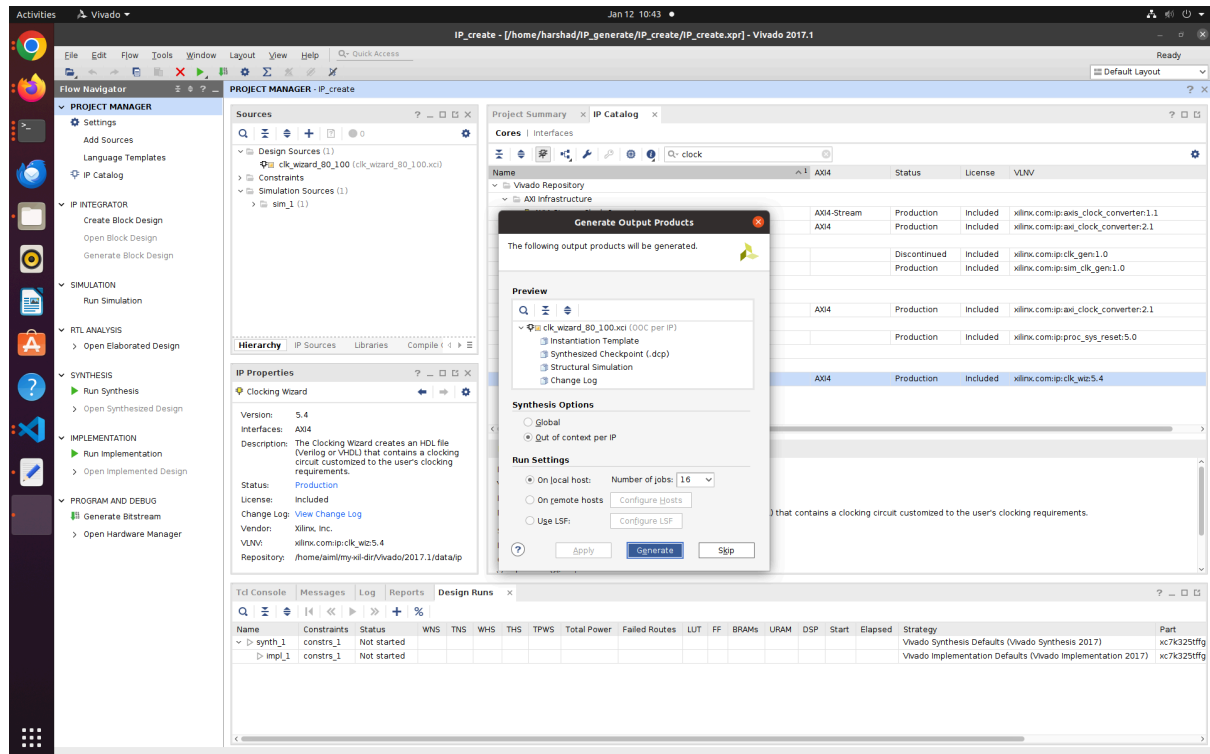
Target Connections

[illegible]

(input is System differential clock)



Step 4: Generate the IP, wait for the completion of synthesis.



Step 5: go to <project_name>.srcs folder, inside this you will find the IP folder, contents of which are as follows, (ensure it has a .xci file)

