



VC709 MIG Design Creation

January 2013

XTP235

Revision History

Date	Version	Description
01/18/13	3.0	Regenerated for 2012.4. Added AR53420.
10/23/12	2.0	Regenerated for 2012.3.
09/20/12	1.0	Initial version.

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Overview

➤ **VC709 Board**

➤ **VC709 Setup**

➤ **Generate MIG Bank A Example Design**

- Modifications to Example Design
- Compile Example Design
- Run MIG Example Design

➤ **Generate MIG Bank B Example Design**

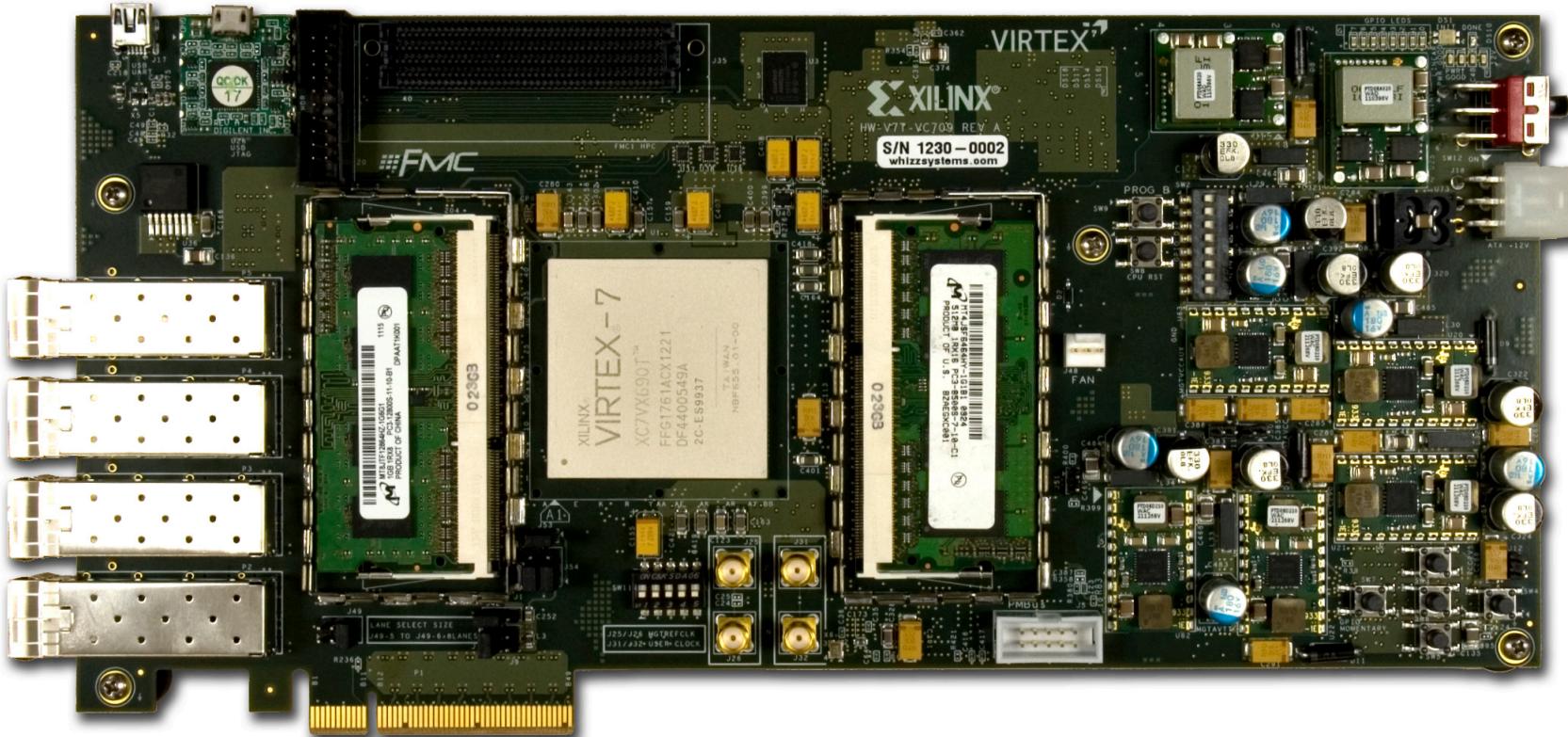
- Modifications to Example Design
- Compile Example Design
- Run MIG Example Design

➤ **Generate MIG Bank A and B Example Design**

- Modifications to Example Design
- Compile Example Design
- Run MIG Example Design

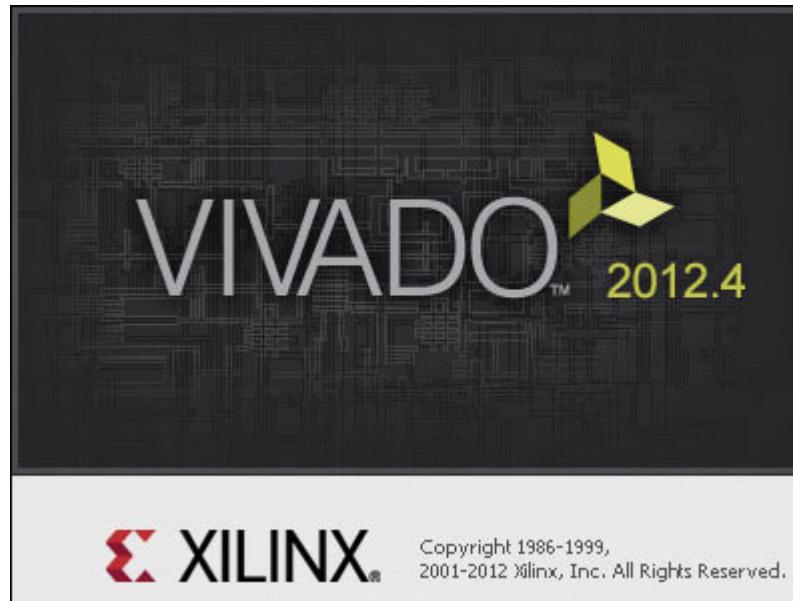
➤ **References**

Xilinx VC709 Board



Vivado Software Requirements

- Xilinx Vivado Design Suite 2012.4, Design Edition



ChipScope Pro Software Requirement

- Xilinx ChipScope Pro 14.4 software



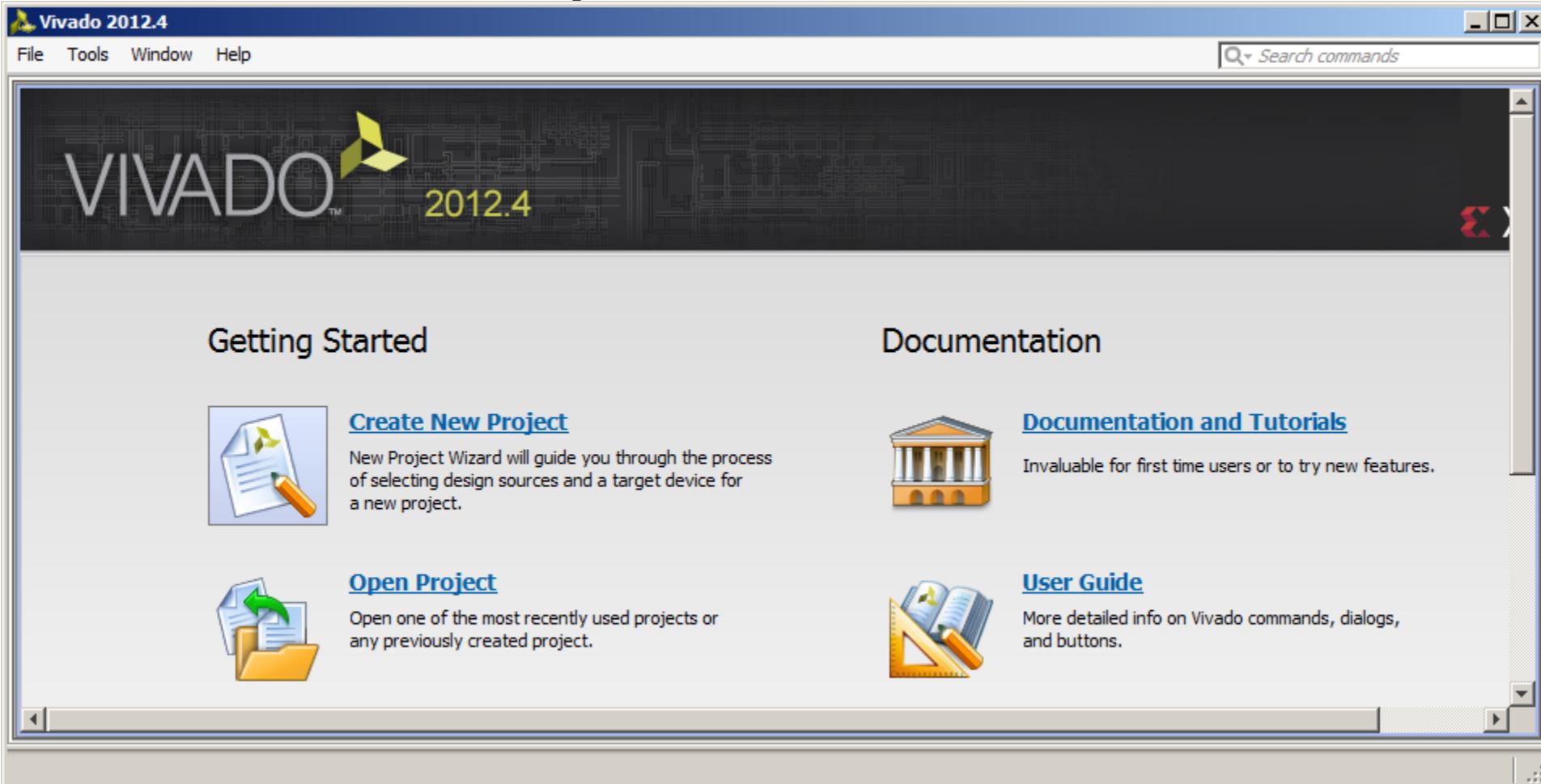
Generate MIG Bank A Example Design

Generate MIG Bank A Example Design

► Open Vivado

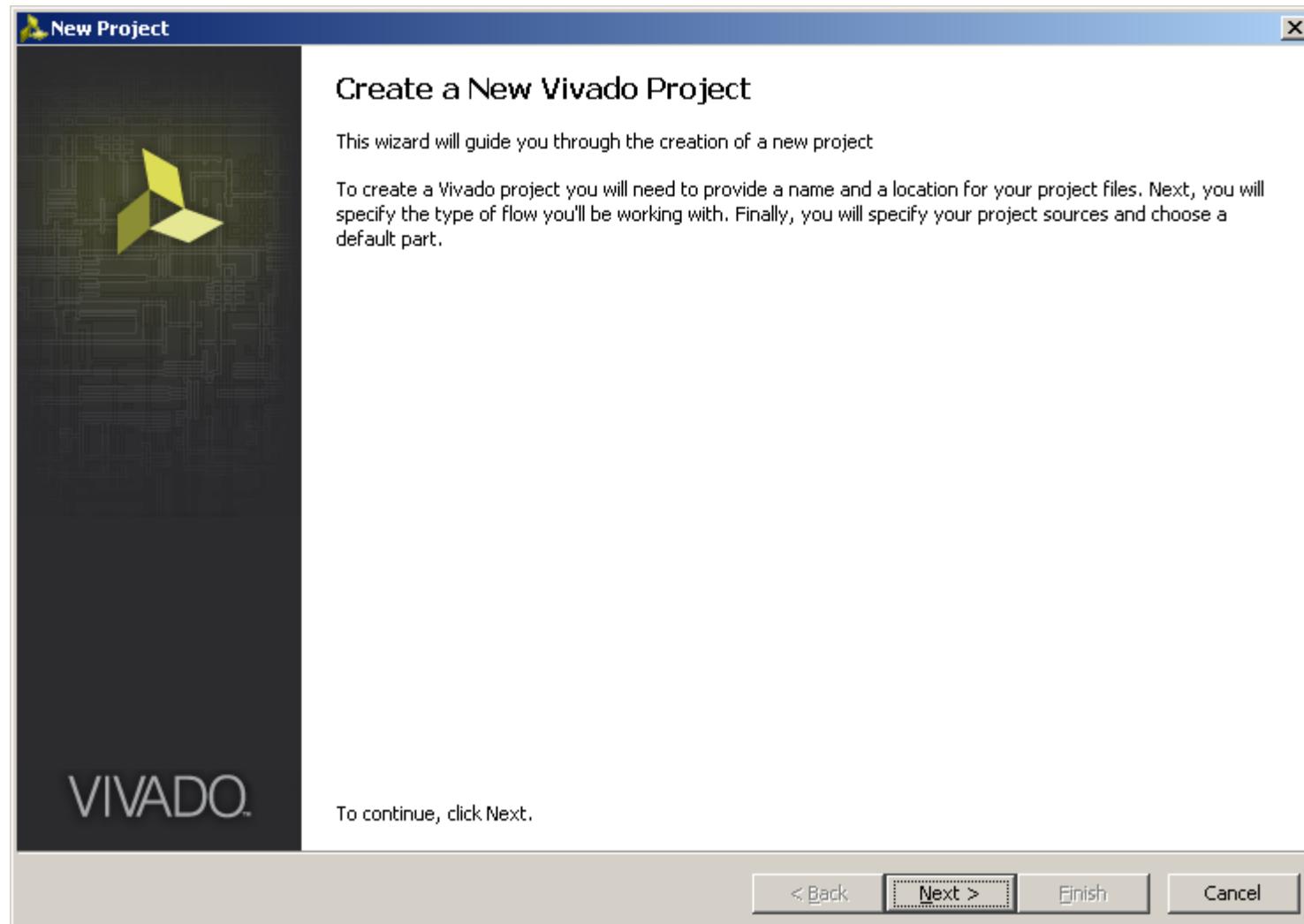
Start → All Programs → Xilinx Design Tools → Vivado 2012.4 → Vivado

► Select Create New Project



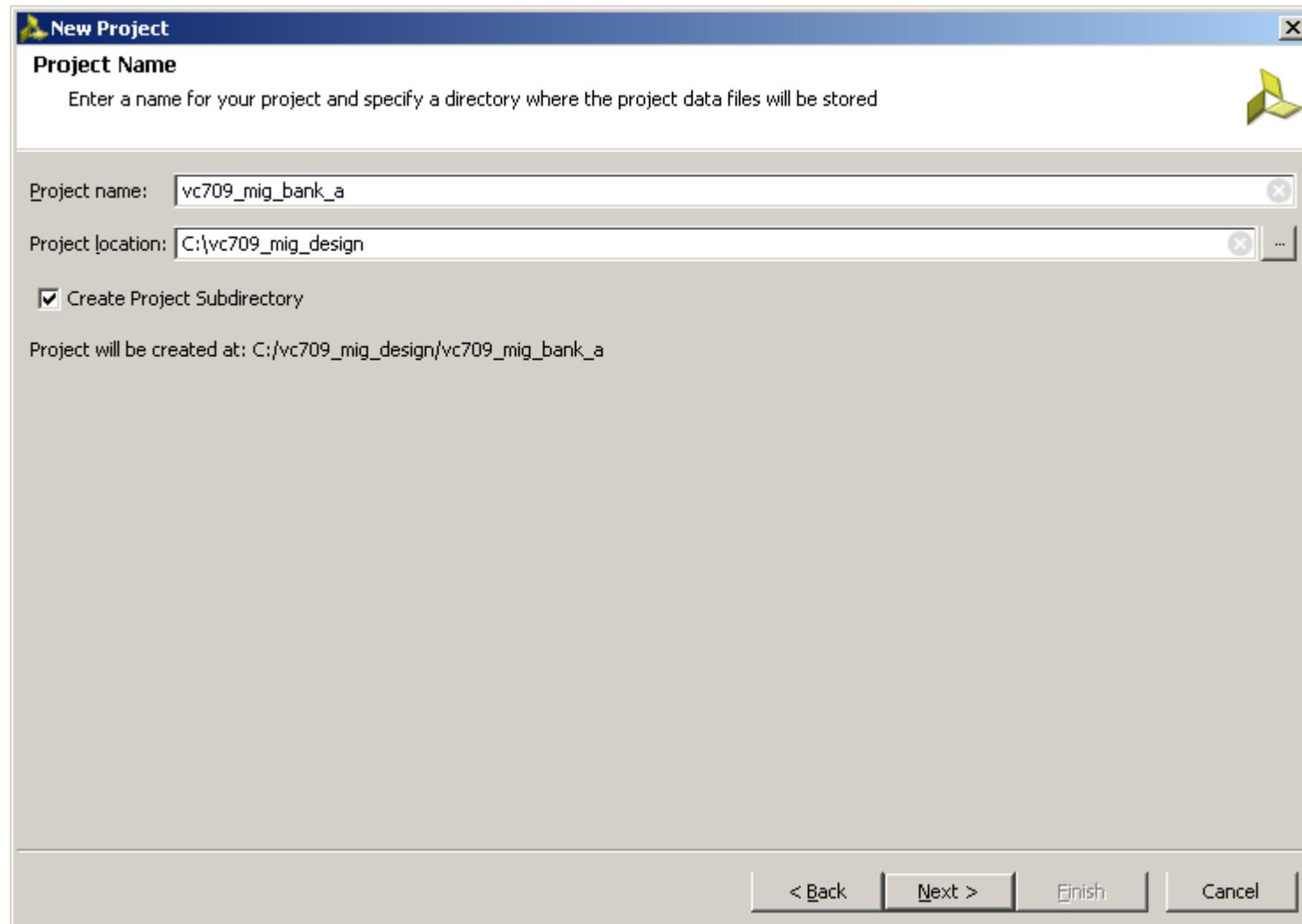
Generate MIG Bank A Example Design

► Click Next



Generate MIG Bank A Example Design

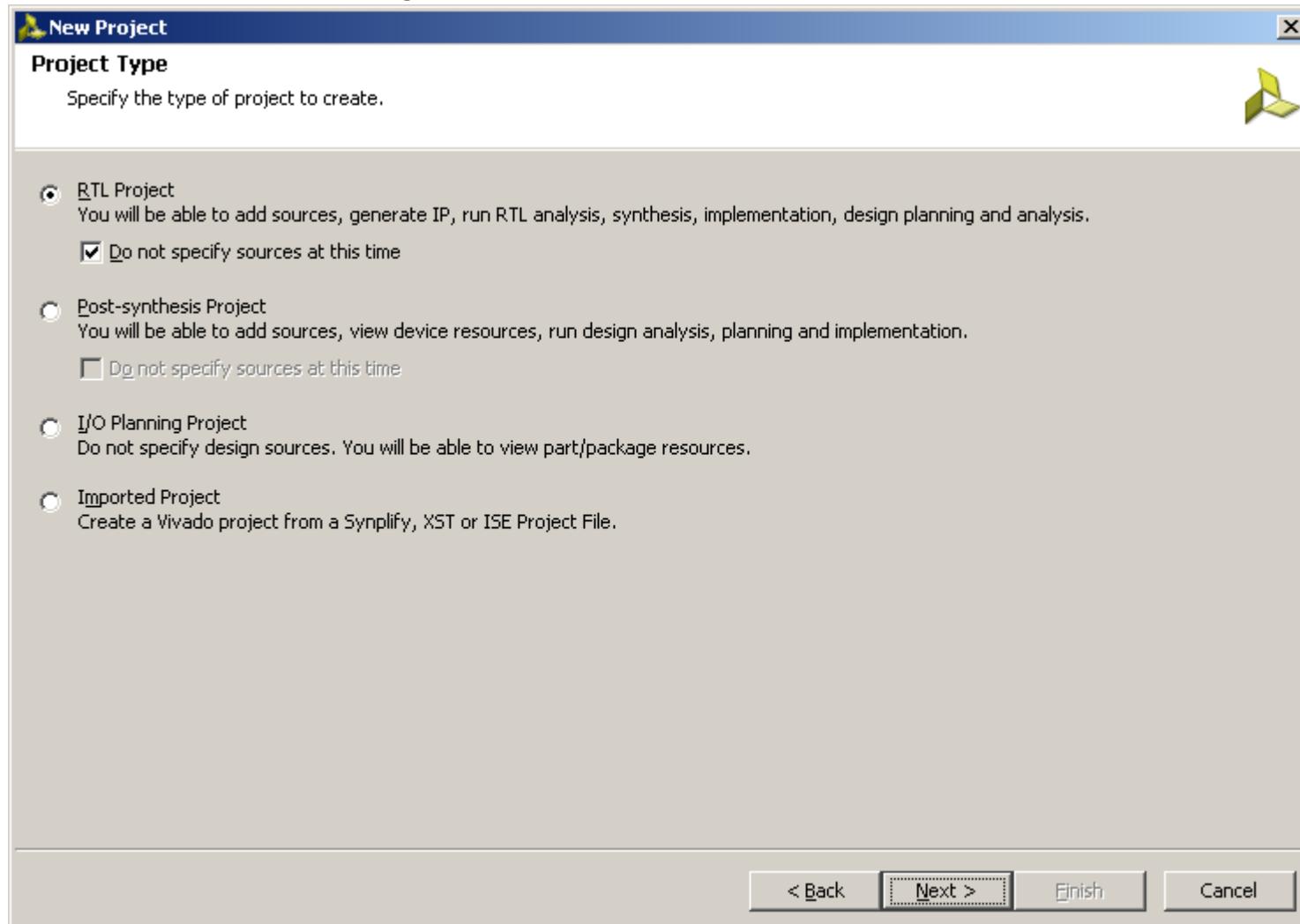
- Set the Project name to vc709_mig_bank_a and location to C:\vc709_mig_design



Generate MIG Bank A Example Design

► Select RTL Project

- Select **Do not specify sources at this time**



Generate MIG Bank A Example Design

- ▶ Select the xc7vx690tffg1761-2 device

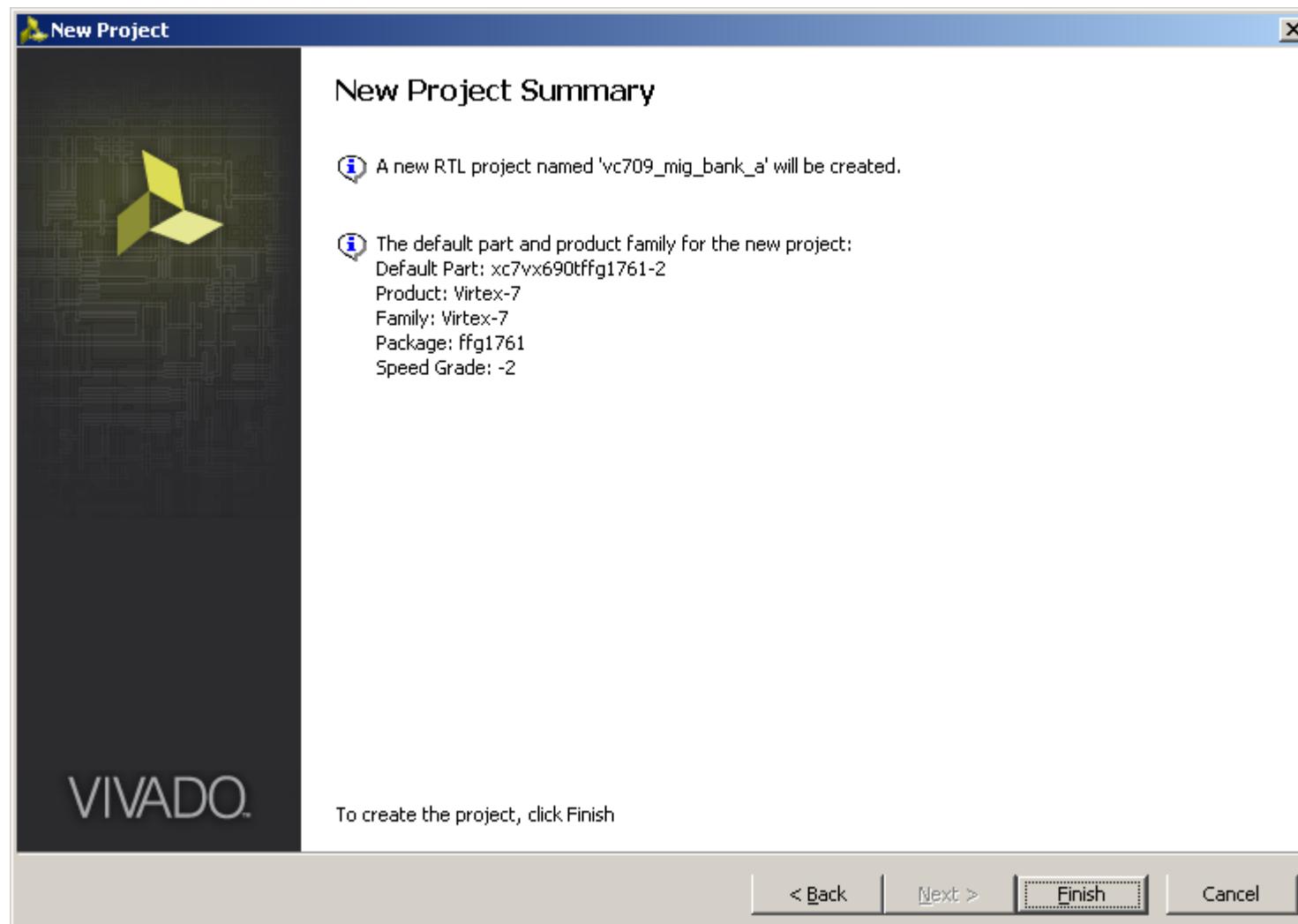
The screenshot shows the 'New Project' dialog box with the title 'Default Part'. The 'Parts' tab is selected in the sidebar. The filter settings are set to 'Product category: All', 'Package: FFG1761', 'Family: Virtex-7', 'Speed grade: -2', and 'Temp grade: All Remaining'. A search bar at the bottom left contains the text 'xc7vx690tffg1761-2'. The main table lists four device options:

Device	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	DSPs	Gb Transceivers	PCI Buses
xc7v585tffg1761-2	1,761	850	364200	728400	795	1260	36	3
xc7vx330tffg1761-2	1,761	700	204000	408000	750	1120	28	2
xc7vx485tffg1761-2	1,761	700	303600	607200	1030	2800	28	4
xc7vx690tffg1761-2	1,761	850	433200	866400	1470	3600	36	3

At the bottom of the dialog, there are buttons for '< Back', 'Next >', 'Finish', and 'Cancel'.

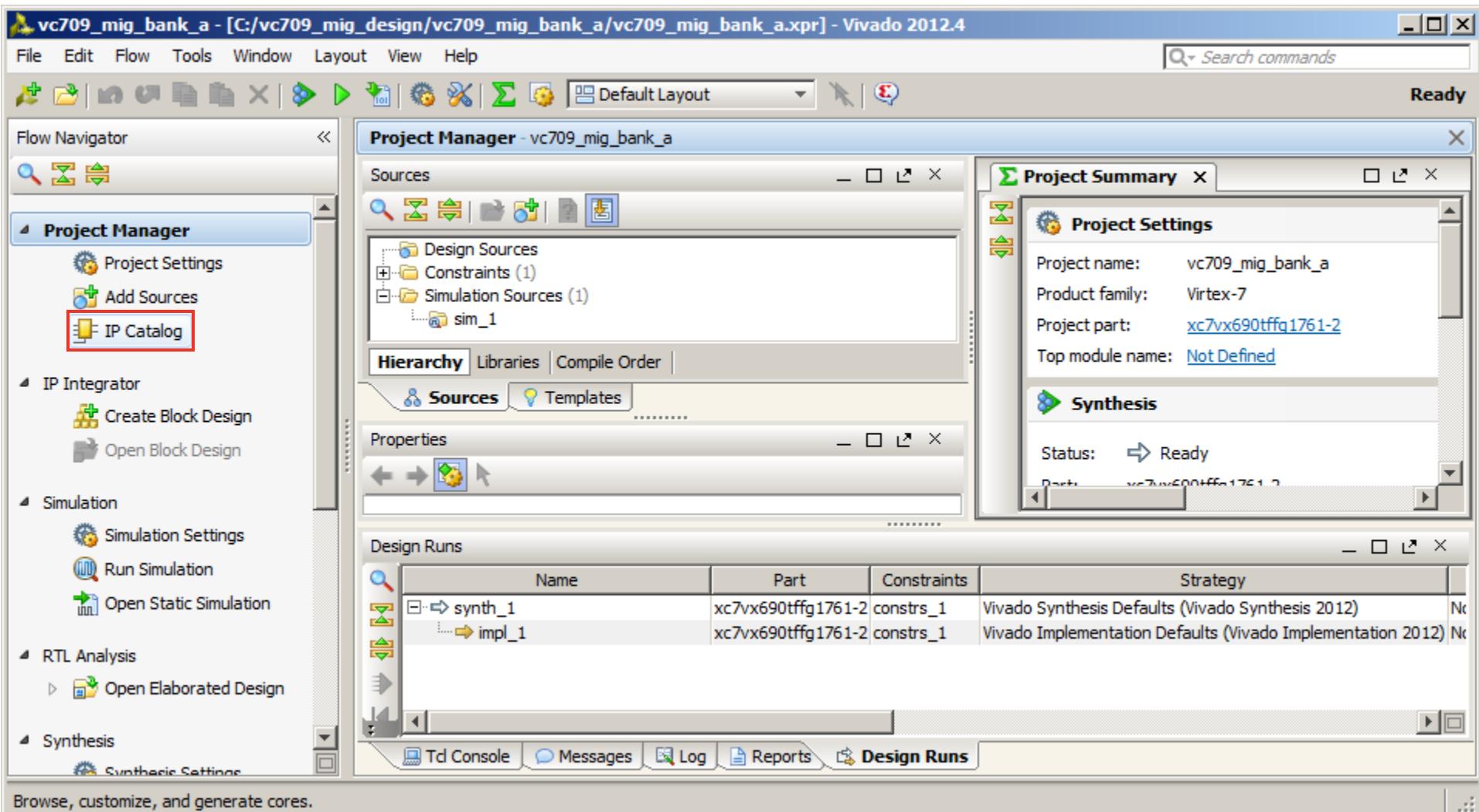
Generate MIG Bank A Example Design

► Click Finish



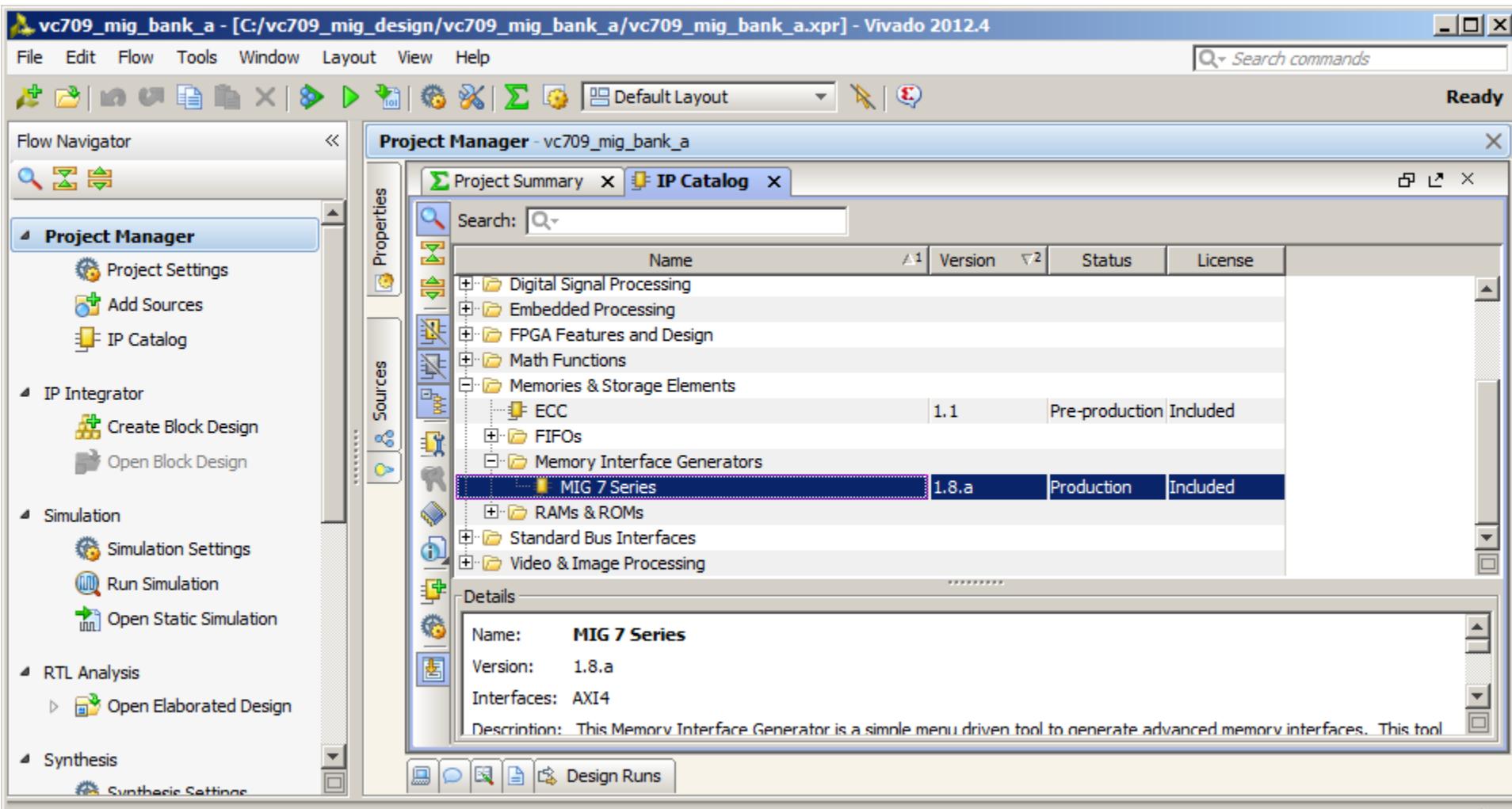
Generate MIG Bank A Example Design

► Click on IP Catalog



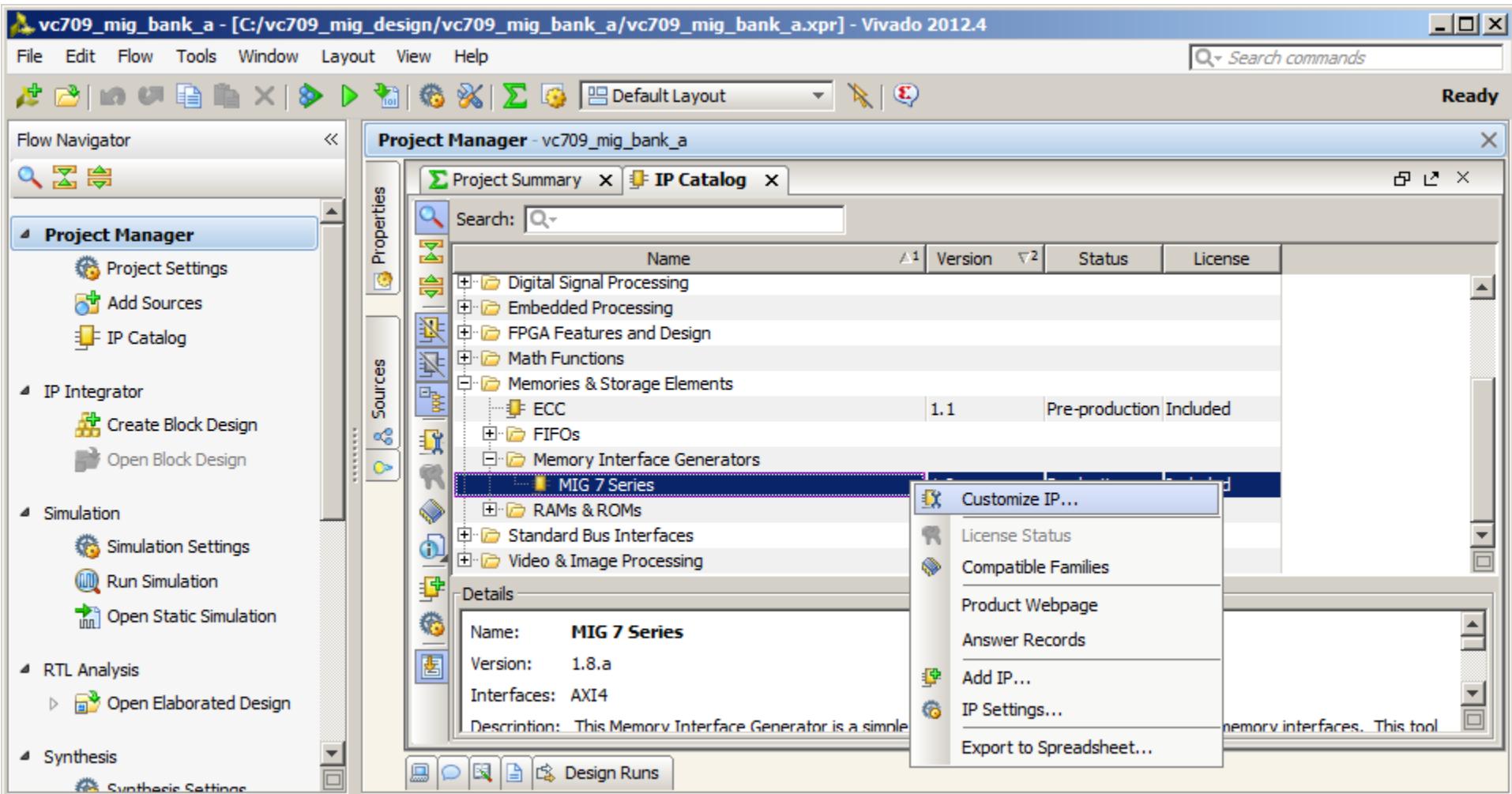
Generate MIG Bank A Example Design

► Select MIG 7 Series under Memory Interface Generators

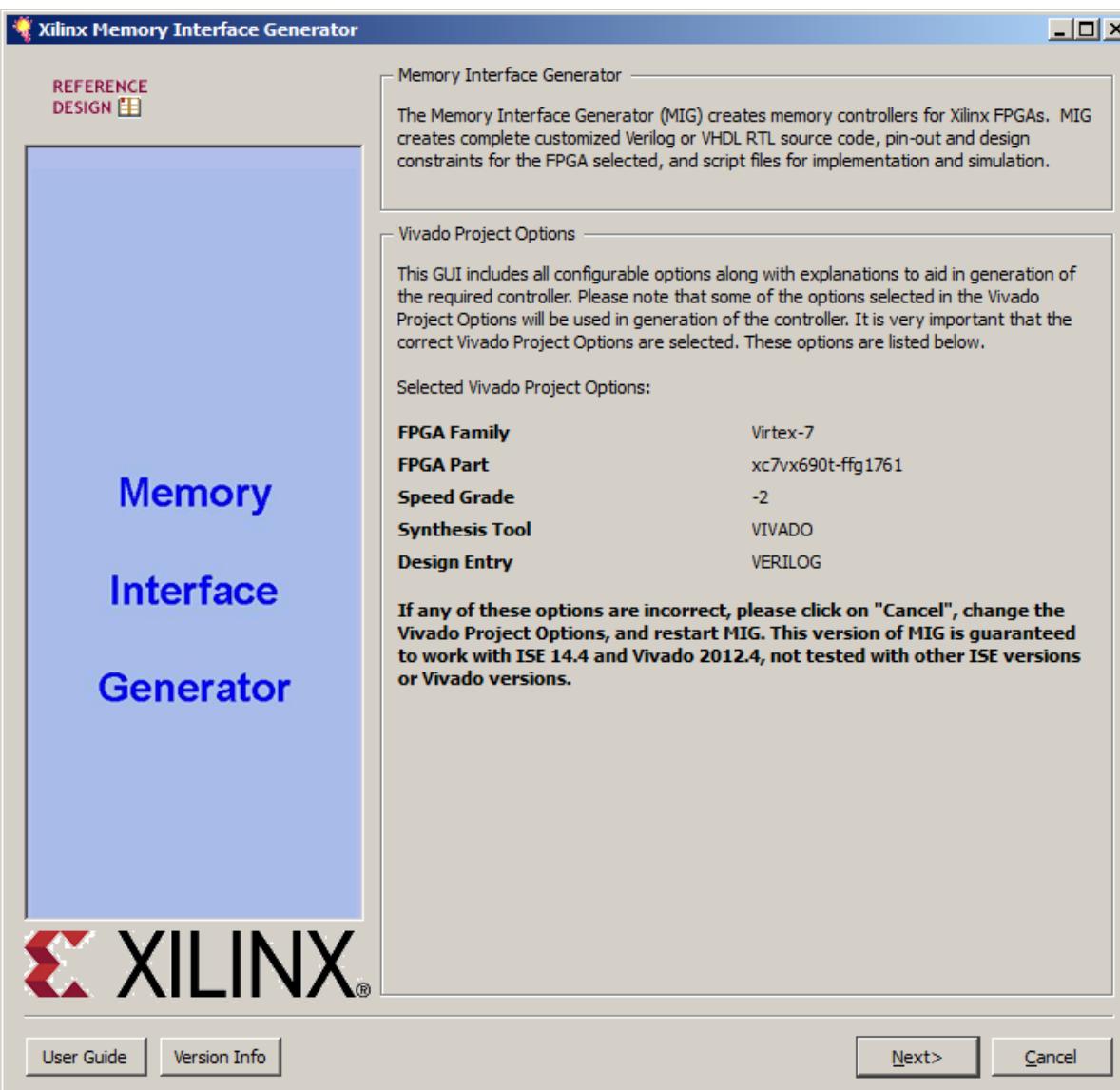


Generate MIG Bank A Example Design

- Right click on MIG 7 Series Version 1.8.a
 - Select Customize IP

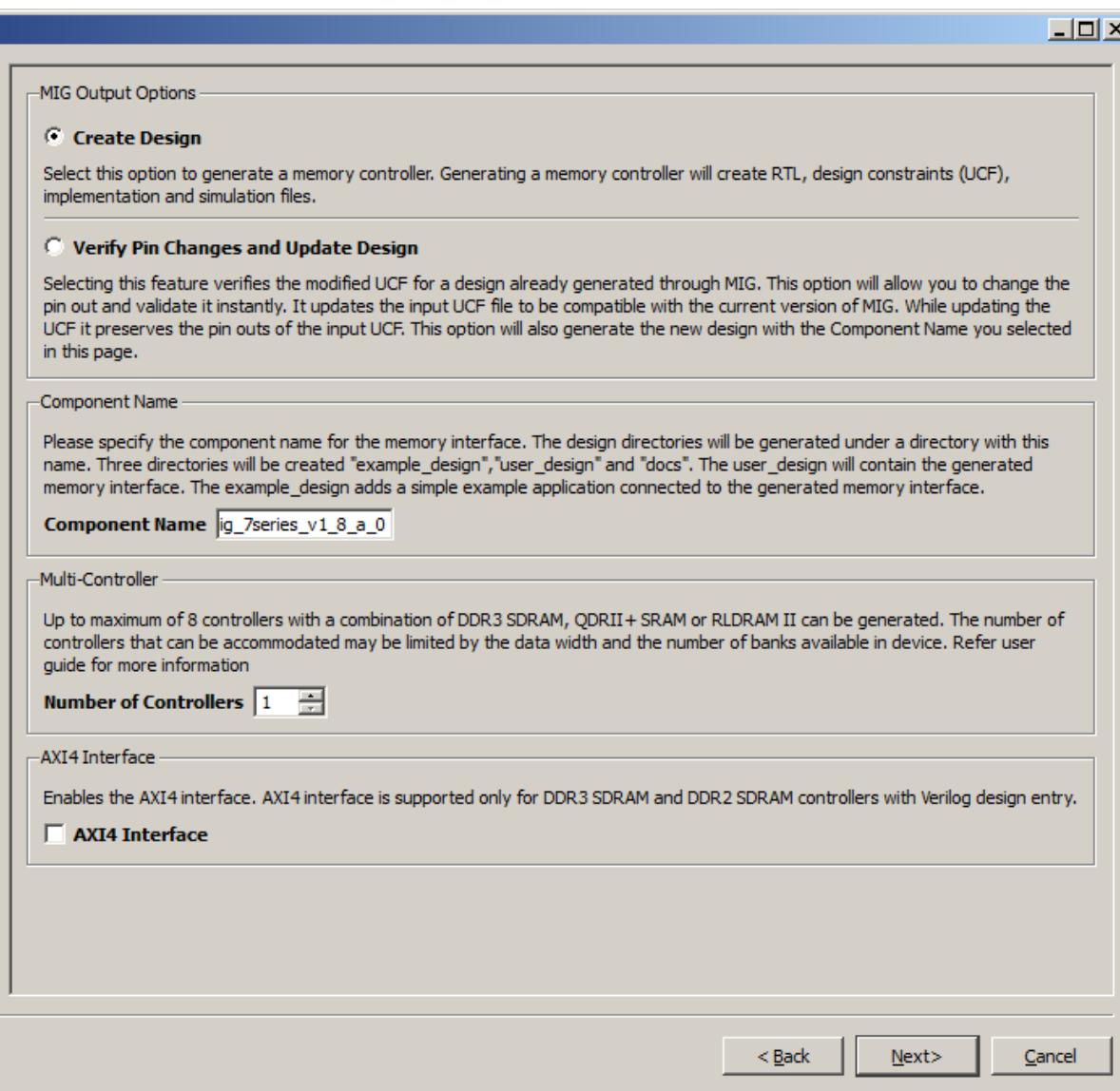


Generate MIG Bank A Example Design



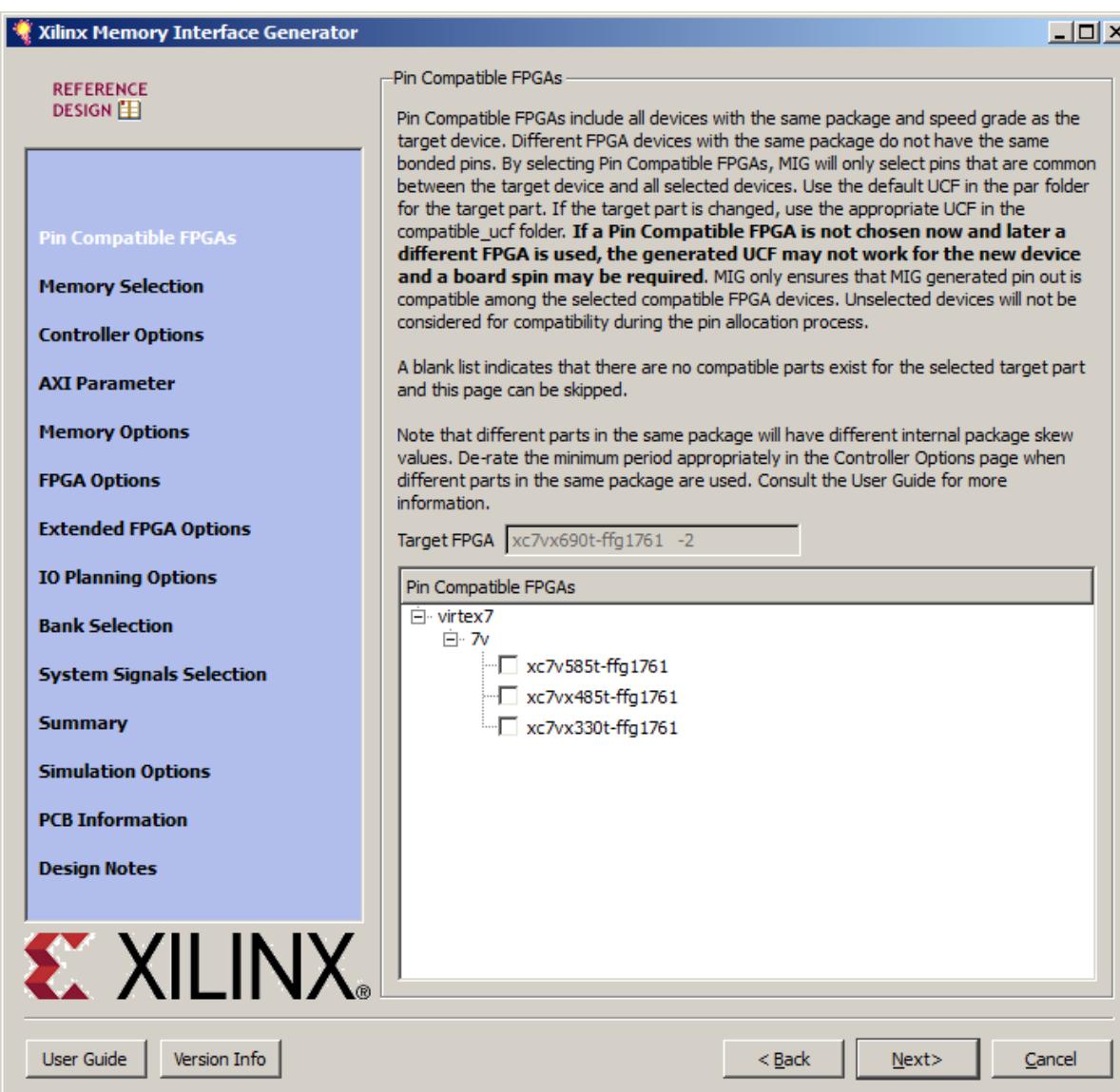
➤ Leave this page as is
– Click Next

Generate MIG Bank A Example Design



➤ Leave this page as is
– Click Next

Generate MIG Bank A Example Design



➤ Leave this page as is
– Click Next

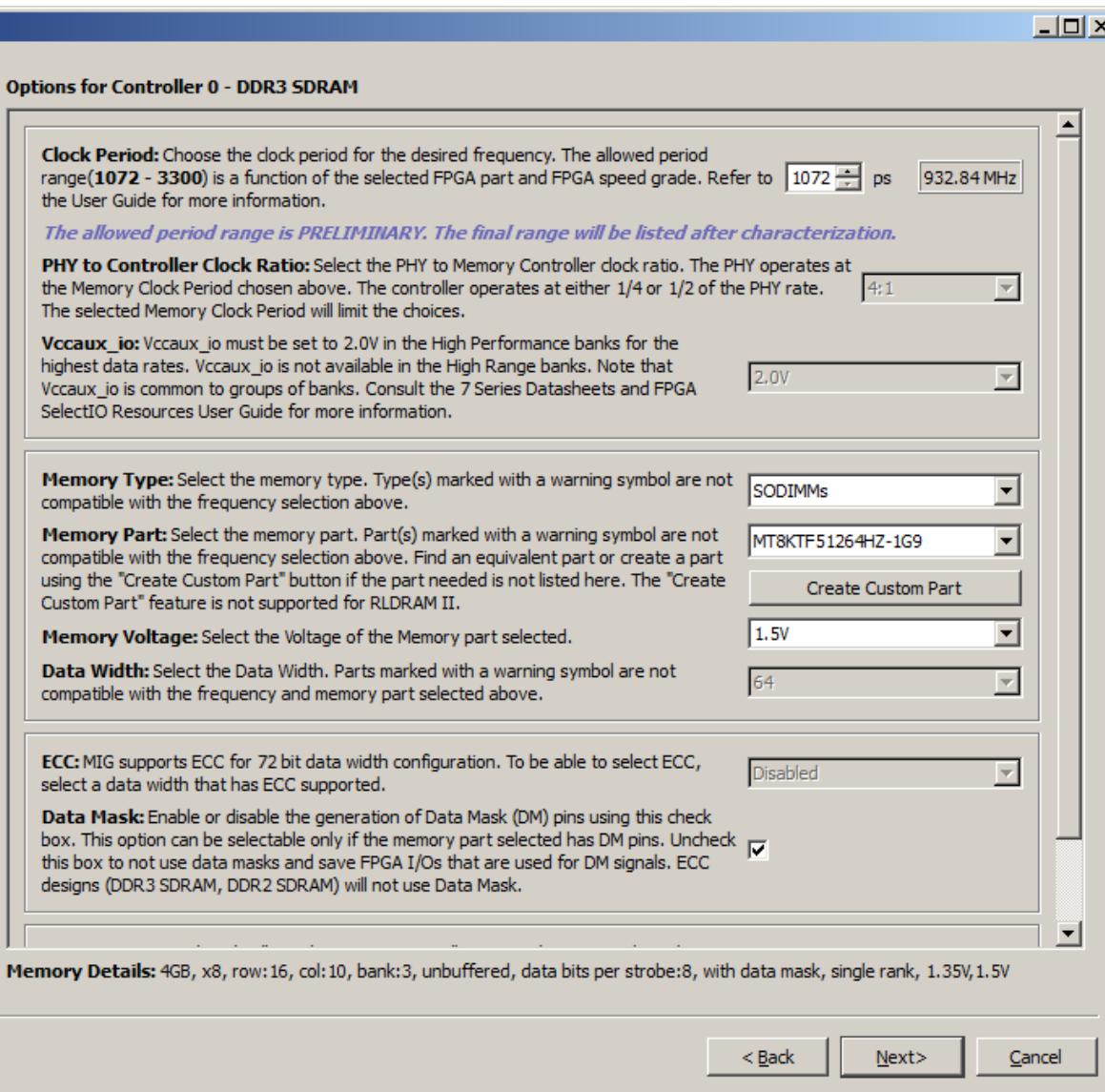
Generate MIG Bank A Example Design



► Select Memory Type

- DDR3 SDRAM
- Click Next

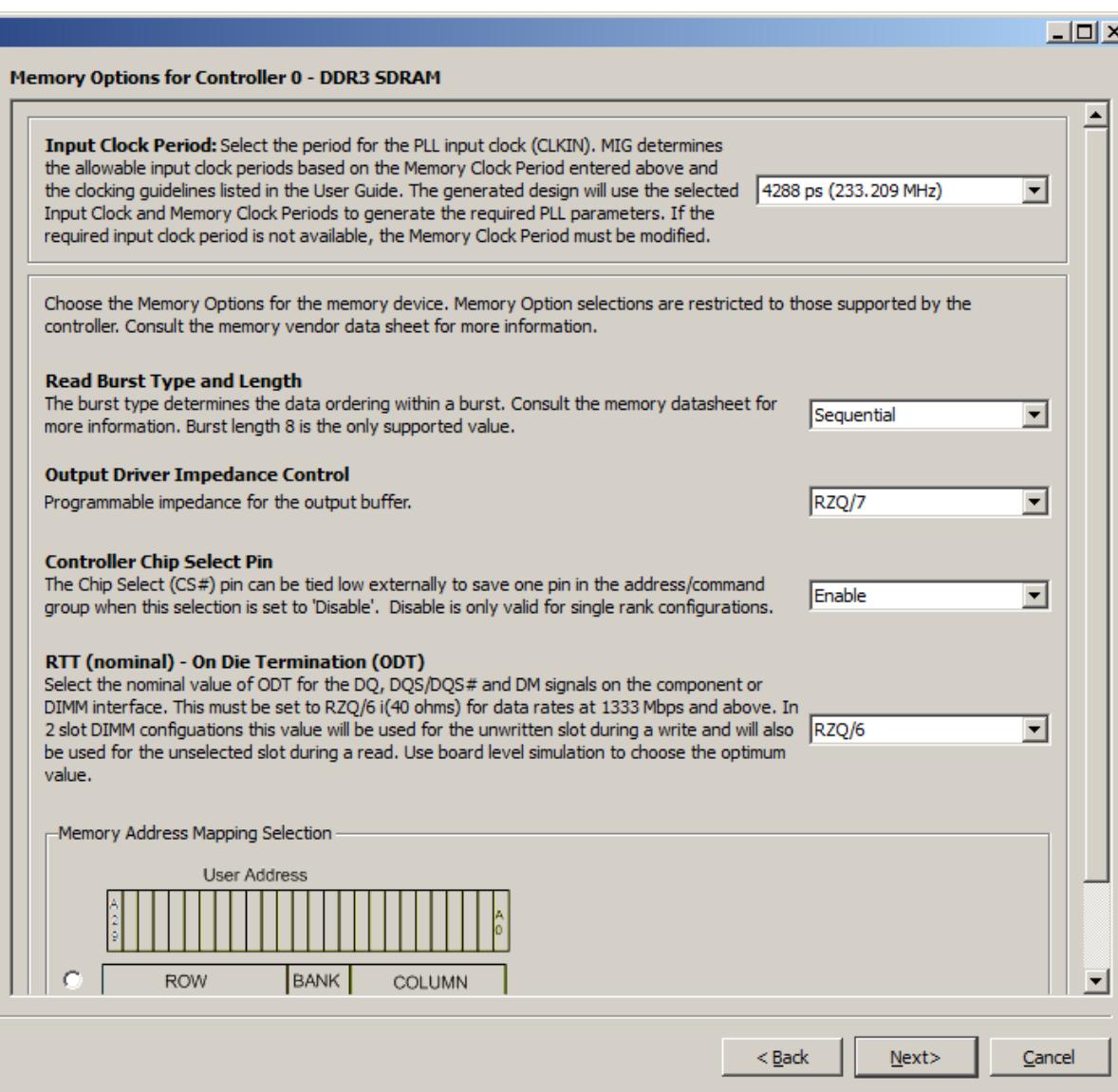
Generate MIG Bank A Example Design



► Select

- Clock Period: **1072 ps**
- Type: **SODIMMs**
- Part:
MT8KTF51264HZ-1G9
- Memory Voltage: **1.5V**
- Data Mask: **Checked**
- Click Next

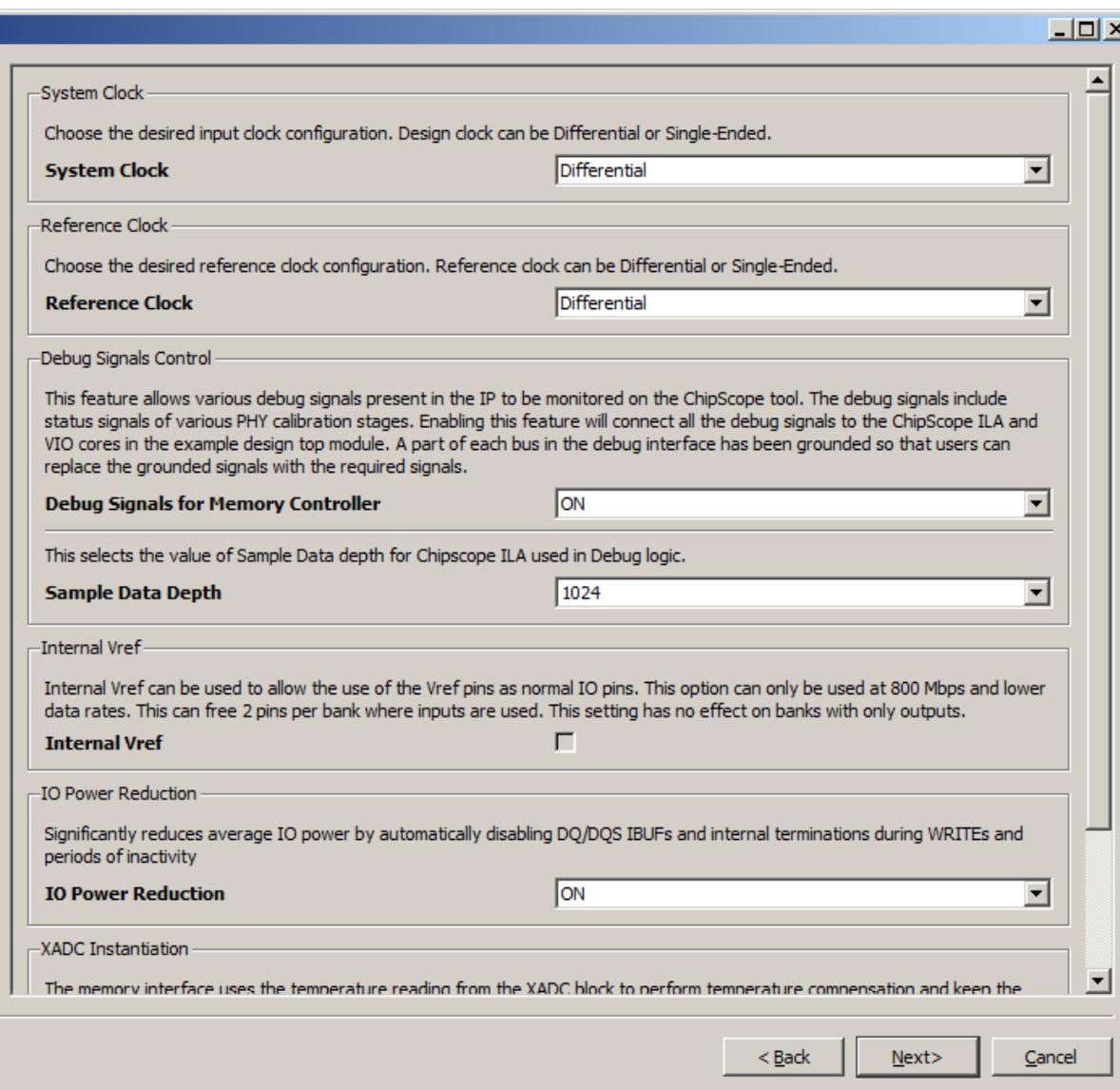
Generate MIG Bank A Example Design



► Select:

- Input Clock Period: **4288 ps**
- RTT: **RZQ/6**
- Click Next

Generate MIG Bank A Example Design



► Select

- Set the System and Reference Clocks to **Differential**
- Debug: **ON**
- Click **Next**

Generate MIG Bank A Example Design



➤ Leave this page as is
– Click Next

Generate MIG Bank A Example Design

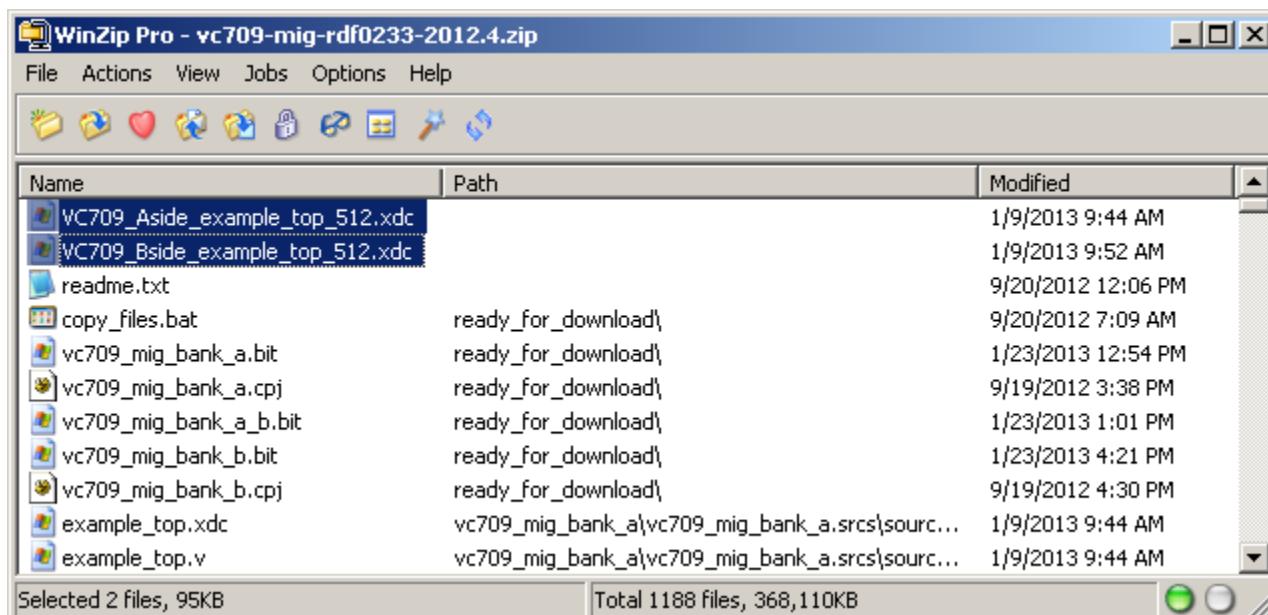


► Select Fixed Pin Out
– Click Next

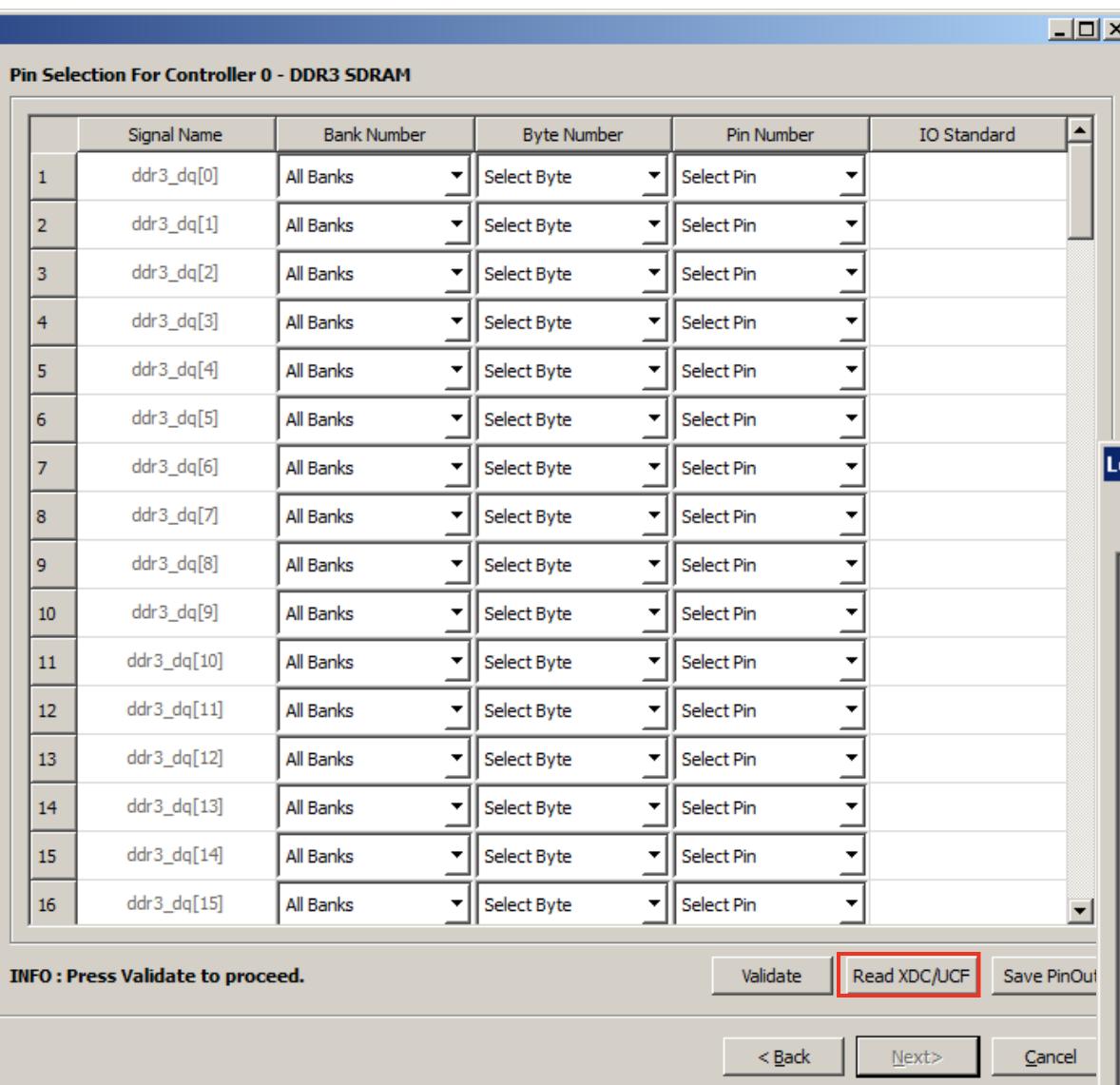
Modifications to Example Design

► Open the VC709 MIG Design Files (2012.4 CES)

- Available through <http://www.xilinx.com/vc709>
- Extract the files, **VC709_Aside_example_top_512.xdc** and **VC709_Bside_example_top_512.xdc** to C:\vc709_mig_design
- Contains the XDC constraints needed for both VC709 MIG interfaces
- This zip file will be needed later in the presentation

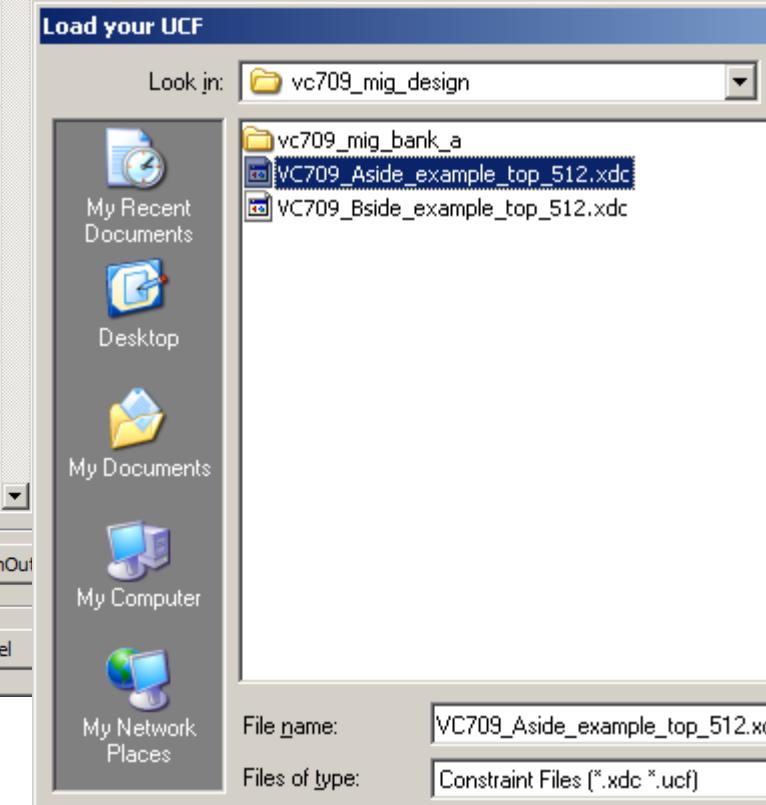


Generate MIG Bank A Example Design

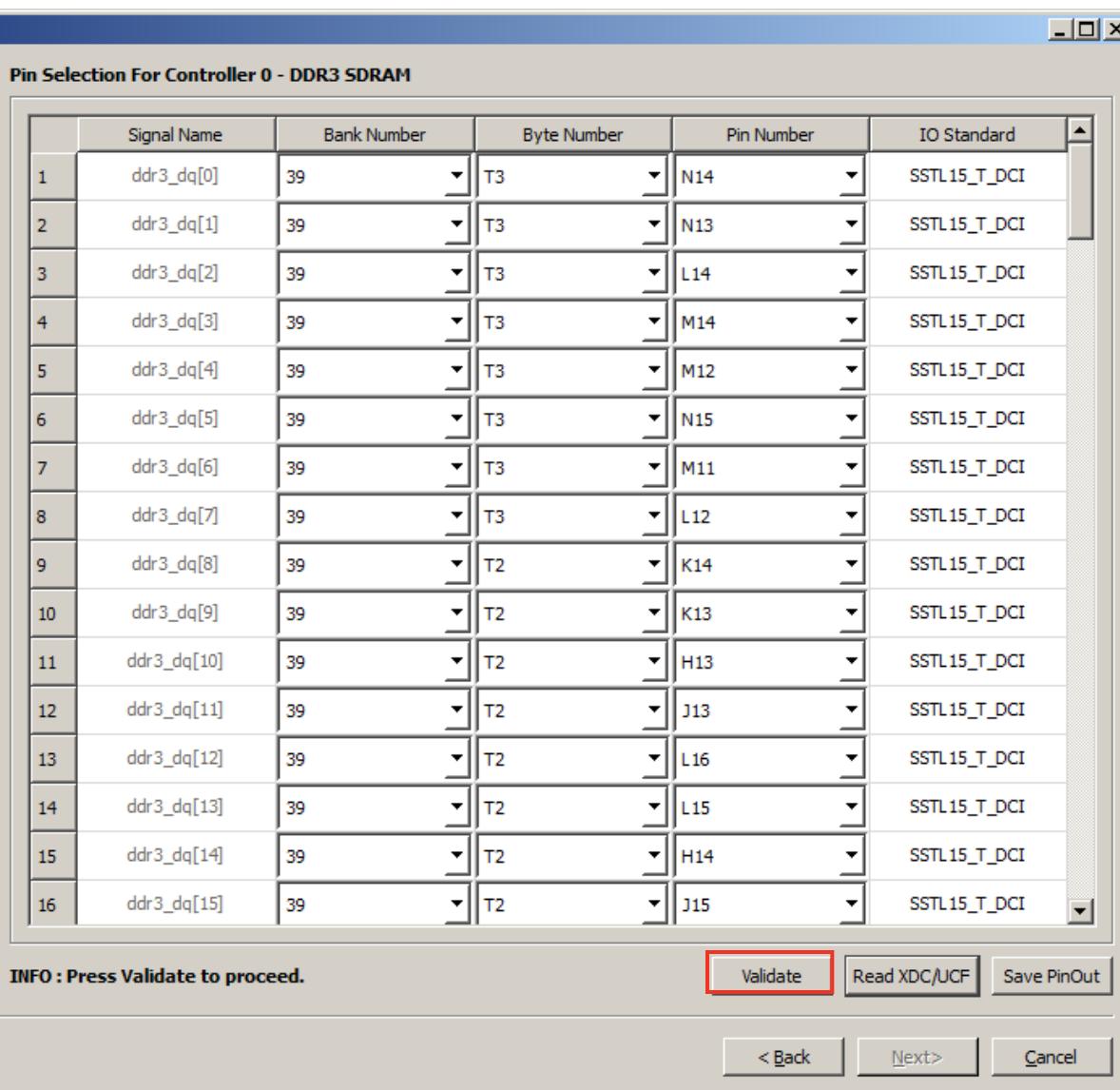


► Select Read XDC/UCF

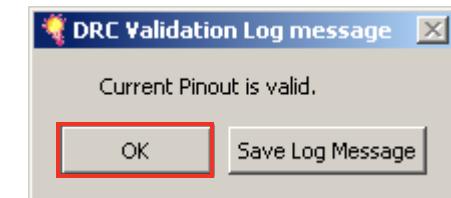
- Open the file:
VC709_Aside_example_top_512.xdc



Generate MIG Bank A Example Design



- Once it finishes reading in the XDC, click Validate
 - Click OK



Generate MIG Bank A Example Design

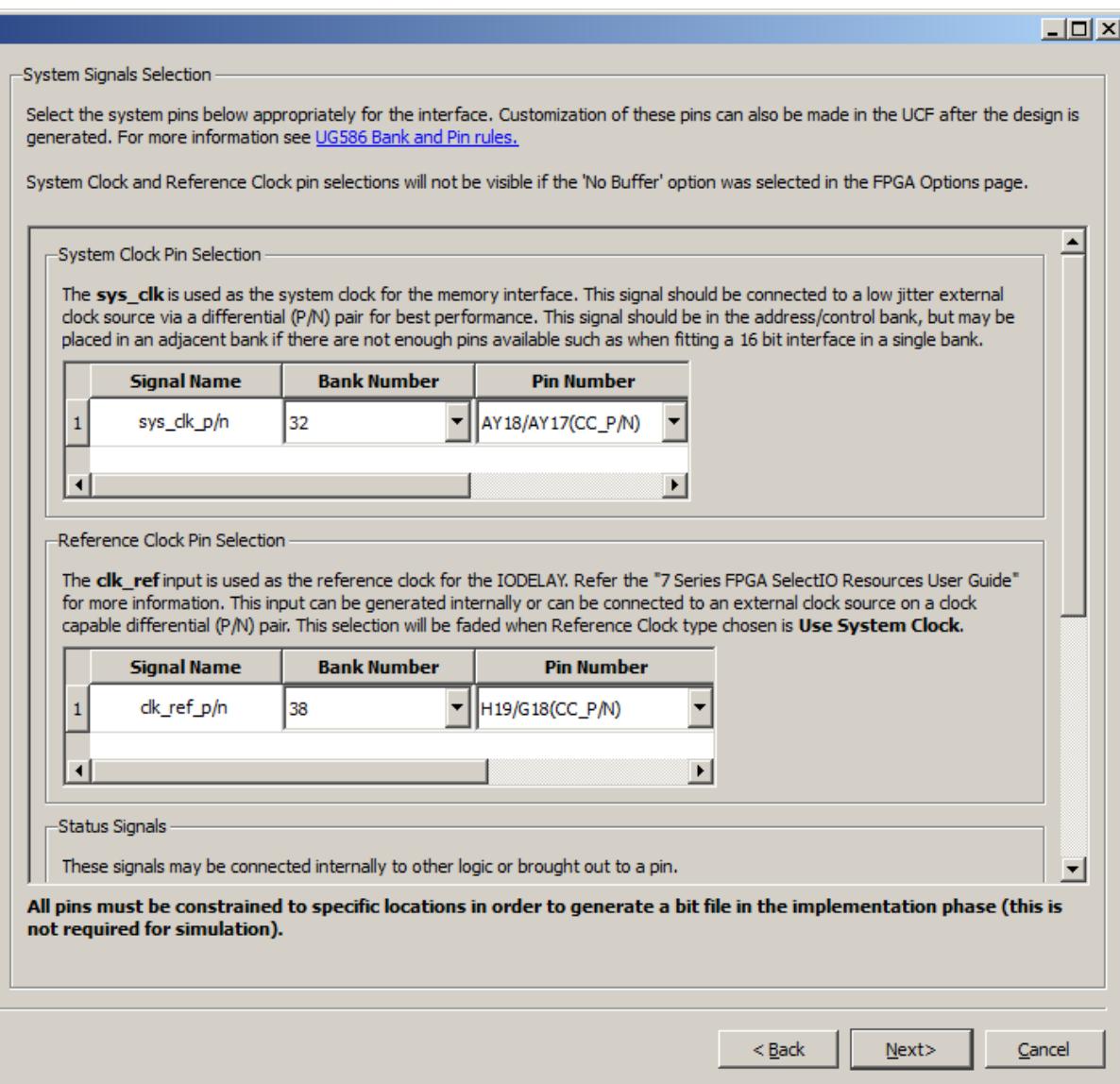
Pin Selection For Controller 0 - DDR3 SDRAM

	Signal Name	Bank Number	Byte Number	Pin Number	IO Standard
1	ddr3_dq[0]	39	T3	N14	SSTL15_T_DCI
2	ddr3_dq[1]	39	T3	N13	SSTL15_T_DCI
3	ddr3_dq[2]	39	T3	L14	SSTL15_T_DCI
4	ddr3_dq[3]	39	T3	M14	SSTL15_T_DCI
5	ddr3_dq[4]	39	T3	M12	SSTL15_T_DCI
6	ddr3_dq[5]	39	T3	N15	SSTL15_T_DCI
7	ddr3_dq[6]	39	T3	M11	SSTL15_T_DCI
8	ddr3_dq[7]	39	T3	L12	SSTL15_T_DCI
9	ddr3_dq[8]	39	T2	K14	SSTL15_T_DCI
10	ddr3_dq[9]	39	T2	K13	SSTL15_T_DCI
11	ddr3_dq[10]	39	T2	H13	SSTL15_T_DCI
12	ddr3_dq[11]	39	T2	J13	SSTL15_T_DCI
13	ddr3_dq[12]	39	T2	L16	SSTL15_T_DCI
14	ddr3_dq[13]	39	T2	L15	SSTL15_T_DCI
15	ddr3_dq[14]	39	T2	H14	SSTL15_T_DCI
16	ddr3_dq[15]	39	T2	J15	SSTL15_T_DCI

INFO : Validation successful. Press Next to proceed.

- The Next button is enabled once the pinout is validated.
 - Click Next

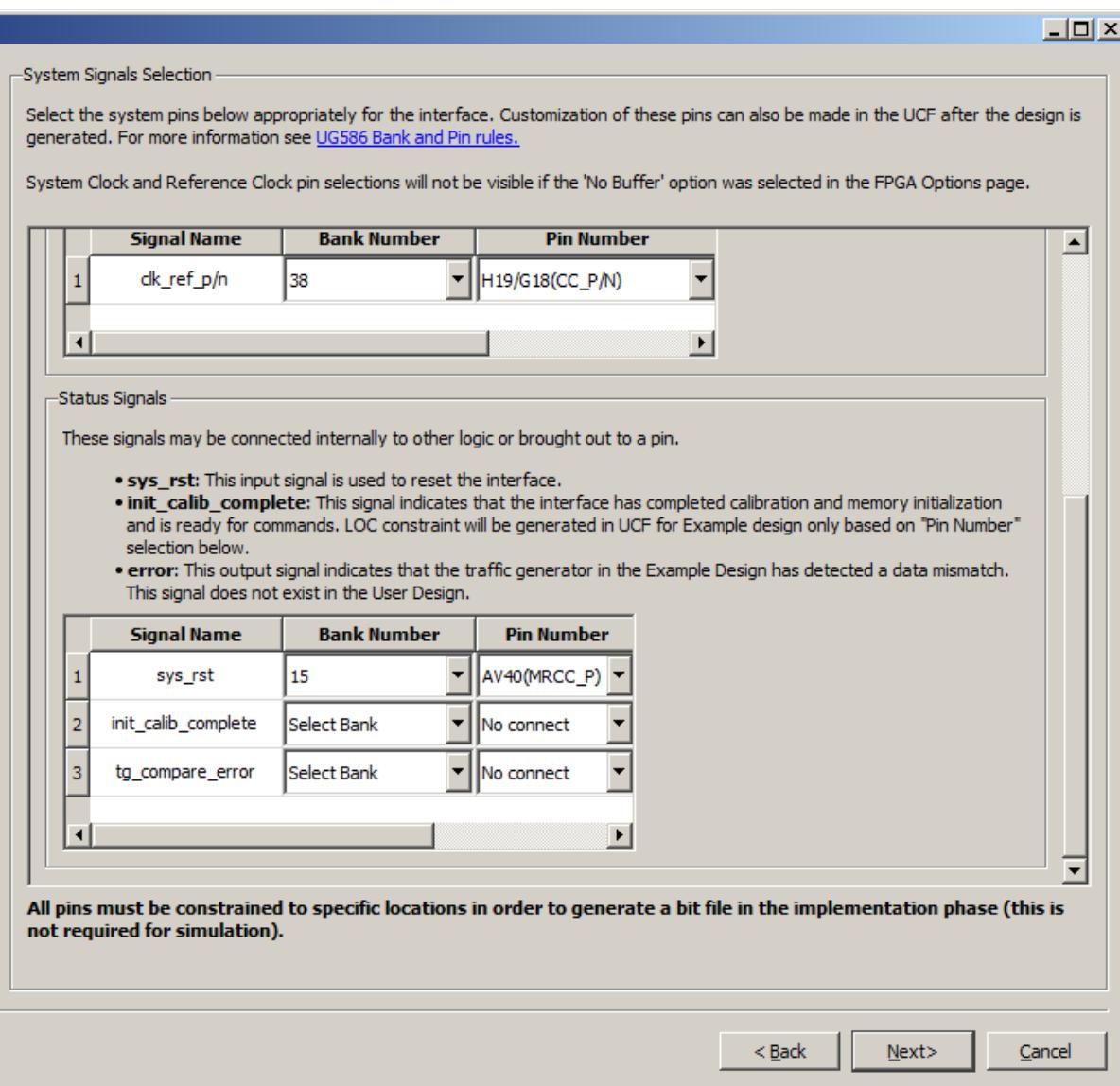
Generate MIG Bank A Example Design



➤ Make the following settings:

- Set sys_clk_p/n to Bank: **32**
- Pin Number: **AY18/AY17(CC_P/N)**
- Set clk_ref_p/n to Bank: **38**
- Pin Number: **H19/G18(CC_P/N)**
- Scroll down

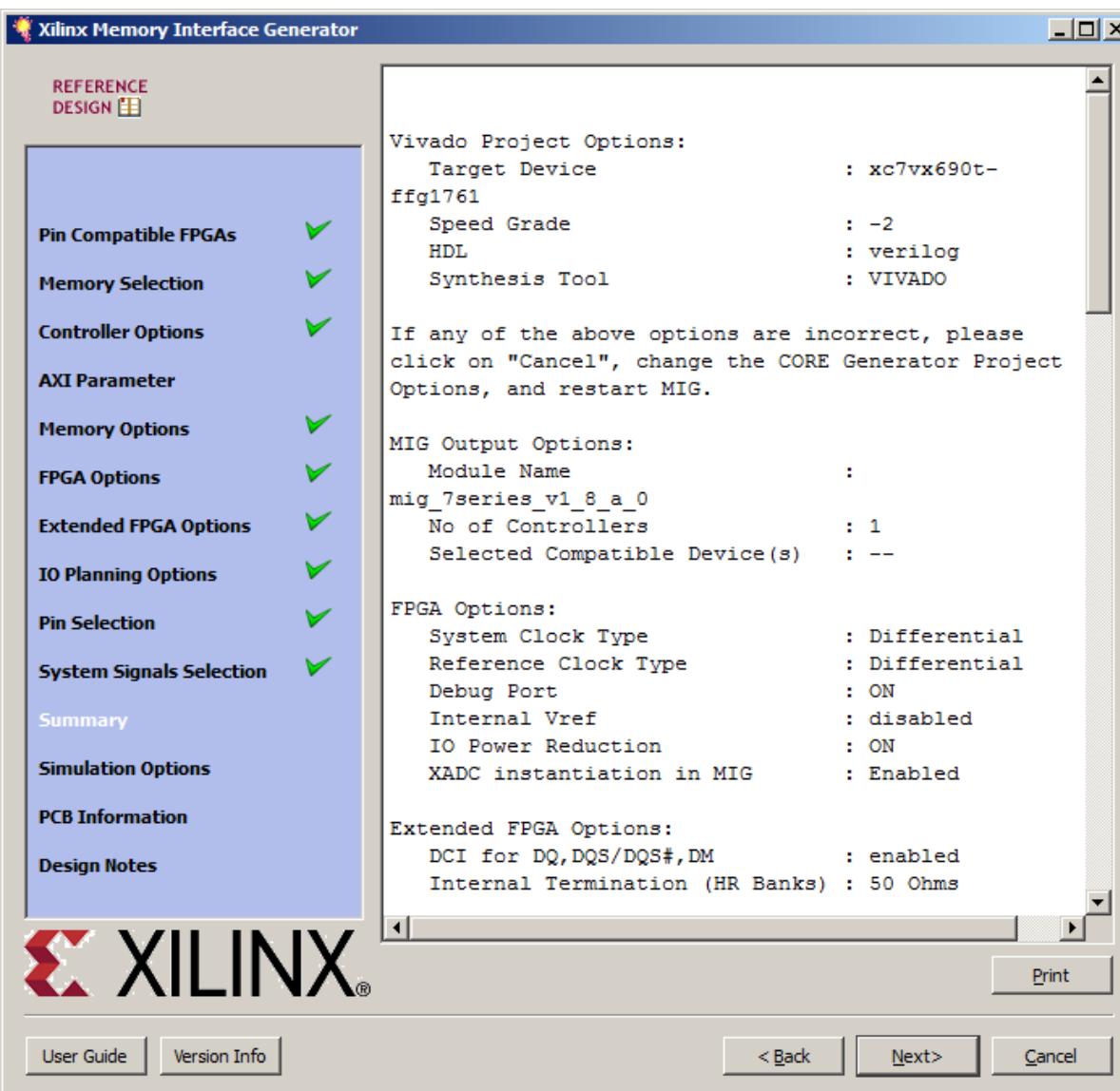
Generate MIG Bank A Example Design



➤ Make the following settings:

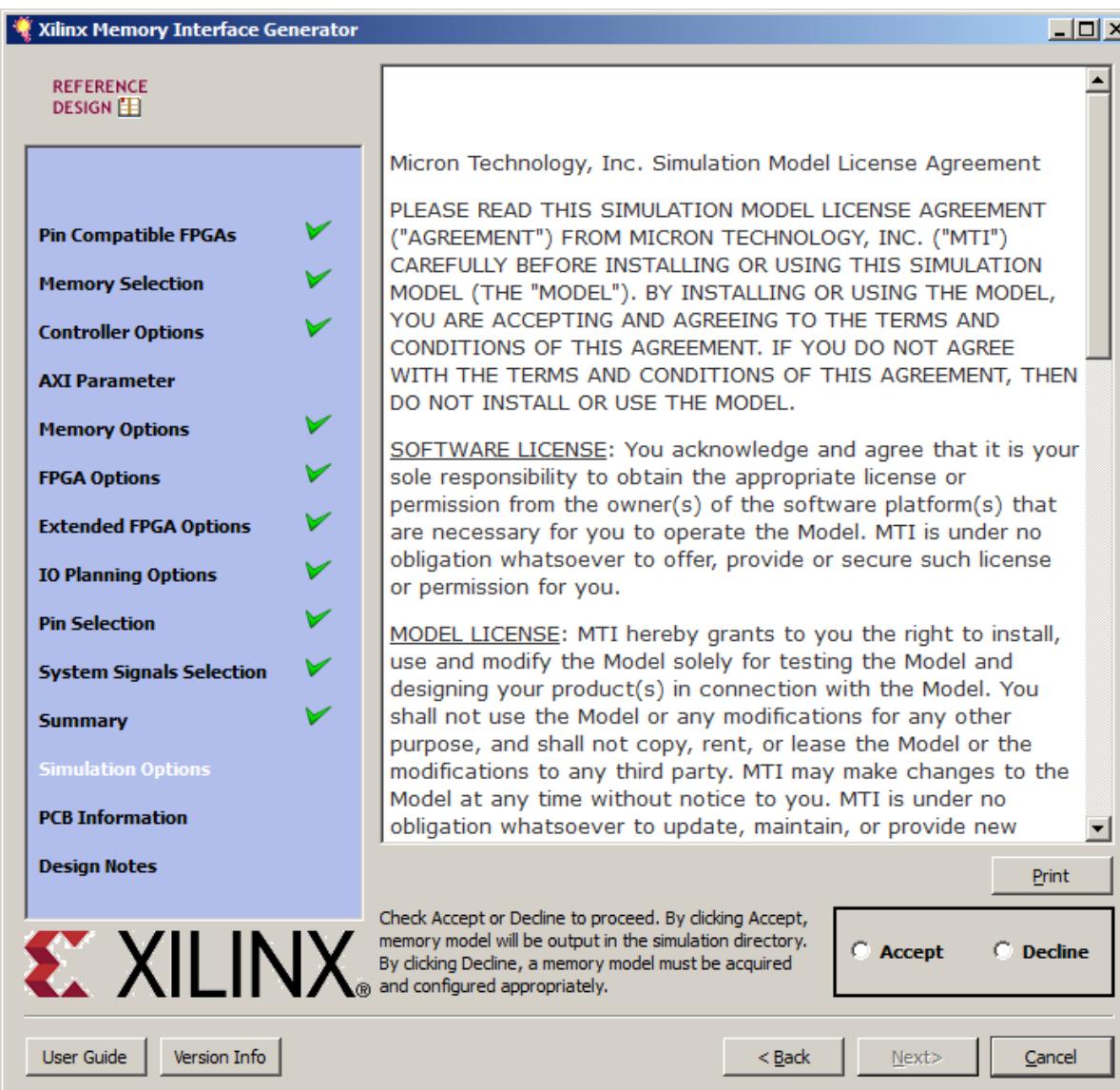
- Set sys_rst to Bank: 15
- Pin Number:
AV40(MRCC_P)
- Click Next

Generate MIG Bank A Example Design



► Leave this page as is
– Click Next

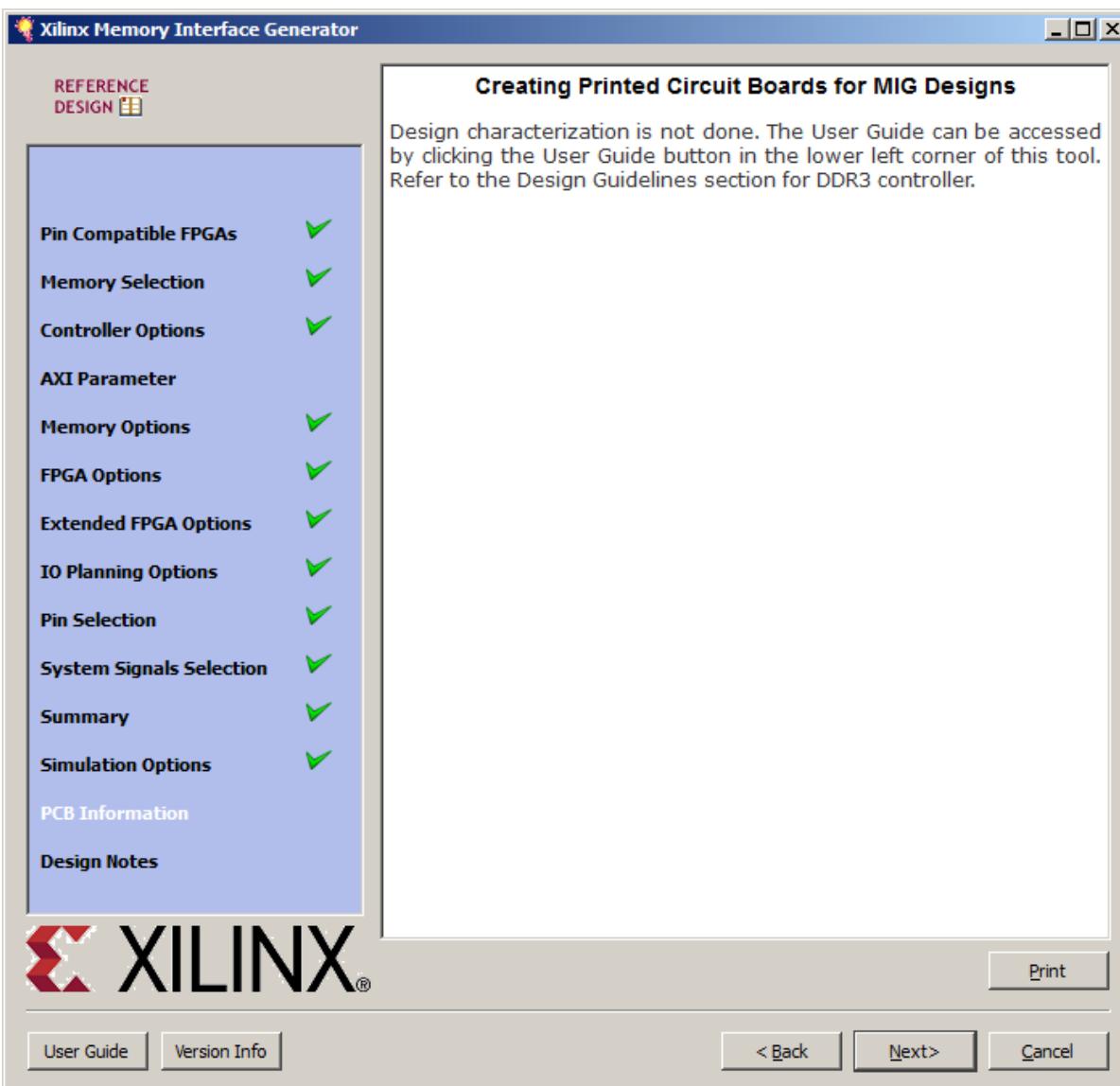
Generate MIG Bank A Example Design



➤ Accept Simulation license, if desired

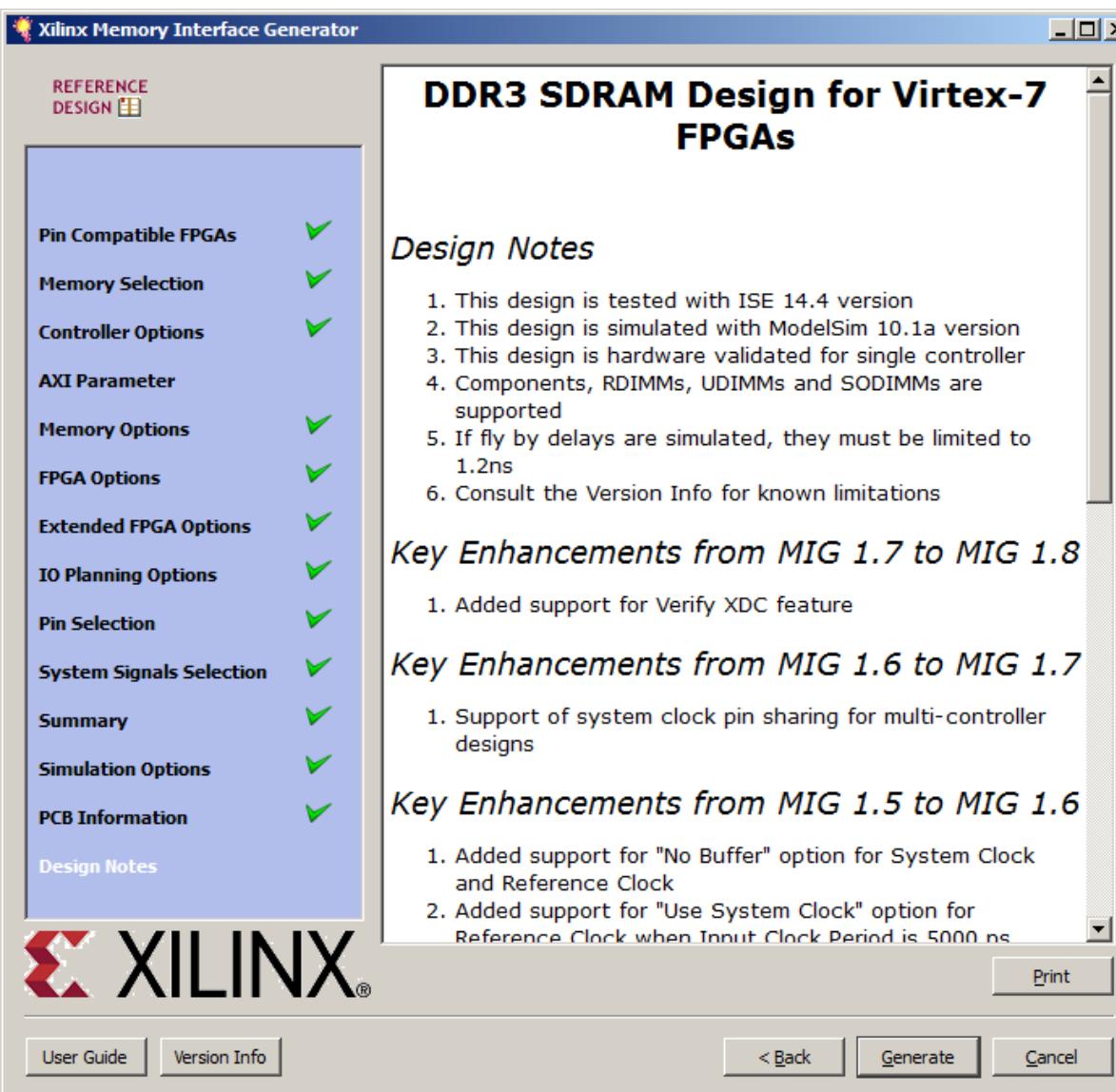
- Otherwise, Decline license
- Click Next

Generate MIG Bank A Example Design



➤ Leave this page as is
– Click Next

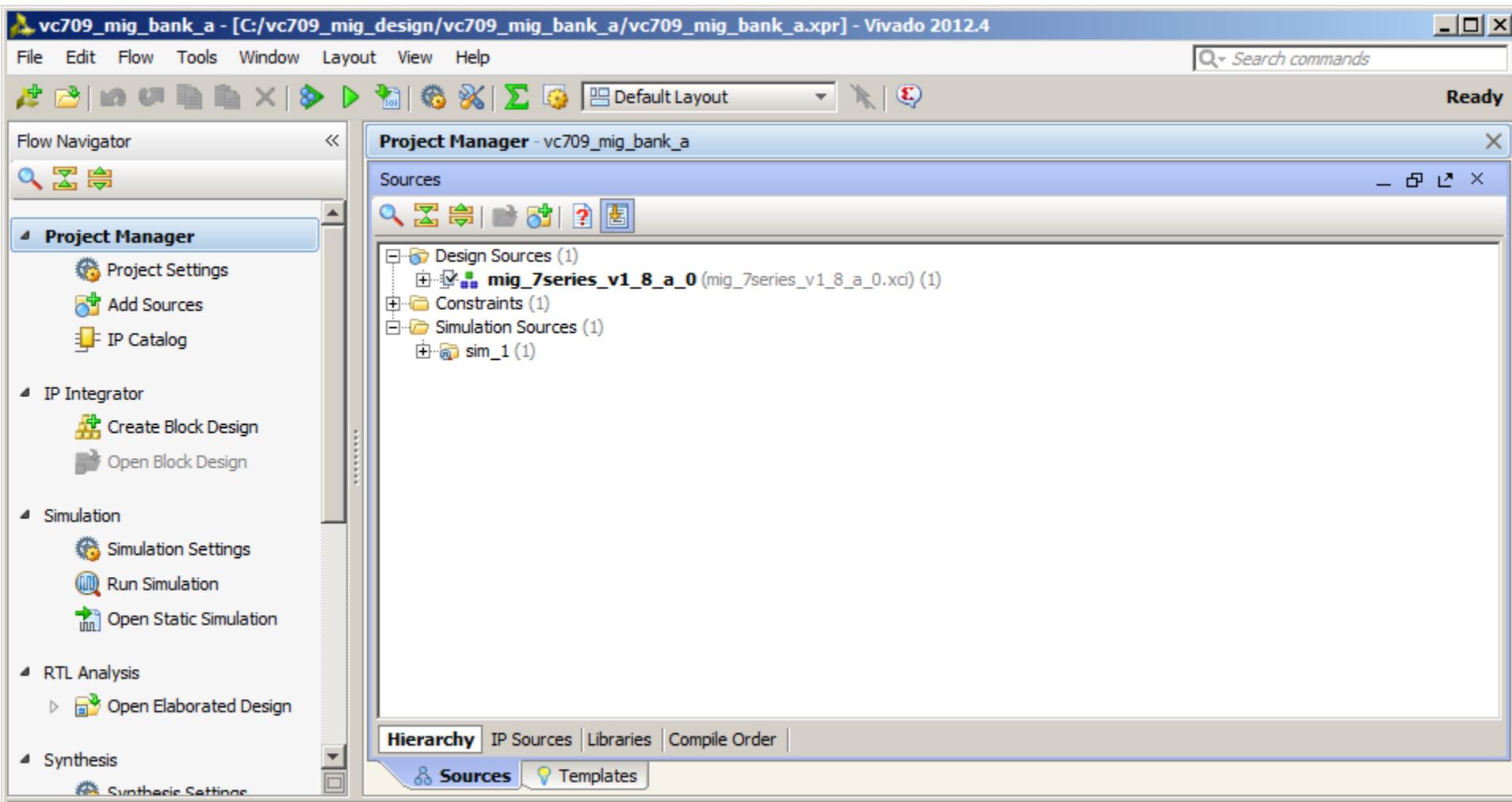
Generate MIG Bank A Example Design



► Click Generate

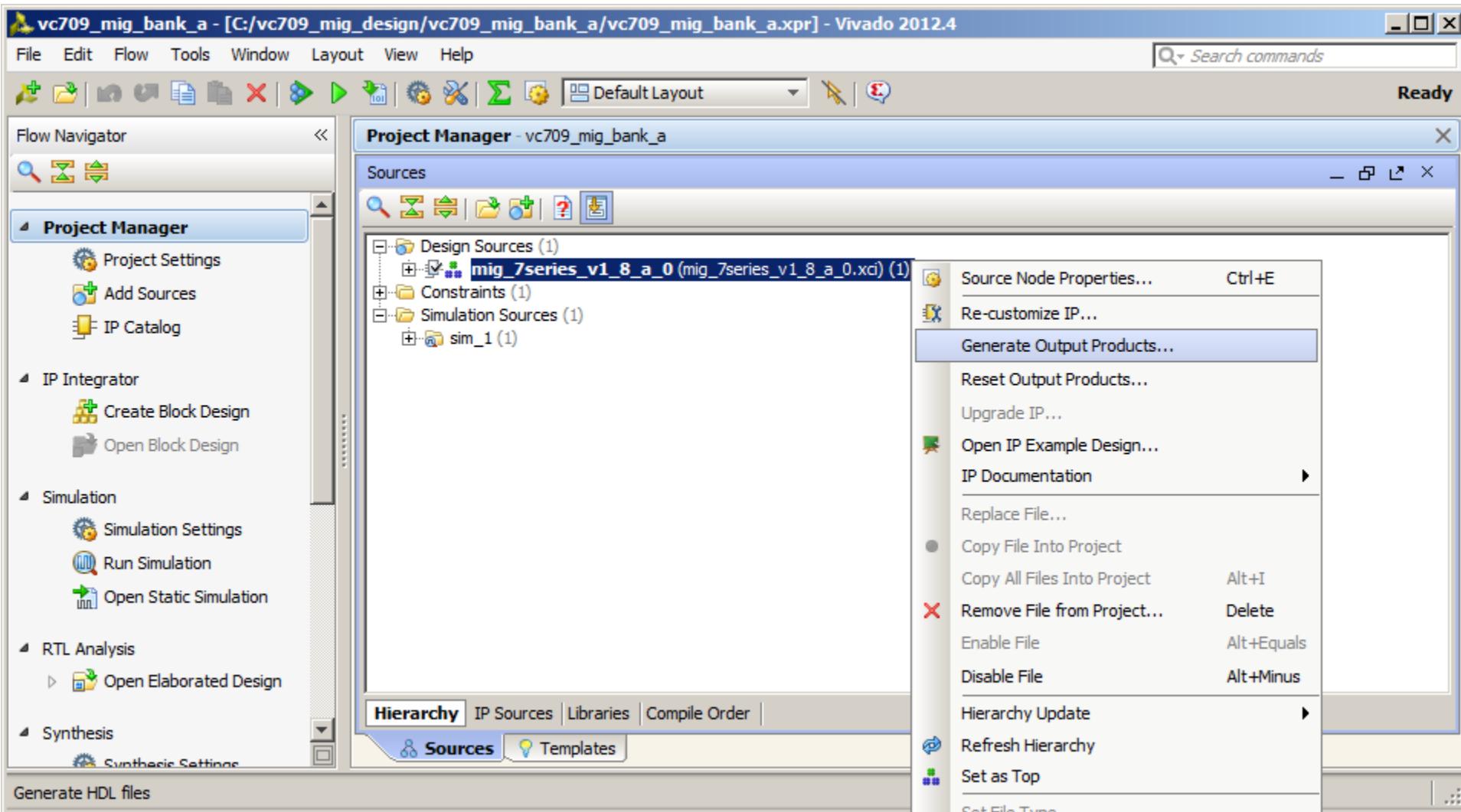
Generate MIG Bank A Example Design

- MIG design appears in Design Sources



Compile MIG Bank A Example Design

- Right-click on mig_7series_v1_8_a_0 and select Generate Output Products...

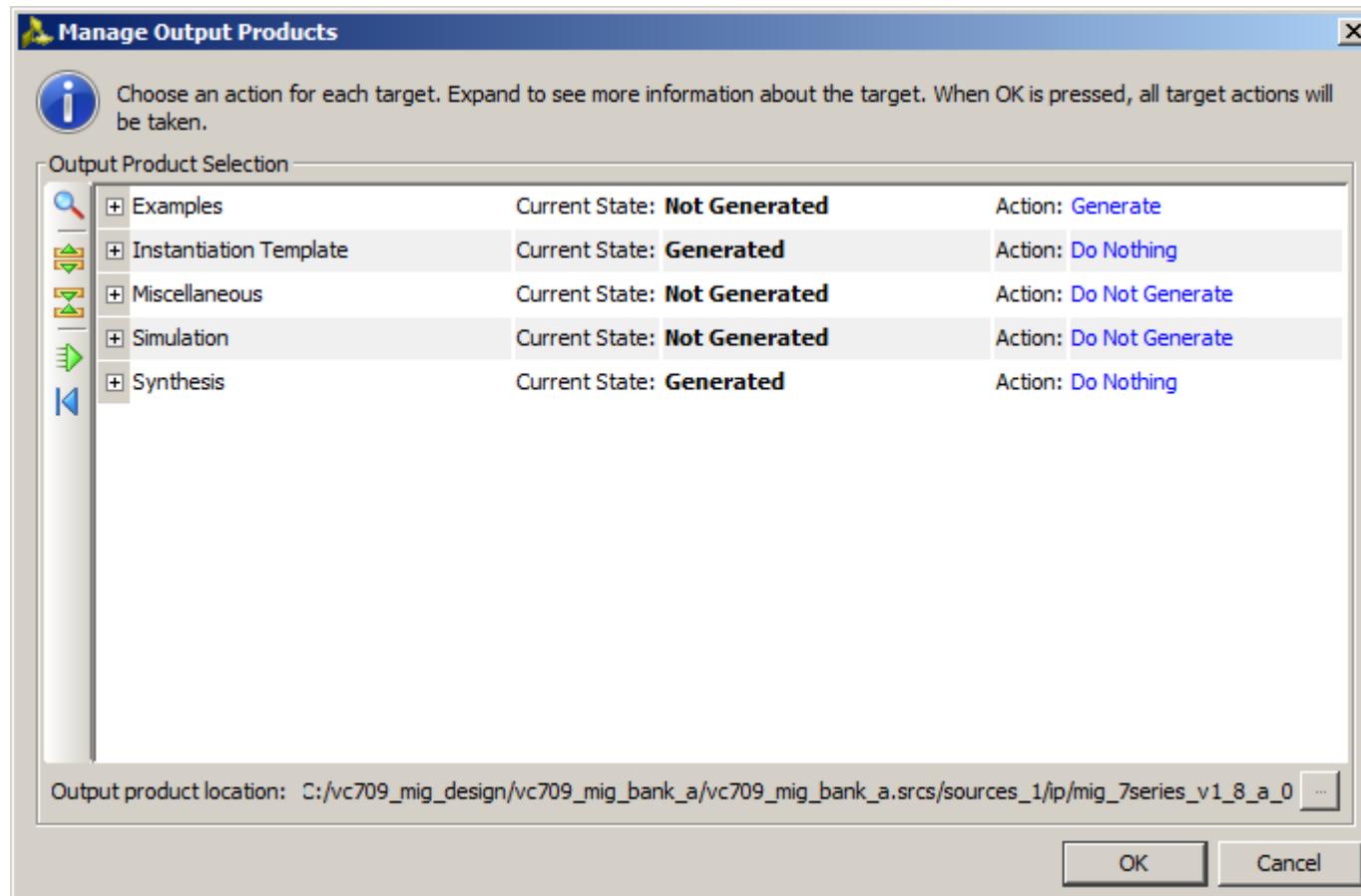


Note: Presentation applies to the VC709

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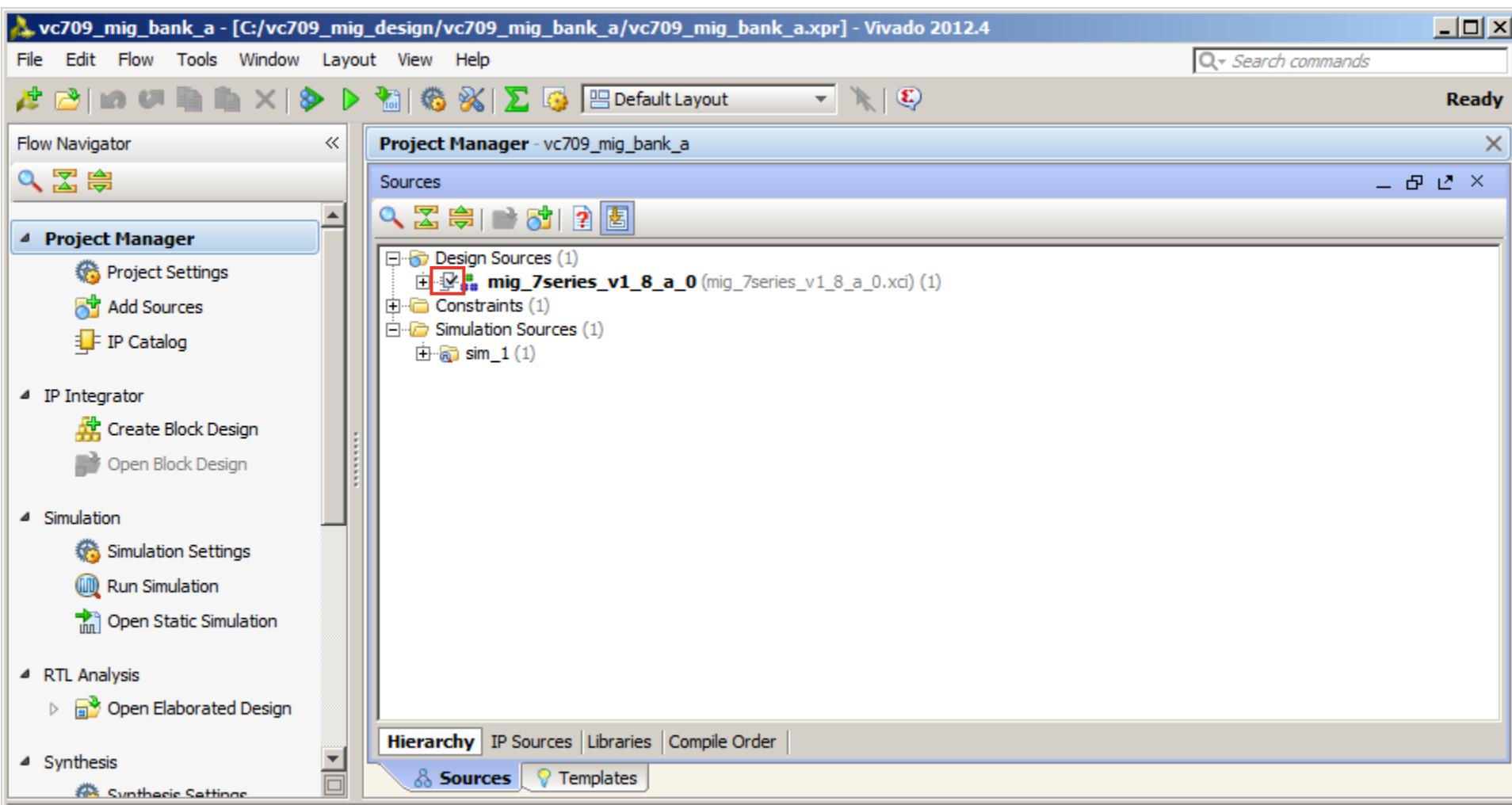
Compile MIG Bank A Example Design

- Select Examples as the target to generate



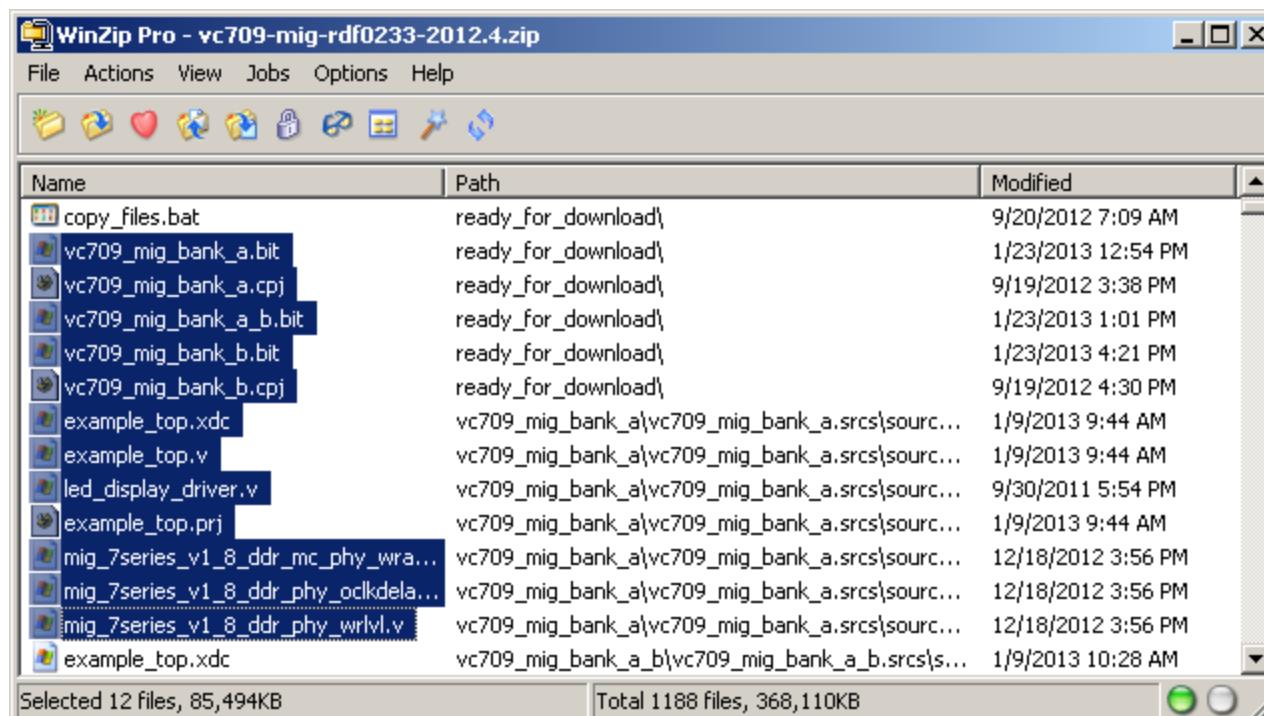
Compile MIG Bank A Example Design

► Once the Generate step is complete, a check (re)appears on the IP



Modifications to MIG Bank A Example Design

- ▶ Open the VC709 MIG Design Files (2012.4 CES) and extract these files to your C:\vc709_mig_design directory
 - **ready_for_download*** and **vc709_mig_bank_a***
 - Contains several changes needed to support Virtex-7 devices with MIG, including [AR53420](#)
 - This zip file also contains precompiled versions of these three MIG designs



Modifications to MIG Bank A Example Design

► Modifications to the example design

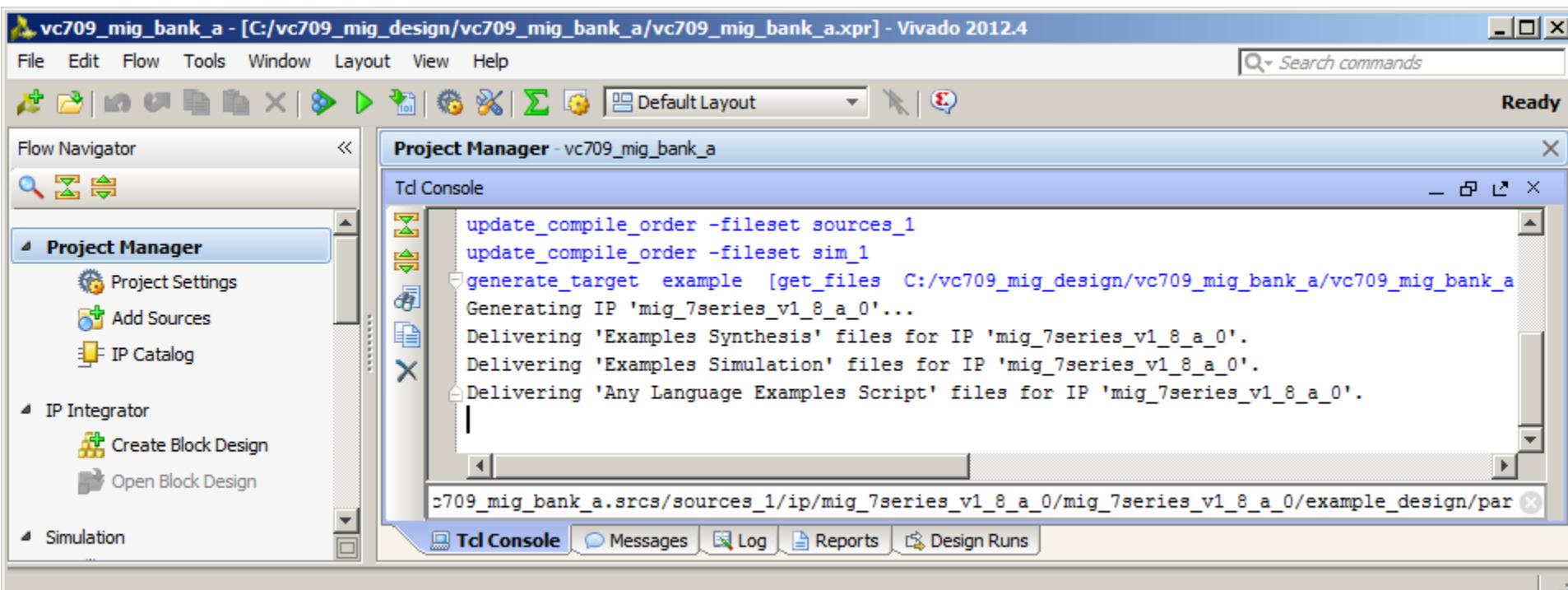
- Added RTL and XDC modifications to drive LEDs
- Changed RST_ACT_LOW to “0”; refer to [UG586](#) for more details on using the RST_ACT_LOW parameter
- Added [AR53420](#) – Required MIG Calibration Patch

Compile MIG Bank A Example Design

► At the Tcl Console enter this command:

```
cd
```

```
C:/vc709_mig_design/vc709_mig_bank_a/vc709_mig_bank_a.srcs/sources_1/ip/mig_7series_v1_8_a_0/mig_7series_v1_8_a_0/example_design/par
```

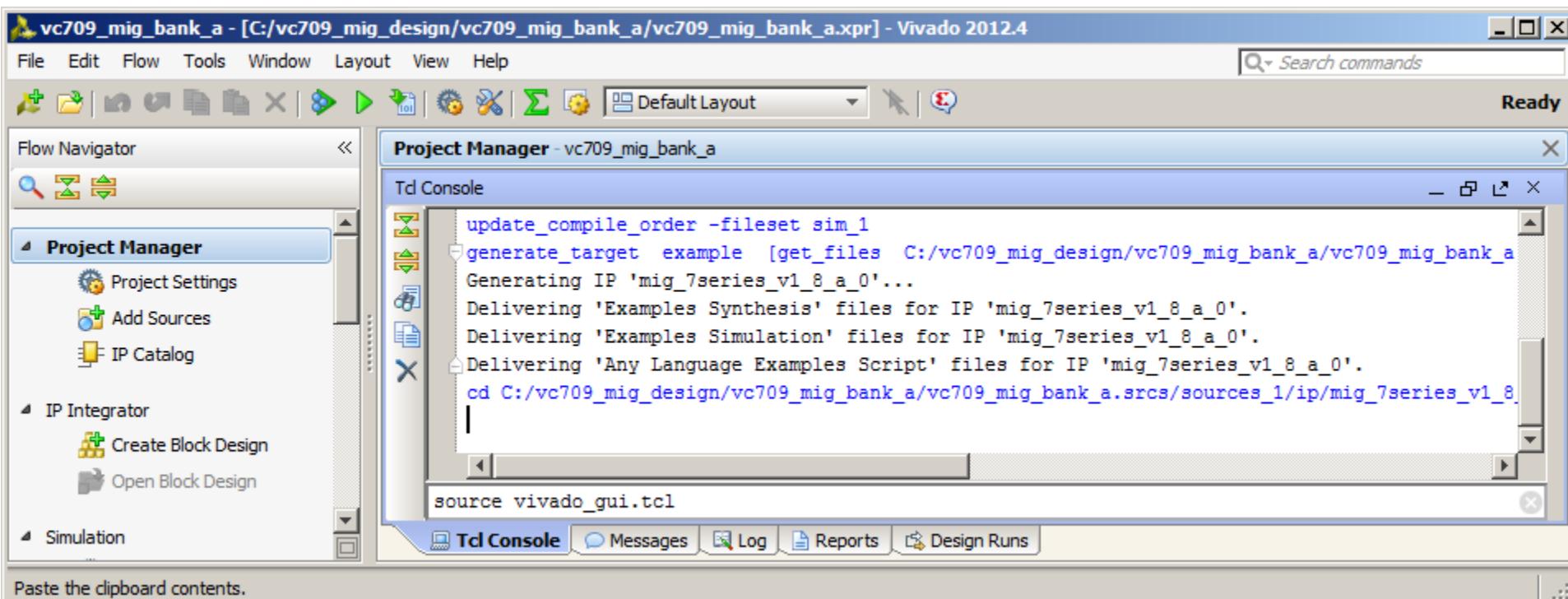


Compile MIG Bank A Example Design

► At the Tcl Console enter this command:

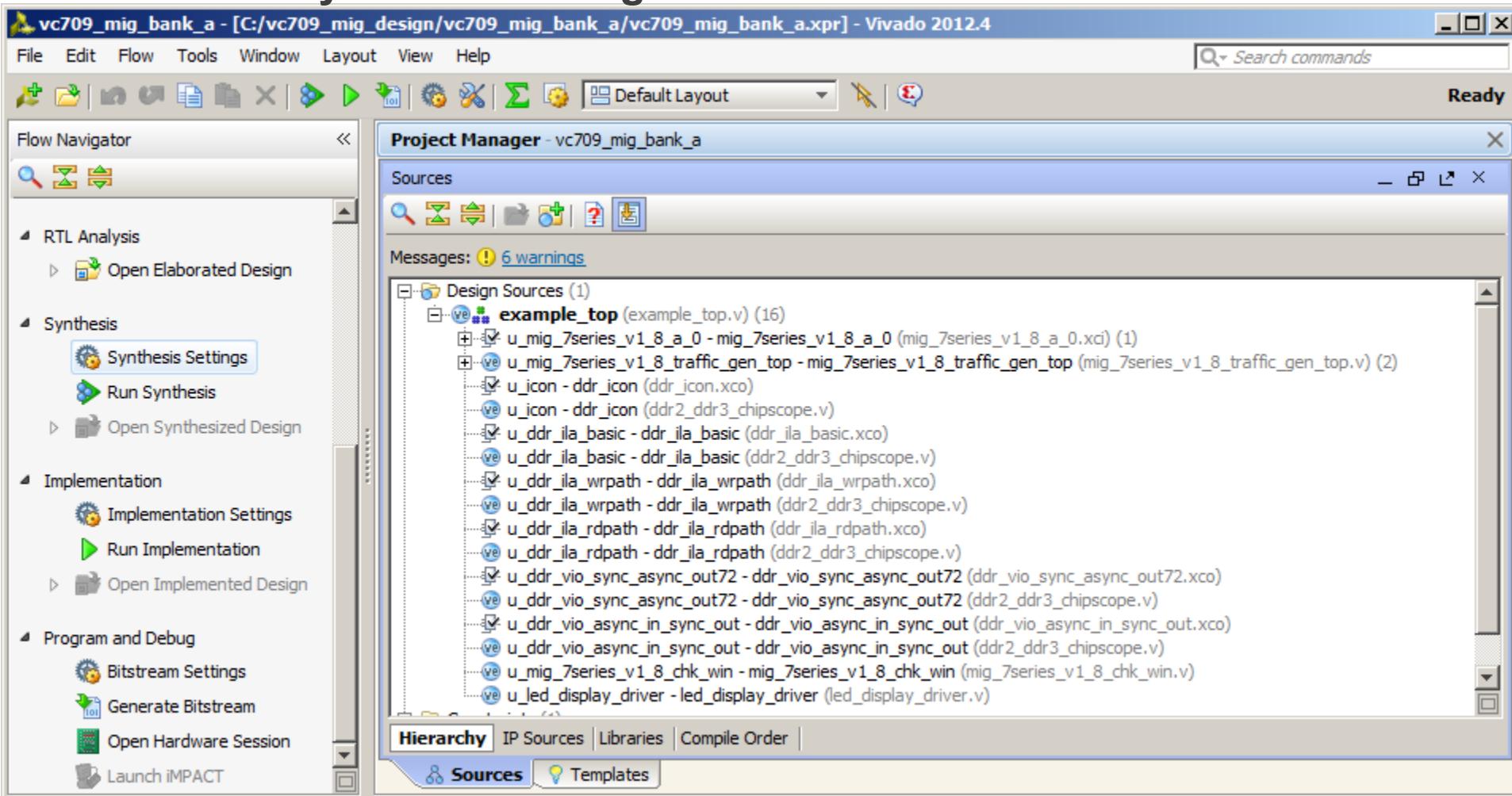
```
source vivado_gui.tcl
```

► This command adds the necessary design files and compiles the ChipScope IP



Compile MIG Bank A Example Design

- The design files, IP and constraints have been added/generated
- Click on Synthesis Settings



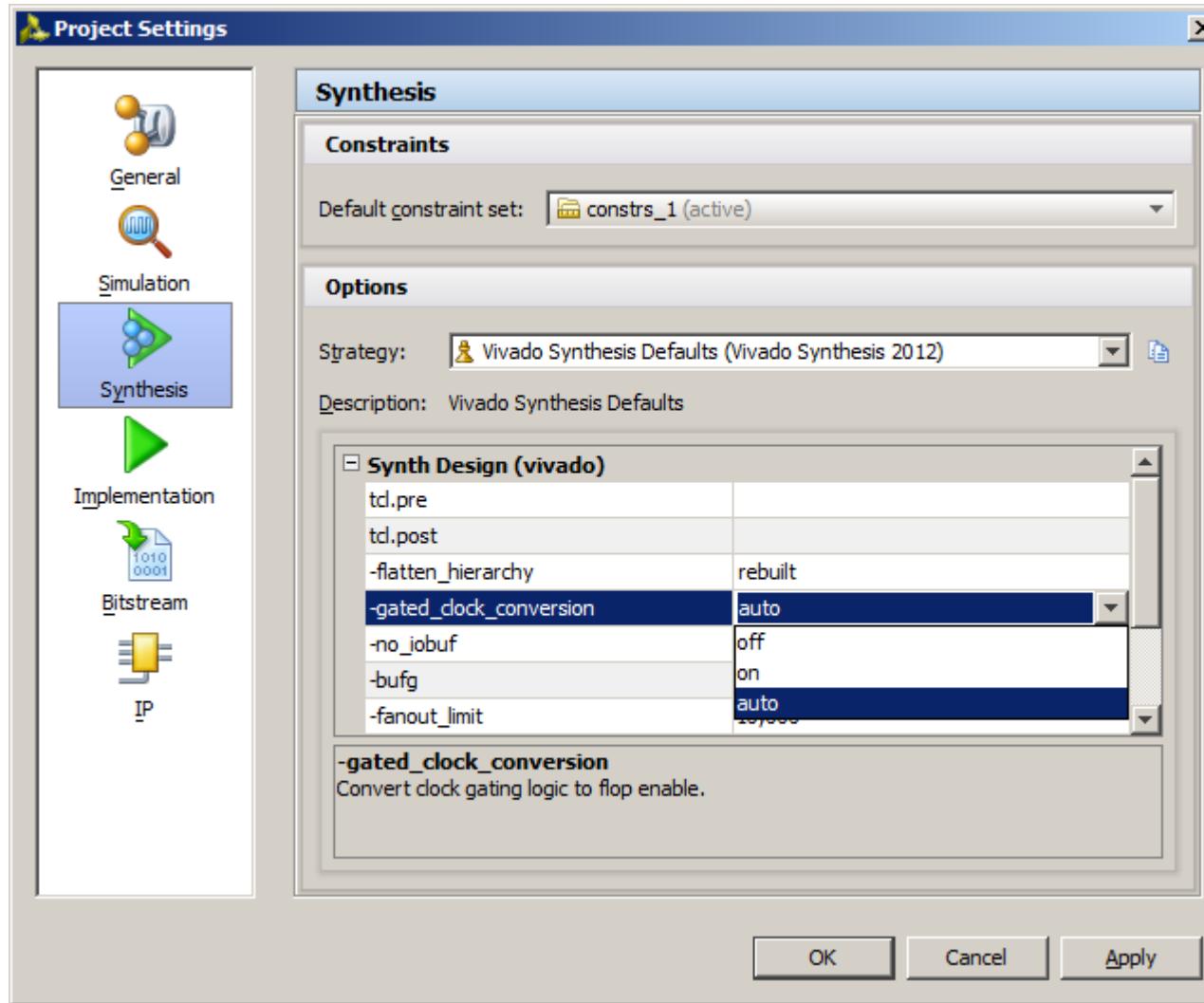
Open synthesis settings to change options.

Note: Presentation applies to the VC709

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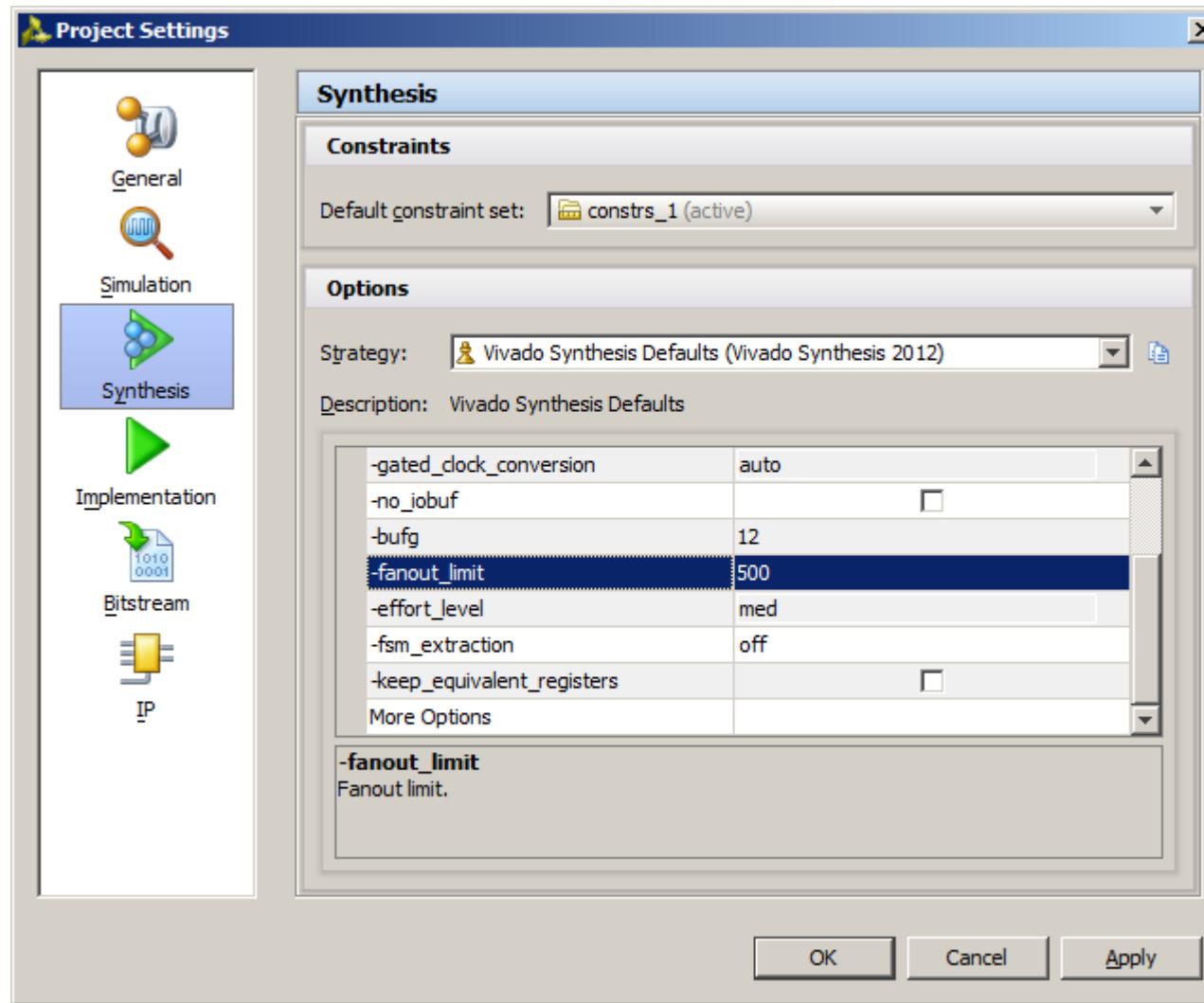
Compile MIG Bank A Example Design

- Set the `gated_clock_conversion` to auto



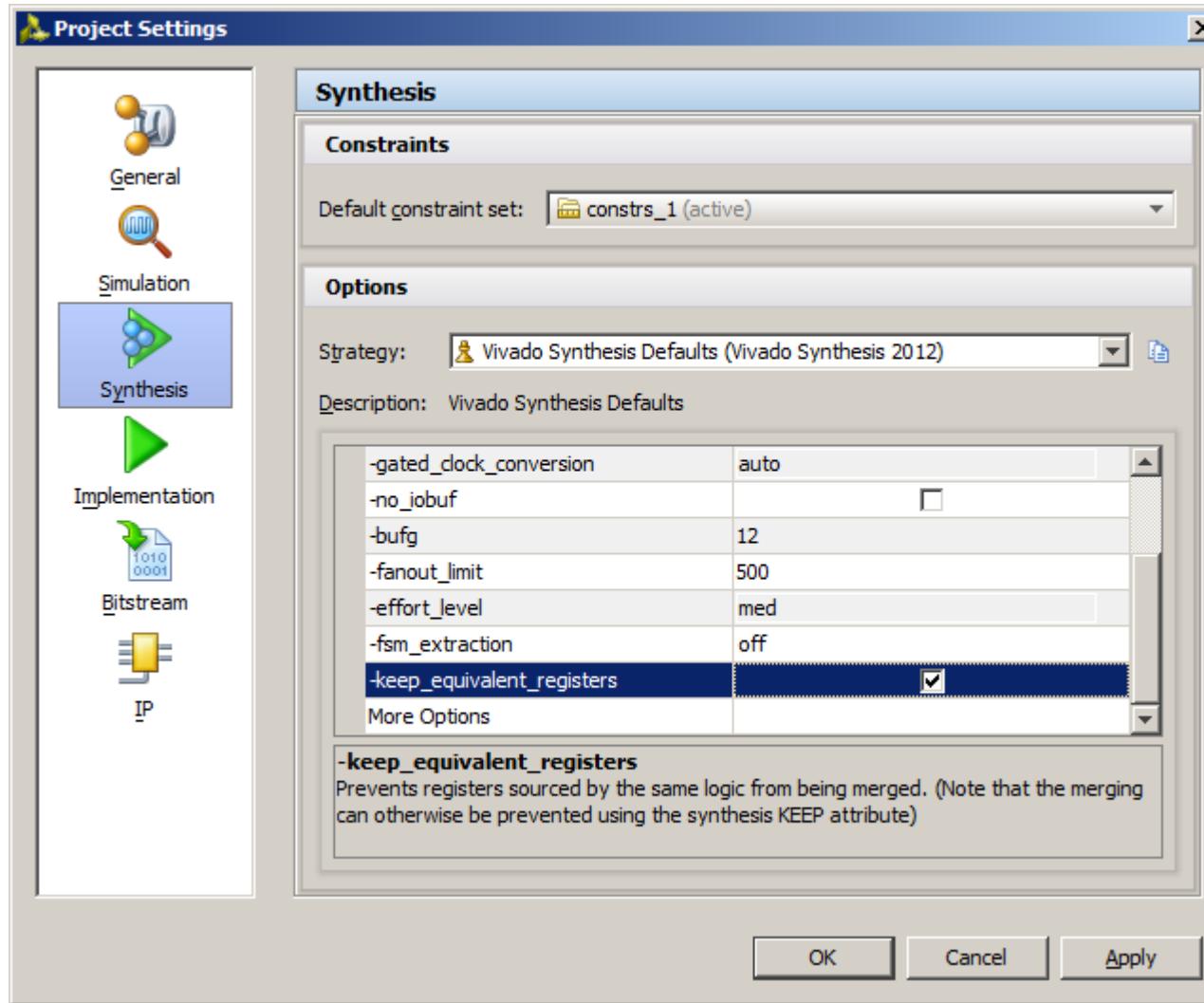
Compile MIG Bank A Example Design

- Set the fanout_limit to 500



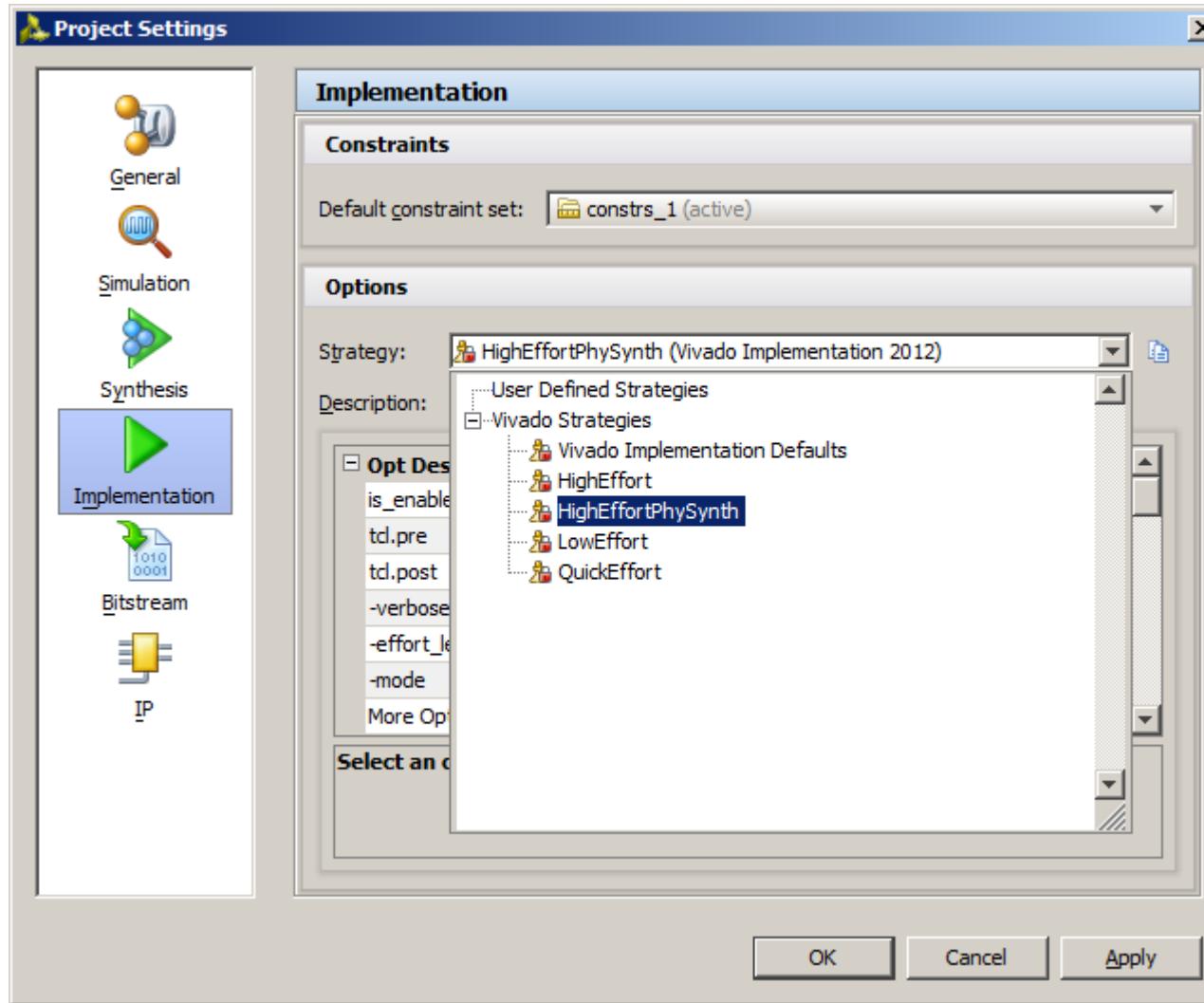
Compile MIG Bank A Example Design

- Check the `keep_equivalent_registers` option



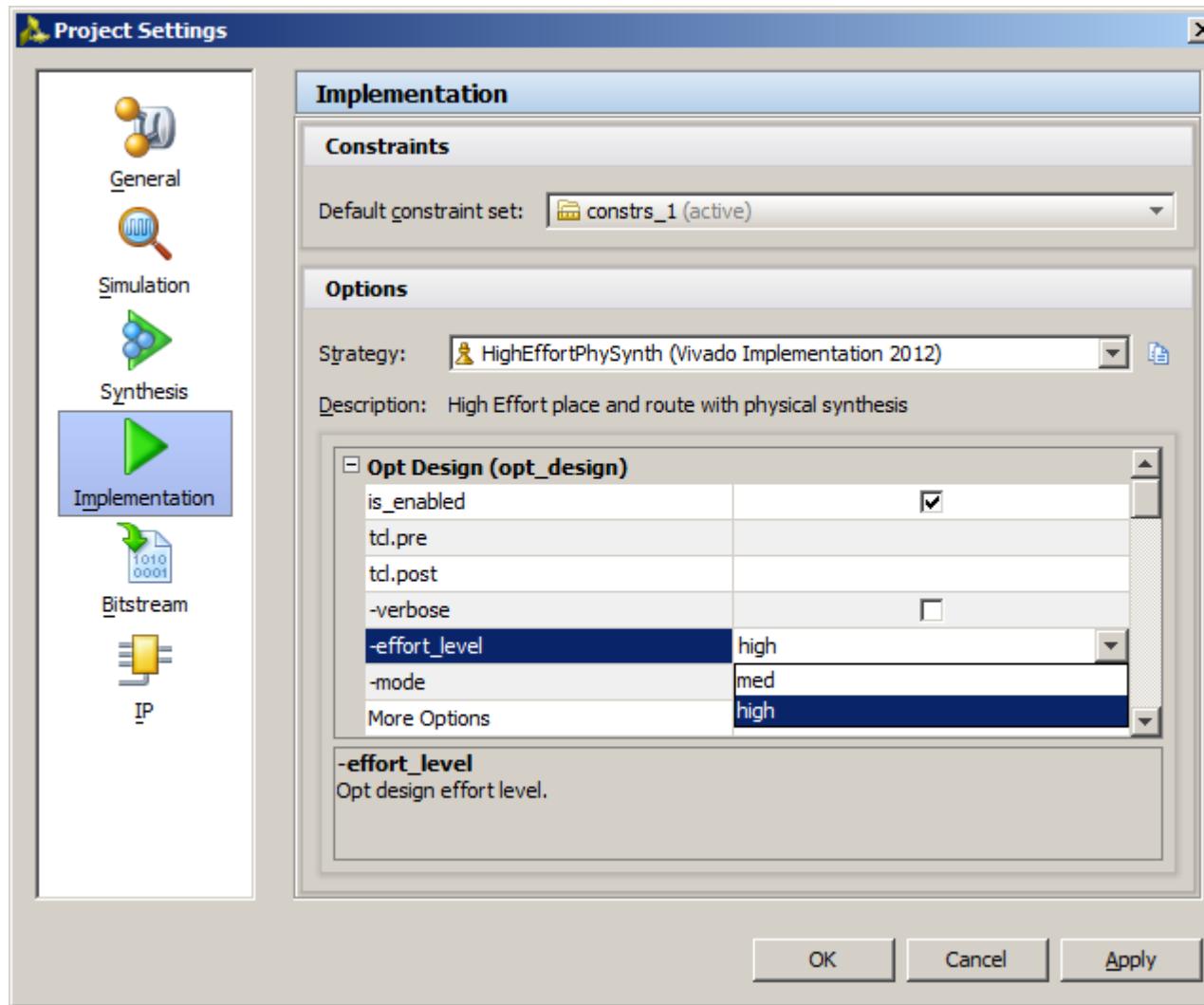
Compile MIG Bank A Example Design

► Select Implementation and select HighEffortPhySynth



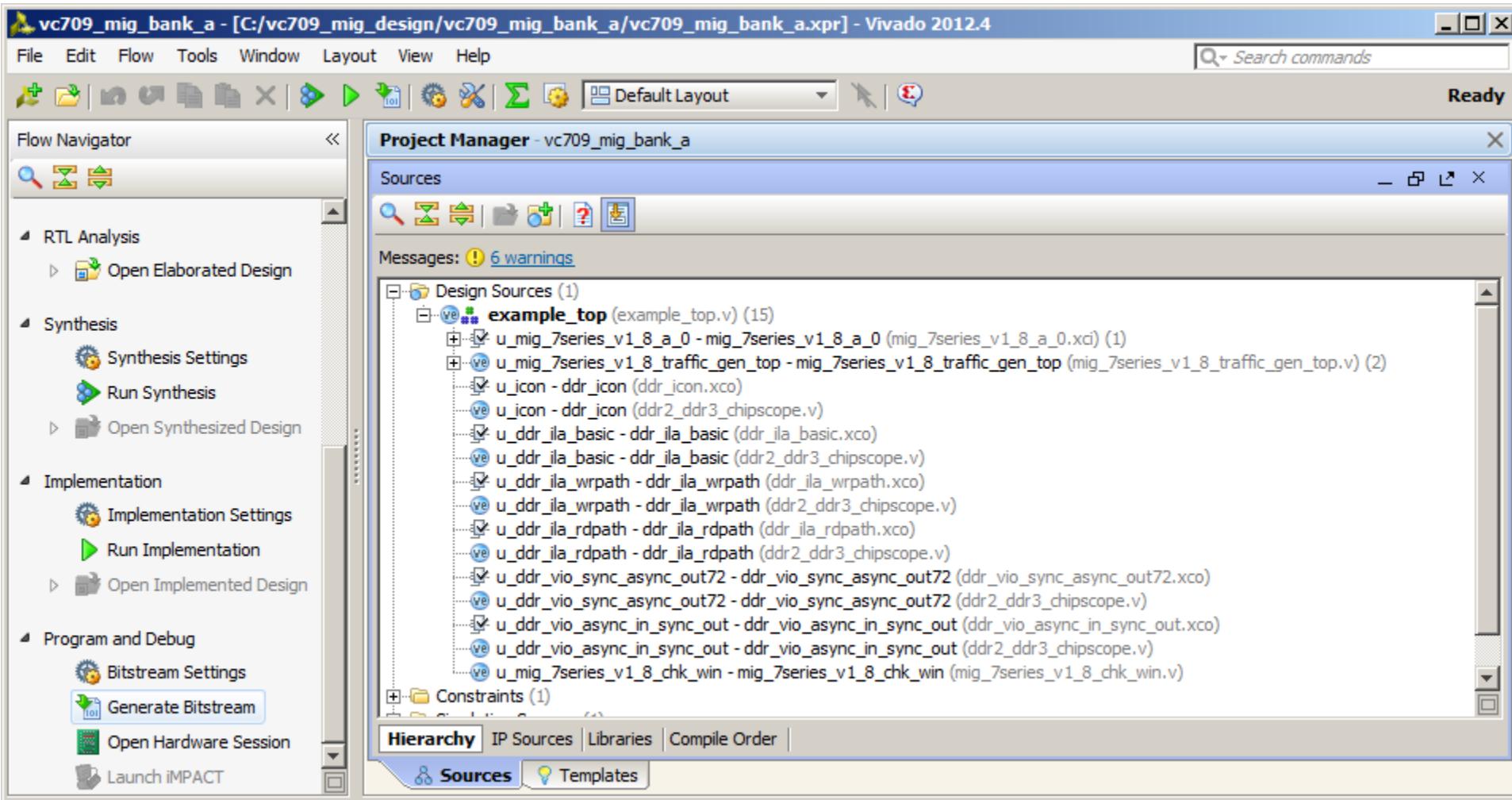
Compile MIG Bank A Example Design

- Under Opt Design set effort_level to high



Compile MIG Bank A Example Design

► Click on Generate Bitstream



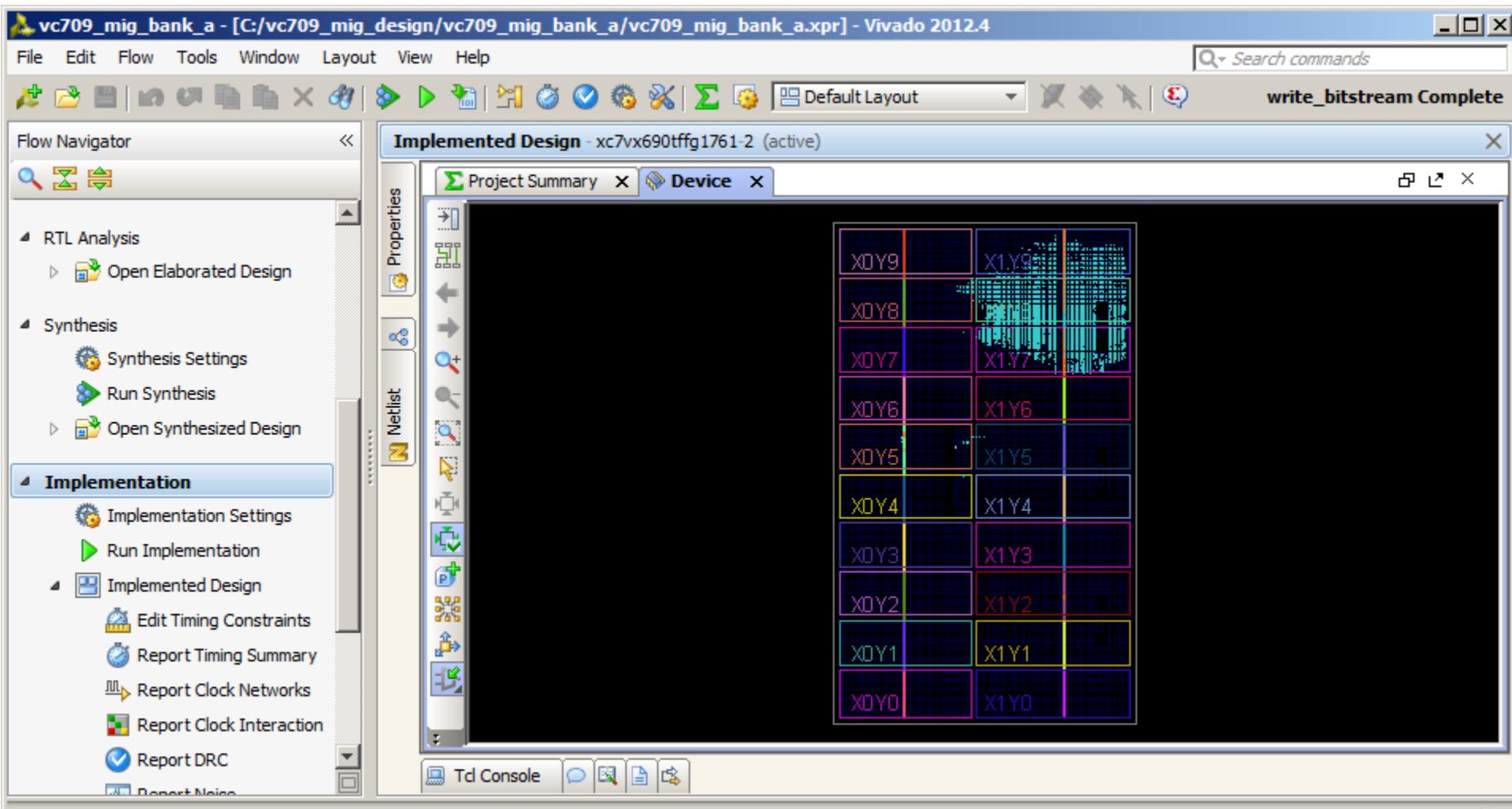
Generate a programming file after implementation.

Note: Presentation applies to the VC709

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Compile MIG Bank A Example Design

► Open and view the implemented design



Hardware Setup

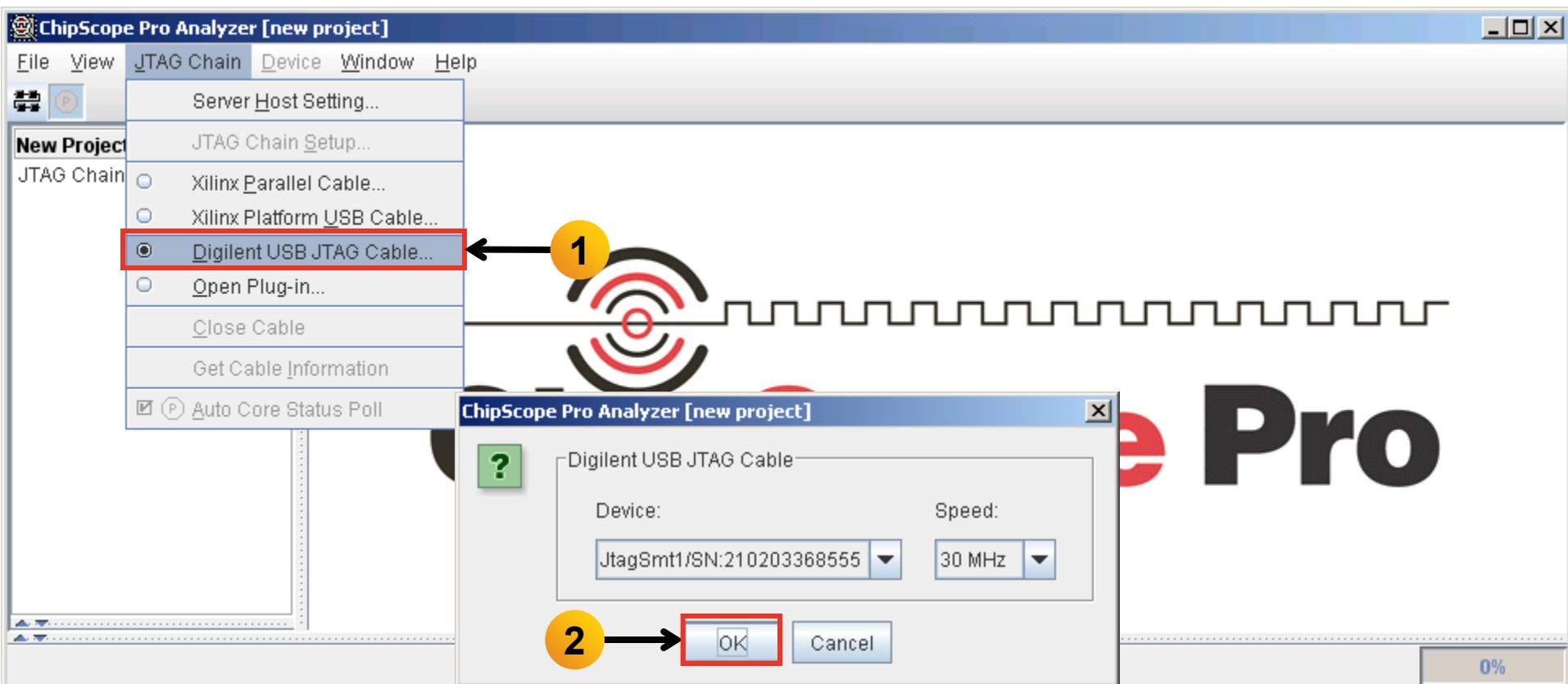
► Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the VC709 board

- Connect this cable to your PC
- Power on the VC709 board



Run MIG Bank A Example Design

- Open ChipScope Pro and select JTAG Chain → Digilent USB Cable... (1)
- Verify 30 MHz operation and click OK (2)



Run MIG Bank A Example Design

► Click OK (1)

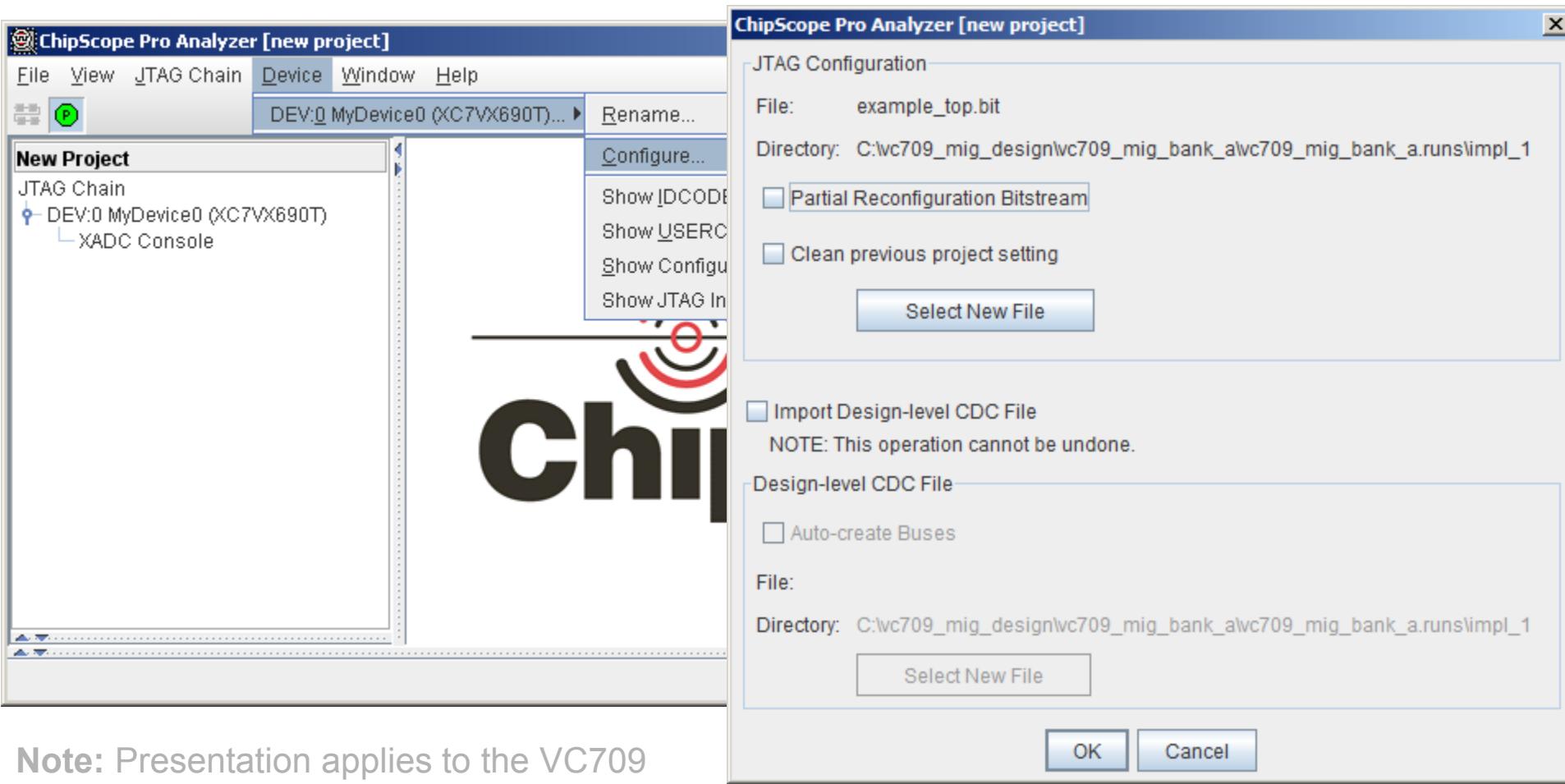


Run MIG Bank A Example Design

► Select Device → DEV:0 MyDevice0 (XC7VX690T) → Configure...

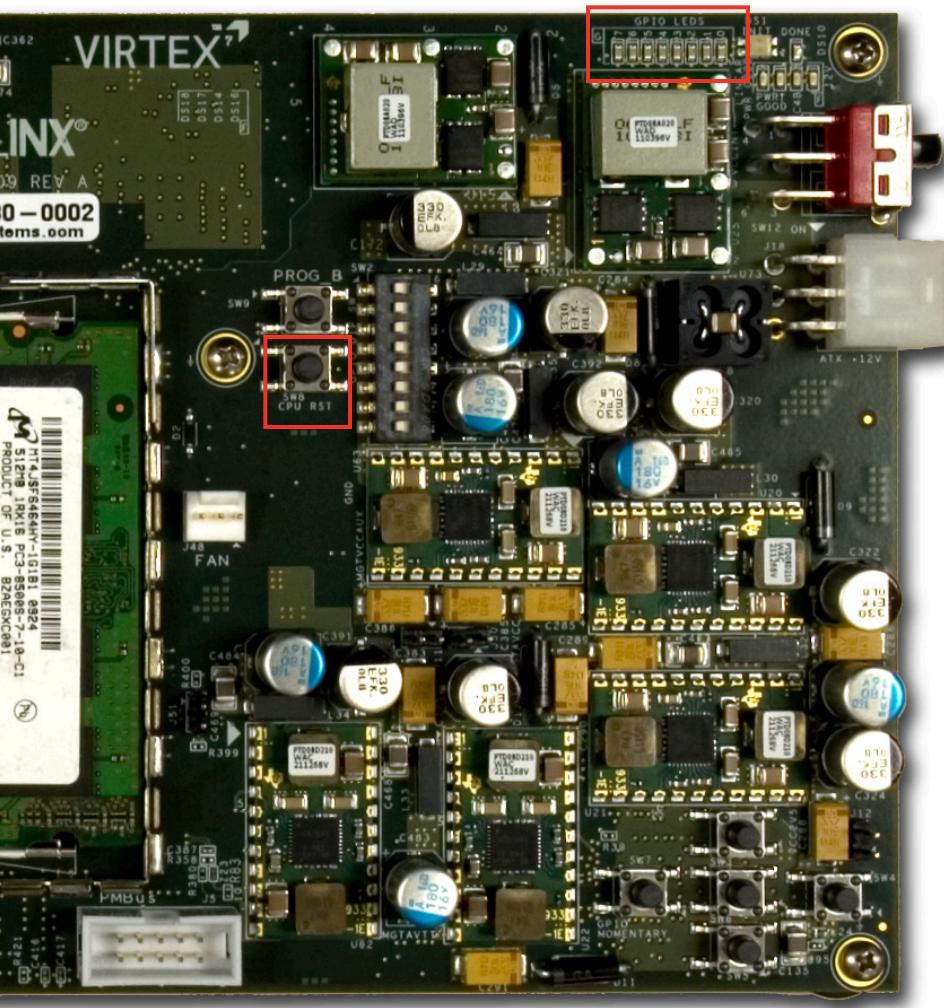
► Select <Design

Path>\vc709_mig_bank_a\vc709_mig_bank_a.runs\impl_1\example_top.bit



Note: Presentation applies to the VC709

Run MIG Bank A Example Design



- After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking
- LED 3 will light and stay on
 - This indicates Calibration has completed
- If an error occurs, LED 0 will go out and LED 2 will light
 - SW8 is the reset

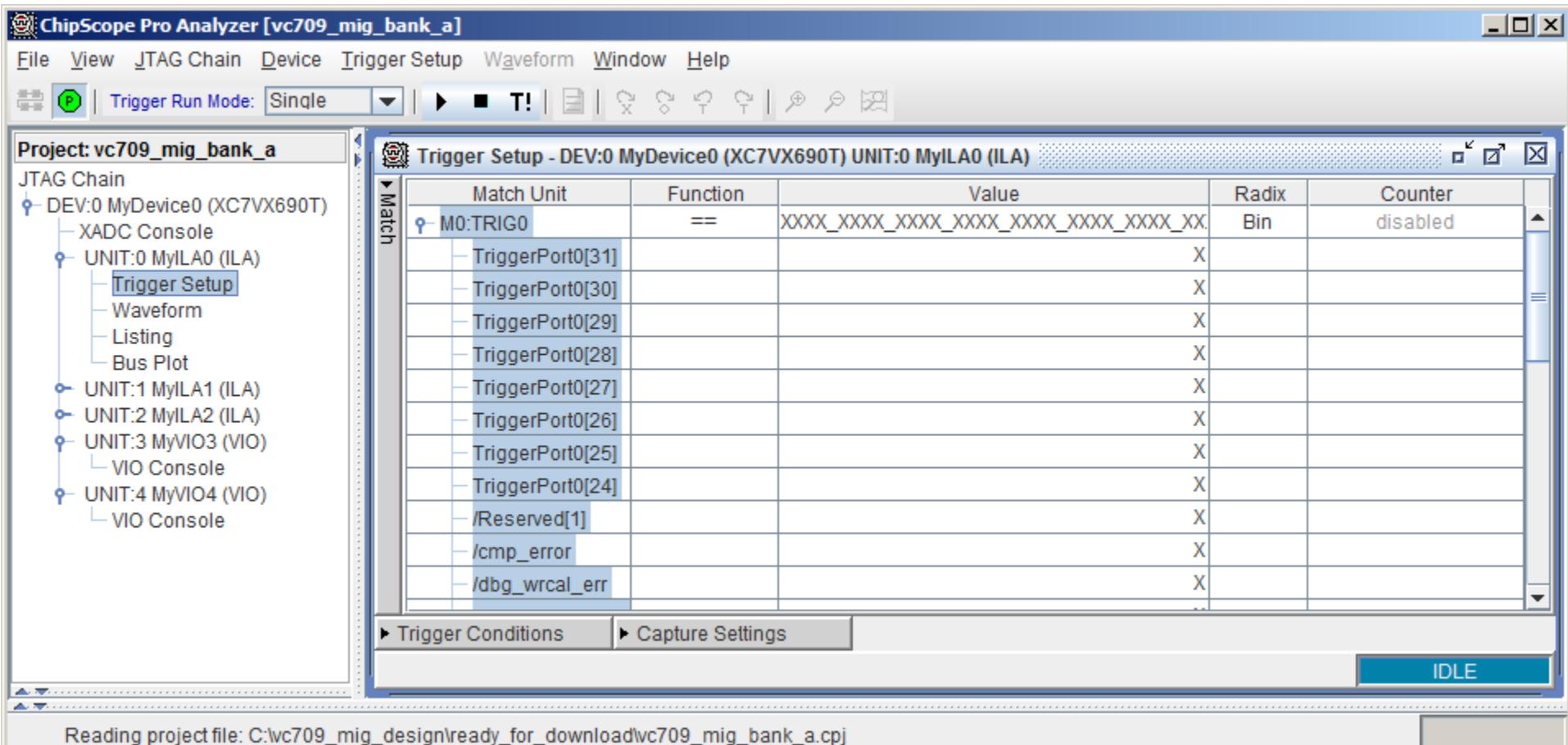
Run MIG Bank A Example Design

- Select File → Open Project...
- Select <Design Path>\ready_for_download\vc709_mig_bank_a.cpj



Run MIG Bank A Example Design

► Click on Trigger Setup to view trigger settings

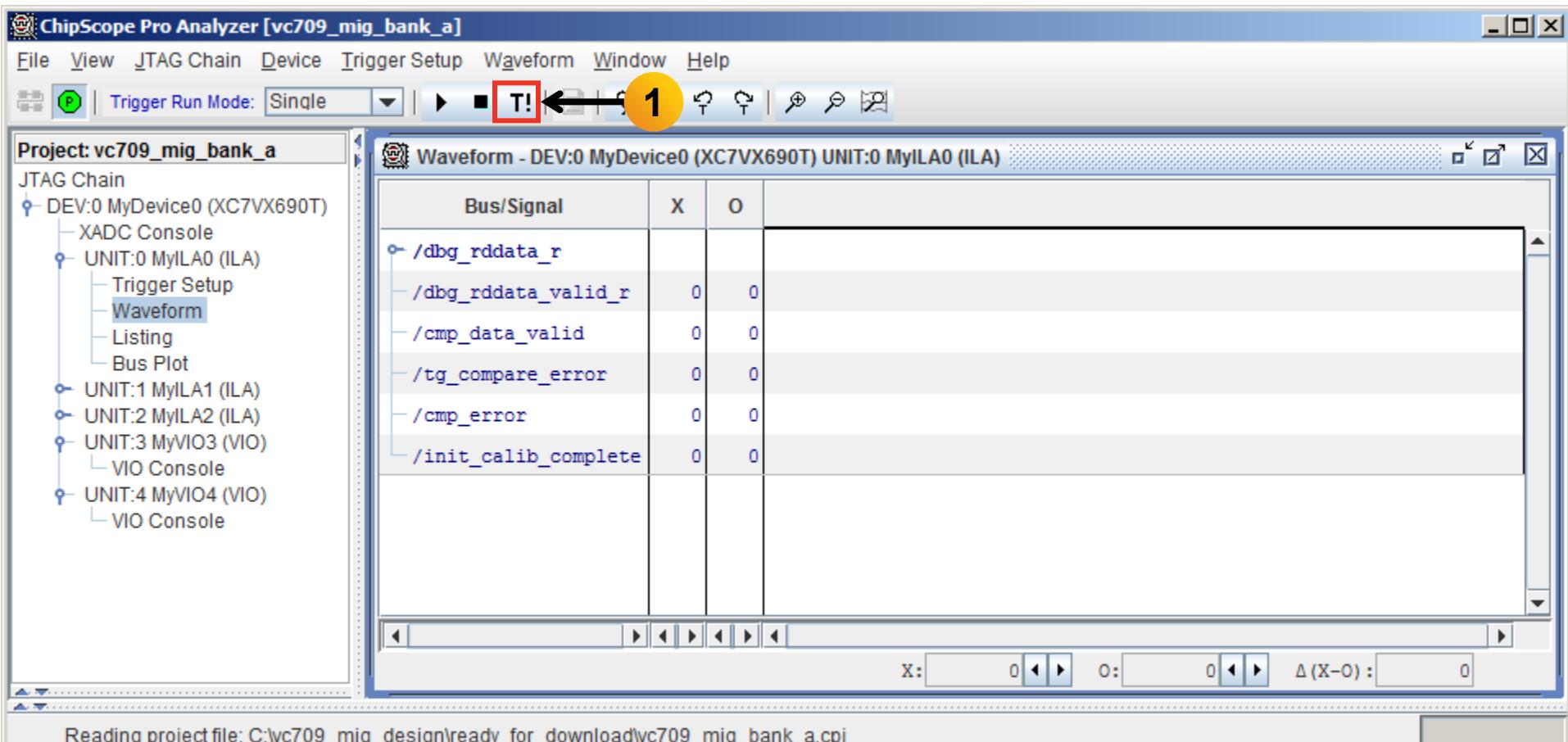


Match Unit	Function	Value	Radix	Counter
M0:TRIG0	==	XXXX_XXXX_XXXX_XXXX_XXXX_XXXX_XXXX_XX	Bin	disabled
TriggerPort0[31]			X	
TriggerPort0[30]			X	
TriggerPort0[29]			X	
TriggerPort0[28]			X	
TriggerPort0[27]			X	
TriggerPort0[26]			X	
TriggerPort0[25]			X	
TriggerPort0[24]			X	
/Reserved[1]			X	
/cmp_error			X	
/dbg_wrcal_err			X	

Reading project file: C:\vc709_mig_design\ready_for_download\vc709_mig_bank_a.cpj

Run MIG Bank A Example Design

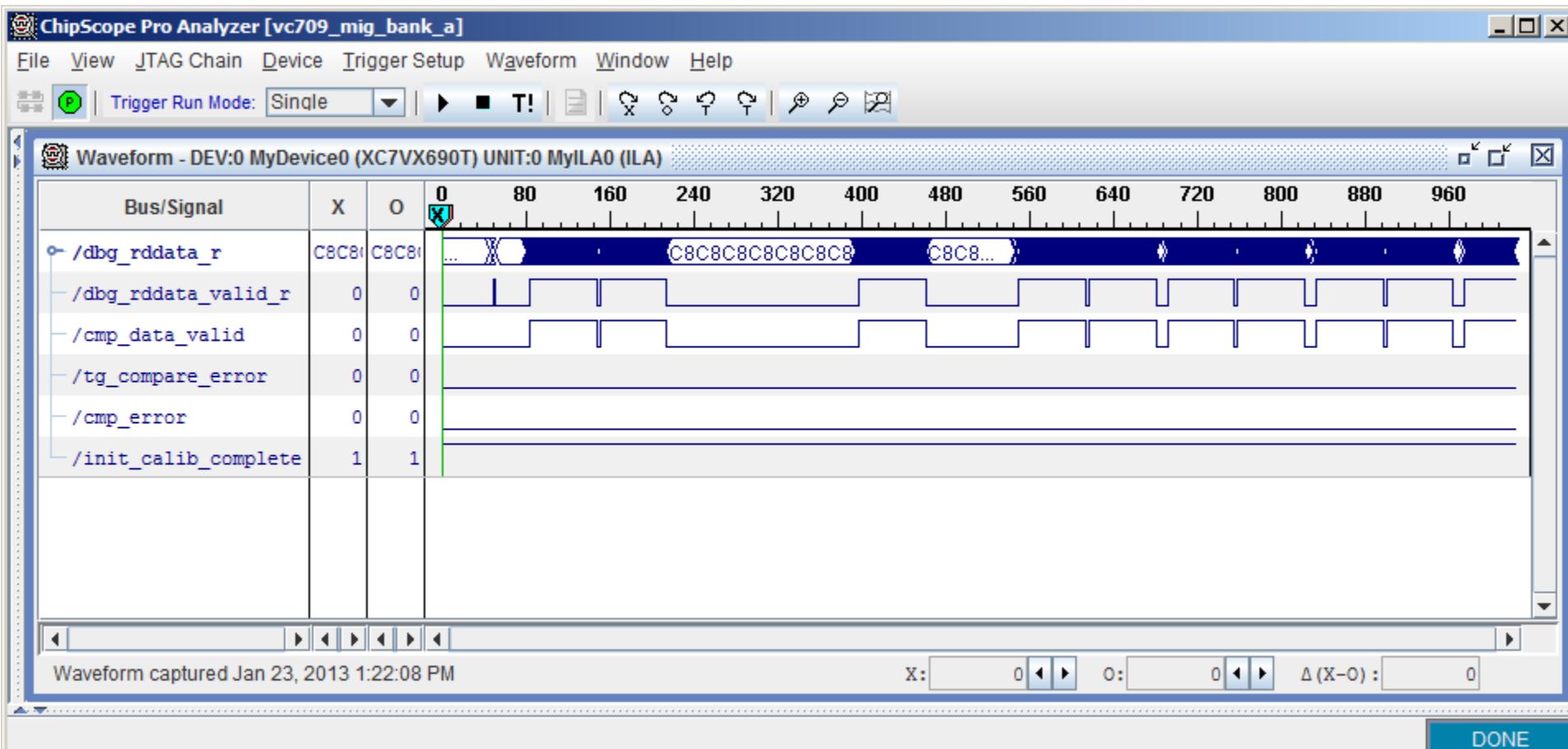
► Click on Waveform; click the Trigger Immediate button (1)



Reading project file: C:\vc709_mig_design\ready_for_download\vc709_mig_bank_a.cpj

Run MIG Bank A Example Design

- View waveforms
 - Data is valid when `dbg_rddata_valid` is high

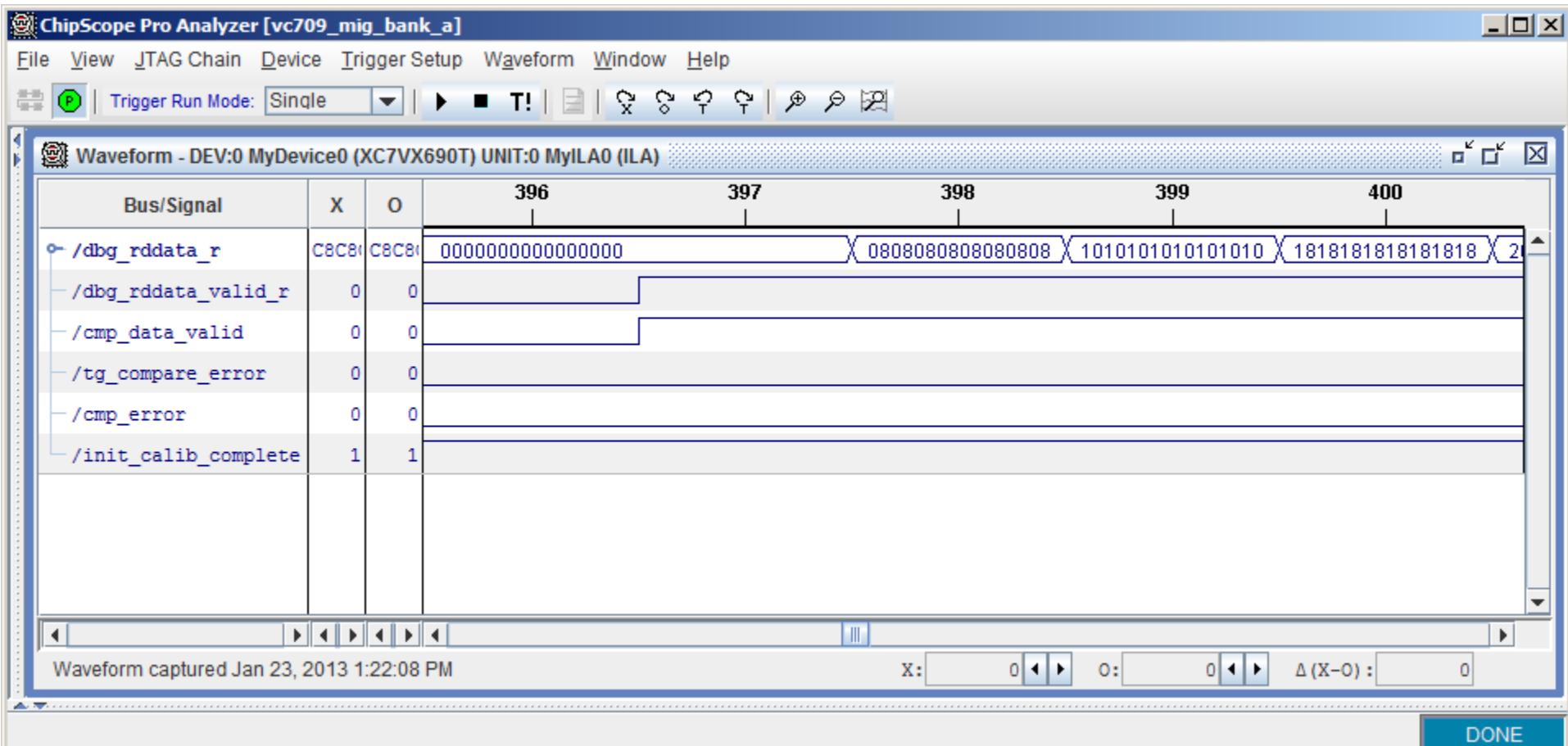


Note: Presentation applies to the VC709

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Run MIG Bank A Example Design

► Zoom in to view data



Adjust Data Pattern using VIO Console

- Select VIO Console 3
- Set `vio_modify_enable` to 1

The screenshot shows the ChipScope Pro Analyzer interface with the project "vc709_mig_bank_a" open. The left sidebar displays the JTAG Chain structure, including DEV:0 MyDevice0 (XC7VX690T), XADC Console, and several MyILA and MyVIO units. The "UNIT:3 MyVIO3 (VIO)" node is expanded, and its "VIO Console" sub-node is selected. The main window is titled "VIO Console - DEV:0 MyDevice0 (XC7VX690T) UNIT:3 MyVIO3 (VIO)". It contains a table with columns "Bus/Signal" and "Value". The "vio_modify_enable" signal is highlighted with a red box around its value cell, which is set to 1. Other signals listed include vio_data_mask_gen, vio_pause_traffic, dbg_clear_error, vio_addr_mode_value, vio_bl_mode_value, vio_fixed_bl_value, vio_fixed_instr_value, vio_instr_mode_value, and vio_data_mode_value, each with their respective numerical values.

Bus/Signal	Value
vio_modify_enable	1
vio_data_mask_gen	0
vio_pause_traffic	0
dbg_clear_error	0
vio_addr_mode_value	3
vio_bl_mode_value	2
vio_fixed_bl_value	16
vio_fixed_instr_value	1
vio_instr_mode_value	2
vio_data_mode_value	2

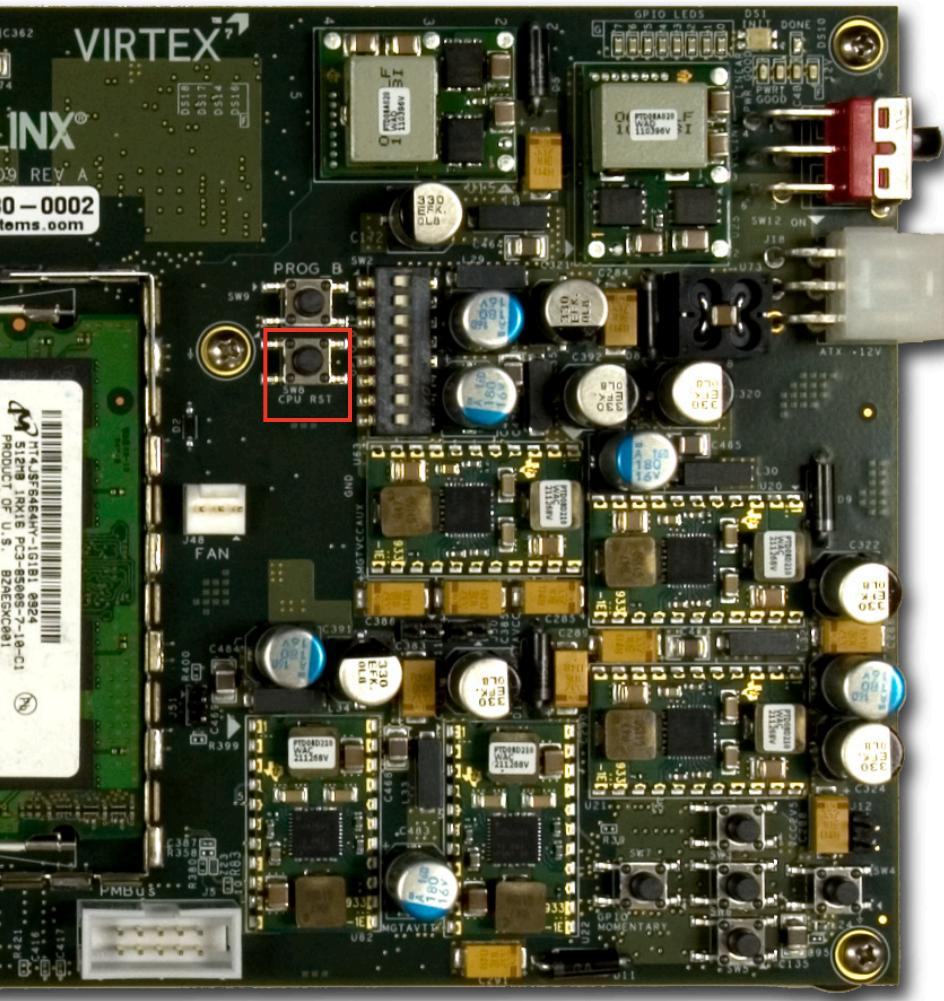
Adjust Data Pattern using VIO Console

- Set `vio_data_mode_value` to “7” for `PRBS_DATA`

The screenshot shows the ChipScope Pro Analyzer interface. The left sidebar displays the JTAG Chain structure for project `vc709_mig_bank_a`, including units `MyDevice0`, `MyILA0`, `MyILA1`, `MyILA2`, `MyVIO3`, and `MyVIO4`. The `VIO Console` under `MyVIO3` is selected. The main window is titled "VIO Console - DEV:0 MyDevice0 (XC7VX690T) UNIT:3 MyVIO3 (VIO)". It contains a table with columns "Bus/Signal" and "Value". The row for `vio_data_mode_value` is highlighted in yellow, indicating it is being edited. The current value is 7, shown in a blue input field.

Bus/Signal	Value
<code>vio_modify_enable</code>	1
<code>vio_data_mask_gen</code>	0
<code>vio_pause_traffic</code>	0
<code>dbg_clear_error</code>	0
<code>vio_addr_mode_value</code>	3
<code>vio.bl_mode_value</code>	2
<code>vio.fixed.bl_value</code>	16
<code>vio.fixed.instr_value</code>	1
<code>vio.instr.mode_value</code>	2
<code>vio.data.mode_value</code>	7

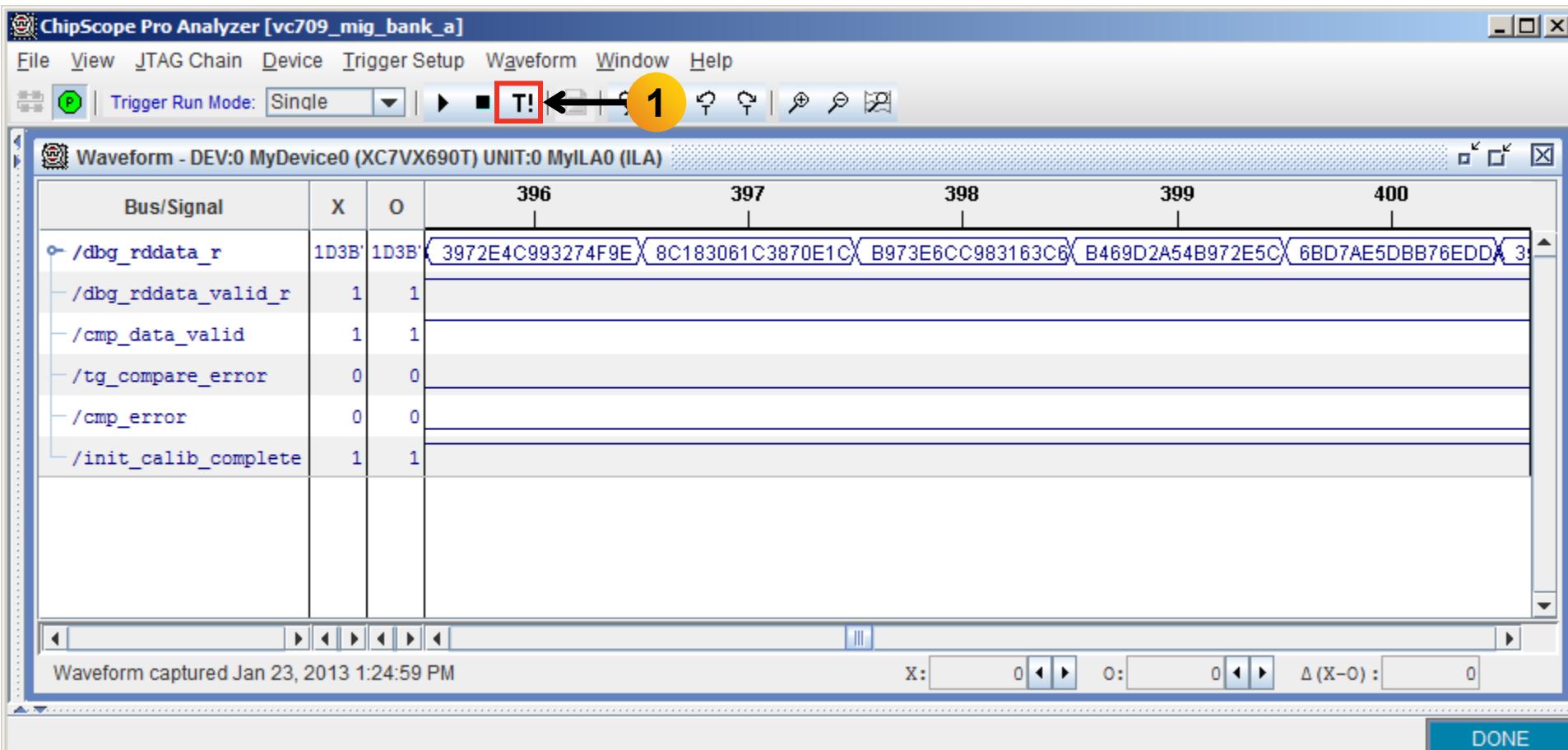
Run MIG Bank A Example Design



▶ Press and release the CPU
RESET switch, SW8, after each
change to vio_modify_enable
or vio_data_mode_value

Run MIG Bank A Example Design

- Click on Waveform; click the Trigger Immediate button (1)
- View PRBS data



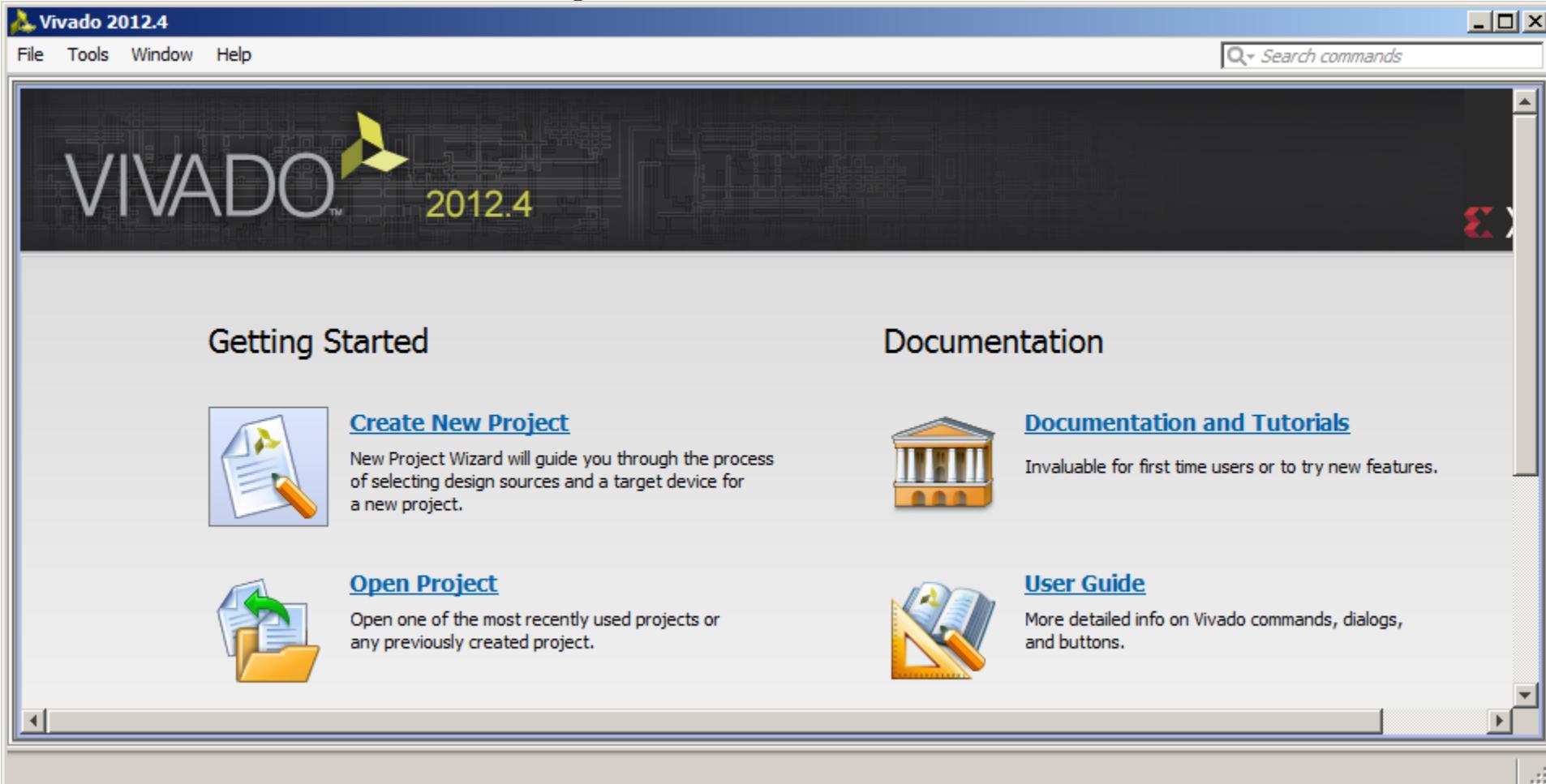
Generate MIG Bank B Example Design

Generate MIG Bank B Example Design

► Open Vivado

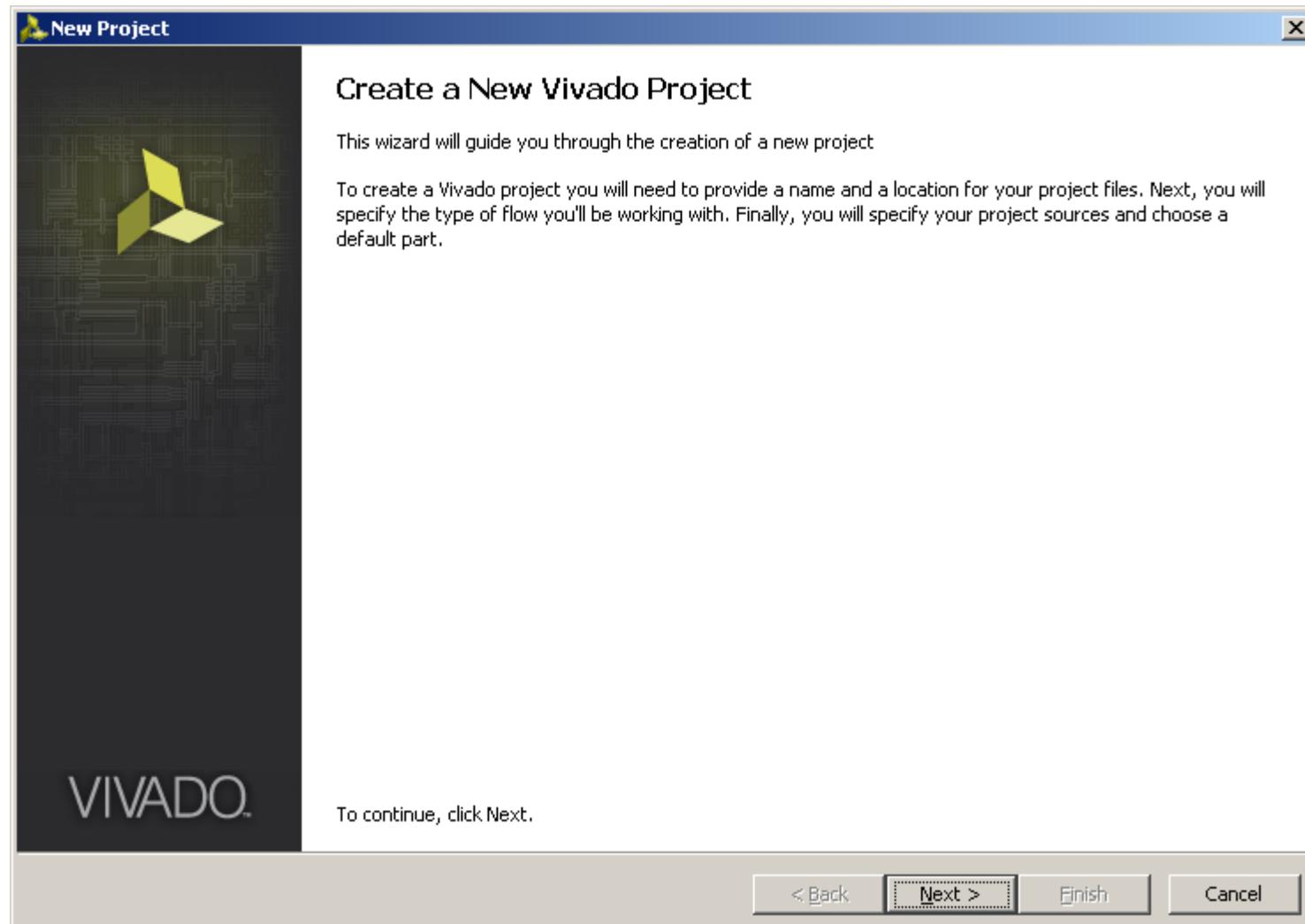
Start → All Programs → Xilinx Design Tools → Vivado 2012.4 → Vivado

► Select Create New Project



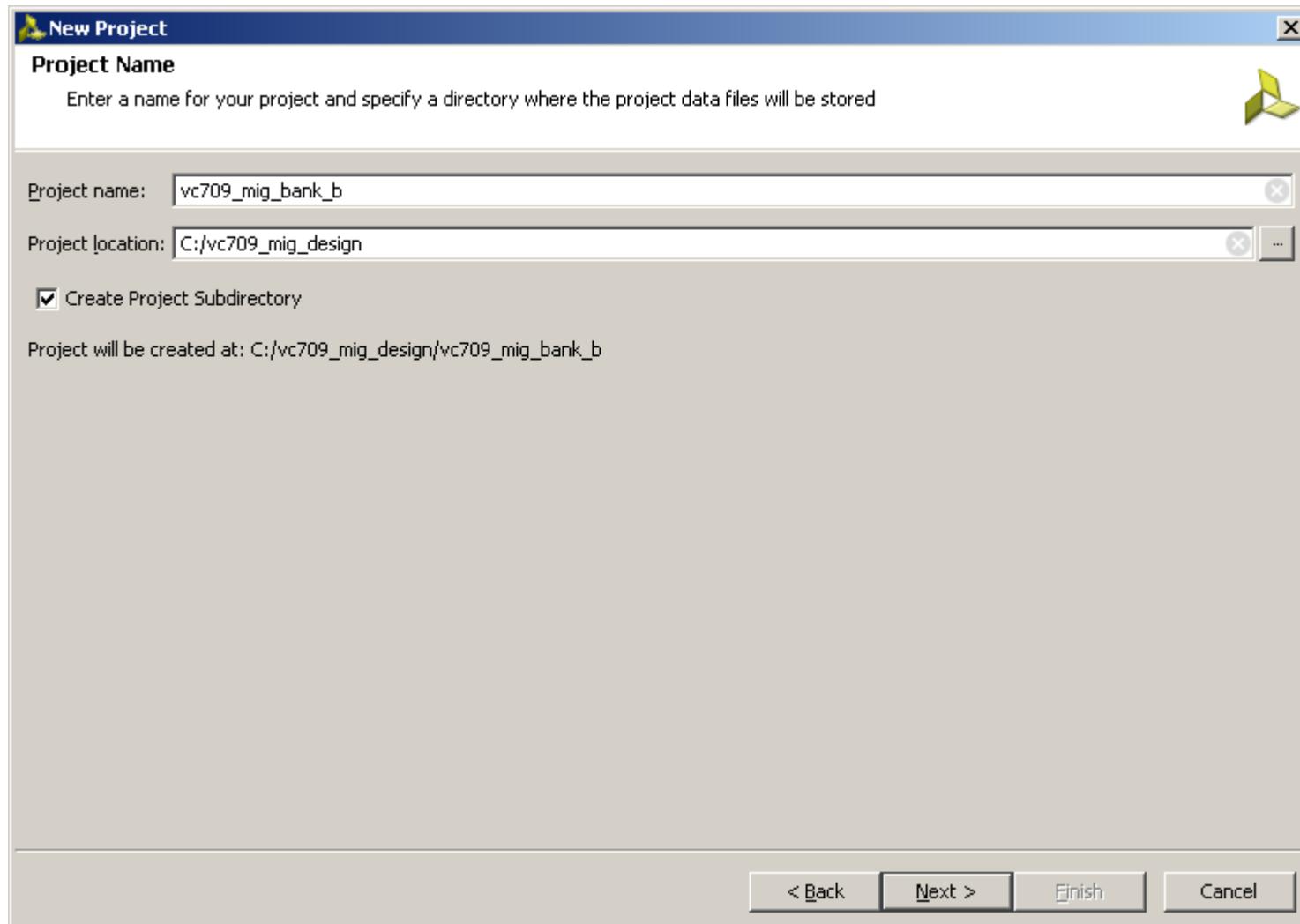
Generate MIG Bank B Example Design

► Click Next



Generate MIG Bank B Example Design

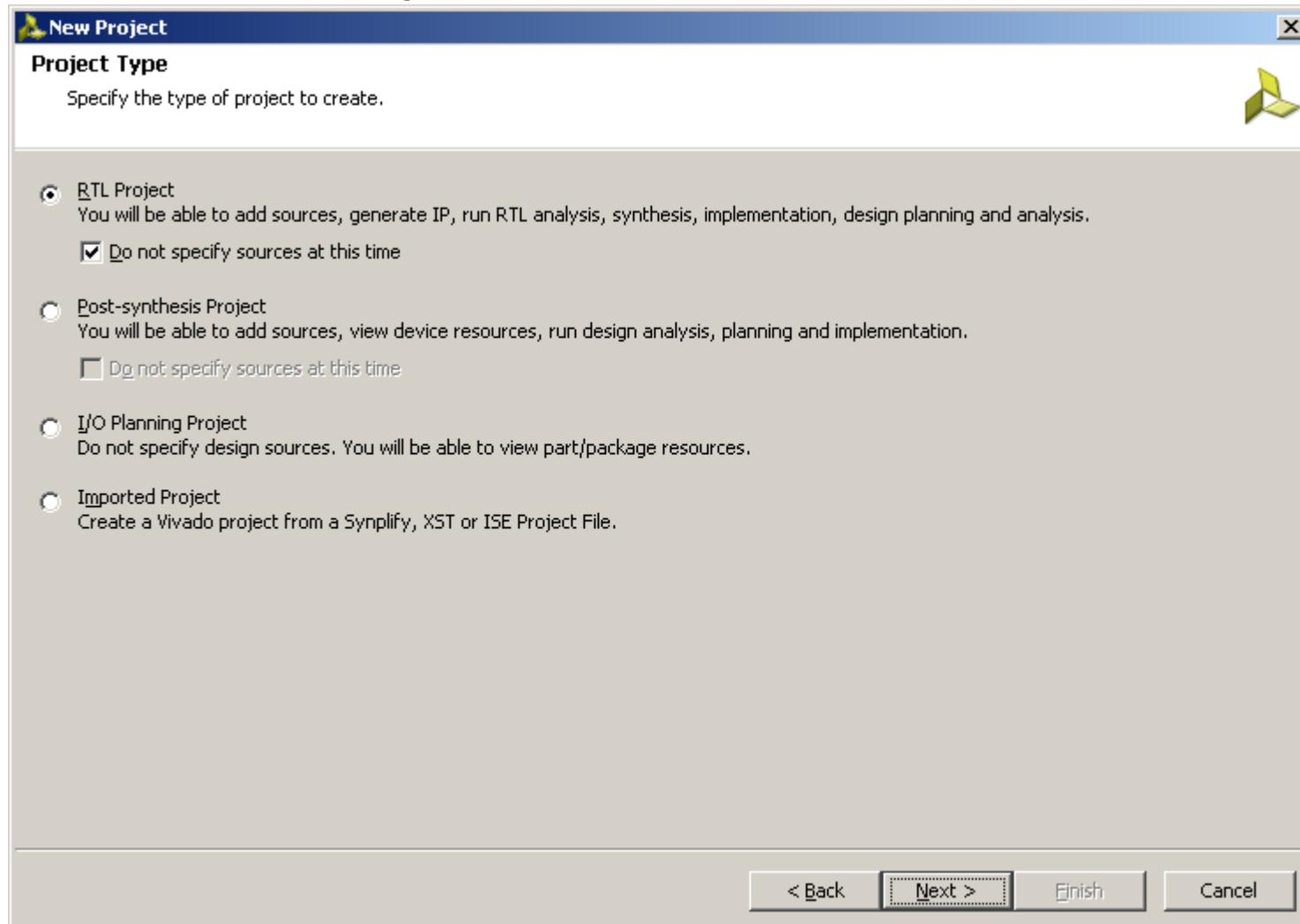
- Set the Project name to vc709_mig_bank_b and location to C:\vc709_mig_design



Generate MIG Bank B Example Design

► Select RTL Project

- Select **Do not specify sources at this time**



Generate MIG Bank B Example Design

- ▶ Select the xc7vx690tffg1761-2 device

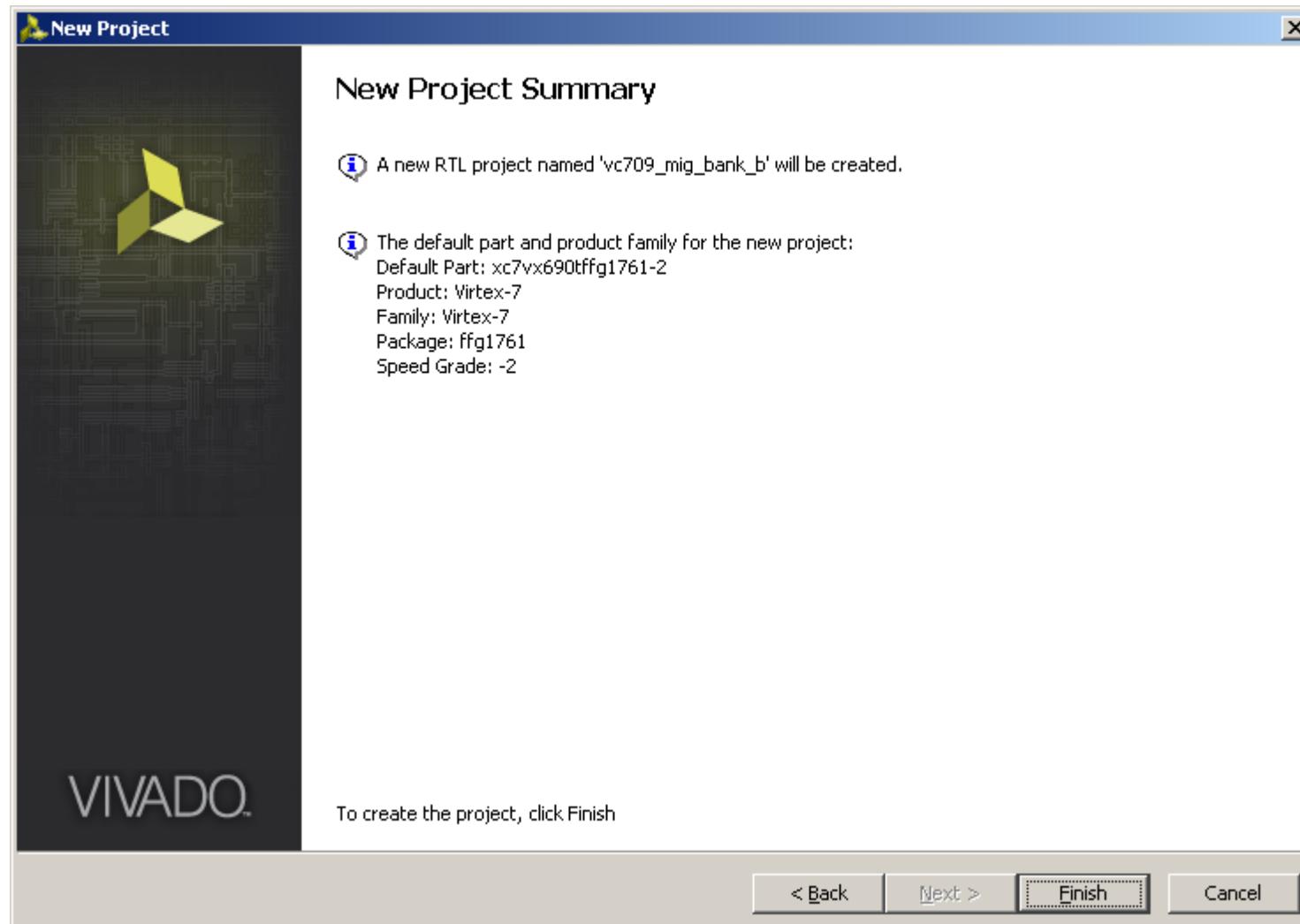
The screenshot shows the 'New Project' dialog box with the title 'Default Part'. The 'Parts' tab is selected in the sidebar. The filter settings are set to 'Product category: All', 'Package: FFG1761', 'Family: Virtex-7', 'Sub-Family: All Remaining', and 'Speed grade: -2'. A search bar at the bottom left contains the text 'xc7vx690tffg1761-2'. The main table lists four device options:

Device	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	DSPs	Gb Transceivers	PCI Buses
xc7v585tffg1761-2	1,761	850	364200	728400	795	1260	36	3
xc7vx330tffg1761-2	1,761	700	204000	408000	750	1120	28	2
xc7vx485tffg1761-2	1,761	700	303600	607200	1030	2800	28	4
xc7vx690tffg1761-2	1,761	850	433200	866400	1470	3600	36	3

At the bottom of the dialog, there are buttons for '< Back', 'Next >', 'Finish', and 'Cancel'.

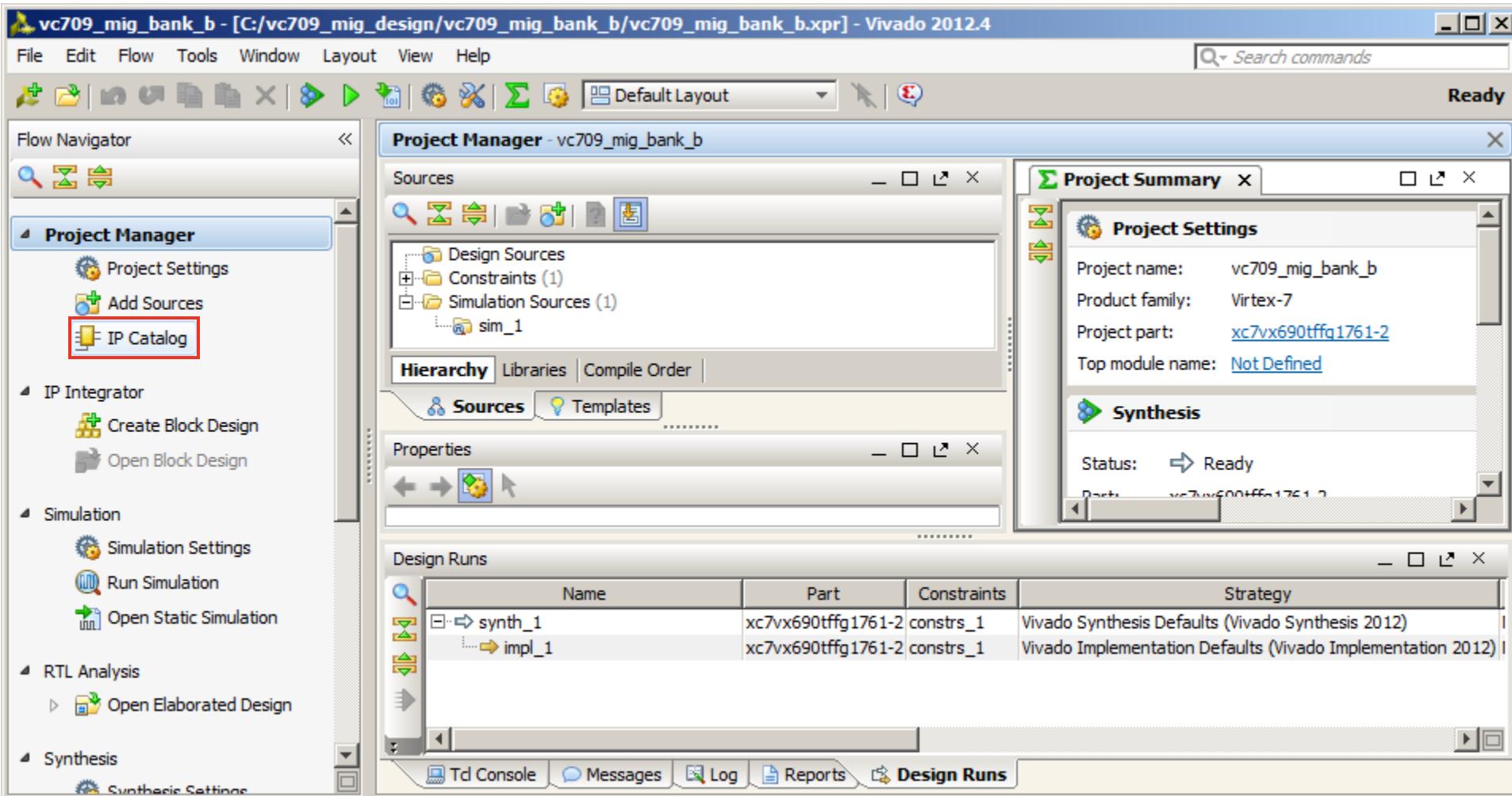
Generate MIG Bank B Example Design

► Click Finish



Generate MIG Bank B Example Design

► Click on IP Catalog



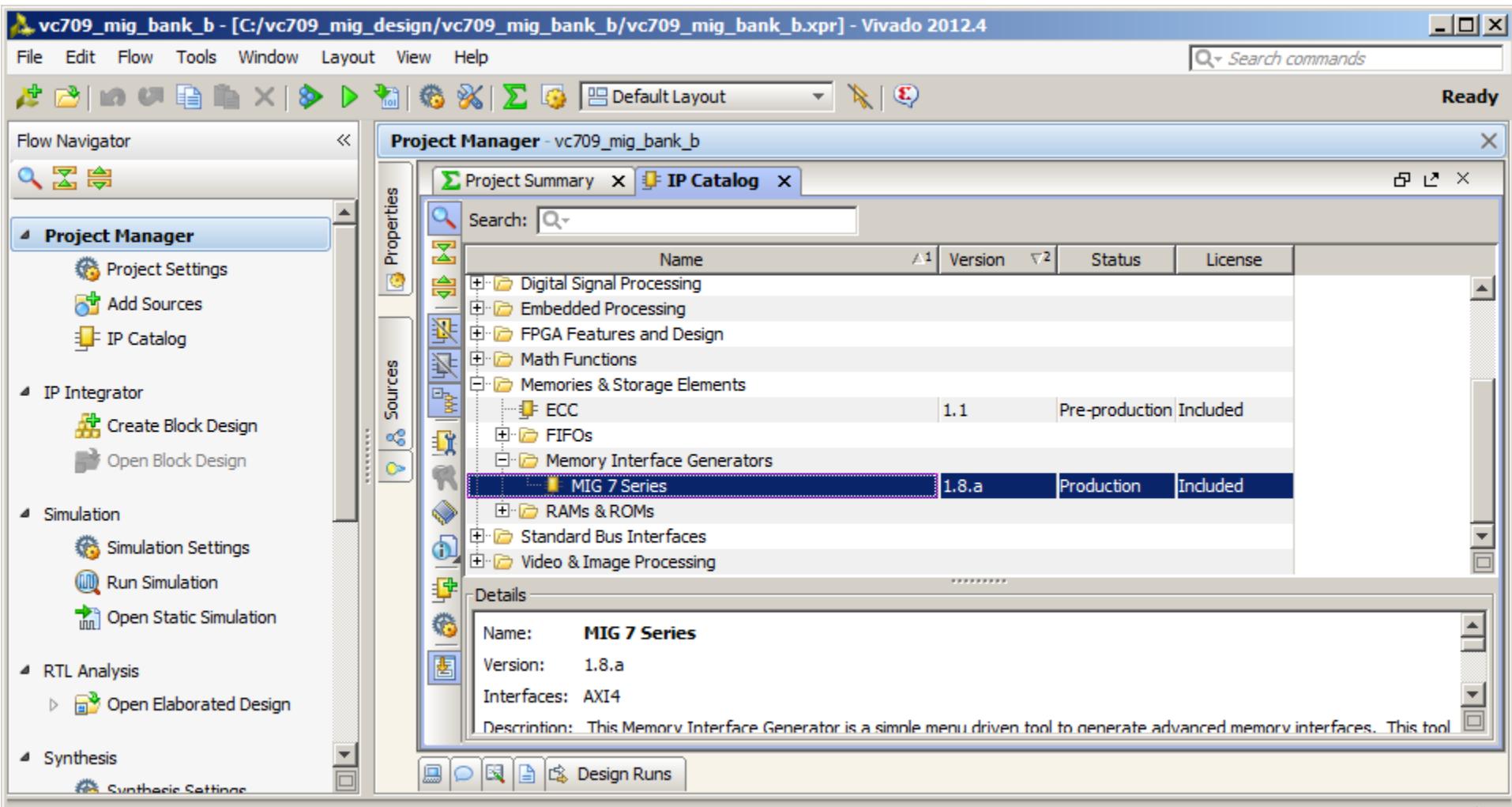
Browse, customize, and generate cores.

Note: Presentation applies to the VC709

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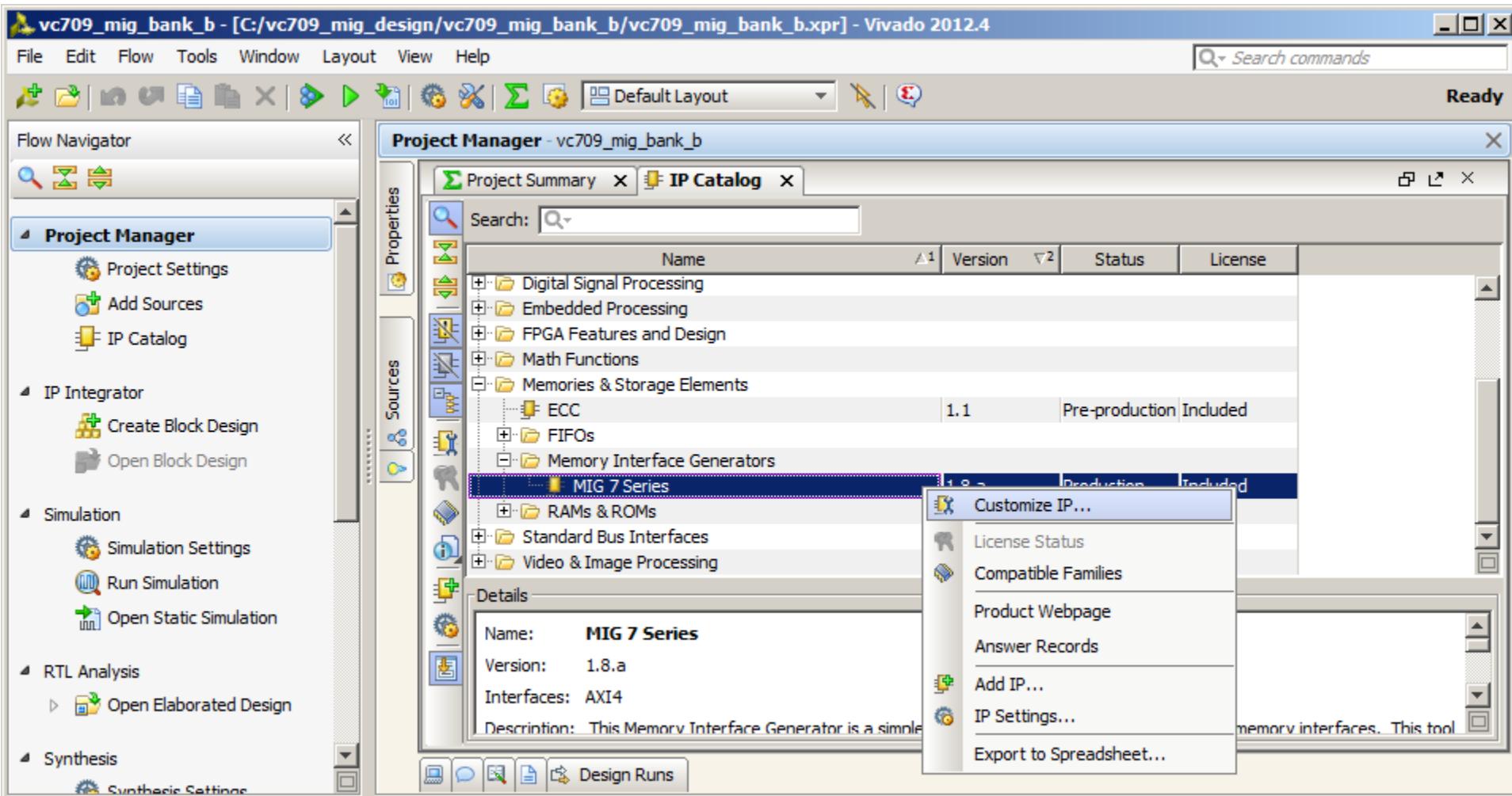
Generate MIG Bank B Example Design

► Select MIG 7 Series under Memory Interface Generators



Generate MIG Bank B Example Design

- Right click on MIG 7 Series Version 1.8.a
 - Select Customize IP

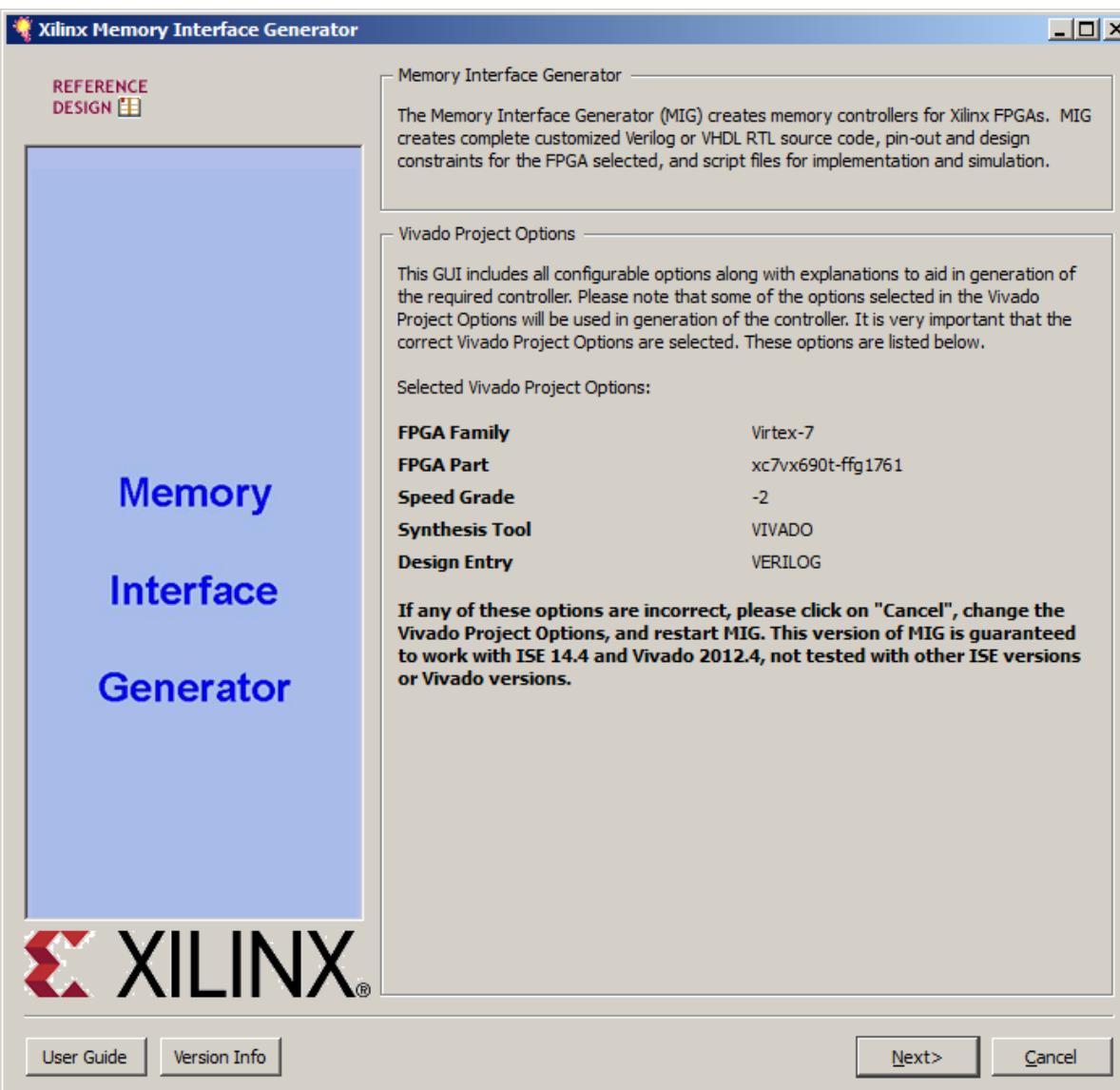


Customize the selected core

Note: Presentation applies to the VC709

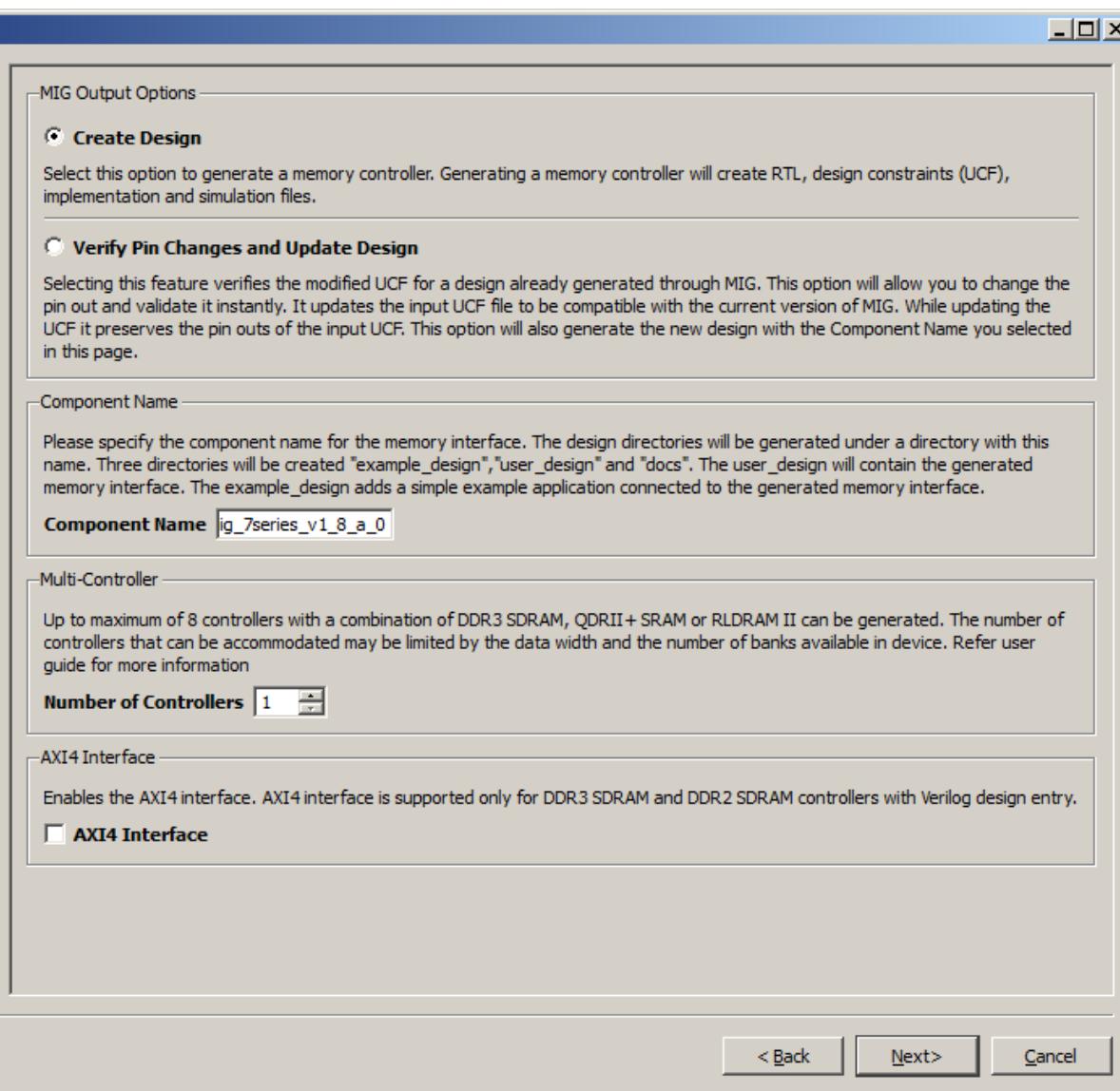
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Generate MIG Bank B Example Design



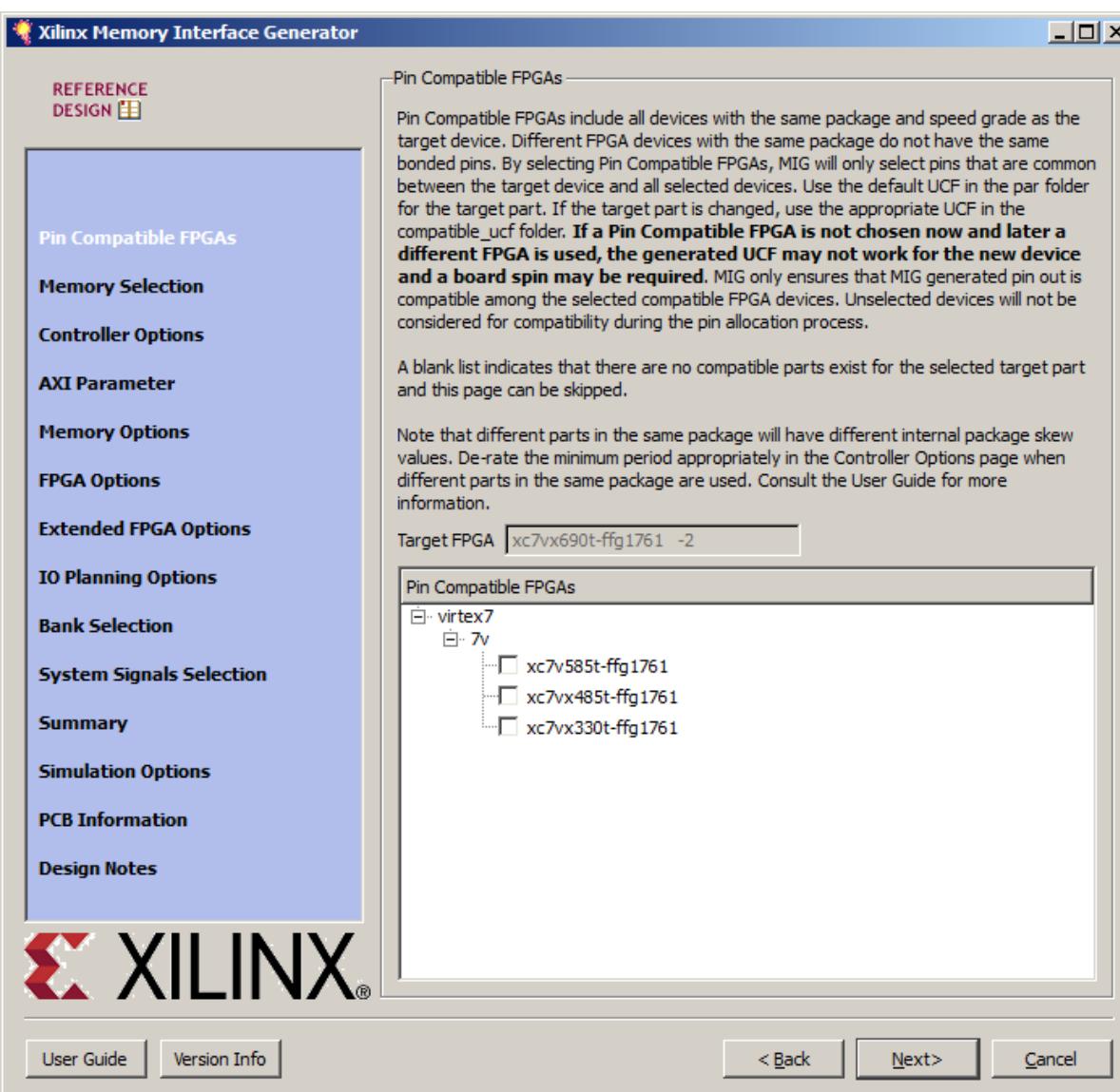
➤ Leave this page as is
– Click Next

Generate MIG Bank B Example Design



➤ Leave this page as is
– Click Next

Generate MIG Bank B Example Design



➤ Leave this page as is
– Click Next

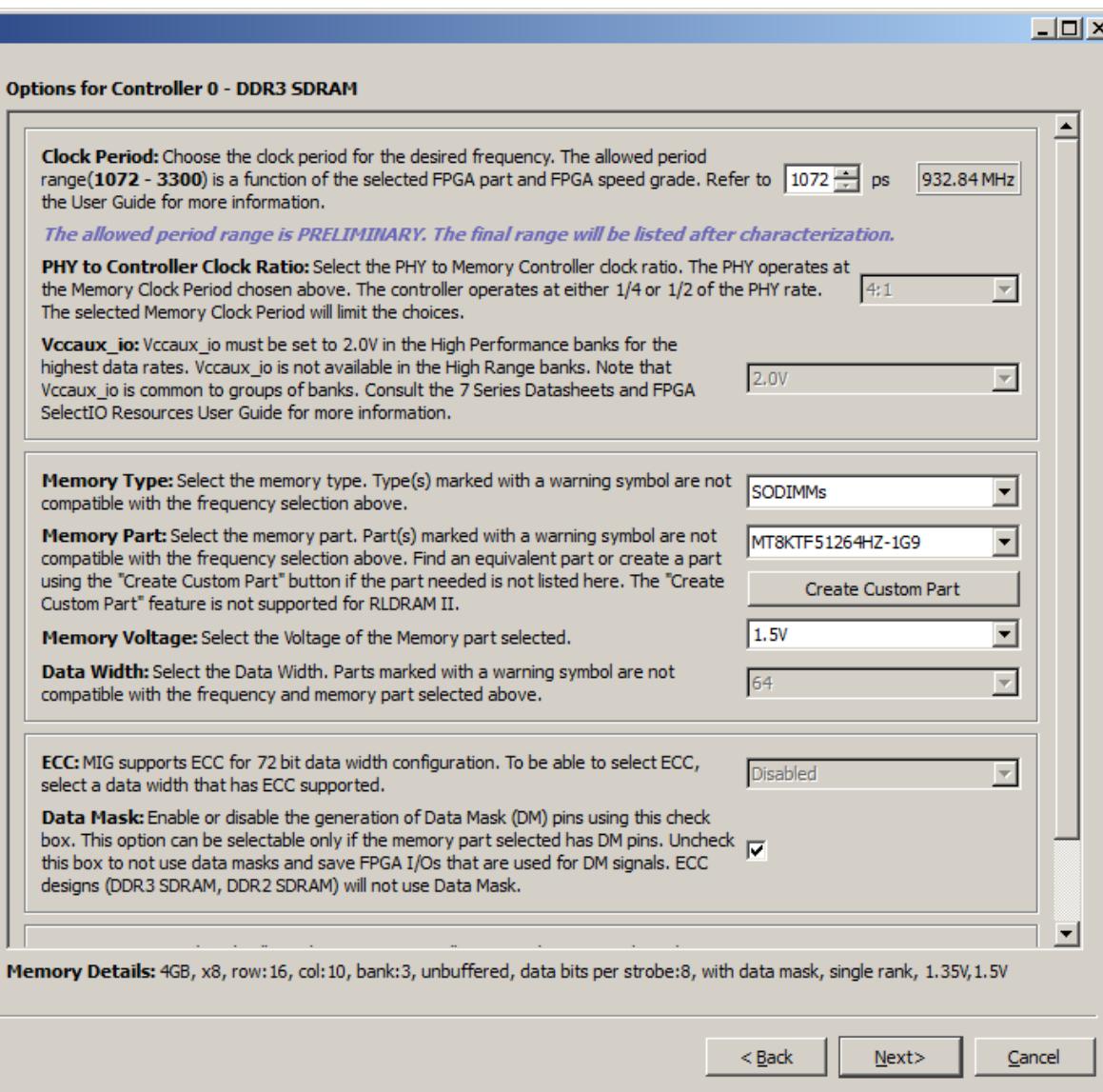
Generate MIG Bank B Example Design



➤ Select Memory Type

- DDR3 SDRAM
- Click Next

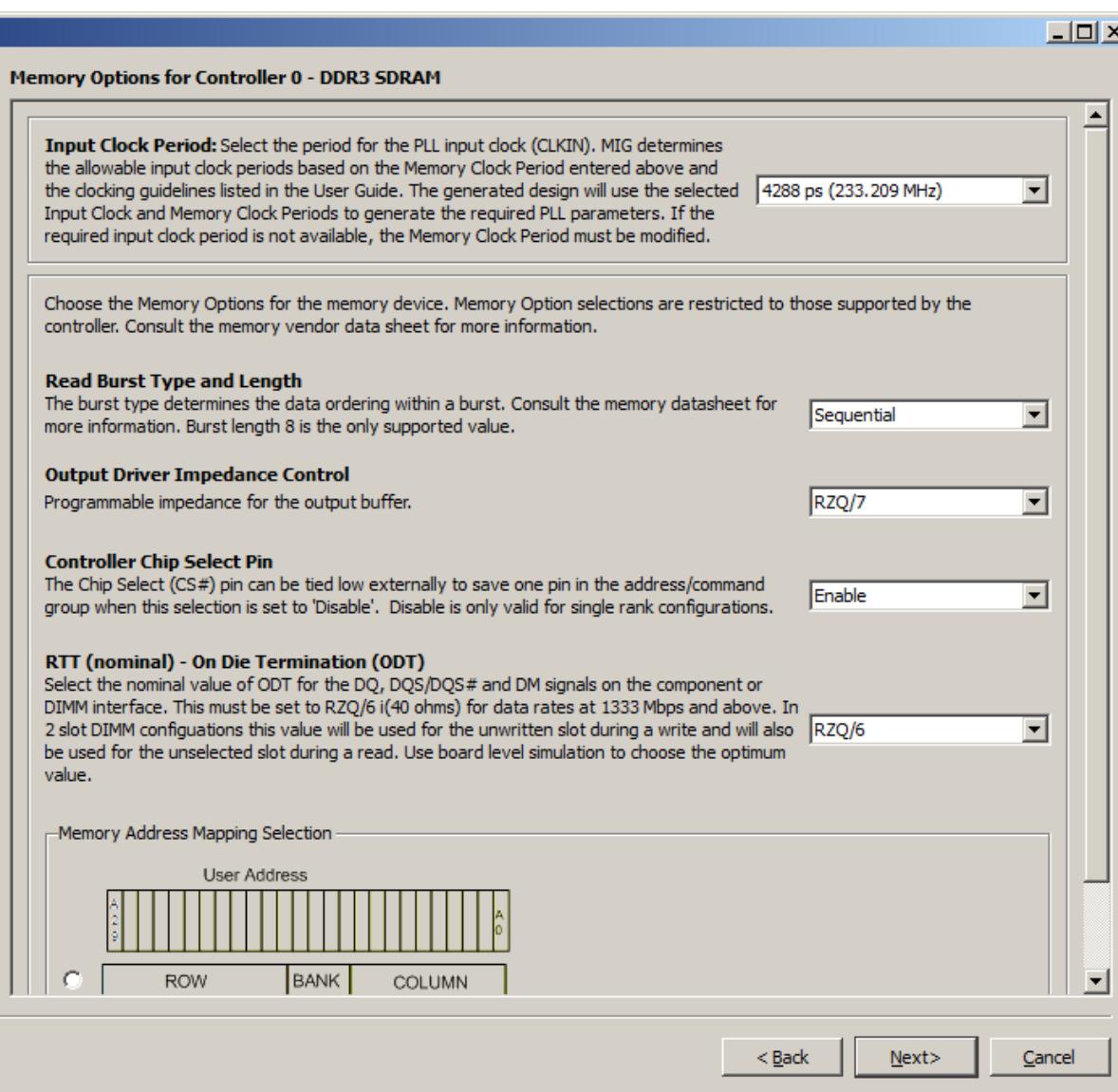
Generate MIG Bank B Example Design



► Select

- Clock Period: **1072 ps**
- Type: **SODIMMs**
- Part:
MT8KTF51264HZ-1G9
- Memory Voltage: **1.5V**
- Data Mask: **Checked**
- Click Next

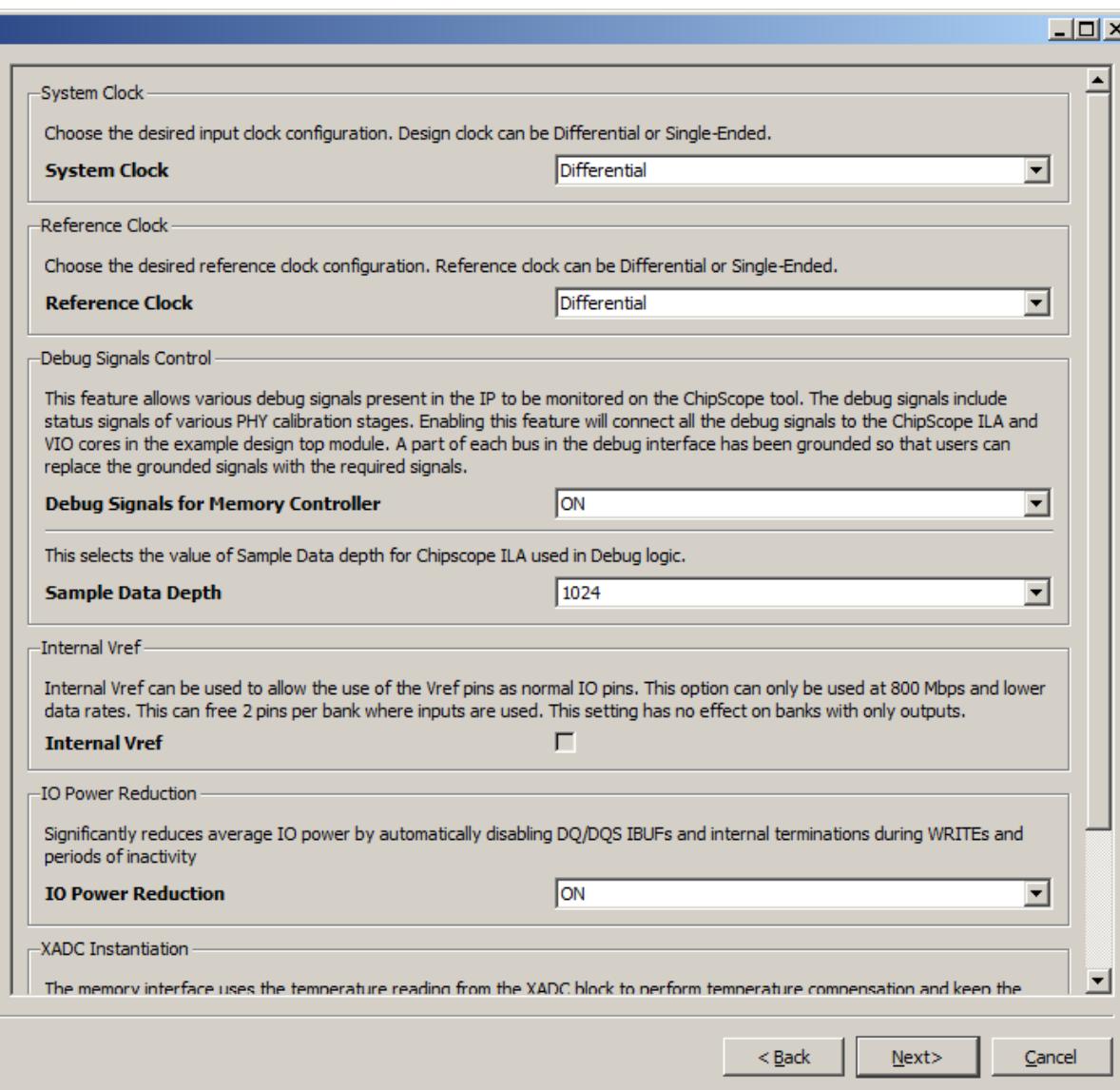
Generate MIG Bank B Example Design



► Select:

- Input Clock Period: **4288 ps**
- RTT: **RZQ/6**
- Click Next

Generate MIG Bank B Example Design



► Select

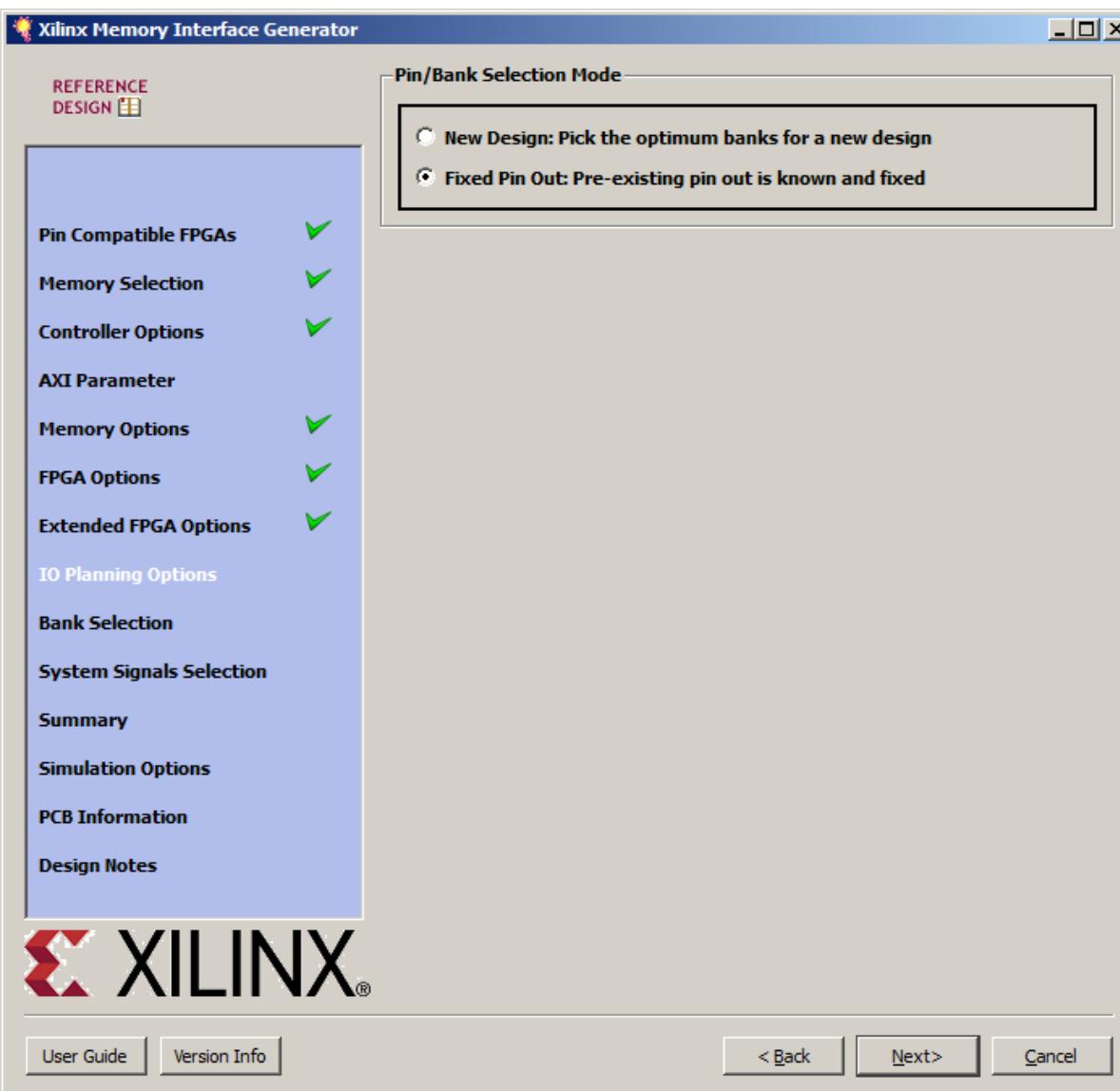
- Set the System and Reference Clocks to **Differential**
- Debug: **ON**
- Click Next

Generate MIG Bank B Example Design



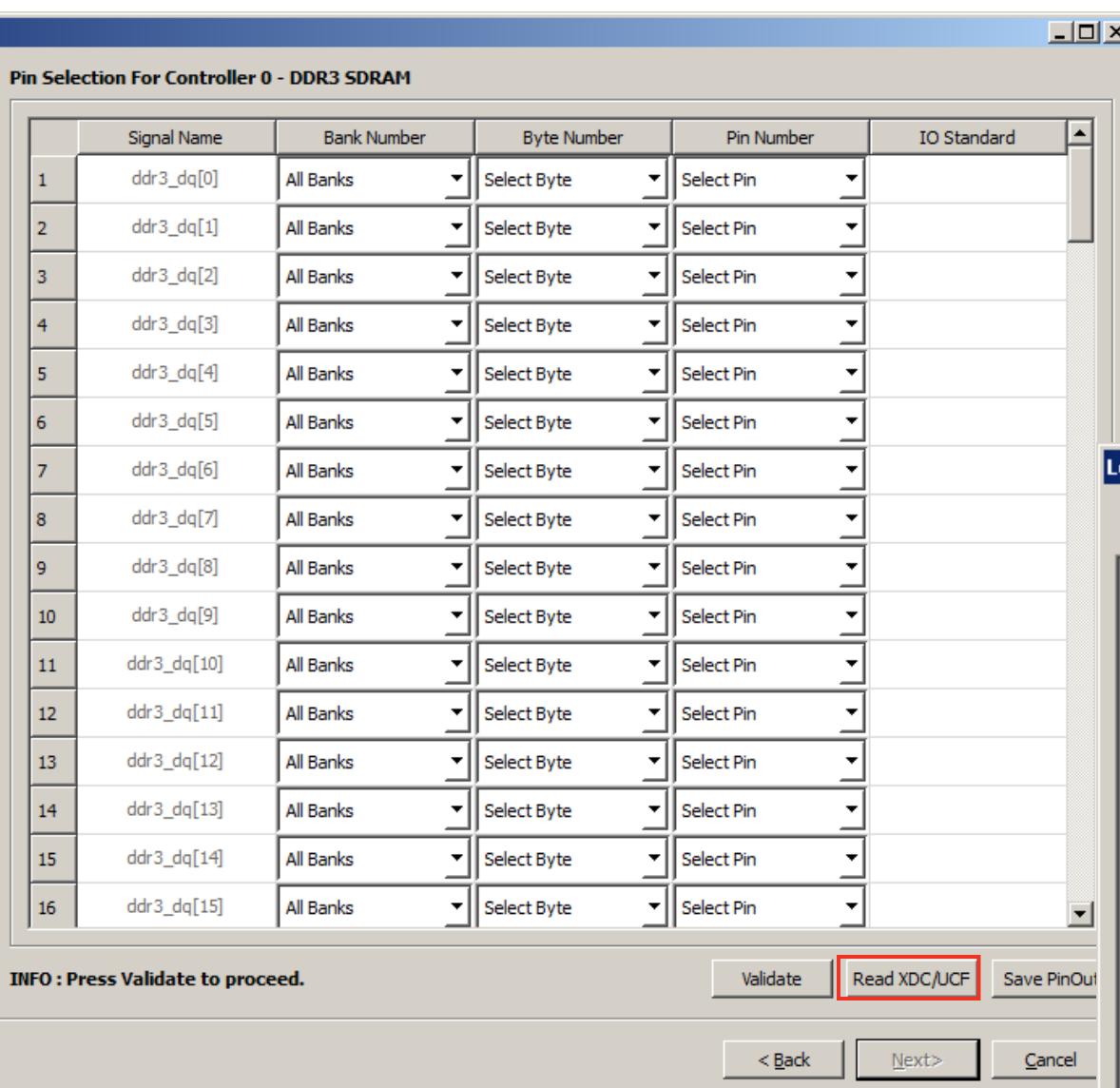
➤ Leave this page as is
– Click Next

Generate MIG Bank B Example Design



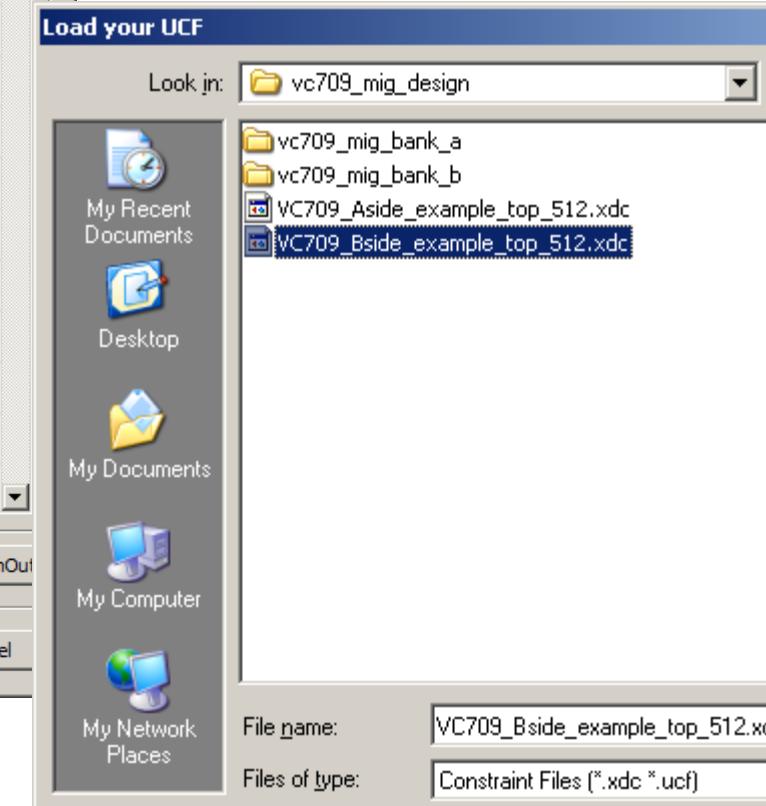
► Select Fixed Pin Out
– Click Next

Generate MIG Bank B Example Design



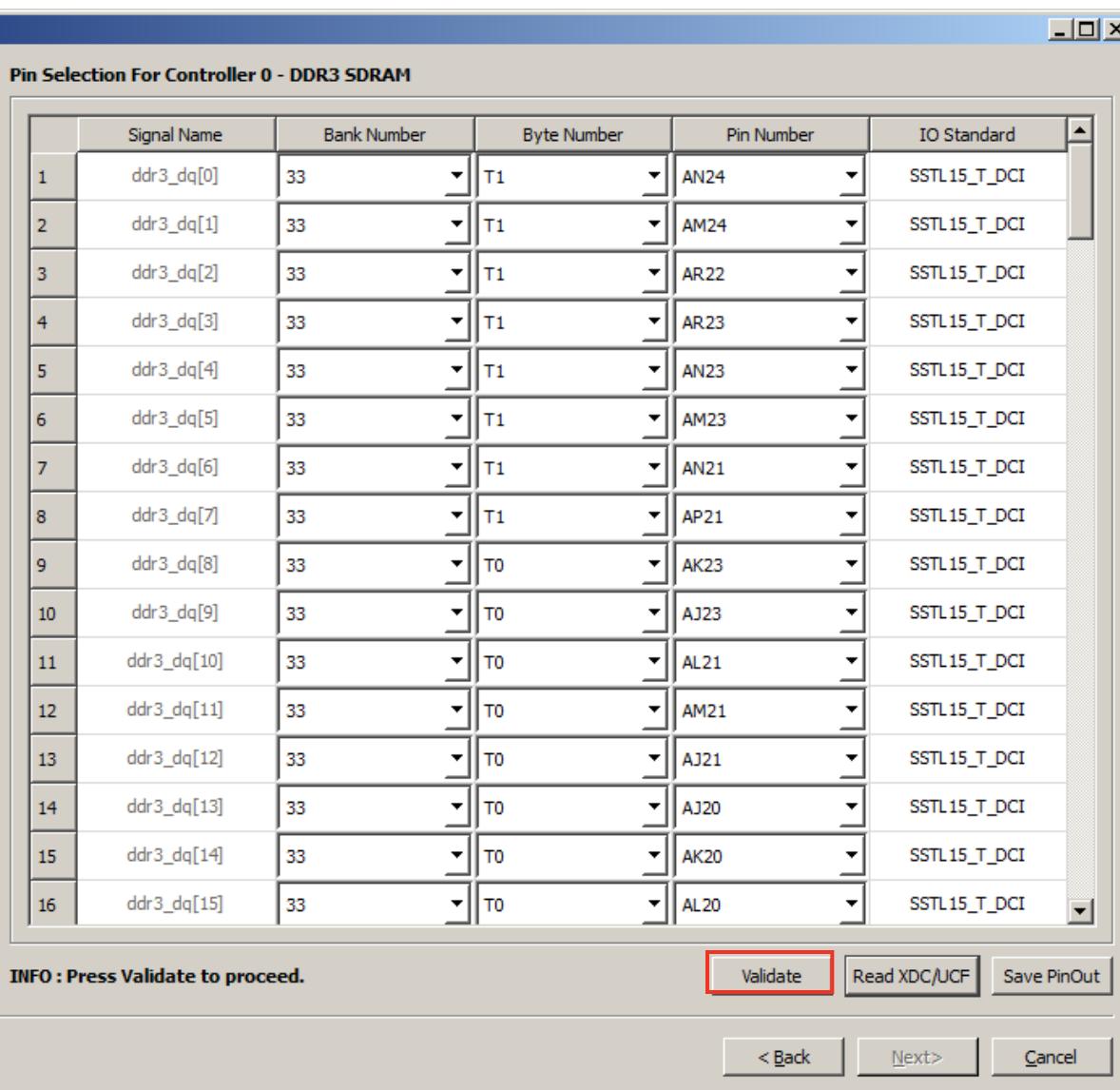
► Select Read XDC/UCF

- Open the file:
VC709_Bside_example_top_512.xdc

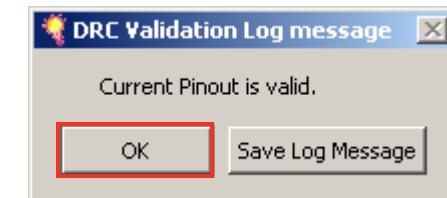


Note: Presentation applies to the VC709

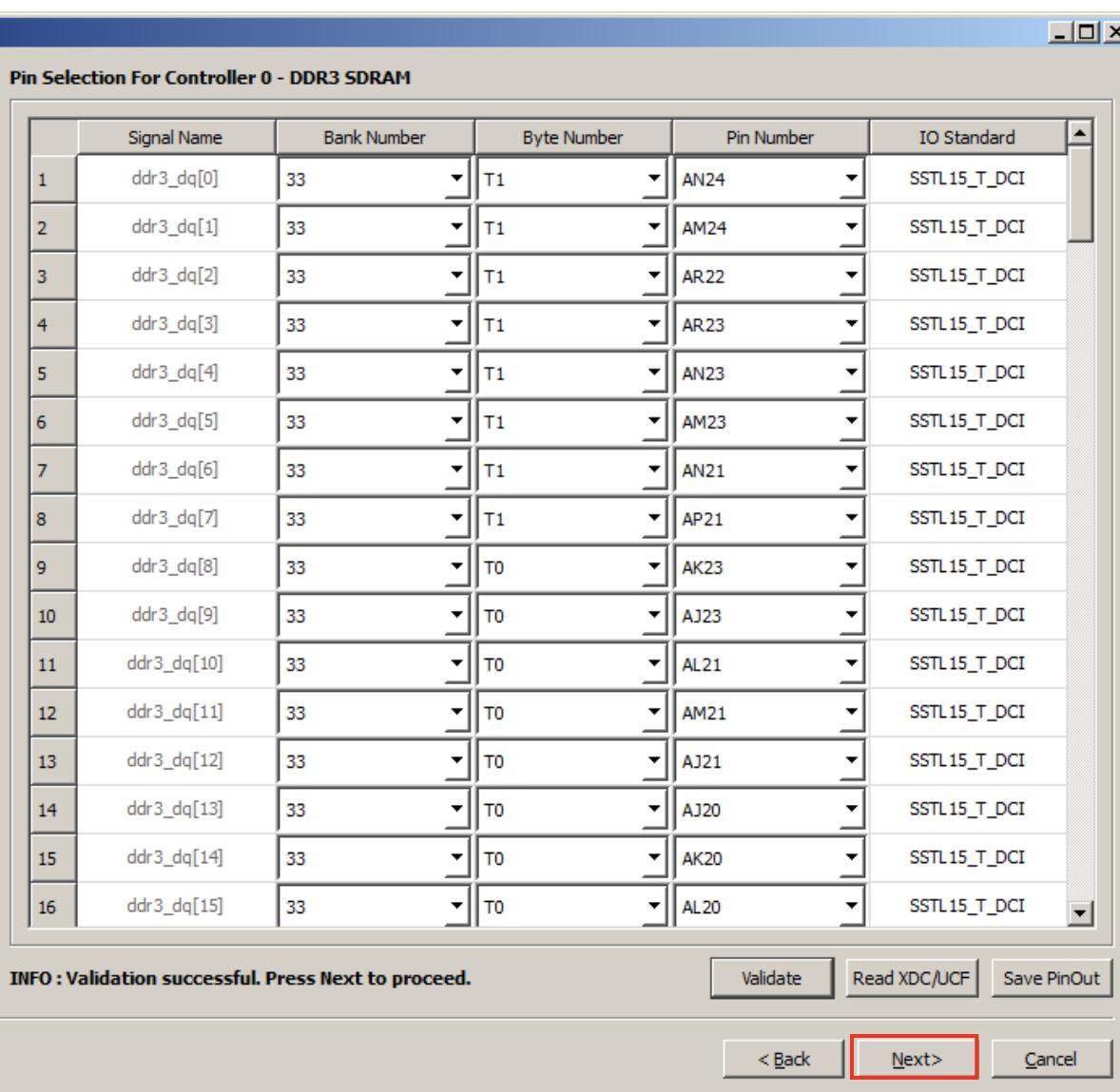
Generate MIG Bank B Example Design



- Once it finishes reading in the XDC, click Validate
 - Click OK

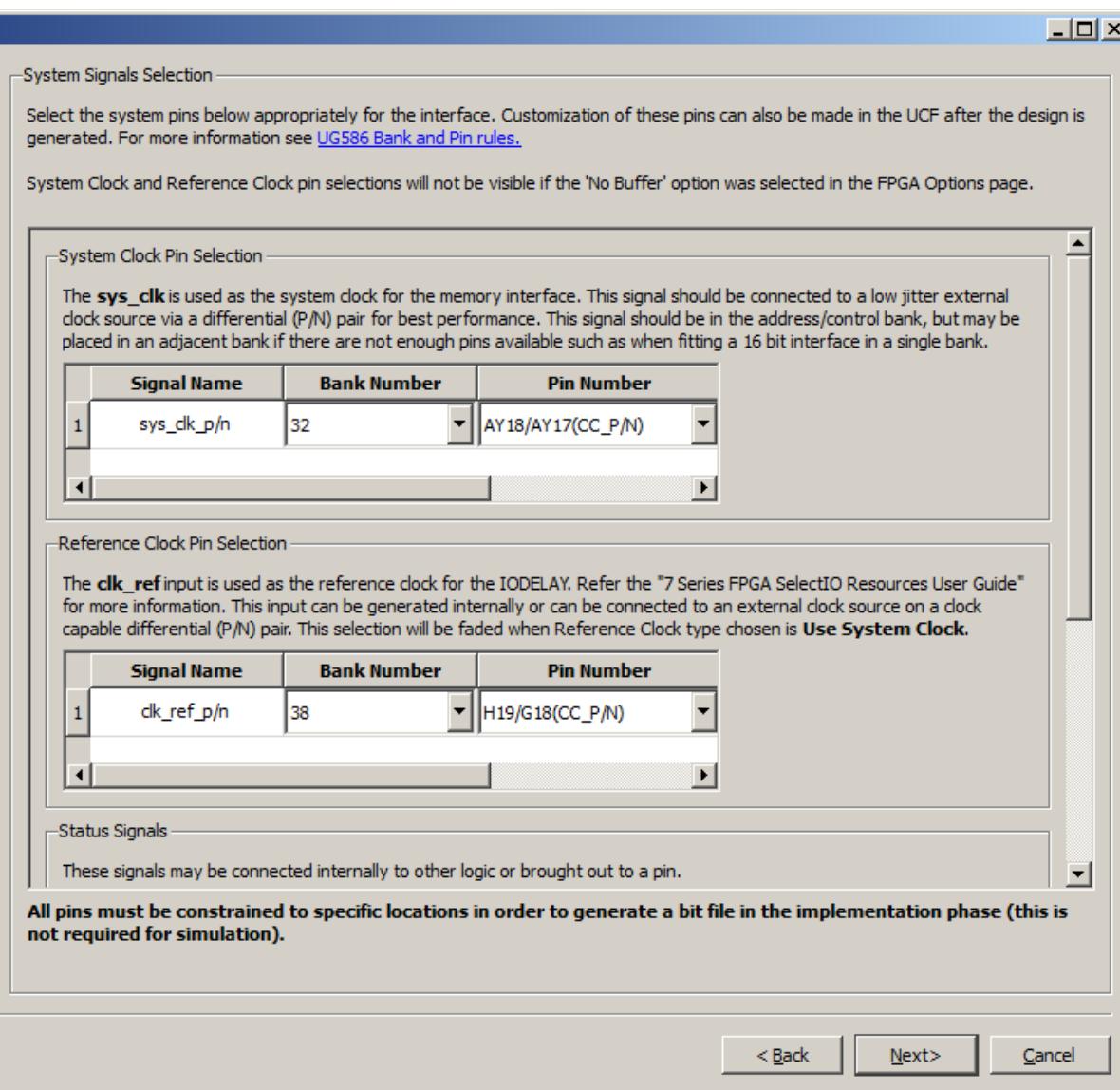


Generate MIG Bank B Example Design



➤ The Next button is enabled once the pinout is validated.
– Click Next

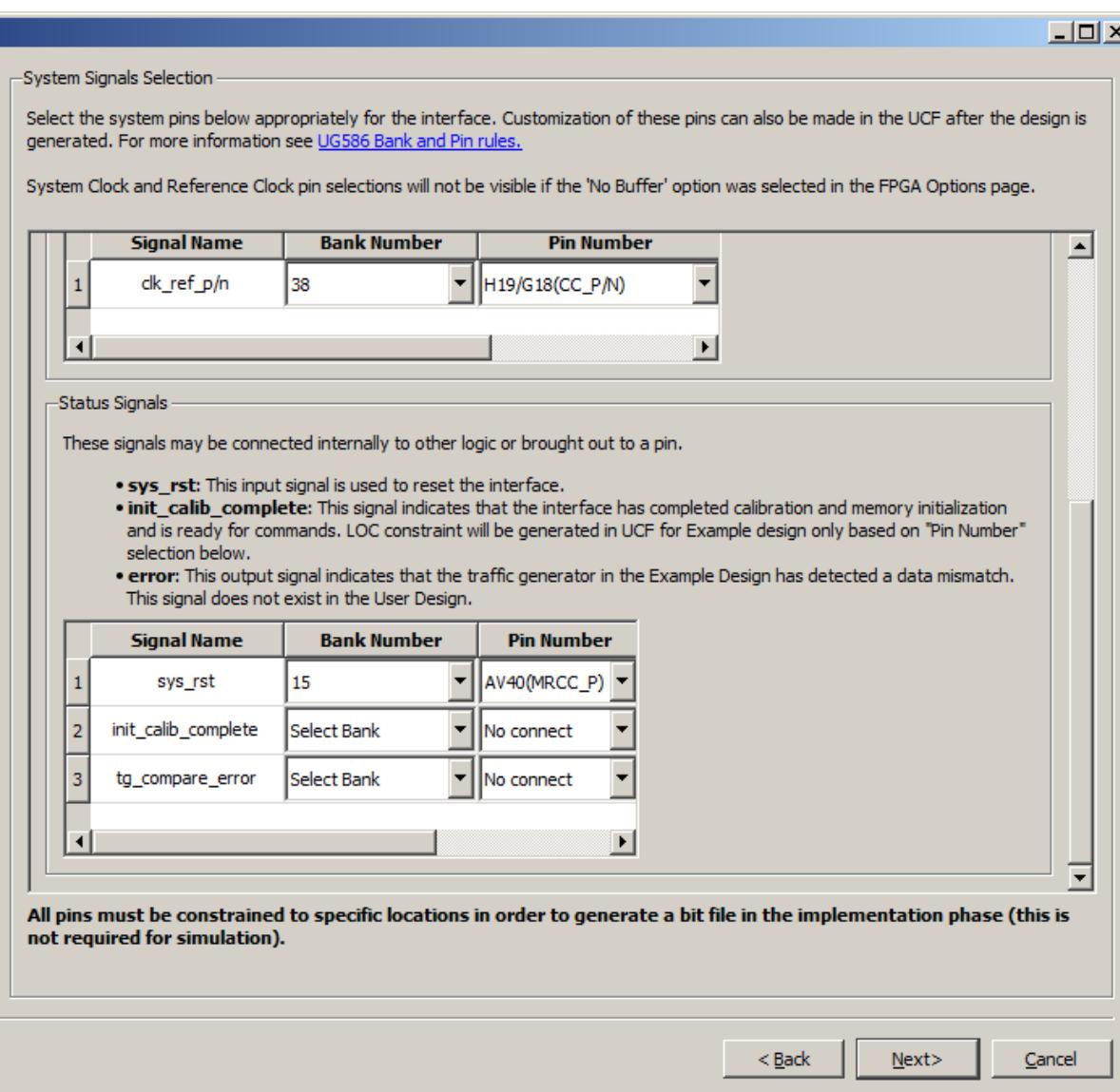
Generate MIG Bank B Example Design



➤ Make the following settings:

- Set sys_clk_p/n to Bank: **32**
- Pin Number: **AY18/AY17(CC_P/N)**
- Set clk_ref_p/n to Bank: **38**
- Pin Number: **H19/G18(CC_P/N)**
- Scroll down

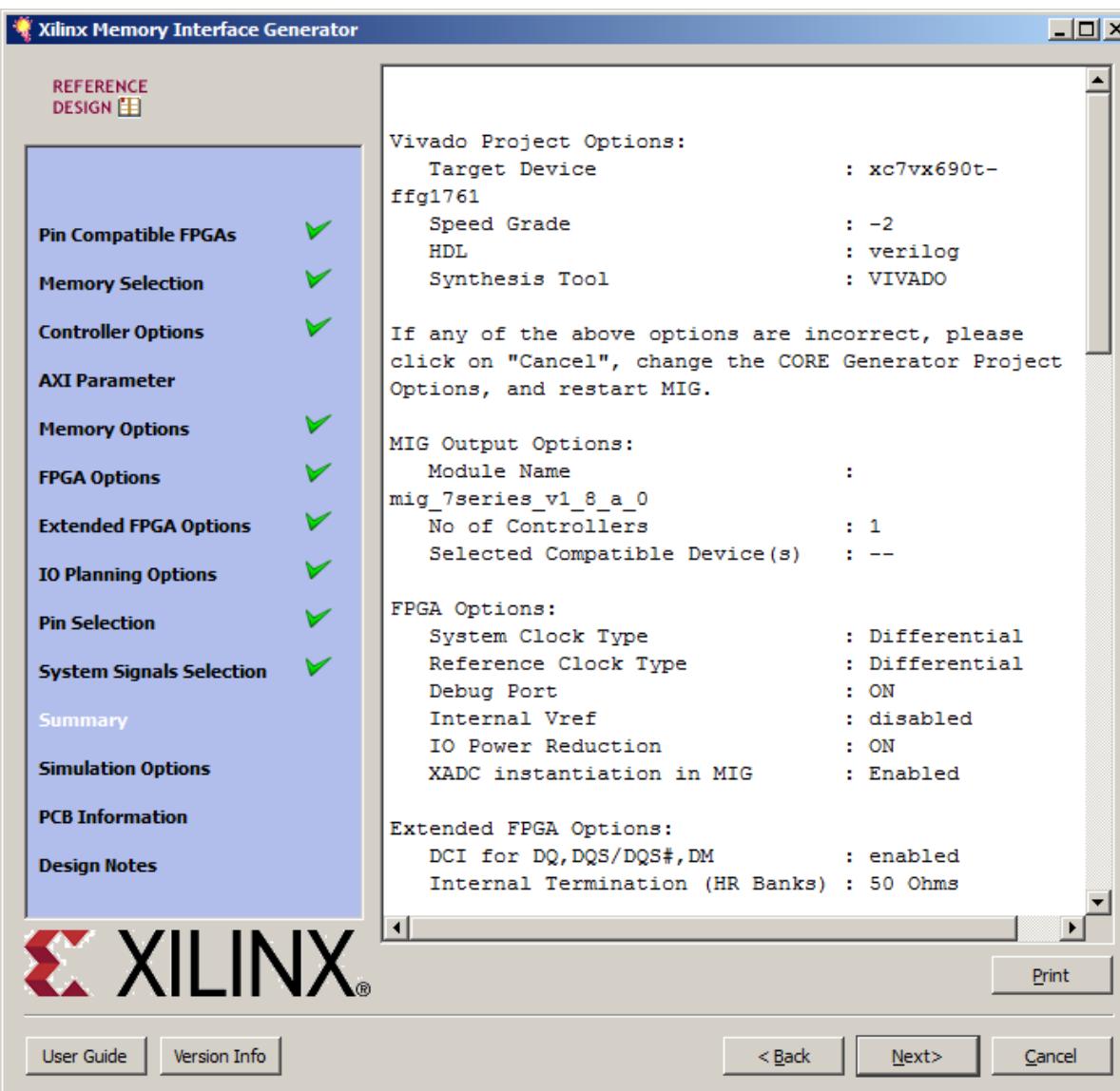
Generate MIG Bank B Example Design



➤ Make the following settings:

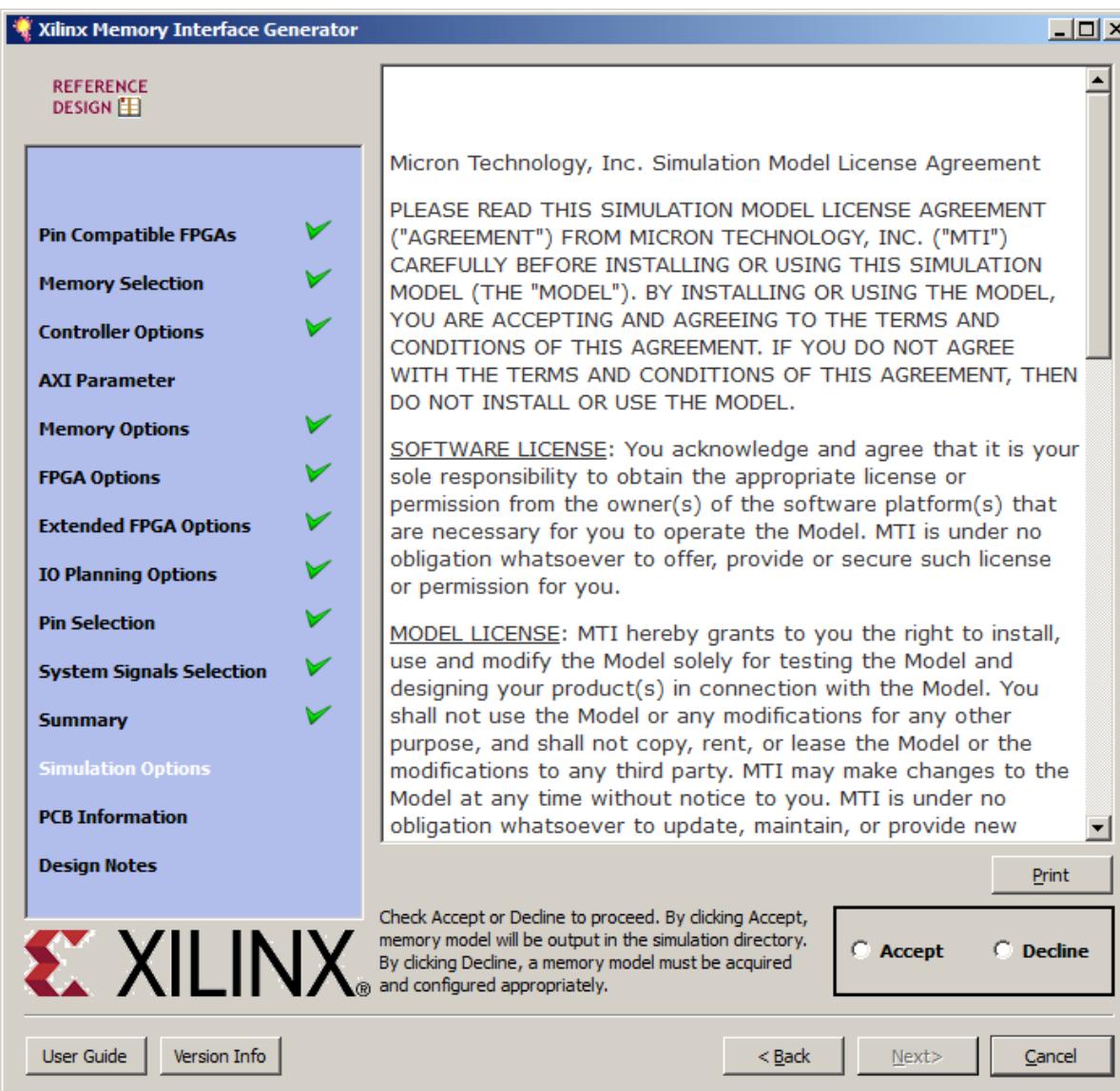
- Set sys_rst to Bank: 15
- Pin Number:
AV40(MRCC_P)
- Click Next

Generate MIG Bank B Example Design



► Leave this page as is
– Click Next

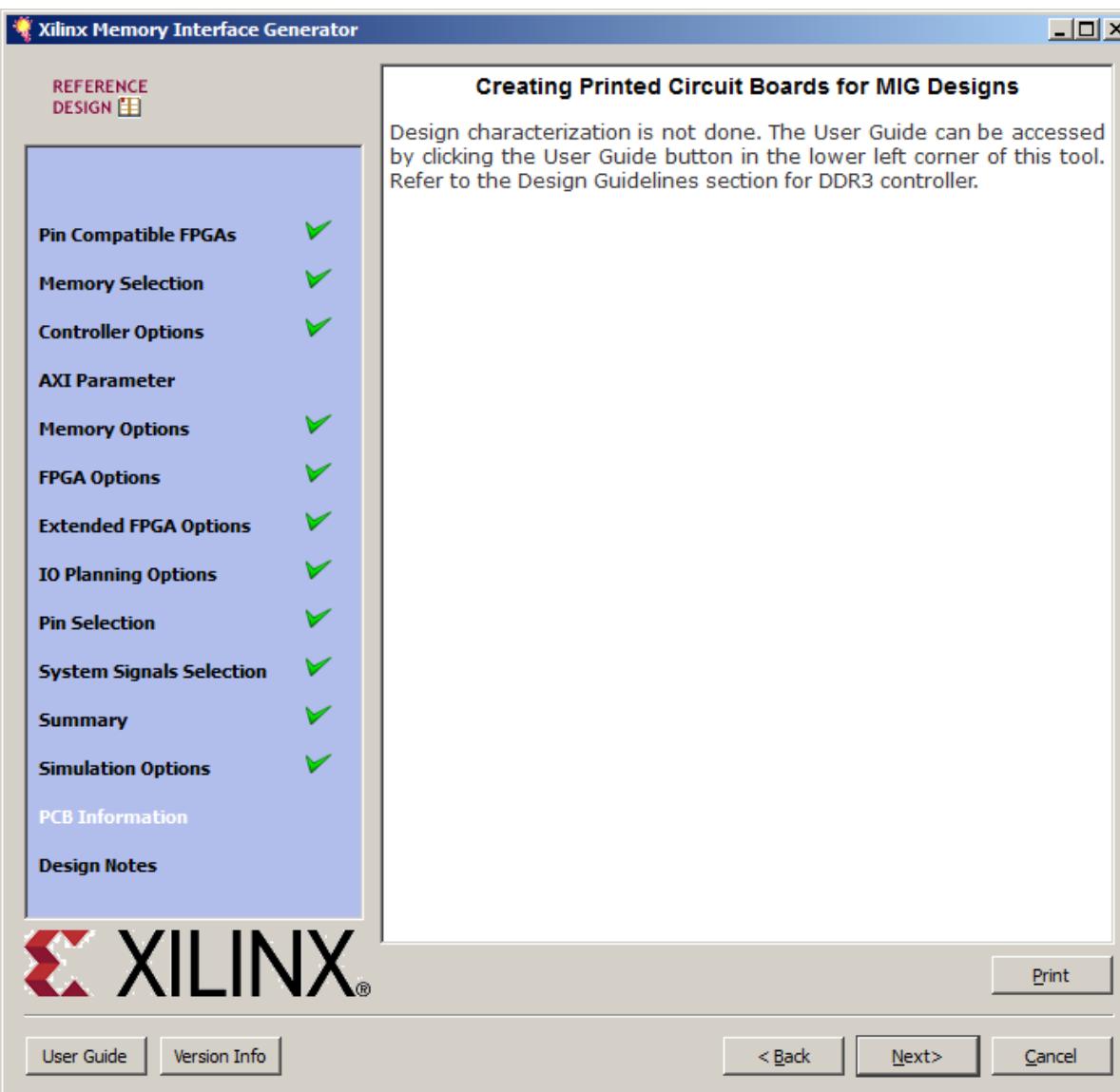
Generate MIG Bank B Example Design



➤ Accept Simulation license, if desired

- Otherwise, Decline license
- Click Next

Generate MIG Bank B Example Design



➤ Leave this page as is
– Click Next

Generate MIG Bank B Example Design

Xilinx Memory Interface Generator

REFERENCE DESIGN

Pin Compatible FPGAs ✓

Memory Selection ✓

Controller Options ✓

AXI Parameter

Memory Options ✓

FPGA Options ✓

Extended FPGA Options ✓

IO Planning Options ✓

Pin Selection ✓

System Signals Selection ✓

Summary ✓

Simulation Options ✓

PCB Information ✓

Design Notes

DDR3 SDRAM Design for Virtex-7 FPGAs

Design Notes

1. This design is tested with ISE 14.4 version
2. This design is simulated with ModelSim 10.1a version
3. This design is hardware validated for single controller
4. Components, RDIMMs, UDIMMs and SODIMMs are supported
5. If fly by delays are simulated, they must be limited to 1.2ns
6. Consult the Version Info for known limitations

Key Enhancements from MIG 1.7 to MIG 1.8

1. Added support for Verify XDC feature

Key Enhancements from MIG 1.6 to MIG 1.7

1. Support of system clock pin sharing for multi-controller designs

Key Enhancements from MIG 1.5 to MIG 1.6

1. Added support for "No Buffer" option for System Clock and Reference Clock
2. Added support for "Use System Clock" option for Reference Clock when Input Clock Period is 5000 ns

Print

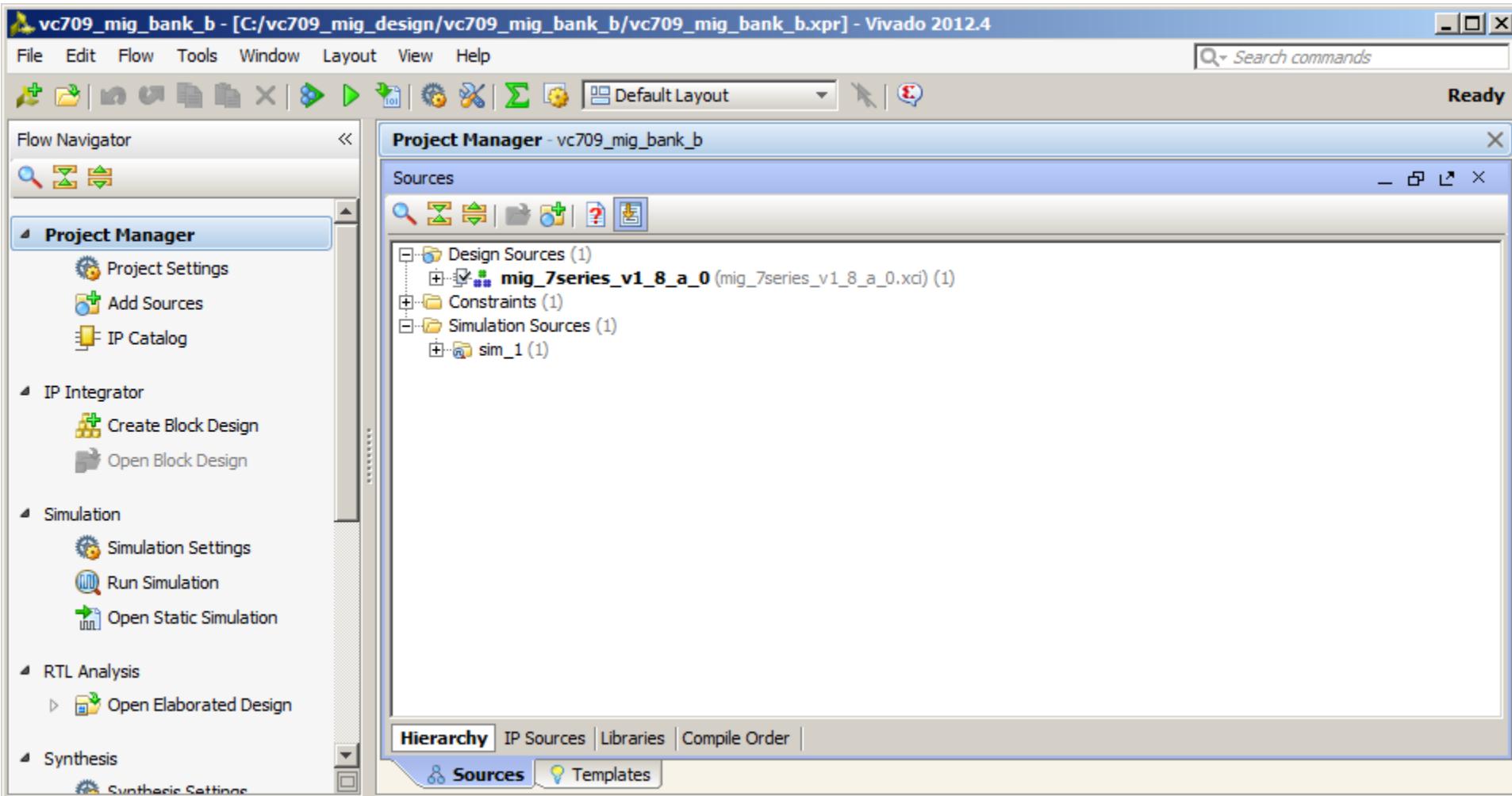
< Back Generate Cancel

XILINX

Click Generate

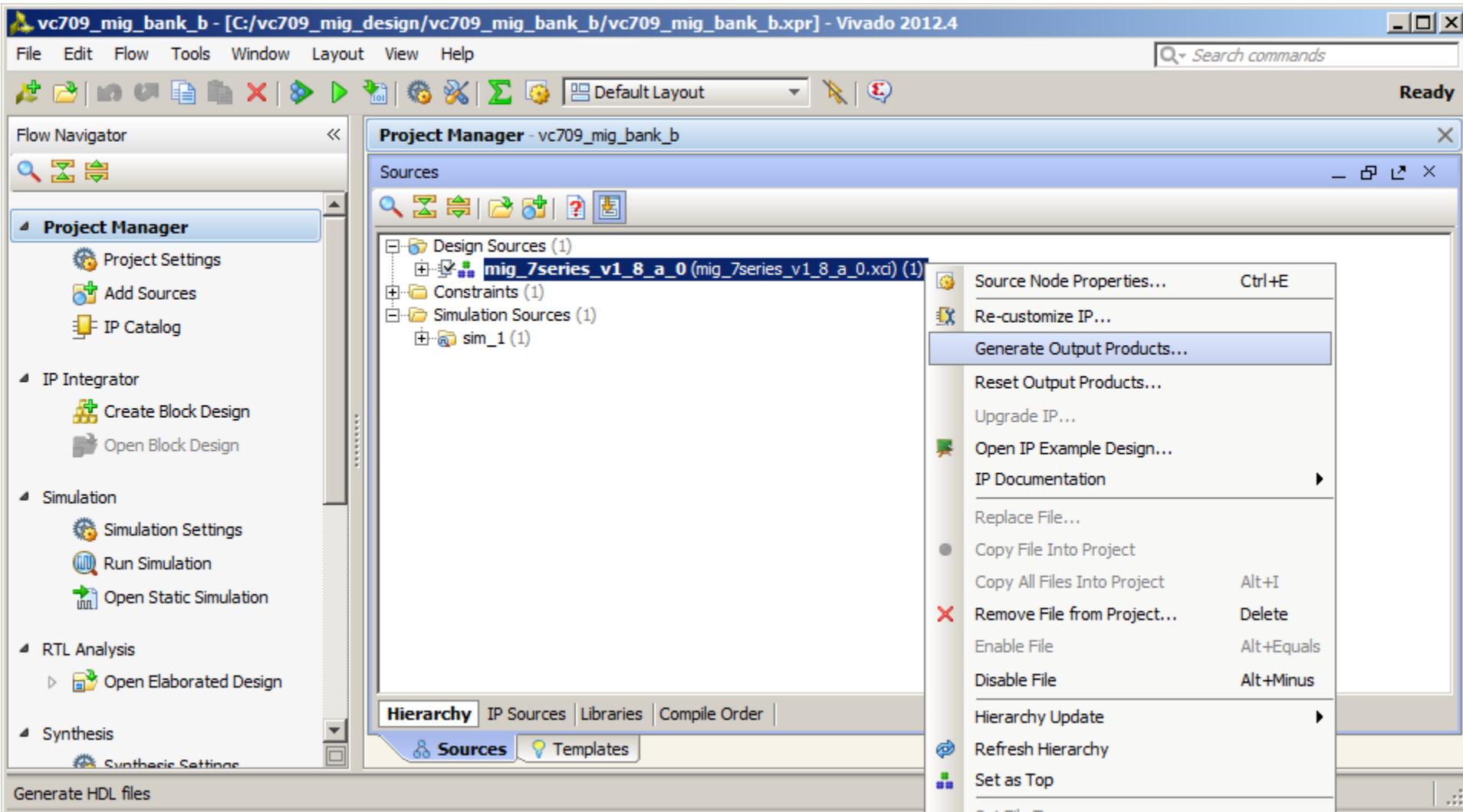
Generate MIG Bank B Example Design

- MIG design appears in Design Sources



Compile MIG Bank B Example Design

- Right-click on mig_7series_v1_8_a_0 and select Generate Output Products...

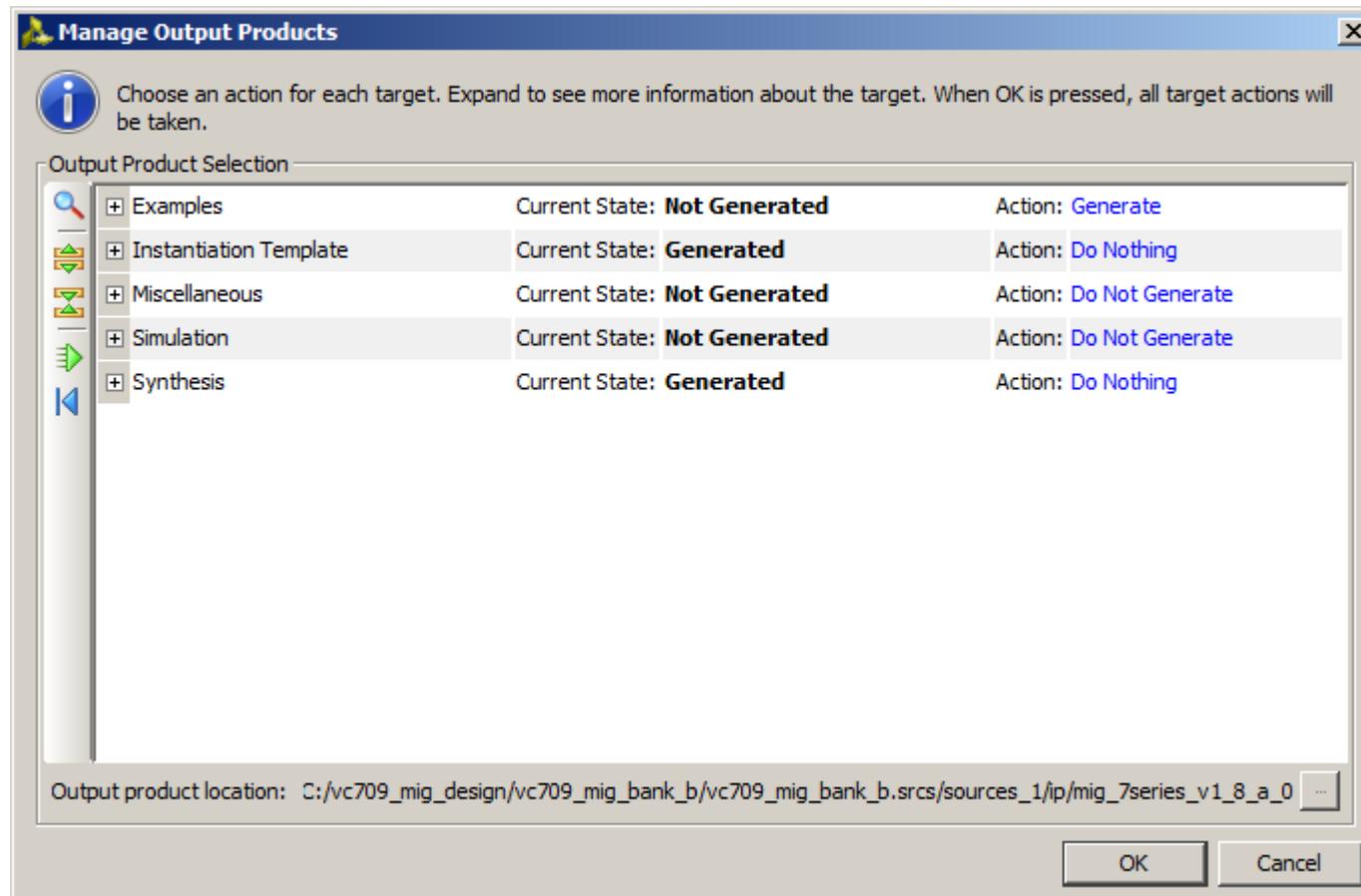


Note: Presentation applies to the VC709

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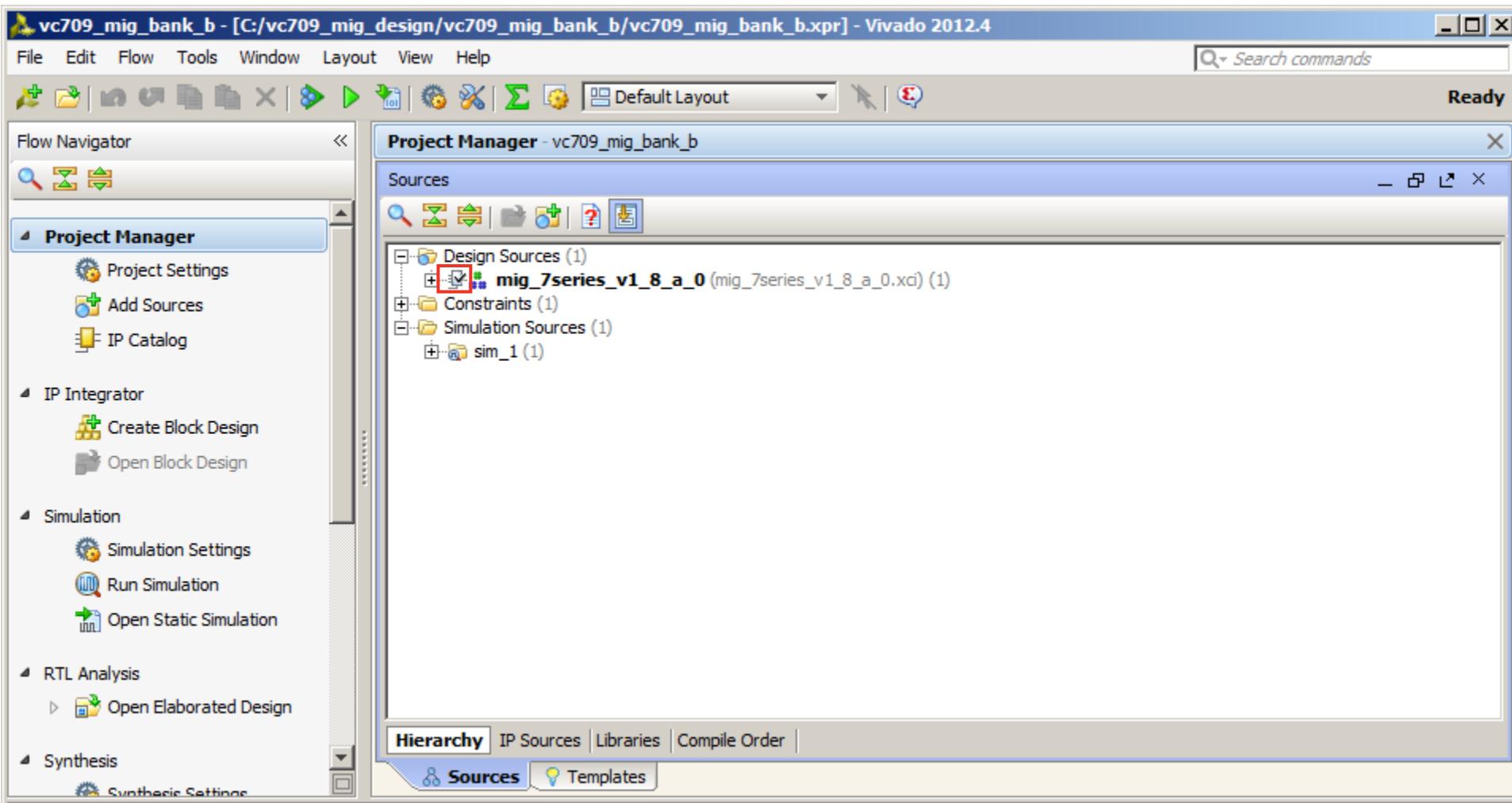
Compile MIG Bank B Example Design

- Select Examples as the target to generate



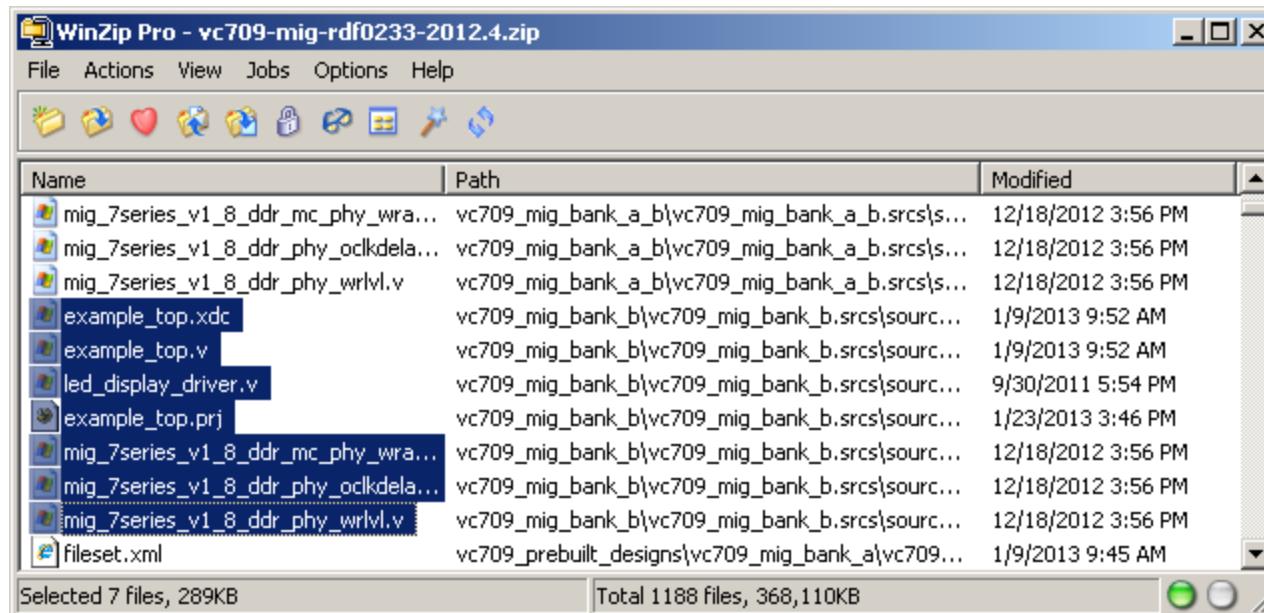
Compile MIG Bank B Example Design

► Once the Generate step is complete, a check (re)appears on the IP



Modifications to MIG Bank B Example Design

- Open the VC709 MIG Design Files (2012.4 CES) and extract these files to your C:\vc709_mig_design directory
 - vc709_mig_bank_b*
 - Contains several changes needed to support Virtex-7 devices with MIG, including [AR53420](#)



Modifications to MIG Bank B Example Design

► Modifications to the example design

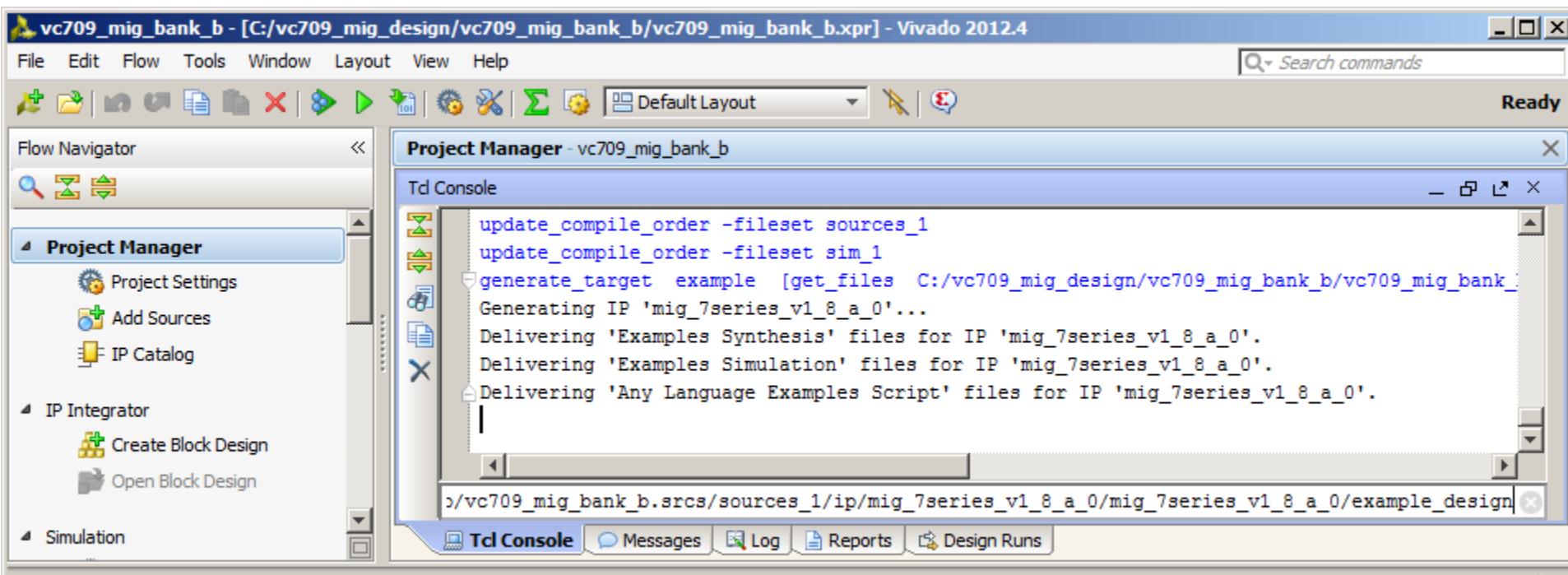
- Added RTL and XDC modifications to drive LEDs
- Changed RST_ACT_LOW to “0”; refer to [UG586](#) for more details on using the RST_ACT_LOW parameter
- Added [AR53420](#) – Required MIG Calibration Patch

Compile MIG Bank B Example Design

► At the Tcl Console enter this command:

```
cd
```

```
C:/vc709_mig_design/vc709_mig_bank_b/vc709_mig_bank_b.srcs/sources_1/ip/mig_7series_v1_8_a_0/mig_7series_v1_8_a_0/example_design/par
```

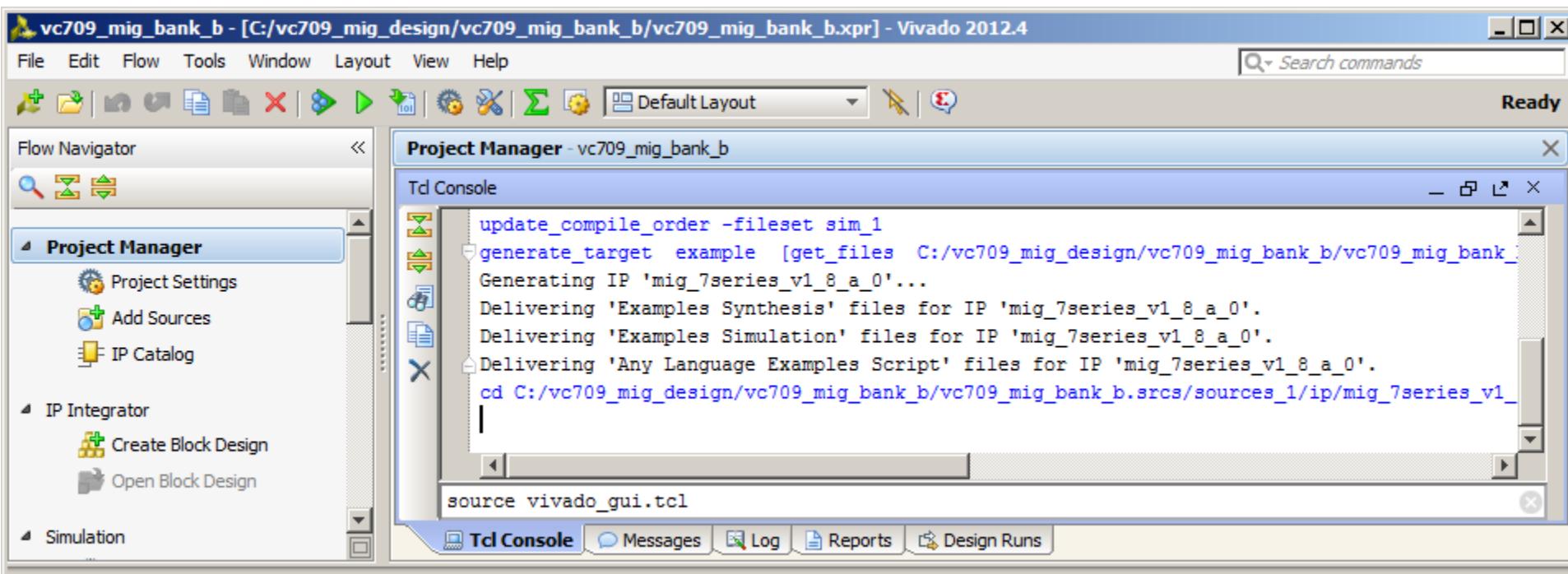


Compile MIG Bank B Example Design

► At the Tcl Console enter this command:

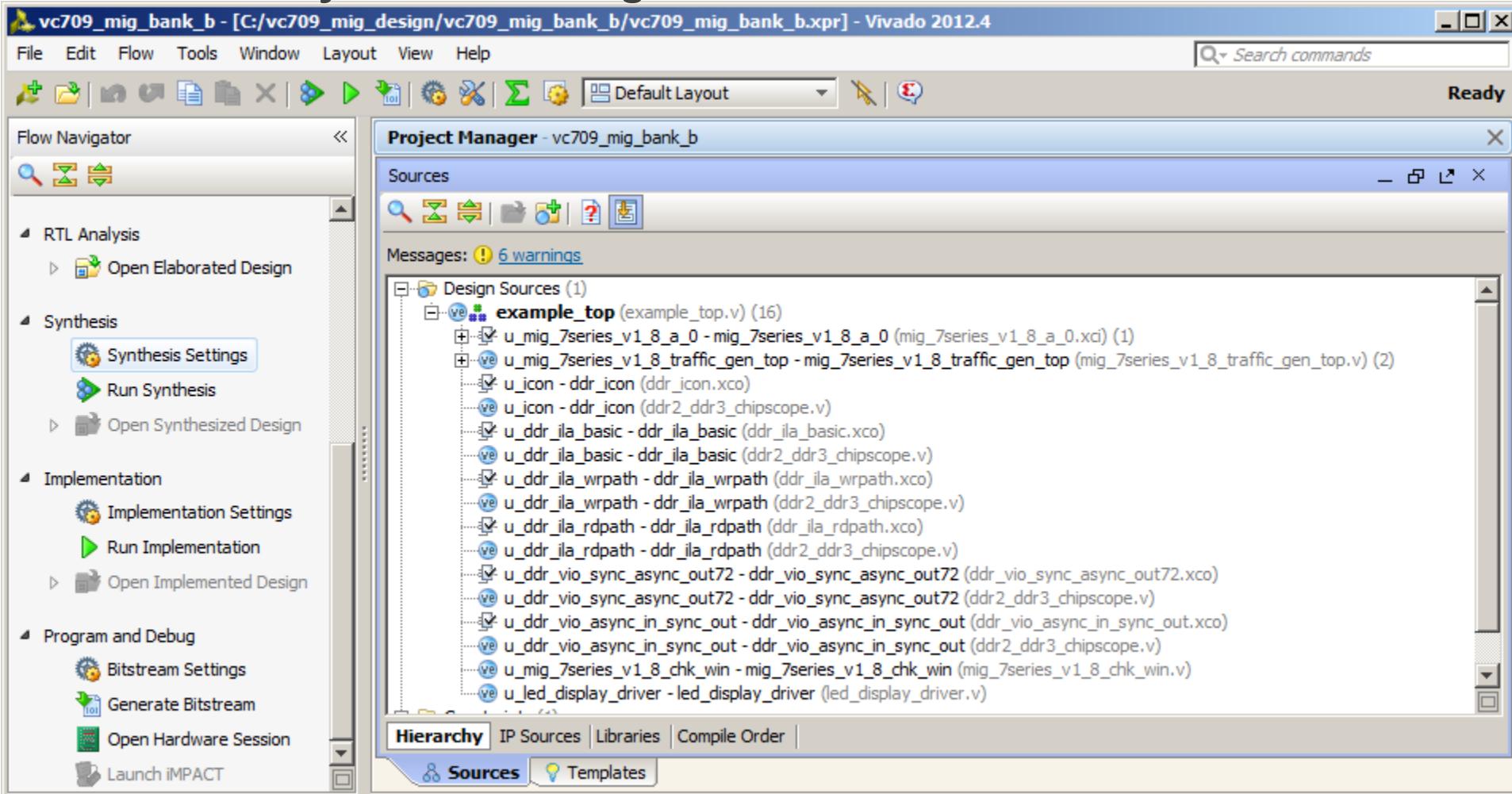
```
source vivado_gui.tcl
```

► This command adds the necessary design files and compiles the ChipScope IP



Compile MIG Bank B Example Design

- The design files, IP and constraints have been added/generated
- Click on Synthesis Settings

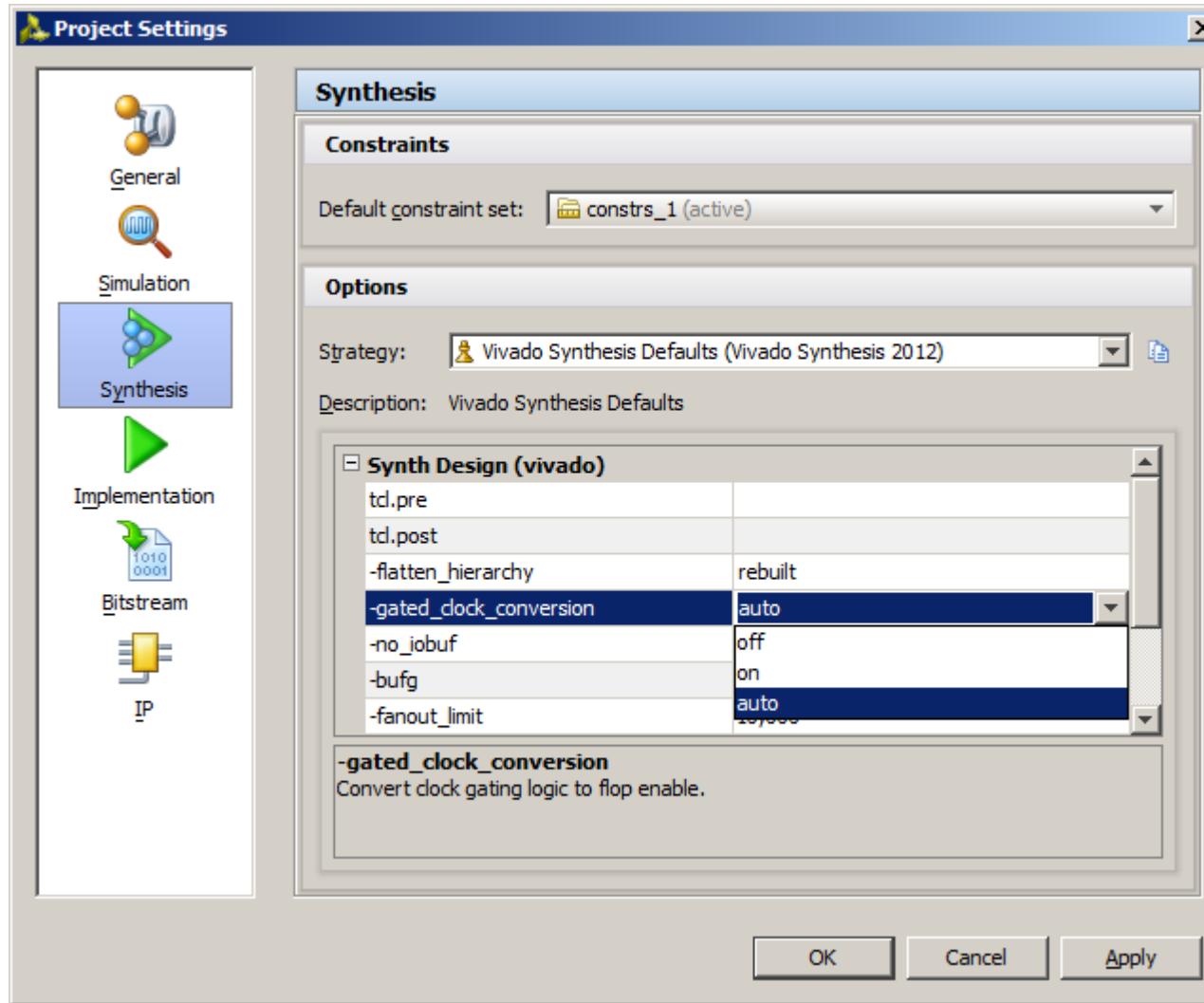


Note: Presentation applies to the VC709

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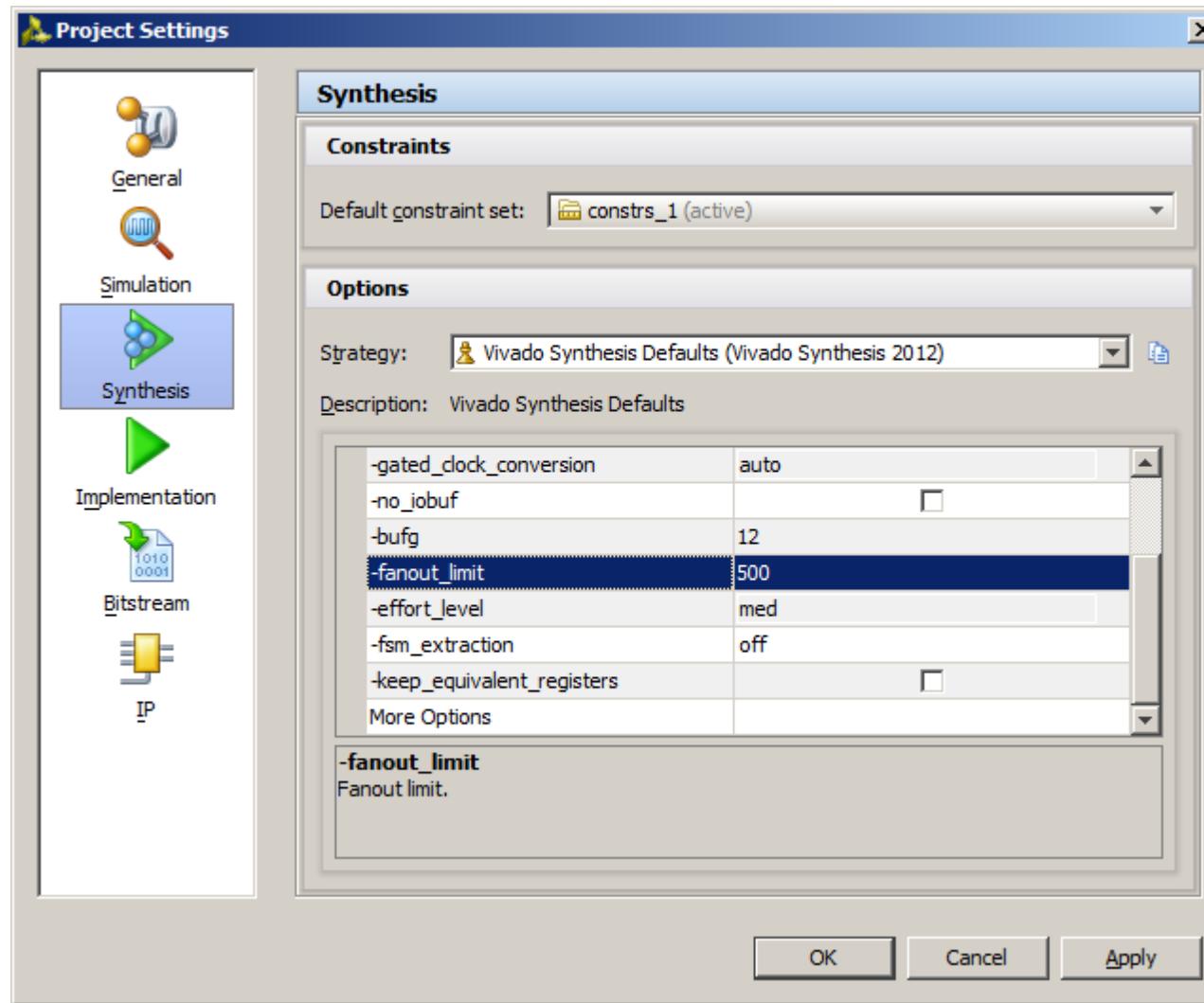
Compile MIG Bank B Example Design

- Set the `gated_clock_conversion` to auto



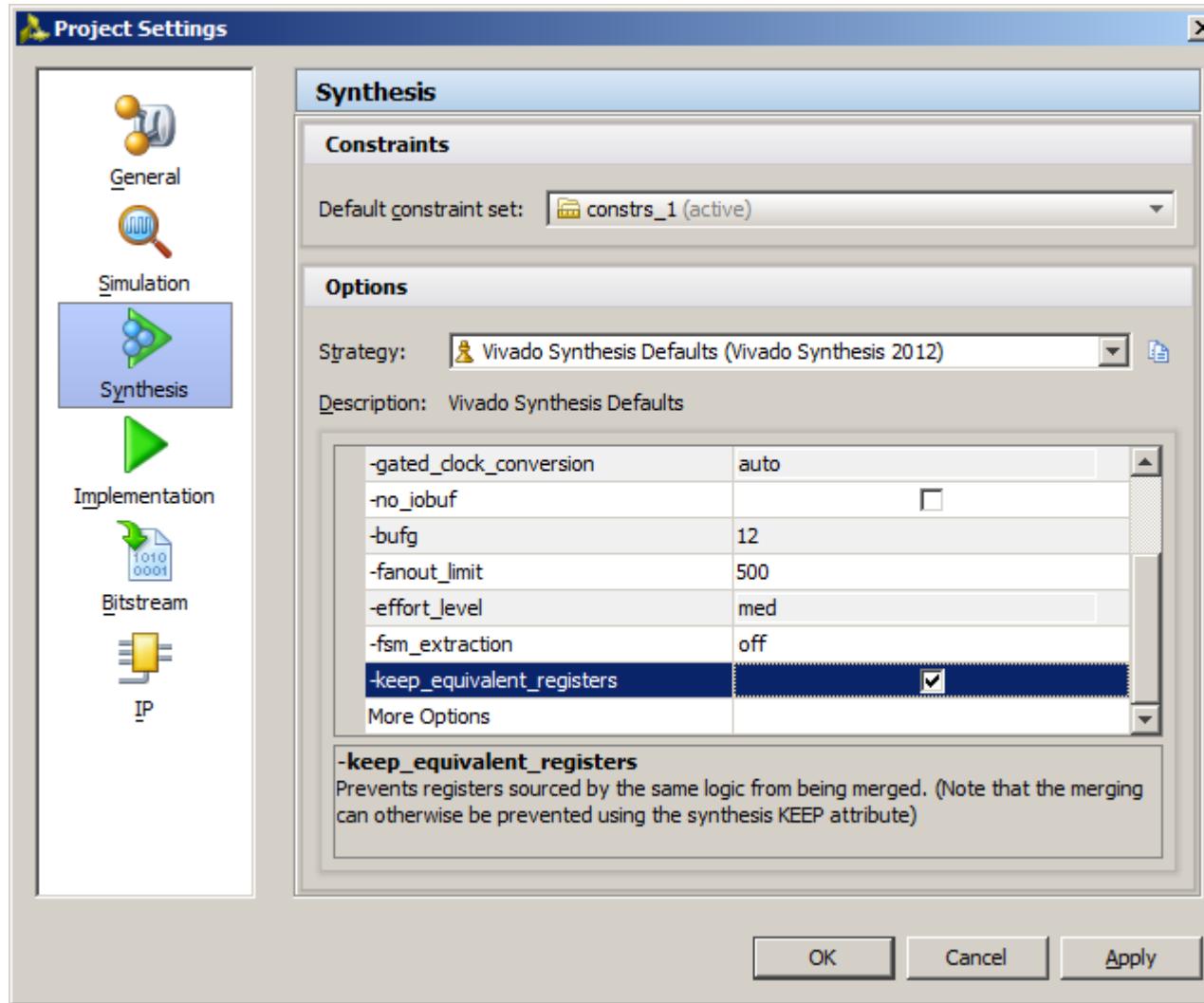
Compile MIG Bank B Example Design

- Set the fanout_limit to 500



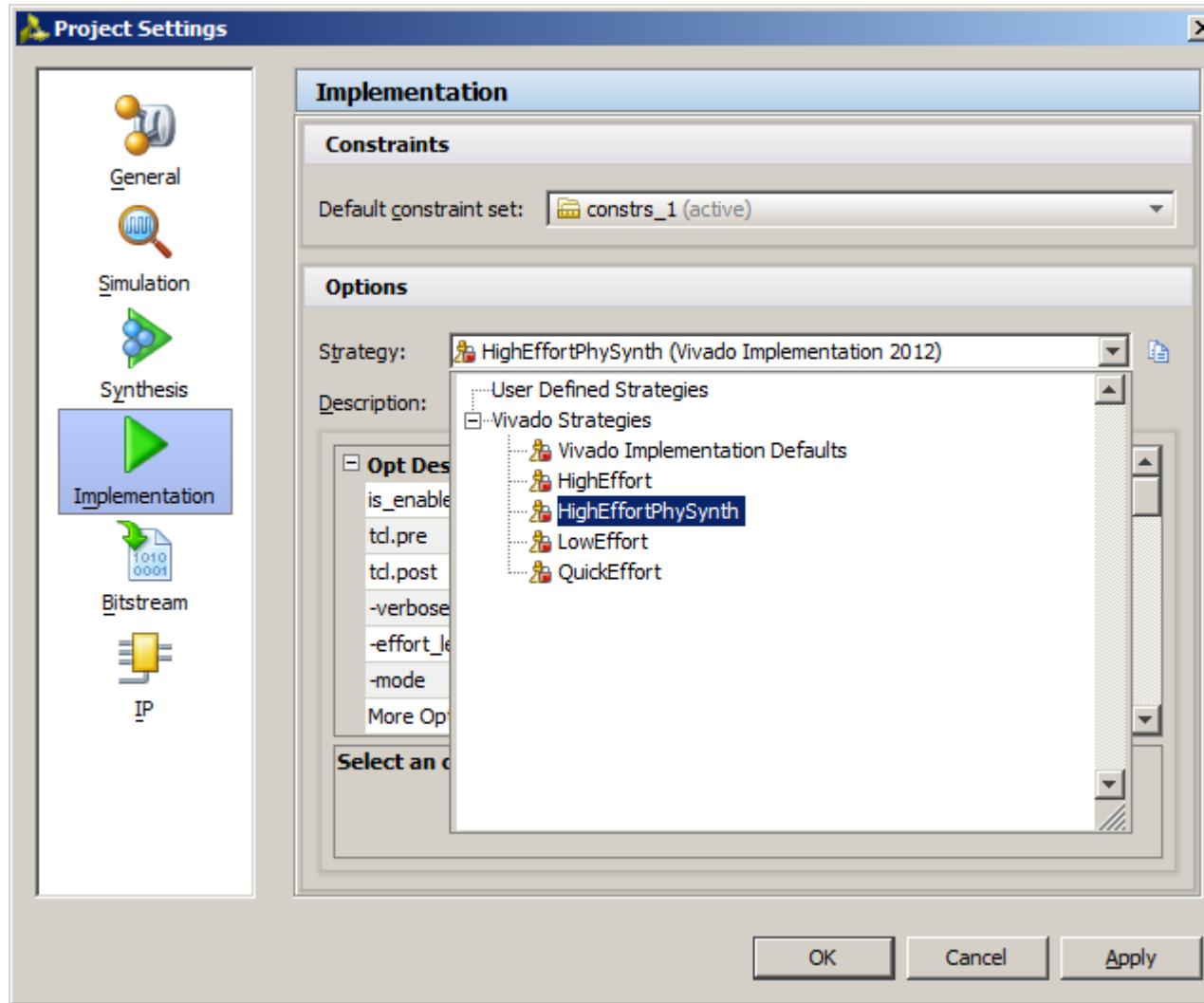
Compile MIG Bank B Example Design

- Check the `keep_equivalent_registers` option



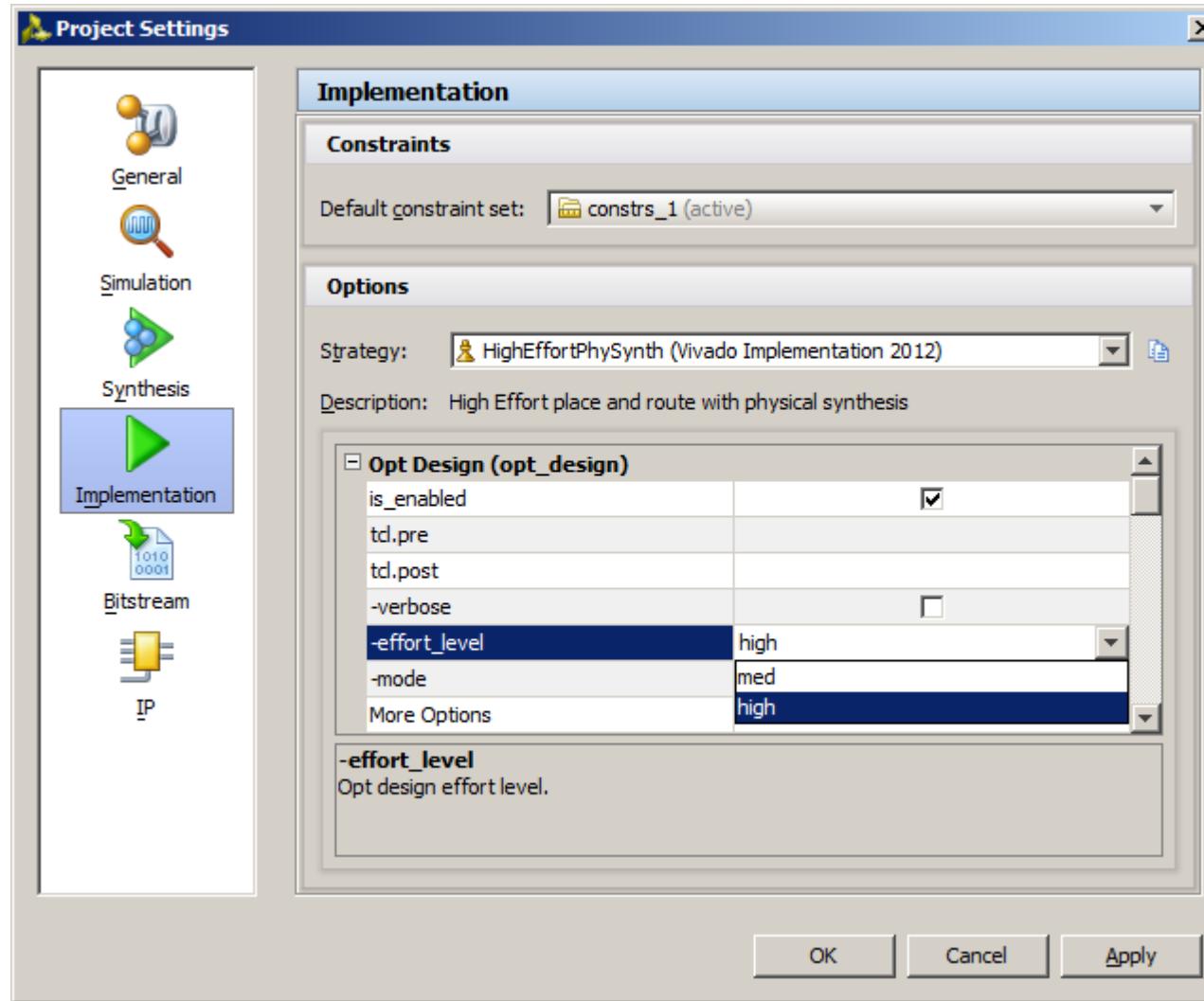
Compile MIG Bank B Example Design

► Select Implementation and select HighEffortPhySynth



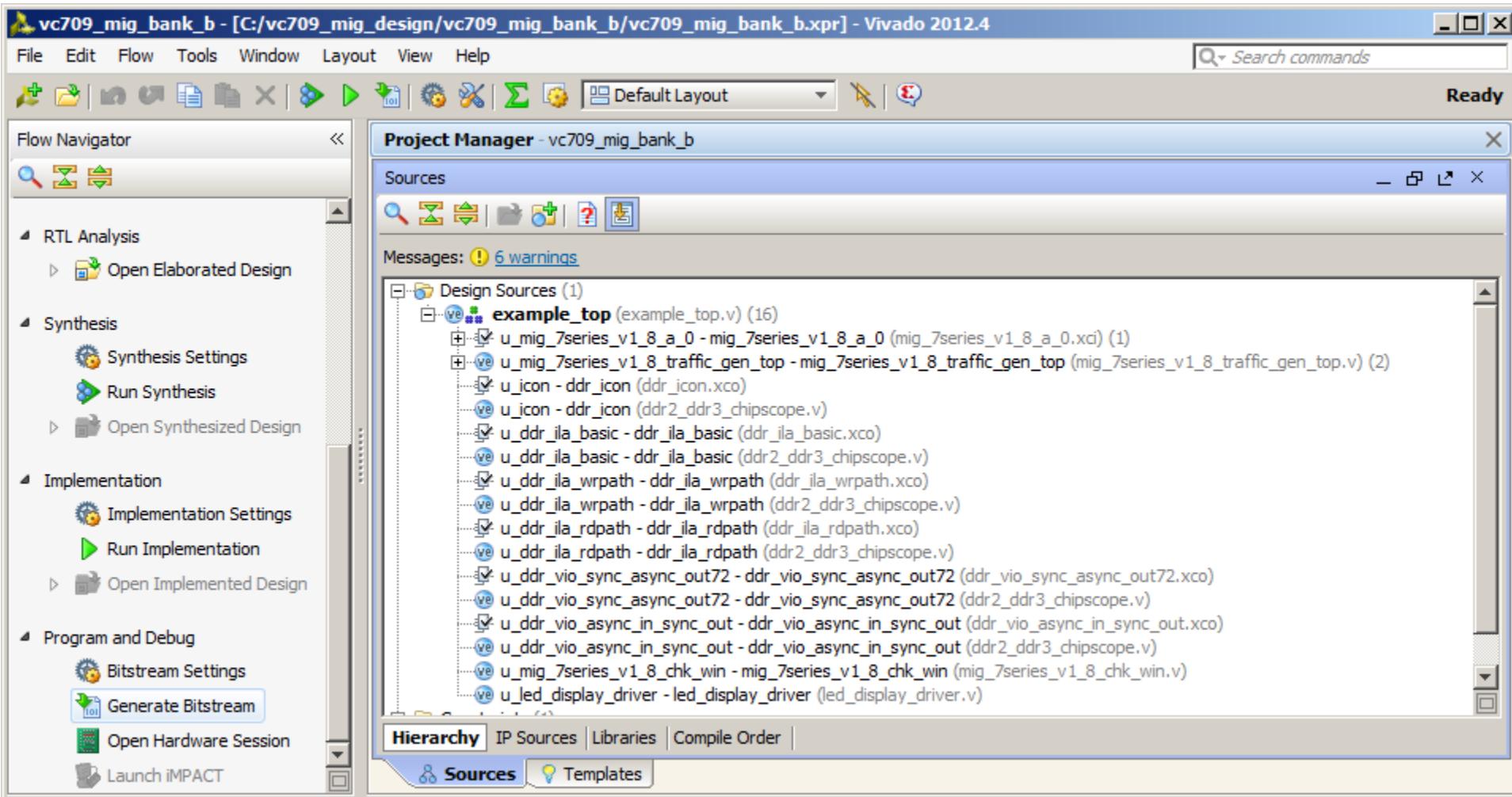
Compile MIG Bank B Example Design

► Under Opt Design set effort_level to high; set mode to area



Compile MIG Bank B Example Design

► Click on Generate Bitstream



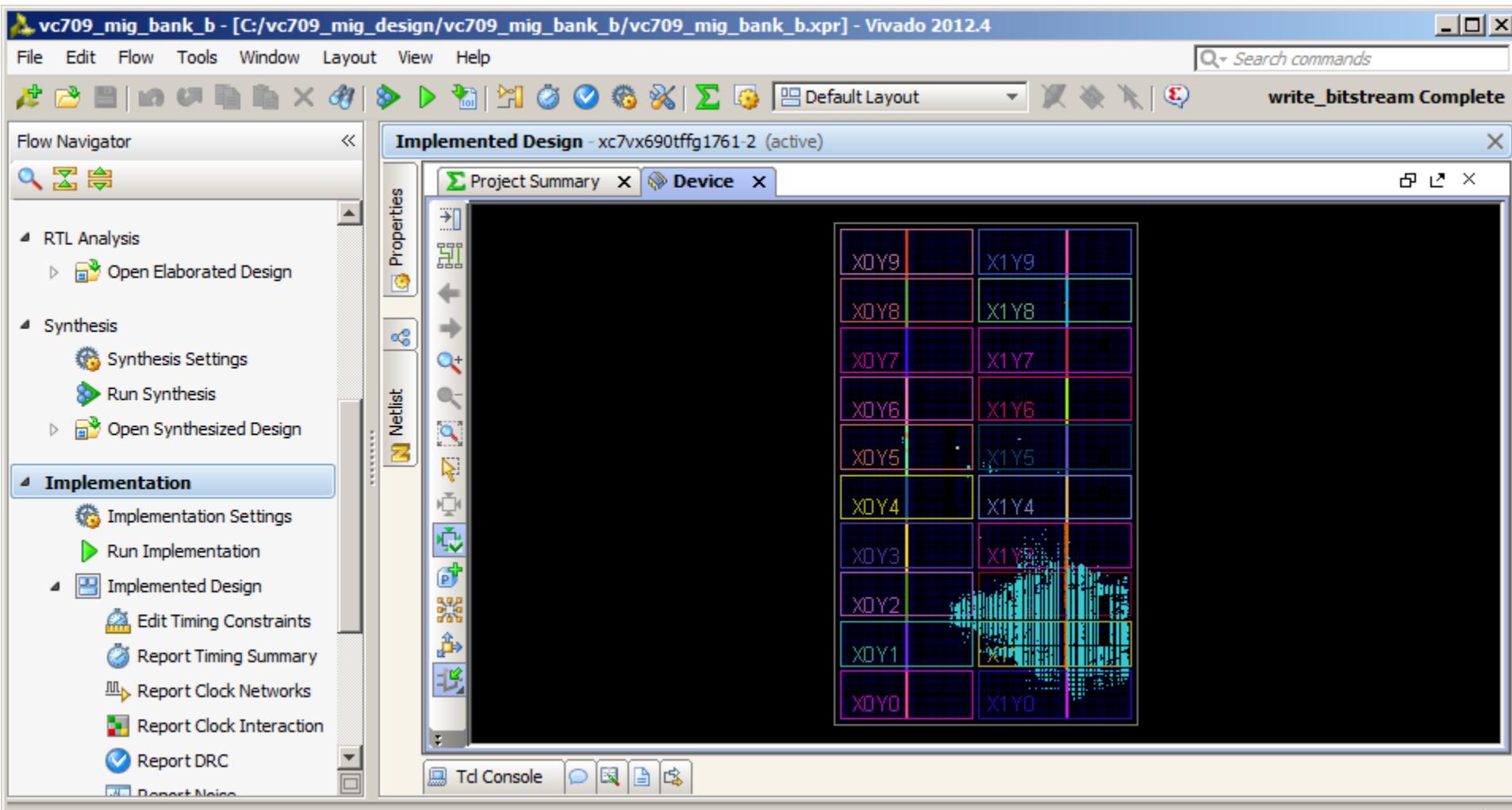
Generate a programming file after implementation.

Note: Presentation applies to the VC709

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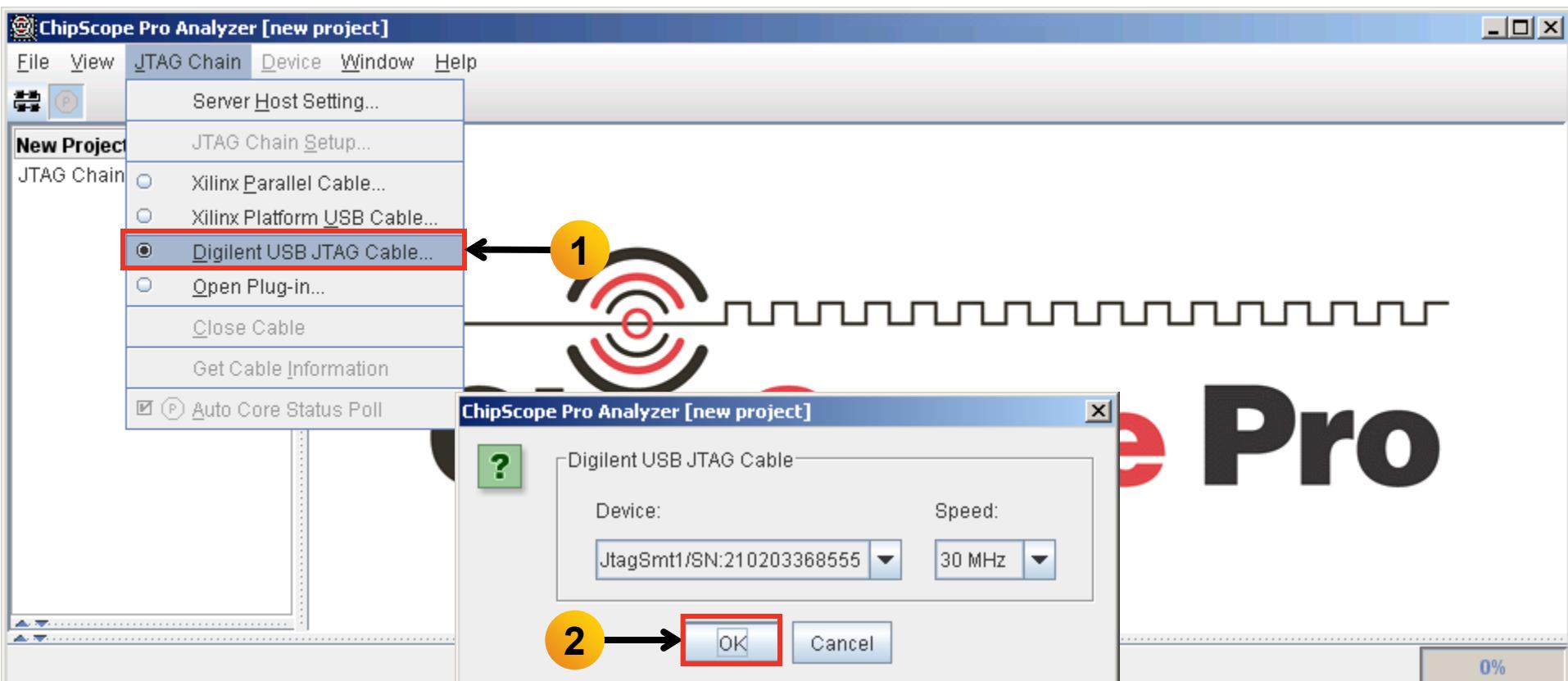
Compile MIG Bank B Example Design

► Open and view the completed design



Run MIG Bank B Example Design

- Open ChipScope Pro and select JTAG Chain → Digilent USB Cable... (1)
- Verify 30 MHz operation and click OK (2)



Run MIG Bank B Example Design

► Click OK (1)

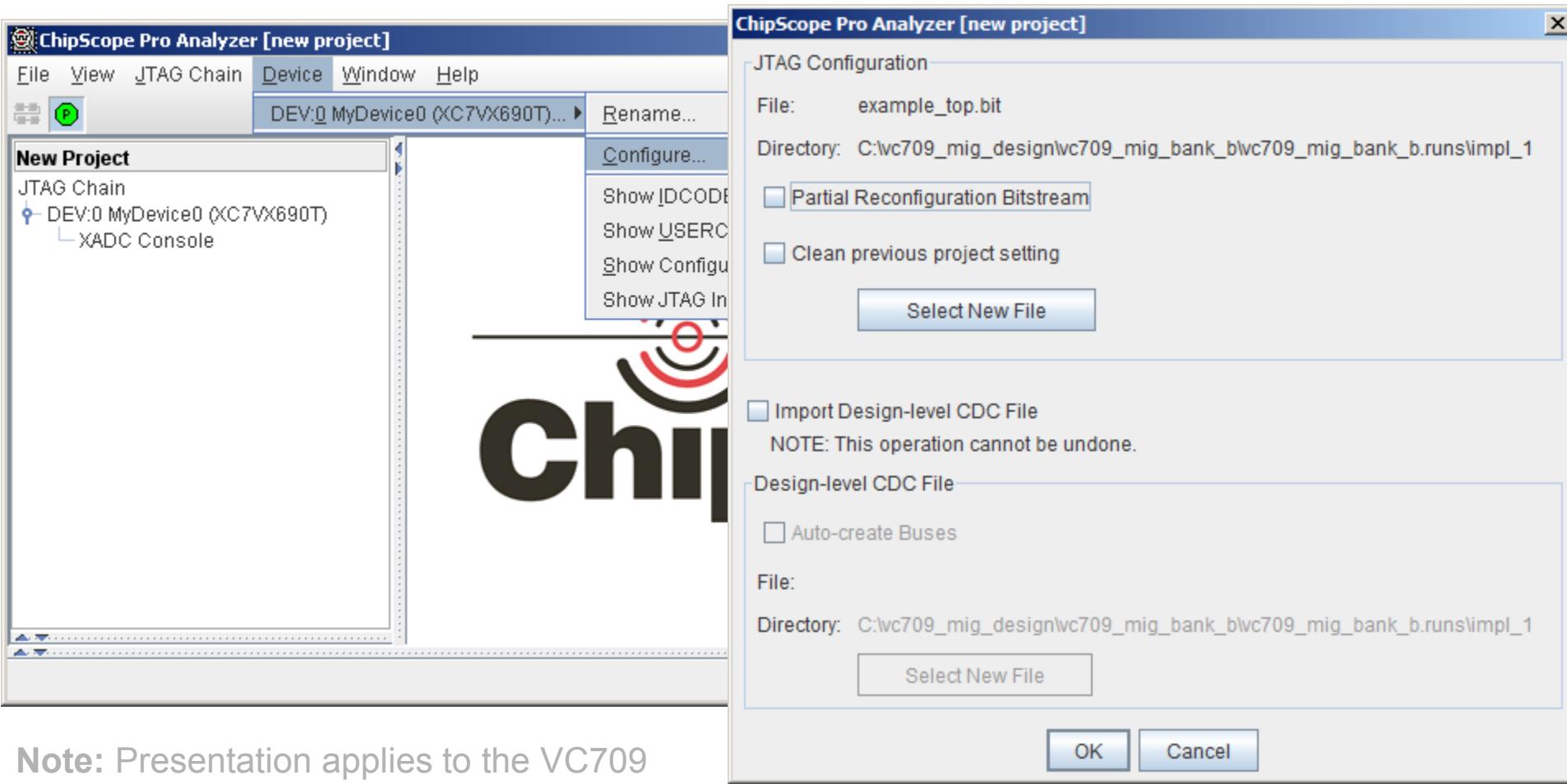


Run MIG Bank B Example Design

► Select Device → DEV:0 MyDevice0 (XC7VX690T) → Configure...

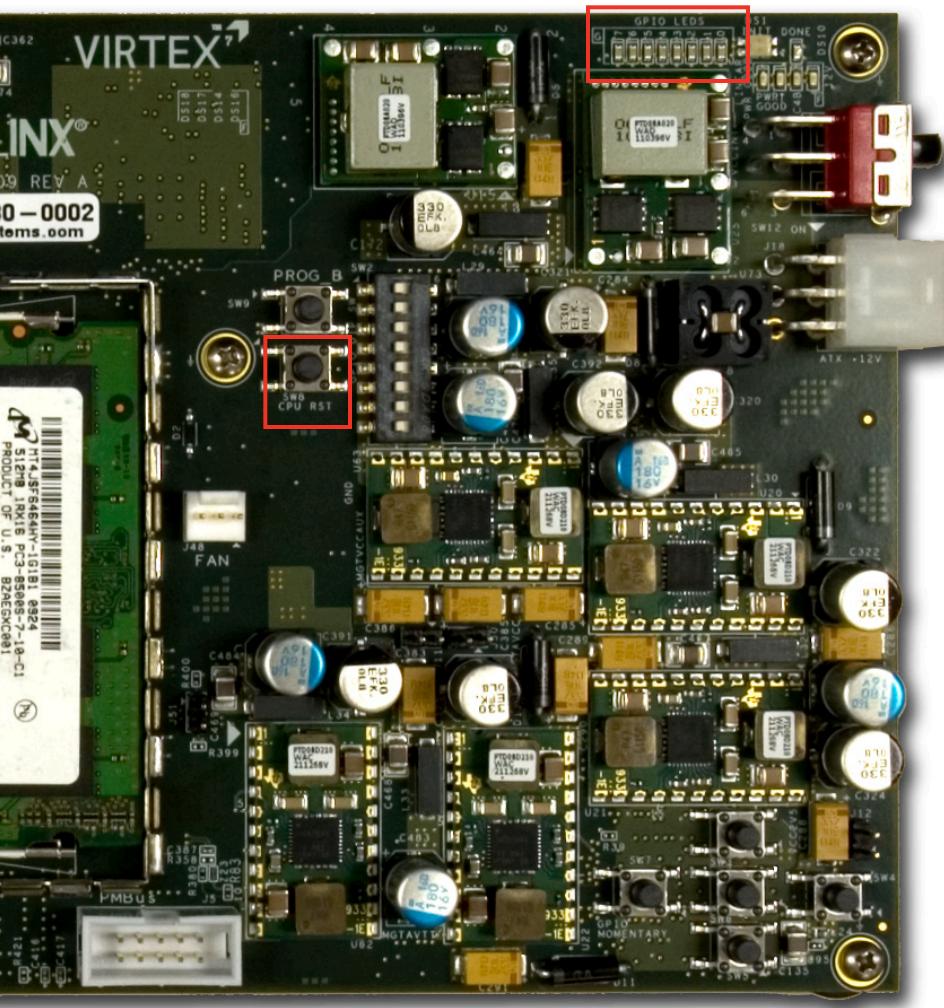
► Select <Design

Path>\vc709_mig_bank_b\vc709_mig_bank_b.runs\impl_1\example_top.bit



Note: Presentation applies to the VC709

Run MIG Bank B Example Design



- After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking
- LED 3 will light and stay on
 - This indicates Calibration has completed
- If an error occurs, LED 0 will go out and LED 2 will light
- SW8 is the reset

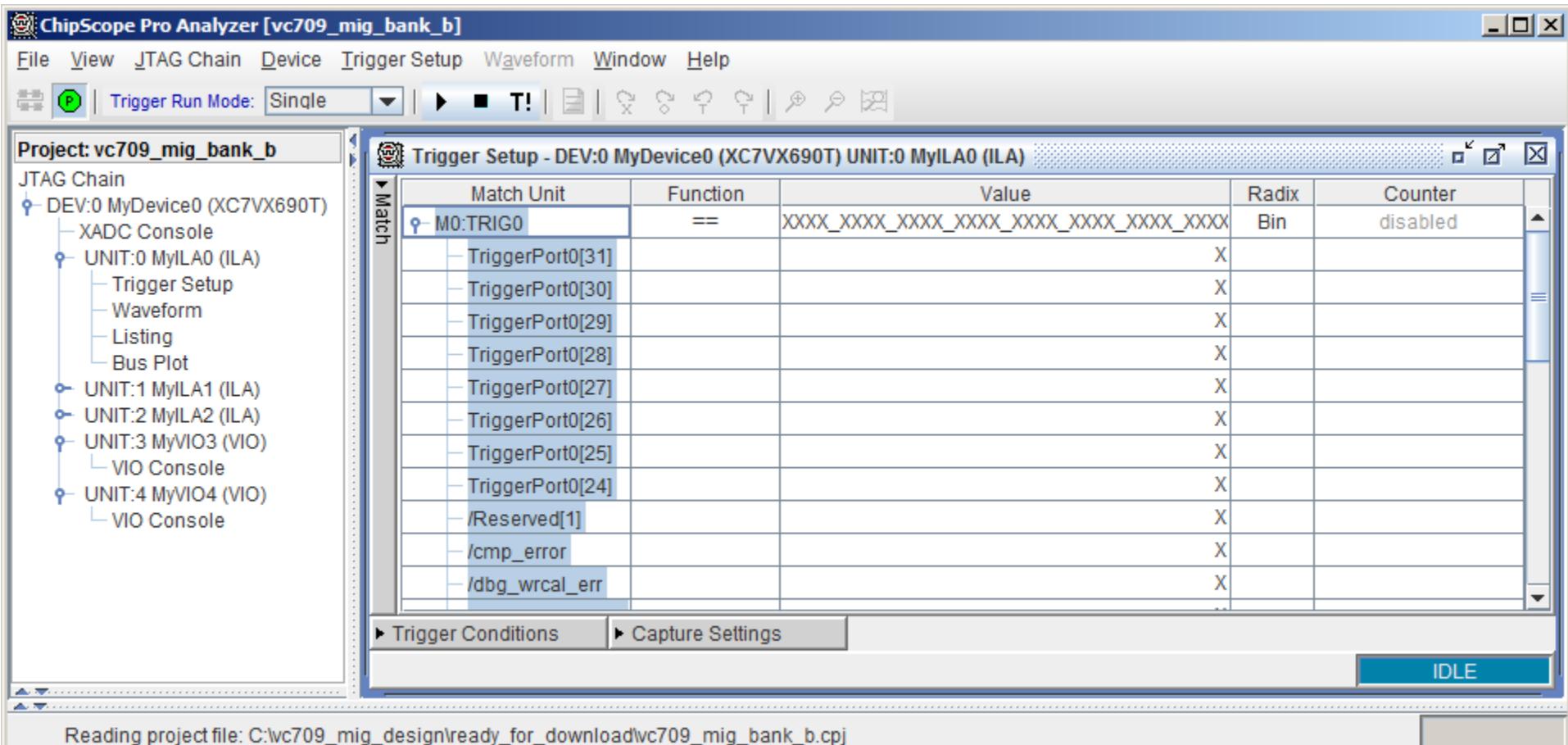
Run MIG Bank B Example Design

- Select File → Open Project...
- Select <Design Path>\ready_for_download\vc709_mig_bank_b.cpj



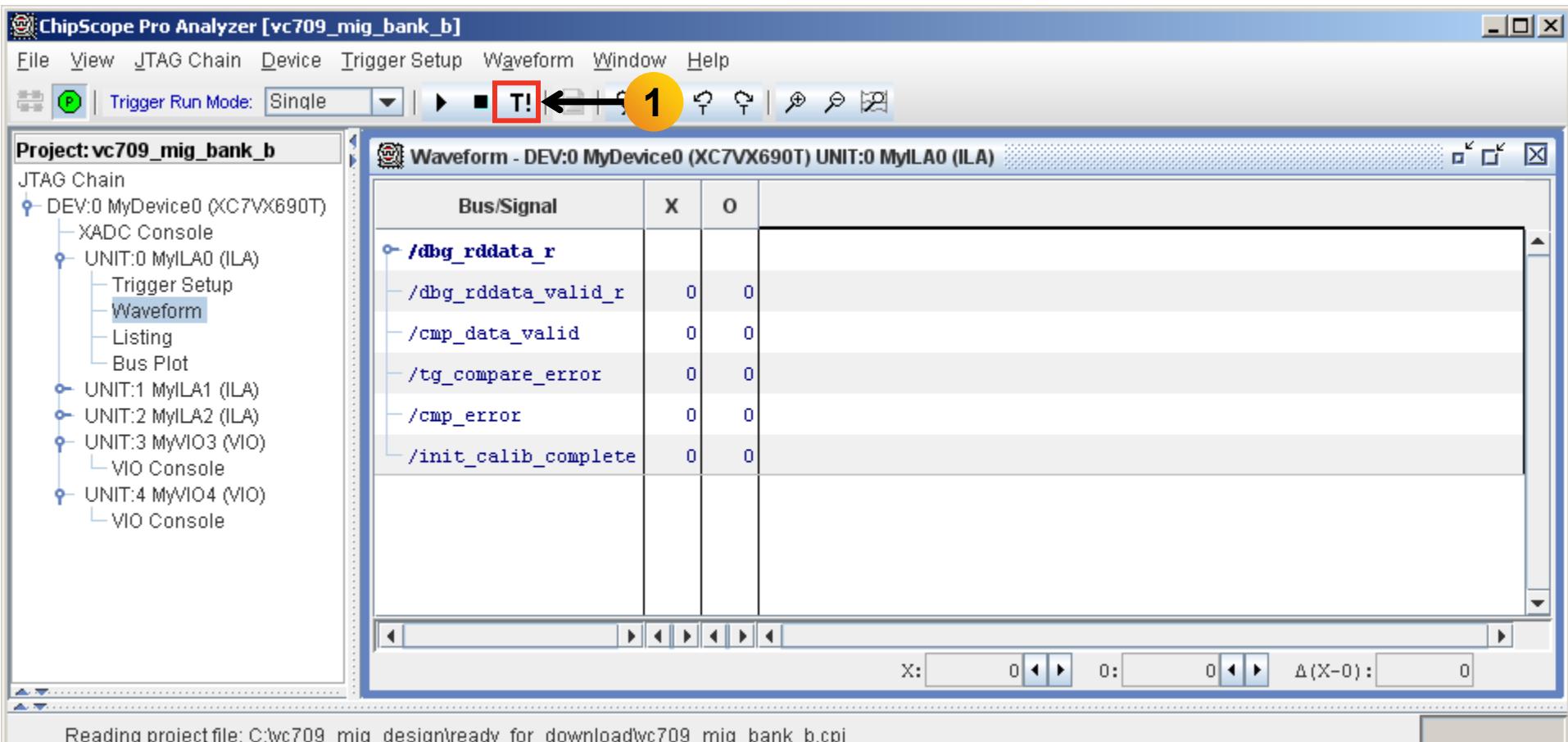
Run MIG Bank B Example Design

► Click on Trigger Setup to view trigger settings



Run MIG Bank B Example Design

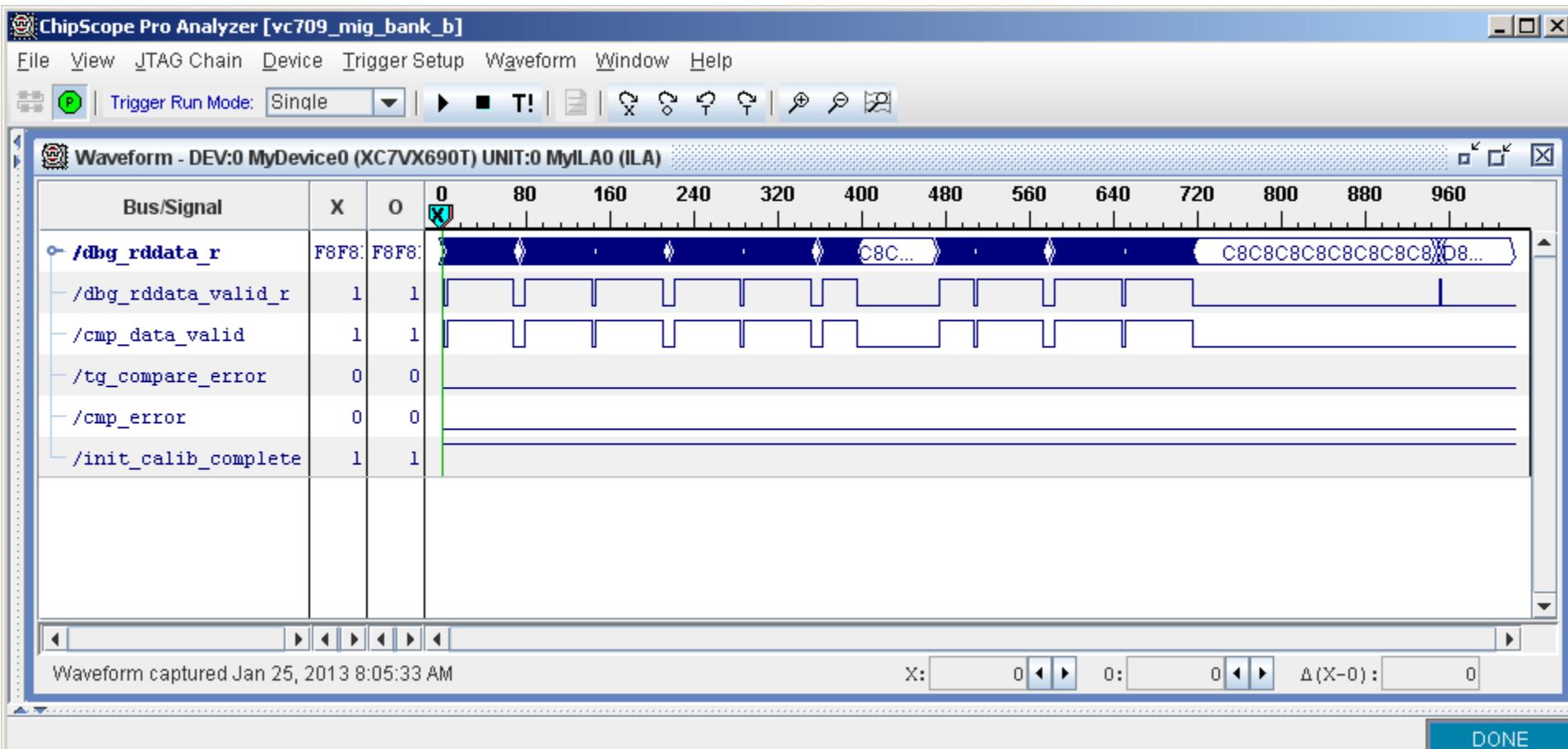
► Click on Waveform; click the Trigger Immediate button (1)



Reading project file: C:\vc709_mig_design\ready_for_download\vc709_mig_bank_b.cpj

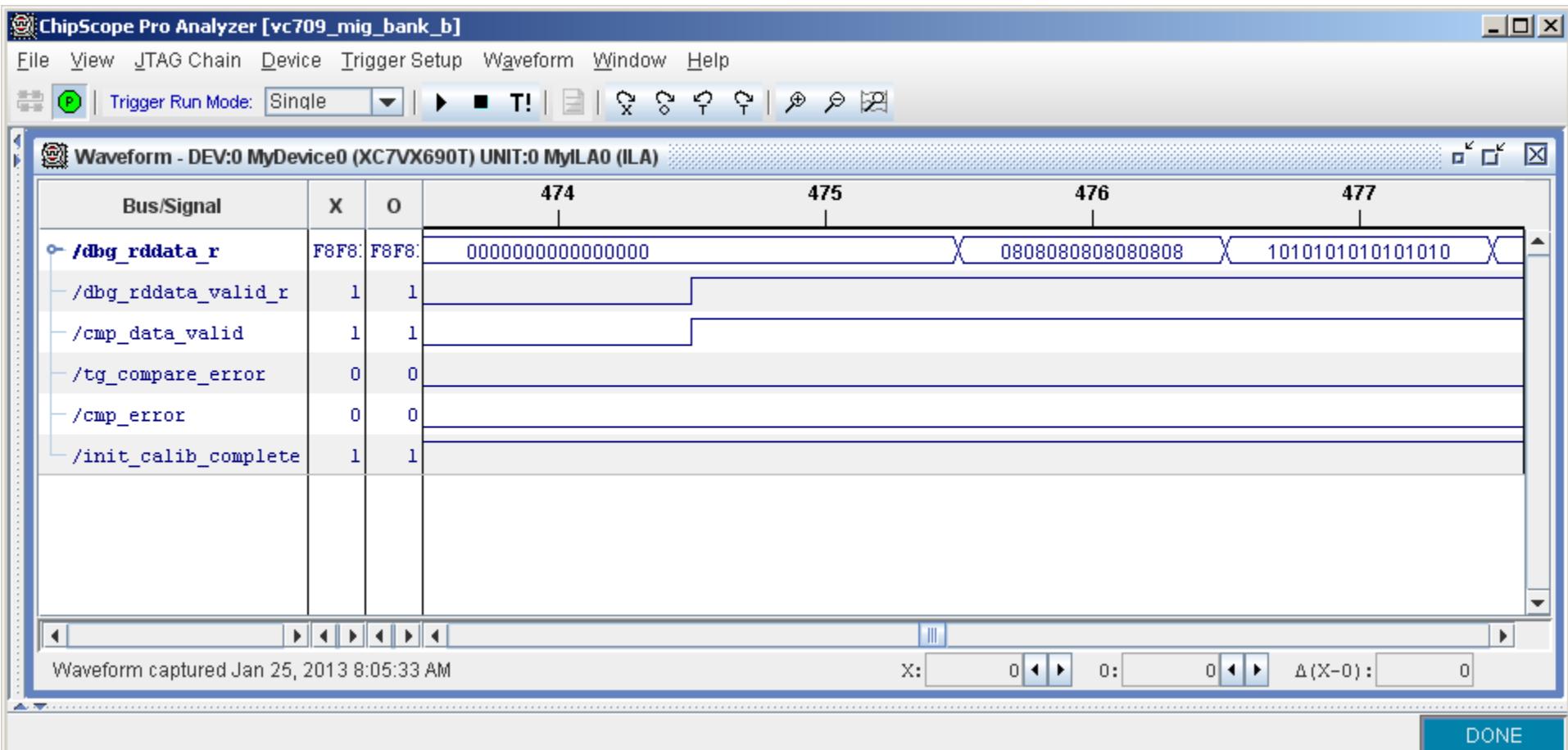
Run MIG Bank B Example Design

- View waveforms
- Data is valid when `dbg_rddata_valid` is high



Run MIG Bank B Example Design

► Zoom in to view data



Adjust Data Pattern using VIO Console

- Select VIO Console 3
- Set `vio_modify_enable` to 1

The screenshot shows the ChipScope Pro Analyzer interface with the project "vc709_mig_bank_b" open. The left sidebar displays the JTAG Chain structure, including DEV:0 MyDevice0 (XC7VX690T), UNIT:0 MyILAO (ILA), UNIT:1 MyILA1 (ILA), UNIT:2 MyILA2 (ILA), UNIT:3 MyVIO3 (VIO) which is selected and highlighted in blue, and UNIT:4 MyVIO4 (VIO). The main window shows the "VIO Console - DEV:0 MyDevice0 (XC7VX690T) UNIT:3 MyVIO3 (VIO)" configuration table. The table has two columns: "Bus/Signal" and "Value". The "vio_modify_enable" signal is set to 1, which is highlighted with a red box. Other signals listed include vio_data_mask_gen, vio_pause_traffic, dbg_clear_error, vio_addr_mode_value (value 3), vio_b1_mode_value (value 2), vio_fixed_b1_value (value 16), vio_fixed_instr_value (value 1), vio_instr_mode_value (value 2), and vio_data_mode_value (value 2).

Bus/Signal	Value
<code>vio_modify_enable</code>	1
<code>vio_data_mask_gen</code>	0
<code>vio_pause_traffic</code>	0
<code>dbg_clear_error</code>	0
<code>vio_addr_mode_value</code>	3
<code>vio_b1_mode_value</code>	2
<code>vio_fixed_b1_value</code>	16
<code>vio_fixed_instr_value</code>	1
<code>vio_instr_mode_value</code>	2
<code>vio_data_mode_value</code>	2

Adjust Data Pattern using VIO Console

- Set `vio_data_mode_value` to “7” for `PRBS_DATA`

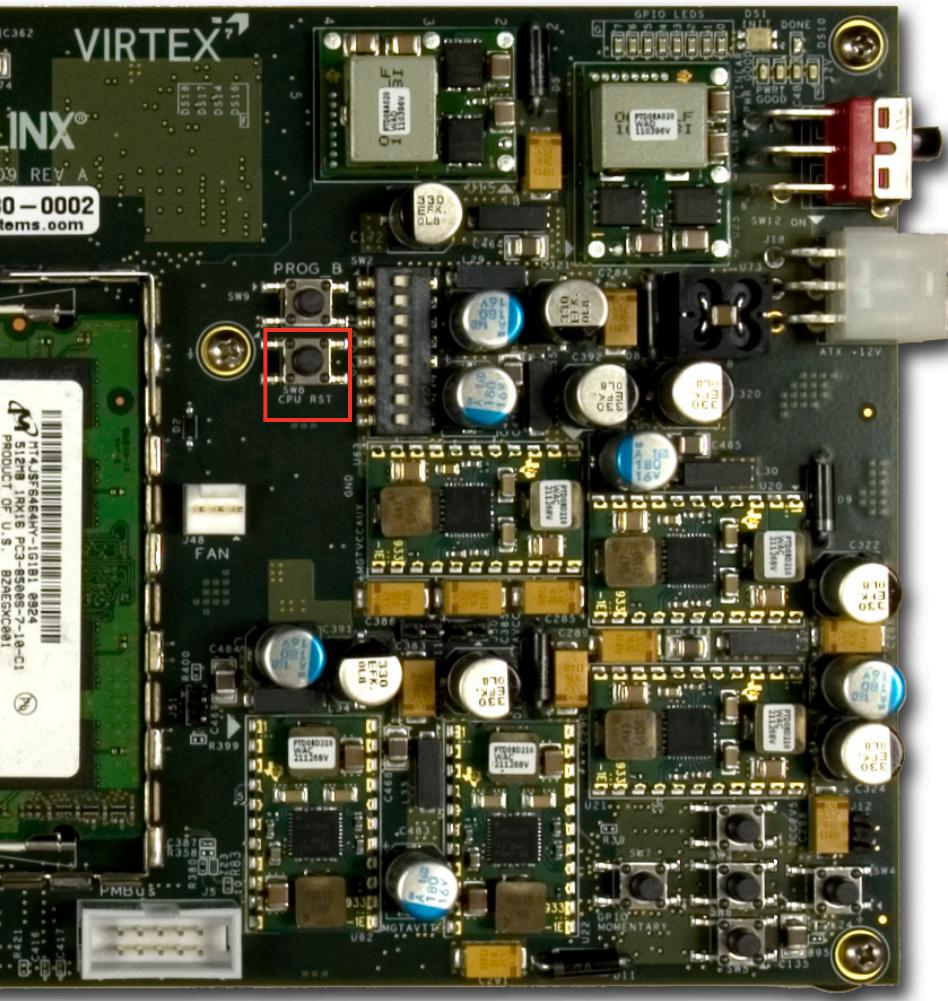
The screenshot shows the ChipScope Pro Analyzer interface with the title bar "ChipScope Pro Analyzer [vc709_mig_bank_b]". The menu bar includes File, View, JTAG Chain, Device, VIO, Window, and Help. The toolbar has icons for JTAG Scan Rate (250 ms), S!, U!, and a red asterisk. The left sidebar displays the project structure under "Project: vc709_mig_bank_b": JTAG Chain, DEV:0 MyDevice0 (XC7VX690T), XADC Console, UNIT:0 MyILA0 (ILA), Trigger Setup, Waveform, Listing, Bus Plot, UNIT:1 MyILA1 (ILA), UNIT:2 MyILA2 (ILA), UNIT:3 MyVIO3 (VIO) (selected), VIO Console, and UNIT:4 MyVIO4 (VIO). The main window is titled "VIO Console - DEV:0 MyDevice0 (XC7VX690T) UNIT:3 MyVIO3 (VIO)". It contains a table with columns "Bus/Signal" and "Value". The table rows are:

Bus/Signal	Value
<code>vio_modify_enable</code>	1
<code>vio_data_mask_gen</code>	0
<code>vio_pause_traffic</code>	0
<code>dbg_clear_error</code>	0
<code>vio_addr_mode_value</code>	3
<code>vio.bl_mode_value</code>	2
<code>vio.fixed.bl_value</code>	16
<code>vio.fixed.instr_value</code>	1
<code>vio.instr_mode_value</code>	2
<code>vio.data_mode_value</code>	7

A "DONE" button is at the bottom right.

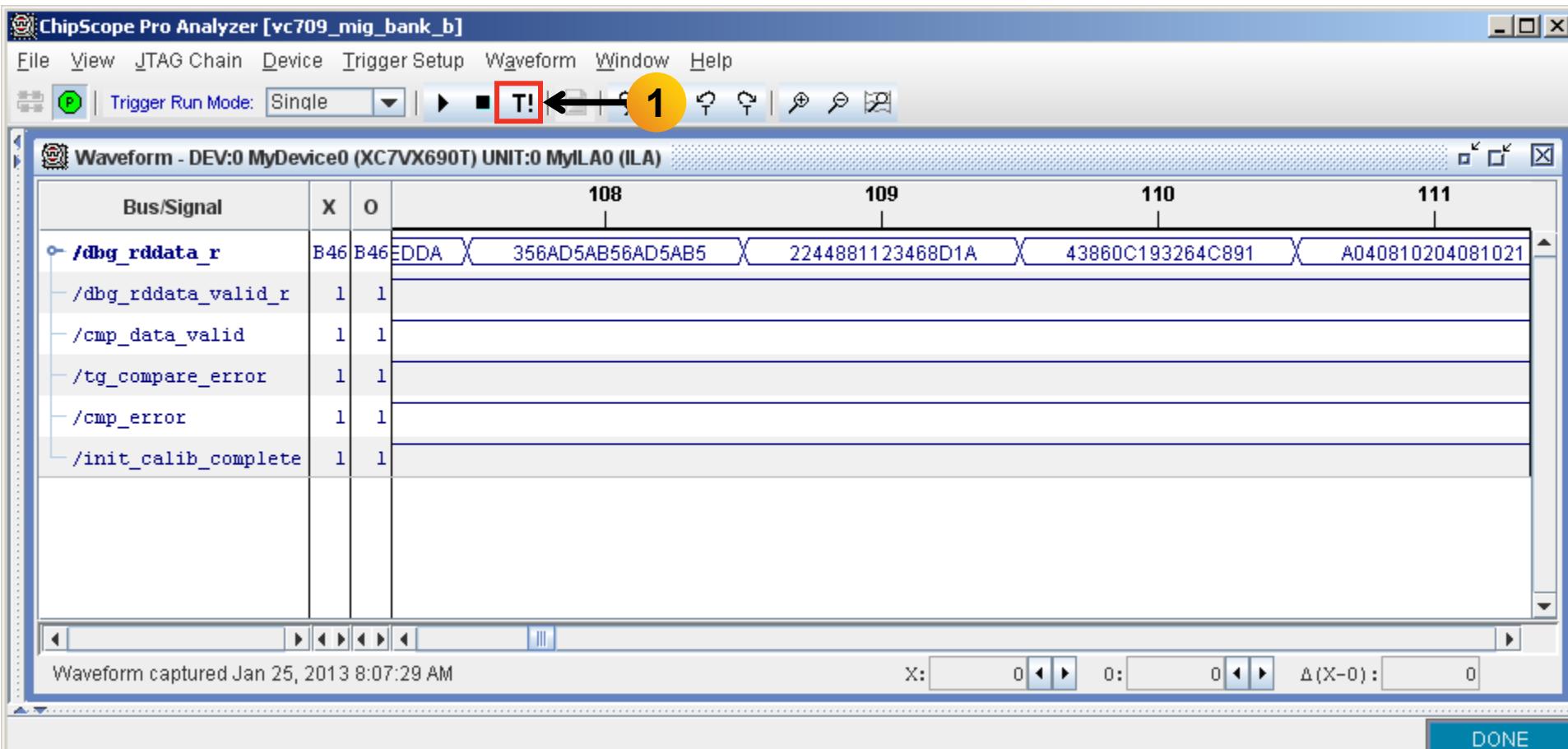
Run MIG Bank B Example Design

► Press and release the CPU RESET switch, SW8, after each change to vio_modify_enable or vio_data_mode_value



Run MIG Bank B Example Design

- Click on Waveform; click the Trigger Immediate button (1)
- View PRBS data



Generate MIG Bank A and B Example Design

Generate MIG Bank A and B Example Design

► Open Vivado

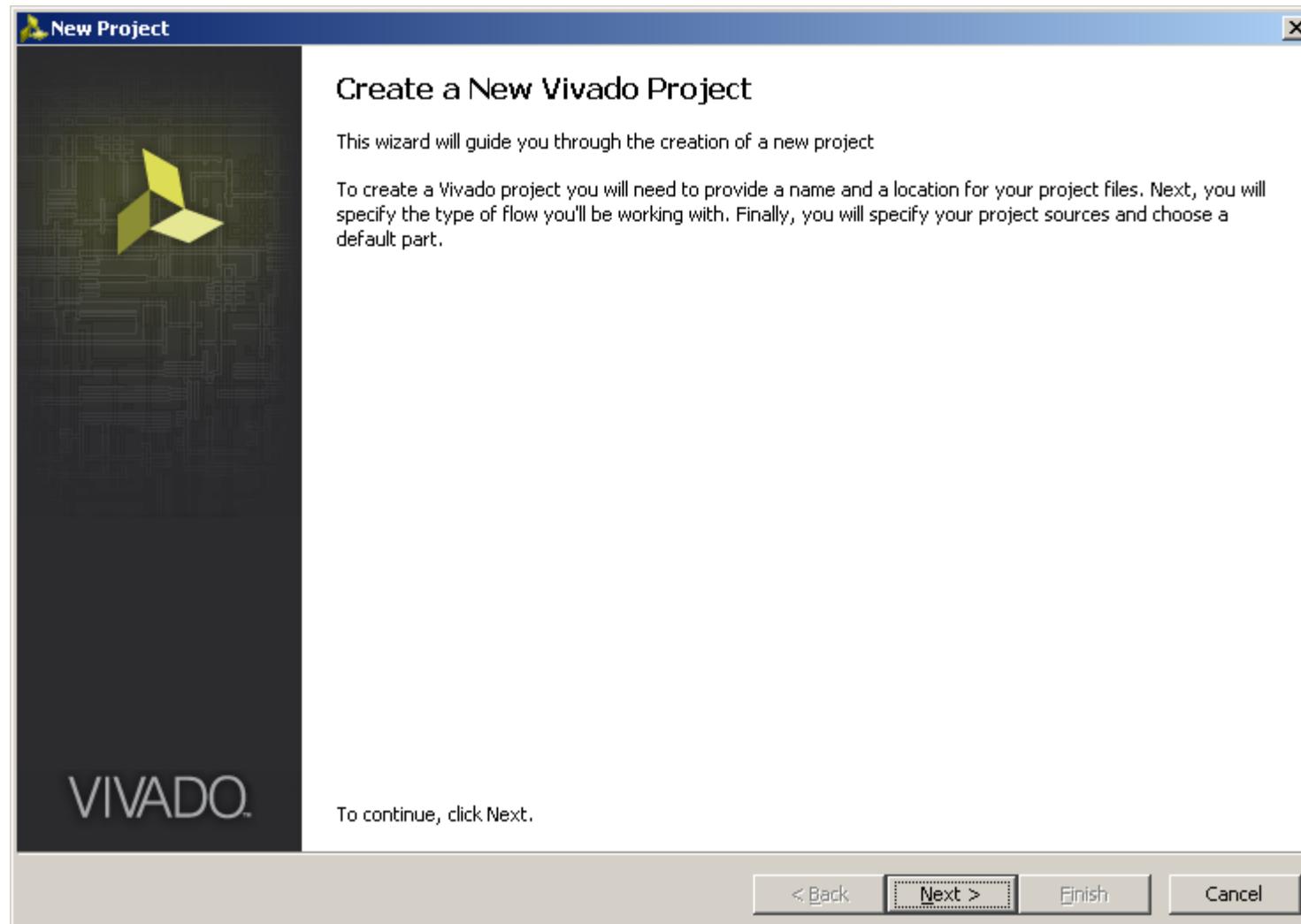
Start → All Programs → Xilinx Design Tools → Vivado 2012.4 → Vivado

► Select Create New Project



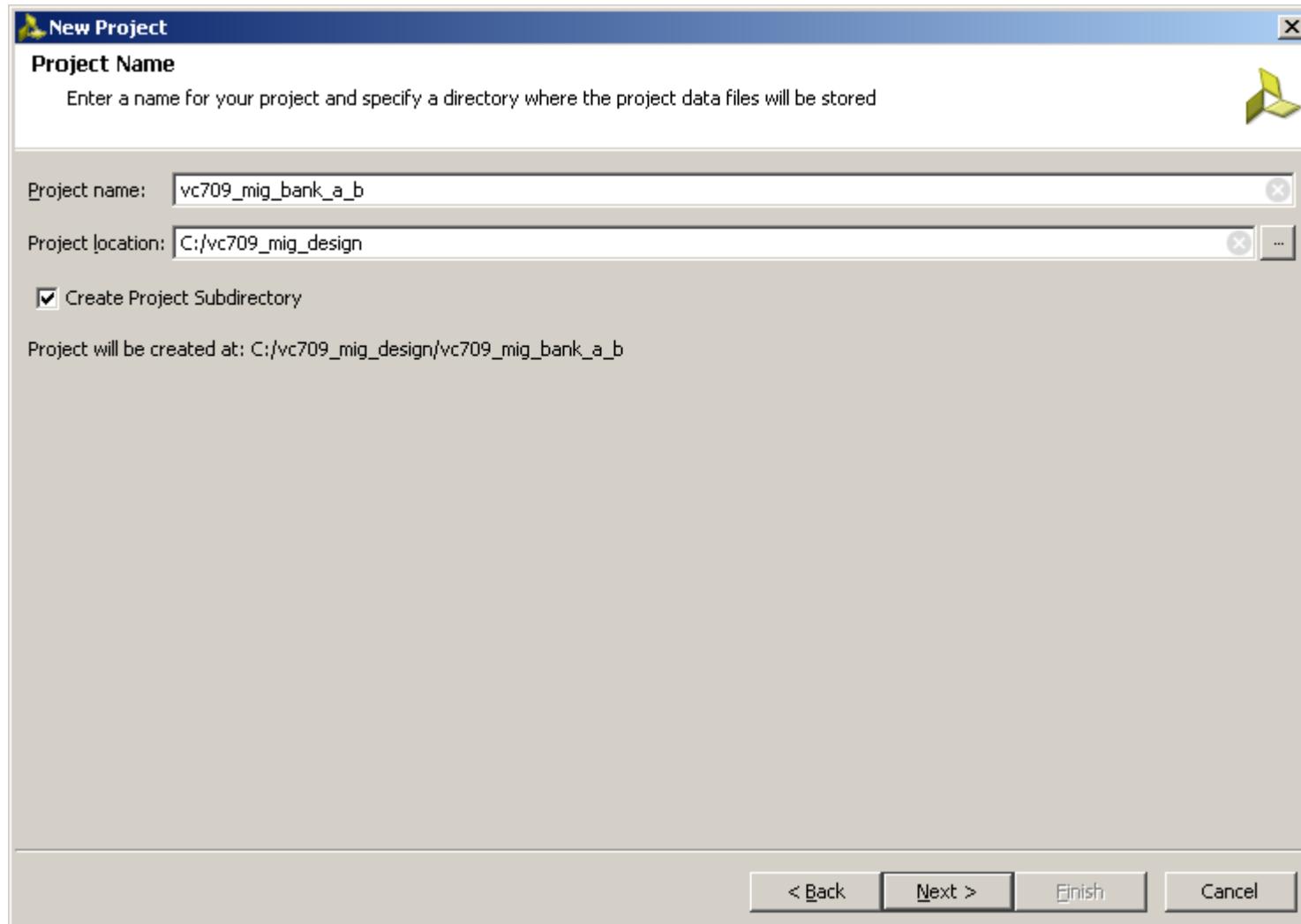
Generate MIG Bank A and B Example Design

► Click Next



Generate MIG Bank A and B Example Design

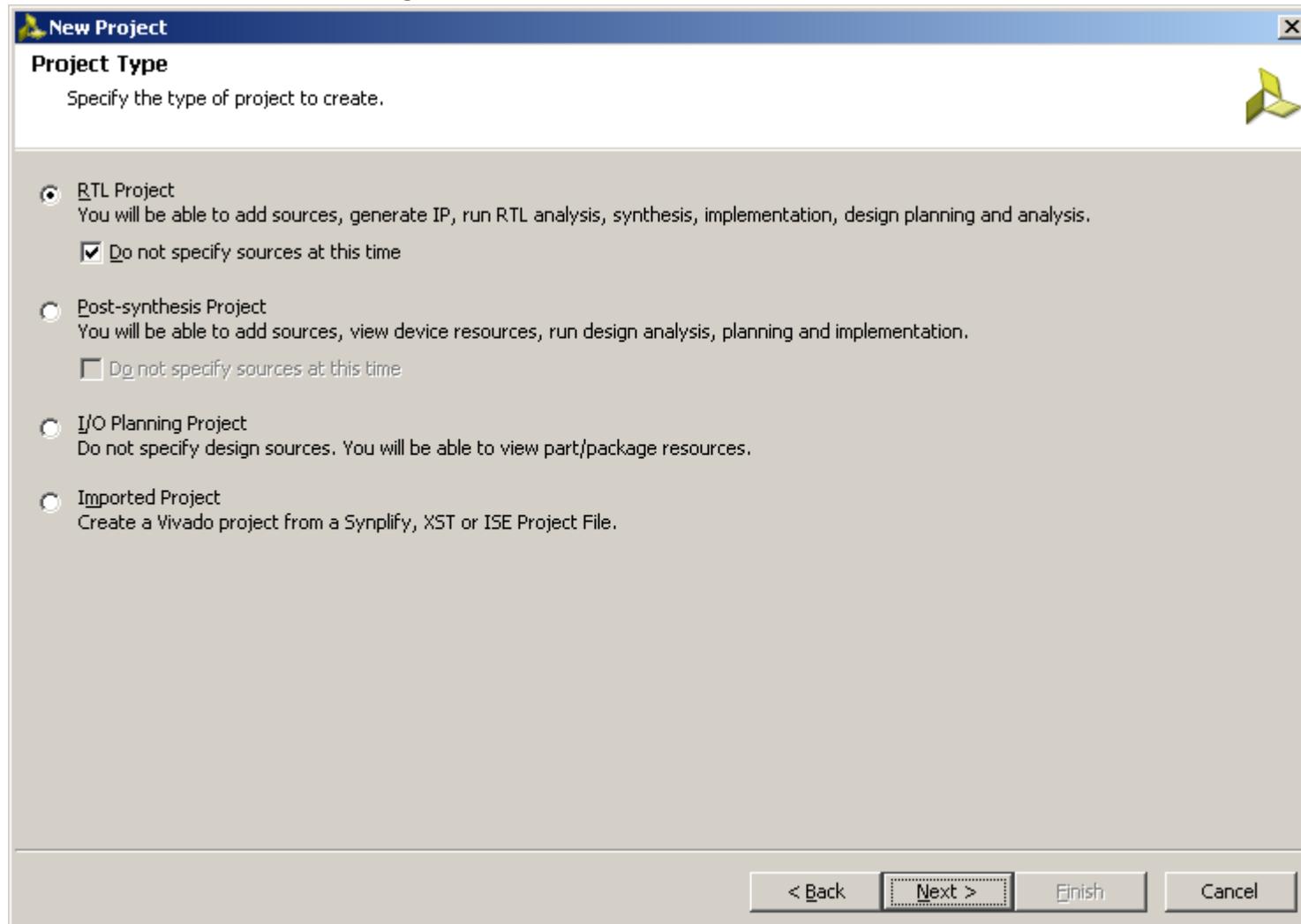
- Set the Project name to vc709_mig_bank_a_b and location to C:\vc709_mig_design



Generate MIG Bank A and B Example Design

► Select RTL Project

- Select **Do not specify sources at this time**



Generate MIG Bank A and B Example Design

► Select the xc7vx690tffg1761-2 device

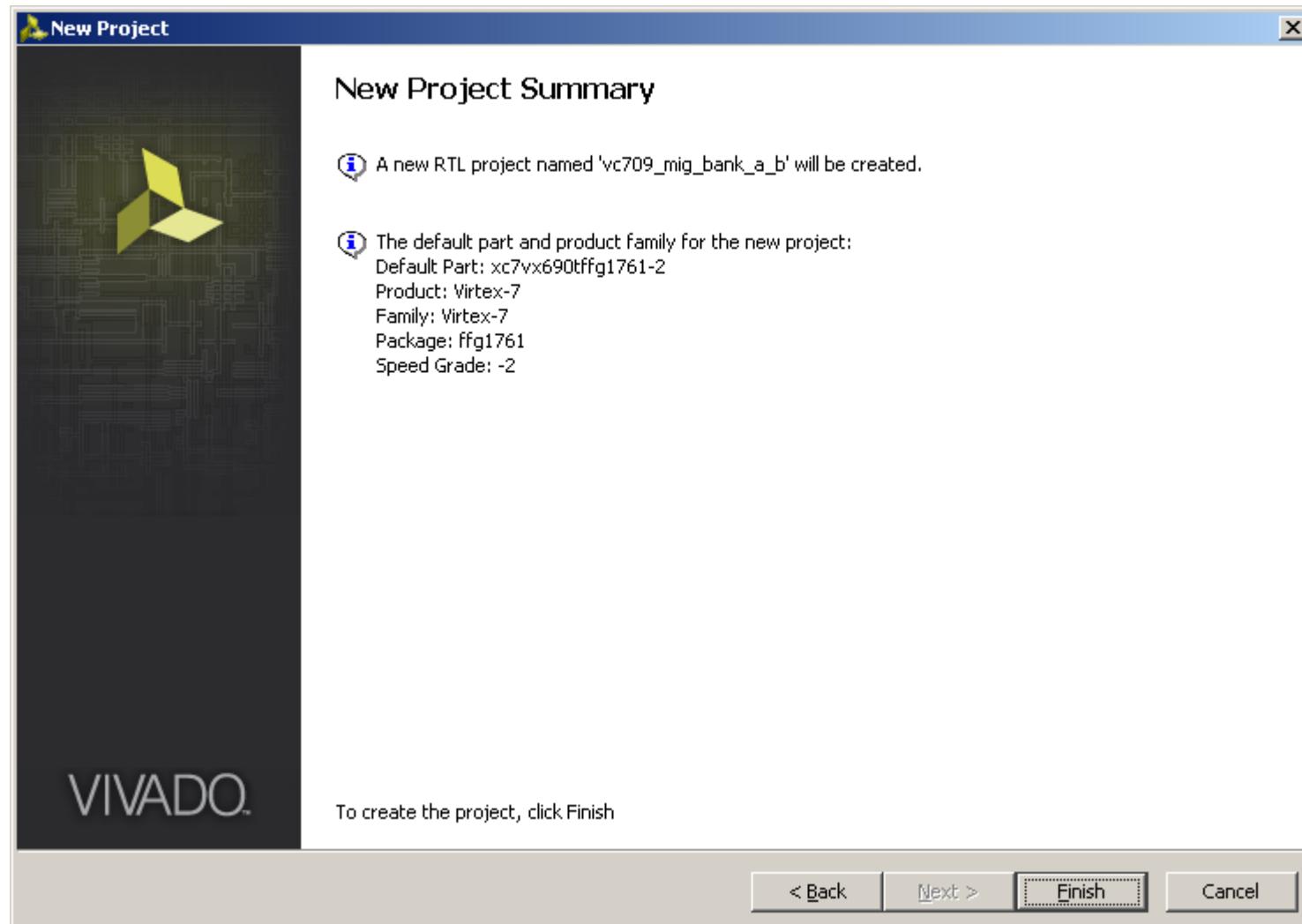
The screenshot shows the 'New Project' dialog box with the title 'Default Part'. The 'Parts' tab is selected in the sidebar. The filter settings are set to 'Product category: All', 'Family: Virtex-7', 'Sub-Family: All Remaining', 'Package: FFG1761', 'Speed grade: -2', and 'Temp grade: All Remaining'. A 'Reset All Filters' button is located below the filters. A search bar with a magnifying glass icon is present. The main area displays a table of device specifications:

Device	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	DSPs	Gb Transceivers	PCI Buses
xc7v585tffg1761-2	1,761	850	364200	728400	795	1260	36	3
xc7vx330tffg1761-2	1,761	700	204000	408000	750	1120	28	2
xc7vx485tffg1761-2	1,761	700	303600	607200	1030	2800	28	4
xc7vx690tffg1761-2	1,761	850	433200	866400	1470	3600	36	3

At the bottom of the dialog, there are navigation buttons: '< Back', 'Next >', 'Finish', and 'Cancel'.

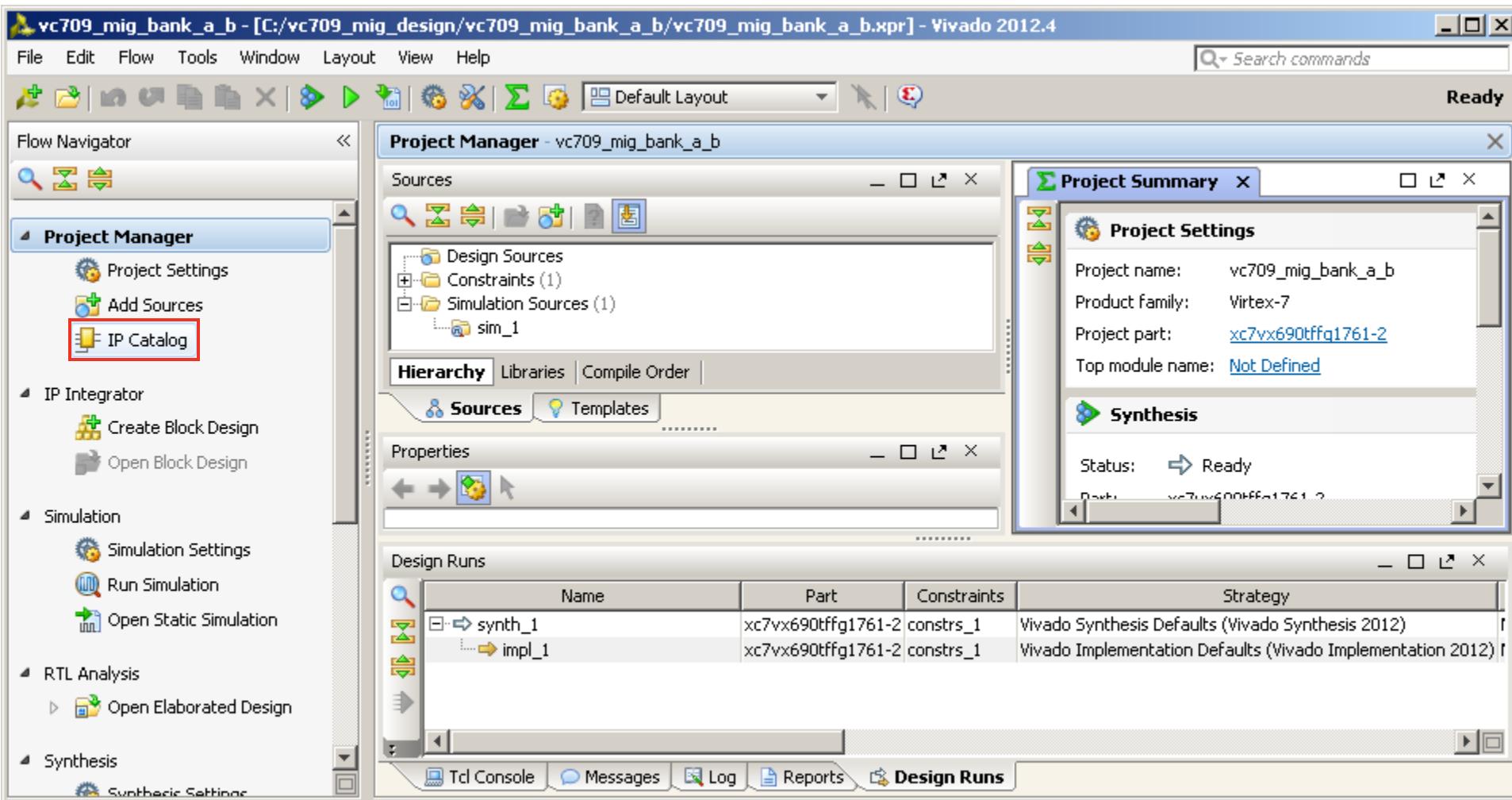
Generate MIG Bank A and B Example Design

► Click Finish



Generate MIG Bank A and B Example Design

► Click on IP Catalog



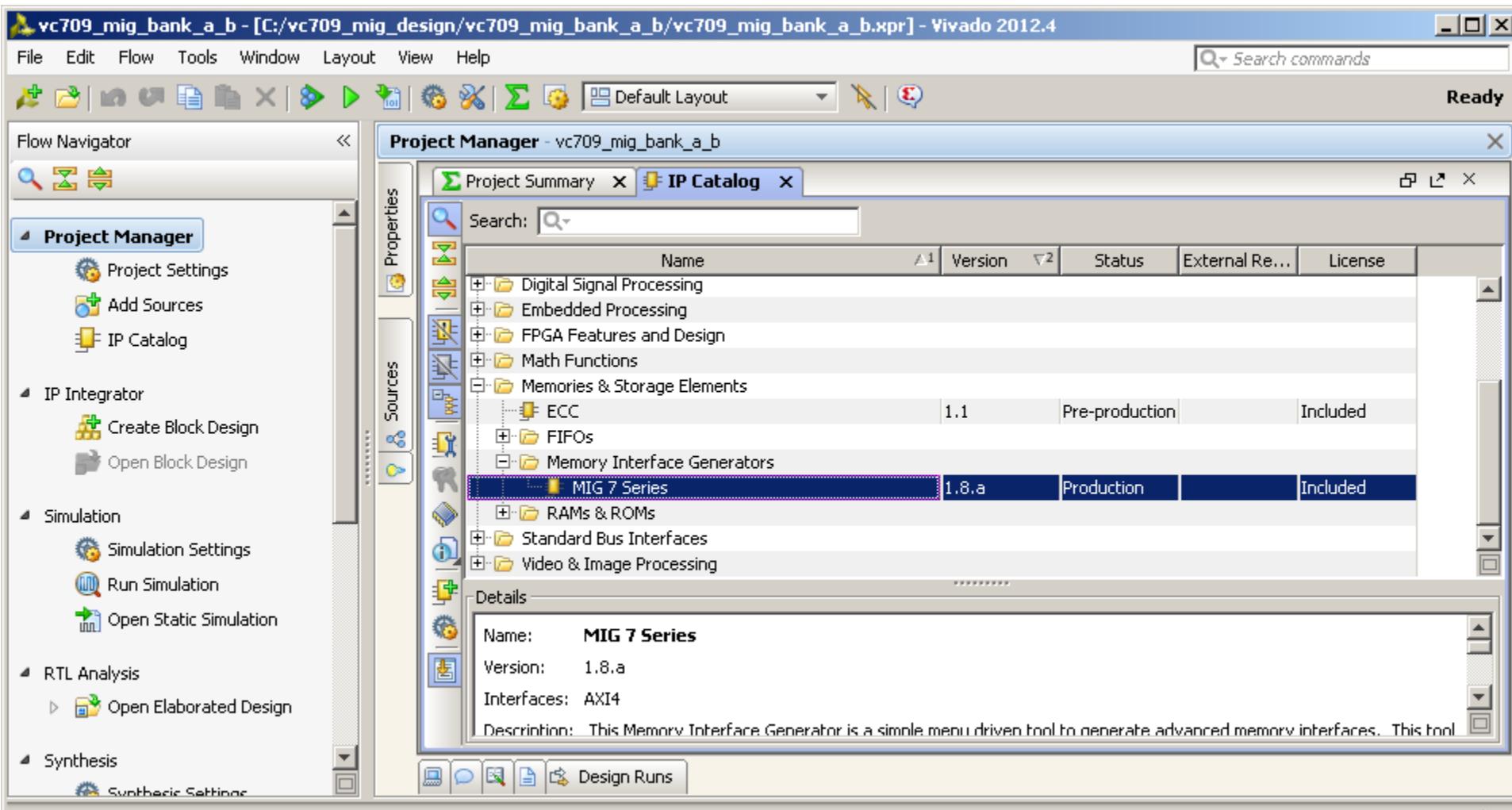
Browse, customize, and generate cores.

Note: Presentation applies to the VC709

XILINX ➤ ALL PROGRAMMABLE

Generate MIG Bank A and B Example Design

► Select MIG 7 Series under Memory Interface Generators



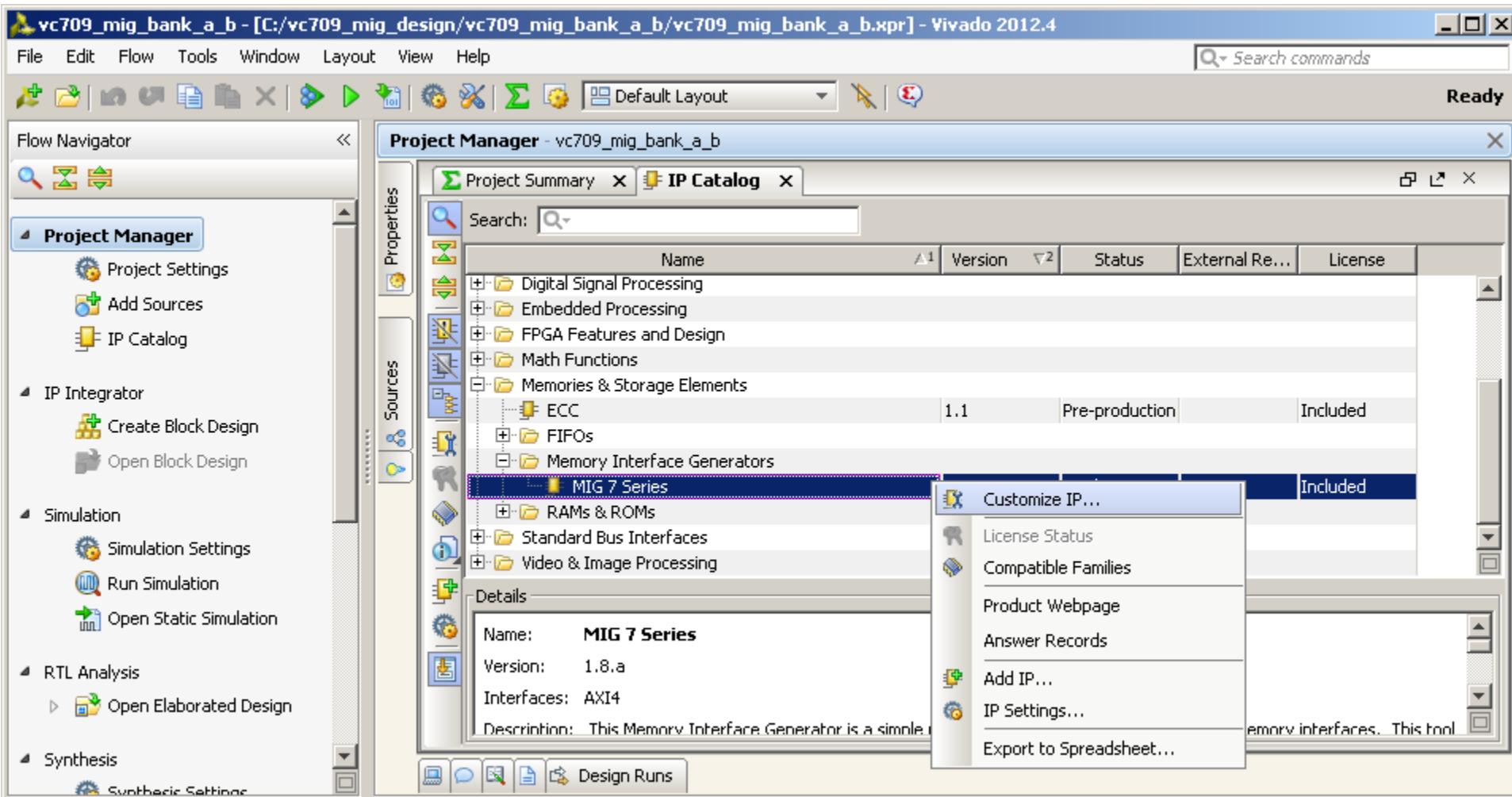
IP: MIG 7 Series

Note: Presentation applies to the VC709

XILINX ➤ ALL PROGRAMMABLE™

Generate MIG Bank A and B Example Design

- Right click on MIG 7 Series Version 1.8.a
 - Select Customize IP

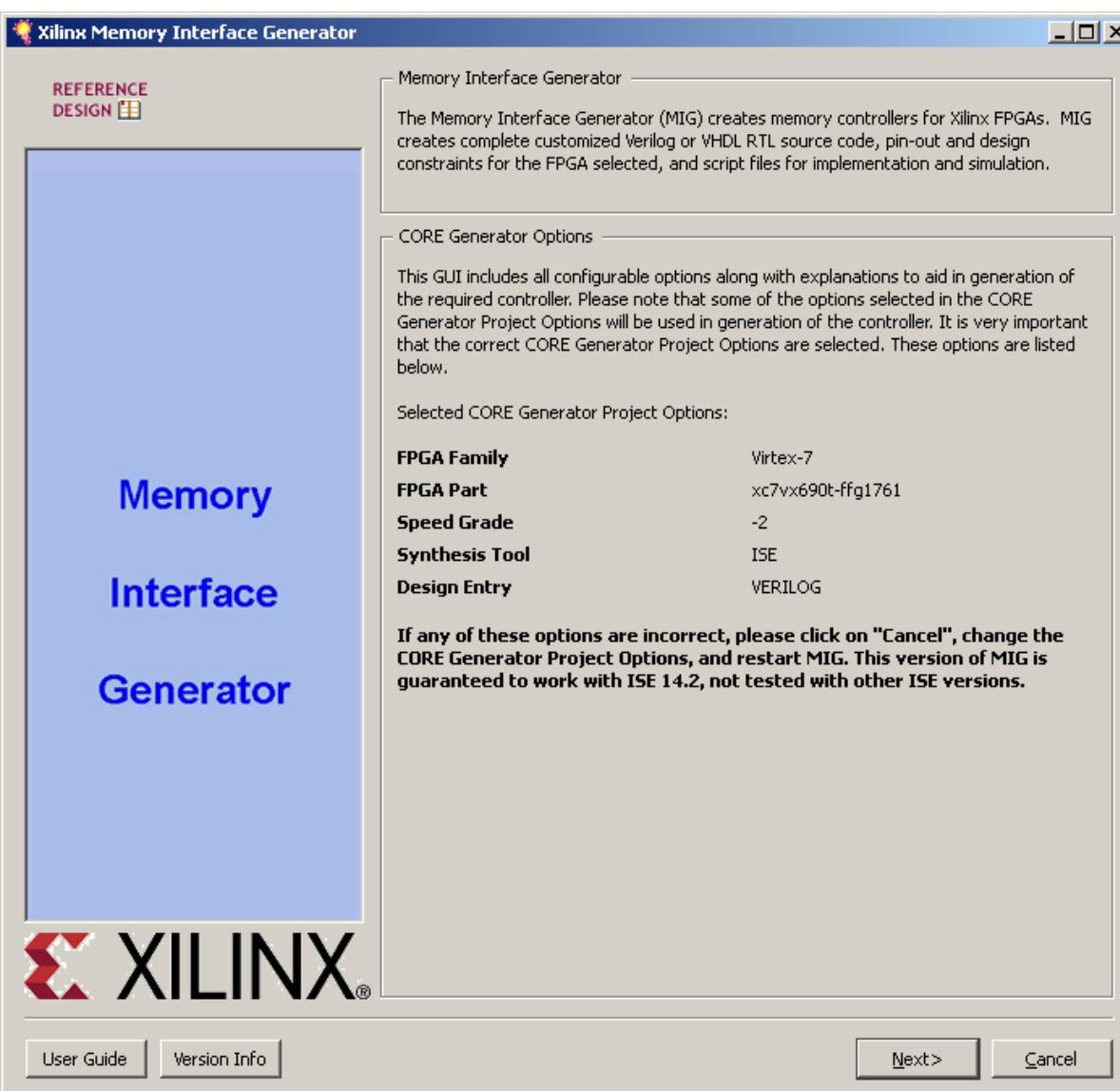


Customize the selected core

Note: Presentation applies to the VC709

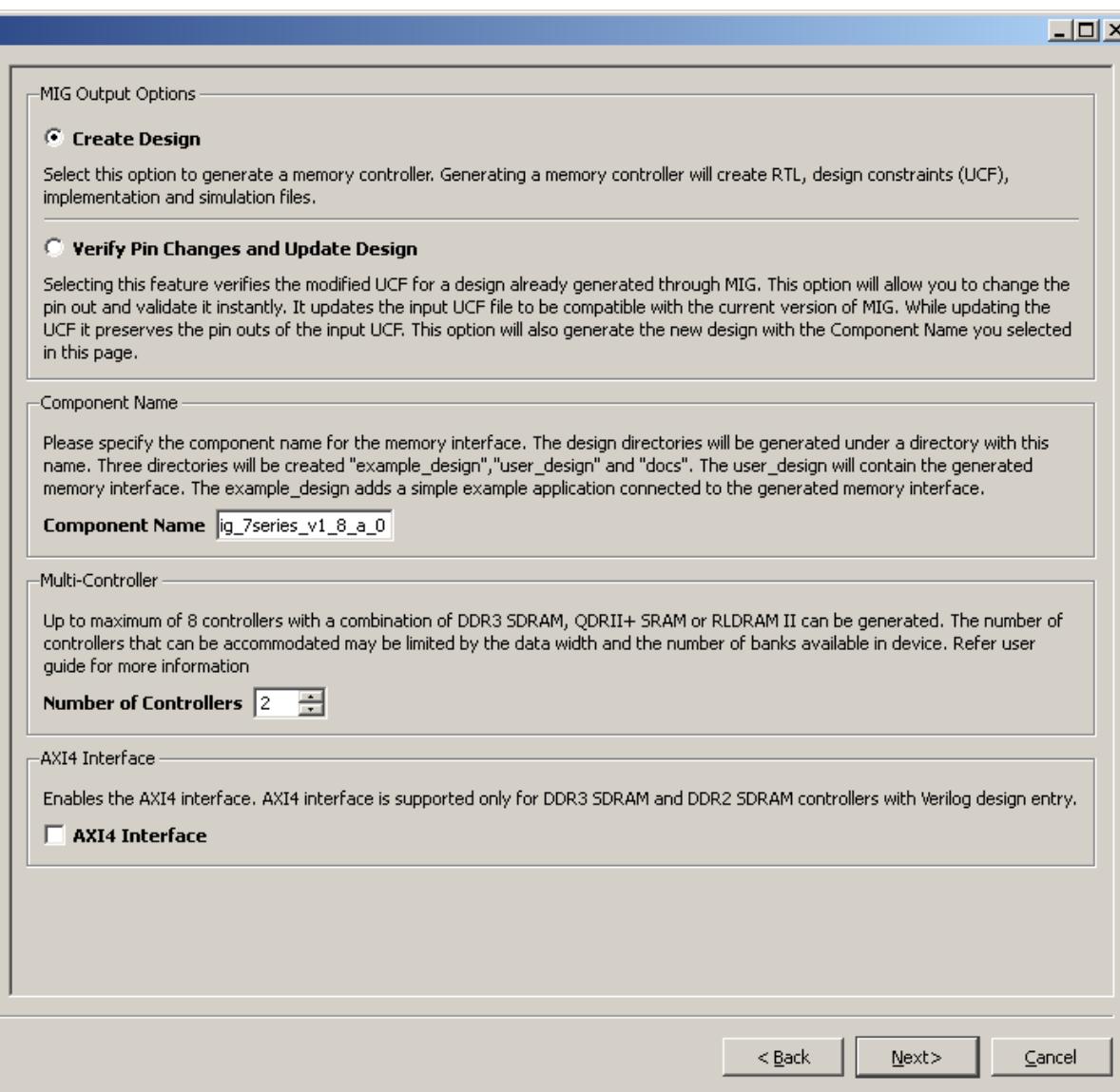
XILINX ➤ ALL PROGRAMMABLE™

Generate MIG Bank A and B Example Design



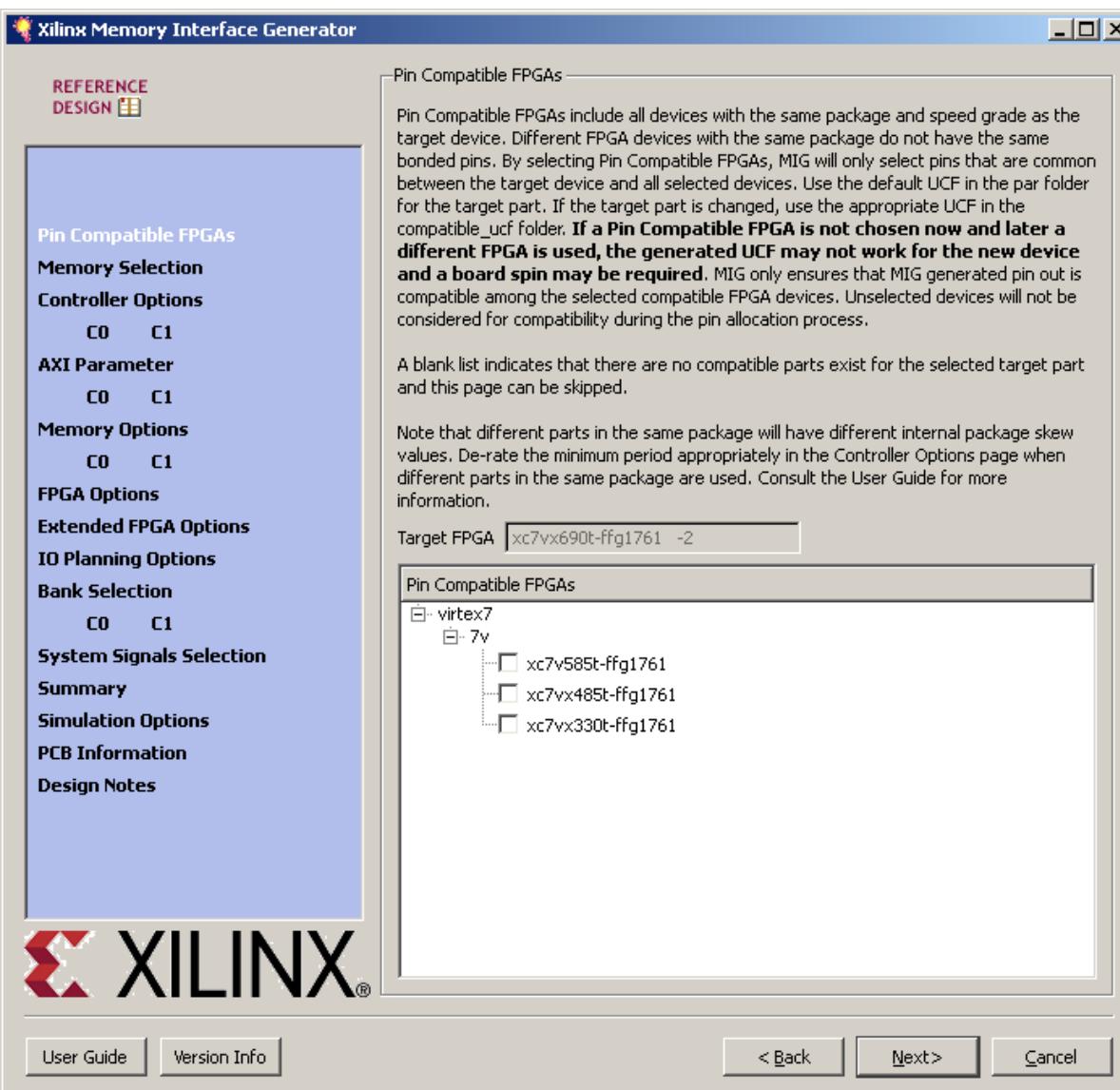
➤ Leave this page as is
– Click Next

Generate MIG Bank A and B Example Design



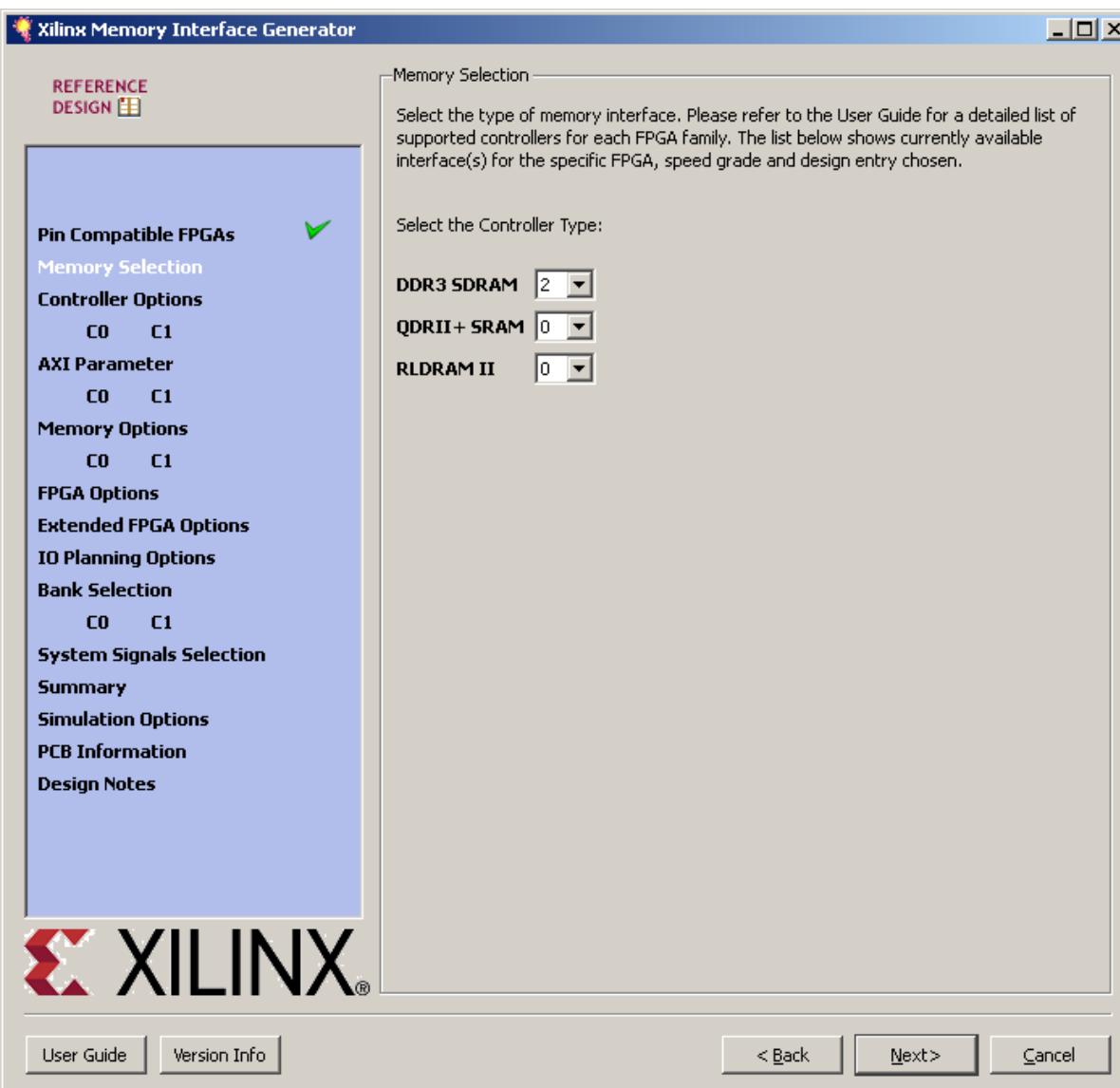
- Set the number of controllers to 2
 - Click Next

Generate MIG Bank A and B Example Design



➤ Leave this page as is
– Click Next

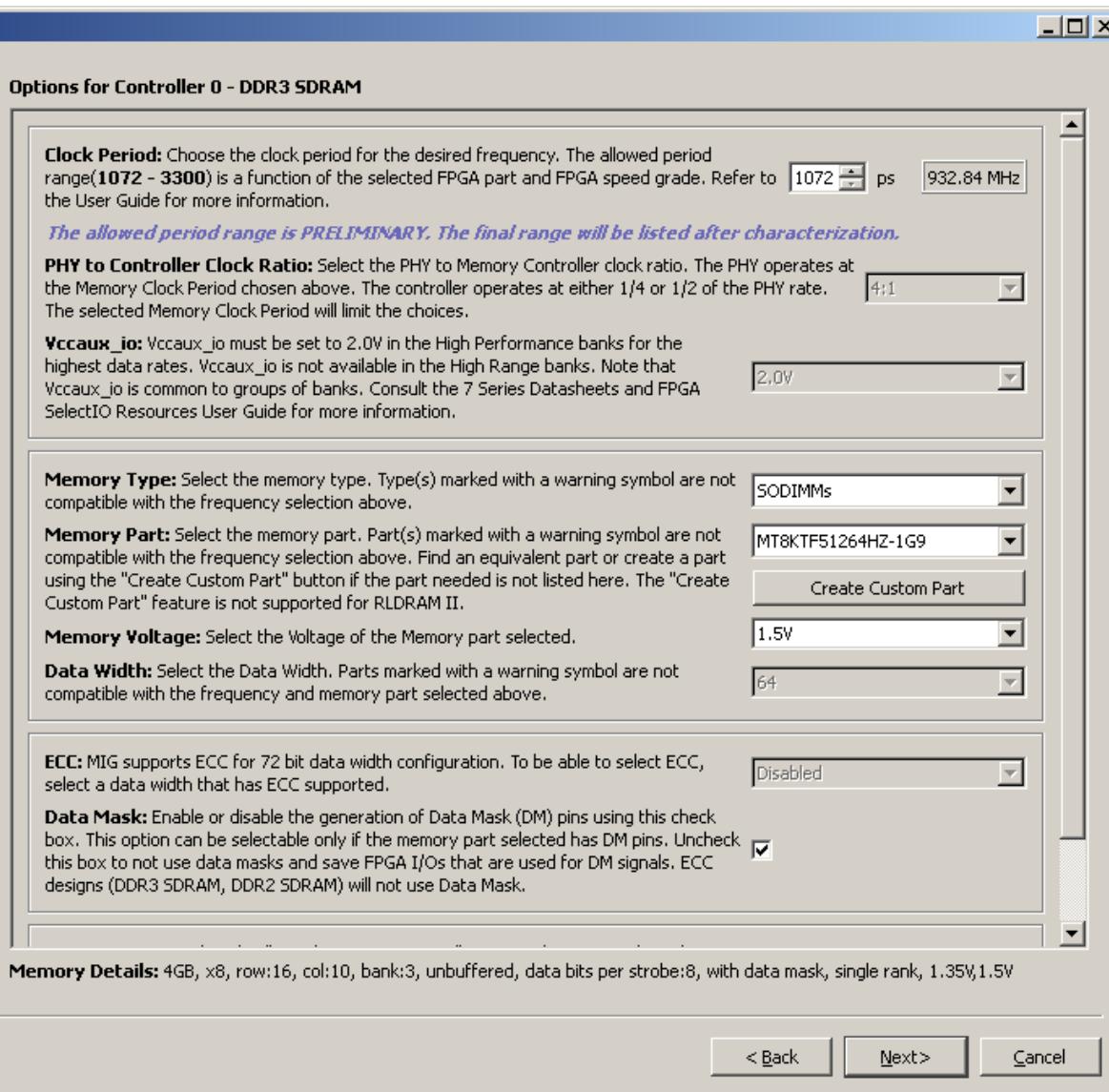
Generate MIG Bank A and B Example Design



► Select Memory Type

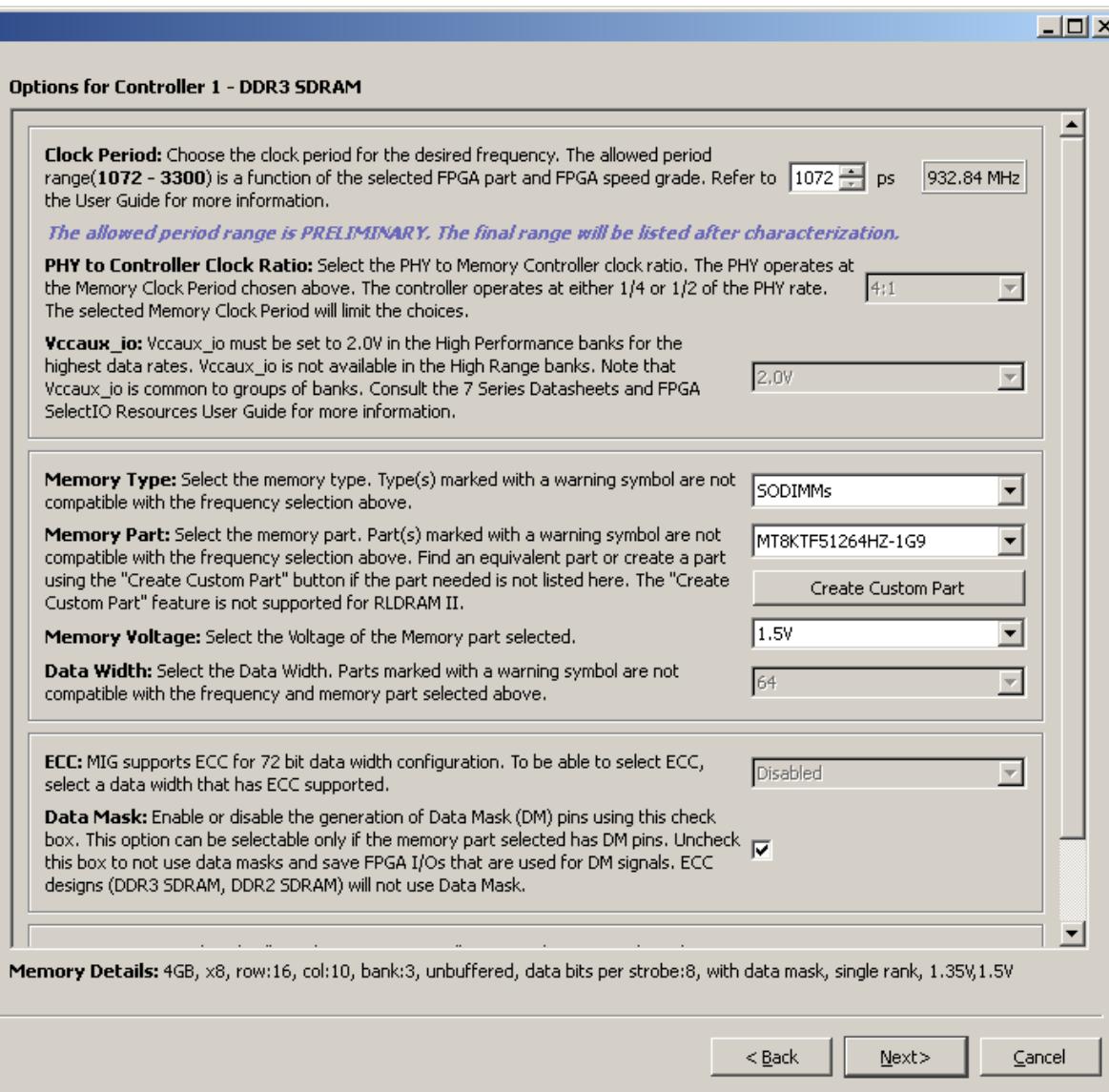
- 2 each of DDR3 SDRAM
- Click Next

Generate MIG Bank A and B Example Design



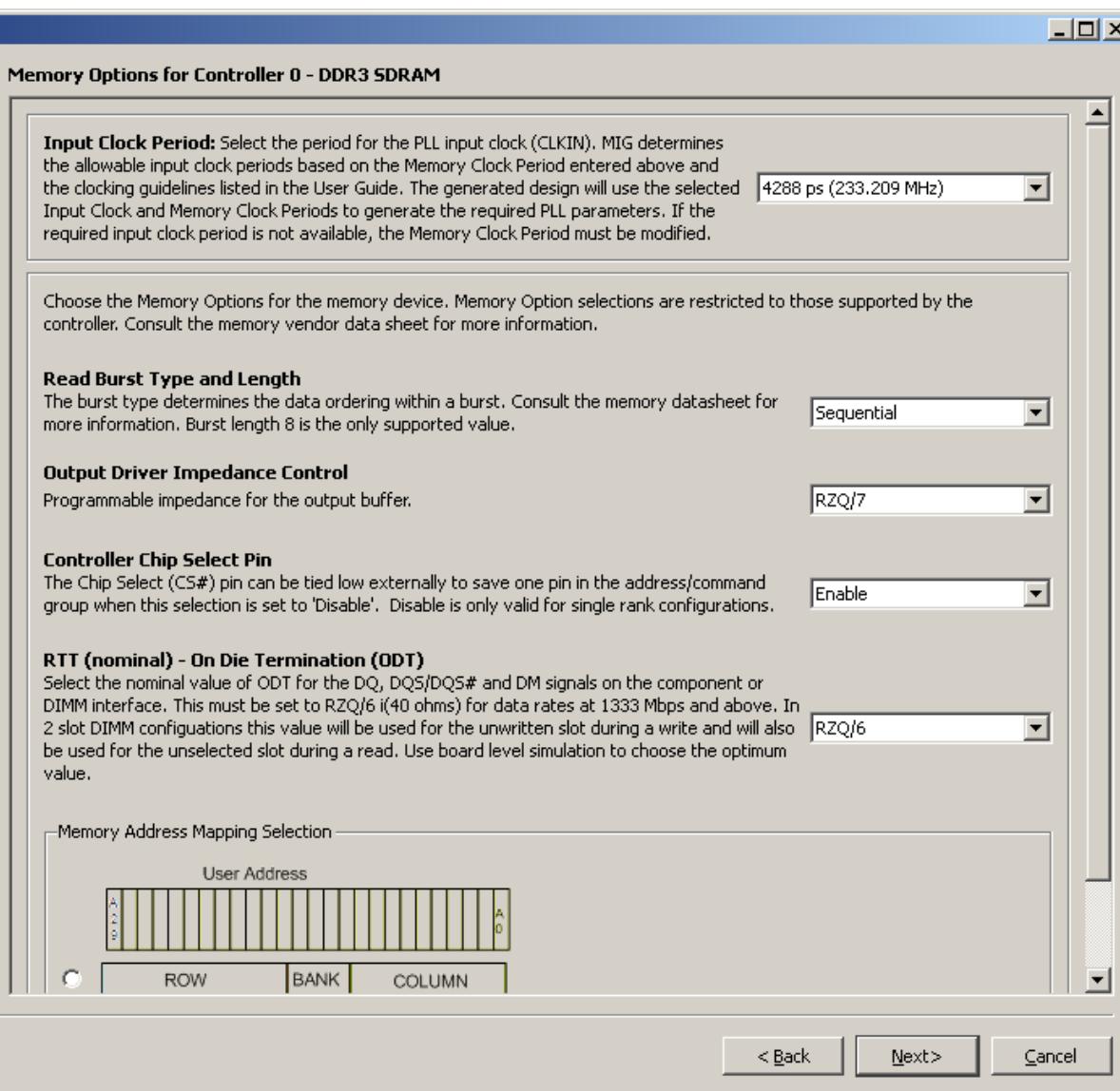
- For Controller 0, select
- Clock Period: **1072 ps**
 - Type: **SODIMMs**
 - Part:
MT8KTF51264HZ-1G9
 - Memory Voltage: **1.5V**
 - Data Mask: **Checked**
 - Click Next

Generate MIG Bank A and B Example Design



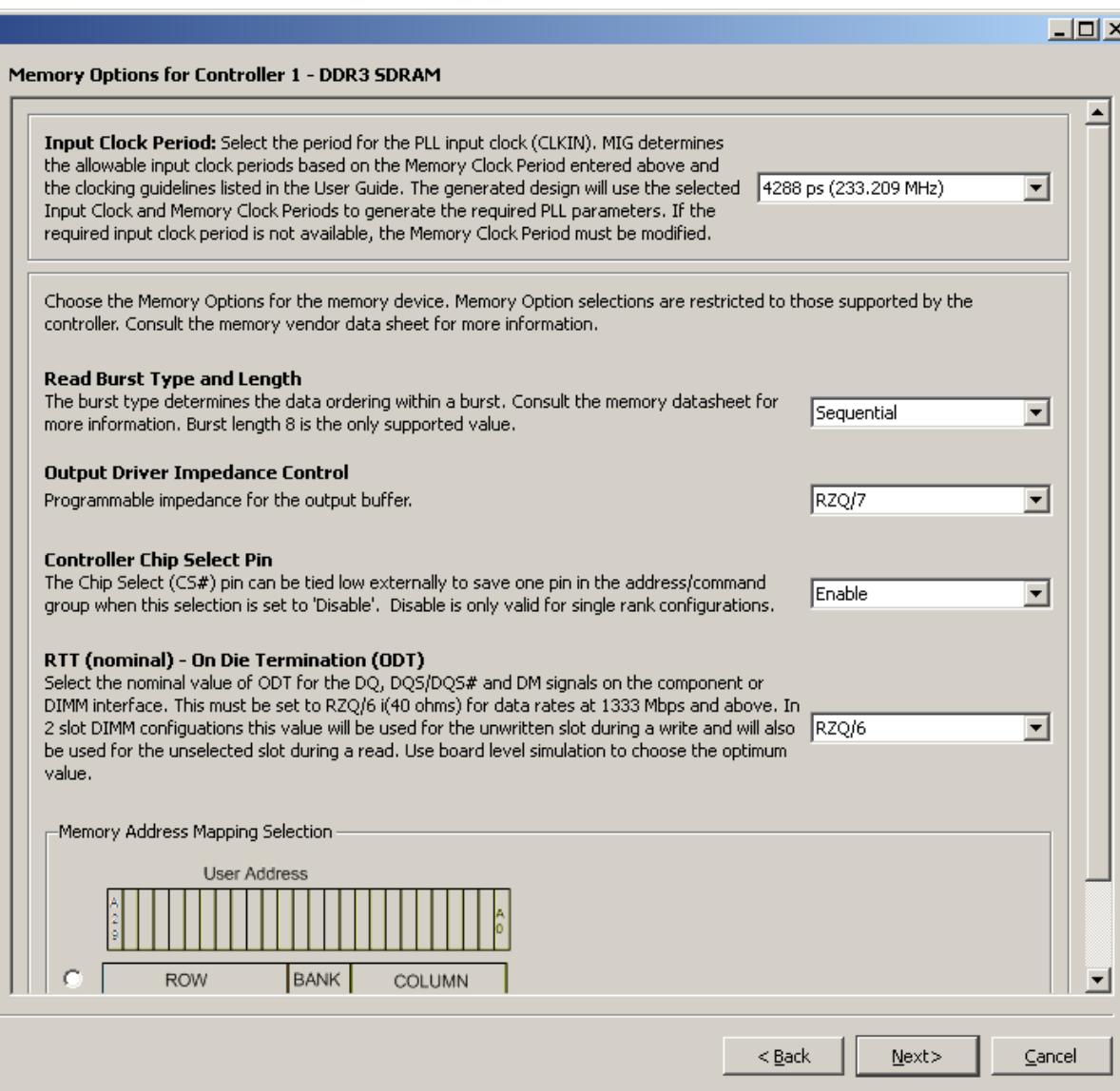
- For Controller 1, select
- Clock Period: **1072 ps**
 - Type: **SODIMMs**
 - Part:
MT8KTF51264HZ-1G9
 - Memory Voltage: **1.5V**
 - Data Mask: **Checked**
 - Click Next

Generate MIG Bank A and B Example Design



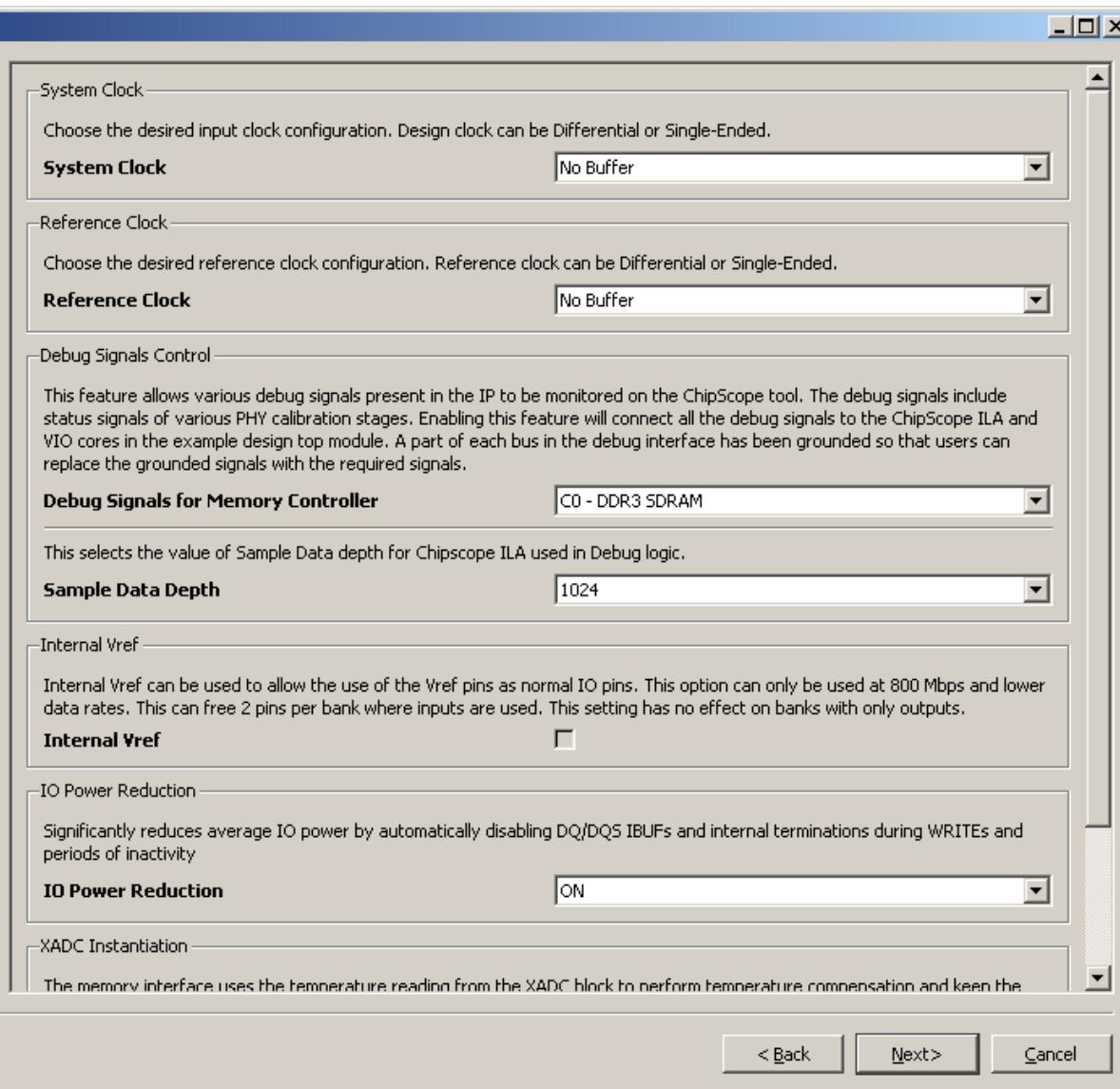
- For Controller 0, select:
- Input Clock Period: 4288 ps
 - RTT: RZQ/6
 - Click Next

Generate MIG Bank A and B Example Design



- For Controller 1, select:
- Input Clock Period: 4288 ps
 - RTT: RZQ/6
 - Click Next

Generate MIG Bank A and B Example Design



➤ Select

- Set System Clock to **No Buffer**
- Set Reference Clock to **No Buffer**
- Debug: **C0 – DDR3 SDRAM**
- Click Next

Generate MIG Bank A and B Example Design



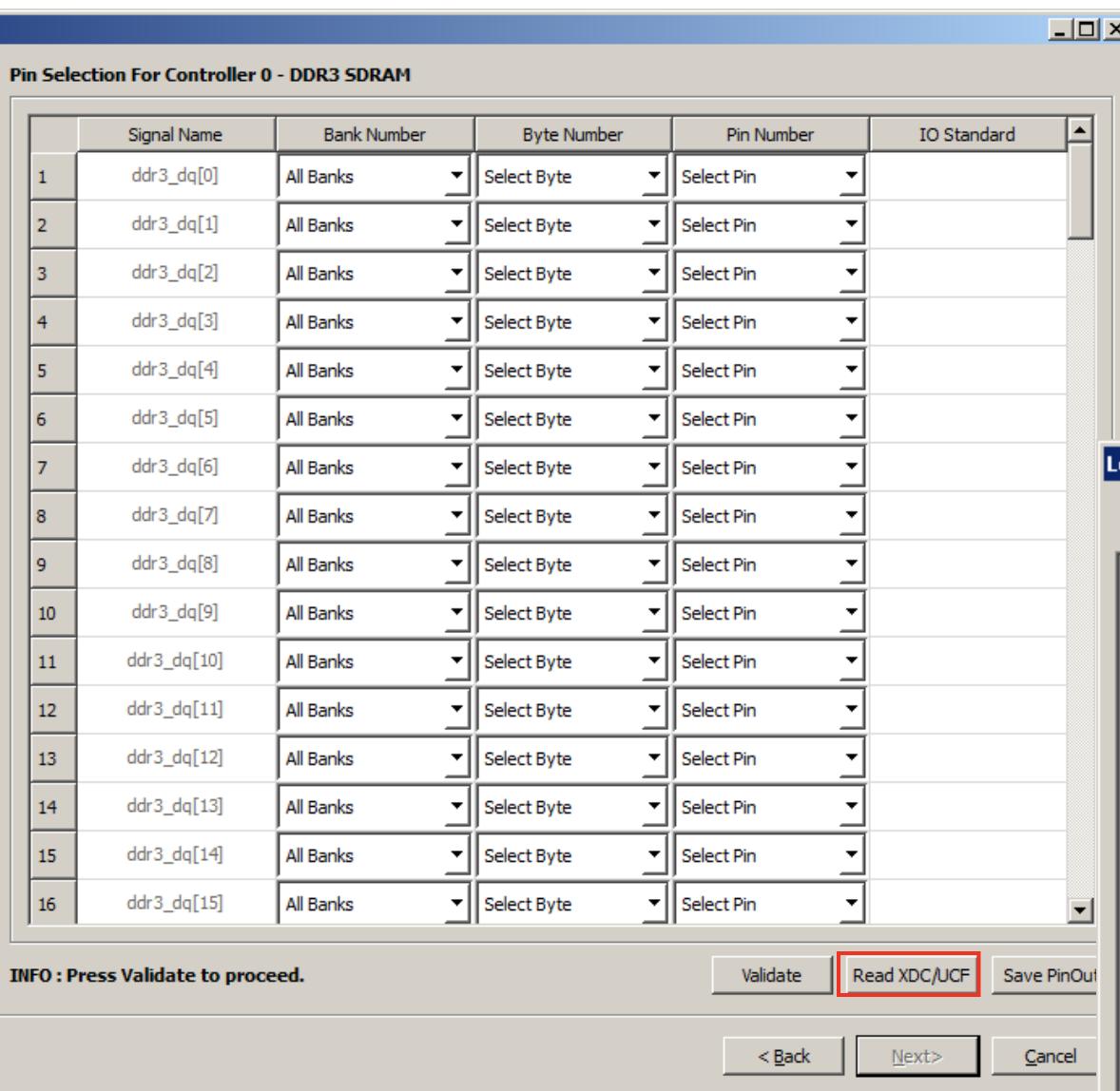
➤ Leave this page as is
– Click Next

Generate MIG Bank A and B Example Design

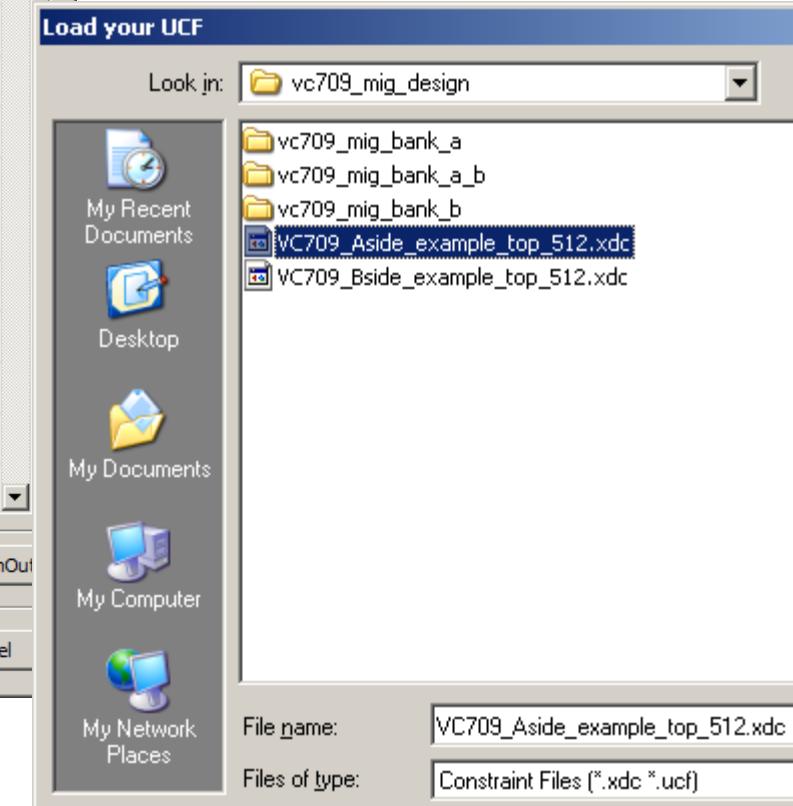


► Select Fixed Pin Out
– Click Next

Generate MIG Bank A and B Example Design

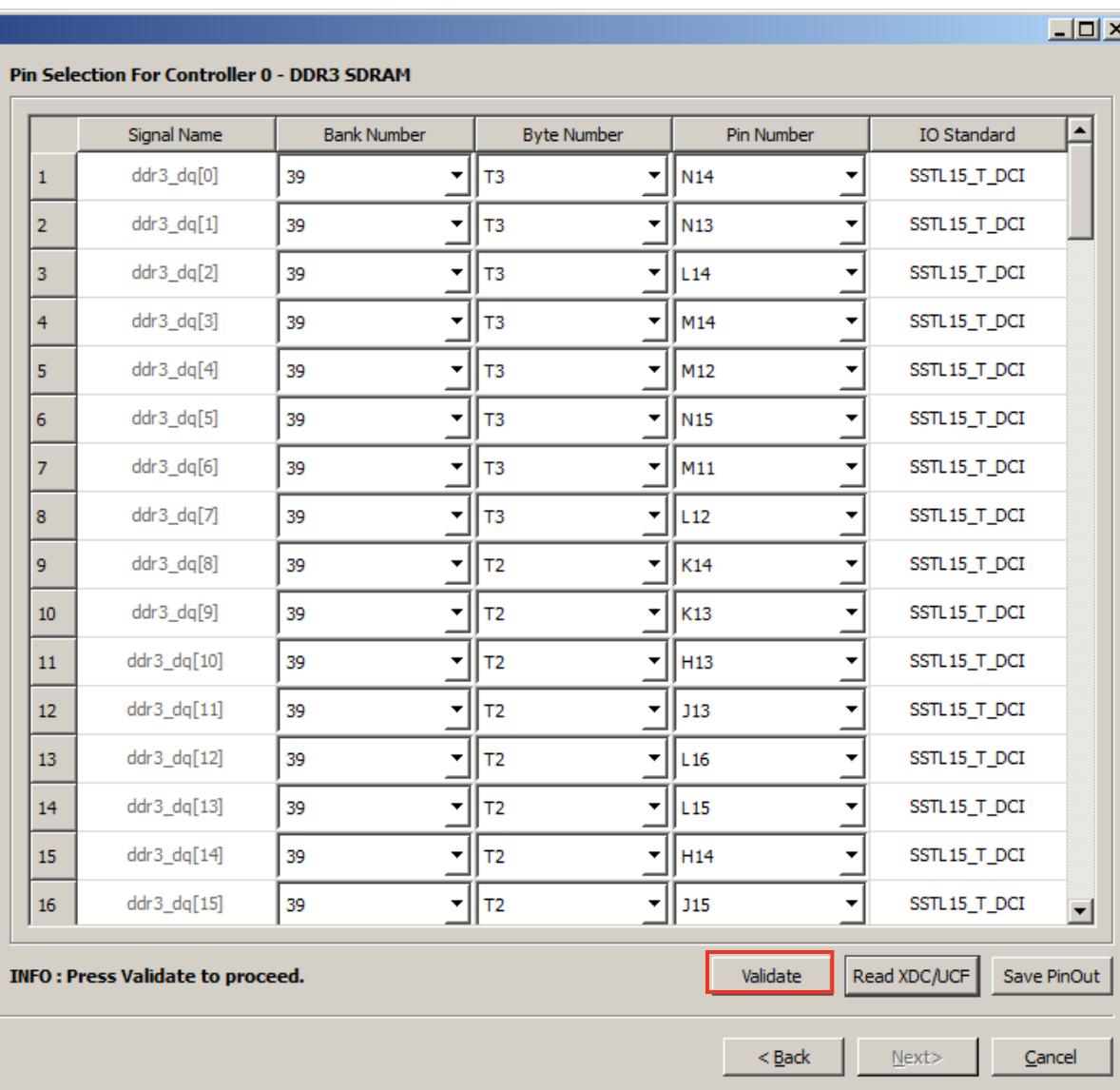


► For Controller 0, select Read XDC/UCF
– Open the file:
VC709_Aside_example_top_512.xdc



Note: Presentation applies to the VC709

Generate MIG Bank A and B Example Design



- Once it finishes reading in the XDC, click Validate
 - Click OK



Generate MIG Bank A and B Example Design

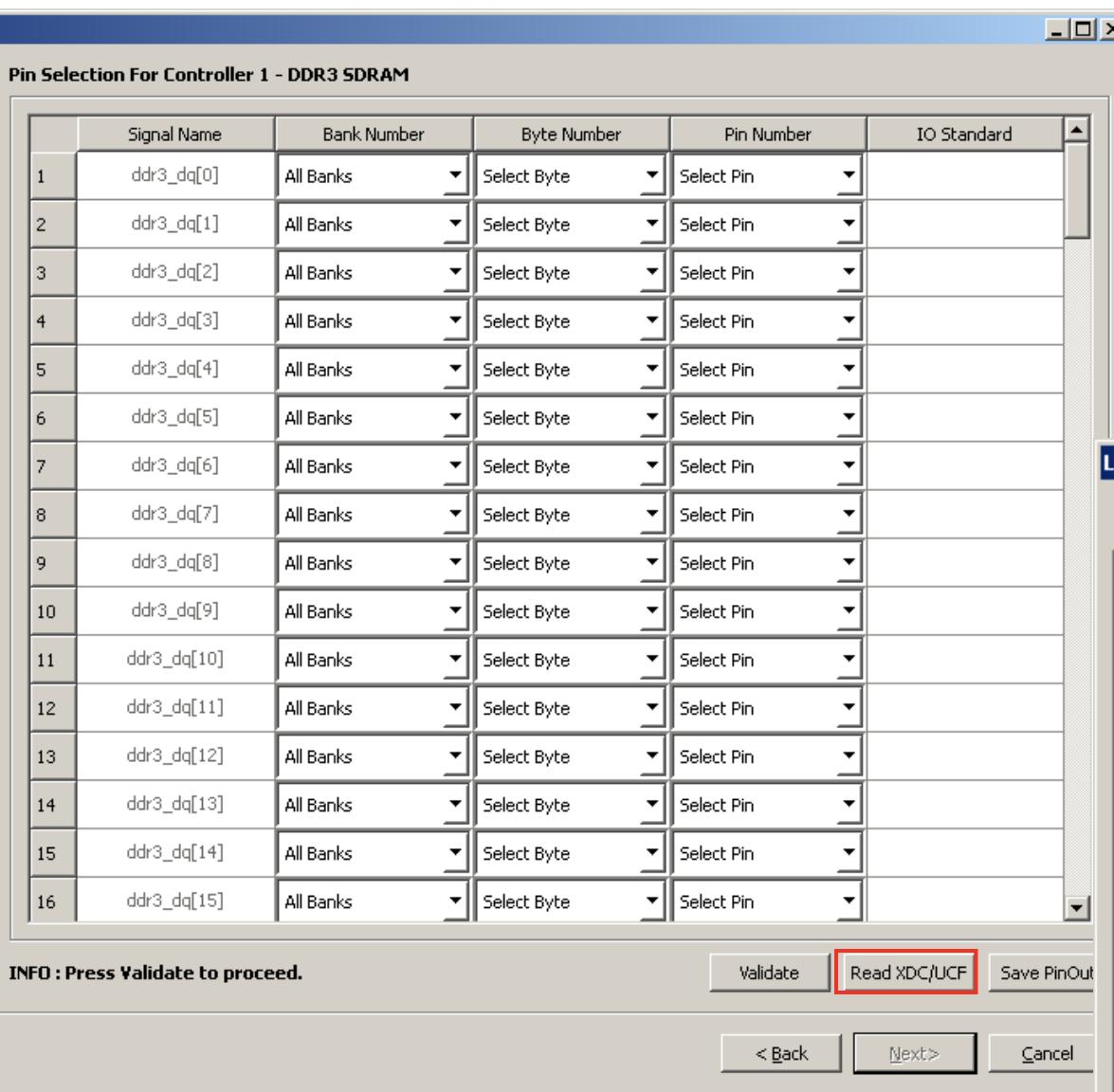
Pin Selection For Controller 0 - DDR3 SDRAM

	Signal Name	Bank Number	Byte Number	Pin Number	IO Standard
1	ddr3_dq[0]	39	T3	N14	SSTL15_T_DCI
2	ddr3_dq[1]	39	T3	N13	SSTL15_T_DCI
3	ddr3_dq[2]	39	T3	L14	SSTL15_T_DCI
4	ddr3_dq[3]	39	T3	M14	SSTL15_T_DCI
5	ddr3_dq[4]	39	T3	M12	SSTL15_T_DCI
6	ddr3_dq[5]	39	T3	N15	SSTL15_T_DCI
7	ddr3_dq[6]	39	T3	M11	SSTL15_T_DCI
8	ddr3_dq[7]	39	T3	L12	SSTL15_T_DCI
9	ddr3_dq[8]	39	T2	K14	SSTL15_T_DCI
10	ddr3_dq[9]	39	T2	K13	SSTL15_T_DCI
11	ddr3_dq[10]	39	T2	H13	SSTL15_T_DCI
12	ddr3_dq[11]	39	T2	J13	SSTL15_T_DCI
13	ddr3_dq[12]	39	T2	L16	SSTL15_T_DCI
14	ddr3_dq[13]	39	T2	L15	SSTL15_T_DCI
15	ddr3_dq[14]	39	T2	H14	SSTL15_T_DCI
16	ddr3_dq[15]	39	T2	J15	SSTL15_T_DCI

INFO : Validation successful. Press Next to proceed.

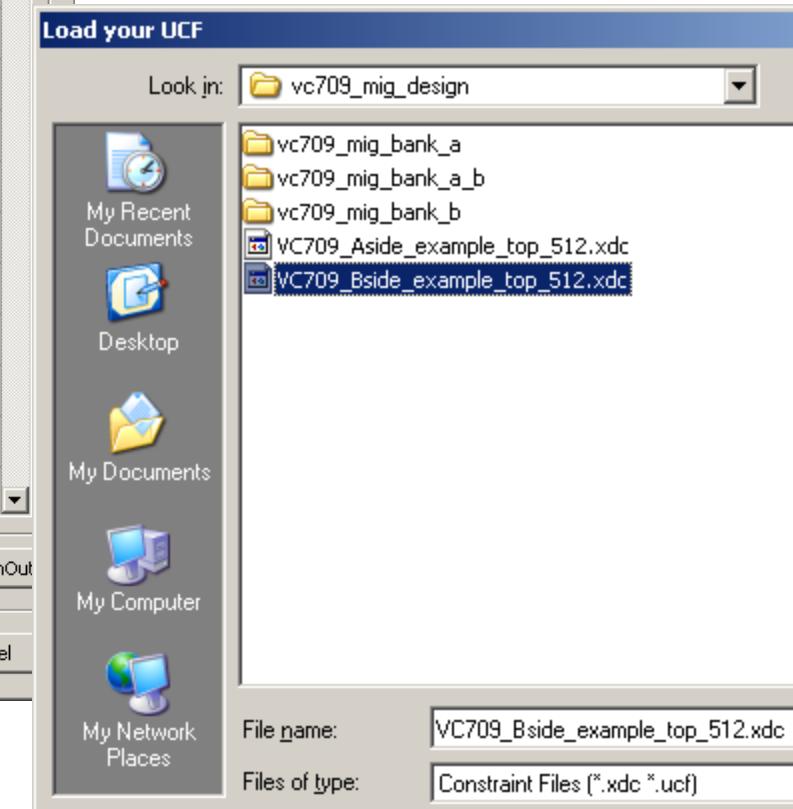
- The Next button is enabled once the pinout is validated.
 - Click Next

Generate MIG Bank A and B Example Design



➤ For Controller 1, elect ReadUCF

- Open the file:
VC709_Bside_example_top_512.xdc



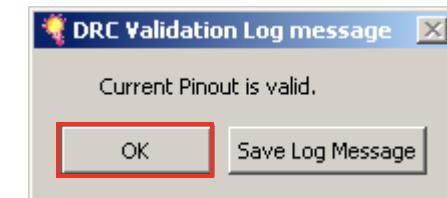
Generate MIG Bank A and B Example Design

Pin Selection For Controller 1 - DDR3 SDRAM

	Signal Name	Bank Number	Byte Number	Pin Number	IO Standard
1	ddr3_dq[0]	33	T1	AN24	SSTL15_T_DCI
2	ddr3_dq[1]	33	T1	AM24	SSTL15_T_DCI
3	ddr3_dq[2]	33	T1	AR22	SSTL15_T_DCI
4	ddr3_dq[3]	33	T1	AR23	SSTL15_T_DCI
5	ddr3_dq[4]	33	T1	AN23	SSTL15_T_DCI
6	ddr3_dq[5]	33	T1	AM23	SSTL15_T_DCI
7	ddr3_dq[6]	33	T1	AN21	SSTL15_T_DCI
8	ddr3_dq[7]	33	T1	AP21	SSTL15_T_DCI
9	ddr3_dq[8]	33	T0	AK23	SSTL15_T_DCI
10	ddr3_dq[9]	33	T0	AJ23	SSTL15_T_DCI
11	ddr3_dq[10]	33	T0	AL21	SSTL15_T_DCI
12	ddr3_dq[11]	33	T0	AM21	SSTL15_T_DCI
13	ddr3_dq[12]	33	T0	AJ21	SSTL15_T_DCI
14	ddr3_dq[13]	33	T0	AJ20	SSTL15_T_DCI
15	ddr3_dq[14]	33	T0	AK20	SSTL15_T_DCI
16	ddr3_dq[15]	33	T0	AL20	SSTL15_T_DCI

INFO : Press Validate to proceed.

- Once it finishes reading in the UCF, click Validate
 - Click OK



Generate MIG Bank A and B Example Design

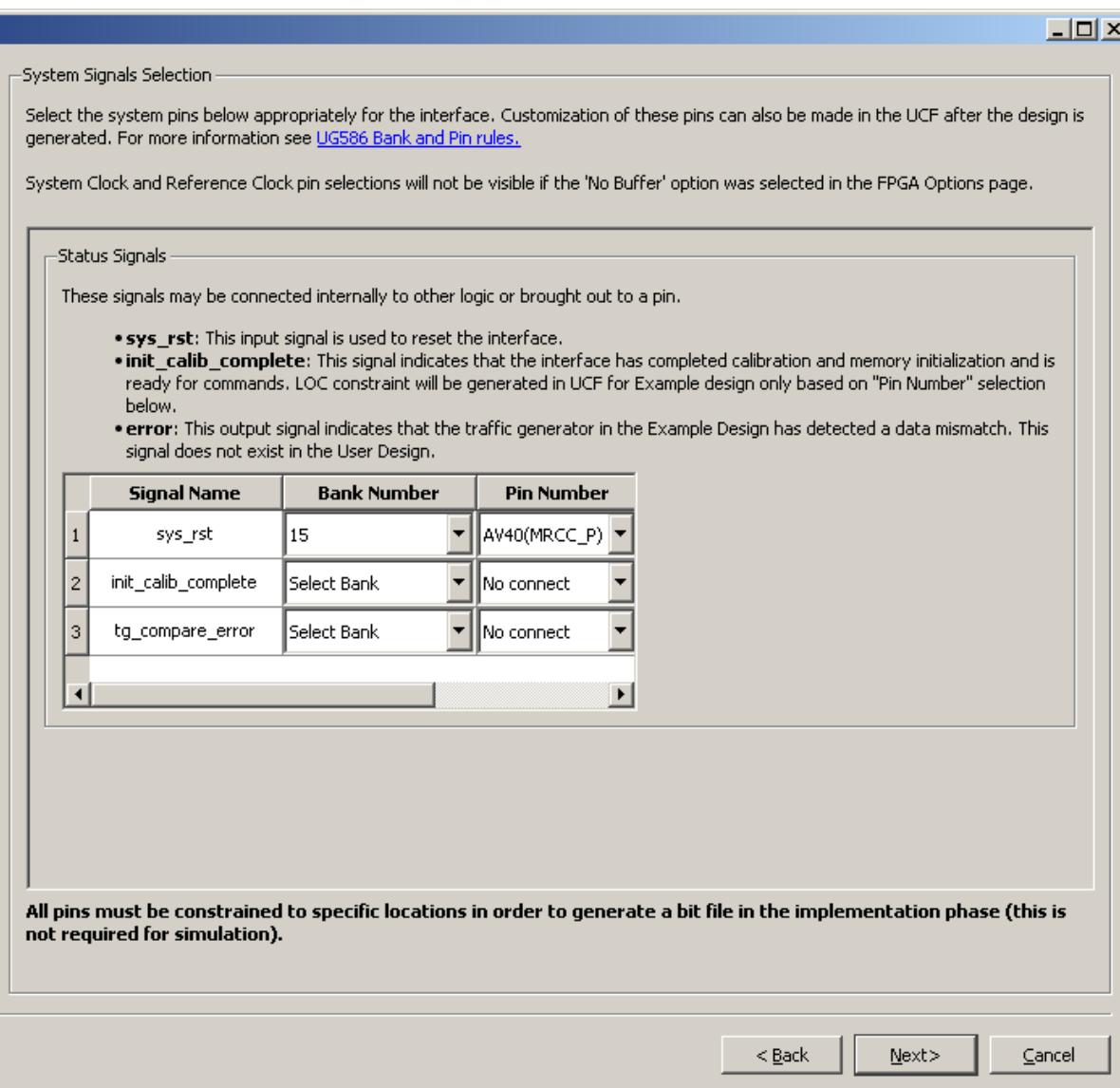
Pin Selection For Controller 1 - DDR3 SDRAM

	Signal Name	Bank Number	Byte Number	Pin Number	IO Standard
1	ddr3_dq[0]	33	T1	AN24	SSTL15_T_DCI
2	ddr3_dq[1]	33	T1	AM24	SSTL15_T_DCI
3	ddr3_dq[2]	33	T1	AR22	SSTL15_T_DCI
4	ddr3_dq[3]	33	T1	AR23	SSTL15_T_DCI
5	ddr3_dq[4]	33	T1	AN23	SSTL15_T_DCI
6	ddr3_dq[5]	33	T1	AM23	SSTL15_T_DCI
7	ddr3_dq[6]	33	T1	AN21	SSTL15_T_DCI
8	ddr3_dq[7]	33	T1	AP21	SSTL15_T_DCI
9	ddr3_dq[8]	33	T0	AK23	SSTL15_T_DCI
10	ddr3_dq[9]	33	T0	AJ23	SSTL15_T_DCI
11	ddr3_dq[10]	33	T0	AL21	SSTL15_T_DCI
12	ddr3_dq[11]	33	T0	AM21	SSTL15_T_DCI
13	ddr3_dq[12]	33	T0	AJ21	SSTL15_T_DCI
14	ddr3_dq[13]	33	T0	AJ20	SSTL15_T_DCI
15	ddr3_dq[14]	33	T0	AK20	SSTL15_T_DCI
16	ddr3_dq[15]	33	T0	AL20	SSTL15_T_DCI

INFO : Validation successful. Press Next to proceed.

- The Next button is enabled once the pinout is validated.
 - Click Next

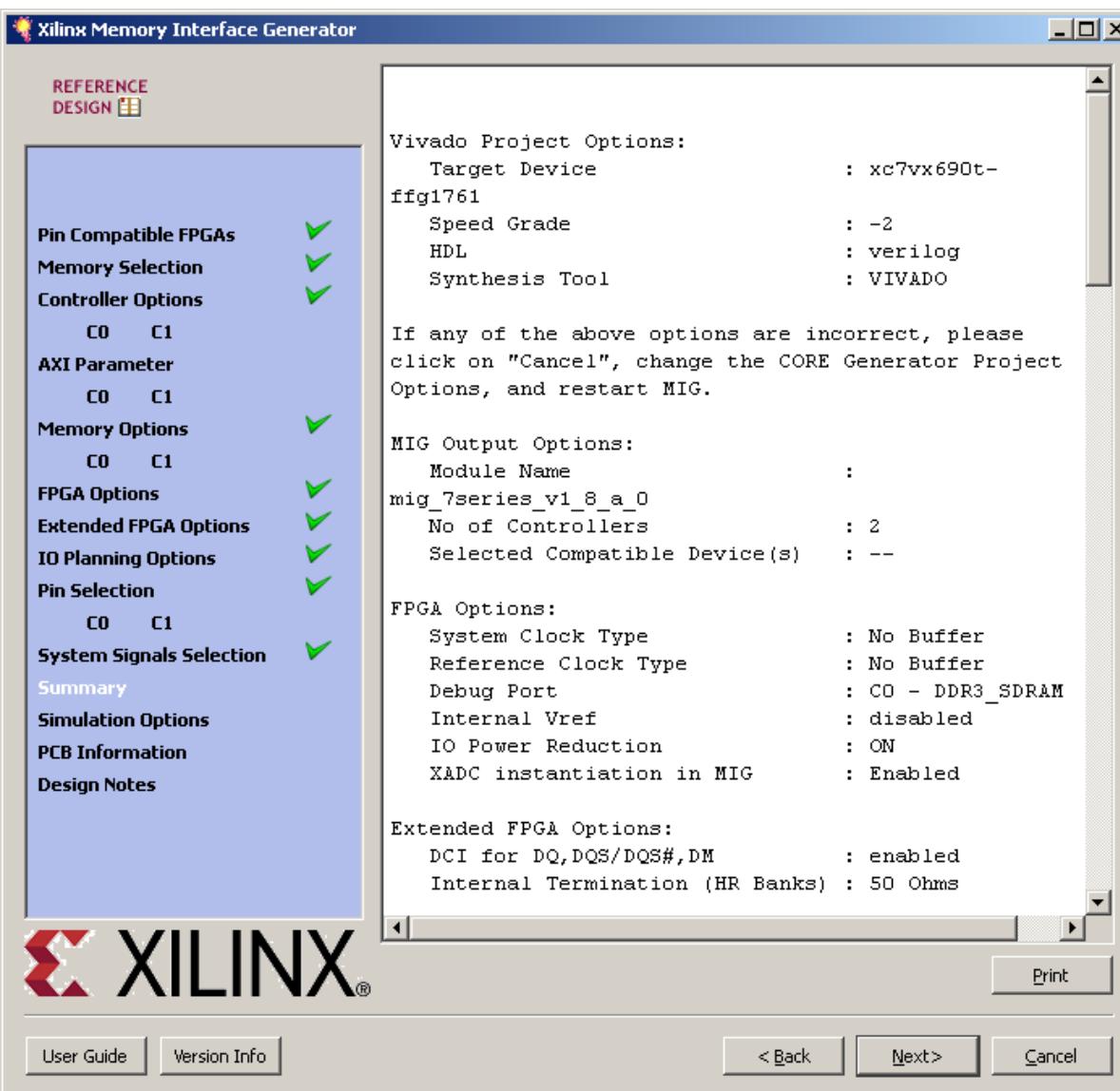
Generate MIG Bank A and B Example Design



➤ Make the following settings:

- Set `sys_rst` to Bank: **15**
- Pin Number:
AV40(MRCC_P)
- Click Next

Generate MIG Bank A and B Example Design



➤ Leave this page as is
– Click Next

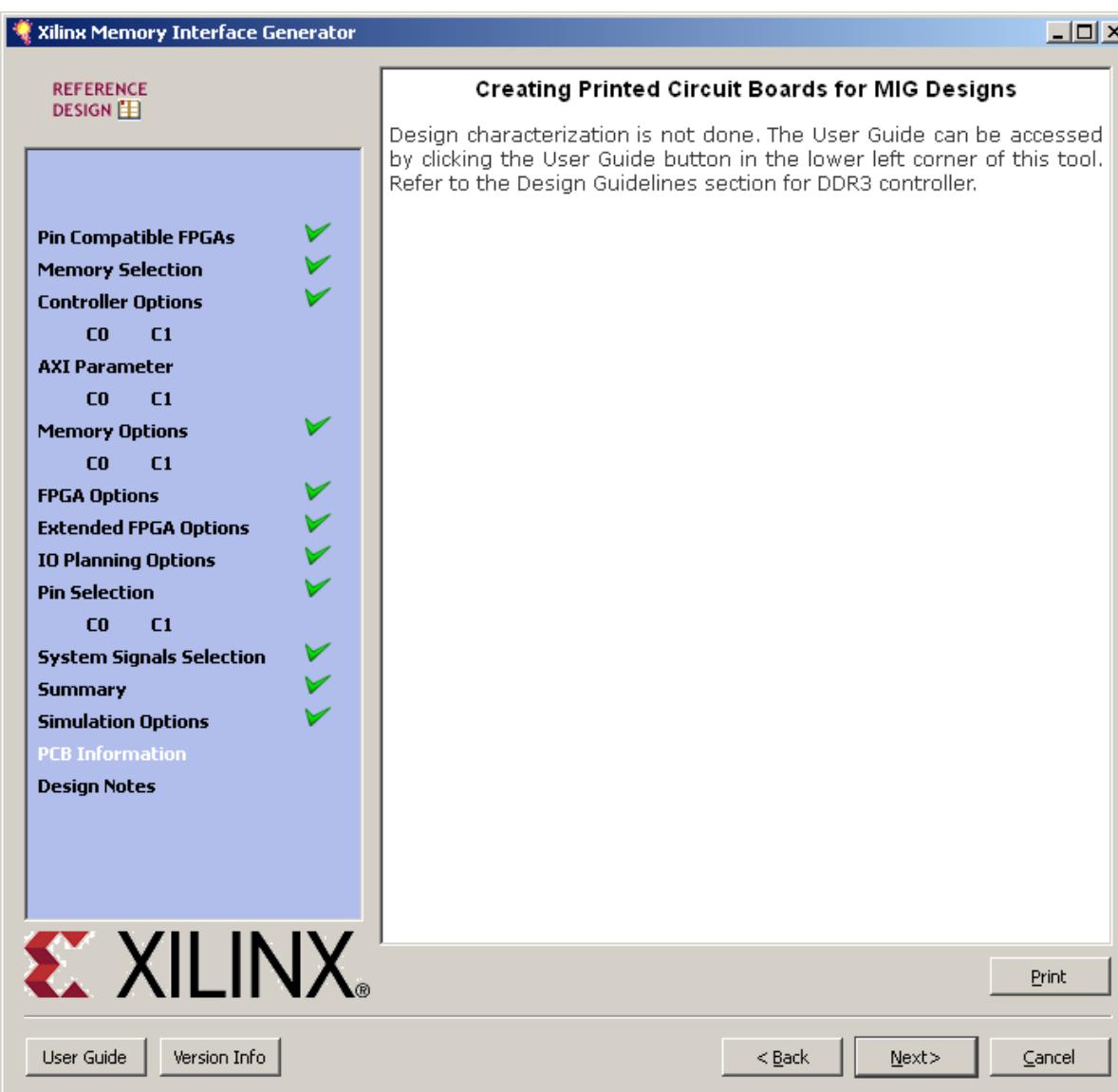
Generate MIG Bank A and B Example Design



➤ Accept Simulation license, if desired

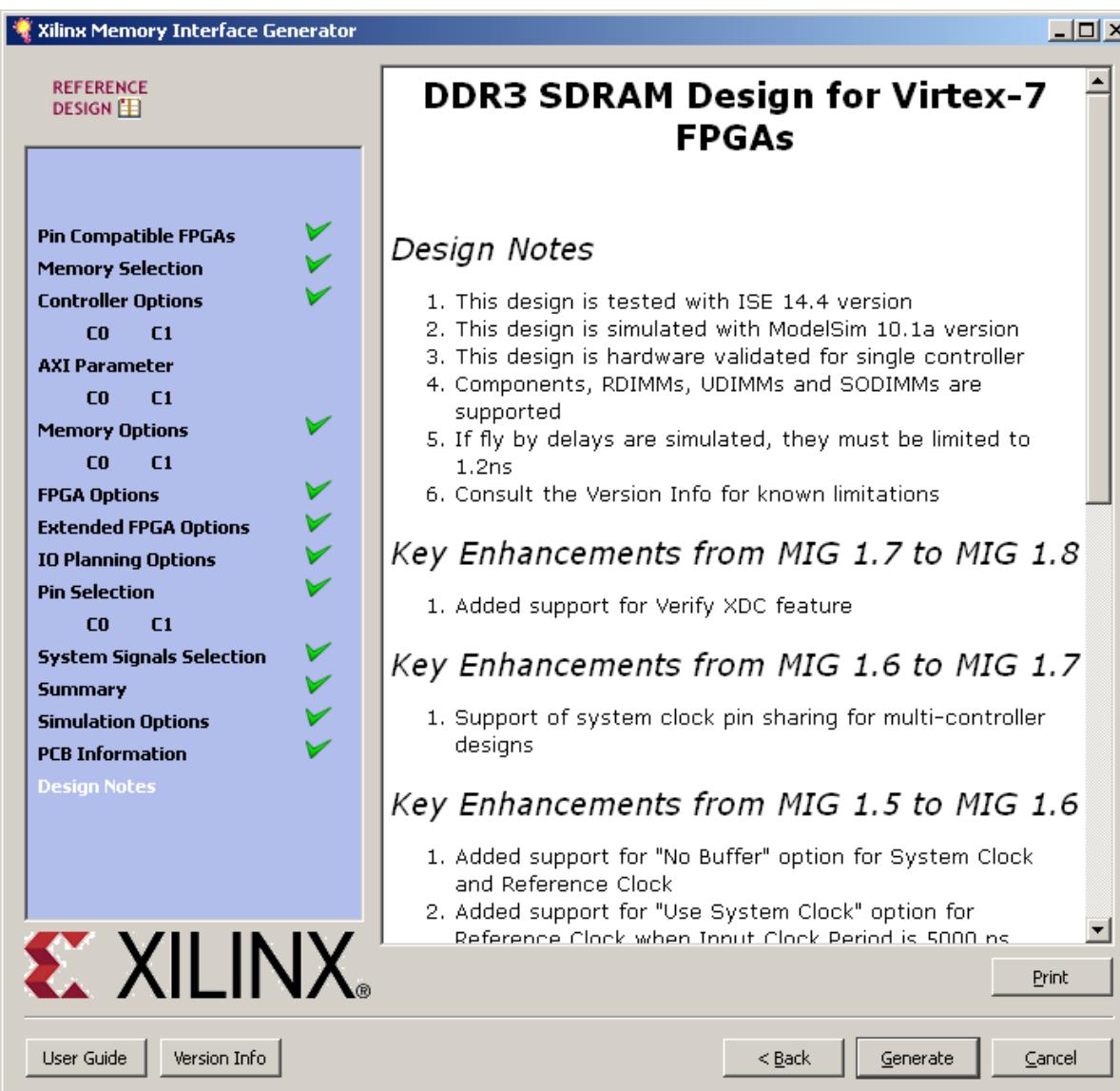
- Otherwise, Decline license
- Click Next

Generate MIG Bank A and B Example Design



➤ Leave this page as is
– Click Next

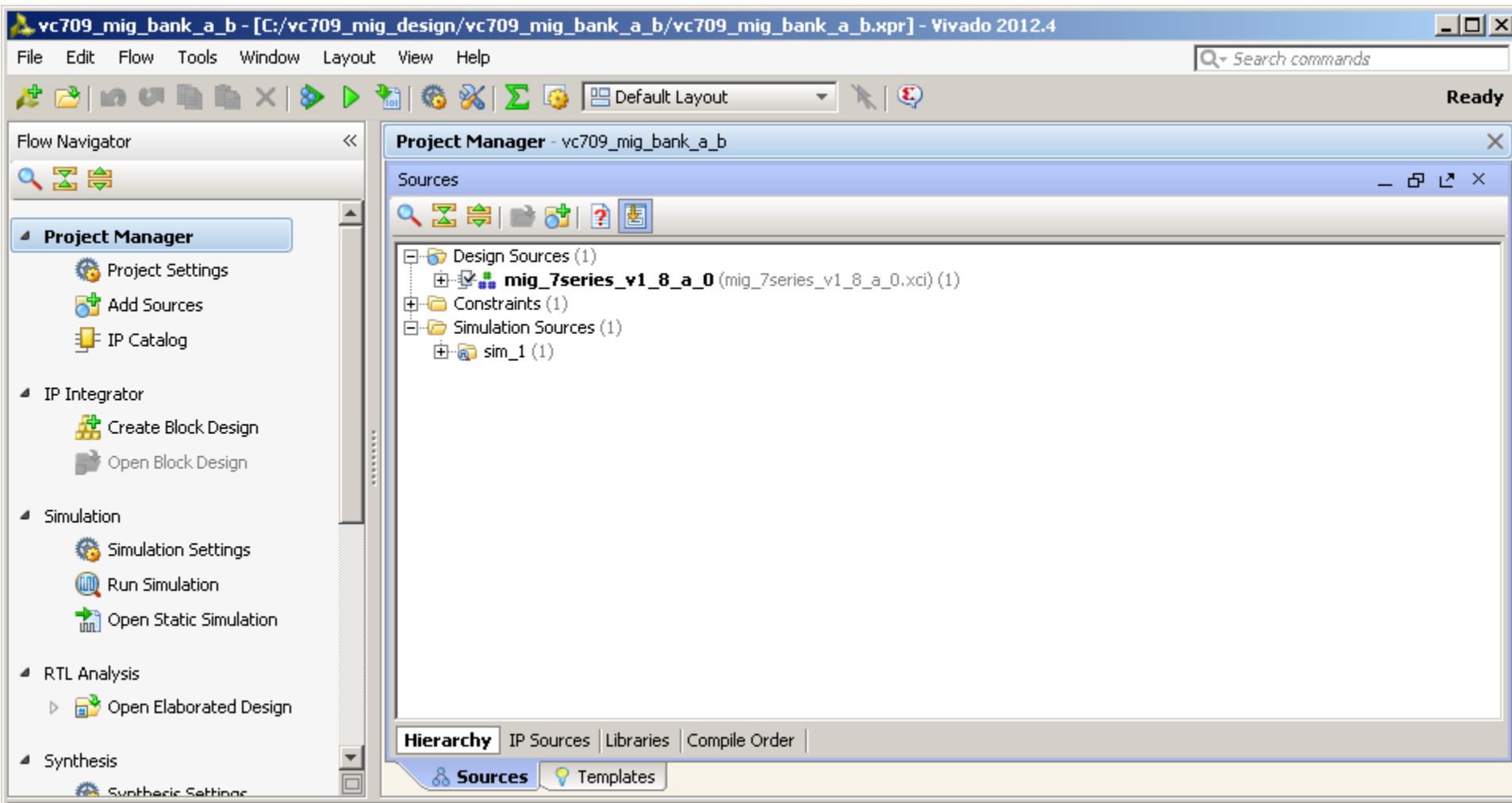
Generate MIG Bank A and B Example Design



► Click Generate

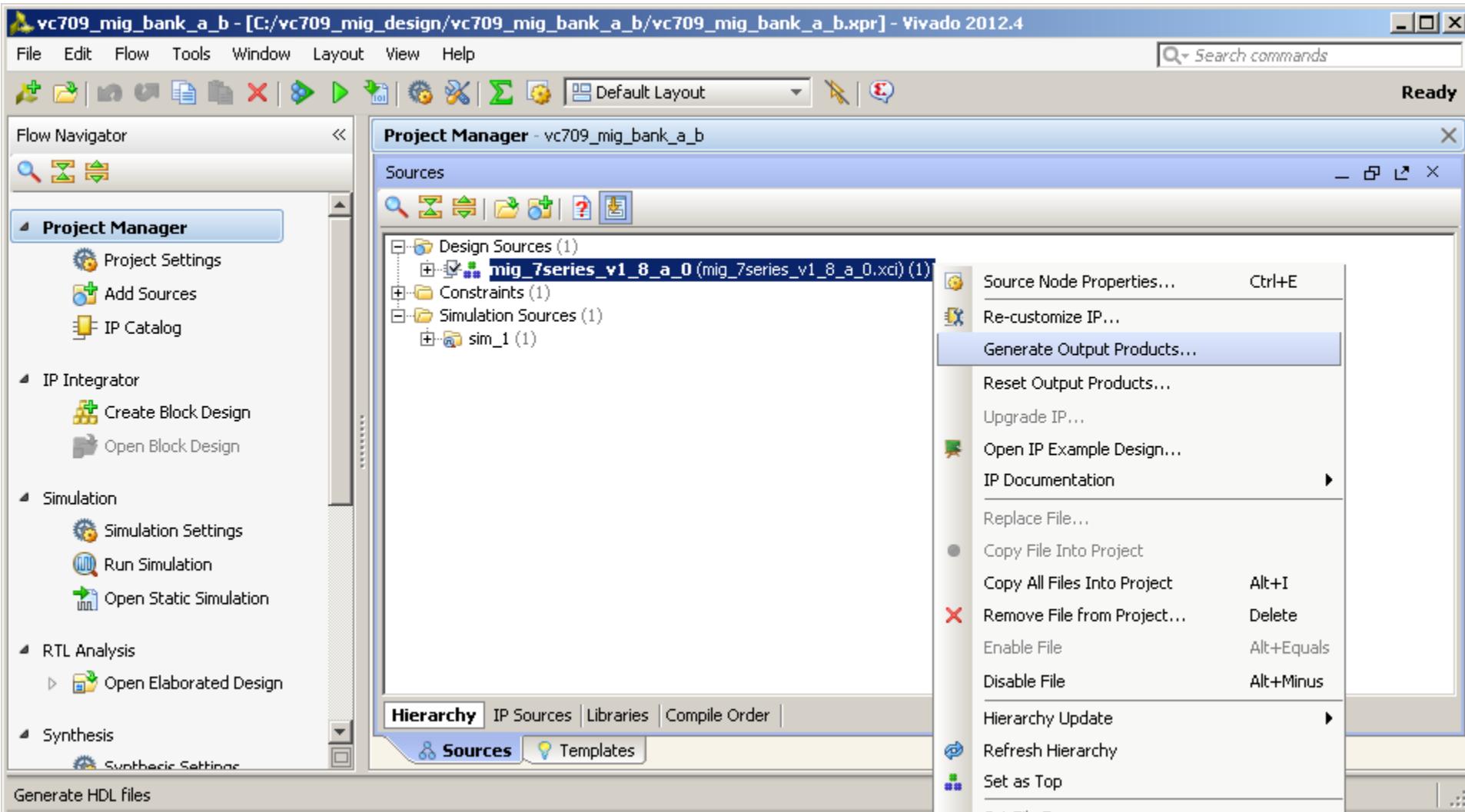
Generate MIG Bank A and B Example Design

► MIG design appears in Design Sources



Compile MIG Bank A and B Example Design

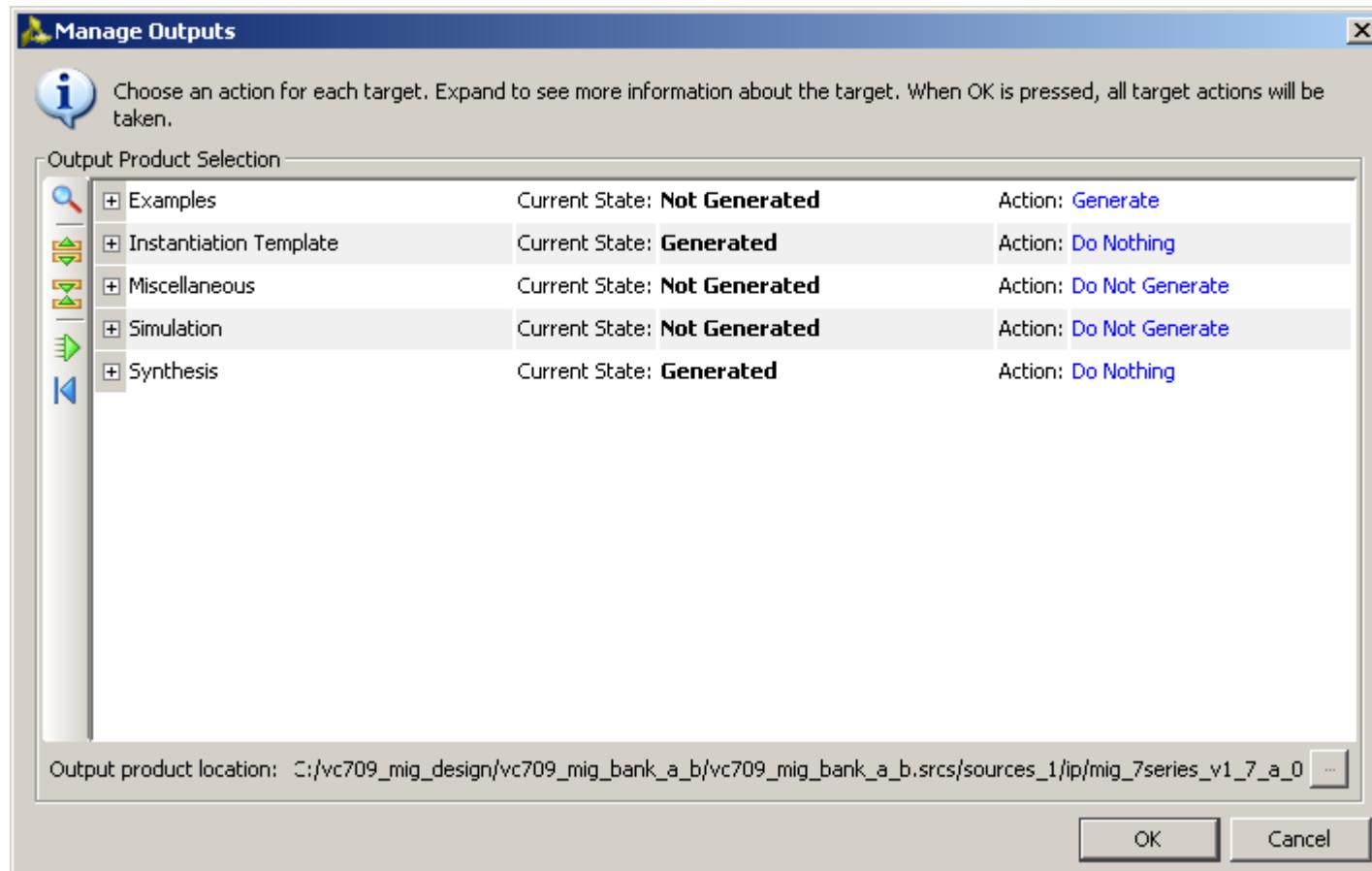
- Right-click on mig_7series_v1_8_a_0 and select Generate Output Products...



Note: Presentation applies to the VC709

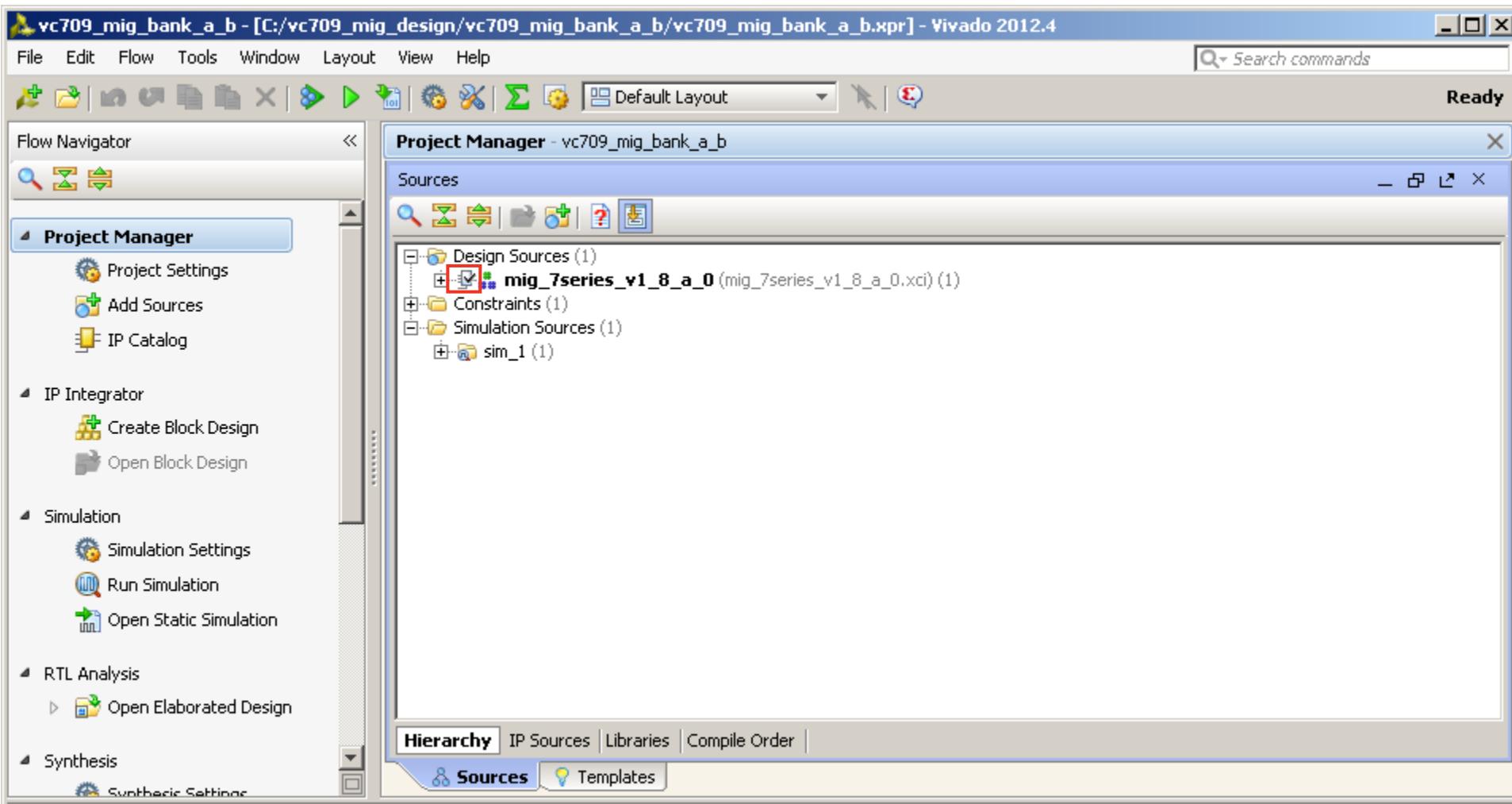
Compile MIG Bank A and B Example Design

- Select Examples as the target to generate



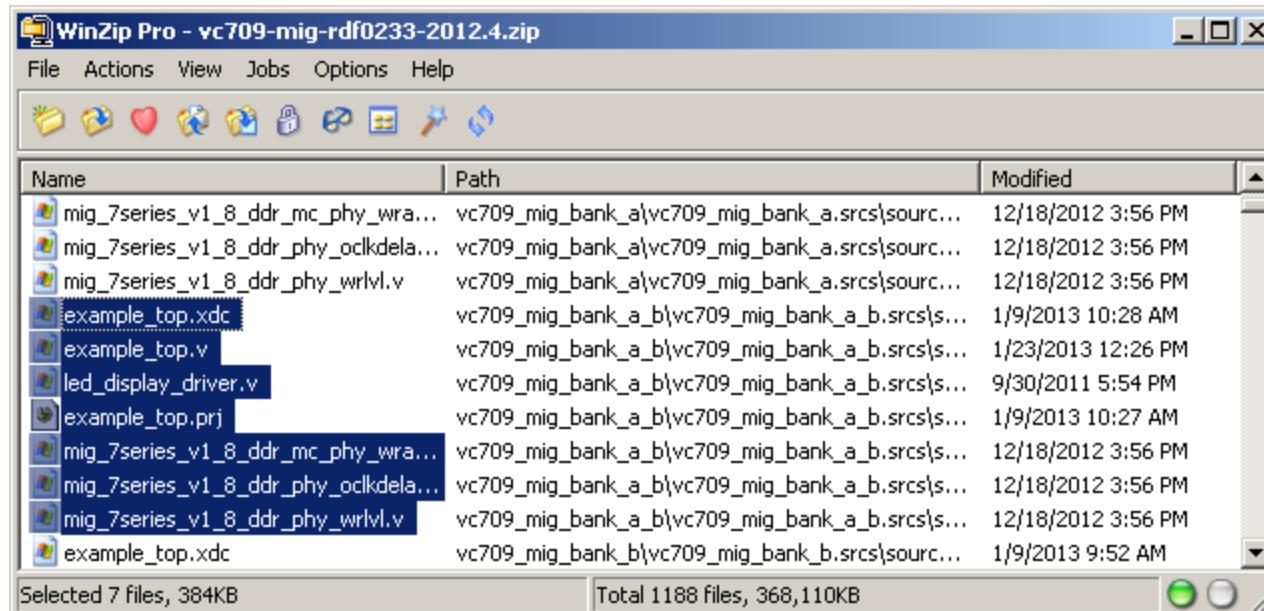
Compile MIG Bank A and B Example Design

► Once the Generate step is complete, a check (re)appears on the IP



Modifications to MIG Bank A & B Example Design

- Open the VC709 MIG Design Files (2012.4 CES) and extract these files to your C:\vc709_mig_design directory
 - vc709_mig_bank_a_b*
 - Contains several changes needed to support Virtex-7 devices with MIG, including [AR53420](#)



Modifications to MIG Bank A & B Example Design

► Modifications to the example design

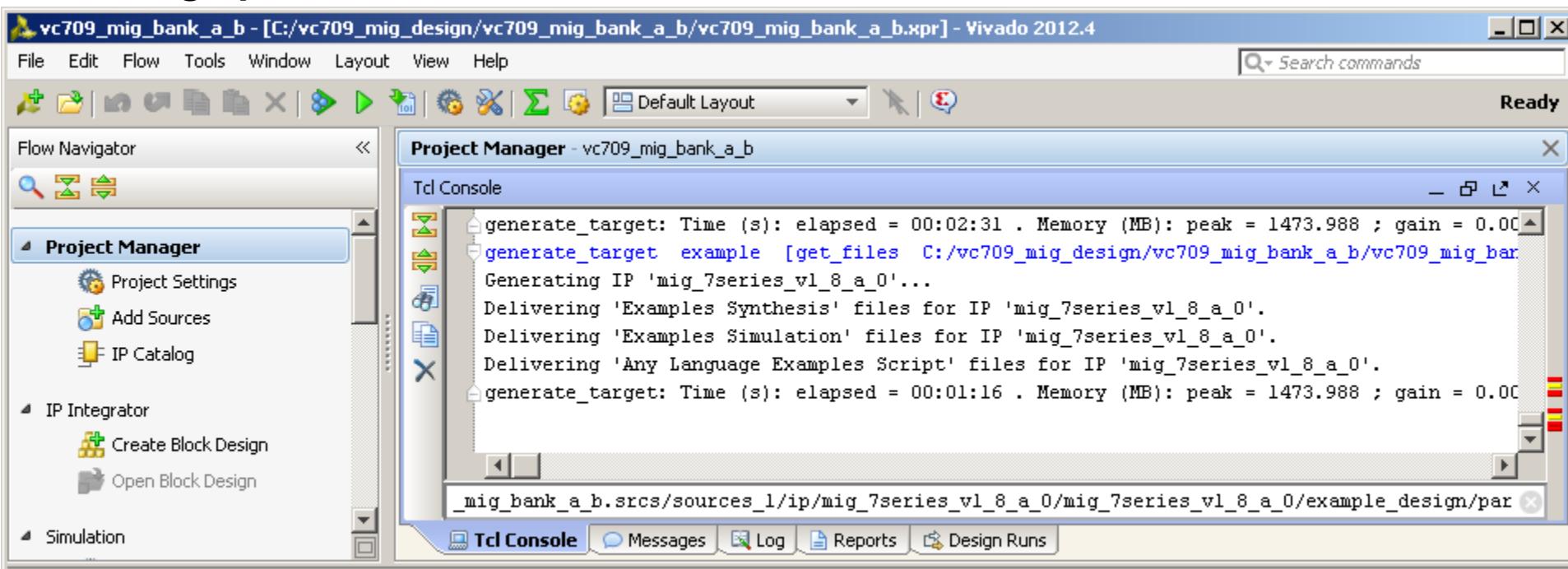
- Added RTL and XDC modifications to drive LEDs
- Changed RST_ACT_LOW to “0”; refer to [UG586](#) for more details on using the RST_ACT_LOW parameter
- Added [AR53420](#) – Required MIG Calibration Patch
- Additional modifications as required for two controller MIG design on the VC709

Compile MIG Bank A and B Example Design

► At the Tcl Console enter this command:

```
cd
```

```
C:/vc709_mig_design/vc709_mig_bank_a_b/vc709_mig_bank_a_b.srcs/sources_1/ip/mig_7series_v1_8_a_0/mig_7series_v1_8_a_0/example_design/par
```

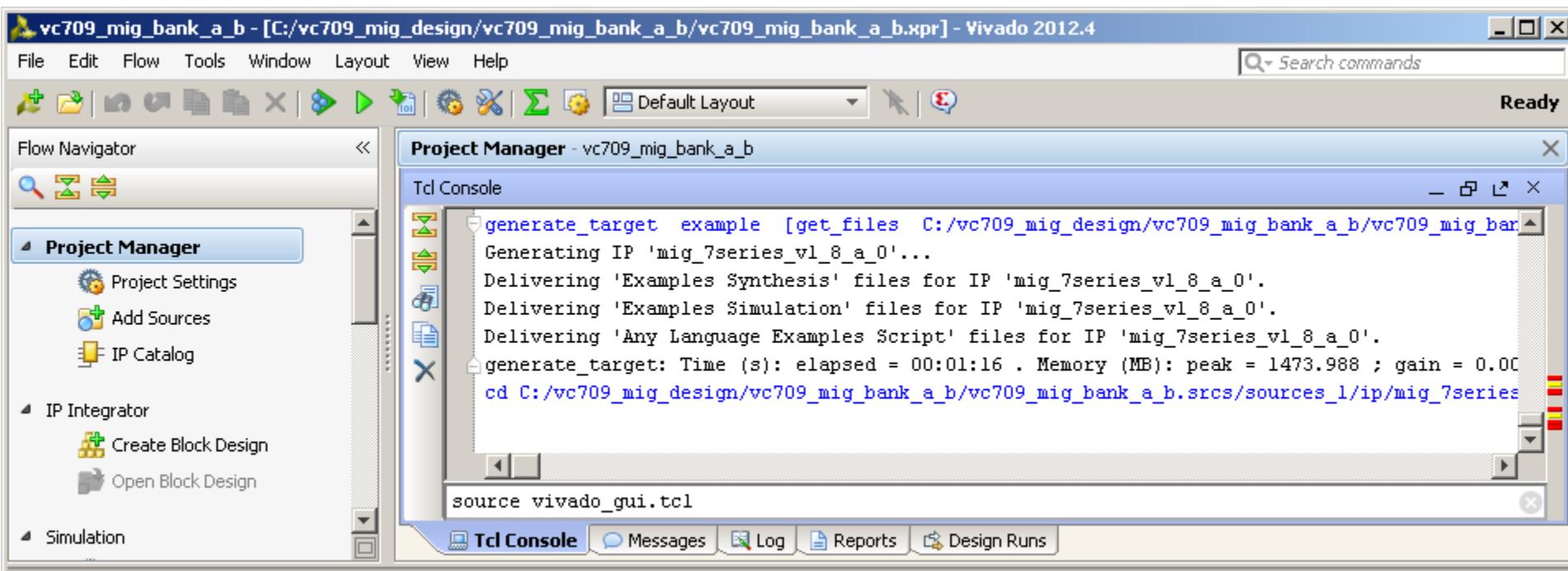


Compile MIG Bank A and B Example Design

► At the Tcl Console enter this command:

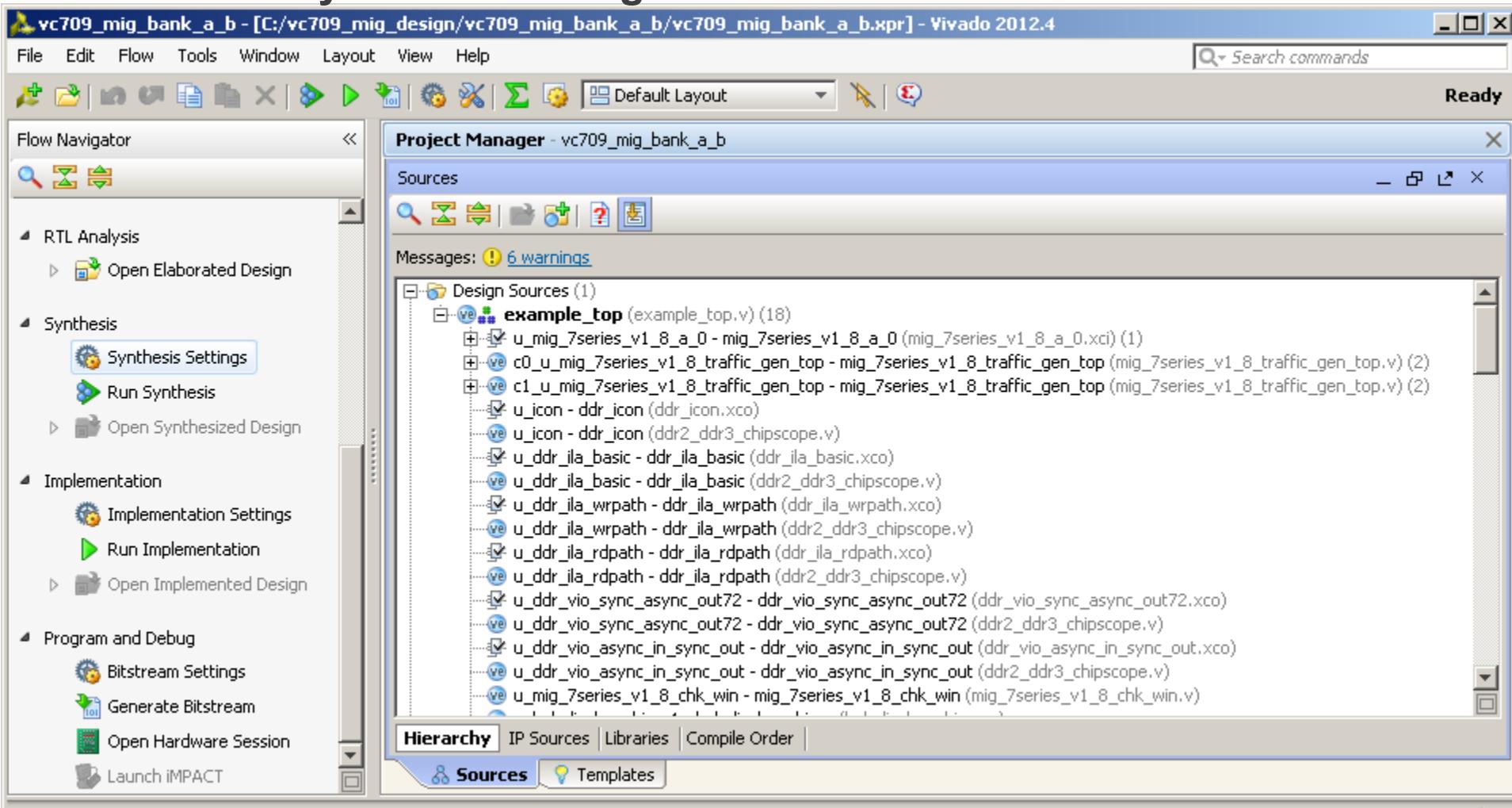
```
source vivado_gui.tcl
```

► This command adds the necessary design files and compiles the ChipScope IP



Compile MIG Bank A and B Example Design

- The design files, IP and constraints have been added/generated
- Click on Synthesis Settings

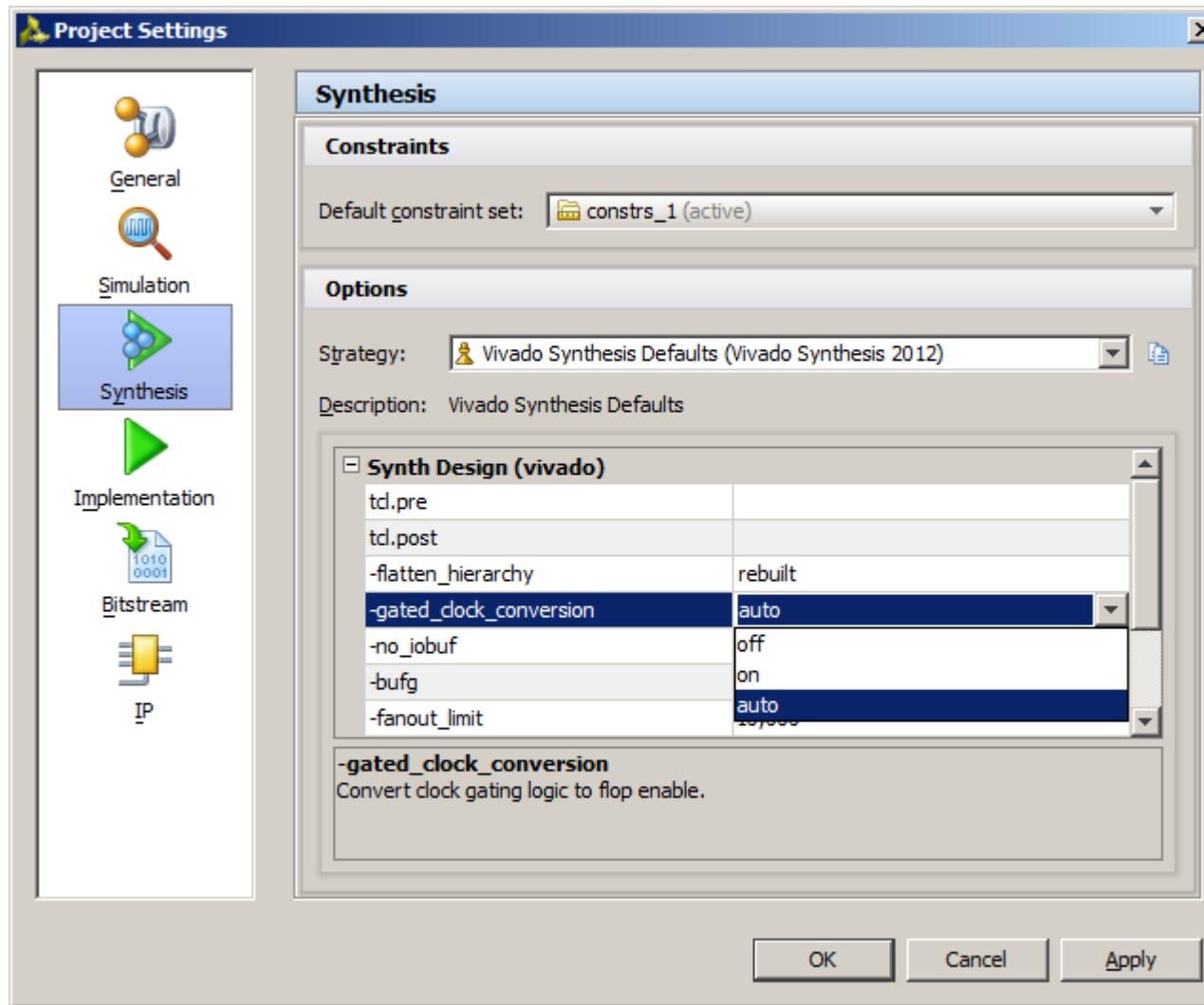


Note: Presentation applies to the VC709

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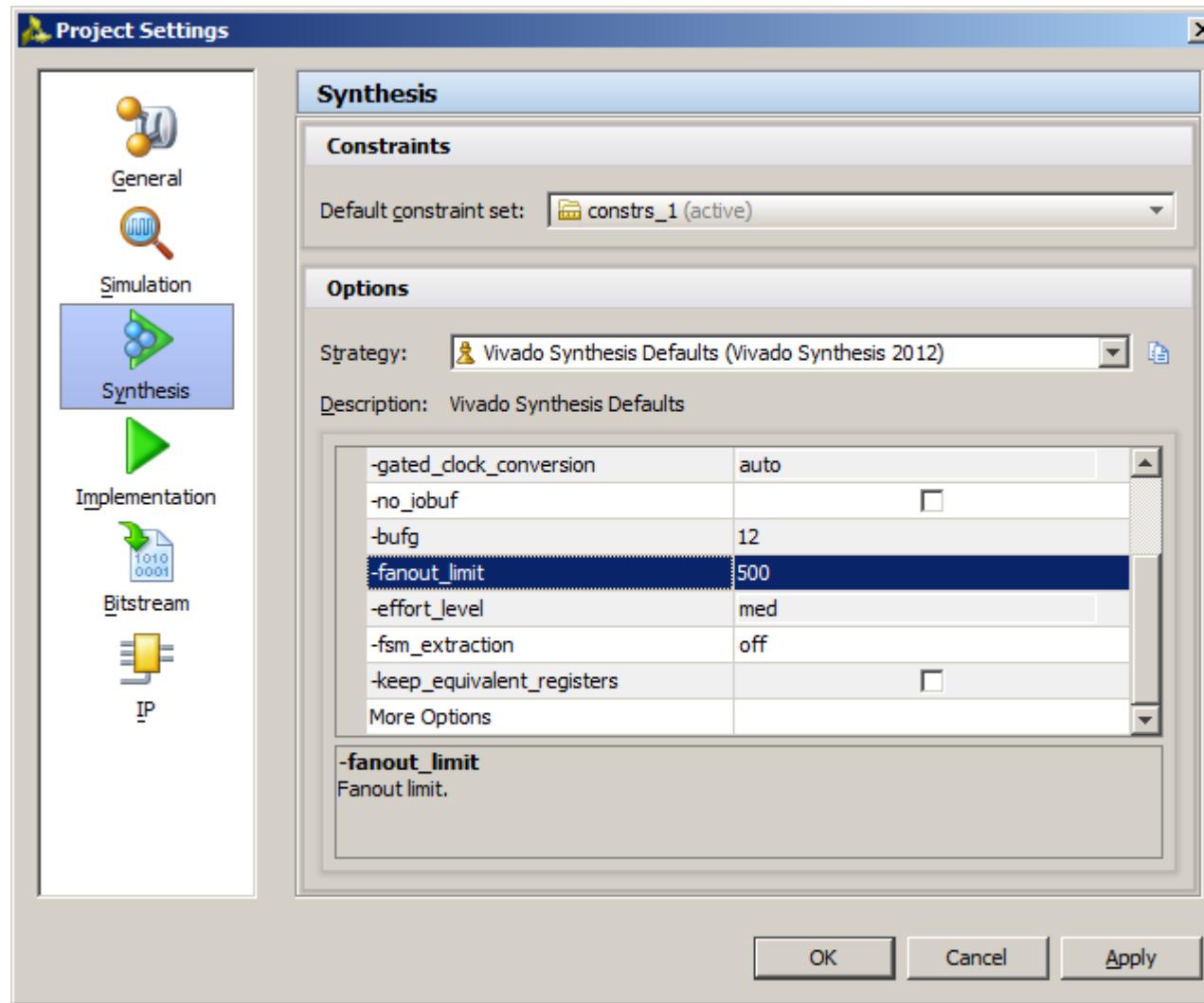
Compile MIG Bank A and B Example Design

- Set the `gated_clock_conversion` to auto



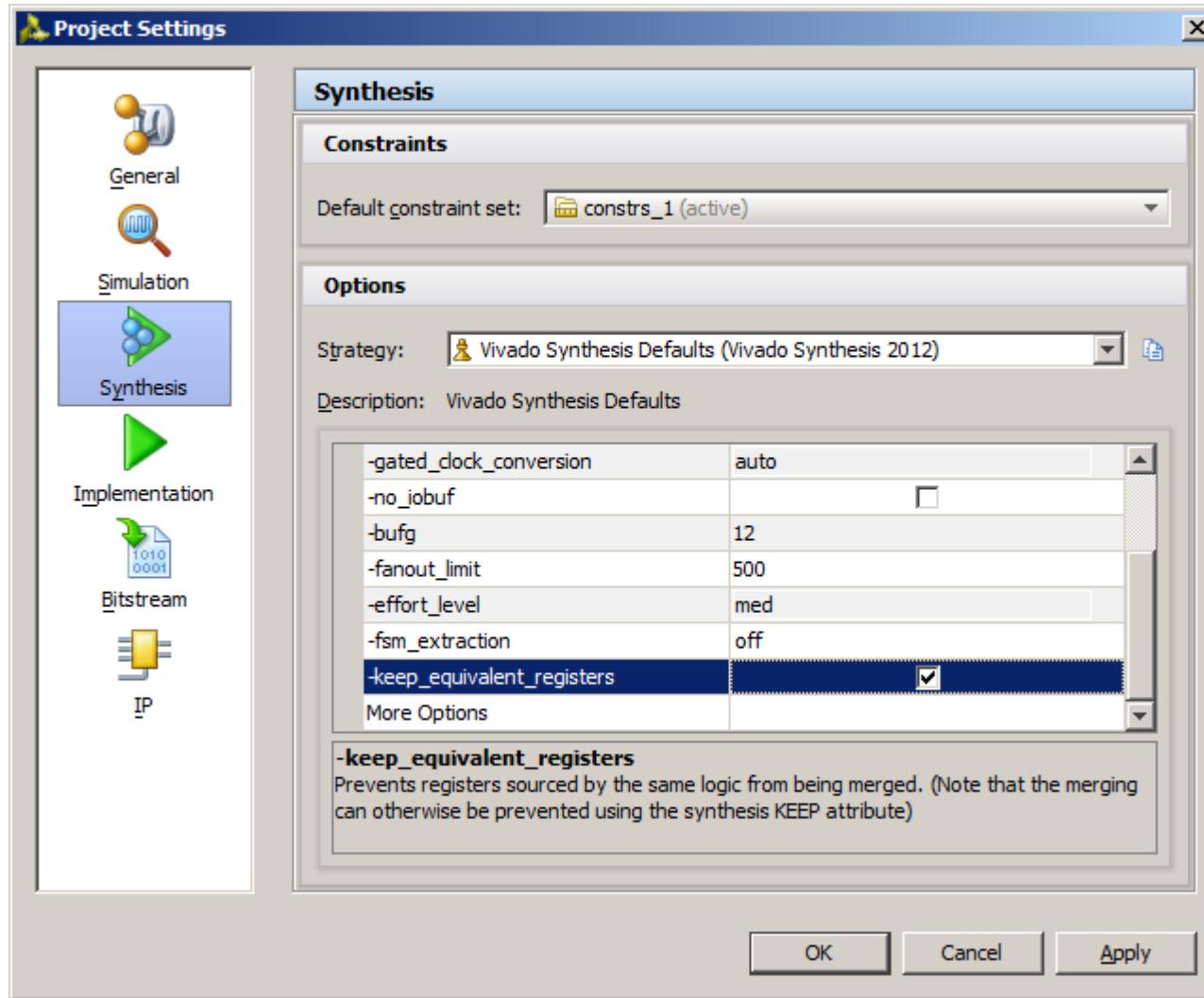
Compile MIG Bank A and B Example Design

- Set the fanout_limit to 500



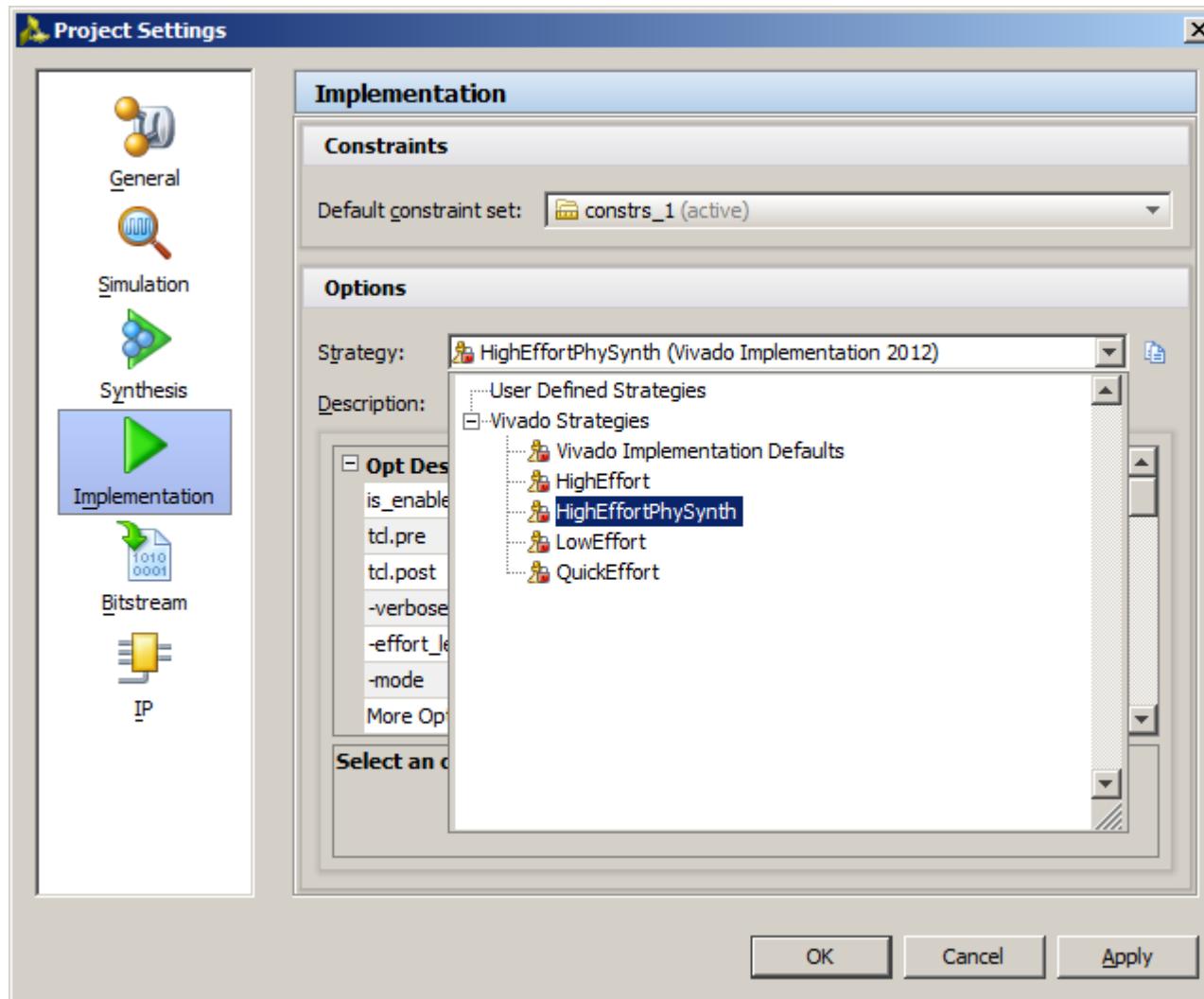
Compile MIG Bank A and B Example Design

- Check the `keep_equivalent_registers` option



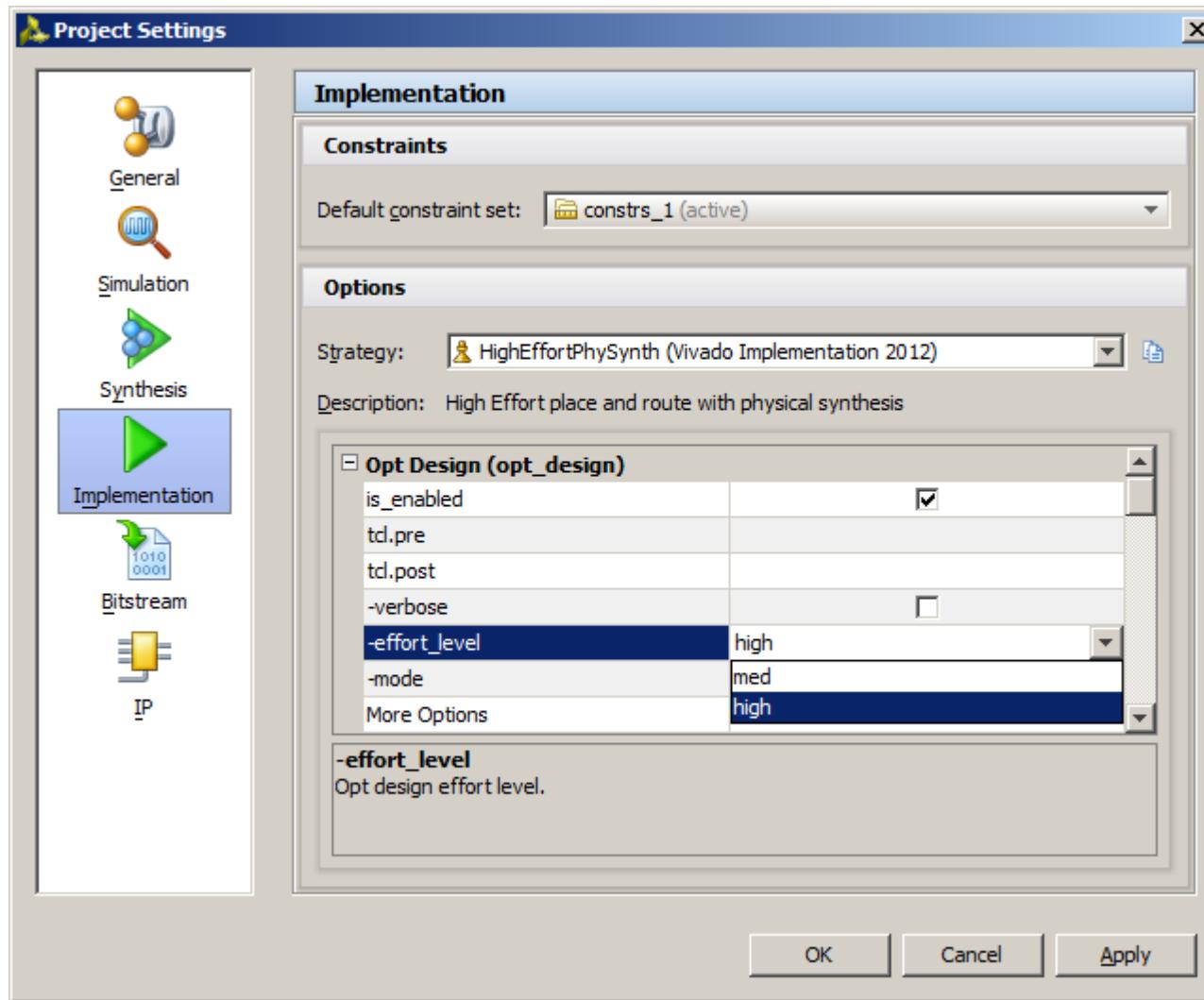
Compile MIG Bank A and B Example Design

► Select Implementation and select HighEffortPhySynth



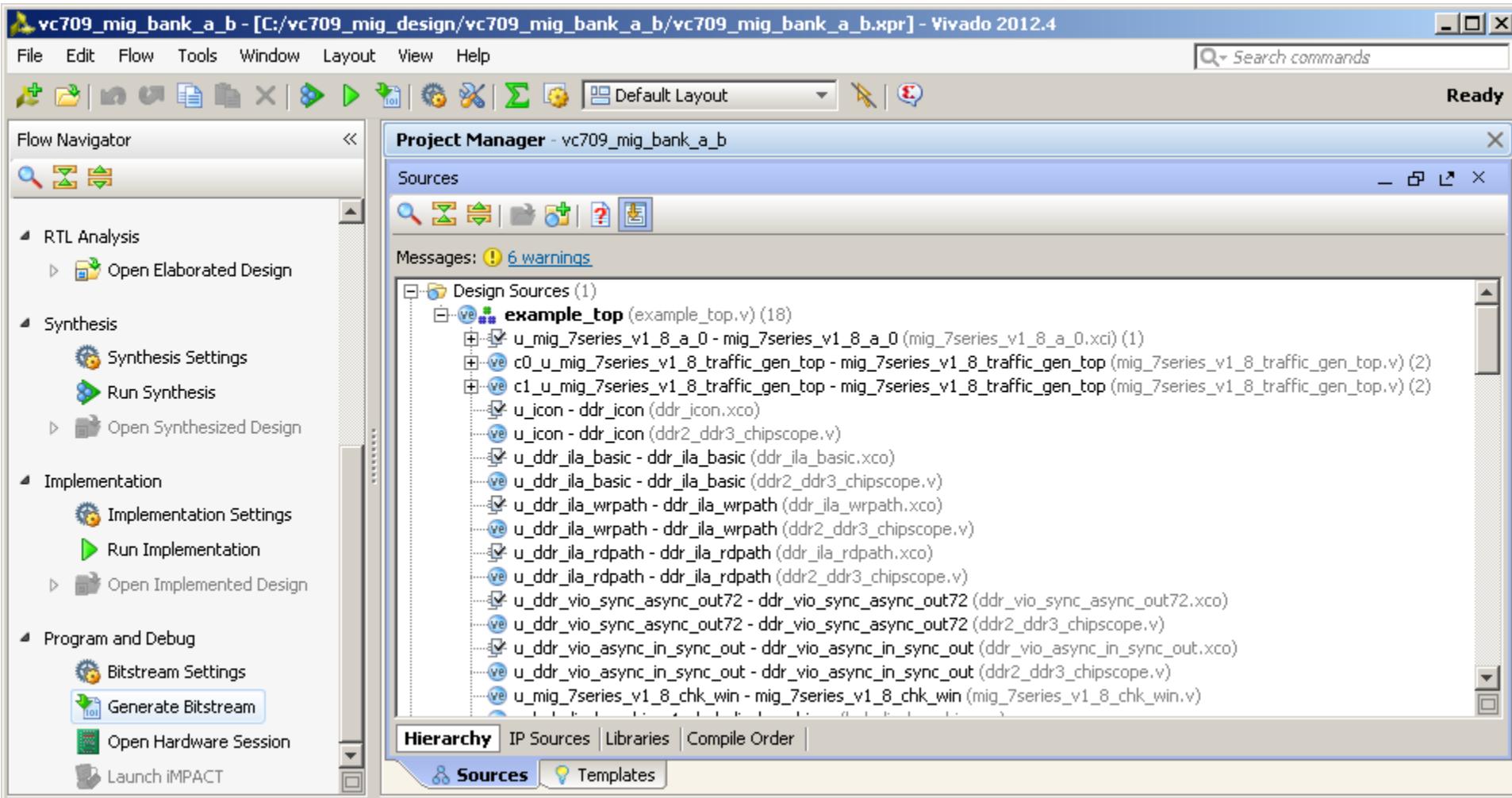
Compile MIG Bank A and B Example Design

- Under Opt Design set **effort_level** to high



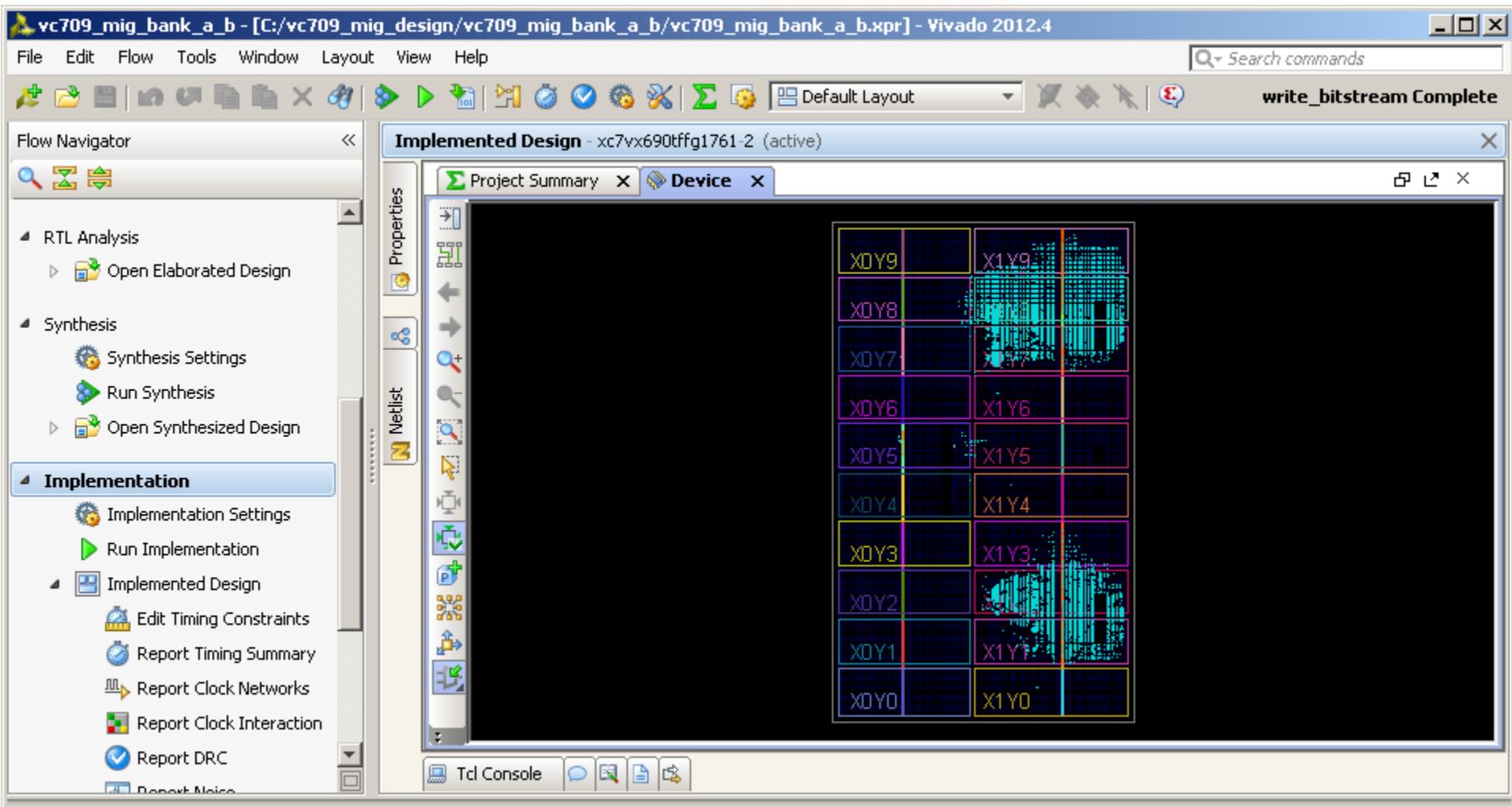
Compile MIG Bank A and B Example Design

► Click on Generate Bitstream



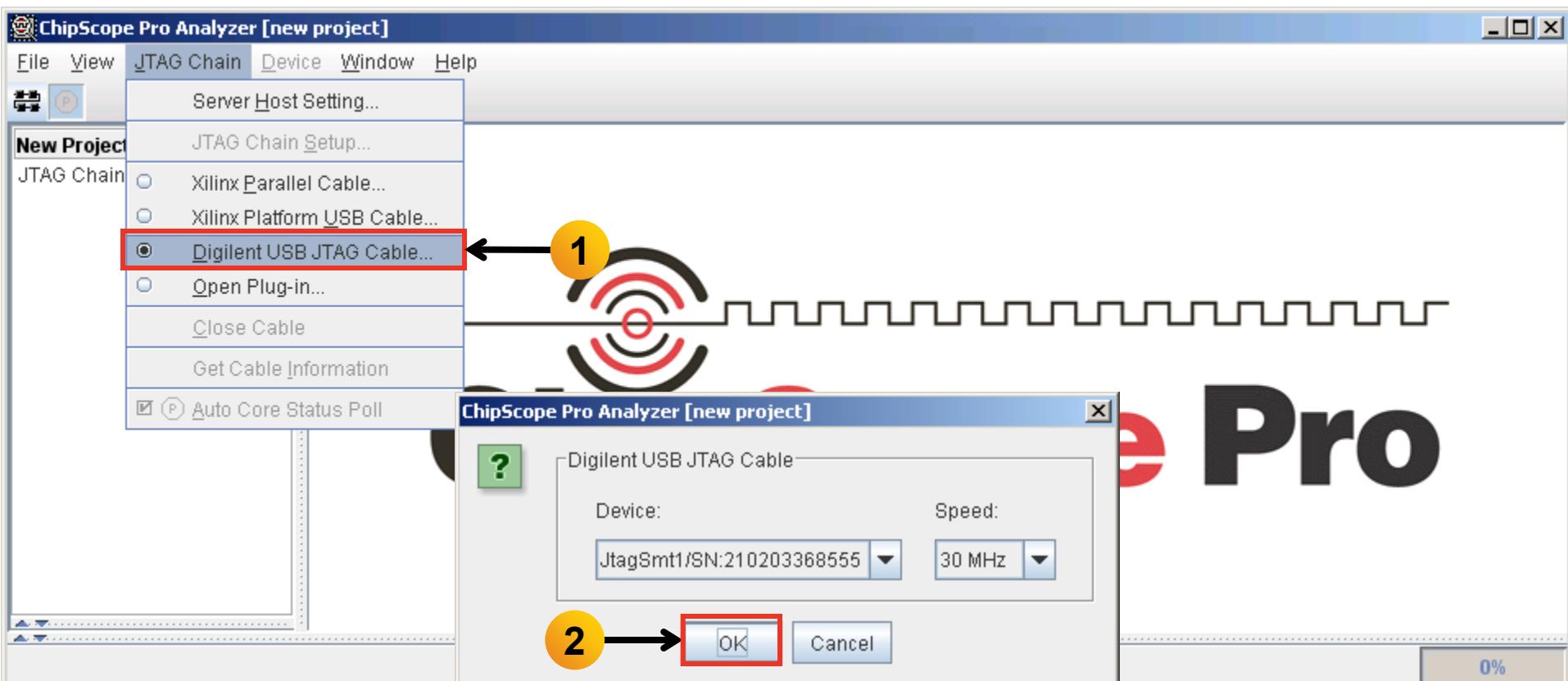
Compile MIG Bank A and B Example Design

► Open and view the completed design



Run MIG Bank A and B Example Design

- Open ChipScope Pro and select JTAG Chain → Digilent USB Cable... (1)
- Verify 30 MHz operation and click OK (2)



Run MIG Bank A and B Example Design

► Click OK (1)

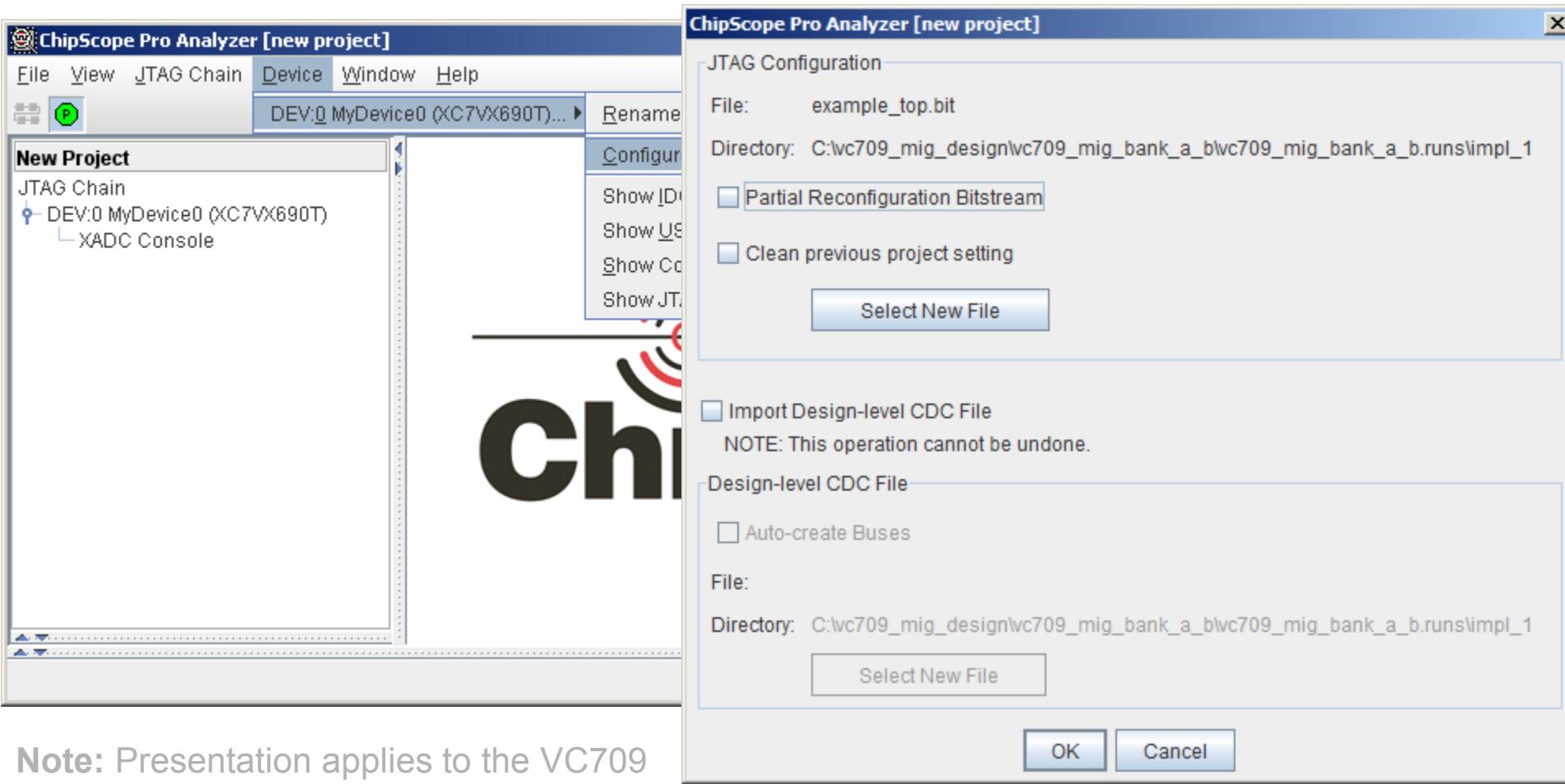


Run MIG Bank A and B Example Design

► Select Device → DEV:0 MyDevice0 (XC7VX690T) → Configure...

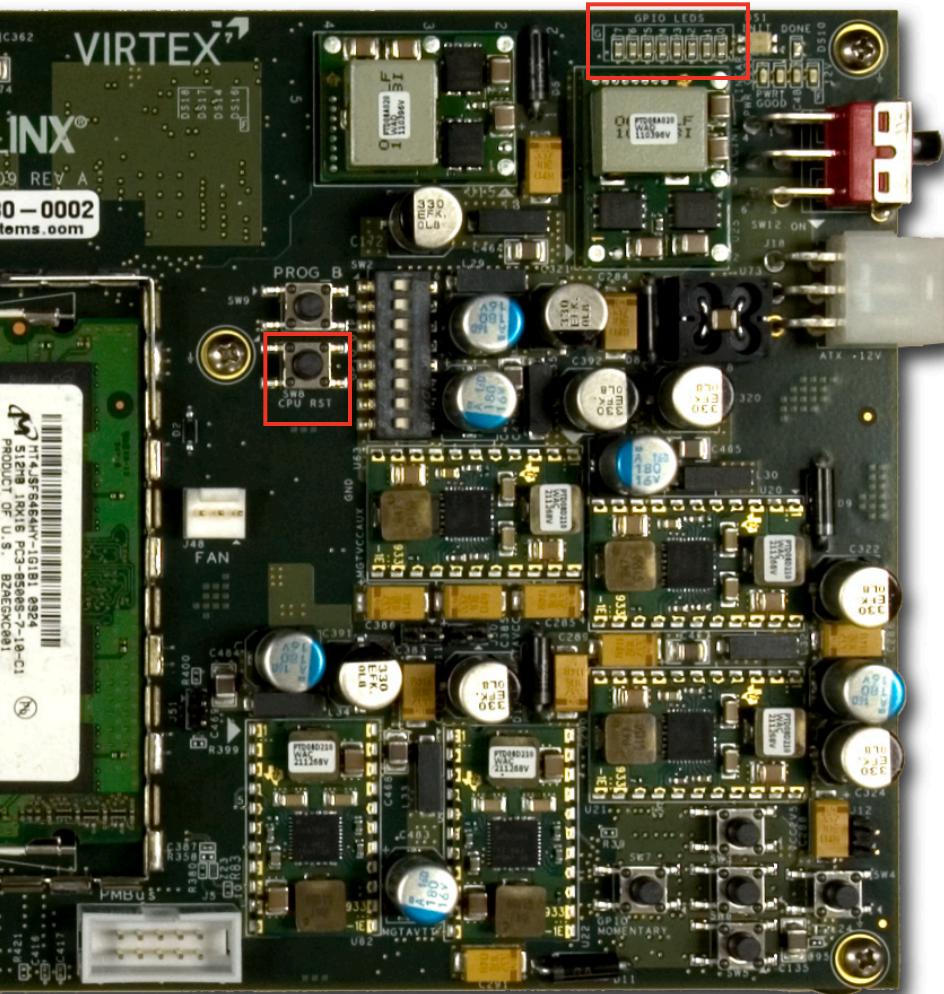
► Select <Design

Path>\vc709_mig_bank_a_b\vc709_mig_bank_a_b.runs\impl_1\example_top.bit



Note: Presentation applies to the VC709

Run MIG Bank A and B Example Design



► Controller 0:

- LED 0 (right most LED) will be lit, and LED1 will be blinking
- LED 3 will light and stay on
- This indicates Calibration has completed
- If an error occurs, LED 0 will go out and LED 2 will light

► Controller 1:

- LED 4 will be lit, and LED5 will be blinking
- LED 7 will light and stay on
- This indicates Calibration has completed
- If an error occurs, LED 4 will go out and LED 6 will light

► SW8 is the reset

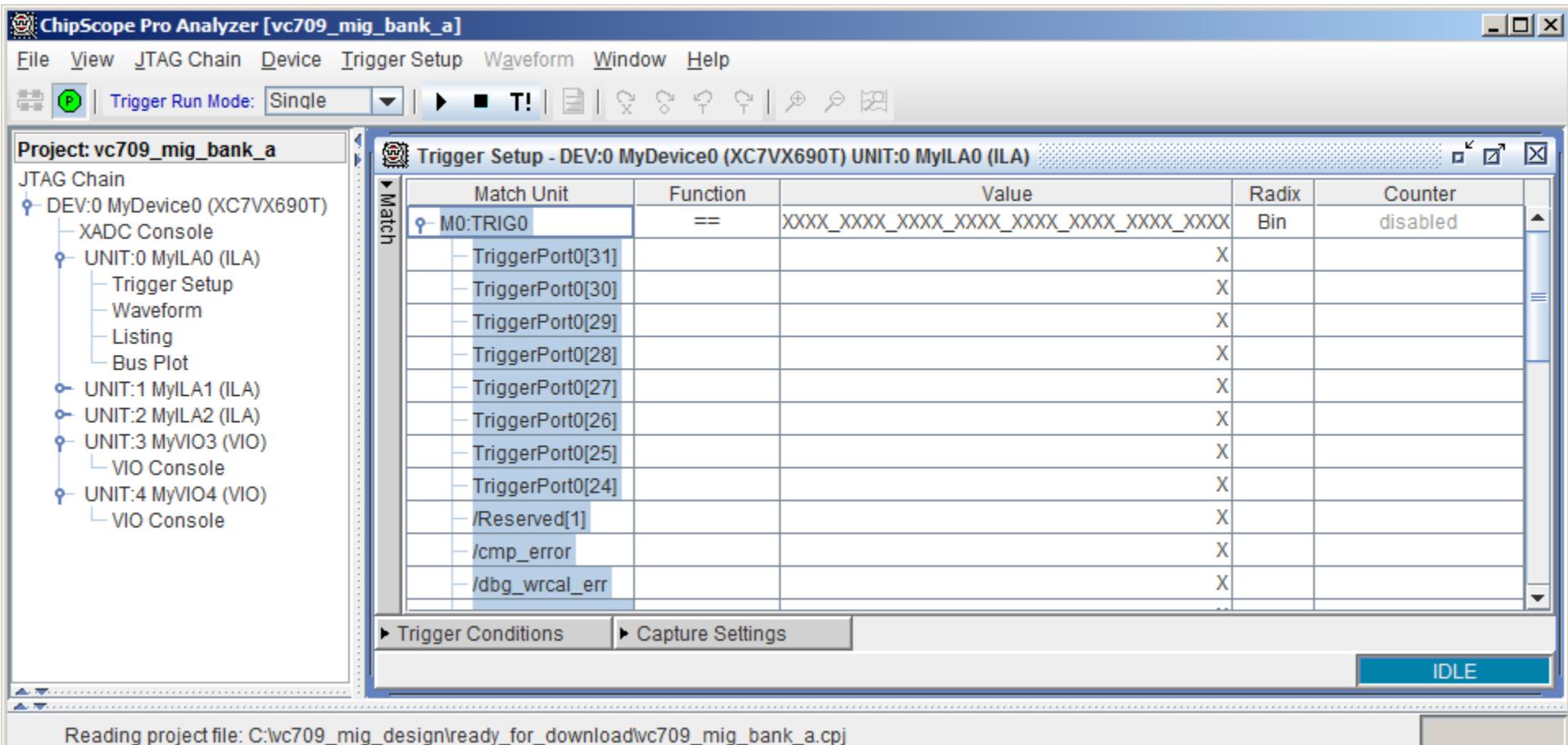
Run MIG Bank A and B Example Design

- Select File → Open Project...
- Select <Design Path>\ready_for_download\vc709_mig_bank_a.cpj



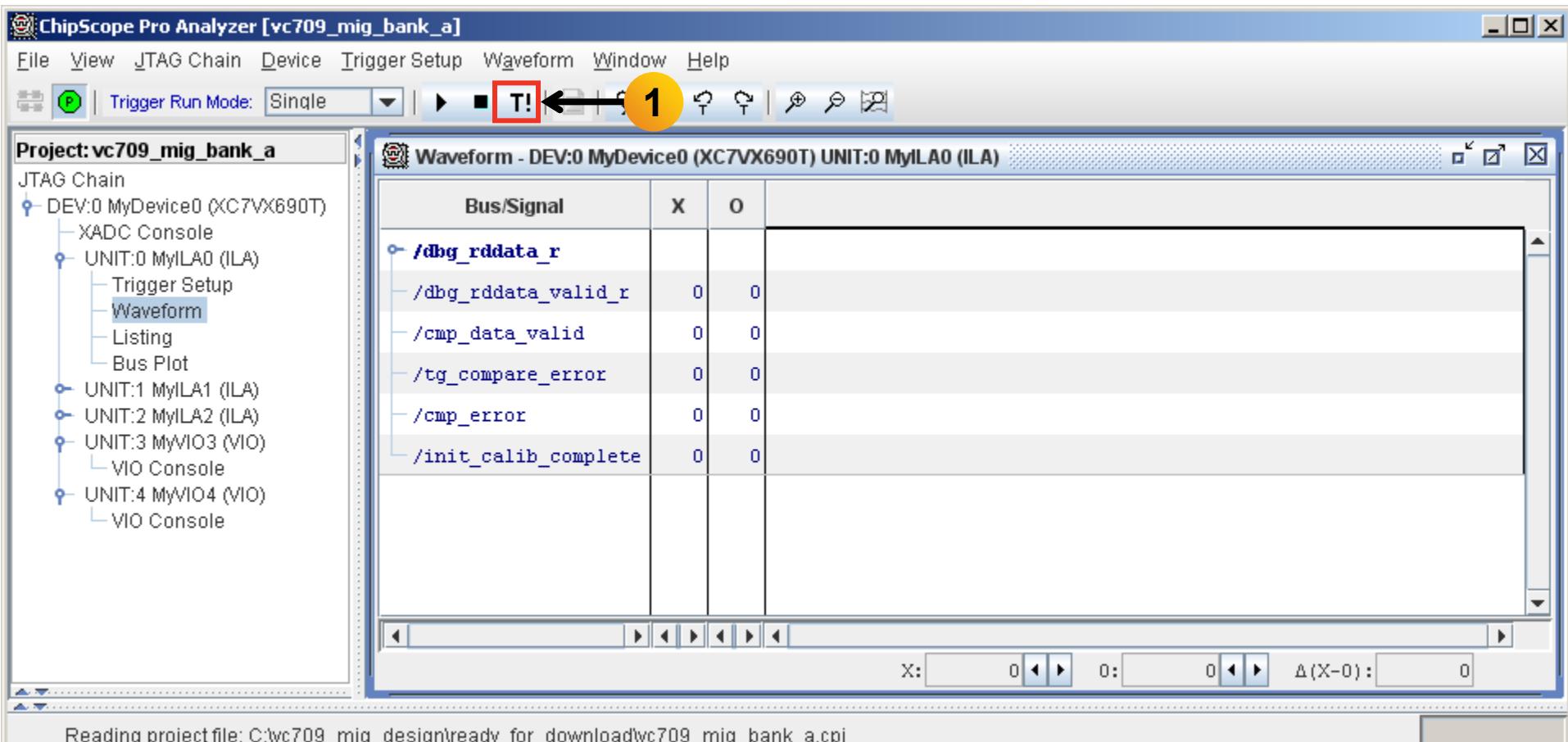
Run MIG Bank A and B Example Design

► Click on Trigger Setup to view trigger settings



Run MIG Bank A and B Example Design

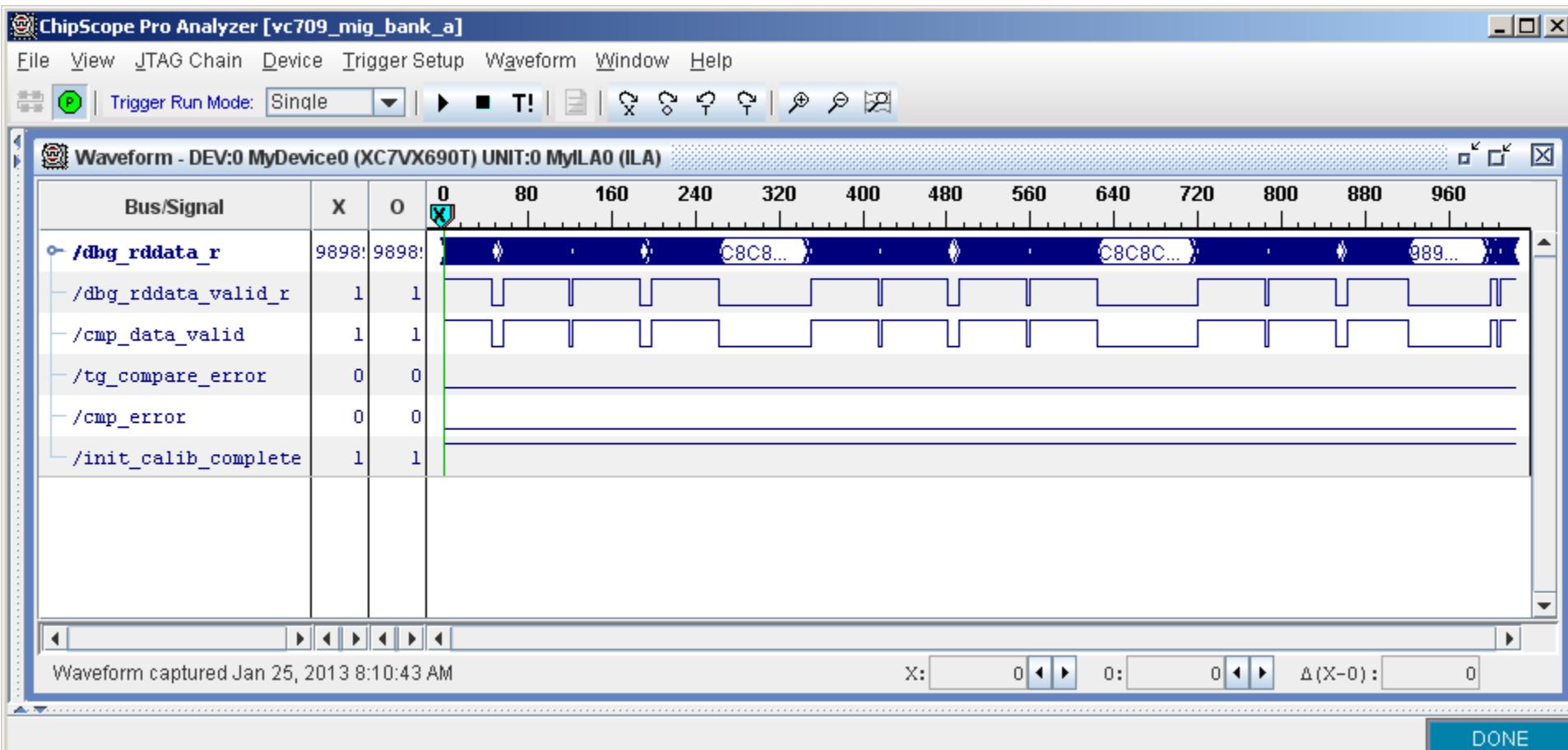
► Click on Waveform; click the Trigger Immediate button (1)



Reading project file: C:\vc709_mig_design\ready_for_download\vc709_mig_bank_a.cpj

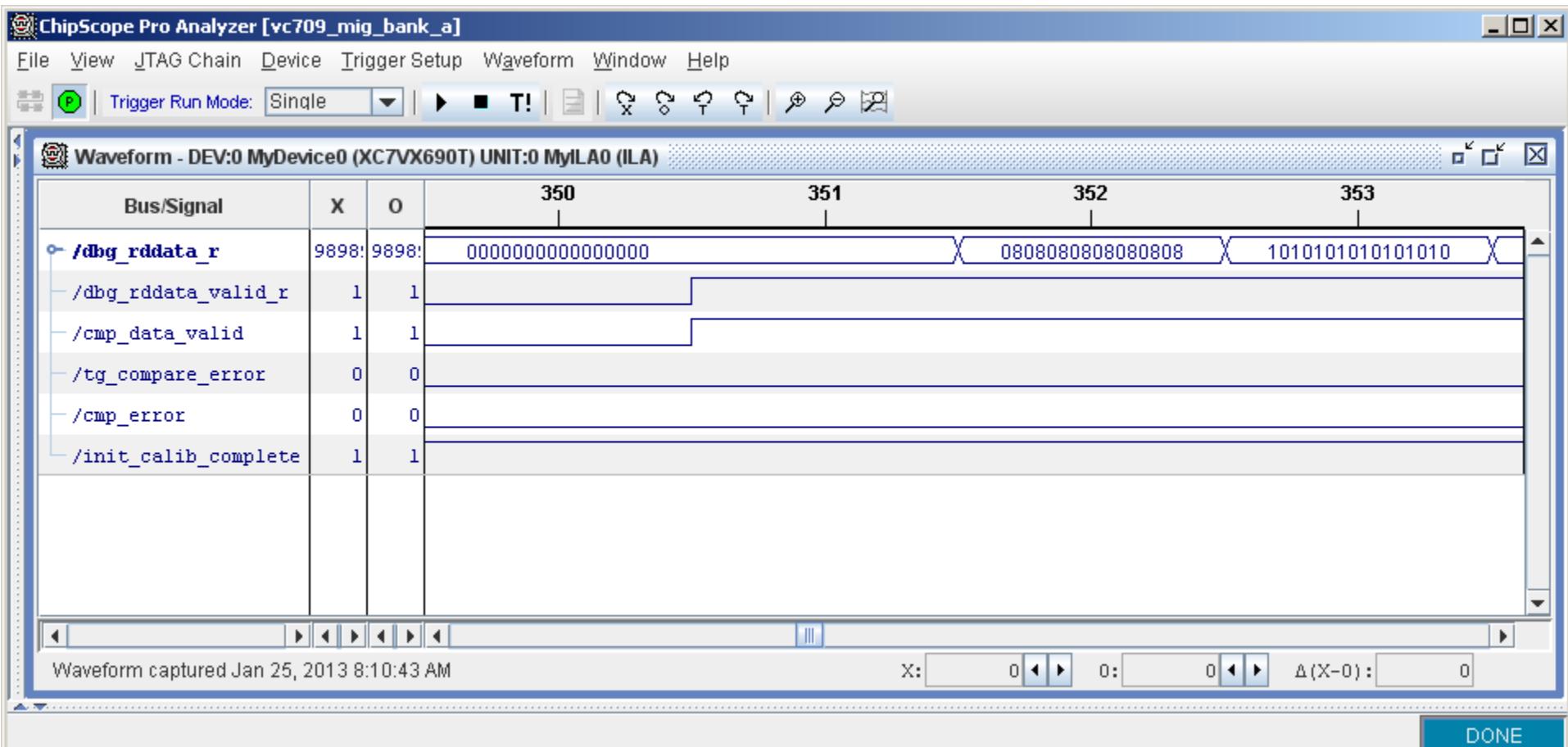
Run MIG Bank A and B Example Design

- View waveforms
- Data is valid when `dbg_rddata_valid` is high



Run MIG Bank A and B Example Design

► Zoom in to view data



Adjust Data Pattern using VIO Console

- Select VIO Console 3
- Set `vio_modify_enable` to 1

The screenshot shows the ChipScope Pro Analyzer interface with the title bar "ChipScope Pro Analyzer [vc709_mig_bank_a]". The menu bar includes File, View, JTAG Chain, Device, VIO, Window, and Help. A toolbar below the menu bar has icons for JTAG Scan Rate (set to 250 ms), and status indicators S!, U!, and a red asterisk. The left sidebar displays the project structure under "Project: vc709_mig_bank_a": JTAG Chain, DEV:0 MyDevice0 (XC7VX690T) containing XADC Console, UNIT:0 MyILA0 (ILA) with Trigger Setup, Waveform, Listing, Bus Plot; UNIT:1 MyILA1 (ILA); UNIT:2 MyILA2 (ILA); UNIT:3 MyVIO3 (VIO) with VIO Console selected; and UNIT:4 MyVIO4 (VIO) with VIO Console. The main window is titled "VIO Console - DEV:0 MyDevice0 (XC7VX690T) UNIT:3 MyVIO3 (VIO)". It contains a table with columns "Bus/Signal" and "Value". The "vio_modify_enable" signal is set to 1, which is highlighted with a red rectangle. Other signals listed include vio_data_mask_gen, vio_pause_traffic, dbg_clear_error, vio_addr_mode_value (3), vio.bl_mode_value (2), vio.fixed.bl_value (16), vio.fixed.instr.value (1), vio.instr.mode.value (2), and vio.data.mode.value (2). A "DONE" button is at the bottom right of the table.

Bus/Signal	Value
vio_modify_enable	1
vio_data_mask_gen	0
vio_pause_traffic	0
dbg_clear_error	0
vio_addr_mode_value	3
vio.bl_mode_value	2
vio.fixed.bl_value	16
vio.fixed.instr.value	1
vio.instr.mode.value	2
vio.data.mode.value	2

Adjust Data Pattern using VIO Console

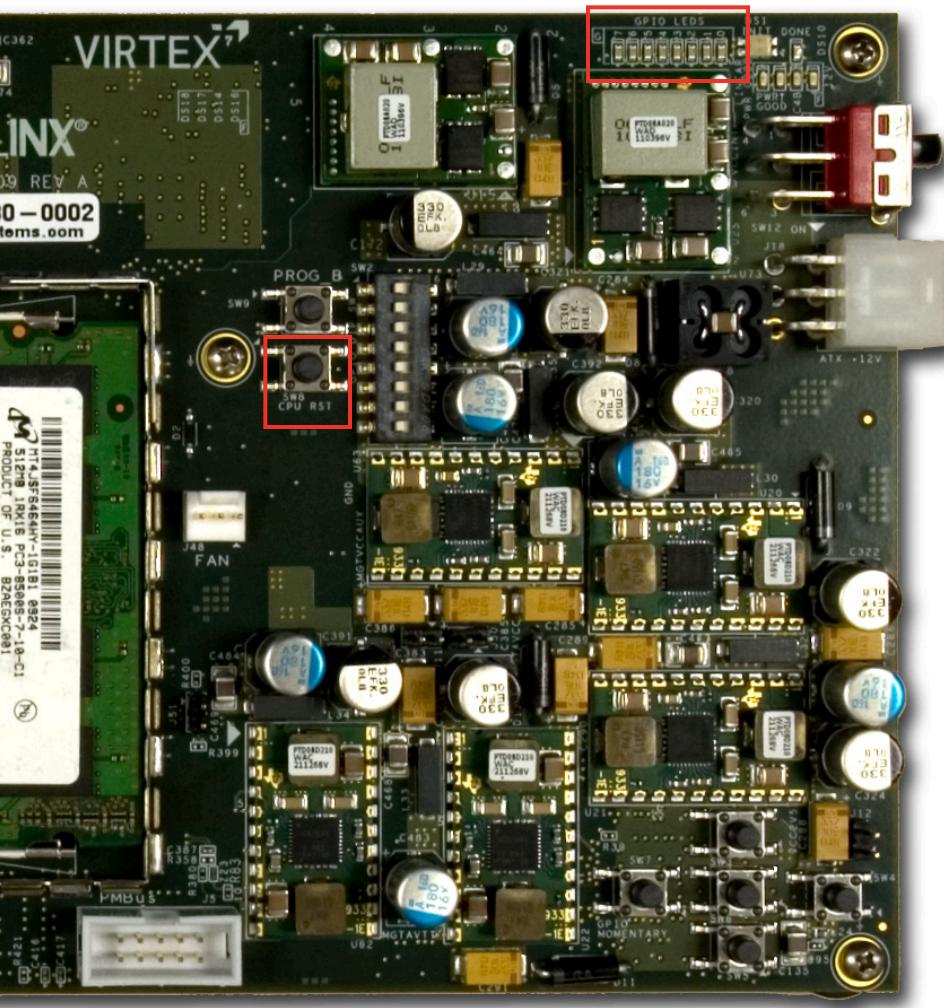
- Set `vio_data_mode_value` to “7” for `PRBS_DATA`

The screenshot shows the ChipScope Pro Analyzer interface with the title bar "ChipScope Pro Analyzer [vc709_mig_bank_a]". The menu bar includes File, View, JTAG Chain, Device, VIO, Window, and Help. A toolbar below the menu bar has icons for Power (green circle), JTAG Scan Rate (250 ms), Stop (S!), Run (U!), Scope (S), and Stop (red asterisk). The left sidebar displays the project structure under "Project: vc709_mig_bank_a": JTAG Chain, DEV:0 MyDevice0 (XC7VX690T), XADC Console, UNIT:0 MyILA0 (ILA), Trigger Setup, Waveform, Listing, Bus Plot, UNIT:1 MyILA1 (ILA), UNIT:2 MyILA2 (ILA), UNIT:3 MyVIO3 (VIO), VIO Console, and UNIT:4 MyVIO4 (VIO), VIO Console. The "VIO Console" node under UNIT:3 is selected. The main window is titled "VIO Console - DEV:0 MyDevice0 (XC7VX690T) UNIT:3 MyVIO3 (VIO)". It contains a table with two columns: "Bus/Signal" and "Value". The table rows are:

Bus/Signal	Value
<code>vio_modify_enable</code>	1
<code>vio_data_mask_gen</code>	0
<code>vio_pause_traffic</code>	0
<code>dbg_clear_error</code>	0
<code>vio_addr_mode_value</code>	3
<code>vio.bl.mode_value</code>	2
<code>vio.fixed.bl.value</code>	16
<code>vio.fixed.instr.value</code>	1
<code>vio.instr.mode.value</code>	2
<code>vio.data.mode.value</code>	7

A "DONE" button is located at the bottom right of the table area.

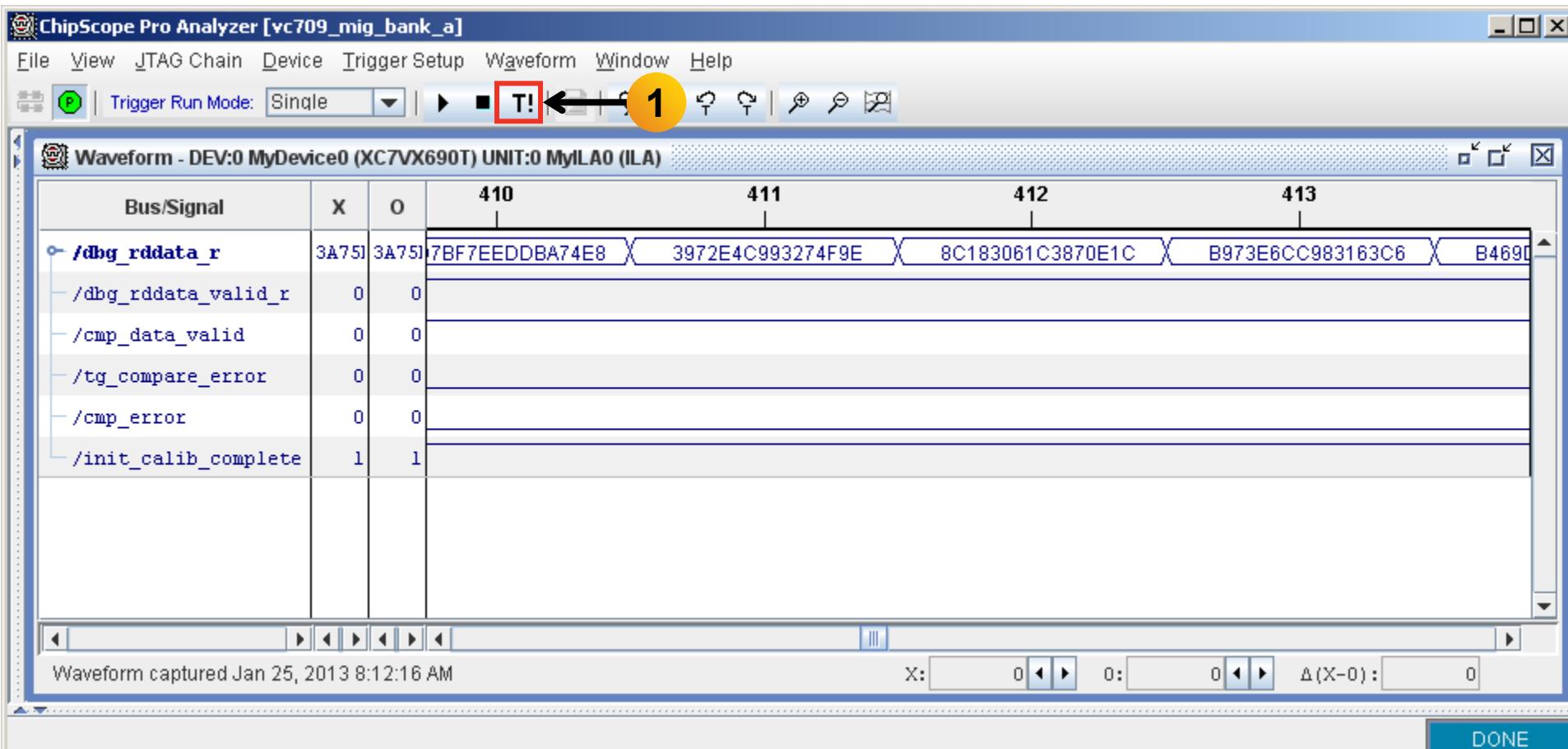
Run MIG Bank A and B Example Design



► Press and release the CPU RESET switch, SW8, after each change to vio_modify_enable or vio_data_mode_value

Run MIG Bank A and B Example Design

- Click on Waveform; click the Trigger Immediate button (1)
- View PRBS data



References

References

➤ Virtex-7 Memory

- 7 Series FPGAs Memory Interface Solutions User Guide – UG586
 - http://www.xilinx.com/support/documentation/ip_documentation/mig_7series/v1_8/ug586_7Series_MIS.pdf

➤ ChipScope Pro

- ChipScope Pro Software and Cores User Guide
 - http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_4/chipscope_pro_sw_cores_ug029.pdf

Documentation

Documentation

➤ Virtex-7

- Virtex-7 FPGA Family
 - <http://www.xilinx.com/products/silicon-devices/fpga/virtex-7/index.htm>

➤ VC709 Documentation

- Virtex-7 FPGA VC709 Evaluation Kit
 - <http://www.xilinx.com/products/boards-and-kits/EK-V7-VC709-CES-G.htm>
- VC709 User Guide
 - http://www.xilinx.com/member/vc709_headstart/ug887-vc709-eval-board-v7-fpga.pdf