30. a.i.	Describe the scalability metrics for achieving parallel scalability.	4	1	3	2
ii.	Discuss in detail the different variants of parallelization methods.	8	1	3	2
	(OR)				
b.i.	Examine the fat-tree network hierarchies for the given scenarios: In a fat-tree network with static routing, what are the consequences of a 4:3 over subscription on the links to the spine switches?	8	2	3	2
ii.	List out the basic performance characteristics of networks in a parallel computers.	4	2	3	2
31. a.i.	With a snippet of code, illustrate how work sharing for loops is implemented in open MP.	8	2	4	2
ii.	With an example, explain the REDUCTION clause.	4	2	4	3
	(OR)				
b.	Elaborate on various ways to convert (or) reduce parallelism to run serial code if parallelism does not pay off.	12	1	4	1
32. a.	Analyze how non-blocking point-to-point communication takes place in a distributed memory parallel programming with MPI.	12	2	5	2
	(OR)				
b.	Examine the operation of synchronization and implicit serialization in order to deliver an efficient MPI programming.	12	2	5	2

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Reg. No.															

B.Tech. DEGREE EXAMINATION, MAY 2023
Sixth & Seventh Semester

18CSE454T – HIGH PERFORMANCE COMPUTING
(For the candidates admitted from the academic year 2018-2019 to 2021-2022)

Note:
(i) **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.
(ii) **Part - B & Part - C** should be answered in answer booklet.

Time: 3 hours Max. Marks: 100

		Marks	BL	CO	PO
	PART – A (20 × 1 = 20 Marks) Answer **ALL** Questions				
1.	The most sensible time measure in benchmarking of processor is (A) Peak time (B) Elapsed time (C) CPU time (D) Load / stone time	1	1	1	1
2.	The power dissipation of CPU is proportional to (A) Clock frequency (B) Supply voltage (C) Third power of supply voltage (D) Third power of clock frequency	1	1	1	1
3.	To execute one instruction in per clock cycle, what is the maximum number of instructions for a pipeline with 5 stages to be issued? (A) 5 (B) 4 (C) 3 (D) 2	1	1	1	1
4.	Several threads on a physical core wait for some event to occur by executing tight loops is known as (A) Loop waiting (B) Spin waiting (C) Bottle neck (D) Stalls	1	1	1	1
5.	Gathering information about a programs behavior is called (A) Hot spots (B) Parallelism (C) Profiling (D) Scaling	1	1	2	1
6.	Shrinking the working set of a code is good because it (A) Raises the probability for cache hits (B) Raises the probability for cache miss (C) Decreases the running time of a code (D) Increases the running time of a code	1	1	2	1
7.	Function in-lining is used to (A) Reduce elapsed time (B) Reduce runtime (C) Increase elapsed time (D) Increase runtime	1	1	2	1
8.	_____ occurs if the CPU does not have enough registers to hold all the required operands inside a complex computation or loop body. (A) Inlining (B) Aliasing (C) Profiling (D) Register pressure	1	1	2	2

9. In a distributed memory system — 1 1 3 1
   (A) All processor share the same global memory
   (B) There is an interconnection network connecting the processors
   (C) Processes share the same heap
   (D) A processor can access data from another processor's memory using the load/store instruction

10. In ccNUMA machines, bus logic like chipsets or memory interfaces keep track of the location and state of each cache line is called — 1 1 3 1
   (A) False sharing
   (B) Front side bus
   (C) Directory-based protocol
   (D) Quick path

11. Parallel efficiency is defined as — 1 1 3 1
   (A) Speedup / N
   (B) N / speedup
   (C) Speedup / N–1
   (D) N–1/ speedup

12. Multiple processors working on different part of the data is known as — 1 1 3 2
   (A) Multitasking
   (B) Data parallelism
   (C) Domain decomposition
   (D) Functional decomposition

13. Which command is used to set the number of threads in open MP programming? — 1 1 4 1
   (A) OMP_NUM_THREAD
   (B) OMP_THREADS_NUM
   (C) OMP_NUM_THREADS
   (D) OMP_THREAD_NUM

14. Identify the MPI function that support the creation and handling of virtual topologies. — 1 1 4 1
   (A) MPI_CART_CREATE( )
   (B) MPI_COORS( )
   (C) MPI_CART( )
   (D) MPI_SHIFT( )

15. Which MPI function supports the non-blocking point to point communication? — 1 1 4 1
   (A) MPI_SEND( )
   (B) MPI_SSEND( )
   (C) MPI_BSEND( )
   (D) MPI_ISEND( )

16. Within a parallel region, declared variables are by default — 1 1 4 1
   (A) Private
   (B) Local
   (C) Loco
   (D) Shared

17. A _____ construct by itself creates a "single program multiple data" program i.e each thread execute the same code, — 1 1 5 1
   (A) Parallel
   (B) Section
   (C) Single
   (D) Master

18. _____ is a form of parallelization across multiple processor in parallel computing environments. — 1 1 5 1
   (A) Work-sharing constructs
   (B) Data parallelism
   (C) Functional parallelism
   (D) Handling loops

19. The format for MPI_FINALIZE is _____. — 1 1 5 1
   (A) int MPI_Finalize (void)
   (B) char MPI_Finalize (void)
   (C) int MPI_Finalize (int)
   (D) int MPI_Finalize (int, int)

20. Which function distributer distinct messages from a single source task to each task in the group? — 1 1 5 1
   (A) MPI_Scatter
   (B) MPI_Gather
   (C) MPI_Reduce
   (D) MPI_Allreduce

PART – B (5 × 4 = 20 Marks) — Marks BL CO PO
Answer **ANY FIVE** Questions

21. List out the design principles of vector processors for vectorizing the code for massive parallelism. — 4 2 1 1

22. Mention and describe any four events that can be monitored by hardware performance counters. — 4 2 2 1

23. State any two scalability laws for parallelism. — 4 1 3 2

24. Explain how cache coherence protocols are implemented in shared memory computers. — 4 1 3 1

25. How task directive is used as a work sharing construct in open MP? — 4 1 4 1

26. Analyze the various MPI constructs used for collective communication. — 4 2 5 1

27. List the communication parameters and protocols used in point-to-point message transfer in MPI. — 4 1 5 2

PART – C (5 × 12 = 60 Marks) — Marks BL CO PO
Answer **ALL** Questions

28. a. With a neat sketch illustrate how multi-threading enhances the instruction throughput by eliminating the pipeline bubbles. — 12 1 1 1

(OR)

b.i. What is pipelining? What are the pitfalls involved in executing instructions through pipelining? — 6 1 1 1

ii. Discuss in detail the pros and cons of cache mapping techniques. — 6 1 1 1

29. a. Examine the function and line-based runtime profiling while optimizing the serial code. — 12 2 2 2

(OR)

b. Using suitable examples, examine the procedures of dynamic memory management involved in C++ optimization. — 12 2 2 2