Reg. No.															

B.Tech. DEGREE EXAMINATION, MAY 2019
Fourth Semester

CS1008 – COMPUTER ORGANIZATION AND ARCHITECTURE
(For the candidates admitted during the academic year 2013 – 2014 and 2014 – 2015)

Note:
(i) **Part - A** should be answered in OMR sheet within first 45 minutes and OMR sheet should be handed over to hall invigilator at the end of 45th minute.
(ii) **Part - B** and **Part - C** should be answered in answer booklet.

Time: Three Hours Max. Marks: 100

PART – A (20 × 1 = 20 Marks)
Answer ALL Questions

1. A source program is usually in _____.
   (A) Assembly language (B) Machine level language
   (C) High-level language (D) Natural language

2. The small extremely fast, RAM's are called as
   (A) Cache (B) Heaps
   (C) Accumulators (D) Stacks

3. The decoder instruction is stored in .
   (A) IR (B) PC
   (C) Registers (D) MDR

4. In case of, zero address instruction method the operands are stored in _____.
   (A) Registers (B) Accumulators
   (C) Push down stack (D) Cache

5. The addressing mode, where you directly specify the operand value is _____.
   (A) Immediate (B) Direct
   (C) Definite (D) Relative

6. The sign followed by the string of digits is called as _____.
   (A) Significant (B) Determinant
   (C) Mantissa (D) Exponent

7. In IEEE 32-bit representations, the mantissa of the fraction is said to occupy _____ bits.
   (A) 24 (B) 23
   (C) 20 (D) 16

8. The 32 bit representation of the decimal number is called as _____.
   (A) Double-precision (B) Single-precision
   (C) Extended format (D) Significant

9. The product of 1101 and 1011 is
   (A) 10001111 (B) 10101010
   (C) 11110000 (D) 11001100

10. The method used to reduce the maximum numbers of summands by half is _____.
    (A) Fast multiplication (B) Bit-pair recoding
    (C) Quick multiplication (D) Floating point

11. The disadvantage of DRAM over SRAM is/ are _____.
    (A) Lower data storage capacities (B) Higher heat descipation
    (C) The cells are not static (D) Higher cost

12. The DMA controller has _____ registers.
    (A) 4 (B) 3
    (C) 2 (D) 1

13. A _____ is used to restore the contents of the cells.
    (A) Sense amplifier (B) Refresh counter
    (C) Restorer (D) Counter

14. To get the row address of the required data _____ is enables.
    (A) CAS (B) RAS
    (C) CS (D) Sense/ write

15. What does the RUN signal do?
    (A) It causes the termination of a signal (B) It causes a particular signal to perform its operation
    (C) It causes a particular signal to end (D) It increments the step counter by one

16. In micro-programmed approach, the signals are generated by _____.
    (A) Machine instructions (B) System programs
    (C) Utility tools (D) Assembly programs

17. The time taken to transfer a word of data to or from the memory is called as _____.
    (A) Access time (B) Cycle time
    (C) Memory latency (D) Threshold time

18. The effectiveness of the cache memory is based on the property of _____.
    (A) Locality of reference (B) Memory localization
    (C) Memory size (D) Latency size

19. The DMA transfer are performed by a control circuit called as _____.
    (A) Device interface (B) DMA controllers
    (C) Data controller (D) Over looker

20. The centralized bus arbitration is similar to _____ interrupt circuit
    (A) Priority (B) Parallel
    (C) Single (D) Daisy chain

PART – B (5 × 4 = 20 Marks)
Answer **ANY FIVE** Questions

21. Differentiate RISC and CISC.

22. Discuss about basic functional units and give their functions.

23. Multiply −13 and + 23 using bit pair recoding.

24. List down the steps involved in restoring and non-restoring division.

25. Explain the role of cache memory.

26. Draw the diagram of internal organization of memory chips.

27. Illustrate the use of DMA controller in a computer systems.

PART – C (5 × 12 = 60 Marks)
Answer **ALL** Questions

28. a. Illustrate the various addressing modes of instructions using suitable diagram.

(OR)

b. Explain in detail about software performance.

29. a. Explain carrysave addition of summands with example.

(OR)

b. Perform multiplication on −15 and −8 using Booth recoding and bit pair recoding.

30. a. Explain various types of hazards in pipelining using example.

(OR)

b. Describe hardwired control in detail with necessary diagram.

31. a. Write a detailed notes on cache memory.

(OR)

b. Briefly explain virtual memory and its management.

32. a. Illustrate bus arbitration in DMA.

(OR)

b. Describe the working principle of USB.

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