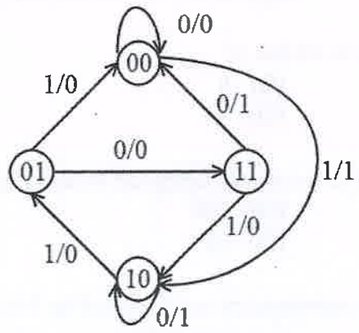
27. a.i.	Describe the RTL-NOR gate operation with a circuit diagram and truth table.	5	1	1	1
ii.	Describe the DTL-NAND gate operation with a circuit diagram and truth table.	5	1	1	1
	(OR)				
b.	Explain the operation of TTL NAND gate operation with a neat circuit diagram and truth table.	10	1	1	1
28. a.	Reduce using Quine McCluskey method $F(a,b,c,d) = \Sigma m(2,3,7,9,11,13) + \Sigma d(1,10,15)$	10	2	2	2
	(OR)				
b.	Design half adder using data flow modeling.	10	2	5	2
29. a.	A sequential circuit has one input and one output the state diagram is shown. Design the sequential circuit with D-FF.	10	3	3	2



	(OR)				
b.	Design an asynchronous sequential circuit that has two internal states and one output. The excitation and output function describing the circuit are as follows: $Y_1 = x_1x_2 + x_1y_2 + x_2y_1$ $Y_2 = x_2 + x_1y_1y_2 + x_1y_1$ $Z = x_2 + y_1$ (i) Draw the logic diagram of the circuit (ii) Derive the transition table output map and flow table	10	3	3	2
30. a.	Develop a 2-bit synchronous binary counter using T flip-flop.	10	2	3	2
	(OR)				
b.	Derive the expression for the output voltage for 100 binary input to R-2R ladder DAC along with neat circuit diagram. Also draw the transfer characteristics of 3 bit DAC.	10	2	3	2

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Reg. No.															

B.Tech. DEGREE EXAMINATION, MAY 2022
Third Semester

18CSS201J – ANALOG AND DIGITAL ELECTRONICS
(For the candidates admitted from the academic year 2018-2019 to 2019-2020)

Note:
(i) **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.
(ii) **Part - B** should be answered in answer booklet.

Time: 2½ Hours Max. Marks: 75

PART – A (25 × 1 = 25 Marks)
Answer **ALL** Questions

	Marks	BL	CO	PO
1. JFET is a _____ controlled device, which has _____. (A) Current, high input impedance (B) Voltage, low input impedance (C) Current, high noise level (D) Voltage, high input impedance	1	1	1	1
2. Transistor works as an amplifier when (A) Input junction is forward biased and the output junction is reverses biased (B) Input junction is reverse biased and output junction is forward biased (C) Both input and output junction are forward biased (D) Both input and output junction are reverse biased	1	1	1	1
3. Determine the gain of non-inverting op-amp with resistors R_1 = 1 K Ω and R_F = 99 KΩ. (A) 100 (B) $\frac{1}{100}$ (C) $\frac{-1}{100}$ (D) –100	1	2	1	2
4. For a current shunt feedback amplifier, the current gain of the forward amplifier A_I = 100, feedback Nework gain β = 0.19. Find current gain with feedback. (A) 2 (B) 3 (C) 4 (D) 5	1	2	1	2
5. Pin number 3 of 555 timer is _____. (A) Trigger (B) Threshold (C) Output (D) Reset	1	1	1	1
6. Operating temperature range for commercial application of digital IC is (A) 0 to 70°C (B) 10 to 70°C (C) 0 to 17°C (D) 50 to 70°C	1	1	1	1
7. The device with short propagation delay has (A) Medium speed (B) Low speed (C) High speed (D) Very low speed	1	1	1	1

8. The third state of tri-state buffer mainly known as? 1 1 1 1
(A) High impedance (B) Low impedance
(C) High resistance (D) Low resistance

9. Consider the following statements with respect to ECL gate 1 1 1 1
(A) Switching speed is high and it provide OR and NOR logic operation (B) Power dissipation is small as compared to other logic gates
(C) Its logic levels are compatible with other logic family gates (D) It provides AND logic operation

10. In HDL which of the following is the basic building block of a design? 1 1 5 1
(A) Architecture (B) Entity
(C) Process (D) Package

11. _____ is also called as data selector. 1 1 2 1
(A) MUX (B) DEMUX
(C) HDL (D) Encoder

12. In K map, for M variable, _____ cells are required. 1 1 2 1
(A) M (B) 2^M
(C) 2^{2M} (D) M*M

13. Full adder circuit adds _____ number of bits at a time. 1 1 2 1
(A) 3 (B) 2
(C) 4 (D) 5

14. If A = 1010 and B = 0101 then the comparator output is 1 1 2 1
(A) A > B (B) A = B
(C) A < B (D) A – B

15. The expression for C_3 in carry look ahead adder is 1 1 2 1
(A) $C_3 = G_0 + P_0C_{in}$
(B) $C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_{in}$
(C) $C_3 = G_1 + P_1C_{in}$
(D) $C_3 = G_1 + P_1G_0 + P_1P_0C_{in}$

16. In a SR flip-flop indeterminate state means 1 1 2 1
(A) Set Q = 1 and $\overline{Q}$ =0 (B) Set Q = 0 and $\overline{Q}$ = 1
(C) Input SR are = 0 (D) Input SR are = 1

17. The present output Q_n of an edge triggered JK flip-flop is logic 1. If K = 1, then Q_{n+1} will be 1 1 2 1
(A) 1 (B) 0
(C) Don't care (D) Can't be determined

18. The input and control signal to T flip flop are T =1, preset = 0, clear = 1. Assume Q = 1 then output of flip flop will be 1 1 2 1
(A) 0 (B) 1
(C) Don't care (D) Can't be determined

19. Any two states of a synchronous sequential circuit is said to be equivalent if 1 1 2 1
(A) For event input the output are the same (B) For every input the outputs and next states are the same
(C) For every input the next states are the same (D) For every input the outputs may be different but the next states are the same

20. The characteristic equation of J-K flip flop is 1 1 2 1
(A) $Q(n+1) = JQ(n) + \overline{K}Q(n)$ (B) $Q(n+1) = \overline{J}Q(n) + \overline{K}Q(n)$
(C) $Q(n+1) = J\overline{Q}(n) + K\overline{Q}(n)$ (D) $Q(n+1) = J\overline{Q}(n) + \overline{K}Q(n)$

21. A four-bit SISO right shift register is initialized to a value 0001. Input to the shift register is 1111. Identify the number of clock pulses required to obtain 1110 from the initial values. 1 2 3 2
(A) 2 (B) 3
(C) 4 (D) 5

22. A 3-bit counter has a maximum modulus of _____. 1 1 3 1
(A) 3 (B) 6
(C) 8 (D) 10

23. The final decimal number count in a counter designed with 8 flip flops is 1 1 3 1
(A) 255 (B) 256
(C) 31 (D) 32

24. How many numbers of op-amp comparators are required in 3-bit flash type ADC? 1 1 3 1
(A) 3 (B) 6
(C) 7 (D) 8

25. What is the smallest change in voltage which may be produced at the output due to the step change in the input of the DAC? 1 1 3 1
(A) Linearity (B) Accuracy
(C) Monotonicity (D) Resolution

PART – B (5 × 10 = 50 Marks) Marks BL CO PO
Answer **ALL** Questions

26. a.i. Give the pin details of IC 741 op-amp. 2 1 1 1

ii. What are the characteristics of an ideal op-amp? 4 1 1 1

iii. Analyse the gain of inverting op-amp. 4 1 1 1

(OR)

b. With a neat diagram for voltage series feedback amplifier, obtain the expression for 4 1 1 1
(i) Voltage gain with feedback 2 1 1 1
(ii) Input impedance with feedback 2 1 1 1
(iii) Output impedance with feedback 2 1 1 1