Reg. No.															

B.Tech. DEGREE EXAMINATION, NOVEMBER 2023

Sixth Semester

18CSE454T – HIGH PERFORMANCE COMPUTING

(For the candidates admitted from the academic year 2020-2021 & 2021-2022)

Note:

(i) **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

(ii) **Part - B & Part - C** should be answered in answer booklet.

Time: 3 hours Max. Marks: 100

PART – A (20 × 1 = 20 Marks)

Answer **ALL** Questions

	Marks	BL	CO	PO
1. The process of not having to wait until all the arguments of an operation are available is known as (A) Masking (B) Chaining (C) Vectorizing (D) Pipelining	1	1	1	1
2. Pipeline bubbles are (A) Stall cycles (B) Multi-track pipeline (C) Cache mapping (D) Data dependencies	1	1	1	1
3. Interleaving loop iterations in order to meet latency requirements is (A) Super scalarity (B) Software pipelining (C) Wind-up phase (D) Wind-down phase	1	1	1	1
4. _____ is a Boolean register with vector length, allows selective execution of loop iterations. (A) Mask memory (B) Cache memory (C) Mask register (D) Cache register	1	1	1	1
5. Code instrumentation technique of profiling is limited to (A) Basic blocks (B) Functions (C) Lines (D) Subroutines	1	1	2	1
6. The _____ of a code is the amount of memory it uses in the course of a calculation. (A) Basic block (B) Functions (C) Working set (D) Code instrumentation	1	1	2	1
7. _____ is an optimization technique that replaces a function call by the body of the caller (A) Sampling (B) Line profiling (C) Function profiling (D) Function in lining	1	1	2	1
8. Caches can only have a positive effect on performance if the data access pattern of an application (A) Cache reuse ratio (B) Streaming patterns (C) Cache lines (D) Locality of reference	1	1	2	1

9. Which one of these statements are true? 1 1 3 1

(A) Von Neumann architecture is not suitable for realizing SIMD
(B) Vector processors can handle data level parallelism
(C) Vector processors contain only vector register
(D) Cache memory and constant memory are unified for all streaming multiprocessor

10. Which of the following is not true about superscalar execution? 1 1 3 1

(A) Multiple instructions may be issued together
(B) The same stage of multiple instructions may execute together
(C) Hardware logic for various stages is replicated to a large extent
(D) Data dependency issues are resolved to a large extent

11. Which of the following is not a reason for non-vanishing serial part? 1 1 3 1

(A) Bottlenecks
(B) Communication
(C) Startup overhead
(D) Application speedup

12. In switched network, the maximum number of hops required to connect two arbitrary devices is called 1 1 3 1

(A) Bandwidth
(B) Bisection bandwidth
(C) Diameter
(D) Crossbar

13. MPI_CART_CREATE( ) function support the creation and handling of _____. 1 1 4 1

(A) Virtual topologies
(B) Bus topologies
(C) Star topologies
(D) Mesh topologies

14. MPI_FINALIZE( ) is used to _____ the parallel program in MPI. 1 1 4 1

(A) Finalize
(B) End
(C) Exit
(D) Shutdown

15. Which programming model dedicates a separate thread to handle MPI calls while other thread execute user code? 1 1 4 1

(A) OpenMP programming
(B) MPI programming
(C) Hybrid programming
(D) Integrated programming

16. The _____ specifies that the iterations of the for loop should be executed in parallel by multiple threads? 1 1 4 1

(A) Section construct
(B) Single construct
(C) For pragma
(D) Parallel construct

17. _____ function returns the number of threads that are currently active in the parallel section region. 1 1 5 1

(A) omp_get_num_procs( )
(B) omp_get_num_threads( )
(C) omp_get_thread_num( )
(D) omp_set_num_threads( )

18. _____ causes no synchronization overhead and can maintain data locality when data fits in cache. 1 1 5 1

(A) Guided
(B) Auto
(C) Runtime
(D) Static

19.	Which of the following command determines the rank of calling process in the communicate? (A) MPI_COMM_WORLD (B) MPI_COMM_SIZE (C) MPI_COMM_RANK (D) MPI_COMM_GROUP	1	1	5	1
20.	Programs that can maintain a constant efficiency without increasing the problem size are sometimes said to be (A) Scalable (B) Strongly scalable (C) Weakly scalable (D) Not scalable	1	1	5	1

PART – B (5 × 4 = 20 Marks)
Answer **ANY FIVE** Questions

		Marks	BL	CO	PO
21.	List any four performance metrics of processors and explain it with the vector trial benchmark.	4	1	1	1
22.	Mention and explain any two common sense guidelines for performance optimization in a serial code.	4	1	2	2
23.	How cache coherence is applied in ccNUMA shared memory systems?	4	1	3	1
24.	Describe the scalability metrics for achieving parallel scalability.	4	1	2	1
25.	Illustrate how schedule clause is used for loop work sharing.	4	2	4	2
26.	List out the chain of events for the standard MPI Ping-Pong on shared memory systems.	4	1	5	1
27.	Describe any four events that can be monitored by hardware performance counters.	4	1	1	2

PART – C (5 × 12 = 60 Marks)
Answer **ALL** Questions

		Marks	BL	CO	PO
28. a.i.	Elaborate the design principles of vector processors.	6	1	1	1
ii.	Illustrate how the branching instructions are vectored on a vector processors.	6	2	1	1
	(OR)				
b.i.	Bring out the advantages and disadvantages of multi-core processors.	4	1	1	2
ii.	How pre-fetching of instructions avoids the latency penalties for a vector norm loop? Illustrate with a timing diagram.	8	1	1	1
29. a.	Apply the various steps available to improve the performance of the code by optimizing the loops using suitable examples.	12	2	2	2
	(OR)				

	b. Investigate the role of compilers in optimization of code.	12	2	2	1
30. a.i.	Illustrate how, the basic communication models are used for possible refinements performance models.	8	2	3	2
	ii. State any two scalability laws for parallelism.	4	1	3	3
	(OR)				
	b.i. With a neat sketch, explain how cache coherence protocols are implemented in shared memory computers.	6	1	3	1
	ii. Illustrate a UMA system with two single-core processors and two dual-core processors.	6	2	3	2
31. a.i.	With a snippet of code illustrate how, the synchronization is achieved with the help of critical region directive in open MP.	8	2	4	1
	ii. Explain the different ways to create PRIVATE variables in open MP with a code snippet.	4	1	4	2
	(OR)				
	b. Privatization should be given priority over synchronization. Justify this statement with respect to open MP serialization.	12	2	4	1
32. a.	Analyze various constructs in MPI that are used in point-to-point communication with a suitable program fragment.	12	2	5	1
	(OR)				
	b. Identify and describe the mapping issues and aggregating messages to be followed in order to reduce the communication overhead by using MPI.	12	2	5	1

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