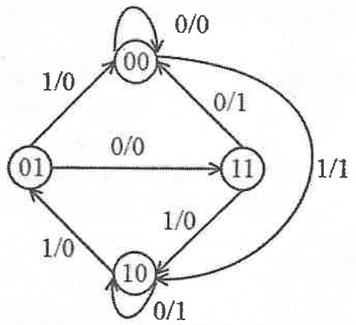
b. Design a sequential logic circuit for the given state diagram, using RS-flip flop.



32. a. Design a mod-12 synchronous counter using T-flip flop.

(OR)

b. Describe the following DAC with a neat diagrams.
   (i) Weighted resistor type
   (ii) R-2R ladder type

* * * * *

Reg. No.														

B.Tech. DEGREE EXAMINATION, NOVEMBER 2019
Third Semester

18CSS201J – ANALOG AND DIGITAL ELECTRONICS
(For the candidates admitted during the academic year 2018-2019 onwards)

Note:
(i) **Part - A** should be answered in OMR sheet within first 45 minutes and OMR sheet should be handed over to hall invigilator at the end of 45th minute.
(ii) **Part - B** and **Part - C** should be answered in answer booklet.

Time: Three Hours Max. Marks: 100

PART – A (20 × 1 = 20 Marks)
Answer **ALL** Questions

1. Which type of power amplifier is based for operation at less than 180° of the cycle?
   (A) Class A (B) Class B or AB
   (C) Class C (D) Class D

2. Which of the following is not an example for non-sinusoidal oscillator?
   (A) Saw tooth generators (B) Blocking oscillators
   (C) Multivibrator (D) Crystal oscillators

3. Which operating condition is satisfied by the transistor if it is supposed to function in cut-off region?
   (A) $V_{CE} > 0$ (B) $V_{CE} = 0$
   (C) $V_{CE} < 0$ (D) $V_{CE} = V_{CC}$

4. The inverting operational amplifier has gain of −1000 and feedback resistance (R_f) = 1 mΩ, find the value of input resistance (R_i) =
   (A) 1 kΩ (B) 100 Ω
   (C) 100 kΩ (D) 10 kΩ

5. If the digital IC family has a fan out of 6, it implies that the gate can supply the current to _____ of same family.
   (A) 6 inputs (B) 6 outputs
   (C) 12 nodes (D) 12 branches

6. Which type of unipolar logic family exhibits its usability for the applications requiring low power consumption?
   (A) PMOS (B) NMOS
   (C) CMOS (D) ECL

7. _____ is the bipolar logic families which is specifically adopted for high speed applications.
   (A) DTL (B) TTL
   (C) ECL (D) I^2L

8. FPGA stands for _____.
   (A) Field-programmable gate array (B) Field-propagation gate array
   (C) Function-propagation gate array (D) Function-programmable gate array

9. A multiplexer with three selection line inputs represents:
   (A) 4:1 mux (B) 8:1 mux
   (C) 16:1 mux (D) 32:1 mux

10. How many 3 line-to-8 line decoders are required for a 1-of-32 decoder?
   (A) 1 (B) 2
   (C) 4 (D) 8

11. _____ gate is best suitable for basic comparator.
   (A) NOR (B) OR
   (C) Exclusive-OR (D) AND

12. Which of the following expressions in in the product of sums forms?
   (A) (A+B) (C+D) (B) (AB) (CD)
   (C) AB (CD) (D) AB + CD

13. Best examples for the use of an S-R flip flop is _____.
   (A) Transition pulse generator (B) Racer
   (C) Switch debouncer (D) Astable oscillator

14. The truth table for an S-R flip flop has how many valid entries.
   (A) 1 (B) 2
   (C) 3 (D) 4

15. When both inputs of a J-K flip-flop cycle is high, the output will _____.
   (A) be invalid (B) Change
   (C) Not change (D) Toggle

16. The logic circuits whose outputs at any instant of time depend only on the present input but also on the past outputs are called _____.
   (A) Combinational circuits (B) Sequential circuits
   (C) Mux (D) Full adder

17. The register is a type of _____.
   (A) Sequential circuit (B) Combinational circuit
   (C) CPU (D) Latches

18. Registers are classified into _____ types.
   (A) 2 (B) 3
   (C) 4 (D) 5

19. The "D" register stands for _____.
   (A) Delay (B) Decrement
   (C) Data (D) Decay

20. The main difference between a register and a counter is _____.
   (A) Register has no specific sequence of states (B) Counter has no specific sequence of states
   (C) A registers counts data (D) Register can store one bit data but counter has N-bit

PART – B (5 × 4 = 20 Marks)
Answer **ANY FIVE** Questions

21. List out the uses of BJT.

22. Write short notes on the effects of negative feedback amplifier.

23. Design the logic present in transistor as switch with related logic table.

24. Compare PMOS and NMOS.

25. Write short notes on magnitude comparator.

26. Design a D-flip flop with truth table, circuit diagram and characteristics equation.

27. List out the applications of shift registers.

PART – C (5 × 12 = 60 Marks)
Answer **ALL** Questions

28. a. With a neat circuit, describe the operation of voltage shunt feedback amplifier and derive the expression for input impedance, output impedance and transresistance.

(OR)

b. Explain the following, with a neat diagram
   (i) UJT-relaxation oscillator
   (ii) 555 timer

29. a. Describe the operation of TTL logic family with related circuit diagram.

(OR)

b. Analyze and explain the concept of different types of CMOS logic circuit with a neat sketch.

30. a. Find the minimal SOP for the Boolean expression,
$F(A,B,C,D) = \Sigma m(1,2,3,7,8,9,10,11,14,15)$ using Quine McCluskey method.

(OR)

b. Explain the operation of the following
   (i) 8:1 multiplexer with neat logic diagram
   (ii) 1:8 demultiplexer with neat logic diagram

31. a. Design the operation of master-slave JK-flip flop with positive and negative clock pulses with neat diagram.

(OR)