Reg. No.															

B.Tech. DEGREE EXAMINATION, NOVEMBER 2019
Third Semester

18CSC203J – COMPUTER ORGANIZATION AND ARCHITECTURE
(For the candidates admitted during the academic year 2018-2019 onwards)

Note:
(i) **Part - A** should be answered in OMR sheet within first 45 minutes and OMR sheet should be handed over to hall invigilator at the end of 45th minute.
(ii) **Part - B** and **Part - C** should be answered in answer booklet.

Time: Three Hours Max. Marks: 100

PART – A (20 × 1 = 20 Marks)
Answer **ALL** Questions

1. The instruction → Add LOCA, Ro _____.
   (A) Adds the value of LOCA to Ro and stores in the temp register
   (B) Adds the value of Ro to the address of LOCA
   (C) Adds the value of both LOCA and Ro and stores it in Ro
   (D) Adds the value of LOCA with a value in accumulator and stores it in Ro

2. _____ is used to choose between incrementing the PC (or) performing ALU operations.
   (A) Conditional codes
   (B) Multiplexer
   (C) Control unit
   (D) Demultiplexer

3. Which memory device is generally made of semiconductors?
   (A) RAM
   (B) Hard disk
   (C) Floppy disk
   (D) CD

4. The instruction MOV AX, # 0005H belongs to the addressing mode
   (A) Register
   (B) Direct
   (C) Immediate
   (D) Register relative

5. Perform binary addition of 110H 0010 is _____.
   (A) 1110
   (B) 1111
   (C) 0111
   (D) 11101

6. Booth's algorithm is applied on _____.
   (A) Decimal numbers
   (B) Binary numbers
   (C) Hexadecimal numbers
   (D) Octal numbers

7. _____ is a straight forward method of representing positive and negative number.
   (A) Radix
   (B) Complement
   (C) Sign magnitude
   (D) Encode

8. The sign magnitude representation of −9 is _____.
   (A) 00001001
   (B) 11111001
   (C) 10001001
   (D) 11001

9. The pipelining process is also called as
   (A) Superscalar operation (B) Assembly line operation
   (C) Von Neumann cycle (D) Harvard cycle

10. The situation where in the data of operands are not available is called _____.
   (A) Data hazard (B) Stock
   (C) Dead lock (D) Structural hazard

11. A word whose individual bits represent a control signal is _____.
   (A) Command word (B) Control word
   (C) Co-ordination word (D) Generation word

12. Each stage in pipelining should be completed within _____ cycle.
   (A) 1 (B) 2
   (C) 3 (D) 4

13. When instruction 'i' and instruction 'j' tends to write in same register (or) memory location, it is called
   (A) Input dependence (B) Output dependence
   (C) Ideal pipeline (D) Digital call

14. SIMD represents an organization that _____.
   (A) Refers to a computer system capable of processing several programs at same time (B) Represents organization of single computer containing a control unit, processor unit
   (C) Includes many processing units under the supervision of a common control unit (D) Refers to a system capable of processing single program at a same time

15. Von Neumann architecture is _____.
   (A) SISD (B) SIMD
   (C) MIMD (D) MISD

16. Multithreading allows multiple-threads for sharing functional units of a
   (A) Multiple processor (B) Single processor
   (C) Dual core (D) Core i5

17. The correspondence between the main memory blocks and those in that cache is given by
   (A) Hash function (B) Mapping function
   (C) Locale function (D) Assign function

18. The temporal aspect of the locality of reference means _____.
   (A) That the recently executed instruction won't be executed soon (B) That the recently executed instruction is temporarily not referred
   (C) That the recently executed instruction will be executed soon again (D) That recently executed instruction will never be executed again

19. _____ is used to implement virtual memory organization
   (A) Page table (B) Frame table
   (C) MMU (D) Page table register

20. _____ translates the logical address into a physical address.
   (A) MMU (B) Translator
   (C) Computer (D) Linker

PART – B (5 × 4 = 20 Marks)
Answer **ANY FIVE** Questions

21. Draw and explain the connections between the processor and memory.

22. Define byte addressability and what are the two ways the byte address can be assigned across words?

23. Write down the steps for non-restoring division.

24. What is a pipeline hazard? Mention its types and define each type of hazards.

25. Write down the control sequence for MOVE (R_1), R_2.

26. Specify the types of parallelism in software and hardware.

27. List and explain any four types of ROM.

PART – C (5 × 12 = 60 Marks)
Answer **ALL** Questions

28. a. List and explain various addressing modes, with its formats and example.

(OR)

b. Represent the arithmetic statement $F = (A - B) / (C + D * E)$ in various instruction formats.

29. a. Write booth's algorithm, perform Booth multiplication of -23×-19.

(OR)

b. Write restoring division algorithm. Perform restoring division of 10/3.

30. a. List and explain the steps involved in the execution of complete instruction.

(OR)

b. Describe the generation of control signals using hardwires control unit, with necessary diagrams.

31. a. Explain Flynn's classification and the four architectures in detail.

(OR)

b.i. Elaborate on software parallelism and its types.

ii. Brief about the hardware multithreading.

32. a. Discuss on various mapping schemes used in cache design.

(OR)

b. Explain how virtual memory address translation method works based on the concept of fixed length pages? Discuss with a diagram.

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