28. a.i.	Write the sequence of operation to fetch word from Memory.	5	2	4	1.6.1
ii.	Categorize the different ways to design the control unit.	5	2	3	1.6.1
	(OR)				
b.	What is meant by pipeline hazard? Discuss in detail about the types of hazards?	10	3	3	1.6.1
29. a.	Classify the different types of Computer Architecture proposed by Flynn's.	10	3	4	1.61.
	(OR)				
b.	Discuss in detail the cache coherence problem and the protocol that is used to overcome cache coherence.	10	3	4	1.6.1
30. a.	Discuss the possible methods for specifying where memory blocks are placed in the cache.	10	4	5	1.6.1
	(OR)				
b.i.	Differentiate Memory mapped I/O and I/O mapped I/O.	5	2	5	1.6.1
ii.	Write a short note on DMA data transfer.	5	2	5	1,6,1

* * * * *

Reg. No.															

B.Tech. DEGREE EXAMINATION, MAY 2022

Third & Fifth Semester

18CSC203J – COMPUTER ORGANIZATION AND ACHITECTURE

(For the candidates admitted from the academic year 2018-2019 to 2019-2020)

Note:

(i) **Part - A** should be answered in OMR sheet within first 40 minutes and OMR sheet should be handed over to hall invigilator at the end of 40th minute.

(ii) **Part - B** should be answered in answer booklet.

Time: 2½ Hours Max. Marks: 75

		Marks	BL	CO	PO
	PART – A (25 × 1 = 25 Marks) Answer **ALL** Questions				
1.	Which memory unit is used for reducing the access time from memory? (A) DRAM (B) SRAM (C) Cache Memory (D) Secondary Memory	1	1	1	1.6.1
2.	In Big Indian format, of 64 bit data, what is the starting byte address of the aligned words? (A) 0, 8, 16 (B) 0, 2, 4 (C) 0, 4, 8 (D) 2, 4, 6	1	2	1	1.6.1
3.	In which type of addressing there is no memory related operation? (A) Register Indirect Addressing (B) Register Addressing (C) Direct Addressing (D) Indirect Addressing	1	1	1	1.6.1
4.	Which of the following registers are used for performing count operation in 8086? (A) BX (B) AX (C) CX (D) DX	1	1	1	1.6.1
5.	A DB 30 DUP ('Hi'), how many bytes of memory are defined and reserved by this instruction? (A) 60 (B) 30 (C) 40 (D) 32	1	2	1	1.6.1
6.	-7 is represented in computer system as (A) 1 0 1 0 (B) 1 1 1 1 (C) 1 1 0 1 (D) 1 0 0 1	1	2	2	1.6.1
7.	How many full address are used in 4 – bit binary adder circuits? (A) 6 (B) 4 (C) 8 (D) 2	1	1	2	1.6.1
8.	What is the recoded value of 10111101100 using Booth recoding? (A) −1 +1 0 0 0 −1 +1 0 −1 0 (B) +1 −1 0 0 0 +1 −1 0 −1 0 (C) −1 +1 0 0 0 −1 0 0 −1 0 (D) 0 0 0 −1 +1 0 0 +1 −1 −1	1	2	2	1.6.1

9. Carry look ahead adder will _____. 1 1 2 1.6.1

(A) Calculate one or more carry bits before the sum, which reduces the wait time
(B) Calculate one or more carry bits after the sum, which reduces the wait time
(C) Calculate one or more carry bits before the sum, which increases the wait time
(D) Calculate one or more carry bits after the sum, which increases the wait time

10. The size of mantissa fraction in double precision floating point number is _____ 1 1 2 1.6.1

(A) 51 bit
(B) 52 bit
(C) 48 bit
(D) 32 bit

11. During the execution of a program which gets initialized first? 1 1 3 1.6.1

(A) MDR – Memory Data Register
(B) IR – Instruction Register
(C) PC – Program Counter
(D) MAR – Memory Address Register

12. In micro programmed approach, the signals are generated by 1 1 3 1.6.1

(A) Machine Instruction
(B) System Programs
(C) Utility Tools
(D) System Files

13. Each phase of the pipeline must be completed within the cycle of _____ 1 2 3 1.6.1

(A) 1
(B) 2
(C) 3
(D) 4

14. What approach is used to identify the data dependencies when dealing with software? 1 1 3 1.6.1

(A) Operand Forwarding
(B) Bubbling
(C) NoP
(D) Wait Signal

15. _____ is used to keep track of the control steps 1 1 3 1.6.1

(A) Control step counter
(B) Program Counter
(C) Index Counter
(D) Binary Counter

16. The sun micro systems processors usually follow _____ architecture 1 1 4 1.6.1

(A) CISC
(B) ISA
(C) ULTRA SPARC
(D) RISC

17. _____ is the another name given to Multi-threading 1 1 4 1.6.1

(A) Simultaneity
(B) Gross current
(C) Concurrency
(D) Recurrent

18. Which class of systems belongs to Von Neumann Computer 1 2 4 1.6.1

(A) Single Instruction Multiple Data
(B) Multiple Instruction Multiple Data
(C) Multiple Instruction Single Data
(D) Single Instruction single data

19. Scheduler shift threads in 1 2 4 1.6.1

(A) Multi-level queue scheduling
(B) Priority Scheduling
(C) Round Robin Fashion
(D) Multi-Level feedback queue scheduling

20. A write is only performed liberally in MESI protocol, if the each line is in 1 2 4 1.6.1

(A) Modified state only
(B) Shared state on Invalid State
(C) Shared State only
(D) Either Modified or Exclusive State

21. Which block replacement algorithm is not generally used in cache operation? 1 1 5 1.6.1

(A) LIFO
(B) FIFO
(C) LRU
(D) Random

22. If the main memory is 4 GB, cache memory size is 16MB, block size is 1KB, then what is the tag size for an 8 way associate cache? 1 2 5 1.6.1

(A) 8
(B) 9
(C) 10
(D) 11

23. _____ bit is used to signify the updation of cache Location 1 1 5 1.6.1

(A) Flag bit
(B) Reference bit
(C) Update bit
(D) Duty bit

24. The techniques which move the program blocks to or from the physical memory is called as _____ 1 1 5 1.6.1

(A) Paging
(B) Virtual Memory
(C) Overlays
(D) Framing

25. The method which offers higher speeds of I/O transfers is _____ 1 1 5 1.6.1

(A) Interrupts
(B) Memory Mappy
(C) Program – Controlled I/O
(D) DMA

PART – B (5 × 10 = 50 Marks) Marks BL CO PO

Answer **ALL** Questions

26. a. Illustrate with examples the different types of addressing modes 10 4 1 1.6.1

(OR)

b.i. Write an ALP to perform 8 bit addition of two numbers. 6 3 1 1.6.1

ii. With a neat sketch explain the steps in processing an instruction. 4 3 1 1.6.1

27. a.i. Convert 3251.1732 to single precision format. 4 3 2 1.6.1

ii. Apply Booth's Algorithm to multiply the signed numbers +13 and -6. 6 3 2 1.6.1

(OR)

b. Use restoring division and perform division of 8 by 3. 10 3 2 1.6.1