BIST Architecture Using Different Pattern Generators

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**Abstract.** In the proposed paper, a comparison of BIST with different PRPGs (Pseudo Random Pattern Generators) is implemented. This architecture contains a PRPG, arithmetic logic unit (ALU), read-only memory (ROM), and a comparator. Some PRPGs are examined, including Linear Feedback Shift Registers (LFSR), Complete Feedback Shift Registers (CFSR), Bit Swapped-LFSR (BS-LFSR), and Bit Swapped-CFSR (BS-CFSR). Each type of PRPG is used to enhance test pattern generation based on its ability to improve power efficiency, fault coverage, and overall performance. LFSR is popular for its ability to generate pseudo-random sequences efficiently, but it may not cover all possible patterns, especially for certain resistant fault sites. CFSR extends LFSR's capabilities by generating all possible sequences, including zero patterns, thus improving fault detection. Bit Swapping LFSR and CFSR further reduce transitions, which leads to lower power dissipation while maintaining fault coverage. These BIST implementations are evaluated in detail concerning power, area, gate count, and timing analyses. In this paper, the effectiveness of methods to reduce transitions, reduce power, and improve fault coverage is demonstrated. The extensive simulations and comparison schematics for an 8-bit variant designed across a 90 nm technology node are performed. The findings emphasize the benefits of advanced LFSR and CFSR architectures and demonstrate how they may provide more affordable, efficient, and dependable testing solutions for contemporary integrated circuits.

**Keywords:** Built-in self-test (BIST), Linear feedback shift resistor (LFSR), Complete feedback shift resistor (CFSR), Bit Swapped-LFSR (BS-LFSR), and Bit Swapped-CFSR (BS-CFSR), Arithmetic Logic Unit (ALU).

1. Introduction

BIST stands for Built-in self-test; it has brought a vast change in the testing of integrated circuits since it allows circuits to test themselves rather than requiring testing equipment. This innovation is instrumental to improving the functionality and dependability of integrated circuits. A key building block in BIST is the Pseudo-Random Pattern Generators (PRPGs), which are highly effective for generating the test patterns. This paper focuses on several types of PRPGs, such as Linear Feedback Shift Registers (LFSR), Complete Feedback Shift Registers (CFSR) [4], Bit Swapped-LFSR (BS-LFSR) [5], and Bit Swapped-CFSR (BS-CFSR). Every PRPG type has benefits for transition reduction, specific power values, and fault coverage [14]. Analyzing these generators, the study aims to find the most effective bis implementations from the point of view of area, power, gate count, and timing in different technology nodes. Therefore, this analysis is imperative in designing efficient and effective testing solutions for today’s sophisticated integrated circuits.

1. Literature survey

The table provides an overview of various research studies focused on improving the efficiency and performance of Linear Feedback Shift Registers (LFSRs) and Built-in Self-Test (BIST) technologies, especially in terms of power consumption. Several papers, including [1], [2], [3], [5], and [8], emphasize low-power LFSR designs, particularly the bit-swapping LFSR (BS-LFSR), which is shown to reduce dynamic power dissipation compared to conventional LFSRs. The integration of BIST with these LFSR variations is a common theme, as seen in [1], [4], [5], [9], and [10], where the studies explore different Automatic Test Pattern Generator (ATPG) techniques to enhance self-testing in digital circuits. Some papers, like [7] and [9], delve into FPGA implementations, while [11] introduces BIST for analog circuits using ON/OFF keying and delay monitoring. Additionally, [4] and [10] focus on comparing ATPG techniques and introducing reversible logic, respectively, to further optimize power usage during test phases. Overall, the studies illustrate diverse approaches to achieving power-efficient and scalable BIST architectures across both digital and analog domains.

## Table 1. Summary of Literature Survey

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|  |  |  |  |
| --- | --- | --- | --- |
| Reference | Paper Title | Paper Study | Year |
| [1] | Bit swapping linear feedback shift register for low power application using 130nm complementary metal oxide semiconductor technology. | The study conducted a comparative analysis of different Automatic Test Pattern Generator (ATPG) techniques—specifically LFSR, BS-CFSR, and CA—integrated with Built-in Self-Test (BIST) for ISCAS benchmark circuits (74XX series). | 2017 |
| [2] | Design of 8 and 16 bit lfsr with maximum length feedback polynomial using verilog | In the analysis of the results, it was observed that the proposed BS LFSR method offered lower dynamic power dissipation than the conventional LFSR design. | 2014 |
| [3] | Designing and implementing a power efficient BIST in BCD multiplier. | It aimed to reduce power dissipation in LFSRs while maintaining performance by implementing BS-LFSR. BS-LFSR demonstrated significant reductions in dynamic power dissipation compared to traditional LFSRs. | 2023 |
| [4] | Comparison of various ATPG techniques to determine optimal BIST | Comparison of BIST with traditional and BSCFSR pattern generator. | 2018 |
| [11] | Structural Built In Self Test of Analog Circuits using ON/OFF Keying and Delay Monitors | In this paper, propose a robust and low-cost structural BIST method for analog circuits, relying on perturbing the circuit at an injection point and observing the result as a digitally measurable time delay | 2024 |
| [10] | Designing Power-Efficient BIST Architecture: Leveraging Reversible Logic for Scalable Digital Systems | The study introduces an innovative BIST controller architecture using reversible logic to optimize power usage during test phases, crucial for energy-sensitive applications | 2024 |
| [9] | Low power BIST based multiplier design and simulation using FPGA | It presents a BIST-based multiplier implementation, emphasizing the importance of high speed, low power, and self-testing in digital signal processing applications. | 2016 |
| [8] | Bit-swapping LFSR for low-power BIST | A modified linear feedback shift register (LFSR) using a bit-swapping technique reduces transitions at circuit-under-test inputs by 25%. Experimental results on ISCAS'85 and '89 benchmark circuits show up to 45% power reduction during tests | 2008 |
| [7] | FPGA Implementation of of 8,16 And 32 Bit LFSR with Maximum | This paper examines 8, 16, and 32-bit LFSRs on FPGA using VHDL, analysing gate count, memory, and speed. A comparative study and simulation challenges for longer-bit LFSRs on FPGA are also discussed | 2014 |
| [5] | Design and Implementation of 8-bit LFSR, Bit-Swapping LFSR and Weighted Random Test Pattern Generator: A Performance Improvement | This paper discusses a conventional LFSR, BS-LFSR, and multiple WRTPG. | 2019 |

1. Design Methodology

This design methodology explores advanced techniques to enhance traditional shift registers by incorporating bit-swapping mechanisms. We delve into implementing Bit Swapping Linear Feedback Shift Registers (BS-LFSR) and Bit Swapping Complete Feedback Shift Registers (BS-CFSR). These designs utilize multiplexers controlled by higher-order bits to optimize performance and reduce transitions while ensuring nearly all possible output sequences for testing purposes. By maintaining specific bits unchanged, these configurations enhance overall functionality and reliability [12].

3.1 Test Pattern Generator:

The Test Pattern Generator generates the test patterns that will be applied to the Circuit Under Test (CUT). We formulated the results through 4 different types of Test Pattern Generators, and they are Linear Feedback Shift Register (LFSR), Complete Feedback Shift Register (CFSR), Bit Swapped- LFSR(BS-LFSR), Bit Swapped CFSR(BS-CFSR). The feedback polynomial determines the sequences' length [13].

• **Linear Feedback Shift Register (LFSR):**

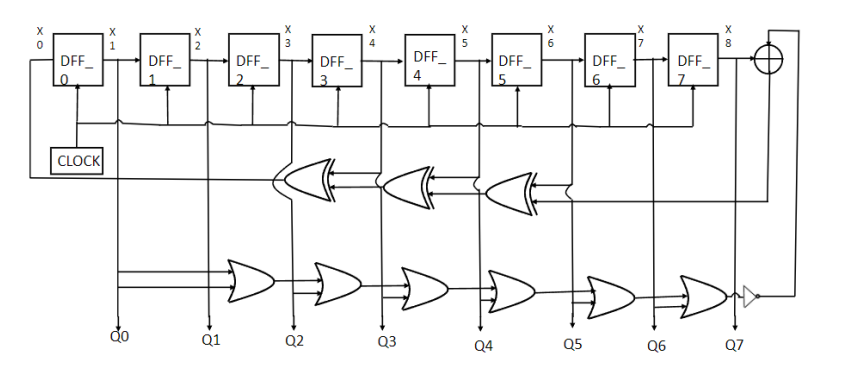
The LFSR is initialized with a starting state (seed value), typically nonzero. During each clock cycle, the contents of the register shift one position to the right (or left, depending on the implementation). The feedback polynomial determines whether a flip-flop is toggled (XORed) based on the current state of the register.

A LFSR generates sequences where n is the number of bits

An 8-bit LFSR generates maximum sequences i.e. 28 − 1 = 255 random states with the polynomial X8 + X6 + X5 + X4 + 1.

• **Complete Feedback Shift Register (CFSR):**

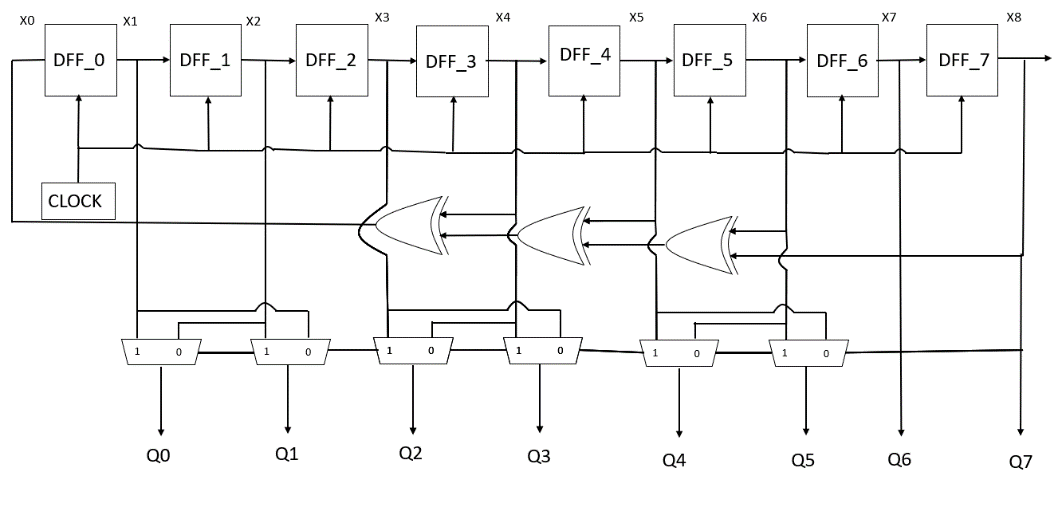
LFSR can generate most of the possible output. There are still some patterns that this kind of LFSR cannot generate. test vectors but not an all-zero-activity pattern for an otherwise inactive neuron. Some resistant fault sites (RP Resistant) need all zero vectors to sensitize, whereas the classical model cannot be used. An n-bit LFSR can be converted into an n-bit CFSR by adding an n-1 input NOR connected to all except the last bit. CFSR has better fault coverage than LFSR, as it can generate sequences and sequence ‘0’ can be fed as seed, and for 8bit, all 256 sequences are generated as shown in Figure 3.2.



**Fig 3.2** 8-bit CFSR

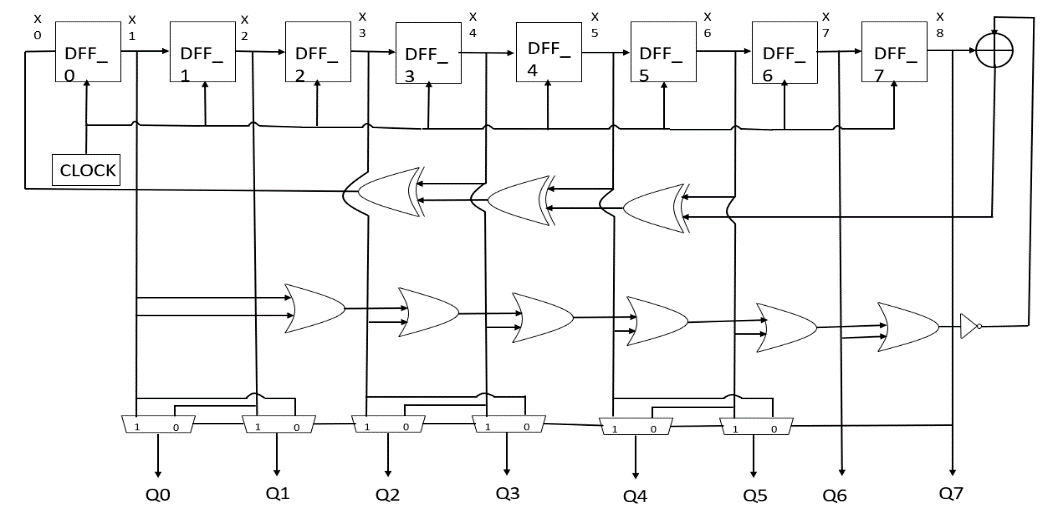
• **Bit Swapping LFSR:**

A Bit Swapping Linear Feedback Shift Register (BS-LFSR) [5] is an enhancement of the traditional Linear Feedback Shift Register (LFSR) designed to reduce transitions and improve performance. In the BS-LFSR, specific bits are swapped to achieve these benefits. For instance, in an 8-bit BS-LFSR, as shown in Figure 3.3 (where the bit length n is 8, which is even), the 0th bit is swapped with the 1st bit using a multiplexer. The 7th bit, the highest bit, is the control signal for the multiplexer that handles this swapping. It’s important to note that the 7th bit itself does not change due to the even number of flip-flops involved. This design allows the BS-LFSR to produce nearly all possible output sequences that you would need for testing purposes. However, one notable exception is that it cannot generate an output sequence that is entirely zeros.

**Fig 3.3** 8-bit BS-LFSR

• **Bit Swapping CFSR:**

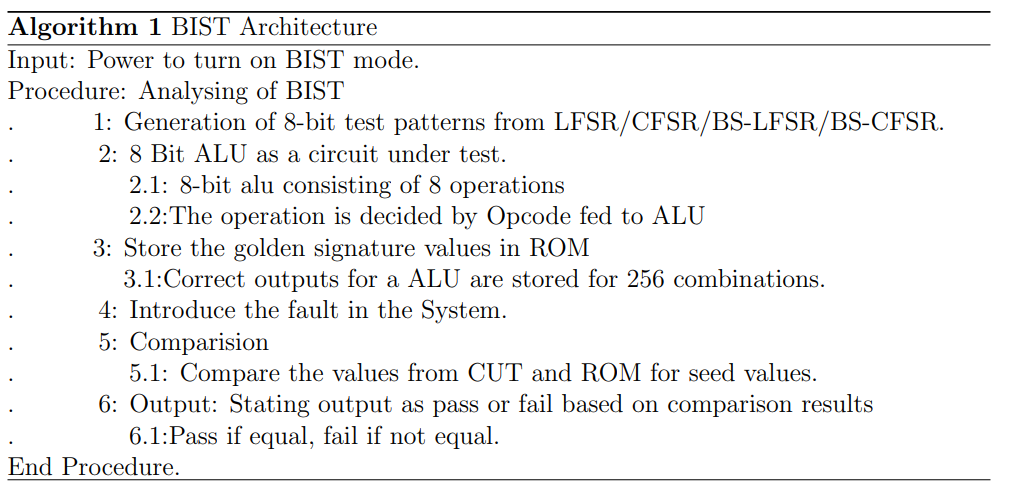
A Bit Swapping Complete Feedback Shift Register (BS-CFSR) enhances performance and lowers transitions in a traditional Complete Feedback Shift Register (CFSR). Consider an 8-bit BS-LFSR (n=8, an even number). In this configuration, the 0th bit is swapped with the 1st bit using a multiplexer, with the 7th bit serving as the select line for these multiplexers. It is important to note that the 7th bit remains unchanged because of the even number of flip-flops. An 8-bit BS-CFSR shown in Figure 3.4 with the second-to-last output bit (the 6th bit) remaining unchanged is utilized for this specific design.

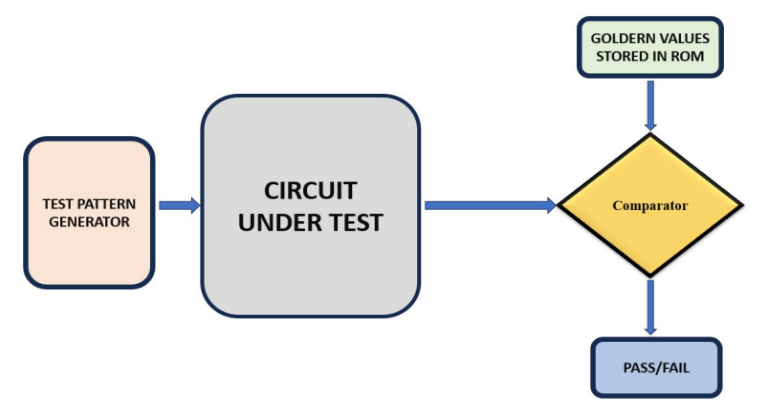


**Fig 3.4** 8-bit BS-CFSR

* 1. Design and implementation:

This section introduces the proposed algorithm for the BIST Architecture.



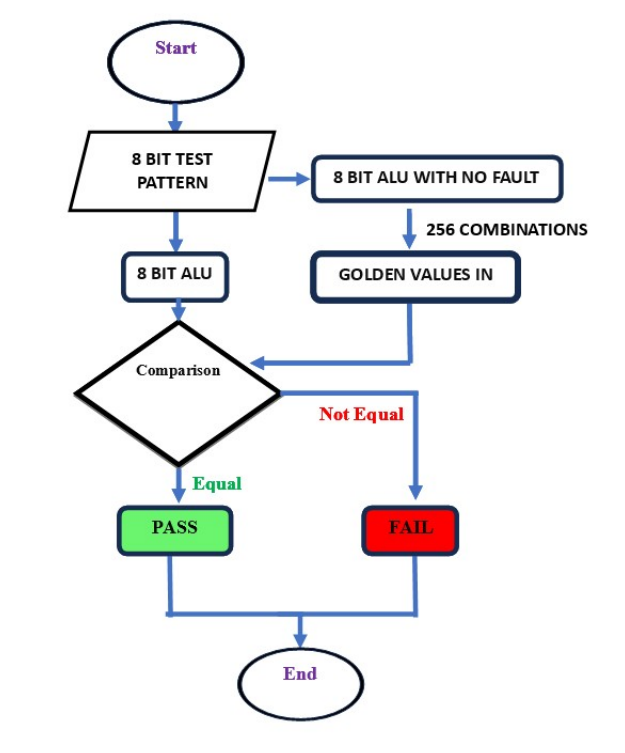


**Fig 3.5**: BIST Architecture.

The BIST architecture, as shown in Figure 3.5, validates the functionality of an 8-bit ALU by generating 8-bit test patterns through LFSR, CFSR, BS-LFSR, or BS-CFSR, which are then fed to the ALU, the circuit under test (CUT). The ALU, capable of eight operations dictated by Opcode, is evaluated against precomputed golden signature values stored in ROM for all 256 input combinations. Following fault introduction, the ALU’s outputs are compared to the ROM values. If the outputs match, the system passes; if not, it fails.

3.3 Flowchart:

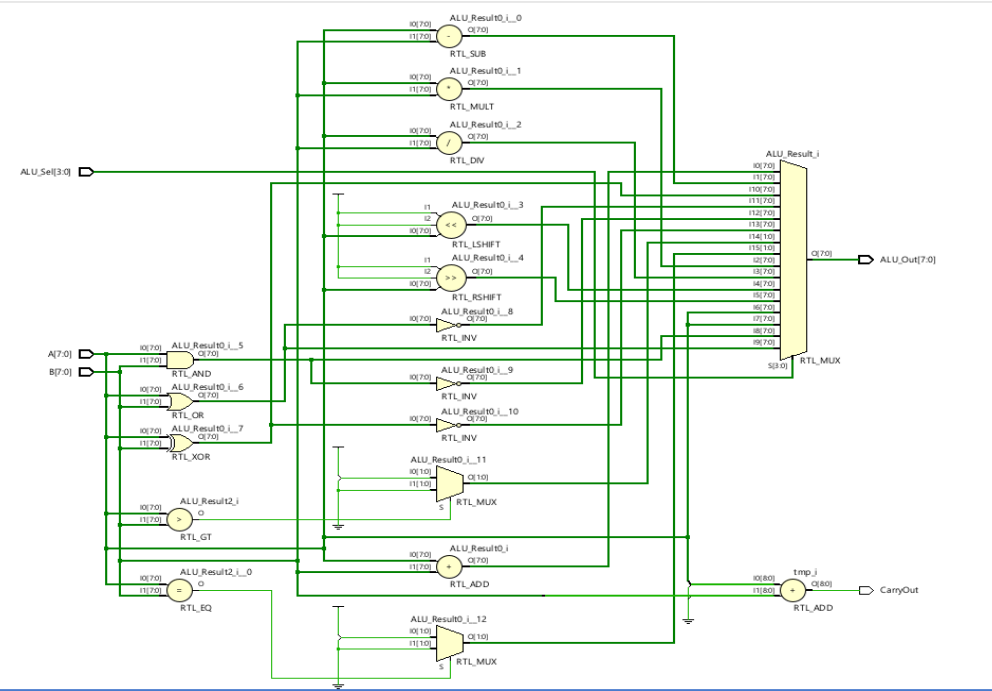
The flowchart in Figure 3.6 illustrates a visual representation of the project’s workflow in the form of a flow chart, explaining the sequential steps involved in the process.



**Fig 3.6** Flow chart for BIST Architecture

3.4 Circuit Under Test (CUT):

The Circuit Under Test is the actual circuit or device being tested within the BIST using LFSR architecture as shown in Figure 3.7. Depending on the design, the CUT may include various functional blocks, logic gates, memory cells, or other components. We used 8-bit ALU, which consists of some arithmetical and logical operations. The input to the ALU is the Random patterns generated from the Random pattern generators.



**Fig 3.7** BIST using LFSR

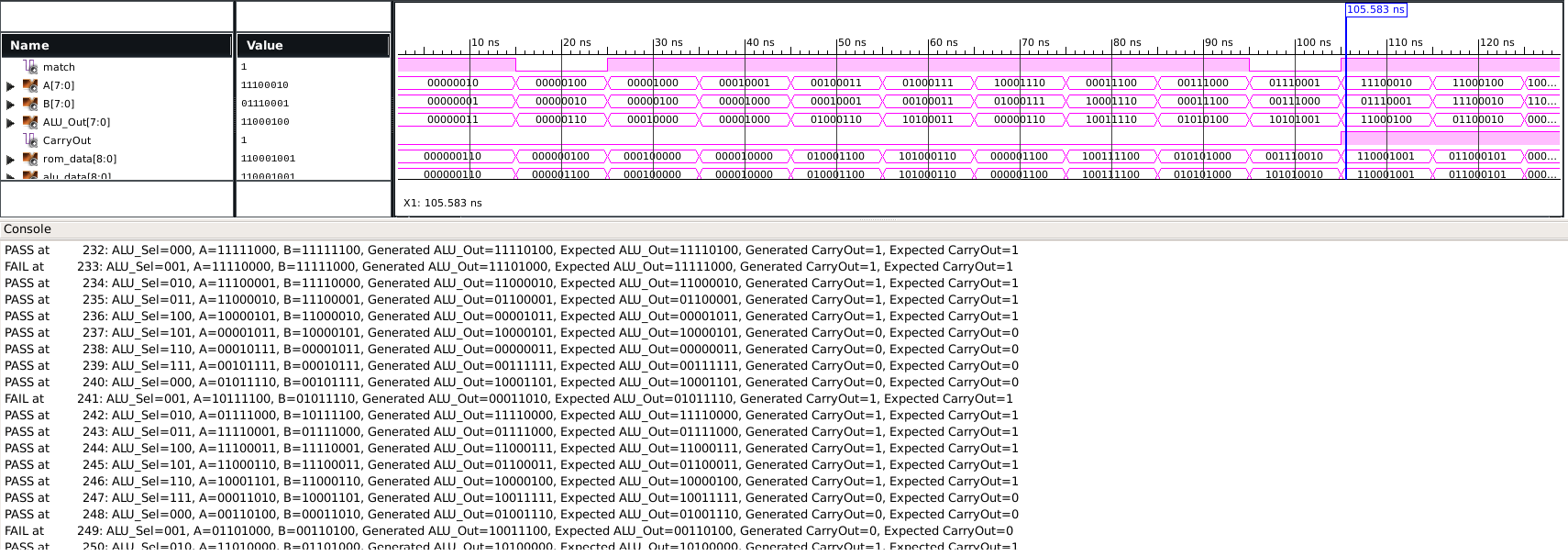
4. Results and Analysis

The implementation of design in Cadence and simulations were conducted separately for the pattern generators and BIST configurations using ISE 14.7 and Vivado. Detailed power, area, and timing analyses were performed using the Cadence Genus (Tm) tool to evaluate performance and efficiency. Stuck-at faults, where a node is fixed at a logical '1' or '0', bridge faults involving incorrect shorting of signals, open circuit faults due to broken connections, timing faults from signal delays, and functional faults from errors in logic or connections were detected during the simulation.

4.1 Simulation Results:

* BIST using **LFSR**: Figure 4.1 has Input A=00000010

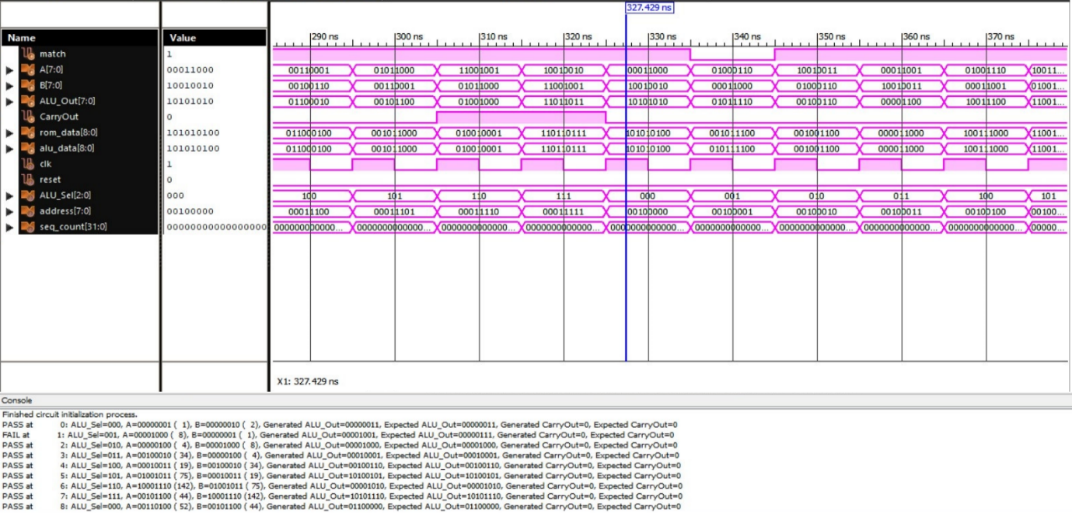
Input B=00000010.



**Fig 4.1** Simulation of BIST using LFSR

* BIST using **BS-LFSR**: Figure 4.2 has Input A=00000010

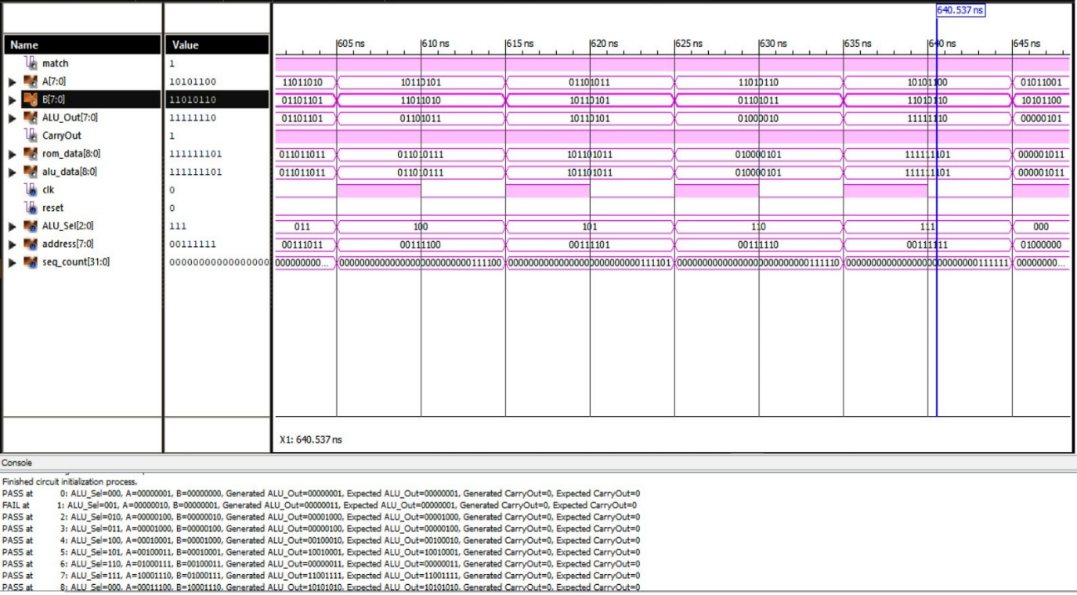
Input B=00000010.



**Fig 4.2** Simulation of BIST using BS-LFSR

* BIST using **CFSR**: Figure 4.3 has Input A=00000010

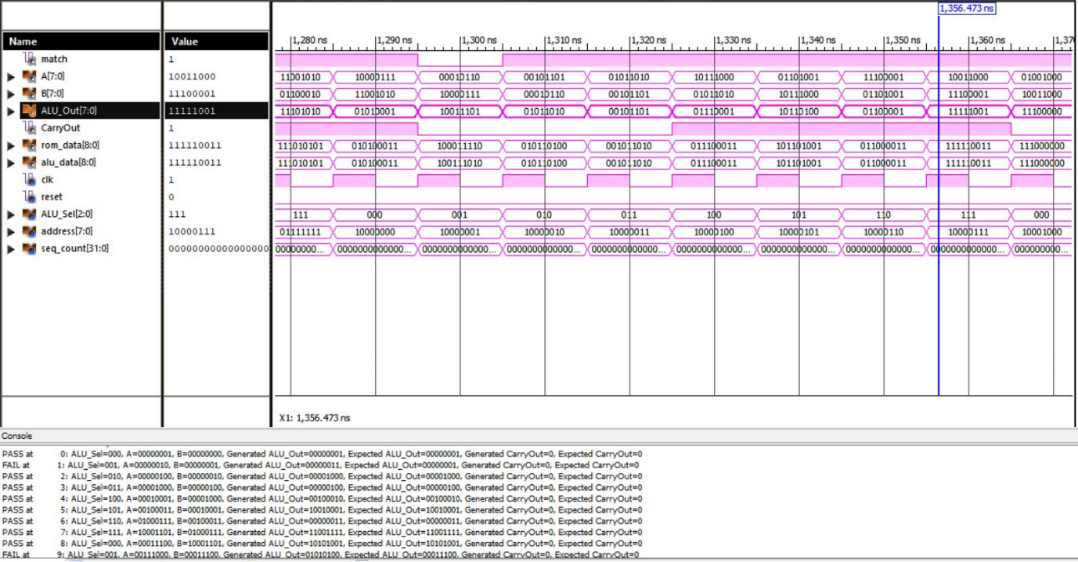
Input B=00000000.



**Fig 4.3** Simulation of BIST using CFSR

* BIST using **BS-CFSR**: Figure 4.4 has Input A=00000010

Input B=00000000.



**Fig 4.4** Simulation of BIST using BS-CFSR

**Table 1:** Power, Area, and Delay characteristics of BIST using different pattern generator designs at 90nm technology nodes.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| BIST | Static Power  (nW) | Dynamic Power  (nW) | Total Power(nW) | Total Area ( | Total Delay(ns) | Slack  (ps) |
| BIST\_LFSR | 4153.475 | 128479.976 | 132633.451 | 905.252 | 3983 | 17 |
| BIST\_BSLFSR | 3700.745 | 127711.730 | 131412.475 | 885.573 | 3705 | 295 |
| BIST\_CFSR | 4191.570 | 129891.542 | 134083.111 | 934.015 | 3998 | 2 |
| BIST\_BSCFSR | 3959.957 | 128996.631 | 132956.589 | 923.418 | 3636 | 364 |

Table 1 shows the analysis of different architectures when implemented in Cadence using a 90nm technology library, and the detailed analysis is discussed below.

**Power**: Among the analyzed BIST modules, BIST BSLFSR stands out with the lowest power consumption, featuring the least static power (3700.745 nW) and dynamic power (127711.730 nW), resulting in the lowest total power (131412.475 nW). Conversely, BIST CFSR exhibits the highest total power consumption among the modules.

**Area:** BIST BSLFSR is the module with the lowest area need, with the smallest area footprint at 885.573 um². BIST CFSR, on the other hand, has the biggest area footprint of all the modules that were examined.

**Delay:** BIST BSCFSR demonstrates the lowest total delay of 3636ps, indicating the fastest performance in signal propagation and processing. In contrast, BIST LFSR exhibits the highest total delay among the modules analyzed.

**Slack:** BIST CFSR has the least slack of 2ps, implying it operates closest to its timing constraints and may require meticulous timing optimization. On the other hand, BIST BSLFSR exhibits the highest slack among the modules.

Hence, particular design priorities BIST BSLFSR for maximum power and area efficiency and BIST BSCFSR for greatest performance speed with the least delay—determine which module is the best.

5. Conclusion

This work investigated the effectiveness of various Built-In Self-Test (BIST) implementations based on different Pseudo-Random Pattern Generators (PRPGs) for an 8-bit ALU. The analysis focused on area, power consumption, gate count, and timing characteristics across different technology nodes. By evaluating Linear Feedback Shift Registers (LFSRs), Complete Feedback Shift Registers (CFSRs), Bit-Swapped LFSRs (BS-LFSRs), and Bit-Swapped CFSRs (BS-CFSRs), the study aimed to identify the most efficient BIST design for contemporary integrated circuits. We also analyzed the power, delays, and area characteristics of BIST for all 4 pattern generators. This research provides valuable insights for engineers developing BIST architectures. The findings can guide the selection of appropriate PRPGs to achieve optimal testing solutions considering factors like area constraints, power limitations, and performance requirements in modern chip design.

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