BIST Architecture Using Different Pattern Generators

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**Abstract.** In the proposed paper, a comparison of BIST with different PRPGs (Pseudo Random Pattern Generators) is implemented. This architecture contains a PRPG, arithmetic logic unit (ALU), read-only memory (ROM), and a comparator. Some PRPGs are examined, including Linear Feedback Shift Registers (LFSR), Complete Feedback Shift Registers (CFSR), Bit Swapped-LFSR (BS-LFSR), and Bit Swapped-CFSR (BS-CFSR). These BIST implementations are evaluated in detail concerning power, area, gate count, and timing analyses. In this paper, the effectiveness of methods to reduce transitions, reduce power, and improve fault coverage is demonstrated. The extensive simulations and comparison schematics for an 8-bit variant designed across a 90 nm technology node are performed. The findings emphasize the benefits of advanced LFSR and CFSR architectures and demonstrate how they may provide more affordable, efficient, and dependable testing solutions for contemporary integrated circuits.

**Keywords:** Built-in self-test (BIST), Linear feedback shift resistor (LFSR), Complete feedback shift resistor (CFSR), Bit Swapped-LFSR (BS-LFSR), and Bit Swapped-CFSR (BS-CFSR), Arithmetic Logic Unit (ALU).

1 Introduction

BIST stands for Built-in self-test; it has brought a vast change in the testing of integrated circuits since it allows circuits to test themselves rather than requiring testing equipment. This innovation is instrumental to improving the functionality and dependability of integrated circuits. A key building block in BIST is the Pseudo-Random Pattern Generators (PRPGs), which are highly effective for generating the test patterns. This paper focuses on several types of PRPGs, such as Linear Feedback Shift Registers (LFSR), Complete Feedback Shift Registers (CFSR) [4], Bit Swapped-LFSR (BS-LFSR) [5], and Bit Swapped-CFSR (BS-CFSR). Every PRPG type has benefits for transition reduction, specific power values, and fault coverage [14]. FSRs provide all required sequences, but they cannot generate zero sequences. Therefore, CFSRs are used, which provide all possible sequences. However, both LFSR and CFSR designs have excessive transitions, leading to increased power consumption. To reduce transitions and power, BS-LFSRs and BS-CFSRs are utilized. Analysing these generators, the study aims to find the most effective BIST implementations from the point of view of area, power, gate count, and timing in different technology nodes. Therefore, this analysis is imperative in designing efficient and effective testing solutions for today’s sophisticated integrated circuits.

2 Literature survey

The table provides an overview of various research studies focused on improving the efficiency and performance of Linear Feedback Shift Registers (LFSRs) and Built-in Self-Test (BIST) technologies, especially in terms of power consumption. Several papers, including [1], [2], [5], and [8], emphasize low-power LFSR designs, particularly the bit-swapping LFSR (BS-LFSR), which is shown to reduce dynamic power dissipation compared to conventional LFSRs. The integration of BIST with these LFSR variations is a common theme, as seen in [1], [3], [5], [9], and [10], where the studies explore different Automatic Test Pattern Generator (ATPG) techniques to enhance self-testing in digital circuits. Some papers, like [7] and [9], delve into FPGA implementations, while [11] introduces BIST for analog circuits using ON/OFF keying and delay monitoring. Additionally, [4] and [10] focus on comparing ATPG techniques and introducing reversible logic, respectively, to further optimize power usage during test phases. Overall, the studies illustrate diverse approaches to achieving power-efficient and scalable BIST architectures across both digital and analog domains.

|  |  |  |  |
| --- | --- | --- | --- |
| SL.No | Paper Title | Paper Study | Year |
| [1] | Bit swapping linear feedback shift register using 130nm CMOS technology. | A 4-bit BS-LFSR achieved an active area of 1241.16µm², consuming 53.88nW with 19.43% power savings. | 2017 |
| [2] | Design of 8 and 16 bit LFSR with maximum length feedback polynomial using Verilog. | 8-bit and 16-bit LFSRs were designed using Verilog HDL and implemented on FPGA to evaluate performance, randomness, and resource usage. | 2014 |
| [4] | Comparison of various ATPG techniques to determine optimal BIST. | I The study evaluates ATPG techniques (LFSR, BS-CFSR, CA) for BIST in ISCAS circuits, finding BS-CFSR reduces power and CA improves randomness and fault coverage at 45 nm. | 2016 |
| [8] | Bit-swapping LFSR for low-power BIST. | Achieved up to 45% power reduction on ISCAS'85 and '89 benchmarks. | 2008 |
| [10] | Design and Implementation of 8-bit LFSR, Bit-Swapping LFSR and Weighted Random Test Pattern Generator. | This paper discusses a conventional LFSR, BS-LFSR, and multiple WRTPG. | 2024 |
| [11] | Structural Built In Self Test of Analog Circuits using ON/OFF Keying and Delay Monitors. | This paper proposes a low-cost structural BIST method for analog circuits by perturbing the circuit at an injection point. | 2024 |

Table 1. Summary of Literature Survey

3 Design Methodology

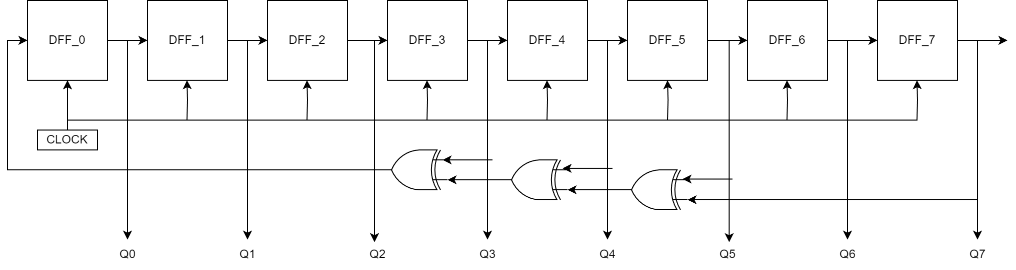
This design methodology explores advanced techniques to enhance traditional shift registers by incorporating bit-swapping mechanisms. We delve into implementing Bit Swapping Linear Feedback Shift Registers (BS-LFSR) and Bit Swapping Complete Feedback Shift Registers (BS-CFSR). These designs utilize multiplexers controlled by higher-order bits to optimize performance and reduce transitions while ensuring nearly all possible output sequences for testing purposes. By maintaining specific bits unchanged, these configurations enhance overall functionality and reliability [12].

3.1 Test Pattern Generator:

The Test Pattern Generator generates the test patterns that will be applied to the Circuit Under Test (CUT). We formulated the results through 4 different types of Test Pattern Generators, and they are Linear Feedback Shift Register (LFSR), Complete Feedback Shift Register (CFSR), Bit Swapped- LFSR(BS-LFSR), Bit Swapped CFSR(BS-CFSR). The feedback polynomial determines the sequences length [13].

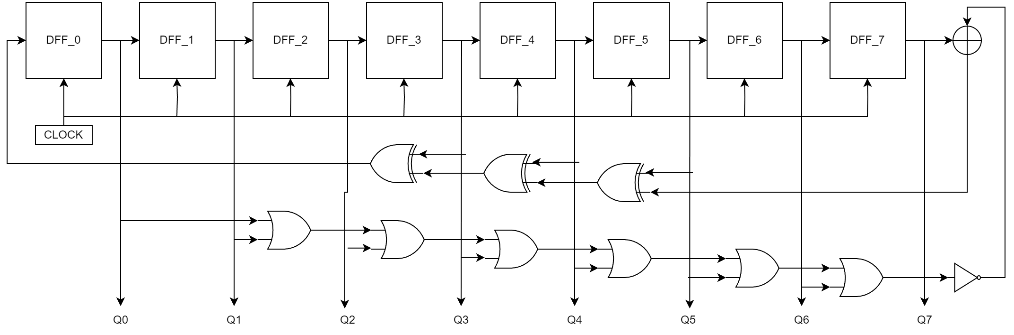
**3.1.1 Linear Feedback Shift Register (LFSR):**

The LFSR is initialized with a starting state (seed value), typically nonzero. During each clock cycle, the contents of the register shift one position to the right (or left, depending on the implementation). The feedback polynomial determines whether a flip-flop is toggled (XORed) based on the current state of the register. A LFSR generates sequences where n is the number of bits. An 8-bit LFSR generates maximum sequences i.e., 28 − 1 = 255 random states with the polynomial X8 + X6 + X5 + X4 + 1.

 **Fig 3.1** 8-bit LFSR

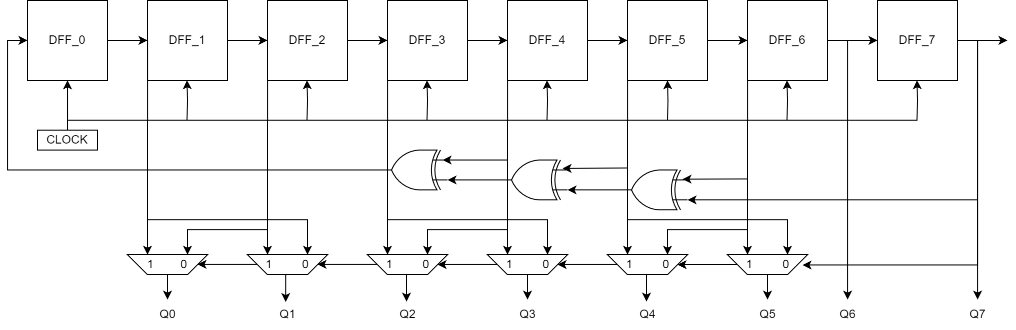
**3.1.2 Complete Feedback Shift Register (CFSR):**

LFSR can generate most of the possible output. There are still some patterns that this kind of LFSR cannot generate. test vectors but not an all-zero-activity pattern for an otherwise inactive neuron. Some resistant fault sites (RP Resistant) need all zero vectors to sensitize, whereas the classical model cannot be used. An n-bit LFSR can be converted into an n-bit CFSR by adding an n-1 input NOR connected to all except the last bit. CFSR has better fault coverage than LFSR, as it can generate sequences and sequence ‘0’ can be fed as seed, and for 8bit, all 256 sequences are generated as shown in Figure 3.2.

 **Fig 3.2** 8-bit CFSR

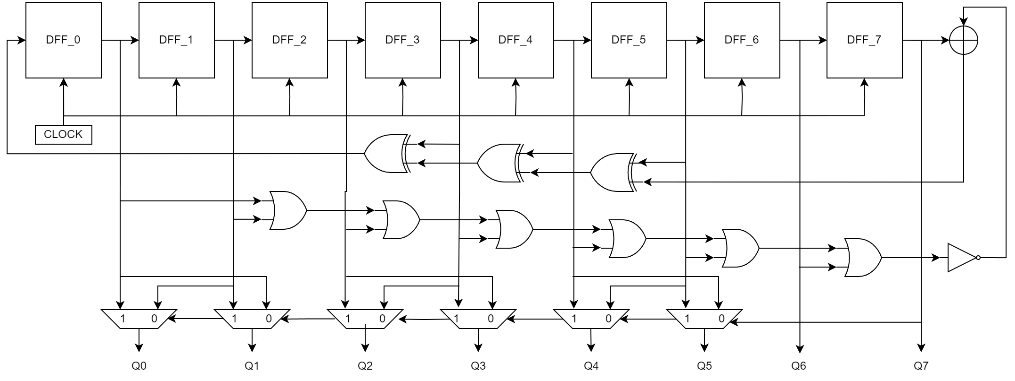
**3.1.3 Bit Swapping LFSR:**

A Bit Swapping Linear Feedback Shift Register (BS-LFSR) [5] is an enhancement of the traditional Linear Feedback Shift Register (LFSR) designed to reduce transitions and improve performance. In the BS-LFSR, specific bits are swapped to achieve these benefits. For instance, in an 8-bit BS-LFSR, as shown in Figure 3.3 (where the bit length n is 8, which is even). The 7th bit, the highest bit, is the control signal for the multiplexer that handles this swapping. when the nth bit is ‘0’ then Swapping is done between 0th and 1st and so on till (n-2) states using multiplexers and if there are odd number of states, swapping is done till (n-1) states. It’s important to note that the 7th bit itself does not change due to the even number of flip-flops involved. This design allows the BS-LFSR to produce nearly all possible output sequences that you would need for testing purposes. However, one notable exception is that it cannot generate an output sequence that is entirely zeros.

 **Fig 3.3** 8-bit BS-LFSR

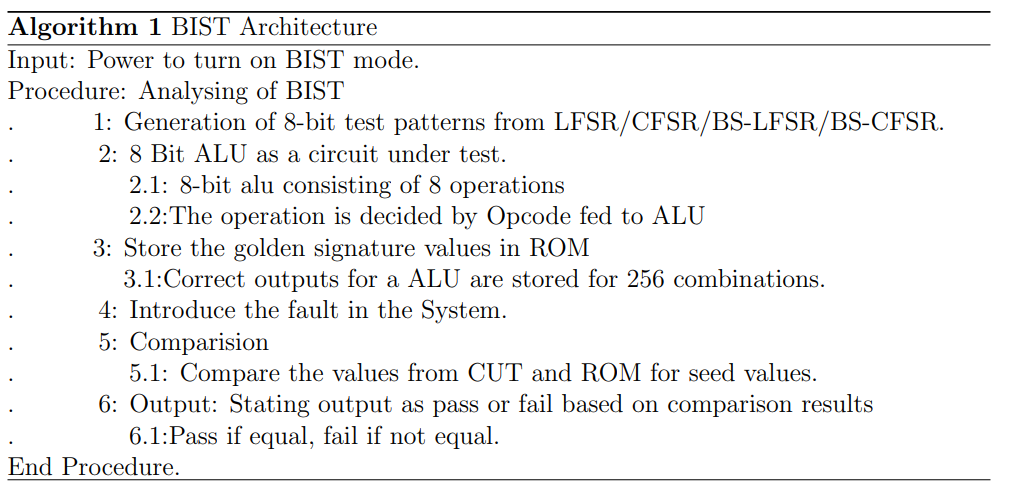
**3.1.4 Bit Swapping CFSR:**

A Bit Swapping Complete Feedback Shift Register (BS-CFSR) enhances performance and lowers transitions in a traditional CFSR. It is important to note that the 7th bit remains unchanged because of the even number of flip-flops. An 8-bit BS-CFSR produces 256 transactions with reduced number of transitions as compared to CFSR.

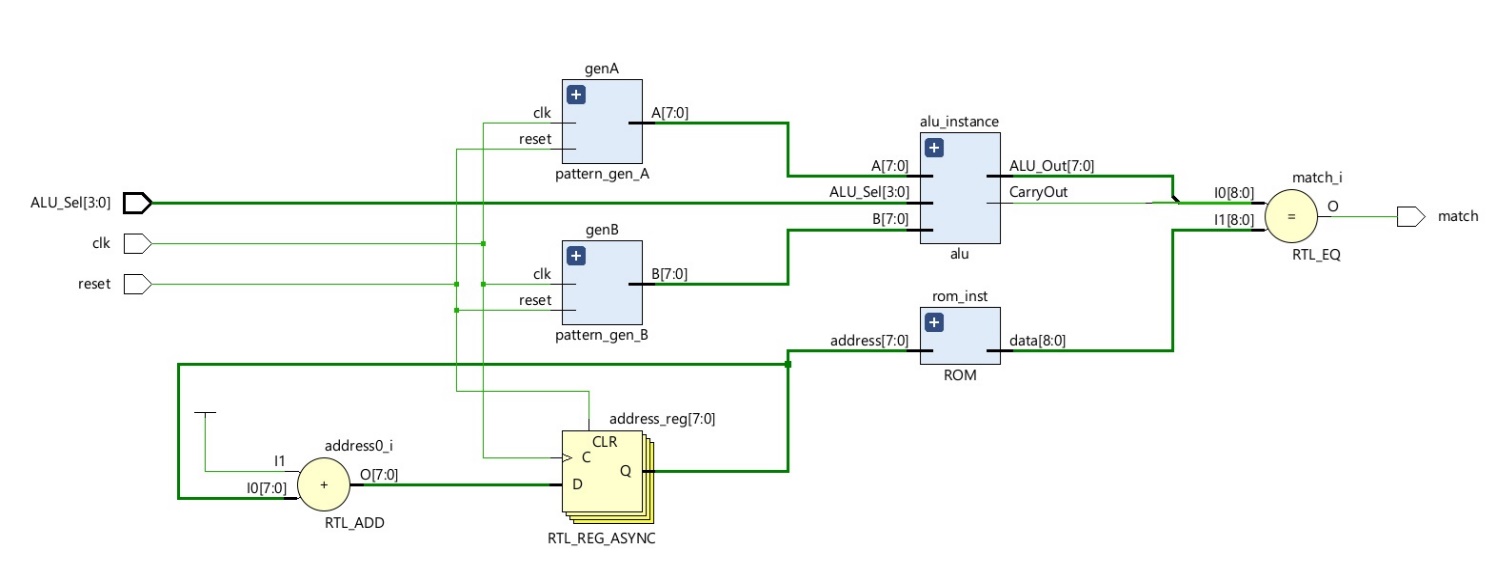
**Fig 3.4** 8-bit BS-CFSR

3.2 Design and implementation:

This section introduces the proposed algorithm for the BIST Architecture.

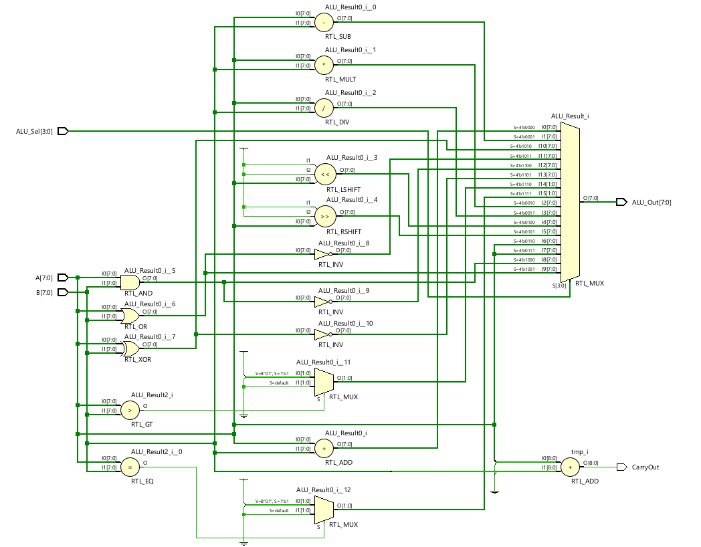


The BIST architecture, as shown in Figure 3.5, validates the functionality of an 8-bit ALU by generating 8-bit test patterns through LFSR, CFSR, BS-LFSR, or BS-CFSR, which are then fed to the ALU, the circuit under test (CUT). The ALU, capable of eight operations dictated by Opcode, is evaluated against precomputed golden signature values stored in ROM for all 256 input combinations. Following fault introduction, the ALU’s outputs are compared to the ROM values. If the outputs match, the system passes; if not, it fails.



**Fig 3.5**: BIST Architecture

3.3 Circuit Under Test (CUT):

The Circuit Under Test is the actual circuit or device being tested within the BIST architecture as shown in Figure 3.7. Depending on the design, the CUT may include various functional blocks, logic gates, memory cells, or other components. We used 8-bit ALU, which consists of some arithmetical and logical operations. The input to the ALU is the Random patterns generated from the Random pattern generators.

**Fig 3.6:** 8-Bit ALU

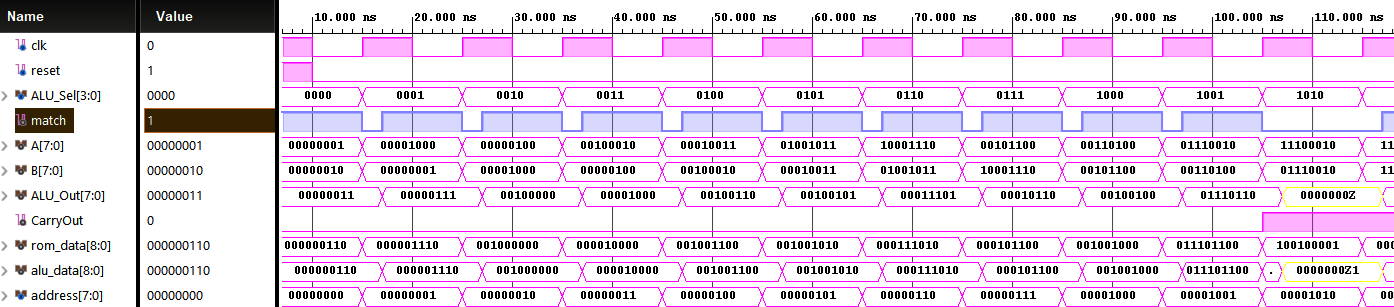
4 Results and Analysis

The implementation of design and simulations were conducted separately for the pattern generators and BIST configurations using ISE 14.7 and Vivado. Detailed power, area, and timing analyses were performed using the Cadence Genus (Tm) tool to evaluate performance and efficiency. Stuck-at faults, where a node is fixed at a logical '1' or '0', bridge faults involving incorrect shorting of signals, open circuit faults due to broken connections, timing faults from signal delays, and functional faults from errors in logic or connections were detected during the simulation.

4.1 Simulation Results:

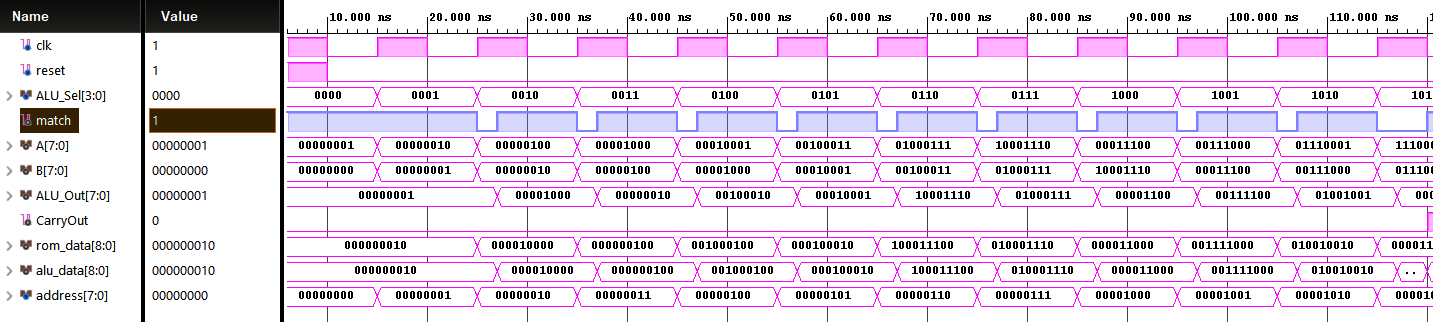
In the simulations given below, the match variable is used to identify the faults, which were introduced to the ALU.

* BIST using **BS-LFSR**: Figure 4.2 has Input A=00000010 and Input B=00000001.

**Fig 4.1** Simulation of BIST using BS-LFSR

* BIST using **BS-CFSR**: Figure 4.4 has Input A=00000010

Input B=00000000.

**Fig 4.2** Simulation of BIST using BS-CFSR

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **BIST ARCHITECHTURES** | **Total Power(nW)** | **Total Area (** | **Data Path Delay(ps)** | **Total Delay(ps)** | **Slack**  **(ps)** |
| BIST\_LFSR | 132633.451 | 905.252 | 1983 | 2983 | 17 |
| BIST\_BSLFSR | 131412.475 | 885.573 | 1705 | 2705 | 295 |
| BIST\_CFSR | 134083.111 | 934.015 | 1998 | 2998 | 2 |
| BIST\_BSCFSR | 132956.589 | 923.418 | 1636 | 2636 | 364 |

Table 2: Power, Area, and Delay characteristics of BIST using different pattern generator designs at 90nm technology node.

Table 2 shows the analysis of different architectures when implemented in Cadence using a 90nm technology library on 250Mhz clock frequency, the detailed analysis is discussed below.

**Power**: Among the analyzed BIST modules, BIST BSLFSR stands out with the lowest power consumption, featuring the least static power (3700.745 nW) and dynamic power (127711.730 nW), resulting in the lowest total power (131412.475 nW). Conversely, BIST CFSR exhibits the highest total power consumption among the modules.

**Area:** BIST BSLFSR is the module with the lowest area need, with the smallest area footprint at 885.573 um². BIST CFSR, on the other hand, has the biggest area footprint of all the modules that were examined.

**Delay:** BIST BSCFSR demonstrates the lowest total delay of 2636ps, indicating the fastest performance in signal propagation and processing. In contrast, BIST\_CFSR exhibits the highest total delay among the modules analyzed.

**Slack:** BIST\_BSCFSR has the has highest slack, implying that at the circuit has a greater timing margin, reducing the risk of timing violations. On the other hand, BIST\_CFSR exhibits the lowest slack among the modules.

Hence, particular design priorities BIST BSLFSR for maximum power and area efficiency and BIST BSCFSR for greatest performance speed with the least delay—determine which module is the best.

5 Conclusion

This work investigated the effectiveness of various Built-In Self-Test (BIST) implementations based on different Pseudo-Random Pattern Generators (PRPGs) for an 8-bit ALU. The analysis focused on area, power consumption, gate count, and timing characteristics across different technology nodes. By evaluating Linear Feedback Shift Registers (LFSRs), Complete Feedback Shift Registers (CFSRs), Bit-Swapped LFSRs (BS-LFSRs), and Bit-Swapped CFSRs (BS-CFSRs), the study aimed to identify the most efficient BIST design for contemporary integrated circuits. We also analyzed the power, delays, and area characteristics of BIST for all 4 pattern generators. This research provides valuable insights for engineers developing BIST architectures. The findings can guide the selection of appropriate PRPGs to achieve optimal testing solutions considering factors like area constraints, power limitations, and performance requirements in modern chip design.

**References**

1. N Binti Mohd Hanib, F Choong, M Bin Ibne Reaz, N Kamal, and T Badal,” Bit swapping linear feedback shift register for low power application using 130nm complementary metal oxide semiconductor technology”. *International Journal of Engineering*, 30(8):1126–1133, 2017.
2. Purushottam Y Chawke and RV Kshirsagar,” Design of 8 and 16 bit lfsr with maximum length feedback polynomial using verilog”. *In Proceedings of 13th IRF International Conference*, 2014.
3. CHRISTY RACHEL SAM,” Designing and implementing a power efficient bist in a bcd multiplier”, *Authorea Preprints*, 2023.
4. Ravi Trivedi, Sandeep Dhariwal, and Abhishek Kumar,”Comparison of various ATPG techniques to determine optimal BIST”, *In 2018 International Conference on Intelligent Circuits and Systems (ICICS)*, pages 93–98. IEEE, 2018.
5. A. Bagalkoti, S. B. Shirol, R. S, P. Kumar and R. B. Shettar, "Design and Implementation of 8-bit LFSR, Bit-Swapping LFSR and Weighted Random Test Pattern Generator: A Performance Improvement," *2019 International Conference on Intelligent Sustainable Systems (ICISS)*, Palladam, India, 2019, pp. 82-86, doi: 10.1109/ISS1.2019.8908063.
6. P. Girard, C. Landrault, S. Pravossoudovitch and A. Virazel, "Comparison between random and pseudo-random generation for BIST of delay, stuck-at and bridging faults," *Proceedings 6th IEEE International On-Line Testing Workshop (Cat. No.PR00646), Palma de Mallorca, Spain*, 2000, pp. 121-126, doi: 10.1109/OLT.2000.856623.
7. Amit Kumar Panda, Praveena Rajput, Bhawna Shukla,“FPGA Implementation of of 8,16 And 32 Bit LFSR with Maximum “, *Proceedings of 13th IRF International Conference*, 20th July-2014, Pune, India, ISBN: 978-93-84209-37-7107
8. A.S. Abu-Issa and S.F. Quigley, “Bit-swapping LFSR for low-power BIST,” *Electronics Letters*, Vol. 44 No. 6, 13th March 2008.
9. Mishra, B., Jain, R., & Saraswat, R. (2016, March),” Low power BIST based multiplier design and simulation using FPGA”, *In 2016 IEEE Students' Conference on Electrical, Electronics and Computer Science (SCEECS)* (pp. 1-6). IEEE.
10. Shirol, Suhas, S. Ramakrishna, and Rajashekhar B. Shettar. "Designing Power-Efficient BIST Architecture: Leveraging Reversible Logic for Scalable Digital Systems." *Journal of Electrical Systems* 20.2 (2024): 2747-2762.
11. S. K. Kashyap, C. Raghavendra, S. Natarajan and S. Ozev, "Structural Built In Self Test of Analog Circuits using ON/OFF Keying and Delay Monitors," *2024 IEEE 42nd VLSI Test Symposium (VTS)*, Tempe, AZ, USA, 2024, pp. 1-7, doi: 10.1109/VTS60656.2024.10538672.
12. Suhas B Shirol, Rajashekar B Shettar, “A Comparative Study of Low Power Testing Techniques for Digital Circuits”, *International Journals of Advanced Research in Computer Science and Software Engineering*, 2017.
13. R. Kademani, S. Shirol, S. Siddamal, V. H M and R. M, "GUI Implementation of Logic Built in Self-Test[LBIST]," *2024 3rd International Conference for Innovation in Technology (INOCON)*, Bangalore, India, 2024, pp. 1-6, doi: 10.1109/INOCON60754.2024.10511846.
14. S. Gupta, G. Goyal and A. K. Rana, "Analysis of Different LFSRs for VLSI IC Testing," *2024 IEEE 4th International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI SATA)*, Bangalore, India, 2024, pp. 1-5, doi: 10.1109/VLSISATA61709.2024.10560316.