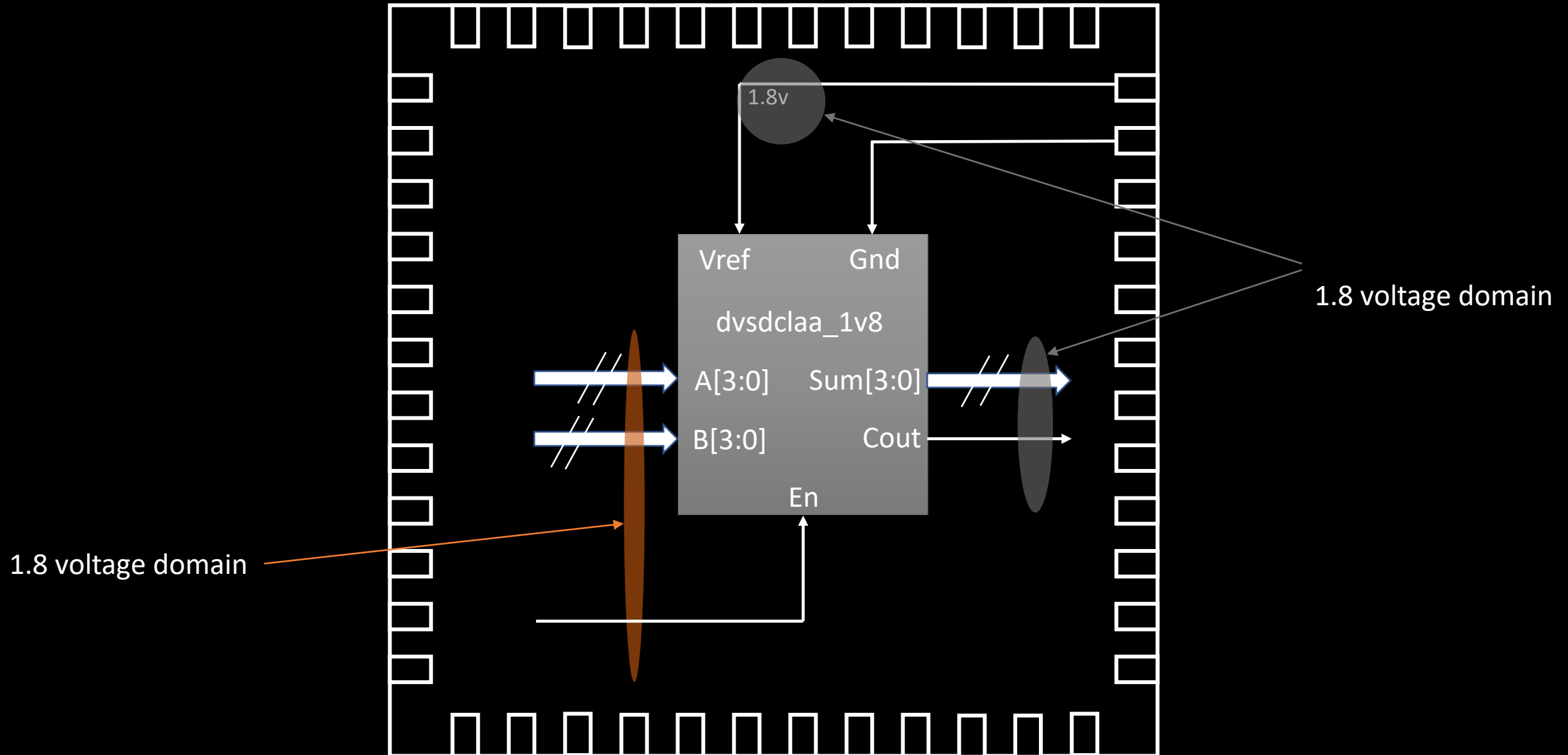


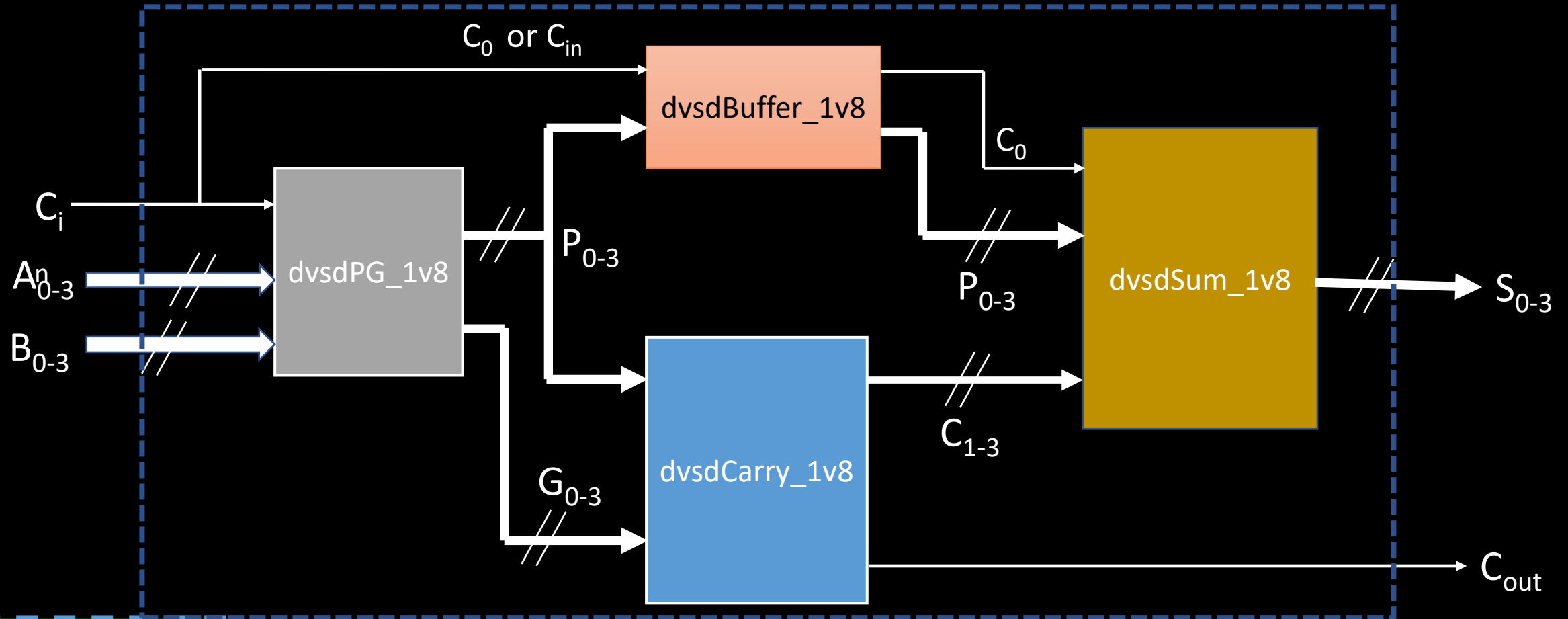
4-bit CLA adder spec sheet for 130nm tech node

- Specs Released under APACHE LICENSE 2.0
- For any query please contact aman4585imp@gmail.com

Application note for 4-bit CLA Adder (dvsdclaa 1v8)



Inside view of dvsdclaa_1v8

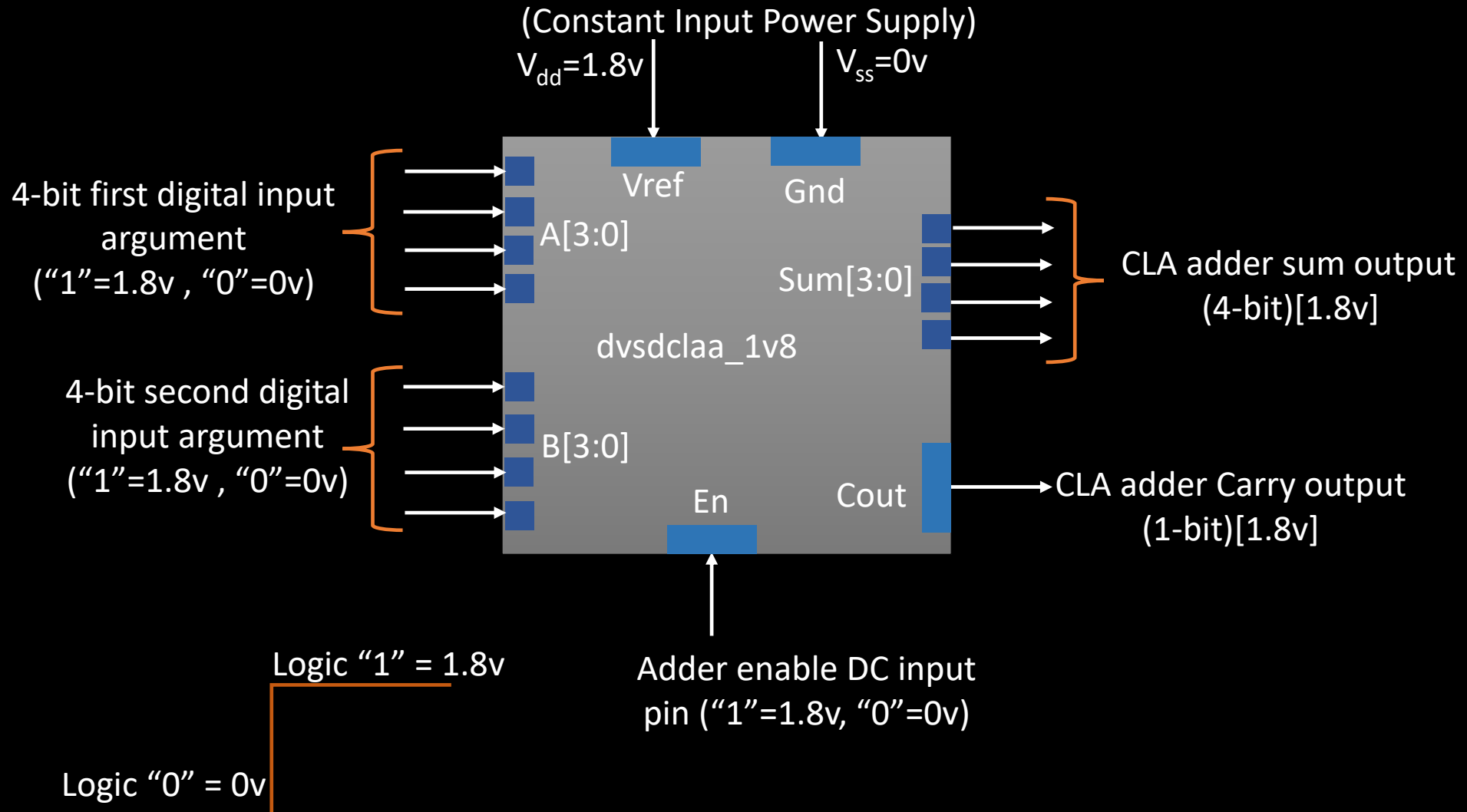


For each block

$V_{dd}=1.8v$

$V_{ss}=0v$

dvsdclaa_1v8 Operating Modes



dvsdclaa_1v8 Operating Modes

Propagation
Delay (T_{pd})=7ns

Any output
Pin (in Volt)

1.8

0

5.000

5.010

Time axis
(in us)

4-bit digital input
(0 to 1.8v)

$V_{dd}=1.8v$

$V_{ss}=0v$

Vref

Gnd

A[3:0]

Sum[3:0]

dvsdclaa_1v8

B[3:0]

En

Cout

CLA adder
sum output
(4-bit)[0.5 to
1.9v]

CLA adder
Carry output
(1-bit)[1.8v]

Adder enable DC input
pin (1.8v)

Operating

Free air Temperature range :
0° to 70° C

Storage Temperature range :
-65° to 150° C

Propagation delay occurs due to Rising or Falling
edges in input signals

For less distortion T_{rd} or T_{fd} = 1ps to 100ns

T_{rd}

T_{fd}

1.8v ("1")

0v ("0")