ΣΧΕΔΙΑΣΗ ΨΗΦΙΑΚΩΝ ΣΥΣΤΗΜΑΤΩΝ

ΑΣΚΗΣΗ 2

ΑΠΟΚΩΔΙΚΟΠΟΙΗΤΗΣ 2 ΣΕ 4

```
library ieee;
use ieee.std_logic_1164.all;

entity decoder2to4 is
        begin
        port(
        a: in STD_LOGIC_VECTOR(1 downto 0);
        b: in STD_lOGIC_VECTOR(3 downto 0)
);
        end decoder2to4;



architecture arc of decoder2to4 is
 begin
        process(a)
        begin
        case a is
        when "00" => b <= "0001";when "01"=> b <= "0010";when "10"=> b <= "0100";when "11"=> b <= "1000";
        end case;
```

```vhdl
        end process;

end arc;
```

ΠΟΛΥΠΛΕΚΤΗΣ 2 ΣΕ 1 ΜΕ ΕΠΙΛΟΓΗ

```vhdl
library ieee;
use ieee.std_logic_1164.all;

entity decoder2to4 is
        begin
        port(
        a: in STD_LOGIC_VECTOR(1 downto 0);
        b: in STD_lOGIC_VECTOR(3 downto 0)
);
        end decoder2to4;




architecture arc of decoder2to4 is
 begin
        process(a)
        begin
        case a is
        when "00" => b <= "0001";when "01"=> b <= "0010";when "10"=> b <= "0100";when
"11"=> b <= "1000";
        end case;


        end process;
end arc;
```

ΑΠΟΚΩΔΙΚΟΠΟΙΗΤΗΣ 2 ΣΕ 4

```vhdl
library ieee;
use ieee.std_logic_1164.all;


entity decoder2to4 is
        begin
        port(
        a: in STD_LOGIC_VECTOR(1 downto 0);
        b: in STD_lOGIC_VECTOR(3 downto 0)
);
        end decoder2to4;




architecture arc of decoder2to4 is
 begin
        process(a)
        begin
        case a is
        when "00" => b <= "0001";when "01"=> b <= "0010";when "10"=> b <= "0100";when
"11"=> b <= "1000";
        end case;


        end process;
end arc;
```

ΤΡΙΠΛΟΣ ΠΟΛΥΠΛΕΚΤΗΣ (3 ΒΙΤ) 2 ΣΕ 1

```vhdl
 entity  mux_3bit_2to1 is
 port(
s : in STD_LOGIC;
a , b: in STD_LOGIC_VECTOR(2 DOWNTO 0);
```

```vhdl
d : out STD_LOGIC_VECTOR(2 DOWNTO 0)
);
END mux_3bit_2to1;


 architecture arc of mux_3bit_2to1 is
begin
d <= a when s = '0' else
     b when s='1' else
     null;
end arc;
```