Theoretical calculation for sizing of transistors.

Design Specification and Parameters:

- Target gain (A_v): 25
- Frequency (f): 100MHz
- Supply Voltage: 1.8V
- Choosen G_m/I_d Ratio: $15V^{-1}$
- Overdrive Voltage assumed: 0.2V
- Current (I_d): 50μA
- Technology used: 180nm
- Parameters:
  - Electron mobility (μ_n): $400 cm^2/V.s$
  - Oxide capacitance per unit area (C_{ox}): $7.8 fF/m^2$

Gain Calculation

The gain of the OTA can be expressed as:-

$$A_v = g_m \cdot R_{out}$$

Given the target gain:

$$A_v = 25$$

Transconductance (G_m) Calculation

Using (G_m/I_d) ratio and drain current (I_d):

$$g_m = \left(\frac{G_m}{I_d}\right) \times I_d = 15 \times 50 \times 10^{-6} S = 0.75 mS.$$

Load Resistance Calculation.

Using the target gain and Calculated g_m:

$$R_{load} = \frac{A_v}{g_m} = \frac{25}{0.75 \times 10^{-3}} = 33.33 K\Omega$$

Transistor Sizing

Using parameters of 180 nm technology, conductance parameter (k):

$$k = \mu_n \cdot C_{ox}$$

$$k = 400\ cm^2/(V \cdot ps) \times 7.8\ fF/\mu m^2 = 3.12 \times 10^{-6} A/V^2$$

For M1 and M2:

Given the drain current (I_d) and overdrive voltage (V_{ov}), calculate the aspect ratio (W/L):

$$I_d = \frac{1}{2} k \left(\frac{W}{L}\right) V_{ov}^2$$

$$\left(\frac{W}{L}\right) = \frac{2I_d}{kV_{ov}^2}$$

$$\left(\frac{W}{L}\right) = \frac{2I_d}{KV_{ov}^2}$$

$$= \frac{2 \times 50 \times 10^{-6}}{3.12 \times 10^{-6} \times (0.2)^2} \approx 27.78$$

This aspect ratio matches the given sizes in the netlist for M1 and M2:

$$\left(\frac{W}{L}\right) = \frac{10 \times 10^{-6}}{360 \times 10^{-9}} \approx 27.78$$

For M3:

Similarly, for M3:

$$\left(\frac{W}{L}\right) = \frac{9.6 \times 10^{-6}}{360 \times 10^{-9}} \approx 26.67$$

for M6 and M7:

for PMOS transistors M6 and M7

$$\left(\frac{W}{L}\right) = \frac{12 \times 10^{-6}}{360 \times 10^{-9}} \approx 33.33$$

Thus, the Calculated aspect ratio for M1, M2, M3, M6, M7 are consisted with values used in LTspice netlist with little adjustment of values.