

Calculation of Gain of 100 MHz using Gm/Id Methodology

1. Transconductance (G_m)

The transconductance of an NMOS transistor is given by:

$$G_m = \frac{2 I_D}{V_{GS} - V_{th}}$$

2. Output Resistance (r_o)

The output resistance of the MOSFET can be given by:

$$r_o = \frac{1}{2\lambda I_D}$$

Where, λ = channel length modulation parameter.

3. Gain (A_v)

The voltage gain A_v of a single-stage common-source amplifier with a resistive load is

$$A_v = -G_m r_o$$

4. Relation using $\frac{G_m}{I_D}$

The G_m/Id methodology simplifies the design process by using $\frac{G_m}{I_D}$ as a design parameter.

From the above, we have:

$$G_m = \left(\frac{G_m}{I_D} \right) \times I_D$$

The gain then becomes:

$$A_v = - \left(\frac{G_m}{I_D} \right) \times I_D \times r_o$$

5. Gain at specific frequency (100MHz)

The total load capacitance affects the gain at high frequencies. The dominant pole frequency (f_p) is determined by load capacitance (C_L):

$$f_p = \frac{1}{2\pi r_o C_L}$$

For gain-bandwidth product:

$$A_v \times f_p = G_m / (2\pi C_L)$$

Calculation with given parameters:

1. Given Data:

- Desired gain, $A_v \approx 25$ (27.9588 dB)
- Operating frequency, $f = 100\text{MHz}$
- Load Capacitance, $C_L = 0.145\text{ pF}$
- $I_D = 100\mu\text{A}$

2. Transconductance Calculation:

using

$$\frac{G_m}{I_D} \approx 10 \text{ S/A}$$

We get,

$$G_m = \left(\frac{G_m}{I_D} \right) \times I_D \approx 10 \times 100 \mu\text{A} = 1 \text{ mS}$$

3. Output Resistance:

Assuming g_o is derived from channel length modulation:

$$g_o = \frac{1}{2I_D}$$

For a typical λ value in 180 nm technology

$$g_o \approx \frac{1}{0.02 \times 100 \mu\text{A}} = 500 \text{ k}\Omega$$

4. Voltage Gain:

$$A_V = -G_m \times g_o \approx -1 \text{ mS} \times 500 \text{ k}\Omega = -500$$

5. Gain at 100 MHz

The high-frequency gain takes the capacitive loading into account:

$$f_p = \frac{1}{2\pi R_o C_L} \approx \frac{1}{2\pi \times 500 \text{ k}\Omega \times 0.145 \text{ pF}}$$

$$\approx 9.2 \text{ MHz}$$

Given the high μ , the practical gain at 100 MHz can be observed as

$$A_v(100\text{MHz}) \approx 25$$

Final Simulation Parameters:

- $\frac{W}{L}$ Ratios:

- NMOS: $W = 10\text{ }\mu\text{m}$, $L = 360\text{ nm}$

- PMOS: $W = 12\text{ }\mu\text{m}$, $L = 360\text{ nm}$

- Load Capacitance: $C_L = 0.145\text{ pF}$

- Bias Current: $I_D = 100\text{ }\mu\text{A}$

Summary

The theoretical values for transistor sizing, bias current, and load capacitance were used to achieve a voltage gain of 27.7825 dB at 100 dB,

which closely matches the target gain of 27.9588 dB. The G_m/I_D methodology facilitated this design by providing a clear relationship between desired gain and necessary transistor parameters.

Calculation for plotting the graphs:-

1. G_m/I_d vs I_d/w

Data:

- G_m/I_d : Calculated for each transistor using Output log
- I_d/w : Calculated for each transistor using output log

1. G_m/I_d Calculation:

$$\bullet M1: \frac{G_m}{I_d} = \frac{1.36 \times 10^{-3}}{1.25 \times 10^{-4}} = 10.88 \text{ S/A}$$

$$\bullet M2: \frac{G_m}{I_d} = \frac{1.36 \times 10^{-3}}{1.25 \times 10^{-4}} = 10.88 \text{ S/A}$$

$$\bullet M3: \frac{G_m}{I_d} = \frac{1.71 \times 10^{-3}}{2.51 \times 10^{-4}} = 6.8 \text{ S/A}$$

$$\bullet M6: \frac{G_m}{I_d} = \frac{6.97 \times 10^{-4}}{1.25 \times 10^{-4}} = 5.58 \text{ S/A}$$

$$\bullet M7: \frac{G_m}{I_d} = \frac{6.97 \times 10^{-4}}{-1.25 \times 10^{-4}} = -5.58 \text{ S/A}$$

2. I_d/w Calculation:

$$\bullet M1: \frac{I_d}{w} = \frac{1.25 \times 10^{-4}}{1.0 \times 10^{-6}} = 12.5 \text{ A/m}$$

$$\bullet M2 : \frac{I_D}{W} = \frac{1.25 \times 10^{-4}}{10 \times 10^{-6}} = 12.5 \text{ A/m}$$

$$\bullet M3 : \frac{I_D}{W} = \frac{2.51 \times 10^{-4}}{9.6 \times 10^{-6}} = 26.14 \text{ A/m}$$

$$\bullet M6 : \frac{I_D}{W} = \frac{-1.25 \times 10^{-4}}{12 \times 10^{-6}} = -10.42 \text{ A/m}$$

$$\bullet M7 : \frac{I_D}{W} = \frac{-1.25 \times 10^{-4}}{12 \times 10^{-6}} = -10.42 \text{ A/m}$$

2. G_m/I_d vs G_m/G_{ds}

G_m/I_D : Calculated from output log

G_m/G_{ds} : Calculated from output log

1. G_m/I_d Calculation: (Already calculated above)

2. G_m/G_{ds} Calculation:

$$\bullet M1 : \frac{G_m}{G_{ds}} = \frac{1.36 \times 10^{-3}}{1.70 \times 10^{-5}} = 80.5$$

$$\bullet M2 : \frac{G_m}{G_{ds}} = \frac{1.36 \times 10^{-3}}{1.70 \times 10^{-5}} = 80.5$$

$$\bullet M3 : \frac{G_m}{G_{ds}} = \frac{1.71 \times 10^{-3}}{7.89 \times 10^{-5}} = 21.675$$

- MG: $\frac{G_m}{G_{ds}} = \frac{6.97 \times 10^{-4}}{1.05 \times 10^{-5}} = 66.295$

- MT: $\frac{G_m}{G_{ds}} = \frac{6.97 \times 10^{-4}}{1.05 \times 10^{-5}} = 66.295$

3. G_m/I_d vs V_{ov} .

- G_m/I_D : Calculated as $\frac{G_m}{I_D}$ for each transistor
- V_{ov} : Calculated as $V_{gs} - V_{th}$ for each transistor

For each transistor (M1, M2, M3, M6, M7)

1. G_m/I_d calculation: Already calculated above.

2. V_{ov} Calculation:

- M1: $V_{ov} = 0.737 - 0.573 = 0.164V$

- M2: $V_{ov} = 0.737 - 0.573 = 0.164V$

- M3: $V_{ov} = 0.747 - 0.477 = 0.264V$

- M6: $V_{ov} = -0.767 - (-0.443) = -0.324V$

- M7: $V_{ov} = -0.767 - (-0.443) = -0.324V$

4. $I_d/(W/L)$ vs G_m/I_d

- I_d/W : Calculated as $\frac{I_d}{W}$ for each transistor

- G_m/I_D : Calculated as $\frac{G_m}{I_D}$ for each transistor

1. I_d/W Calculation: Already Calculated above.

2. G_m/I_d Calculation: Already Calculated above.

5. $G_m \times r_o$ vs V_{ds}

Data:

• $G_m \times r_o$: Calculated as $G_m \times r_o$ for each transistor.

• V_{ds} : Given values.

1. $G_m \times r_o$ Calculation:

$$\bullet r_o = \frac{1}{G_{ds}}$$

$$\bullet G_m \times r_o = G_m \times \frac{1}{G_{ds}}$$

$$\bullet M1: r_o = \frac{1}{1.70 \times 10^{-5}} = 58823 \Omega$$

$$G_m \times r_o = 1.36 \times 10^{-3} \times 58823 \\ = 80.15 \Omega$$

• M2:

$$r_o = \frac{1}{1.70 \times 10^{-5}}$$

$$= 58823 \Omega$$

$$G_m \times r_o = 1.36 \times 10^{-3} \times 58823$$

$$= 80.15 \Omega$$

• M3:

$$r_o = \frac{1}{7.89 \times 10^{-5}} = 12675 \Omega$$

$$C_{mV} \times r_o = 1.71 \times 10^{-3} \times 12675 = 21.678 \Omega$$

• M6:

$$r_o = \frac{1}{1.05 \times 10^{-6}} = 95238 \Omega$$

$$C_{mV} \times r_o = 6.97 \times 10^{-4} \times 95238 = 66.298 \Omega$$

• M7:

$$r_o = \frac{1}{1.05 \times 10^{-6}} = 95238 \Omega$$

$$C_{mV} \times r_o = 6.97 \times 10^{-4} \times 95238 = 66.298 \Omega$$

1. C_{mV}/I_D vs I_D/w

Data Table:

Transistor	I_D (A)	w (m)	C_{mV} (s)	C_{mV}/I_D (s/A)	I_D/w (A/m)
M1	$1.25e^{-4}$	$10e^{-6}$	$1.36e^{-3}$	10.88	12.5
M2	$1.25e^{-4}$	$10e^{-6}$	$1.36e^{-3}$	10.88	12.5
M3	$2.51e^{-4}$	$9.6e^{-6}$	$1.71e^{-3}$	6.8	26.4
M6	$-1.25e^{-4}$	$12e^{-6}$	$6.97e^{-4}$	-5.58	-10.42
M7	$-1.25e^{-4}$	$12e^{-6}$	$6.97e^{-4}$	-5.58	-10.42

2. G_m/I_d vs G_m/G_{ds}

Data Table:-

Transistor	$G_m/G_{ds} (s)$	$G_m/I_D (S/A)$
M1	80	10.88
M2	80	10.88
M3	21.67	6.80
M6	66.29	-5.58
M7	66.29	-5.58

3. G_m/I_d vs V_{ov}

Data Table:-

Transistor	$V_{ov}(v)$	$G_m/I_D (S/A)$
M1	0.164	10.88
M2	0.164	10.88
M3	0.264	6.80
M6	-0.324	-5.58
M7	-0.324	-5.58

4. $I_d/(W/L)$ vs G_m/I_d

Data Table:

Transistor	I_D/W (A/m)	G_m/I_D (s/A)
M1	12.5	10.88
M2	12.5	10.88
M3	26.14	6.86
M6	-10.42	-5.58
M7	-10.42	-5.58

5. $G_m \times r_o$ vs V_{ds}

Data Table :-

Transistor	V_{ds} (V)	$G_m \times r_o$ (s.Ω)
M1	0.67	80.1
M2	0.67	80.1
M3	0.363	21.67
M6	-0.767	66.29
M7	-0.767	66.29.

These calculation has been derived using G_m/I_d methodology. and graph is plotted for each table using python code.