

# COL215P Assignment 1

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## What we learnt

- Synthesis: to compile the logic gates used in the design
- Implementation: to implement the above design using BASYS3 board
- Bitstream: to convert the implemented design in machine-readable form

## What we experimented

### 1. EDA playground

- We ran the or gate example with shortened testbenches

```
testbench.vhd
10 -- DUT component
11 component or_gate is
12 port(
13   a: in std_logic;
14   b: in std_logic;
15   q: out std_logic;
16 end component;
17
18 signal a_in, b_in, q_out: std_logic;
19
20 begin
21
22 -- Connect DUT
23 DUT: or_gate port map(a_in, b_in, q_out);
24
25 process
26 begin
27   a_in <= '0';
28   b_in <= '0';
29   wait for 1 ns;
30   assert(q_out='0') report "Fail 0/0" severity error;
31
32   a_in <= 'X';
33   b_in <= '1';
34   wait for 1 ns;
35   assert(q_out='1') report "Fail 0/1" severity error;
36
37   a_in <= '1';
38   b_in <= 'X';
39   wait for 1 ns;
40   assert(q_out='1') report "Fail 1/X" severity error;
41
42 -- Clear inputs
43 a_in <= '0';
44 b_in <= '0';
45
46 assert false report "Test done." severity note;
47 wait;
48 end process;
49 end tb;
50
51
```

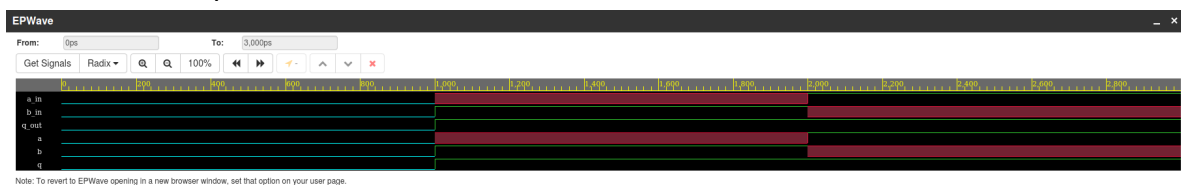
```
design.vhd
1 -- Simple OR gate design
2 library IEEE;
3 use IEEE.std_logic_1164.all;
4
5 entity or_gate is
6 port(
7   a: in std_logic;
8   b: in std_logic;
9   q: out std_logic;
10 end or_gate;
11
12 architecture rtl of or_gate is
13 begin
14   process(a, b) is
15   begin
16     q <= a or b;
17   end process;
18 end rtl;
19
```

Log

```
# SLP: Finished : 0.0 [s]
# ELAB2: You do not have a license to run VHDL performance optimized simulation. Contact Aldec for ordering information - sales@aldec.com.
# ELAB2: Elaboration final pass complete - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of simulation is reduced.
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 5399 kB (elbread=427 elab2=4829 kernel=142 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# EXECUTION:: NOTE : Test done.
# EXECUTION:: Time: 3 ns, Iteration: 0, Instance: /testbench, Process: line_26.
# KERNEL: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
```

Done

- Ep wave:



## - NAND:

testbench.vhd

VHDL Testbench

```
10
11 -- DUT component
12 component nand_gate is
13 port(
14   a: in std_logic;
15   b: in std_logic;
16   q: out std_logic;
17 end component;
18
19 signal a_in, b_in, q_out: std_logic;
20
21 begin
22
23 -- Connect DUT
24 DUT: nand_gate port map(a_in, b_in, q_out);
25
26 process
27 begin
28   a_in <= '1';
29   b_in <= '1';
30   wait for 1 ns;
31   assert(q_out='0') report "Fail 0/0" severity error;
32
33   a_in <= '1';
34   b_in <= '0';
35   wait for 1 ns;
36   assert(q_out='1') report "Fail 0/1" severity error;
37
38   a_in <= '0';
39   b_in <= 'X';
40   wait for 1 ns;
41   assert(q_out='1') report "Fail 1/X" severity error;
42
43 -- Clear inputs
44   a_in <= '0';
45   b_in <= '0';
46
47   assert false report "Test done." severity note;
48   wait;
49 end process;
50 end tb;
51
```

design.vhd

not.vhd

```
15 begin
16   q <= a and b;
17 end process;
18 end rtl;
19
20
21 library IEEE;
22 use IEEE.std_logic_1164.all;
23
24 entity nor_gate is
25 port(
26   a: in std_logic;
27   b: in std_logic;
28   q: out std_logic;
29 end nor_gate;
30
31 architecture rtl of nor_gate is
32 begin
33   process(a, b) is
34   begin
35     q <= a nor b;
36   end process;
37 end rtl;
38
39
40 library IEEE;
41 use IEEE.std_logic_1164.all;
42
43 entity nand_gate is
44 port(
45   a: in std_logic;
46   b: in std_logic;
47   q: out std_logic;
48 end nand_gate;
49
50 architecture rtl of nand_gate is
51 begin
52   process(a, b) is
53   begin
54     q <= not(a and b);
55   end process;
56 end rtl;
```

Log

Share

```
# SDF: Finished : 0.0 [s]
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# EXECUTION:: Time: 3 ns, Iteration: 0, Instance: /testbench, Process: line_26.
# KERNEL: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
```

Done

## - NOR:

testbench.vhd

VHDL Testbench

```
10
11 -- DUT component
12 component nor_gate is
13 port(
14   a: in std_logic;
15   b: in std_logic;
16   q: out std_logic;
17 end component;
18
19 signal a_in, b_in, q_out: std_logic;
20
21 begin
22
23 -- Connect DUT
24 DUT: nor_gate port map(a_in, b_in, q_out);
25
26 process
27 begin
28   a_in <= '0';
29   b_in <= '0';
30   wait for 1 ns;
31   assert(q_out='1') report "Fail 0/0" severity error;
32
33   a_in <= 'X';
34   b_in <= '1';
35   wait for 1 ns;
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38   a_in <= '1';
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42
43 -- Clear inputs
44   a_in <= '0';
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46
47   assert false report "Test done." severity note;
48   wait;
49 end process;
50 end tb;
51
```

design.vhd

not.vhd

```
1 -- Simple OR gate design
2 library IEEE;
3 use IEEE.std_logic_1164.all;
4
5 entity and_gate is
6 port(
7   a: in std_logic;
8   b: in std_logic;
9   q: out std_logic;
10 end and_gate;
11
12 architecture rtl of and_gate is
13 begin
14   process(a, b) is
15   begin
16     q <= a and b;
17   end process;
18 end rtl;
19
20
21 library IEEE;
22 use IEEE.std_logic_1164.all;
23
24 entity nor_gate is
25 port(
26   a: in std_logic;
27   b: in std_logic;
28   q: out std_logic;
29 end nor_gate;
30
31 architecture rtl of nor_gate is
32 begin
33   process(a, b) is
34   begin
35     q <= a nor b;
36   end process;
37 end rtl;
38
```

Log

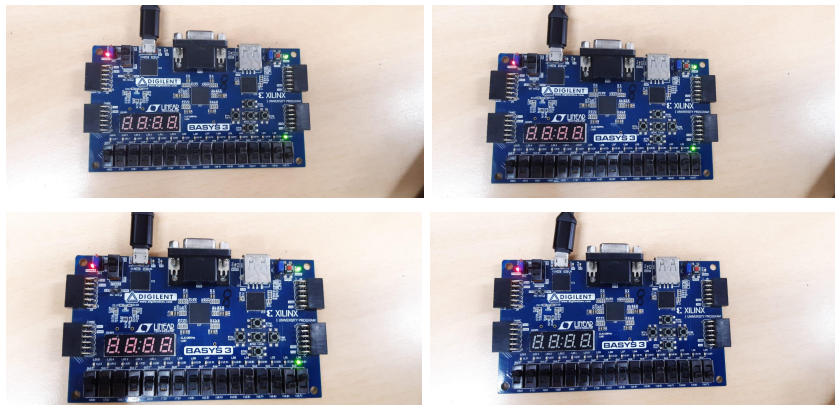
Share

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# EXECUTION:: Time: 3 ns, Iteration: 0, Instance: /testbench, Process: line_26.
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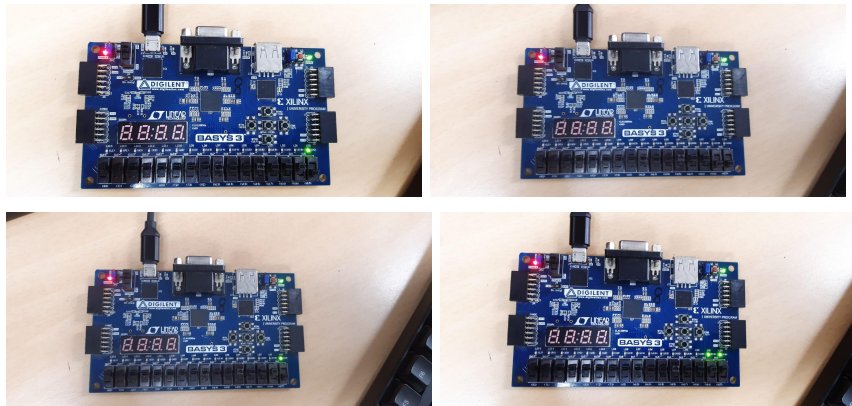
## 2. Vivado

- OR: simply took 2 switches as input and one led as output



- OR + AND (LED) : considered 2 switches for input and created 2 outputs- one led for OR gate and another led for AND gate

[Submitted source file, bit file, Constraint file for this.](#)



- OR + AND (7SD) : implemented the same design but with 7 segment display outputs

