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Random Number Generator in Verilog

Verilog generates a random number by using the $random keyword, but that works only for simulation purposes and cannot be implemented. So, when we need a random number for implementation, i.e., in hardware, it can be achieved using a shift register with some of its bits XOR'd with themselves to create a feedback term.
An N-bit generator will be able to generate $2^N - 1$ random bits before it starts repeating. For example, a 30-bit generator will have 1073741823 random states before repeating, so this can be considered truly random for most practical purposes. This project aims to construct this **random number generator**. The design is achieved by formulating the **Verilog code** using behavioral modeling and simulating the testbench.