SREE VIDYANIKETHAN ENGINEERING COLLEGE

(An Autonomous Institution, Affiliated to JNTUA, Ananthapuramu)

III B.Tech I Semester (SVEC-16) Regular/Supplementary Examinations February - 2021

VLSI DESIGN

[Electronics and Communication Engineering]

Time: 3 hours **Max. Marks: 70**

Answer One Question from each Unit.
All questions carry equal marks

UNIT-I

1	a)	Identify where the diffusion and deposition process are used in NMOS/CMOS fabrication process.	CO1	7 Marks
	b)	Compare the relative merits of three different forms of pull-up for an inverter circuit. What is the best choice for realization in: i) NMOS technology. ii) CMOS technology.	CO2	7 Marks

(OR)

2	a)	Why CMOS inverter is called as ratioless logic? Explain in detail.	CO2	7 Marks
	b)	Consider an NMOS transistor in a 0.6μm process with *W/L* = 4/2 λ (i.e., 1.2/0.6 μm). In this process, the gate oxide thickness is 100 ºA and the mobility of electrons is 350cm^2/V·s. The threshold voltage is 0.7V. Plot *Ids* ***vs.*** *Vds* for *Vgs* = 0, 1, 2, 3, 4 and 5V. ε_{si} = 3.9 x 8.85 x 10^{-14} F/cm.	CO1	7 Marks

UNIT-II

3	a)	A particular layer of MOS circuit has a resistivity p = 1Ω cm. A section of this layer is 55 μm long and 5 μm wide and has a thickness of 1 μm. Calculate the resistance from one end of this section to the other (along the length). Use the concept of sheet resistance *Rs*. What is the value of *Rs*?	CO4	7 Marks
	b)	Explain how delay estimation can be performed for a standard MOS delay unit.	CO3	7 Marks

(OR)

4	a)	Represent the stick diagram of inverter for ratioed and ratioless logic. Illustrate with examples.	CO4	7 Marks
	b)	Construct NMOS inverter layout with the help of λ-based rules. Clearly mention the design rules used in the layout.	CO1	7 Marks

UNIT-III

5	a)	Discuss the use of pass transistor logic for functional unit design. Identify the limitations of pass transistor logic.	CO5	7 Marks
	b)	Estimate CMOS inverter delay using rise-time and fall-time estimation.	CO5	7 Marks

(OR)

6	a)	Explain the construction of transmission gate based adder in detail.	CO4	7 Marks
	b)	Draw the static CMOS logic circuit for the following expression. i) Y= (ABCD)′. ii) Y= [D(A+BC)]′.	CO4	7 Marks

UNIT-IV

7	a)	Differentiate the channeled gate array and channeless gate array.	CO1	7 Marks
	b)	Explain the FPGA design flow and bring out the differences with ASIC design flow.	CO5	7 Marks

(OR)

8	a)	Discuss in detail, different architectures of programmable interconnects in FPGA.	CO1	7 Marks
	b)	Discuss any two types of programming technology used in FPGA design.	CO1	7 Marks

UNIT-V

9	a)	Discuss various fault models used for testing process.	CO6	7 Marks
	b)	Differentiate the process of test vector generation for combinational and sequential circuits.	CO6	7 Marks

(OR)

10	a)	Discuss the use of power management techniques for low power designs.	CO3	7 Marks
	b)	Discuss various approaches available in design for testability.	CO1	7 Marks