CODE No.: 19BT30404 SVEC-19

SREE VIDYANIKETHAN ENGINEERING COLLEGE

(An Autonomous Institution, Affiliated to JNTUA, Ananthapuramu)

II B.Tech I Semester (SVEC-19) Regular Examinations February – 2021

SWITCHING THEORY AND LOGIC DESIGN

[Electronics and Communication Engineering, Electronics and Instrumentation Engineering]

Time: 3 hours **Max. Marks: 60**

Answer One Question from each Unit
All questions carry equal marks

		UNIT-I				
1.	a)	Express the function $F = A + \overline{B}C$ in canonical SOP and POS.	6 Marks	L2	CO1	PO1
	b)	List the first 16 numbers in base 12; use the letters A and B to represent the last two digits. Convert the number $(456)_{12}$ to base 8	6 Marks	L3	CO1	PO3
		(OR)				
2.	a)	Generate even parity hamming code for the data word 10011010.	4 Marks	L4	CO1	PO4
	b)	i) Simplify the given Boolean expression $f = ABC + \overline{A}\,\overline{B}\,C + A\overline{B} + AB\overline{C} + \overline{A}\overline{B}\overline{C}$.	8 Marks	L2	CO1	PO2
		ii) Perform the subtraction using 10^{th} complements. i) $(1000)_{10}$-$(756)_{10}$. ii) $(10)_{10} - (100)_{10}$.				
		UNIT-II				
3.	a)	Implement the following function in multi-level NAND $F = ABC + ABC + ABD + ABD$.	6 Marks	L3	CO1	PO2
	b)	Obtain the simplified expression in POS, implement with NOR gates $F(w,x,y,z) = \sum_m (1, 2, 4, 11, 12, 13) + \sum_d (0, 3, 6, 10)$.	6 Marks	L4	CO1	PO4
		(OR)				
4.	a)	Determine essential prime implicates given Boolean expression using tabulation method $F = ACD + BCD + BCD + ACD$.	6 Marks	L3	CO1	PO2
	b)	Simplify the expression in SOP $F(w,x,y,z) = \sum_m (0, 3, 4, 5, 7) + \sum_d (8, 9, 10, 11, 12, 13, 14, 15)$.	6 Marks	L4	CO1	PO4
		UNIT-III				
5.	a)	Implementing the logic function using a multiplexer 2^{N-1} input line, where N is the number of variables in the function $F(A, B, C, D) = \sum_m (4, 5, 6, 7, 8, 13, 14, 15)$.	6 Marks	L3	CO1	PO4
	b)	Define encoder. Design Octal to Binary encoder.	6 Marks	L4	CO2	PO2
		(OR)				
6.	a)	Design a BCD to Decimal Adder Combinational circuit.	6 Marks	L2	CO2	PO1
	b)	Construct 5 to 32 decoder using one 2 to 4 decoder and four 3 to 8 decoders.	6 Marks	L4	CO2	PO2
		UNIT-IV				
7.	a)	Convert JK Flip Flop to T Flip Flop.	6 Marks	L3	CO2	PO3
	b)	Design a Universal Shift Register and explain the operation with neat diagram.	6 Marks	L3	CO1	PO6
		(OR)				
8.	a)	Design 3 Bit UP/Down Synchronous counter using T Flip Flop.	6 Marks	L3	CO2	PO6
	b)	Design a 5 Bit Ring counter and explain the operation.	6 Marks	L3	CO2	PO6

UNIT-V

9.	a)	A combinational circuit is defined by the function $F_1(A, B, C) = \sum_m (3, 5, 6, 7)$ $F_2=\sum_m (0, 2, 4,7)$. Implement the circuit with PLA having 3 inputs, 4 product terms and two outputs.	6 Marks	L3	CO3	PO2
	b)	Realize a Logic function using $F (A, B, C) = \Sigma_m (2, 4, 5, 6)$ using Hazard Free logic gate network.	6 Marks	L2	CO3	PO7
		(OR)				
10.	a)	Distinguish the following. i) PROM. ii) PAL. iii) PLA.	6 Marks	L1	CO4	PO2
	b)	Implement the following function using PROM $F_1(A, B, C) = \sum_m (0, 1, 2)$ $F_2=\sum_m (4, 5, 6, 7)$.	6 Marks	L3	CO3	PO2