CODE No.:16BT30403 SVEC-16

SREE VIDYANIKETHAN ENGINEERING COLLEGE

(An Autonomous Institution, Affiliated to JNTUA, Ananthapuramu)

II B.Tech II Semester (SVEC-16) Regular Examinations, December – 2020

SWITCHING THEORY AND LOGIC DESIGN

[Electrical and Electronics Engineering]

Time: 3 hours **Max. Marks: 70**

Answer One Question from each Unit
All questions carry equal marks

UNIT-I

1	a)	Convert the following number from given base to other three bases Decimal 623.72 to binary, octal and hexa decimal	CO1	7 Marks
	b)	Determine the value of base if $(172)_x = (598)_8$	CO1	3 Marks
	c)	Perform the following subtraction using 1's and 2's, complement method. 55 + (-77) Find the result in sign-magnitude.	CO1	4 Marks

(OR)

2	a)	Convert each of the following to the other canonical form: i) $F(X,Y, Z) = \Sigma_m (2, 5, 6)$ ii) $F(A, B, C, D) = \Pi_m (0, 1, 2, 4, 7, 9, 12)$.	CO5	7 Marks
	b)	If the Hamming code sequence 1100110 is transmitted and due to an error in one position, is received as 1110110, locate the position of the error bit using parity checks and give the method for obtaining the correct sequence.	CO1	7 Marks

UNIT-II

3	a)	Minimize the following function in standard POS form using K-map. $f(A, B, C, D) = \Sigma_m (0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$	CO5	4 Marks
	b)	Simplify the following Boolean function using Quine-McCluskey method $F(A, B, C, D) = \Sigma_m (1, 2, 3, 5, 9, 12, 14, 15) + d (4, 8, 11)$	CO1	10 Marks

(OR)

4		Reduce the following function using K-map technique and indicate the prime implicants. $F(A,B,C,D,E) = \Sigma_m (0, 1, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 18, 19, 20, 21, 22, 23, 26, 27)$	CO5	14 Marks

UNIT-III

5	a)	Design a 16:1 MUX using: i) 3:1 MUX and OR gate ii) 8:1 and 2:1 MUX	CO2	7 Marks
	b)	Design a 4-bit Gray to Binary converter using truth table, K-maps and logic circuits.	CO4	7 Marks

(OR)

6	a)	Design Half-Adder using appropriate decoder and relevant basic gates.	CO4	5 Marks
	b)	Implement BCD to seven segment display.	CO6	9 Marks

UNIT-IV

7	a)	Write a short notes on: i) State diagram ii) State table iii) Stated reduction iv) State assignment.	CO5	4 Marks
	b)	Design a sequence generator using D flip-flop to generate the sequence 101100110.	CO2	10 Marks

(OR)

8	a)	Draw a neat circuit diagram of clocked J-K flip flop using NAND gates. Give its truth table and explain race-around condition.	CO2	7 Marks
	b)	Design a 3-bit synchronous counter using J-K flip flops. Use K-maps.	CO2	7 Marks

UNIT-V

9	a)	Realize the following equations with a suitable PLA. Draw the logic diagram using PLA: i) $F_1(A,B,C,D) = A\overline{B}D + \overline{A}B\overline{D}$ ii) F_2 (A,B,C,D) = $A + B\overline{D}$	CO3	7 Marks
	b)	A 3-I/P, 4-O/P combinational circuit has the following O/P functions. A(X,Y,Z) = Σ_m(1,2,4,6) B(X,Y,Z) = Σ_m(1,3,6,7) C(X,Y,Z) = Σ_m(1,2,4,6,7) D(X,Y,Z) = Σ_m(1,2,3,5,7 Implement the circuit using a suitable PAL.	CO3	7 Marks

(OR)

10	a)	Implement the following functions on PLA $f(w, x, y, z) = \Sigma_m$ (0, 2, 6, 7, 8, 9, 12, 13)	CO3	7 Marks
	b)	Design an Excess-3 to BCD code converter using a PAL.	CO3	7 Marks