CODE No.:16BT40402 SVEC-16

SREE VIDYANIKETHAN ENGINEERING COLLEGE

(An Autonomous Institution, Affiliated to JNTUA, Ananthapuramu)

II B.Tech II Semester (SVEC-16) Regular Examinations May - 2018

DIGITAL IC APPLICATIONS

[Electronics and Communication Engineering]

Time: 3 hours **Max. Marks: 70**

Answer One Question from each Unit
All questions carry equal marks

UNIT-I

1	a)	Explain the CMOS inverter circuit behaviour with resistive loads.	CO2	7 Marks
	b)	Draw the circuit diagram of two input NAND gate by using CMOS logic and explain its operation along with the truth table.	CO2	7 Marks
		(OR)		
2	a)	Draw and explain the concept of CMOS / TTL interfacing along with one example.	CO1	8 Marks
	b)	List out the differences between TTL, ECL and CMOS logic families.	CO1	6 Marks

UNIT-II

3	a)	Design a logic circuit to detect prime number of a 4-bit input. Write the Verilog HDL program for the same in structural style of modelling.	CO5	8 Marks
	b)	Briefly explain a typical design flow for designing VLSI IC circuits using the block diagram.	CO4	6 Marks
		(OR)		
4	a)	Write the Verilog description of 4-bit ripple carry adder at gate level abstraction.	CO4	7 Marks
	b)	Discuss different loop statements in Verilog HDL.	CO6	7 Marks

UNIT-III

5	a)	Implement the following Boolean expression using 74X151 IC. F = AB + BC + AC.	CO4	8 Marks
	b)	Explain the different functions performed by the 74X181 4-bit ALU.	CO3	6 Marks
		(OR)		
6	a)	Draw the logic diagram of IC 74X280 and explain its operation with the help of a truth table.	CO3	7 Marks
	b)	Sketch the logic diagram and write a Verilog HDL code for 74X148 IC.	CO5	7 Marks

UNIT-IV

7	a)	Design a 4-bit binary synchronous counter using 74X74. Write VHDL program for this logic.	CO3	8 Marks
	b)	Explain the functional and internal behaviour of Master Slave JK flipflop.	CO1	6 Marks
		(OR)		
8	a)	Design a 3-bit LFSR counter using 74X194. List out the sequence assuming that the initial state is 111.	CO4	8 Marks
	b)	Write short notes on: i) Clock Skew. ii) Gating the Clock.	CO1	6 Marks

UNIT-V

9	a)	With the help of timing waveforms, explain Read and Write operations of SRAM.	CO1	6 Marks
	b)	Explain the necessity of 2-dimensional decoding mechanism in memories. Draw MOS transistor memory cell in ROM and explain the operation.	CO4	8 Marks
		(OR)		
10	a)	Draw the internal structure of synchronous SRAM and explain its operating modes.	CO1	7 Marks
	b)	With neat diagrams, explain Logic Block architecture of XC4000 FPGA.	CO1	7 Marks

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