SREE VIDYANIKETHAN ENGINEERING COLLEGE

(An Autonomous Institution, Affiliated to JNTUA, Ananthapuramu)

II B.Tech II Semester (SVEC-16) Regular Examinations May - 2018

SWITCHING THEORY AND LOGIC DESIGN

[Electrical and Electronics Engineering]

Time: 3 hours **Max. Marks: 70**

Answer One Question from each Unit
All questions carry equal marks

UNIT-I

1	a)	Perform the subtraction on the given unsigned binary numbers using the 2' s complement: i) 100111 – 10001. ii) 1001 – 101000.	CO4	6 Marks
	b)	The state of a 12 bit register is 100010010111. What is its contents if it represents: i) Three decimal digits in BCD. ii) Three decimal digits in the excess-3 code. iii) Three decimal digits in the 84-2-1 code. iv) A binary number.	CO1	8 Marks
		(OR)		
2	a)	Show that the dual of the exclusive-OR is equal to its complement.	CO1	6 Marks
	b)	Detect and correct the errors of even parity hamming code word i) 1101010. ii) 0101101.	CO4	8 Marks

UNIT-II

3	a)	Simplify the Boolean function using map method. $F(A,B,C,D) = A'B'CD' + B'C'D' + A'B'D' + B'CD' + A'CD + A'BD$	CO1	8 Marks
	b)	Draw a logic diagram using only two- input NOR gates to implement the function. $F(A,B,C,D) = (A'B'+AB)(C'D+CD')$	CO1	6 Marks
		(OR)		
4		Using Quine-McCluskey method simplify the Boolean function. $F(A,B,C,D,E) = \Sigma(0,1,4,5,16,17,21,25,29)$	CO1	14 Marks

UNIT-III

5	a)	Implement the following Boolean function with a multiplexer. $F(A,B,C,D) = \Sigma(0,2,5,8,10,14)$	CO3	6 Marks
	b)	Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to-4-line decoder.	CO4	8 Marks
		(OR)		
6	a)	Design 4 bit Magnitude Comparator and explain in detail.	CO3	8 Marks
	b)	Write the design procedure for combinational circuits.	CO2	6 Marks

UNIT-IV

7	a)	Draw the logic diagram of a SR latch using NOR gates. Explain its operation using excitation table.	CO2	6 Marks
	b)	Design a mod-10 Ripple counter using T flip-flops and explain.	CO6	8 Marks
		(OR)		
8	a)	Construct a JK flip-flop using a D flip-flop, a 2x1 multiplexer and an inverter.	CO3	8 Marks
	b)	What is race around condition? How it can be eliminated?	CO1	6 Marks

UNIT-V

9	a)	Draw a PLA circuit to implement the functions. $F_1 = A'B + AC + A'BC'$ and $F_2 = (AC + AB + BC)'$	CO3	7 Marks
	b)	Explain about sequential circuits, state table and state diagram.	CO5	7 Marks
		(OR)		
10	a)	The output Z of a fundamental mode, two input sequential circuit is to change from 0 to 1 only when x_2 changes from 0 to 1 while $x_1 = 1$. The output changes from 1 to 0 only when x_1 changes from 1 to 0 while $x_2 = 1$. Find a minimum row reduced flow table.	CO6	10 Marks
	b)	Design and implement Full adder with PLA.	CO1	4 Marks

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