CODE No.:16BT30403 SVEC-16

SREE VIDYANIKETHAN ENGINEERING COLLEGE

(An Autonomous Institution, Affiliated to JNTUA, Ananthapuramu)

II B.Tech I Semester (SVEC-16) Regular/Supplementary Examinations November - 2018

SWITCHING THEORY AND LOGIC DESIGN

[Electronics and Communication Engineering, Electronics and Instrumentation Engineering]

Time: 3 hours **Max. Marks: 70**

Answer One Question from each Unit
All questions carry equal marks

UNIT-I

1	a)	Reduce the following Boolean expression. i) $F = YZ + \overline{X}\overline{Y}Z + XY\overline{Z}$ ii) $F = (X + Z)(W + X)(\overline{Y} + Z)(W + \overline{Y})$	CO5	8 Marks
	b)	Convert the given expression in the standard SOP form. i) $F(X,Y,Z) = \overline{X}(\overline{Y} + Z) + \overline{Z}$ ii) $F(X,Y,Z) = (X + \overline{Y})(X + Z)$	CO4	6 Marks

(OR)

2	a)	Deduce X from the following. i) $(BA0.C)_{16} = (X)_8$. ii) $(10101100)_2 = (X)_{16}$. iii) $(FFE.C)_{16}=(X)_2$. iv) $(7562)_8 = (X)_2$.	CO1	8 Marks
	b)	The hamming code 101101101 is received. Correct it if any errors. There are four parity bits and odd parity is used.	CO2	6 Marks

UNIT-II

3	a)	Simplify the following using K-map method. $F(A, B, C, D, E) = \Sigma(0, 2, 4, 6, 9, 11, 13, 15, 17, 21, 25, 27, 31)$.	CO4	9 Marks
	b)	Implement the following function with NAND gates. $F(x,y) = \Sigma(1, 2)$.	CO3	5 Marks

(OR)

4	a)	Simplify the following using Tabular method. $F(A , B , C , D , E) = \Sigma(0, 2, 4, 6, 9, 11, 14, 22, 25, 28, 31)$.	CO4	9 Marks
	b)	Implement the following function with NAND gates. $F(x, y, z) = \Sigma(0 , 6)$.	CO3	5 Marks

UNIT-III

5	a)	Implement the following Boolean function with a multiplexer. i) $F(A, B, C, D) = \sum(1, 2, 5, 8, 6, 10,12,14)$. ii) $F(A, B, C, D) = \sum(1, 2, 5, 6, 12)$.	CO4	8 Marks
	b)	Design and implement Full adder with two half adders and OR gate.	CO3	6 Marks

(OR)

6	a)	Define Multiplexer and Implement a 32x1 MUX by Using 4x1 Multiplexers.	CO4	7 Marks
	b)	Design Binary to Gray converter.	CO6	7 Marks

UNIT-IV

7	a)	Design a JK flip flop using AND gates and NOR gates. Explain the operation of the JK flip flop with the help of characteristic table and characteristic equation. Explain the Race around condition and also explain how to eliminate it.	CO5	7 Marks
	b)	Explain the operation of 5-stage twisted ring counter with circuit diagram, state transition diagram and state table.	CO5	7 Marks

(OR)

8	a)	Give the transition table for SR, JK, D and T flip flops. Convert an SR flip flop into D flip flop.	CO2	7 Marks
	b)	Draw the logic diagram of a SR latch using NOR gates. Explain its Operation using excitation table.	CO2	7 Marks

UNIT-V

9	a)	Design a BCD to excess-3 code converter and implement using suitable PLA.	CO3	7 Marks
	b)	Reduce the number of states in the state table and tabulate the reduced state table and give proper assignment.	CO4	7 Marks

PS	NS,Z	
	X=0	X=1
A	F, 0	B, 0
B	D, 0	C, 0
C	F, 0	E, 0
D	G, 1	A, 0
E	D, 0	C, 0
F	F, 1	B, 1
G	G, 0	H, 0
H	G, 1	A, 0

(OR)

10	a)	Design a combinational circuit using ROM. The circuit accepts 3-bit binary number and generates its equivalent excess-3 code.	CO3	7 Marks
	b)	Implement the following functions using a PROM. $G(W,X,Y,Z) = \sum(0, 1, 2, 3, 4, 5, 7, 8, 10, 11, 12, 13, 14, 15)$.	CO3	7 Marks