CODE No.: 19BT40403 SVEC-19

Roll No. | | | | | | | | | | |

# SREE VIDYANIKETHAN ENGINEERING COLLEGE

(An Autonomous Institution, Affiliated to JNTUA, Ananthapuramu)

## II B.Tech II Semester (SVEC-19) Regular Examinations August – 2021

### LINEAR AND DIGITAL IC APPLICATIONS

**[ Electronics and Communication Engineering, Electronics and Instrumentation Engineering ]**

**Time: 3 hours** **Max. Marks: 60**

**Answer One Question from each Unit**
**All questions carry equal marks**

| | | | | | | |
|---|---|---|---|---|---|---|
| | | **UNIT-I** | | | | |
| 1. | a) | Illustrate the operation of instrumentation amplifier with neat sketches. | 6 Marks | L2 | CO1 | PO1 |
| | b) | List out and explain the applications of PLL. | 6 Marks | L1 | CO1 | PO2 |
| | | **(OR)** | | | | |
| 2. | a) | Draw the functional block diagram of timer in Astable mode and derive expression for free running frequency. | 6 Marks | L2 | CO1 | PO2 |
| | b) | List out and explain the applications of monostable multivibrator. | 6 Marks | L1 | CO1 | PO2 |
| | | **UNIT-II** | | | | |
| 3. | a) | Explain the operation of R-2R DAC. | 6 Marks | L2 | CO2 | PO3 |
| | b) | Explain about second order HPF with neat sketches and derive the expression for $F_L$. | 6 Marks | L2 | CO2 | PO3 |
| | | **(OR)** | | | | |
| 4. | a) | Explain the operation of Dual Slope ADC. | 6 Marks | L2 | CO2 | PO3 |
| | b) | Design a second order LPF with a cutoff frequency of 10KHz. | 6 Marks | L4 | CO2 | PO3 |
| | | **UNIT-III** | | | | |
| 5. | a) | Write the basics in HDL programming using structural and data flow modeling. | 6 Marks | L2 | CO3 | PO5 |
| | b) | Write a process based HDL program for the prime-number detector of 4-bit input and explain the flow using logic circuit. | 6 Marks | L3 | CO3 | PO5 |
| | | **(OR)** | | | | |
| 6. | a) | Explain about dataflow design elements of VHDL. | 6 Marks | L2 | CO3 | PO5 |
| | b) | Write a VHDL code for basic gates in dataflow model. | 6 Marks | L3 | CO3 | PO5 |
| | | **UNIT-IV** | | | | |
| 7. | a) | Write a VHDL program for 4x1 Multiplexer and 1x4 Demultiplexer. | 6 Marks | L3 | CO4 | PO5 |
| | b) | Explain about parity generator and checker. | 6 Marks | L2 | CO4 | PO5 |
| | | **(OR)** | | | | |
| 8. | a) | Write a HDL code for Barrel Shifter using 74x151 multiplexer. | 6 Marks | L3 | CO4 | PO5 |
| | b) | Write a HDL code 74x181 Arithmetic and Logic Unit. | 6 Marks | L3 | CO4 | PO5 |
| | | **UNIT-V** | | | | |
| 9. | a) | Explain how a JK- flip-flop can be constructed using a T- flip-flop. | 6 Marks | L2 | CO5 | PO1 |
| | b) | Write a HDL code for JK flip-flop. | 6 Marks | L3 | CO5 | PO5 |
| | | **(OR)** | | | | |
| 10. | a) | Draw the circuit of MOD 8 Down ripple counter with D-flip-flops and explain its operation. | 6 Marks | L2 | CO5 | PO1 |
| | b) | Write a HDL code for 74x194 universal shift register. | 6 Marks | L3 | CO5 | PO5 |

❀ ❀ ❀