ESE-2005 Assignment 2 Logic Gate

Exercise

1. Draw the symbol, Boolean equation, and truth table for
   (a) a three-input OR gate.
   (b) a three-input exclusive OR (XOR) gate.
   (c) a four-input XNOR gate.

2. A three-input AND-OR (AO) gate shown in Figure 1.42 produces a TRUE output if both A and B are TRUE, or if C is TRUE. Complete a truth table for the gate.

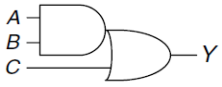

Figure 1: Three-input AND-OR gate

3. A three-input OR-AND-INVERT (OAI) gate shown below produces a FALSE input if C is TRUE and A or B is TRUE. Otherwise it produces a TRUE output. Complete a truth table for the gate.

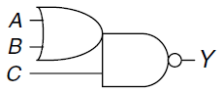

Figure 2: Three-input OR-AND-INVERT gate

4. Is it possible to assign logic levels so that a device with the transfer characteristics shown below would serve as an inverter? If so, what are the input and output low and high levels (VIL, VOL, VIH, and VOH) and noise margins (NML and NMH)? If not, explain why not.

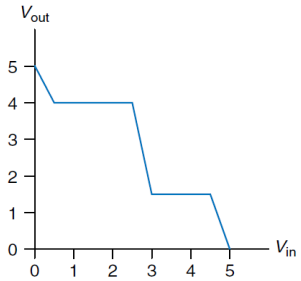

Figure 3: DC transfer characteristics

5. Is it possible to assign logic levels so that a device with the transfer characteristics shown below would serve as an inverter? If so, what are the input and output low and high levels (VIL, VOL, VIH, and VOH) and noise margins (NML and NMH)? If not, explain why not.

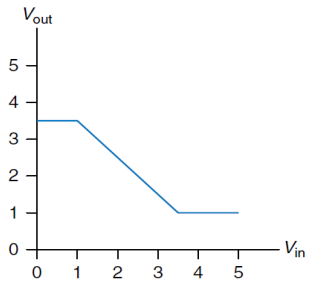

Figure 4: DC transfer characteristics

6. Is it possible to assign logic levels so that a device with the transfer characteristics shown below would serve as an buffer? If so, what are the input and output low and high levels (VIL, VOL, VIH, and VOH) and noise margins (NML and NMH)? If not, explain why not.

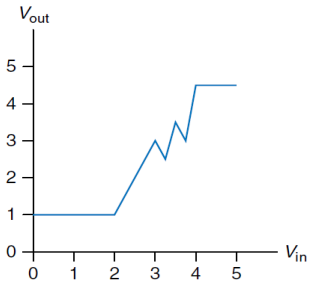

Figure 5: DC transfer characteristics

7. Ben Bitdiddle has invented a circuit with the transfer characteristics shown below that he would like to use as a buffer. Will it work? Why or why not? He would like to advertise that it is compatible with LVCMOS and LVTTL logic. Can Ben's buffer correctly receive inputs from those logic families? Can its output properly drive those logic families? Explain.

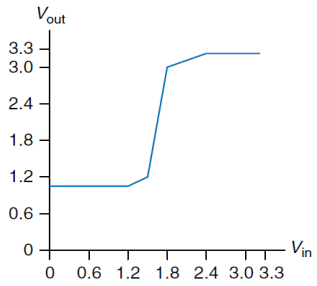

Figure 6: Ben's buffer DC transfer characteristics

8. While walking down a dark alley, Ben Bitdiddle encounters a two input gate with the transfer function shown below. The inputs are A and B and the output is Y.
What kind of logic gate did he find?
What are the approximate high and low logic levels?

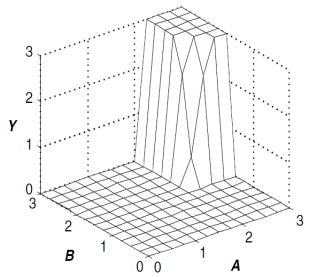

Figure 7: Two-input DC transfer characteristics