A

A/D AND D/A CONVERSION ARCHITECTURES AND TECHNIQUES

SAMEER SONKUSALE
Tufts University
Medford, Massachusetts
TAKIS ZOURNTOS
Texas A&M University
College Station, Texas

1. INTRODUCTION

Data conversion is a broad area of activity that involves both theory and implementation. Our goal in this article is to provide a focused treatment of key fundamentals and an in-depth study of the latest approaches available for data converter design in communication systems. The coverage provided here should allow the reader to plan the design of a data converter integrated circuit or begin an independent investigation of the field.

Since the early 1990s, the transceiver core shown in Fig. 1 has provided a technological backdrop for the analog integrated circuit (IC) engineer. All popular communication devices, including mobile phones, wired modems, and network interface cards, are based on some variant of this system. Although simple in form, the core embodies a wide range of expertise, and usually requires a team of engineers to develop.

This article is concerned with the data conversion subsystem that interfaces the front-end and back-end portions of the transceiver core. A data converter translates signals between analog and digital representations.[1] Our emphasis is on data converters for mobile communication systems in which cost and power savings are a priority. Therefore, although much of our discussion is of a general nature, our presentation is geared toward CMOS integrated circuit implementation and applications with low to moderate bandwidths (e.g., communications with WCDMA, IEEE 802.11a/b, or Bluetooth protocols). The emerging trend in communications of higher data rates and greater mobility necessitates the use of economical IC technologies such as deep-submicrometer CMOS that facilitate full system integration.

The design of data converters can be challenging, particularly if a concurrence of speed, accuracy, and power efficiency are required [1]. Quite often, as one attempts to improve accuracy, the area and power dissipation of a data converter design increase substantially. The tradeoff between speed and converter accuracy is most evident with oversampled converters, in which the suppression of quantization noise is closely related to the sampling rate. Broadband networking protocols such as WCDMA and IEEE 802.11b can require between 80 and 100 dB of dynamic range and signal bandwidths in the multi-megahertz range. Until 1997, such performance had not been achieved using standard CMOS fabrication [2–4].

The current state of the art (as of the end of 2003) for CMOS Nyquist-rate D/A technology provides 10-bit dynamic range at signal bandwidths up to 500 MHz [5], while CMOS Nyquist-rate A/D converters are achieving between 8 and 10 bits of dynamic range with signal bandwidths from 40 to 100 MHz [6–9]. Higher dynamic ranges (around 14 bits) at moderate speeds (up to 10 MHz) have been reported for CMOS architectures employing pipeline techniques. In Section 4, we provide a detailed discussion of the latest flash and pipeline techniques for the design of higher-speed converters.

Oversampled converters exhibit greater tolerance to component nonidealities than do their Nyquist-rate counterparts, so that 15-bit dynamic range can be readily achieved. Using feedback, the effective resolution of a coarse quantizer can be substantially increased (at the expense of reduced conversion speed). However, because of the higher sampling rates required (and limitations imposed by stability requirements on the degree of quantization noise shaping), the signal bandwidths of CMOS oversampled converter ICs are typically on the order of 1 MHz. Section 7 provides an introduction to oversampling techniques and an overview of proven architectures that achieve high resolution for narrowband applications.

1.1. Overview of Data Conversion

Data converters are categorized as either *Nyquist-rate* or *oversampled* architectures. The former class of converter includes architectures that are typically open-loop and that operate at sampling rates that (usually) do not exceed 10 times the Nyquist rate. The Nyquist-rate D/A converter is the basis of many architectures and is formed by a series of passive or active elements, switches, and an output buffer, as shown in Fig. 2 (in binary-weighted form). Oversampled converters are feedback systems that operate with relatively high clock rates, up to 100 times the Nyquist rate or more. The kernel of the oversampled converter is the delta–sigma modulator, described in Section 7, which embeds a quantizer and filter within a feedback loop. The flash or parallel converter, described in Section 4, is perhaps the most straightforward type of Nyquist-rate A/D. A thermometer-coded binary number is generated through approximately 2^N parallel comparisons; conversion to conventional binary code (in addition to error correction) is performed by digital logic. The main advantage of this approach is speed. In Section 4, we present methods to "contain" the high complexity of the flash architecture by invoking pipeline techniques.

Nonidealities, particularly element-size mismatch, can reduce the dynamic range of data converters. Without mismatch compensation techniques (described below), the dynamic range of the converter is limited by the

[1]We define *analog signals* as those with amplitudes that vary over a continuum, for example, signals such as voltage fluctuations induced by electromagnetic or acoustic waves impinging on transducers. Note that analog signals may be either discrete (i.e., sampled) or continuous in time. Digital signals are discrete in both amplitude and time. A system in which both analog and digital signals are used is called a *mixed-signal* system.

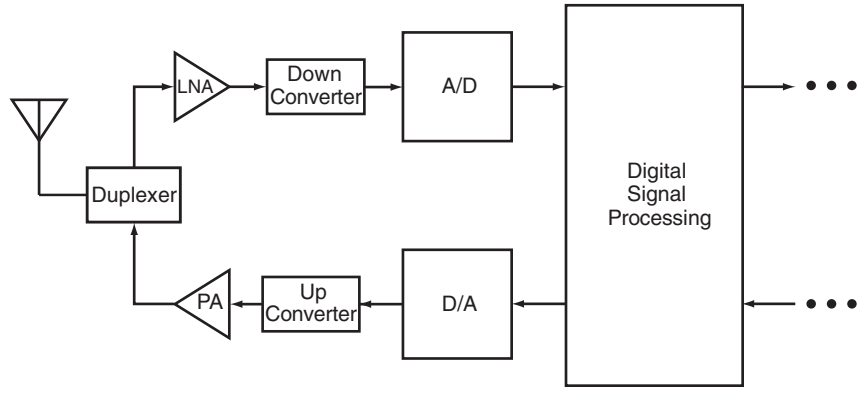

Figure 1. A generic wireless transceiver core for digital communication. The RF front end includes a low-noise amplifier (LNA) for the receiver and a power amplifier (PA) for the transmitter. The data conversion subsystem consists of an analog-to-digital (A/D) converter and a digital-to-analog (D/A) converter.

capabilities of the manufacturing technology, to—in the case of standard CMOS fabrication—approximately 10–12 bits. To see this, note that a D/A converter with N bits of accuracy, by definition, must satisfy

$$\text{Maximum error due to nonidealities} \leq \frac{V_{\text{LSB}}}{V_{\text{ref}}} = \frac{1}{2^N} \quad (1)$$

where the error associated with the converter must be less than the smallest possible change in the output voltage of the converter, defined as V_{LSB} (normalized by the reference voltage). If the D/A has a component mismatch error, which we assume to be the dominant source of error, of 0.1% (the minimum matching precision in standard CMOS [10]), we may write

$$0.001 \leq 2^{-N}$$

$$\Rightarrow \log_2(0.001) \leq -N \log_2(2)$$

$$\Rightarrow N \leq -\log_2(0.001) \approx 10.$$

Therefore, the converter accuracy is limited to approximately 10 bits or 60 dB.

2. DATA CONVERTER FUNDAMENTALS

Data conversion can be viewed as a two-stage process of sampling followed by amplitude quantization, as shown in Fig. 3. In many instances, the sampling operation is implicit in the functioning of the converter. However, it is often helpful to consider sampling as distinct from amplitude quantization, since certain performance degradations can be traced to sampling nonidealities.

In the case of D/A conversion, the sampling operation is simply a resampling and filtering of the digital input signal, which can be realized with digital circuits or software. In the A/D case, sampling is performed by an analog sample-and-hold (sometimes referred to as a "track-and-hold") circuit, as shown in Fig. 4. The design of a suitable sample-and-hold can be challenging. Operating at the sampling rate of the converter, the sample-and-hold circuit must transition from "track" to "hold" mode with a minimum of error and provide an accurate measurement of the analog input with a minimum of signal feedthrough. The reader interested in a more in-depth discussion of sample-and-hold circuits is referred to the book by Johns and Martin [11, Chap. 8]; the remainder of our discussion will focus on the process of amplitude quantization.

The signal band of the data converter is the range of frequencies of width f_b from a minimum frequency (often DC) to a specified maximum frequency. For simplicity we assume throughout this article that the signal band begins at DC, where signals are restricted to the frequency range $[0, f_b]$. Sampling rates for bandlimited analog signals must exceed the Nyquist rate, denoted by $2f_b$, as shown in Fig. 5.

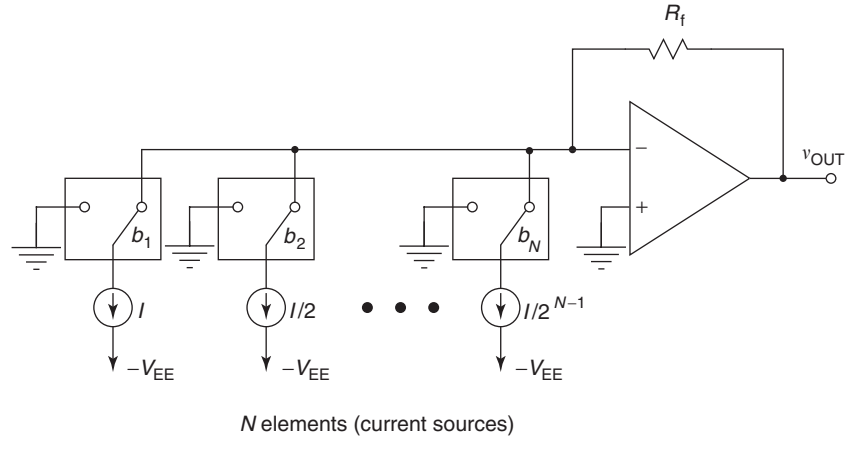

Figure 2. A binary-weighted N-bit Nyquist-rate D/A. Switching elements control current flow through the buffer based on bit values. The analog output voltage is expressed as $v_{\text{out}} = V_{\text{ref}} \Sigma_{i=1}^{N} 2^{-i} b_i$, where $V_{\text{ref}} = 2IR_f$.

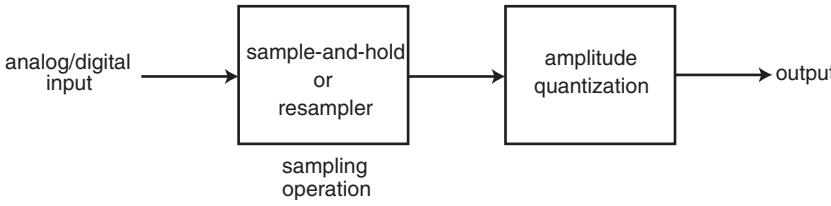

Figure 3. A conceptual view of the data conversion process.

For D/A converters, amplitude quantization can be expressed as a scaling of a digital input by an analog reference quantity. Formally, the amplitude quantization of an N-bit D/A converter (shown in general form in Fig. 6) is expressed as

$$v_{\text{out}} = V_{\text{ref}} \sum_{i=1}^{N} 2^{-i} b_i \tag{2}$$

where b_i are the bits of the input word, $\{b_1, b_2, \ldots, b_N\}$, which may be in either signed or unsigned digital form; b_1 denotes the most significant bit (MSB); and b_N, the least significant bit (LSB). We assume that V_{ref} and v_{out} represent voltages, although other physical quantities (such as current) may be used. In the case of a thermometer code representation, $\{b_1, b_2, \ldots, b_{2^N-1}\}$, of the digital input, we have

$$v_{\text{out}} = \frac{V_{\text{ref}}}{2^N} \sum_{i=1}^{2^N-1} b_i \tag{3}$$

We may provide a similar description for a generalized N-bit A/D converter, shown in Fig. 7. The relationship between analog input v_{in} and output bits is expressed as

$$v_{\text{in}} = V_{\text{ref}} \sum_{i=1}^{N} 2^{-i} b_i + v_{\text{Q}} \tag{4}$$

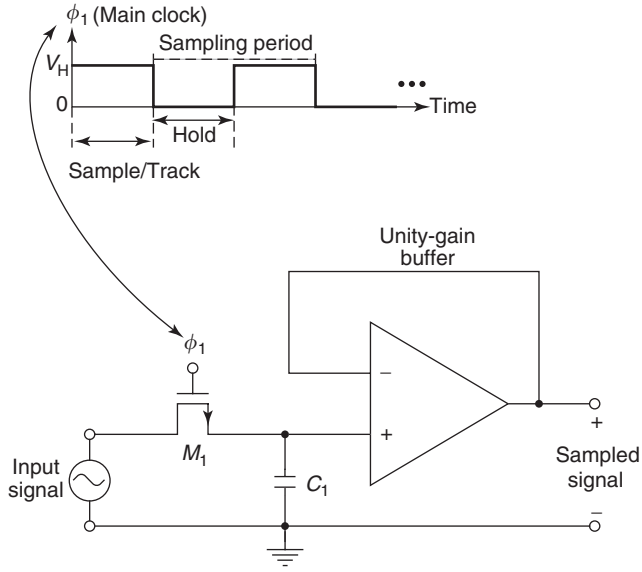

Figure 4. A conceptual sample-and-hold circuit. The sampling rate is set by the frequency of the main clock. During the sample phase, the switch M_1 is on and the capacitor voltage tracks the input signal voltage. During the hold phase, the switch opens and the voltage across C_1 can be read through a unity-gain buffer.

for binary-weighted encoding, or

$$v_{\text{in}} = \frac{V_{\text{ref}}}{2^N} \sum_{i=1}^{2^N-1} b_i + v_{\text{Q}} \tag{5}$$

for thermometer code converters. The variable v_{Q} denotes the quantization error, which we describe in detail below. These equations help us define the "staircase" characteristic that is often seen in A/D converter descriptions (please see Fig. 8). In addition to these equations, the ideal A/D has specific *transition* values for the analog input; Thus the transition points should occur $\frac{1}{2}V_{\text{LSB}}$ away from the midpoints of the staircase characteristic, as shown in Fig. 8. Assuming that v_{in} is within the designated limits of the converter, given by

$$-\frac{V_{\text{ref}}}{2^{N+1}} \le v_{\text{in}} \le \frac{2^{N+1}-1}{2^{N+1}} V_{\text{ref}} \tag{6}$$

[note that the upperbound on v_{in} can be expressed as $V_{\text{ref}} - (V_{\text{LSB}}/2)$], the quantization error should satisfy

$$-\frac{V_{\text{ref}}}{2^{N+1}} \le v_{\text{Q}} \le \frac{V_{\text{ref}}}{2^{N+1}} \tag{7}$$

For dynamic measurements of converter performance, quantization error is often modeled as a uniformly distributed (zero-mean) uncorrelated random variable. Based on (7), the variance (i.e., power) of the quantization error is $V_{\text{LSB}}^2/12$. We can now derive the relationship between signal-to-quantization-noise ratio (SQNR) and N, the number of bits associated with an A/D converter. We assume that v_{in} is a sinusoidal input (commonly used for testing purposes) with amplitude that varies between 0 and V_{ref} [approximately within the bounds indicated by (6)]. We obtain the peak SQNR in units of dB as follows:

$$\begin{aligned}
\text{SQNR} &= 10 \log_{10} \left(\frac{\text{power of sinusoidal input}}{\text{power of quantization error}} \right) \\
&= 10 \log_{10} \left(\frac{\frac{V_{\text{ref}}^2}{8}}{\frac{V_{\text{LSB}}^2}{12}} \right) \\
&= 10 \log_{10} \left(\left(\frac{3}{2} \right) 2^{2N} \right) \\
&\approx 6.02N + 1.76
\end{aligned}$$

Thus we find that the resolution or peak SQNR of an N-bit converter is approximately $6N$ dB; therefore, we often say that 1 bit is equivalent to 6 dB.

The *signal-to-noise-and-distortion ratio* (SNDR) of a data converter is defined as the ratio of the signal power to the signal-band noise and distortion power measured at

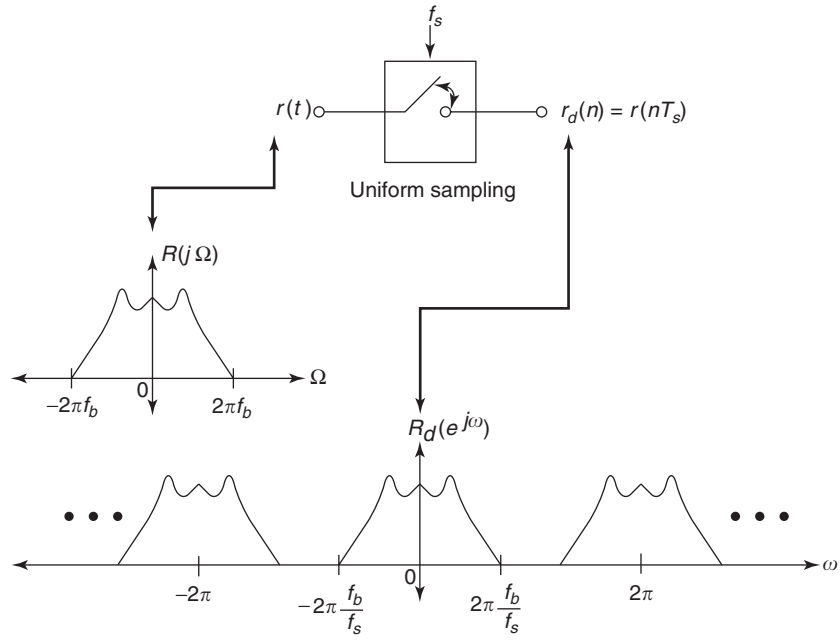

Figure 5. An illustration of Shannon's sampling theorem. The bandlimited analog input signal r is sampled uniformly in time at a sampling rate f_s [note that the sampling interval is given by $T_s = (1/f_s)$]. In the figure, the quantity Ω refers to frequency f in radians per second (i.e., $\Omega = 2\pi f$); the quantity ω is normalized frequency [i.e., $\omega = 2\pi(f/f_s)$] in radians per second. The sampled spectrum $R_d(e^{j\omega})$ consists of copies of the original spectrum $R(j\Omega)$ centered at integer multiples of the sampling frequency. To avoid aliasing (i.e., overlap and superposition of the copies), it is sufficient for f_s to exceed $2f_b$. Note that a generalized sampling theorem exists for bandpass signals that can reduce sampling rate requirements in many applications [12].

the output of the converter. *Noise* includes quantization error, modeled as a random process, and uncorrelated noise arising from circuit components. *Distortion* refers to signals that correlate with the input signal that are often harmonically related to frequency components of the input. The *signal-to-noise ratio* (SNR) is similar to the SNDR, but distortion frequency components are ignored in the calculation.

The DR of a data converter, obtained as illustrated in Fig. 9, is the ratio of the power level of the largest allowable input signal to the power level of the input signal corresponding to an SNDR of unity. The "largest allowable input signal" is the input signal that yields a specified drop in SNDR (sometimes 3 dB [13]) beyond the maximum SNDR. Dynamic range, SNDR, and SNR/SQNR are often expressed in units of bits (where, as mentioned above, 1 bit is equivalent to 6 dB). The *effective number of bits* (ENoB) is usually obtained by dividing the DR (in dB) by 6 dB/bit and provides a measure of the true accuracy of the converter. For example, a 16-bit converter with a dynamic range of 72 dB is accurate to only 12 bits, and, therefore, has an ENOB of 12.

2.1. Nonidealities

Practical data converters typically fall short of ideal performance (specified, e.g., in terms of SNDR or DR). As mentioned, performance flaws can often be traced to mismatches between constituent elements. For example, in the binary-weighted D/A of Fig. 2, each current source must be exactly one-half the size of the next-larger current source in order to achieve an ideal characteristic. Any error in sizing results in a corresponding deviation of the converter characteristic from ideal. The precision with which these elements can be sized depends on the manufacturing technology.

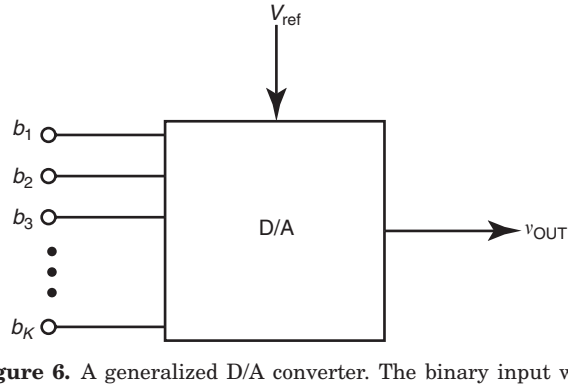

Figure 6. A generalized D/A converter. The binary input word $\{b_1, b_2, \ldots, b_K\}$ describes a conventional (signed or unsigned) code ($K = N$) or a thermometer code ($K = 2^N - 1$).

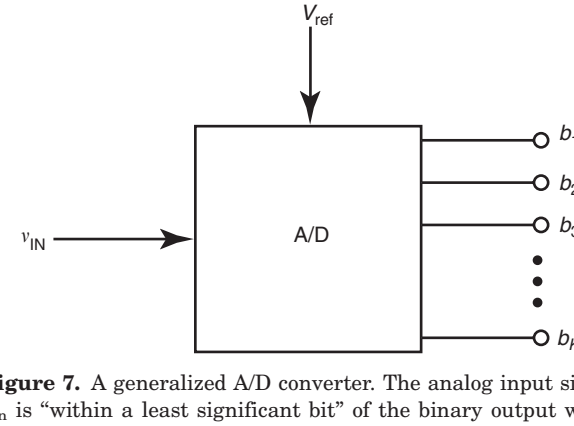

Figure 7. A generalized A/D converter. The analog input signal v_{in} is "within a least significant bit" of the binary output word, $\{b_1, b_2, \ldots, b_K\}$. For conventional (signed or unsigned) codes, $K = N$, and for thermometer codes, $K = 2^N - 1$.

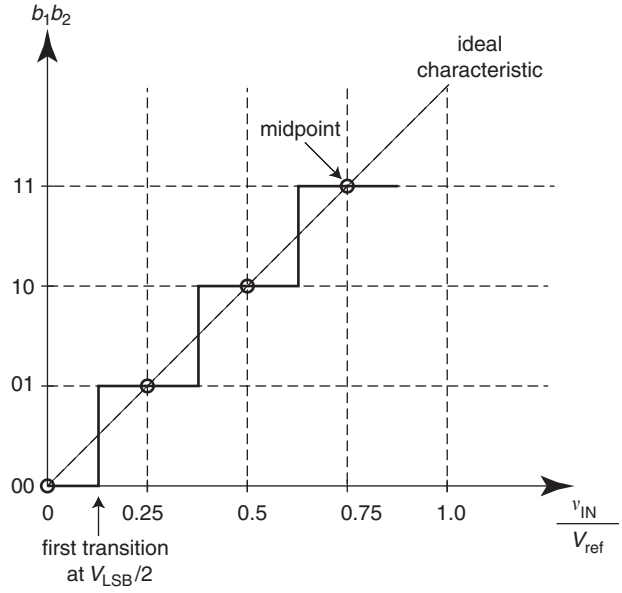

Figure 8. Ideal A/D staircase characteristic (shown here for a 2-bit converter), shown for positive values of v_{in} only. The midpoints of each output are indicated; transitions occur at analog input amplitudes $V_{LSB/2}$ away from the midpoints.

In Fig. 10, we superimpose the ideal and actual (D/A) characteristics to illustrate the various nonidealities that can be observed. For D/A converters, *offset error* is measured as the output corresponding to a zero input (i.e., the input defined by setting all bits to zero), often normalized

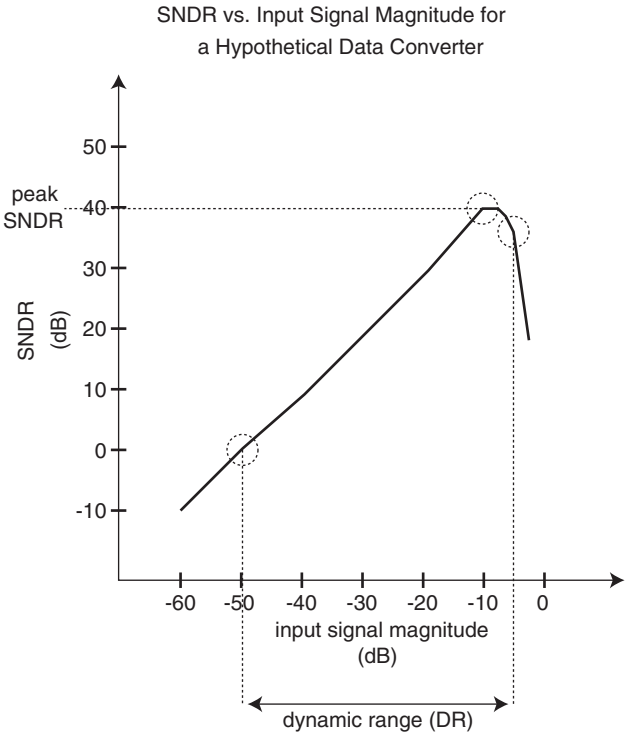

Figure 9. Illustration of SNDR variation with input signal magnitude for a hypothetical data converter. The peak SNDR and DR are indicated on the plot.

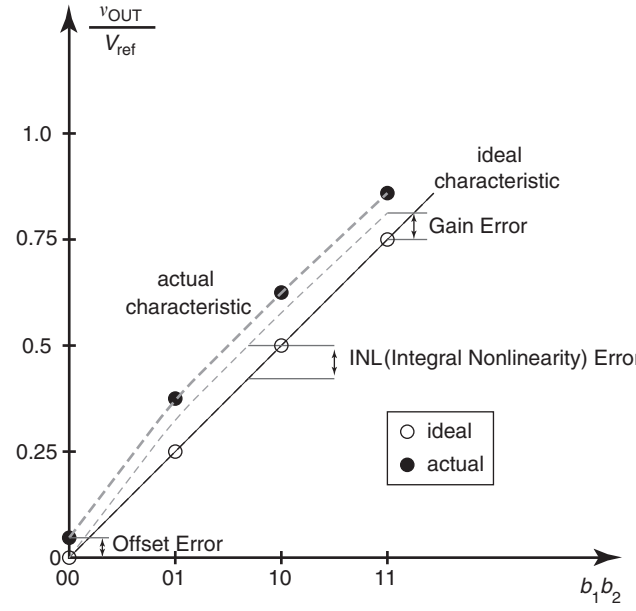

Figure 10. Plot of a 2-bit D/A converter characteristic. Deviations of the actual characteristic from ideal behavior are characterized using a variety of static metrics including offset, gain, and integral nonlinearity errors. Note that the offset error is typically removed before gain and nonlinearity errors are measured.

by V_{LSB}. To find the offset error for A/Ds, we measure the deviation of the lowest transition voltage of the input away from $V_{LSB/2}$. The notion of *gain error* is the endpoint difference between two straight lines (with offset error removed), as illustrated in Fig. 10; one line is defined by the ideal characteristic (for either A/D or D/A converters), and the second line has a slope computed using the extremes of zero and "full-scale" inputs.

Nonlinearity is characterized as either *differential* or *integral*, and is computed after offset error is removed. For D/A converters, differential nonlinearity (often abbreviated as DNL) is given by the difference between the largest step (between two adjacent binary input codes) and V_{LSB}; integral nonlinearity (often abbreviated as INL) is the largest deviation of the actual characteristic from a straight line drawn between the endpoints of the characteristic [1]. Differential and integral non-linearities are calculated in much the same way for A/D converters. Differential nonlinearity is the difference between the largest increase in the analog input needed to generate a transition between consecutive digital output codes and V_{LSB}. Integral nonlinearity is largest difference between the actual A/D characteristic and the straight line formed by joining the endpoints of the actual characteristic.

3. OVERVIEW OF D/A CONVERTER ARCHITECTURES

The digital-to-analog (D/A) converter is one of the basic building blocks of most analog/digital interface systems. For example, in audio-CD players and music synthesizers, D/A converters with accuracy as high as 16–24 bits are desired for speeds in the range of few kilohertz.

Telecommunication applications like radio transmitters require D/A converters (DACs) operating at hundreds of MHz for resolutions in the range of 10–15 bits.

There are several architectures for D/A converters depending on the speed, resolution, complexity, and area requirement [14]. In this section, we will focus on one particular type of D/A converter commonly known as a *current steering array*, which offers high-speed D/A conversion using current as a *unit* element for analog computation of digital input. Other formats such as switched-capacitor architectures or resistor ladder architectures are also used for D/A conversion. In switched-capacitor D/A converters, charge across unit capacitors is used as the *unit* for analog computation instead of current. Such architectures are popular in the design of a coarse D/A converters, also called *multiplying D/A converters* (MDACs) in pipelined A/D converters. Such architectures are introduced in another section on pipelined converters. A resistor ladder architecture uses voltage drop across the *unit* resistors as a basic *unit* for analog computation. More information about resistor ladder DACs and switched capacitor DACs can be found in the literature [1,11,14].

For most applications, the main performance measure for a D/A converter is its spurious-free dynamic range (SFDR). The SFDR measures the ability of the D/A converter to suppress the spurious harmonic tones generated as a result of circuit and system nonidealities. In case of current-steering D/A converters, the SFDR is limited by the matching of the unit current sources. Higher dynamic range is usually achieved through the use of dynamic element matching techniques discussed in brief toward the end of this section. There are three types of current steering D/A converters: binary-coded current steering DACs, thermometer-coded current steering DACs, and segmented current steering DACs. A conceptual binary-coded current steering DACs is shown in Fig. 2.

The binary DACs are not popular for high-resolution applications. This is because of the nonmonotonicity introduced due to current mismatch and momentary glitches during code transitions. Nonmonotonicity occurs because the amount of mismatch introduced by switching in of a new set of current sources for one LSB increase in the input is greater than one LSB with an opposite sign. This causes the output to be nonmonotonic for increasing input. Glitches are another source of dynamic errors and are usually dominant during the worst-case code transition when input changes from 011 $\cdots$1 to 100$\cdots$0. Because of finite delay in the ON time of the switches and mismatch therein, the MSB switch may turn on before (MSB goes from 0 to 1) the LSB switches (LSBs go from 1 to 0), causing a momentary output of all 1 s. This glitch is equal to half the full scale and lasts as long as the delay mismatch between the MSB and the LSB switches. Such glitches are unacceptable for high-performance D/A converters since they affect the SFDR of the D/A converter.

The thermometer-coded D/A converter does not have the limitations described above. In a thermometer code D/A converter, all the current sources are of unit value, and are controlled by a monotonic thermometer code. A binary to thermometer digital logic is used to generate a thermometer code. Since an LSB increase in the digital input corresponds to a simple addition of another unit current source to the output, the monotonicity is guaranteed. Moreover, the glitch is completely eliminated as just one current source is switched on or off for one LSB change in the input. However, the main problem in a thermometer-decoded D/A converter is the complexity in the layout that is needed in generating a thermometer code for high-resolution binary input. Moreover the number of unit current sources to be individually controlled by the thermometer code increases exponentially. In most implementations, a combination of binary-coded D/A converters and a thermometer-coded D/A converter is used. An example for a $(M+K)$-bit D/A converter is shown in the Fig. 11. Such converters are called segmented current steering DACs. A careful RAM-like physical layout usually achieves compact implementation of the thermometer-coded array. A segmented array offers a compromise between the complexity of layout for a thermometer-coded array and the amount of manageable glitch area from a binary-coded array.

In all the current steering D/A converters, the mismatch in the current sources introduces a systematic error wherein, for the same input, the error introduced is

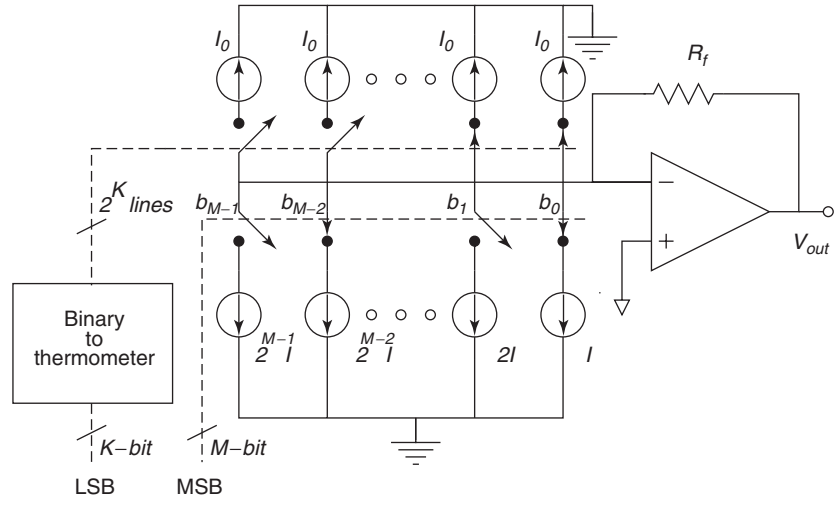

Figure 11. A popular segmented current steering D/A converter for $(N=M+K)$-bit resolution. I is the unit current source, and currents are thermometer coded for the K most significant bits. The remaining M bits are implemented through a binary-weighted current steering D/A converter. The value of the unit current source in the binary-coded array is $I=2^K I_0$, where I_0 is the unit current source for a thermometer array.

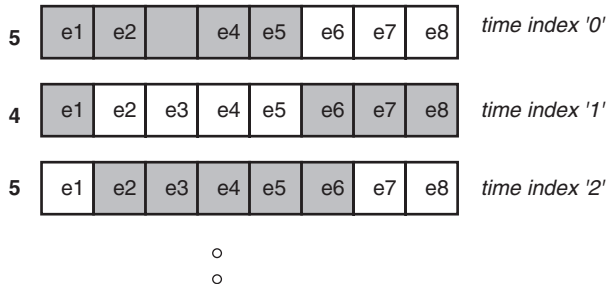

Figure 12. Data-weighted averaging illustrated for a 3-bit converter having eight unit current sources. The shaded squares correspond to the current sources chosen to generate the analog current-domain output. At time index 0, an input of 5 generates an output with a total mismatch error of $e_1+e_2+e_3+e_4+e_5$. At time index 1, the next four current sources (modulus 8) are chosen to generate an output with total mismatch error of $e_6+e_7+e_8+e_1$. The next occurrence of 5 generates an output with total error of $e_2+e_3+e_4+e_5+e_6$, which is different from the previous occurrence of 5. A simple rotation scheme like this provides dynamic element matching through first-order shaping of the mismatch induced noise.

always the same because the same current sources are used in generating the output. Such systematic error introduces pattern noise in the form of spurious tones that appear as harmonics of the input signal frequency. Since harmonics are most undesirable in telecommunications and audio applications, techniques are needed to alleviate this problem. A dynamic element matching (DEM) techniques provide one such solution. Various DEM algorithms have been proposed in the literature offering different flavors, but their end goal is the same [14–17]. The main purpose of the DEM algorithm is to provide either random scrambling or permutation of the current sources such that the amount of error introduced by the D/A converter is not the same for the same input applied at two different time instants. This removes the systematic nature of the error signal and thus alleviate the problem of harmonics. However, depending on the schemes used, the harmonics either move at higher frequency or cause an increase in the noise floor (which can be tolerated in audio and telecommunication applications). A data-weighted averaging (DWA) technique proposed by Redman-White [14] is shown in Fig. 12. The technique provides first-order shaping of mismatch induced noise. However this technique still carries harmonics at higher frequency. Many variants of this technique have been suggested in the literature to avoid such tones [14,17].

4. OVERVIEW OF HIGH-SPEED A/D CONVERTER ARCHITECTURES

This section reviews the existing data converter architectures suitable for high-speed applications, with more emphasis on the analog-to-digital (A/D) converter design. A brief overview of digital-to-analog (D/A) converters is also provided for completeness. The architectures for the A/D converter discussed below are "flash," "two-step," "interpolation," "folding," and "multistage" A/D converters. All the architectures discussed in this section pertain to single-channel ADC implementation. Time interleaved ADC perform parallel A/D conversion with a number of single-channel ADCs connected in parallel, offering high speed for a given resolution. However this is achieved at the cost of higher power consumption and increased area. Design issues related to time-interleaved A/D converters is discussed in detail in the literature [18], and is not discussed here. For communication applications, a behavioral survey and analysis of the A/D converters can also be found [19].

4.1. Flash Converters

Flash A/D converters are potentially the fastest ADCs and relatively easy to design compared to other architectures. Figure 13 shows the block diagram of a simple flash ADC. For an N-bit resolution, flash ADC consists of a resistor ladder that subdivides the main reference voltage into 2^N equally spaced voltage levels, and the 2^N-1 comparators to compare the input signal against these voltage levels. The output of a flash ADC is a thermometer code that is then passed on to the encoder to generate the binary output. Comparators usually consists of a moderate-gain preamplifiers followed by a regenerative-type latch to achieve high speeds. A sample comparator circuit is shown in Fig. 14. Transistors M_1 and M_2 along with the diode connected load form the input preamplifier. The preamplifier amplifies the difference between the input V_{in} and the

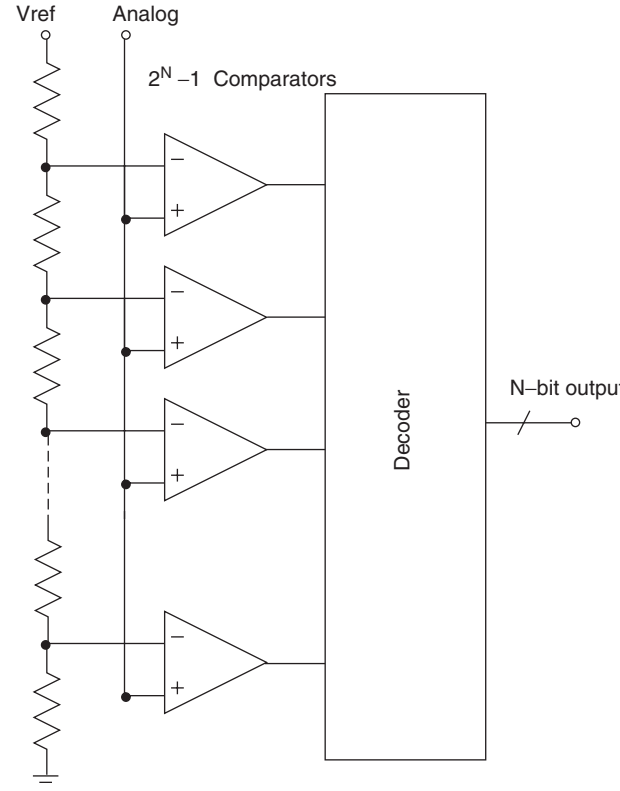

Figure 13. Conceptual flash A/D converter for an N-bit resolution.

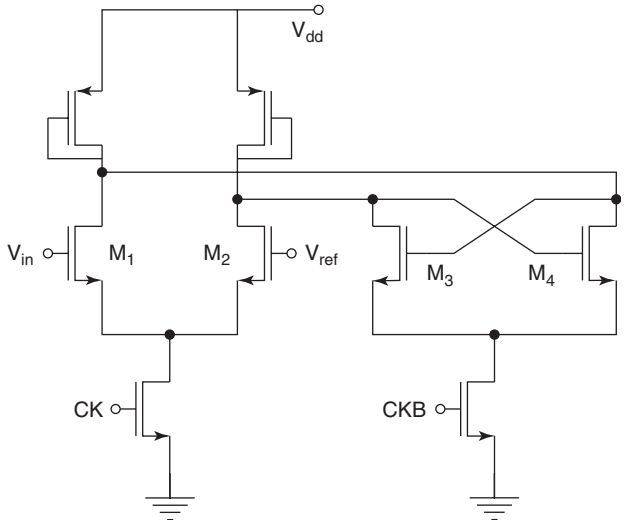

Figure 14. A simple comparator schematic: M_1–M_2 form the input differential pair for preamplification. Transistors M_3–M_4 form a positive-feedback latch for regeneration. CKB is opposite in phase to CK.

reference V_{ref} during clock phase CLK. This amplified difference is regenerated by the positive-feedback latch formed by transistors M_3 and M_4, during clock phase CLKB. More comparator architectures can be found in the literature [1,11,18,20]. Flash ADC essentially performs distributed, parallel processing of the input signal, with no potential need for an explicit front-end sample-and-hold amplifier (SHA), resulting in the highest speeds among the data converter architectures. However, the number of components (e.g., resistors and comparators) increase exponentially with the overall resolution N of the converter. Also, higher resolutions are difficult to achieve from flash ADC because of various static and dynamic nonlinearities.

The main source of static nonlinearity in flash ADC appears from the offsets in the comparators and the resistor mismatch in the reference ladder. Input device transistors having large area is therefore needed to reduce the amount of offset, at the cost of increased nonlinear input capacitance. Large input capacitance at the input of the flash ADC also increases the load on the buffer driving the ADC, increasing its power consumption. Apart from large die-size and increased power consumption, flash ADCs also suffer from various issues such as metastability, kickback noise, slew-dependent sampling point, and clock jitter [1]. Metastability arises when the input to the flash A/D converter is very close to one of the comparator thresholds, which results in long settling times to regenerate the outputs to logic levels. This causes indeterminate latch outputs that are decoded incorrectly to give erroneous digital outputs. Metastability can be removed through gray coding as an intermediate step between the thermometer and binary codes [1]. Sparkles are also a source of static nonlinearity that arise directly from resistor mismatch and comparator offsets. Sparkles are caused when the comparator gives an *out-of-sequence* zero instead of a one due to these offsets. It is also caused by mismatch in the sampling instants of the preamplifiers in the comparator array. Such sparkles can also be caused by slew-dependent sampling points. This occurs for rapidly varying input signals due to finite time between the tracking and the latching phase for certain implementations of the comparator. The rapidly varying input signal at the preamplifier input can cause the comparator to change its decision erroneously during the finite time between the latch phase and track phase. Such sparkles are removed through *bubble correction* in the thermometer to binary encoder. However, *bubble correction* can detect and correct for only a limited number of occurrences of sparkles. Gray-coding provides a soft degradation in performance for increasing number sparkles in the thermometer code and is therefore used in most flash A/D converter implementations. The slew-dependent sampling point and clock jitter can be minimized through the use of a dedicated sample and hold in front of the flash ADC at the expense of more power and area.

Two-step converter architectures trade speed for lower power consumption, small real estate, and lower input capacitance. Alternate architectures such as interpolation and folding maintain the one-step distributed nature of flash A/D conversion, and reduce the power consumption and real estate requirement of the pure flash ADC by reducing the number of preamplifiers and the latches needed in the implementation. Interpolation and averaging have also been shown to improve the differential nonlinearity performance (DNL) of the ADC [1,18].

4.2. Two-Step Converters

Figure 15 shows a two-step ADC architecture that has relatively small die size and low power consumption compared to flash ADCs. In a two-step ADC, the coarse flash A/D converter produces the most significant bit (MSB) decisions and the fine-flash ADC produces the least significant bit (LSB) decisions. The coarse D/A converter generates the coarse analog estimate of the input that has been resolved by the coarse A/D converter. This estimate is then subtracted from the input to generate the residue to be processed by the fine-flash ADC. The residue of the first stage is same as the quantization noise of the first stage, which indicates the portion of the input that is not resolved by the coarse A/D converter. The digital output of the coarse and fine ADC can be added appropriately to give the final ADC output.

Comparing the number of comparators needed in the two-step architecture versus the flash architecture, we can see that significant area savings can be achieved. An 8-bit flash ADC will require 256 comparators, whereas a two-step ADC, with a 4-bit MSB stage and a 4-bit LSB stage, will need only 32 comparators, which is a significant savings in the area. However, the speed of the two-step converter is less than that of a pure flash A/D converter, due to additional delays introduced by the D/A converter and the subtractor. The throughput of the two-step can be made comparable to the flash A/D converter, by adding a sample and hold between the two stages for pipelining. Pipelining can be extended to more than two stages and is covered in detail in a section on multi-stage converters.

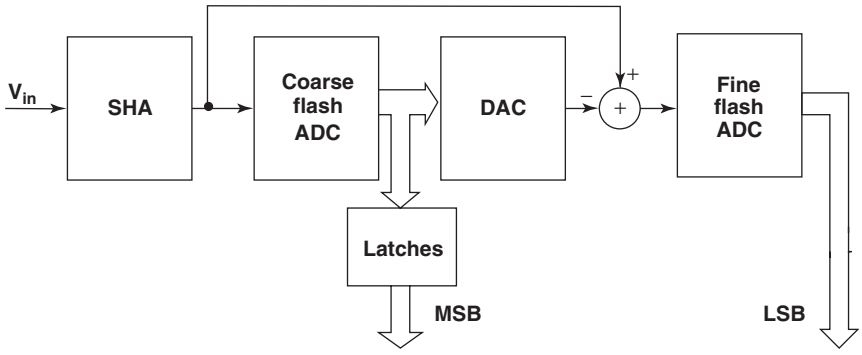

Figure 15. Conceptual schematic of a two-step A/D converter.

A main problem with the two step converter shown in Fig. 15 is that the residue generated for the fine–flash ADC is much smaller in magnitude, requiring that the coarse D/A converter and the subtracter be accurate to the overall resolution of the converter. To solve this problem, the residue output can be first passed through an interstage gain amplifier with a value of 2^M, where M is the resolution of the MSB stage, so as to make the signal swings same for both the coarse and fine ADCs. This also relaxes the offset requirement for the comparator of the fine-flash ADC. As in pipelined converter, if digital error correction is used, the accuracy requirements of the coarse A/D converter is greatly relaxed too. Some implementations of the two-step architecture can be found in the literature [21–23].

4.3. Interpolation-Based Flash Architectures

To reduce the input capacitance, power dissipation, and large area required from flash A/D converters, interpolation can be used. The main idea behind interpolation is to use the linear region of the adjacent preamplifiers to generate additional thresholds for comparison, and hence reduce the number of preamplifiers needed for a given resolution [1,11,18,20].

In flash converters, the linearity of the preamplifier in the comparator is a nonissue, since only the sign of the amplifier outputs is needed for making a decision. However, in case of interpolating flash A/D converters, the linearity of the preamplifiers is needed at least over a small range of the input signal. The overall one-step nature of the flash conversion is still maintained in the interpolating flash A/D converters. Figure 16 shows the basic architecture for interpolation in flash A/D converters for a case of interpolation by 2. For this example, an additional output is generated as an average of the two adjacent preamplifier outputs using a resistor or capacitive dividers as shown in the figure. Since, the additional output resembles a preamplifier output for the threshold at the midpoint of the adjacent comparator thresholds, the number

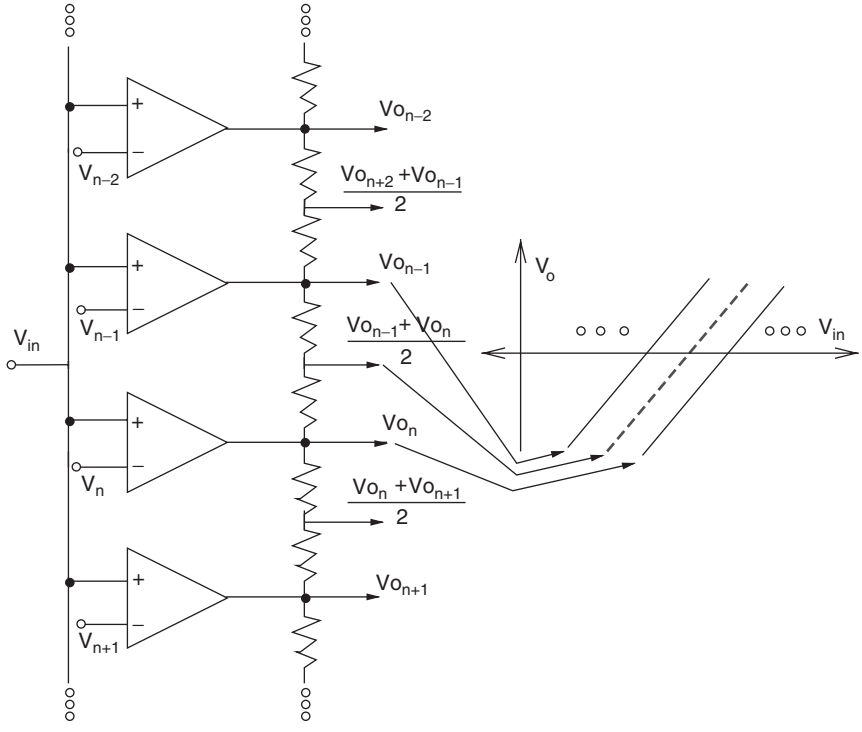

Figure 16. Conceptual schematic of an interpolating A/D converter using resistors. The interpolation is by 2. The dotted line indicates the interpolated waveform generated from the adjacent preamplifier outputs. The outputs V_{o_i} feed the latch to regenerate to logic levels (latch not shown).

of preamplifiers has been reduced by 2 for this flash A/D converter for the given resolution. Thus a reduction in the number of preamplifiers is achieved for a given resolution by interpolation. But the overall number of latches required is still the same as in a pure flash A/D converter. To further reduce component count and power consumption, interpolation is generally used alongside *folding* to enable further area and power savings [24]. Folding will be discussed in detail in the next section. Interpolation can also be pipelined to offset the lower speed and bandwidth attributed to resistive loads, to increase throughput [25].

Interpolation indicates that effective resolution of the flash A/D converter can be increased by interpolating between the outputs of the adjacent preamplifiers. An interesting property of the interpolation is that it improves the differential nonlinearity of the original flash converter. This is evident in Fig. 16, which shows that the effective interpolated reference threshold (level) generated lies between the thresholds of the adjacent preamplifiers, which guarantees that the differential nonlinearity for the interpolated threshold is bounded and is less than that of its pure flash counterpart. The reduction in DNL increases with the factor of interpolation. Since the accuracy of the interpolation depends on the linearity of the preamplifiers, a wider range between the preamplifiers would be required for a higher interpolation factor. Any nonlinearity when interpolating between preamplifiers not in the linear region, can cause deviation of the interpolated threshold from it's ideal value or even a deadband around the interpolated threshold. The main problems of interpolation are the added time constants introduced by the interpolation resistors and capacitances from the following latches, sacrificing speed of conversion. The reduction in bandwidth scales approximately with the square of the interpolation factor, thereby making interpolation not feasible for factor exceeding 4. A conceptual schematic of a folding ADC is illustrated in Fig. 17.

4.4. Folding A/D Converters

In folding A/D converter (shown in Fig. 17), the speed tradeoff of the two-step converter is mitigated by generating the residue for the fine flash ADC of Fig. 15 in parallel using a separate analog preprocessor and is generated independent of the coarse MSB flash stage [1,11,26]. This eliminates the need for the D/A converter and a subtracter, resulting in power savings and reduced delay. The analog pre-processor uses a technique called "folding" to generate the residue independent of the MSB decisions. A simple voltage mode differential folding circuit for a folding factor of 4 is shown in Fig. 18. A folding factor is defined as the number of times the output changes sign (or direction) as the input V_{in} varies over its input range. The input–output characteristic of the folding circuit is also shown in Fig. 18. The ideal expected folder waveform is shown by the triangular dotted line. This is related to the sawtoothlike residue output of the first stage in the two-step ADC through simple reversal of signs and level shift operations. Hence, the folder output waveform can be used by the fine-flash stage instead of the sawtoothlike ideal residue output to generate LSBs. The operation of the circuit in Fig. 18 is given below. When the input is below V_{r1}, transistors M_1, M_3, M_5, and M_7 are off and M_2, M_4, M_6, and M_8 are on. A total of $2I_b$ flows through R_1 and $3I_b$ flows through R_2, pulling down voltage at node OUT$-$ by I_bR below the voltage at node OUT$+$. When input is equal to V_{r1}, equal currents $I_b/2$ flow through transistors M_1 and M_2. However, transistors M_3, M_5, and M_7 are still off and M_4, M_6, and M_8 are still on. This, in essence, steers current $I_b/2$ from resistor R_2 to R_1, causing equal currents of $2.5I_b$ to flow through both resistors and voltages at the node OUT $+$ and OUT$-$ are equal. As input is increased from V_{r1}, but maintained less V_{r2}, M_1 turns on and M_2 turns off. A total of $3I_b$ current now flows through R_1 and $2I_b$ flows through R_2. This causes node OUT$+$ to be I_bR lower than the node OUT$-$. As input approaches V_{r2}, M_3 begins to turn on and M_4 begins to turn off, causing the current to steer from R_1 to R_2, and the output at node OUT$+$ and OUT$-$ changes direction. The circuit behaves in a similar manner as V_{in} is increased further. The number of times the output slope changes sign is equivalent to the number of times, the excess current steers between R_1 and R_2. This number is also equal to the folding factor of the ADC.

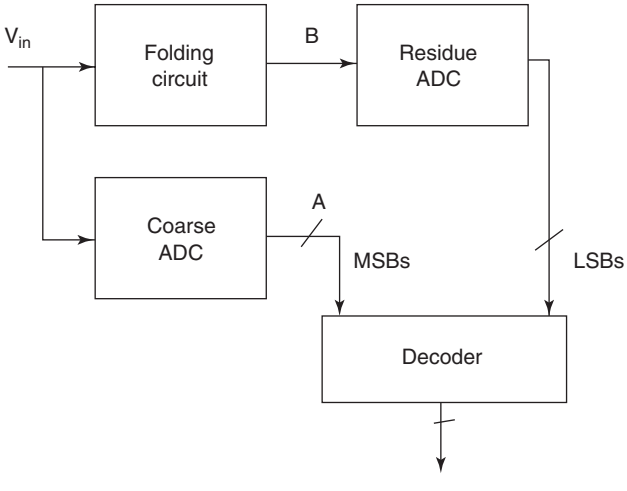

Figure 17. Conceptual schematic of a folding A/D converter.

It is to be noted for best performance, the folding circuit should have exactly one differential pair switch for any given input voltage, which mandates that the reference levels should be spaced far apart. However, this will cause saturation of the outputs for inputs closer to the midpoint of the two reference levels and none of the differential pairs would switch, resulting in deadband and inaccurate folder output around this input region. The main advantage of folding is that it maintains the one-step operation of flash, and does not need a subtractor and interstage D/A converter as in two-step converter, potentially achieving high speeds. Even though the sample-and-hold amplifier is not ideally needed for the folding A/D converter, it is used nevertheless to avoid input dependent errors resulting from clock skew and jitter. Inspite of speed improvements, folding suffers from a few drawbacks. One of them is the increased frequency specifications for the design of the folding circuit. If a ramp input varying from 0 to full scale is applied to the folder with folding factor n, the output of the folder will change from V_{min} to V_{max}, n times.

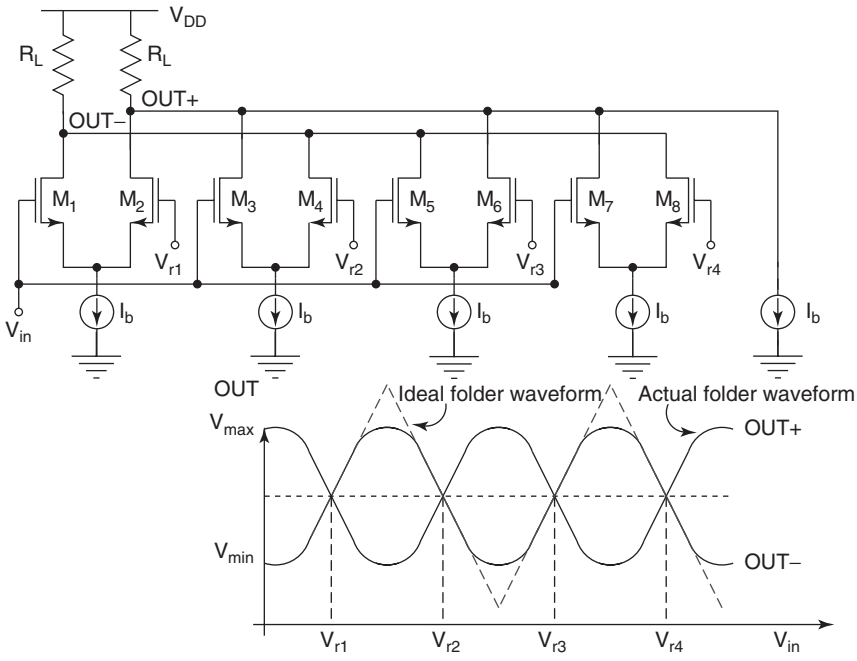

Figure 18. Differential folding circuit that has a folding factor of 4. The folder output feeds the latches that regenerate its output to logic levels. In case of folding and interpolating ADC, the outputs of the folder may be averaged by a resistor network.

This effect results in frequency multiplication by n. Hence the bandwidth and slewing requirements for the folder is n times the maximum allowable input frequency. Therefore, folding with a high folding factor is not effective at high operating frequencies. Another drawback of the folding is substantial nonlinearity in the folder waveform. Comparing the ideal dotted waveform and the actual waveform in Fig. 18, it can be seen that the output of the folder is grossly inaccurate toward the peaks $V_{\max}$ and $V_{\min}$. The effect is similar to residue errors in a two-step converter or a pipelined converter which cause integral nonlinearity or differential nonlinearity. To alleviate this problem, double folding can be used, where the folding waveform is replicated with an additional shift of half the distance between the two reference levels. This ensures that in the region where one of the folders exhibit nonlinearity due to rounding effect, the other folder exhibits high linearity. Then depending on the input level an appropriate folder can be chosen.

The other main drawback of the folding architecture is the need for synchronization in absence of sample-and-holds between the MSB output and the output of the fine stage following the folder. Furthermore, any offset in the MSB stage may result in gross overall error with the magnitude as high as half of the full scale. Folding is usually used along with interpolation to further alleviate the linearity requirement of the folder and for obvious area savings due to reduced number of preamplifiers [1,24]. When interpolation is used between folder outputs for additional comparison thresholds, the nonlinearity of the folder output waveform does not directly affect the overall linearity and resolution of the converter, since the A/D converter extracts all its information from the location of the comparison thresholds (or zero crossings) and not from the amplitude of the folding waveform. However, this does not imply that the folder waveform can be nonlinear, since the accuracy of the comparison thresholds generated after interpolation depends on the linearity of the individual folder waveforms over a large input range. The folding operation can also be pipelined to increase throughput and relax design requirements on the individual folders [6,27].

4.5. Multistage Converters

A multistage converter is a natural extension of the two-step converter discussed in Section 4.2, where more than two stages are used for digitization [1,11,18,28,29]. The second stage in the two-step ADC will also now consist of a sub-D/A converter and subtractor to generate a residue output that can be further digitized by the following stages that may appear identical to the first two stages. Use of an interstage gain amplifier relaxes the resolution requirement of the D/A converter and subtracter and also enables the use of the same flash ADC for all its stages. The bandwidth and the gain of the amplifier used in the MDAC is limited by the op-amp (operational amplifier) settling time, which depends on the speed and resolution specifications of the overall ADC. For an A/D converter without calibration, the finite op-amp gain needed is usually of the order of 2^{M+1}, where M is the number of remaining bits resolved by the following stages in the ADC. The overall speed of the multistage ADC reduces the conversion rate by the number of stages in the ADC, for the same reasons as in a two-step converter. This also puts stringent requirement on the timing skew for the subtractors for each stage. To alleviate this problem, a sample-and-hold amplifier is added at every stage to hold the amplified residue before passing on to the next stage [1,30]. This also increases the overall throughput of the system; the speed is limited by the delay of only one stage. Such an ADC is also called “pipelined” ADC because of the inherent concurrency of the operations. The pipelined converter is discussed in greater detail in the following section.

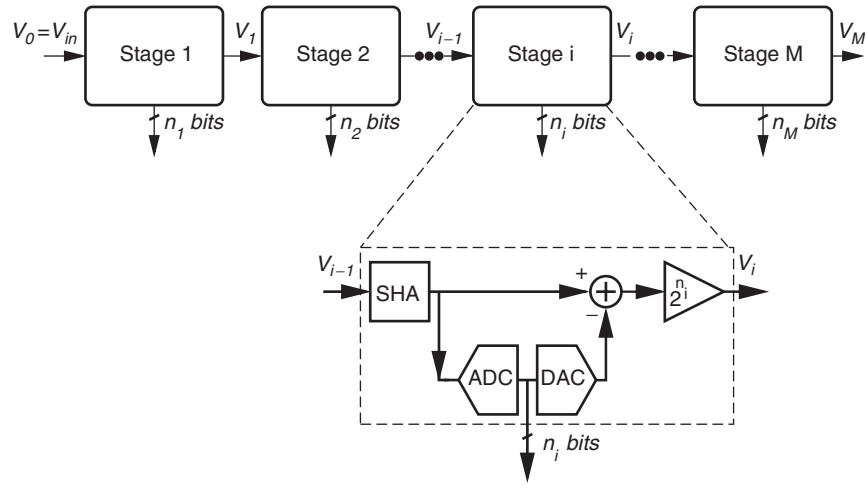

Figure 19. A generic block diagram of a pipelined ADC.

4.6. Pipelined Analog-to-Digital Converters

Pipelined A/D converters (ADCs) are multistage converters that use interstage sample-and-hold amplifiers to enable pipelining and concurrent processing of the input signal [1,18,31–33]. The residue output of one stage is kept on hold and the pipeline stage is not tied up for the fine LSB decisions to be carried out by the following stages. On the contrary, it can sample the next input data for conversion, while the previously held residue signal in the subsequent stage is digitized to make the LSB decisions. Thus pipelined A/D converters behave in concurrent manner and the overall data rate becomes independent of the number of stages. The overall speed is limited only by the speed of one pipeline stage, and therefore a pipelined converter can achieve close to the speeds achieved by flash ADC. Also, the complexity of the pipelined converter ideally scales linearly with the resolution desired, compared to flash which is exponentially related to the desired resolution. This is really beneficial for ADCs with resolutions greater than 8 bits at higher speeds.

5. BASIC PRINCIPLES OF PIPELINED A/D CONVERSION

A simplified block diagram of a multibit per stage pipelined ADC is shown in the Fig. 19. Each stage i resolves its input (or in other words, quantizes its input) into n_i bits of digital output using a coarse ADC (typically a flash-type converter) and then uses a coarse DAC, a subtracter, and an interstage gain amplifier of gain 2^{n_i} to amplify the unresolved input which we had defined as the residue. The operation of D/A conversion, subtraction, and amplification is designated as a MDAC (multiplying D/A conversion) operation. In switched-capacitor implementation, each stage has two nonoverlapping phases of operation: The sampling phase and the MDAC phase. During sampling phase, the residue output of the previous stage (or input if the stage in the first stage in the pipeline) is sampled and held later for subtraction. During this phase, a coarse decision is also made. During the MDAC phase, the MDAC operation is carried out. This is the time when the sampler of the following stage will be active. The waveform for consecutive pipeline stages is shown in Fig. 20.

When stage 1 is sampling input sample for time index n, stage 2 is performing MDAC operation over the residue output of stage 1 corresponding to sample $n-1$, and stage 3 is sampling this residue output corresponding to sample $n-1$, and so on. A pipelined converter therefore exhibits a concurrent nature of processing of input, enabling high-speed operation. As mentioned earlier, the complexity of the pipeline, measured in the number of stages, scales linearly with the desired resolution and therefore pipelined A/D converters show substantial power and area savings for high-resolution applications at high speed.

In the pipeline architecture, as in all multistage ADC, the most significant bits are resolved by the stages earlier in the pipeline and the least significant bits are resolved later in the pipeline. A simple example for a pipeline would be a 1-bit per stage architecture ($n_i = 1$). Each stage of such a pipeline will consist of a simple 1-bit comparator as a coarse ADC, a multiply-by-2 DAC (MDAC) that performs coarse D/A conversion, subtraction, and interstage amplification by 2. A conventional switched-capacitor implementation of a one-bit pipeline stage is shown in Fig. 21. A single ended circuit is shown for simplicity. V_{ref} is the value of the reference voltage, where the complete resolvable input range is $\{-V_{\text{ref}}, +V_{\text{ref}}\}$ [18,34,35].

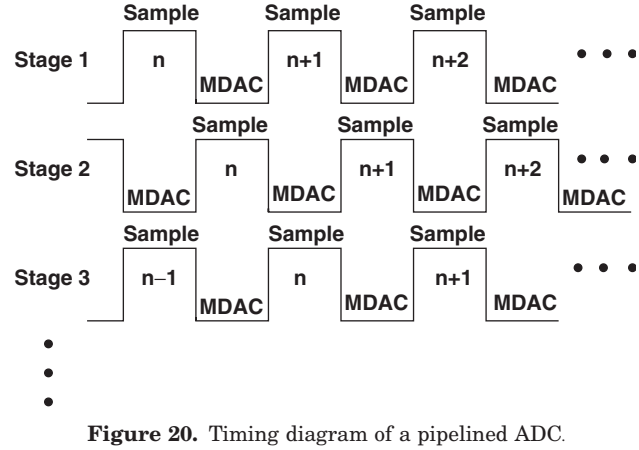

Figure 20. Timing diagram of a pipelined ADC.

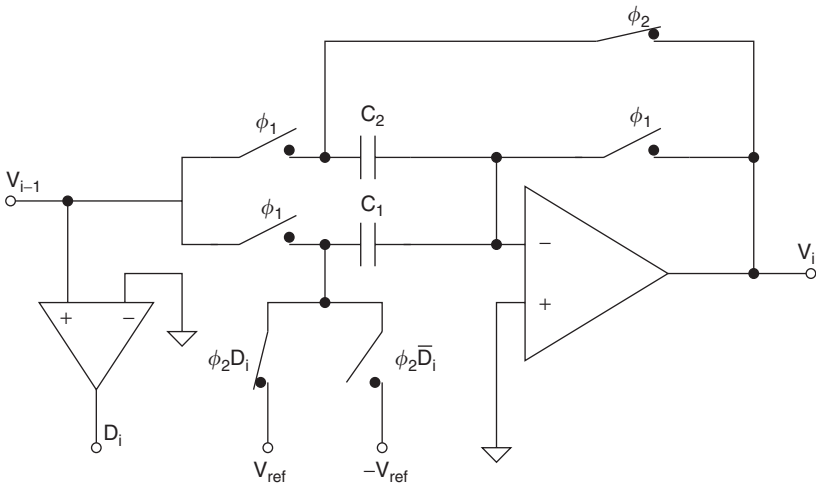

Figure 21. Switched-capacitor (SC) 1-bit pipeline stage (ϕ_1-sampling phase, ϕ_2-multiply-by-2/subtract phase).

Each stage consists of two nominally equal capacitors C_1 and C_2, an operational amplifier (op-amp), and a comparator. During the sampling phase ϕ_1, the comparator produces a digital output D_i by comparing its input V_{i-1} with comparator threshold V_{th}

$$D_i = \begin{cases} 1 & \text{if } V_{i-1} \geq V_{\text{th}} \\ -1 & \text{if } V_{i-1} < V_{\text{th}} \end{cases} \tag{8}$$

where $V_{\text{th}}(=0)$ is the threshold voltage of the comparator. The bipolar representation $\{-1,+1\}$ for the digital bit D_i is chosen instead of {0,1} to facilitate analysis of the pipelined ADC for differential inputs. During the multiply-by-2/subtract (ϕ_2) phase, known as the MDAC phase, the circuit generates a residue voltage output V_i given by

$$V_i = K\left[\left(1+\frac{C_1}{C_2}\right)V_{i-1} - \frac{C_1}{C_2}D_i V_{\text{ref}}\right]$$

$$K = \frac{A_0}{1+\dfrac{C_1}{C_2}+A_0} \tag{9}$$

where the parameter K is an op-amp gain error coefficient (ideally unity) and A_0 is the finite op-amp gain. V_{i-1} is the residue output of the previous stage (for the first stage, the input is $V_0 = V_{\text{in}}$. The output residue voltage of the stage i is then passed to the next stage $i+1$, and the same operation continues. Ideally, we expect the residue output voltage to be

$$V_i = 2V_{i-1} - D_i V_{\text{ref}} \tag{10}$$

The ideal residue output of a one-bit pipeline stage is shown in Fig. 22, assuming $\{-V_{\text{ref}}, +V_{\text{ref}}\}$ as the resolvable input range. We see that as input is increased from $-V_{\text{ref}}$ to $+V_{\text{ref}}$, the output spans the full scale twice, once for the output $D_i = -1$ and for the output $D_i = +1$.

For a multibit per stage pipeline, consider a simple conceptual switched-capacitor implementation in Fig. 23, which indicates a n_i bit per stage output realization. When no error correction is used (see following section), a n_i bit per stage pipeline stage consists of a total of n_i capacitors C_1, C_2,…$C_2 n_i$. During the sampling phase the sub-ADC compares the input with a set of reference voltages possibly a reference ladder to generate the raw bit decisions. At this time the input is also sampled across the 2^{n_i} capacitors. During the MDAC phase, one of the capacitors is connected across the operational amplifier, and the thermometer code corresponding to the raw bit decisions made is applied to the remaining capacitors. This produces an amplified residue output of this stage that will be processed by subsequent sections. The ideal expression for the residue output is given by

$$V_i = 2^{n_i}V_{i-1} - \sum_{k=1}^{k=n_i} 2^{(n_i-k)} D_{Sn_{i-1}+k} V_{\text{ref}} \tag{11}$$

The digital output of stage i is $\{D_i : i = Sn_{i-1}+1, Sn_{i-1}+2 \ldots Sn_i\}$, where $D_{Sn_{i-1}+1}$ is the stage i MSB and D_{Sn_i} is the stage i LSB. Here the variable Sn_i indicates an index to conveniently tag the digital output of the stage i

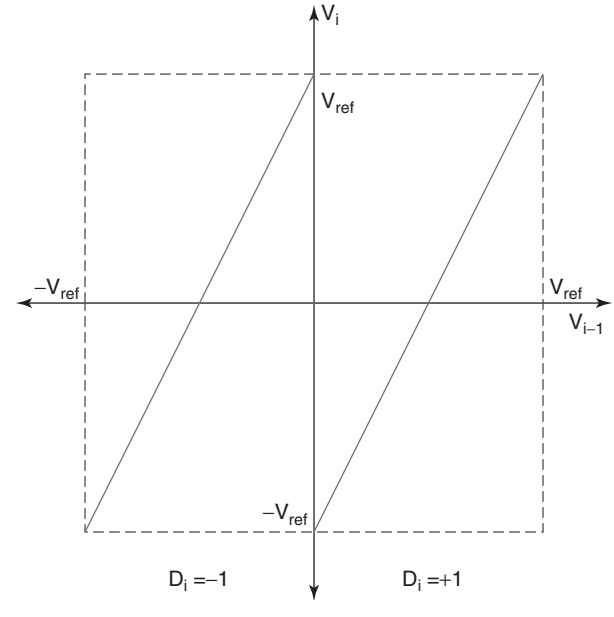

Figure 22. Ideal residue output of a 1-bit pipeline stage.

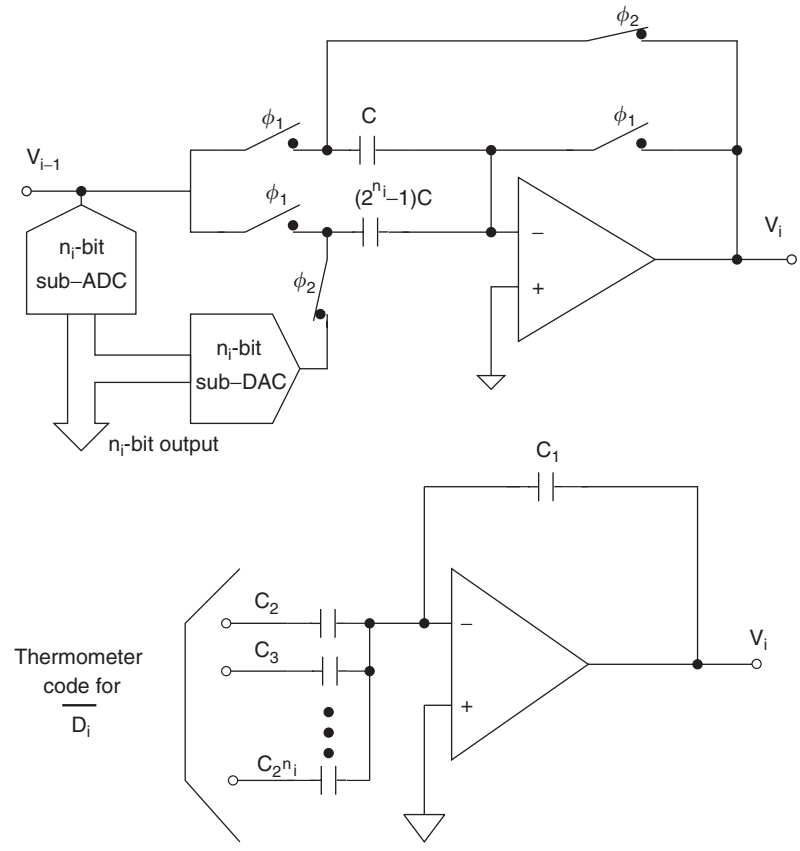

Figure 23. Example of a switched-capacitor (SC) implementation of a multibit pipeline stage.

and is given by

$$Sn_i = \sum_{k=1}^{k=n_i} n_k \qquad (12)$$

$$Sn_0 = 0$$

The ideal residue output for a multibit pipeline stage looks similar to the one-bit case and is shown for a 2-bit pipeline stage in Fig. 24. The bipolar digital outputs for each region are also highlighted in the figure. The main points to note from the residue output plots for an ideal pipeline stage, is that the output spans the complete range of $\{-V_{\text{ref}}, +V_{\text{ref}}\}$, so that each stage input has the same dynamic range. This guarantees linearity for the complete pipelined converter. As is evident from the Eqs. (9) and (10) for a singlebit pipeline, the accuracy of a pipeline stage and hence of the overall converter depends on the accuracy of the residue output generated by the pipeline stage. We see that gain errors are introduced in the overall transfer characteristic because of the term K attributed to the finite amplifier gain and the term C_1/C_2, which deviates from the ideal value of 1 because of poor capacitor matching. The same case is also valid for any multibit pipeline stage. For comparator offsets, the output of the pipeline stage will exceed the allowable input range of the following stage. This results in the *missing decision levels* in the overall ADC transfer characteristic. This is undesirable, since the information about the input is completely lost and cannot be recovered further. Other sources of errors due to capacitor ratio mismatch and finite amplifier gain error result in *missing codes* in the overall transfer characteristics if the overall gain is less than nominal. Although this is undesirable, it is preferred over the case with missing decision levels, since the information about the input is not lost and can be recovered through calibration. Finally, it can also be seen that any nonlinearity in the operational amplifier will affect the linear output curve of the residue and contribute to the overall

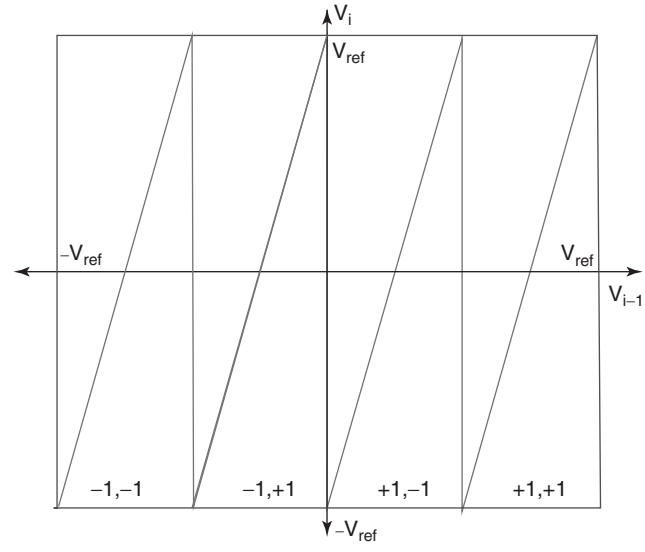

Figure 24. Ideal residue output of a 2-bit pipeline stage.

INL of the ADC. These nonidealities along with errors due to finite amplifier settling and charge injection errors usually limit the overall resolution of the ADC to 8–10 bits without calibration in today's CMOS processes. Charge injection errors can be minimized using bottom-plate sampling techniques [11], and the effect due to comparator offsets can be mitigated through the use of error correction or redundancy [31]. This concept is discussed in the next section.

6. DIGITAL ERROR CORRECTION THROUGH REDUNDANCY

Nonlinearity due to comparator offsets can be mitigated through the use of redundancy [18,31]. For example, with one-bit error correction in a n_i bit per stage pipeline, the interstage gain is chosen as $2^{(n_i-1)}$ instead of 2^{n_i} allowing redundancy so that inputs closer to comparator thresholds that would possibly result in swings beyond the allowable input range can now be resolved by the following pipeline stages.

Consider the modified switched capacitor implementation that incorporates one-bit redundancy (Fig. 25). The stage now consists of two comparators with thresholds on either side of $V_{\text{th}} = 0$, one at $V_{\text{ref}}/4$ and the other at $-V_{\text{ref}}/4$. Also, three different D/A converter outputs are used during the MDAC phase. The main idea behind redundancy is to let prevent the overrange of the residue output when the input is between the two thresholds. This prevents any missing decision levels and improved DNL performance. The expression for the residue output of this 1.5-bit pipeline stage is

$$V_i = 2V_{i-1} - D_i V_{\text{ref}} \tag{13}$$

where D_i is just a conceptual term that can have one of three values $\{-1, 0, 1\}$ instead of the previous bipolar representation $\{-1, 1\}$.

Table 1 suggests the relationship between D_i and D_{i1} and D_{i2}. The residue output of a 1.5-bit pipeline stage is shown in Fig. 26. The transfer characteristic of a 1.5-bit pipeline stage suggests that comparator offsets of up-to

Table 1. Relationship between D_i, D_{i1}, and D_{i2}

D_I	D_{i1}	D_{i2}
-1	-1	-1
0	$+1$	-1
$+1$	$+1$	$+1$

$|V_{\text{ref}}/4|$ can be tolerated without the residue exceeding the following stages resolvable input range.

The digital outputs of individual pipeline stages are now combined by overlapping the adjacent bits as shown in the Fig. 27. A unipolar representation is used for this illustration where the digital output is 00 when input is less than $-V_{\text{ref}}/4$, and 01 when the input is between $-V_{\text{ref}}/4$ and $+V_{\text{ref}}/4$ and 11 when input is greater than $+V_{\text{ref}}/4$.

However, to correct for errors due to capacitor ratio mismatch and finite amplifier gain, calibration schemes (also called error correction schemes in the literature) have to be used. Redundancy will not suffice enough to guarantee a good linearity from the converter, since the shape of the curve still depends on the capacitor ratio mismatch and the finite amplifier gain. Calibration has become an essential building block in today's pipelined data converters designed in deep-sub-micrometer CMOS due to poor technology parameters for realization of analog components such as capacitors, amplifiers, and reference circuits. Without calibration, the resolution of the data converters is limited to 8–10 bits for speeds under 100 MHz in CMOS.

6.1. Linearity Improvement Techniques

Data converters designed in digital CMOS technology for low-cost implementations and to facilitate higher integration do not offer high resolution because of poor component matching, low amplifier gains attributed to lowering supply voltages, charge injection errors, and offset errors. For example, in case of a current steering D/A converter, it is necessary that all the unit current sources be matched to each other. Otherwise, the D/A converter will exhibit nonuniform output transitions, giving rise to static

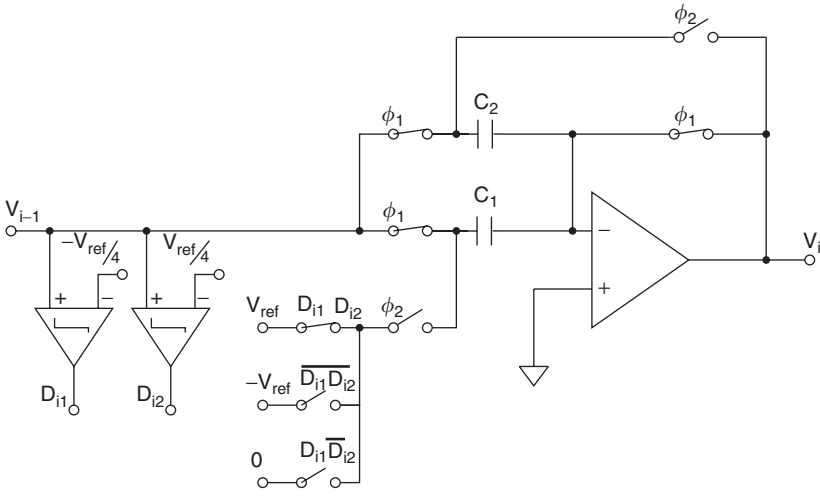

Figure 25. A 1.5-bit pipeline stage that exhibits one-bit redundancy.

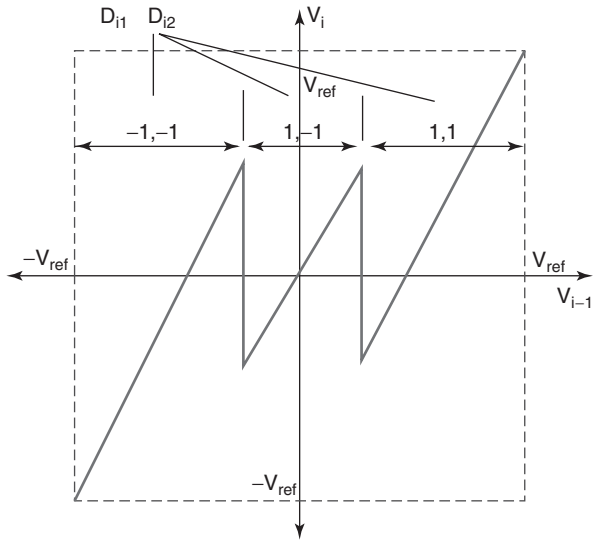

Figure 26. A 1.5-bit pipeline stage that exhibits one-bit redundancy.

nonlinearities that are measured as differential nonlinearity (DNL) and integral nonlinearity (INL) errors. These errors result in poor spectral performance measured by the spurious-free dynamic range (SFDR). When such nonideal D/A converters are used in oversampling A/D converters, the mismatch error adds directly at the input and in most implementations, and is not noise-shaped, resulting in spurious tones in baseband. The nonideal D/A converter used in multibit per stage pipelined A/D converter architectures also gives rise to spurious tones and therefore degrades the dynamic range of the overall A/D converter. Similar issues due to mismatch, offsets, charge injections, and finite amplifier gain errors arise in all architectures for data converters. Therefore, precision techniques need to be developed at both circuit and system levels to improve the resolution performance of the A/D converters.

Dithering and dynamic element matching are two popular techniques that have been widely used to improve the accuracy and the linearity of the converter. *Dithering* involves addition of a pseudorandom dither signal at the input that is either subtracted digitally from the output (a subtractive dither scheme) or not subtracted from the output (an additive dither scheme). The overall result in both cases is an average linearization of the overall converter transfer characteristic, especially around sharp discontinuities [36]. The linearity improvement depends on the magnitude of the dither and that of the discontinuity. A subtractive dither scheme enables high linearity improvement, compared to the additive dither scheme. However, both cases suffer from reduced input dynamic range. *Dynamic element matching* (DEM) techniques, on other hand, perform permutation of the unit elements to convert the systematic error into an error spectrum that is either shaped out of the band of interest or contributes only to increased noise floor. Any spurious tones due to systematic error is removed through DEM schemes. Various DEM schemes have been proposed in the literature depending on the application [2,11,18,36–39].

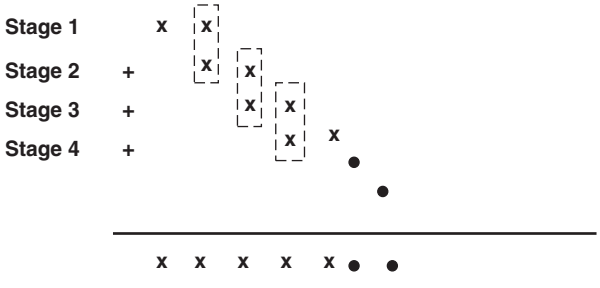

Figure 27. A 1.5-bit pipeline stage that exhibits one-bit redundancy.

Self-calibration is another way to push the resolution performance of the data converters. Many self-calibration schemes have been proposed in the literature for pipelined and multistage ADC [34,35,40–47]. Some of these schemes are implemented in analog domain (e.g., capacitor error-averaging [48], capacitor trimming [46]), and some of them are implemented in digital domain [40–42]. Capacitor error averaging involves mitigating the effect of the capacitor mismatch through averaging of the pipeline output over all permutations of the capacitors. This yields better overall accuracy at the cost of lower speed and increased complexity. Self-trimming of the elements that exhibit mismatch also improve the overall accuracy, but the techniques are usually expensive and can be calibrated only once.

Digital self-calibration schemes have proved to be more robust compared to analog self-calibration schemes [35,40,42] because of their ease of implementation in today's CMOS technology and lower cost. Most of the digital schemes employ techniques to correct for errors by measuring code error transitions in the ADC transfer characteristics. This is achieved by providing appropriate input stimuli [41,42] to the ADC during the calibration phase. The scheme proposed in Ref. 34 performs calibration of both capacitor ratio mismatch and finite amplifier gain in the analog domain for a pipelined A/D converter. It performs continuous calibration by using an extra pipeline stage that is constantly being calibrated in the background while the ADC is in use. Once the extra stage is calibrated, it replaces an active pipeline stage that will be taken out for calibration. Such techniques involving redundant computation show promise for future calibration schemes in emerging CMOS technologies. A few promising digital calibration schemes based on adaptive signal processing techniques have been proposed to correct for errors introduced by finite amplifier gain and capacitor ratio mismatch in a pipeline stage [7,35,44]. One of these schemes needs a separate calibration signal to be added to the input for background calibration, through an adaptive technique for measurement of the gain error introduced for the calibration signal. This technique, proposed in Refs. 35 and 44, adaptively corrects for the residue errors in the pipeline with the use of a slow high-resolution ADC (typically a $\Sigma - \Delta$ ADC) for calibration. This is achieved at the cost of slight increase in hardware and power consumption.

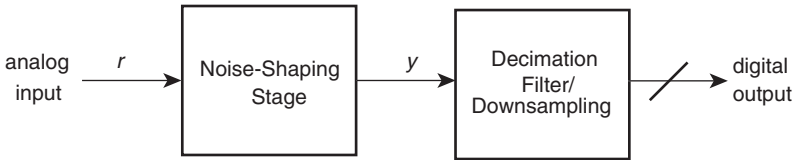

Figure 28. An oversampled analog-to-digital converter. The noise-shaping stage operates at the oversampled clock rate, producing the digital output y that is decimated (filtered and downsampled) to a lower clock rate.

7. OVERSAMPLED CONVERSION

Like Nyquist-rate converters, oversampled converters assume the general form of Fig. 3[2] in which amplitude quantization is also referred to as *noise shaping*. In this section, we cover the basic topologies and methods for achieving noise shaping of analog and digital signals.

An oversampled A/D takes the form shown Fig. 28. Here, the noise-shaping stage is implemented using mainly analog circuitry. Configured as a D/A, the oversampled converter appears as shown in Fig. 29. The noise-shaping stage is completely digital in this system, and therefore any deviation from ideal performance can usually be attributed to imperfections in the Nyquist-rate D/A [17].

All oversampled converters in popular use are derived from the delta–sigma (or sigma–delta) modulator (Fig. 30). It is no wonder, then, that the terms "oversampled" and "delta–sigma" have become interchangeable. A readable and general overview of discrete-time delta–sigma modulation can be found in Ref. 49. Although oversampled converters are often based on a single delta–sigma modulator, it is also possible to interconnect multiple delta–sigma modulators to form a *cascaded* design [2,17]. Well-known variants of the cascaded form include the MASH and Leslie–Singh architectures [50,51]. It is possible to achieve greater SNR performance at lower oversampling ratios with cascading; a more detailed discussion of this approach is provided below.

We note that for oversampled A/D conversion, the delta–sigma modulator is implemented in mixed-signal form, as depicted in Fig. 31. The quantizer block is comprised of a simple Nyquist-rate A/D (generating the output y) and a complementary Nyquist-rate D/A (providing a suitable feedback signal) in cascade. Often, the D/A block is implemented as a thermometer-coded current steering design with dynamic element matching. The use of element matching techniques is necessary to avoid SNR degradation from nonlinearities in the D/A characteristic. For oversampled D/A conversion, the delta–sigma modulator is implemented in purely digital form. Thus the modulator loop itself can be expected to perform ideally. However, the problem of mismatch is now relegated to the cascaded Nyquist-rate D/A, which must be sufficiently linear to allow the oversampled converter to achieve maximum resolution.

Oversampled converters can be developed using a wide range of architectures and technologies. A survey of state-of-the-art oversampled high-speed analog-to-digital converters is provided in Table 2. The results are sorted by signal bandwidth in descending order. With the exception of the technique employed by Paul et al. [52], each design employs a conventional delta–sigma modulator architecture. We see that CMOS oversampled A/Ds now process megahertz-range bandwidths, attaining resolutions of up to 15 bits. Specifically, SNDRs greater than 80 dB are achieved using the basic formula of discrete-time loop filtering and multibit quantization in a cascade (MASH) configuration.

[2]The exception is the case of continuous-time delta–sigma modulation (in which H is realized with continuous-time analog circuitry) in which the sampling operation and amplitude discretization occur simultaneously.

7.1. Design of the Delta–Sigma Modulator

In delta–sigma D/A conversion, the noise shaping stage is implemented digitally, and the system is described in discrete time. In A/D conversion, the delta–sigma modulator is a mixed-signal system, and either continuous-time or discrete-time design descriptions for the loop filter are used.[3] We shall present much of our discussion in a manner that is applicable to either discrete- or continuous-time by employing operator notation; for instance, the symbol H denotes a linear filter that may be considered to be either $H(z)$ or $H(s)$, depending on the context.

The design of the delta–sigma modulator typically proceeds in the frequency domain. Using the pseudolinear model of Fig. 32, the operation of the delta–sigma modulator can be described mathematically as follows:

$$y = G_s r + G_n e_Q \tag{14}$$

where G_s and G_n denote the signal and noise transfer functions, respectively. Both transfer functions are shown conceptually in Fig. 33, where it is seen that, within the designated signal band of the modulator, the magnitude of G_s is roughly unity, while the magnitude of G_n approximates 0 (and describes the noise shaping characteristic of the loop).

The design of the delta–sigma modulator begins with the selection of an appropriate noise transfer function. The loop filter H is in general a two-input system as shown in Fig. 30. Using the expressions for loop filter output

$$\sigma = H_1 r + H_2 y \tag{15}$$

(where H_1 and H_2 describe the responses of H to its first and second inputs, respectively) and overall output according to the pseudolinear model

$$y = e_Q + \sigma \tag{16}$$

[3]Note, however, that although the modulator loop filter may be described in continuous time, the delta–sigma modulator is itself a sampled-data system. Therefore, the overall system must be converted to discrete time as described in Ref. 56 to obtain a correct description of modulator operation.

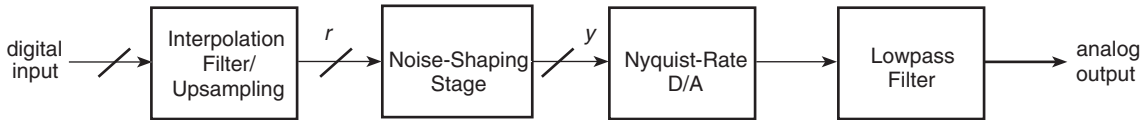

Figure 29. An oversampled digital-to-analog converter. The digital input signal is first upsampled to the oversampled data rate before being encoded by the purely digital noise-shaping stage.

we obtain the closed-loop expression for y as follows:

$$y = H_1(1-H_2)^{-1}r + (1-H_2)^{-1}e_Q \tag{17}$$

Therefore, the signal and noise transfer functions are given by $G_s = H_1(1-H_2)^{-1}$ and $G_n = (1-H_2)^{-1}$. Special attention is paid to the selection of G_n since the level of noise attenuation dictates overall performance and modulator stability [57]. A G_n that exhibits an aggressive profile can drive the system into instability. As a rule of thumb, the peak gain of G_n should be less than 1.5 for single-bit quantization to reduce the likelihood of instability. If finer quantization is employed, the noise transfer function can be more aggressive. Although a sufficient condition exists to ensure stability in the multibit case [58], it is thought to be too conservative, and most designers rely on simulation to assess modulator robustness. Nevertheless, it is important that simulation not be misconstrued as proof of stability, and the designer should anticipate the onset of instability, however infrequent.

A design recipe for achieving any desired SQNR (signal-to-quantization-noise ratio) has been provided [57]. A toolbox developed by Schreier [59] based on Matlab provides an outstanding array of scripts to assist the designer from noise transfer function design to full block-level realization, and is highly recommended. Using this toolbox, we generated the plots of Figs. 34 and 35. These graphs indicate the performance achievable with single- and multibit designs, respectively, in terms of peak SQNR versus (normalized) signal bandwidth. Various orders are shown and optimum noise transfer function zero placement has been used.

The realization of the loop filter H can proceed in several ways; a popular continuous-time structure is shown in Fig. 36. In the continuous-time case where there is significant parametric uncertainty (brought on by mismatch between active and passive circuit elements), loop filter sensitivity is an important issue, particularly for higher-order designs. Filter tuning may be necessary to mitigate the effects of sensitivity [60]. The main advantage of using more sensitive realizations is that some savings in hardware complexity can be achieved. A thorough treatment of discrete-time loop filter realizations is provided in the documentation accompanying the toolbox by Schreier [59].

Cascaded architectures use multiple delta–sigma modulators to achieve greater attenuation of quantization noise without the need to increase oversampling ratio. Figure 37 shows the general form of a cascaded noise-shaper. The main challenge in the design of oversampled A/Ds is that the transfer functions $G_i(z)$ must match quantities that are realized with analog hardware (as shown below). For oversampled D/As, mismatch is not an issue since all blocks (including the modulators) are realized digitally and perfect matching is possible. The analysis in the case of a cascade of modulators proceeds as follows. The outputs of the first, second, and third modulators can be written as:

$$y_1 = H_{11}(1-H_{12})^{-1}r + (1-H_{12})^{-1}e_{Q1} \tag{18}$$

$$y_2 = H_{21}(1-H_{22})^{-1}e_{Q1} + (1-H_{22})^{-1}e_{Q2} \tag{19}$$

and

$$y_3 = H_{31}(1-H_{32})^{-1}e_{Q2} + (1-H_{32})^{-1}e_{Q3} \tag{20}$$

where H_{ij} denotes the jth loop filter transfer function associated with modulator $i \in \{1,2,3\}, j \in \{1,2\}$. The overall noise-shaped output can be written as

$$y = y_1 - G_1 y_2 - G_2 y_3 \tag{21}$$

$$\begin{aligned} &= H_{11}(1-H_{12})^{-1}r + [(1-H_{12})^{-1} - G_1 H_{21}(1-H_{22})^{-1}]e_{Q1} \\ &\quad - [G_1(1-H_{22})^{-1} + G_2 H_{31}(1-H_{32})^{-1}]e_{Q2} \\ &\quad - G_2(1-H_{32})^{-1}e_{Q3} \end{aligned} \tag{22}$$

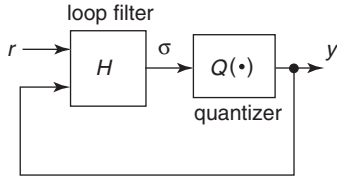

Figure 30. The basic delta–sigma modulator. The output y is a noise-shaped version of the input r. The *quantizer* element is a clocked device, and the *loop filter* is a linear time-invariant (LTI) system. The clock rate of the system is often many times higher than the specified signal bandwidth. For D/A conversion, the modulator is implemented entirely in digital form; for A/D converters, the modulator is a mixed-signal loop.

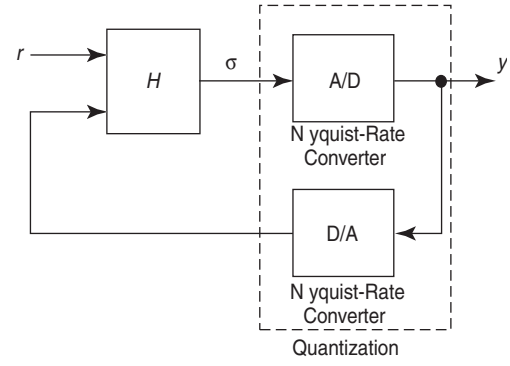

Figure 31. A mixed-signal delta–sigma modulator used in oversampled A/D conversion.

Table 2. Reported High-Speed Oversampled Architectures for A/D Conversion[a]

Peak SNDR (dB)	Signal BW, OSR	Technology	Architecture, Quantization Supply, Power Consumption	Ref.
43	990 MHz, 9	InAlAs/InGaAs, bipolar	CT[b] 2nd-order lowpass, single-bit, 8 V, 1.5 W	[53]
55	50 MHz, 32	InP, bipolar	CT 2nd-order lowpass, single-bit, ±5 V, 1 W	[54]
71	9 MHz, 1	1.2-μm-Si CCD-CMOS	Oversampled pipelined lowpass, multibit, 5/4/3.3 V, 324 mW	[52]
87	2 MHz, 16	0.5-μm-Si CMOS	SC[b] cascaded (2-2-1) lowpass, multibit, 2.5 V, 150 mW	[2]
90	1.25 MHz, 8	0.5-μm-Si CMOS	SC cascaded (2-1-1) lowpass, multibit, 5 V, 270 mW	[3]
89	1.25 MHz, 8	0.6-μm-Si CMOS	SC cascaded pipeline lowpass, multibit, 5/3 V, 550 mW	[4]
82	1.1 MHz, 24	0.5-μm-Si CMOS	SC cascaded (2-1-1) lowpass, single-bit, 3.3 V, 200 mW	[51]
76	1 MHz, 2000	AlInAs/GaInAs, bipolar	CT 4th-order bandpass, single-bit, ±5 V, 3.2 W	[55]
77	0.5 MHz, 32	0.35-μm-SoI BCMOS	SC 2nd-order lowpass, multibit, 2.7 V, 12 mW	[38]

[a]The results indicate the typical performance possible with conventional delta–sigma modulation techniques.
[b]Continuous time.
[c]Switched-capacitor.

from which we see that if the matching conditions

$$G_1 = (1 - H_{12})^{-1}[H_{21}^{-1}(1 - H_{22})] \tag{23}$$

and

$$G_2 = -G_1(1 - H_{32})^{-1}[H_{31}^{-1}(1 - H_{32})] \tag{24}$$

are met, then y becomes

$$y = H_{11}(1 - H_{12})^{-1}r - G_2(1 - H_{32})^{-1}e_{Q3} \tag{25}$$

where e_{Q3} is a residual error that is, in general, strongly attenuated relative to the original single-stage quantization error, e_{Q1}.

Note that the conditions (23) and (24) can imply that the digitally realized transfer functions G_1 and G_2 match responses of filters made from analog components. Thus, in the case of cascaded oversampled A/Ds, careful analog circuit design or the use of adaptive filtering may be necessary to ensure that (23) and (24) approximately hold. In spite of this potential shortcoming, cascaded architectures have achieved the highest performance levels in practice (as shown in the literature). Another distinct advantage of using cascaded noise shaping is that stability may be guaranteed if delta–sigma modulators of order ≤ 2 are employed throughout the design.

7.2. Architectural Choices

We may consider various options in the design of delta–sigma modulators, including the choice of quantizer size, higher-order loop filtering, and continuous-time techniques.

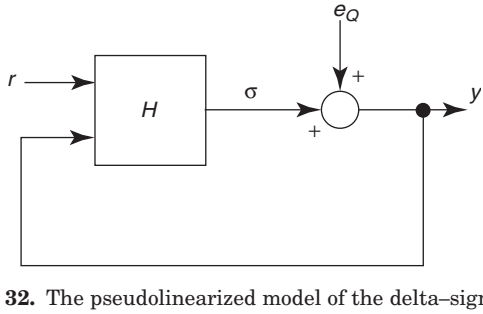

Figure 32. The pseudolinearized model of the delta–sigma modulator. By using a uniformly distributed random variable e_Q, it is possible to approximate the behavior of the actual delta–sigma modulator.

7.2.1. Single-Bit or Multibit Quantization? In general, the in-band noise power for multibit mixed-signal delta–sigma modulators is dominated by component nonidealities, and not by quantization noise. The mismatch amongst elements comprising the quantizer D/A is a dominant noise source (even if mitigated by the use of dynamic element matching). Therefore, multibit modulators are used for higher-speed applications in which lower oversampling ratios mean that the ideal SQNR (signal-to-quantization-noise ratio) of the architecture is moderate (generally less than 90 dB). On the other hand, with the perfect linearity of a single-bit quantizer, single-bit delta–sigma modulators can come much closer to ideal SQNR performance at high oversampling ratios. Thus they are used for narrowband applications (particularly digital audio) in which high resolution is a priority.

Both single-bit and multibit delta–sigma modulators are susceptible to spurious tones, albeit for different reasons. In the single-bit case, dithering as described by

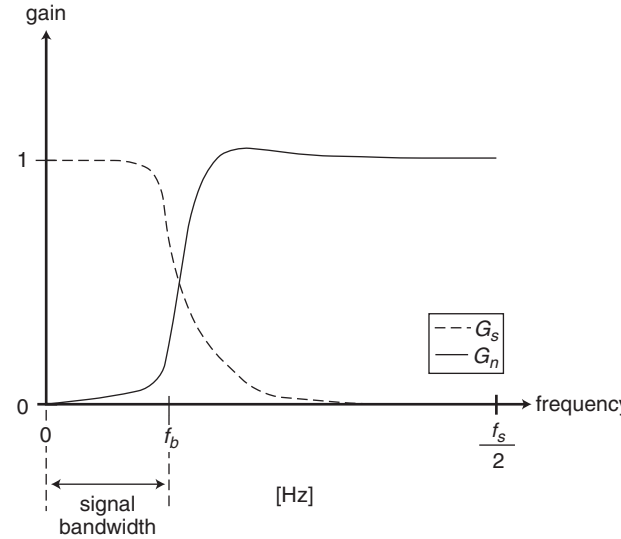

Figure 33. Depictions of modulator noise transfer function (G_n) and signal transfer function (G_s).

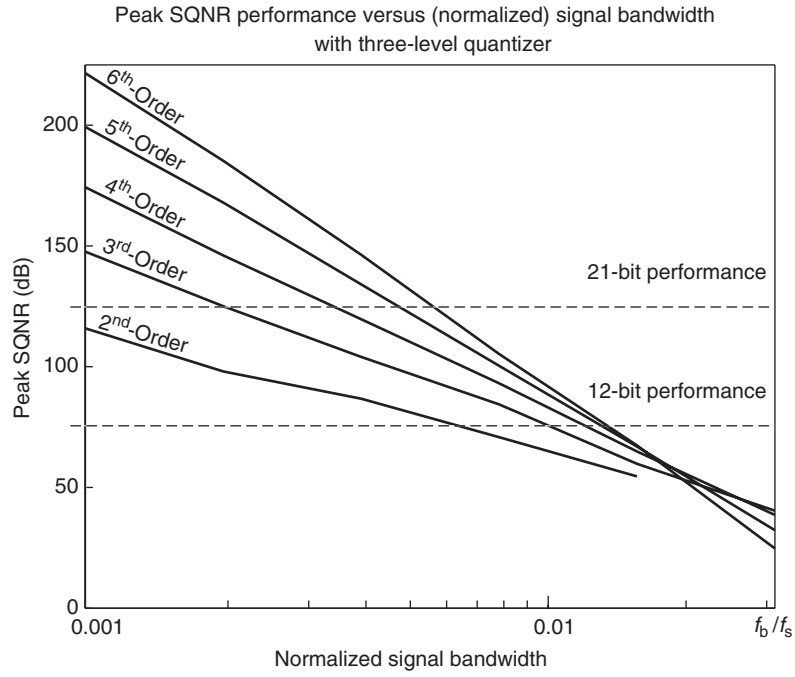

Figure 34. Resolution of single-bit delta–sigma modulators of various orders versus sample-rate-normalized signal bandwidth. The noise-transfer function out-of-band gain is set to 1.5 for all designs.

Norsworthy [61] can be applied to diffuse tones with only a slight impact on dynamic range. Multibit modulators can exploit various techniques for randomizing the selection of D/A elements. This helps to minimize tones generated by any periodicities in the dynamic element matching strategy.

In the case of oversampled D/A conversion, the delta–sigma modulator is implemented digitally; therefore, there are no linearity issues associated with a multibit quantizer. However, a single-bit architecture can be advantageous because the digital circuitry is simplified. Multiplication of a multibit filter coefficient by a single-bit quantity is trivial. An additional complication with multibit delta–sigma D/A converters is that the noise-shaping loop is typically followed by a Nyquist-rate D/A. Therefore, because the Nyquist-rate D/A appears "open loop" in cascade with a digital delta–sigma modulator, it must be highly linear.

7.2.2. Higher-Order/Coarser Quantizer or Lower-Order/Finer Quantizer? A current trend in broadband CMOS delta–sigma A/D converters is the use of low (typically less

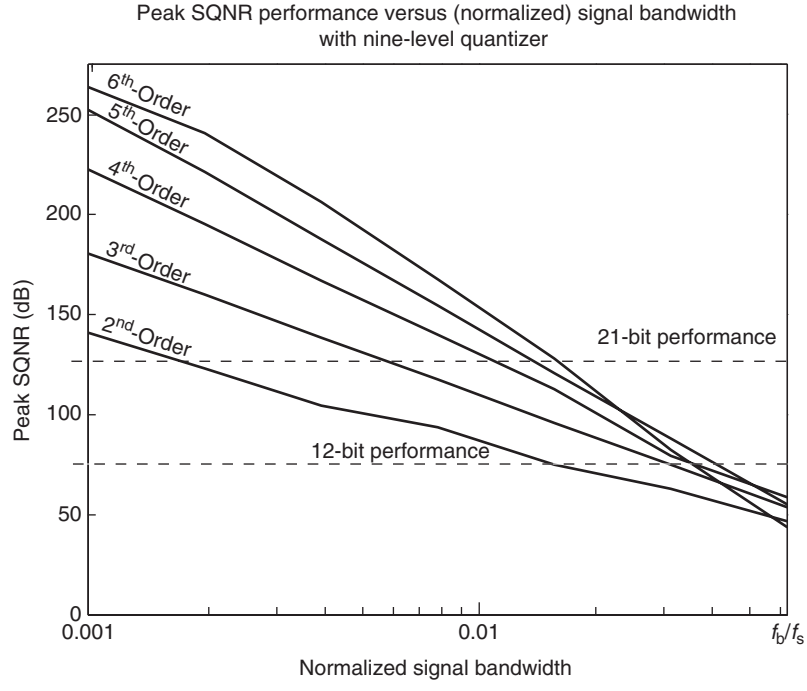

Figure 35. Resolution of 3-bit delta–sigma modulators of various orders versus sample-rate-normalized signal bandwidth. The noise transfer function out-of-band gain is set to 6.0 for all designs.

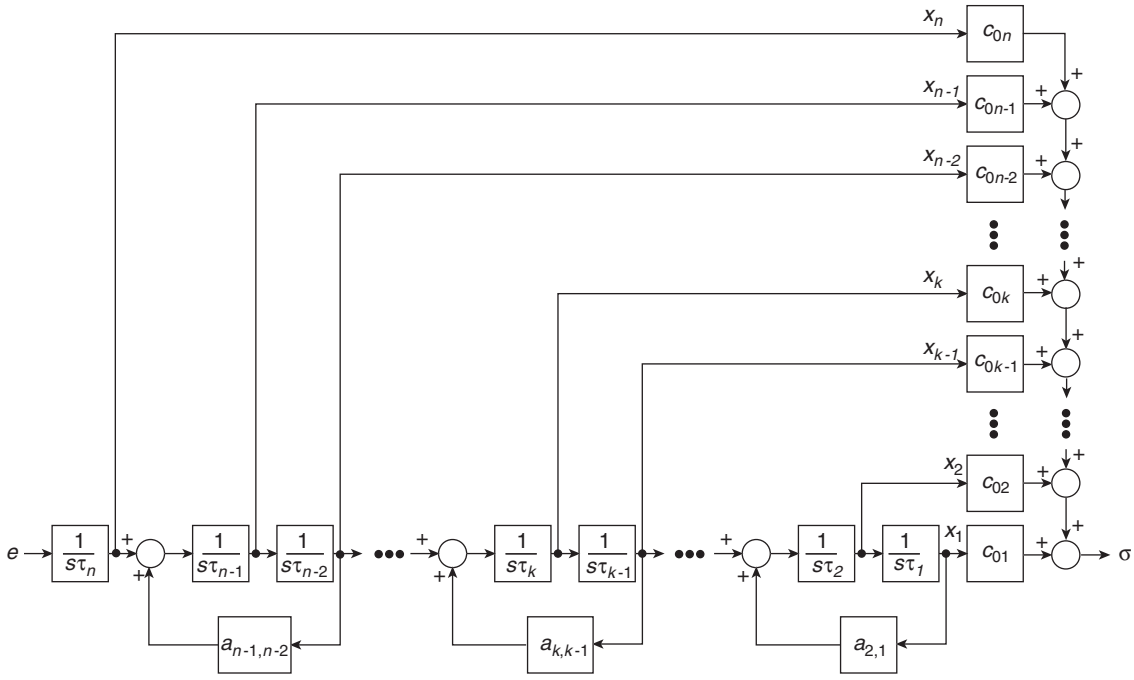

Figure 36. A common loop filter realization for continuous-time delta–sigma modulators (odd order case). If n is even, the leftmost integrator is omitted.

than fourth) order loop filters with finer quantization (up to 5 bits). Such a combination often makes sense because stability is more manageable at lower orders, and greater signal bandwidths can be used because of the SNR "boost" provided by a larger quantizer. A given peak SQNR specification may be achieved either by using a loop filter with sufficiently high order (given a quantizer of fixed size), or by employing a quantizer with sufficiently many bits (given a fixed order for H). The choice is dictated by such considerations as power consumption, chip area, or the designer's own expertise. While higher-order loop filters may result in more analog power consumption, the use of a coarse quantizer helps to conserve digital power consumption at higher sampling rates. Area usage can increase exponentially with the number of quantizer bits; in spite of this, a number of designers have managed to produce compact multibit designs.

7.2.3. Continuous-Time or Discrete-Time *H*? The use of continuous-time loop filtering provides two primary advantages: (1) the maximum clock rate (and hence the oversampling ratio) of the system can be much higher than with discrete-time loop filtering and (2) a sample-and-hold circuit preceding the noise shaping stage of the converter is unnecessary. With discrete-time designs based on switched-capacitor technology, the unity-gain bandwidths of the integrator opamps are required to be between 3 and 5 times the sampling rate of the system [11]. This can place a restrictive upper bound on the maximum rate with which the modulator can be clocked. In contrast, the maximum sampling rate of continuous-time modulators is determined by considerations of excess loop delay (for which compensation is possible) and quantizer metastability [62,63], which are, in general, less severe constraints on the maximum sampling frequency. The sampling operation of a continuous-time modulator occurs at the quantization stage, therefore, a sample-and-hold circuit preceding the modulator is not needed. However, because the signaling scheme of the modulator is in continuous time, any quantizer sampling imperfections (sampling jitter or quantizer metastability), can severely degrade SNR performance. Quantizer metastability is usually the more significant noise source, and strategies exist to counter it (at the expense of greater loop delay).

8. CONCLUSION

This article provides an overview of modern A/D and D/A converter design for integrated circuits. Nyquist-rate and oversampled techniques are covered with an emphasis on fundamental concepts and key strategies for high-performance design.

Nyquist-rate architectures are most suitable for higher bandwidth applications with modest resolution requirements. Flash, folding, and pipelined techniques for converter design offer varying tradeoffs between hardware complexity and conversion speed. Oversampled converters based on delta–sigma modulation are appropriate for narrowband wide-dynamic-range applications. System requirements dictate the selection of noise shaping architecture, modulator loop filter realization, and quantizer characteristics.

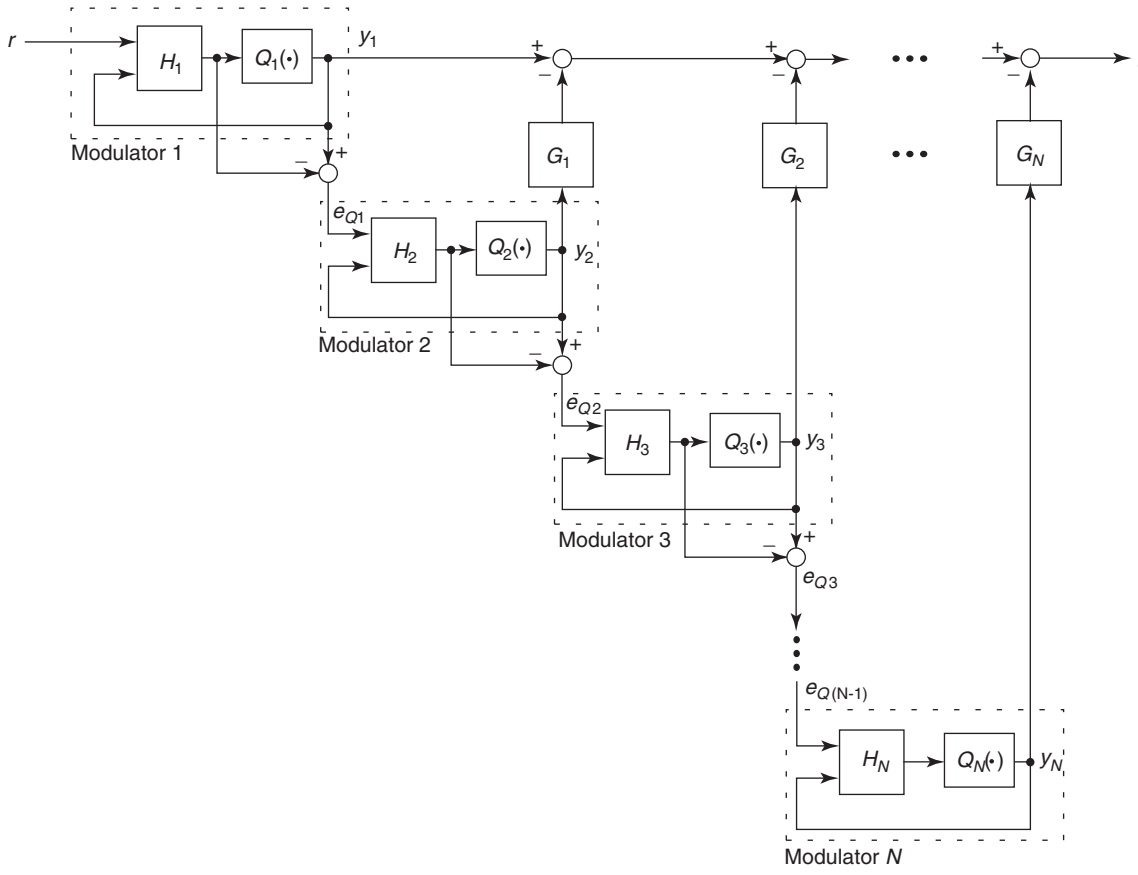

Figure 37. The general form of a cascaded noiseshaping architecture. The delta–sigma modulators are either digital or mixed-signal blocks (depending on the application), and the filter G_i are digital filters.

BIBLIOGRAPHY

1. B. Razavi, *Principles of Data Conversion System Design*, IEEE Press, 1995.
2. K. Vleugels, S. Rabii, and B. A. Wooley, A 2.5-V sigma-delta modulator for broadband communications applications, *IEEE J. Solid-State Circ*. **36**:1887–1899 (2001).
3. I. Fujimori, L. Longo, A. Hairapetian, K. Seiyama, S. Kosic, J. Cao, and S.-L. Chan, A 90-dB SFDR 2.5-MHz output-rate ADC using cascaded multibit delta–sigma modulation at 8 × oversampling ratio, *IEEE J. Solid-State Circ*. **35**: 1820–1828 (2000).
4. T. L. Brooks, D. H. Robertson, D. F. Kelly, A. Del Muro, and S. W. Harston, A cascaded sigma-delta pipeline A/D converter with 1.25 MHz signal bandwidth and 89 dB SNR, *IEEE J. Solid-State Circ*. **32**:1896–1906 (1997).
5. A. van den Bosch, M. A. F. Borremans, M. S. J. Steyaert, and W. Sansen, A 10-bit 1-G Sample/s Nyquist current-steering CMOS D/A converter, *IEEE J. Solid-State Circ*. **36**:315–324 (2001).
6. M.-J. Choe, B.-S. Song, and K. Bacrania, An 8-b 100-M Sample/s CMOS pipelined folding ADC, *IEEE J. Solid-State Circ*. **36**:184–194 (2001).
7. J. Ming and S. H. Lewis, An 8-bit 80-M Sample/s pipelined analog-to-digital converter with background calibration, *IEEE J. Solid-State Circ*. **36**:1489–1497 (2001).
8. R. C. Taft and M. R. Tursi, A 100-MS/s 8-b CMOS subranging ADC with sustained parametric performance from 3.8 V down to 2.2 V, *IEEE J. Solid-State Circ*. **36**:331–338 (2001).
9. L. Sumanen, M. Waltari, and K. A. I. Halonen, A 10-bit 200-MS/s CMOS parallel pipeline A/D converter, *IEEE J. Solid-State Circ*. **36**:1048–1055 (2001).
10. A. Hastings, *The Art of Analog Layout*, Prentice-Hall, 2001.
11. D. A. Johns and K. Martin, *Analog Integrated Circuit Design*, Wiley, 1997.
12. A. Oppenheim and R. Schafer, *Discrete-Time Signal Processing*, Prentice-Hall, 1989.
13. K. Vleugels, *Broadband Oversampling Analog-to-Digital Conversion for Digital Communications*, Ph.D. dissertation, Stanford Univ., 2002.
14. R. van de Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*, Kluwer Academic Publishers, 2003.
15. L. Carley, A noise-shaping coder topology for 15+ bit converters, *IEEE J. Solid-State Circ*. **24**:267–273 (April 1989).
16. R. Schreier and B. Zhang, Noise-shaped multi-bit D/A converter employing unit elements, *IEE Electron. Lett*. **31**: 1712–1713 (Sept. 1995).
17. G. C. Temes, S. Shu, and R. Schreier, Architectures for ΔΣ DACs, in S. Norsworthy, R. Schreier, and G. Temes, eds., *Delta–Sigma Data Converters: Theory, Design and Simulation*, IEEE Press, 1997, pp. 309–332.

18. M. Gustavvson, J. J. Wikner, and N. N. Tan, *CMOS Data Converters for Communications*, Kluwer Academic Publishers, 2000.
19. R. H. Walden, Analog-to-digital converter survey and analysis, *IEEE J. Select. Areas Commun.* **17**:539–550 (April 1999).
20. M. Choi and A. Abidi, A 6-b 1.3-Gsample/s A/D converter in 0.35-μm CMOS, *IEEE J. Solid-State Circ.* **36**:1847–1858 (Dec. 2001).
21. B.-S. Song, S.-H. Lee, and M. F. Tompsett, A 10-b 15-MHz CMOS recycling two-step A/D converter, *IEEE J. Solid-State Circ.* **25**:1328–1338 (1990).
22. H. Van Der Ploeg and R. Remmers, A 3.3 V 10 b 25 M sample/s two-step ADC in 0.35 μm CMOS, *Proc. 1999 IEEE Int. Solid State Circuits Conf.*, Feb. 1999, pp. 318–319.
23. W. Colleran and A. Abidi, A 10-b, 75-MHz two-stage pipelined bipolar A/D converter, *IEEE J. Solid-State Circ.* **28**:1187–1199 (Dec. 1993).
24. R. van de Grift, I. Rutten, and M. ven der Veen, An 8-bit video ADC incorporating folding and interpolation techniques, *IEEE J. Solid-State Circ.* **22**:944–953 (Dec. 1987).
25. K. Kusumoto, A. Matsuzawa, and K. Murata, A 10-b, 20-MHz 30-mW pipelined interpolating CMOS ADC, *IEEE J. Solid-State Circ.* **28**:1200–1206 (Dec. 1993).
26. J. van Valburg and R. van de Plassche, An 8-b 650-MHz folding ADC, *IEEE J. Solid-State Circ.* **27**:1662–1666 (Dec. 1992).
27. M.-J. Choe, B. Song, and K. Barcania, A 13 b 40 M Sample/s CMOS pipelined folding ADC with background offset trimming, *Proc. 2000 IEEE Int. Solid State Circuits Conf.*, Feb. 2000, pp. 36–37.
28. C. Moreland, M. Elliott, F. Murden, J. Young, M. Hensley, and R. Stop, A 14 b 100 M sample/s 3-stage A/D converter, *Proc. 2000 IEEE Int. Solid State Circuits Conf.*, Feb. 2000, pp. 34–35.
29. H. Pan and M. E. A. Segami, A 3.3 V, 12 b, 50 M Sample/s A/D converter in 0.6 μm CMOS with over 80 dB SFDR, *Proc. 2000 IEEE Int. Solid State Circuits Conf.*, Feb. 2000, pp. 40–41.
30. T. Shimizu, M. Hotta, K. Maio, and S. Ueda, A 10-bit 20-MHz two-step parallel A/D converter with internal s/h, *IEEE J. Solid-State Circ.* **24**:13–20 (Feb. 1989).
31. S. H. Lewis, H. S. Fetterman, G. F. Gross, Jr., R. Ramachandran, and T. R. Viswanathan, A 10-b 20-M sample/s analog-to-digital converter, *IEEE J. Solid State Circ.* **27**(3):351–358 (March 1992).
32. Y.-I. Park, S. Karthikeyan, F. Tsay, and E. Bartolome, A 10 b 100 M sample/s CMOS pipelined ADC with 1.8 v power supply, *Proc. 2001 IEEE Int. Solid State Circuits Conf.*, Feb. 2001, pp. 130–131.
33. D. Kelly, W. Yang, I. Mehr, M. Sayuk, and L. Singer, A 3 V 14b 75 MSPS CMOS ADC with 85 dB SFDR at nyquist, *Proc. 2001 IEEE Int. Solid State Circuits Conf.*, Feb. 2001, pp. 134–135.
34. J. Ingino and B. Wooley, A continuously calibrated 12-b, 10-MS/s, 3.3-V A/D converter, *IEEE J. Solid State Circ.*, **33**(12):1920–1931 (Dec. 1998).
35. S. Sonkusale, J. Van der Spiegel, and K. Nagaraj, True background calibration technique for pipelined ADC, *IEE Electron. Lett.* **36**(9):786–788 (April 2000).
36. R. Jewett, K. Poulton, K. C. Hsieh, and J. Doernberg, A 12 b 128 M Sample/s ADC with 0.05 lsb dnl, *Proc. 1997 IEEE Int. Solid State Circuits Conf.*, Feb. 1997, pp. 138–139.
37. P. Yu, S. S. Joharapurkar, A. Chugh, B. A. R., X. Du, S.-U. Kwak, Y. Papantonopoulous, and T. Kuyel, A 14 b 40 M Sample/s pipelined ADC with dfca, *Proc. 2001 IEEE Int. Solid State Circuits Conf.*, Feb. 2001, pp. 136–137.
38. J. Grilo, I. Galton, K. Wang, and R. G. Montemayor, A 12-mW ADC delta–sigma modulator with 80 dB of dynamic range integrated in a single-chip bluetooth transceiver, *IEEE J. Solid-State Circ.* **37**:271–278 (2002).
39. A. Shabra and H.-S. Lee, Oversampled pipeline A/D converters with mismatch shaping, *IEEE J. Solid-State Circ.* **37**: 566–578 (2002).
40. H. S. Lee, A 12-b 600 ks/s digitally self-calibrated pipelined algorithmic ADC, *IEEE J. Solid State Circ.* **29**(4):509–515 (April 1994).
41. A. N. Karanicolas, S.-H. Lee, and K. L. Barcania, A 15-b 1-M sample/s digitally self-calibrated pipeline ADC, *IEEE J. Solid State Circ.* **28**(12):1207–1215 (Dec. 1993).
42. U.-K. Moon and S. B. S., Background digital calibration techniques for pipelined ADC's, *IEEE Trans. Circ. Syst. II: Analog Digital Signal Process.* **44**(2):102–109 (Feb. 1997).
43. S.-U. Kwak, B. S. Song, and K. Barcania, A 15-b 5-M sample/s low-spurious CMOS ADC, *IEEE J. Solid State Circ.* **32**(12): 1866–1875 (Dec. 1997).
44. S. Sonkusale, J. Van der Spiegel, and K. Nagaraj, Background digital error correction technique for pipelined analog-digital converters, *Proc. 2001 IEEE Int. Symp. Circuits and Systems*, May 2001, pp. 408–411.
45. S. H. Lee and B. S. Song, Digital-domain calibration of multistep analog-to-digital converters, *IEEE J. Solid State Circ.* **27**(12):1679–1688 (Dec. 1992).
46. Y. M. Lin, B. Kim, and P. Gray, A 13-b 2.5-MHz self-calibrated pipelined A/D converter in 3-μm CMOS, *IEEE J. Solid State Circ.* **26**:628–636 (April 1991).
47. H. S. Lee, D. A. Hodges, and P. R. Gray, A self-calibrating 15 bit CMOS A/D converter, *IEEE J. Solid State Circ.* **19**(6): 813–819 (Dec. 1984).
48. B. S. Song, M. F. Tompsett, and K. R. Lakshmikumar, A 12-bit 1-M sample/s capacitor error-averaging pipelined A/D converter, *IEEE J. Solid State Circ.* **23**(6):1324–1333 (Dec. 1988).
49. P. Aziz, H. Sorensen, and J. Van der Spiegel, Overview of sigma-delta converters, *IEEE Signal Process. Mag.*, **27**:66–84 (Jan. 1996).
50. M. Rebeschini, The design of cascaded $\Delta\Sigma$ ADCs, in S. Norsworthy, R. Schreier, and G. Temes, eds., *Delta–Sigma Data Converters: Theory, Design and Simulation*, IEEE Press, 1997, pp. 193–218.
51. Y. Geerts, A. M. Marques, M. S. J. Steyaert, and W. Sansen, A 3.3-V, 15-bit, delta–sigma ADC with a signal bandwidth of 1.1 MHz for ADSL applications, *IEEE J. Solid-State Circ.* **34**:927–936 (1999).
52. S. A. Paul, H.-S. Lee, J. Goodrich, T. F. Alailima, and D. D. Santiago, A Nyquist-rate pipelined oversampling A/D converter, *IEEE J. Solid-State Circ.* **34**:1777–1787 (1999).
53. S. Jaganathan, S. Krishnan, D. Mensa, T. Mathew, Y. Betser, Y. Wei, D. Scott, R. Urteaga, and M. Rodwell, An 18-GHz continuous-time Σ-Δ analog-digital converter implemented in InP-transferred substrate HBT technology, *IEEE J. Solid-State Circ.* **36**:1343–1350 (2001).
54. J. F. Jensen, G. Raghavan, A. E. Cosand, and R. H. Walden, A 3.2-GHz second-order delta–sigma modulator implemented in InP HBT technology, *IEEE J. Solid-State Circ.* **30**:1119–1127 (1995).
55. G. Raghavan, J. F. Jensen, J. Laskowski, M. Kardos, M. G. Case, M. Sokolich, and S. Thomas, Architecture, design, and test of continuous-time tunable intermediate-frequency bandpass delta–sigma modulators, *IEEE J. Solid-State Circ.* **36**:5–13 (2001).

56. R. Schreier and B. Zhang, Delta–sigma data converters employing continuous-time circuitry, *IEEE Trans. Circ. Syst. I: Fund. Theory Appl*. **43**:324–332 (1996).
57. R. Adams and R. Schreier, Stability theory for ΔΣ modulators, in S. Norsworthy, R. Schreier, and G. Temes, eds., *Delta–Sigma Data Converters: Theory, Design and Simulation*, IEEE Press, 1997, pp. 141–164.
58. C. Wolff, J. G. Kenney, and L. R. Carley, CAD for the analysis and design of ΔΣ converters, in S. Norsworthy, R. Schreier, and G. Temes, eds., *Delta–Sigma Data Converters: Theory, Design and Simulation*, IEEE Press, 1997, pp. 447–467.
59. R. Schreier, The delta–sigma toolbox (version 2.0), Jan. 2000, URL *http://www.mathworks.com* (search author's last name "Schreier" in Matlab Central file exchange).
60. T. Zourntos, *Compensation of Delta–Sigma Modulators: Stabilization, Signal Restoration and Integrated Circuits*, Ph.D. dissertation, Univ. Toronto, 2003.
61. S. R. Norsworthy, Quantization errors and dithering in ΔΣ modulators, in S. Norsworthy, R. Schreier, and G. Temes, eds., *Delta–Sigma Data Converters: Theory, Design and Simulation*, IEEE Press, 1997, pp. 75–140.
62. J. A. Cherry and W. M. Snelgrove, Clock jitter and quantizer metastability in continuous-time delta–sigma modulators, *IEEE Trans. Circ. Syst. II: Analog Digital Signal Process*. **46**:661–676 (1999).
63. J. A. Cherry and W. M. Snelgrove, Excess loop delay in continuous-time delta–sigma modulators, *IEEE Trans. Circ. Syst. II: Analog Digital Signal Process*. **46**:376–389 (1999).

ACOUSTIC MICROWAVE DEVICES

PETER M. SMITH
McMaster University
Hamilton, Canada

1. INTRODUCTION

Since the first experiments on piezoelectricity by the Curie brothers in 1880, many devices have employed mechanical waves to process electrical signals. While their frequency of operation is usually well beyond the audible range, these waves are referred to as *acoustic waves* because of their mechanical nature. From an electrical standpoint, their principal benefits stem from the relatively low velocities of acoustic waves, which are in the order of 10^5 times lower than the velocity of electromagnetic waves. This leads to very small devices that can be made to meet very stringent specifications.

In virtually all radiofrequency (RF) and microwave applications, the acoustic waves are generated and detected in crystals through piezoelectricity, which couples electric fields to mechanical deformations. There are two broad types of devices:

- *Bulk acoustic wave* (BAW) resonators employ surface electrodes to generate mechanical waves that travel through the interior ("bulk") of the crystal. They have proved to be compact and reliable, and have become ubiquitous in high-precision oscillators having a fundamental frequency of up to 20 MHz. Their resonant frequency depends on the exterior dimensions of the crystal. At high frequencies, standalone bulk crystal resonators become too thin and fragile for most applications.
- *Surface acoustic wave* (SAW) devices employ transducers to generate waves that propagate along the surface of a crystal [1]. They overcome the frequency limitations of the bulk acoustic wave resonators because the frequency of operation becomes independent of the crystal thickness. They also make the acoustic waves accessible along their entire propagation path, thus permitting sampling of the waves at arbitrary points.

2. BAW DEVICE STRUCTURES

At microwave frequencies, the most practical structure for employing bulk acoustic waves is known as the *thin-film bulk acoustic wave* (FBAW) resonator. It consists of a thin-film piezoelectric layer grown between two metal electrodes. The film is normally in the order of 1 μm thick, and the structure is often built on an airbridge in order to isolate it mechanically from the substrate. This is illustrated in Fig. 1.

In general, the FBAW offers less flexibility than does its SAW counterpart. Its main advantage is the ability to integrate multiple FBAWs with electronic circuitry, where they can be used as high-Q circuit elements in filters having passband frequencies of up to $\sim$10 GHz.

3. SAW DEVICE STRUCTURES

3.1. SAW Delay Line

A SAW delay line, illustrated in Fig. 2, is the simplest device of its type. It consists of two thin-film metallic transducers placed on the surface of a piezoelectric substrate. Common substrates are listed in Table 1. The transducers are usually created using a single-step photolithographic process and are made of a light metal such as aluminum to minimize the effect of their mass on the substrate. The

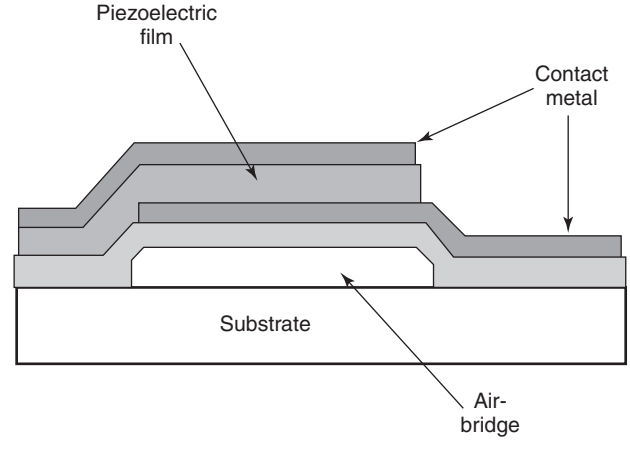

Figure 1. FBAW resonator structure.

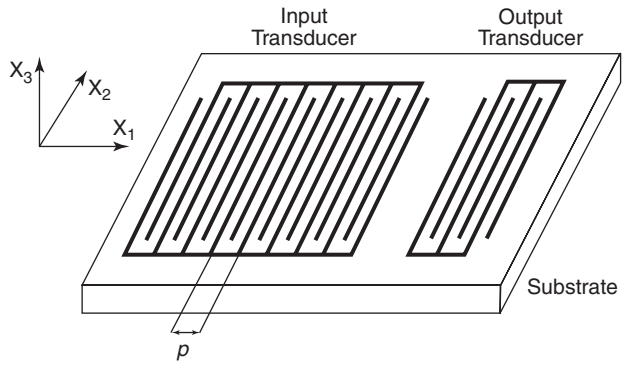

Figure 2. SAW delay line.

photolithographic resolution in the fabrication process limits the frequency of operation of SAW delay lines, where an achievable linewidth of 0.5 μm limits the frequency of operation to ~2 GHz.

The principal benefit of employing SAW devices as delay lines is the large group delays that are possible. For example, a device having a distance (center to center) between transducers of 0.5 cm would produce a delay in the order of 1.5 μs. In addition, because the wave velocity is frequency-independent, this delay would apply to all frequency components that the device supports.

The structure of the transducers varies, but the most common type by far is the *interdigital transducer* (IDT), which consists of an array of parallel strips ("fingers") of alternating polarity. When a RF signal is applied to the input IDT, the electric fields between the metal strips induce mechanical deformations that propagate as waves in the crystal. These waves in turn generate an electric potential between the strips in the output IDT, which produces a current in the load.

The frequency response of the device can be estimated by recognizing that a modulated pulse can approximate the impulse response of each IDT. The frequency response for a device having two identical transducers is thus

$$|H(f)| \approx A \left| \frac{\sin\left[\dfrac{N\pi(f-f_0)}{f_0}\right]}{\dfrac{N\pi(f-f_0)}{f_0}} \right|^2 \tag{1}$$

where A is a constant and N is the number of finger pairs in each transducer. f_0 is the device's center frequency given by

$$f_0 = \frac{v}{p} \tag{2}$$

Here, v is the acoustic wave phase velocity in the transducer region and p is the finger periodicity, shown in Fig. 2.

The insertion loss of a SAW delay line is often high. Since both IDTs are bidirectional three-port (one electrical, two acoustic) devices, each IDT will contribute an inherent 3 dB loss (6 dB in total) when the two electrical ports are matched to the source and load, respectively. This matched condition unfortunately also results in the maximum level of acoustic wave regeneration by each IDT, and leads to severe multipath interference known as *triple-transit interference* (TTI). Consequently, most SAW delay lines are intentionally mismatched at the electrical ports so that acoustic regeneration is reduced. An insertion loss of between 20 and 30 dB is common.

The frequency response of SAW delay lines usually exhibits several other distortions attributed to second-order effects. The dominant effects are direct electromagnetic coupling ("feedthrough") between input to output transducers, reflections from finger edges, acoustic beam diffraction, and bulk wave interference.

3.2. SAW Transversal Filter

The SAW transversal filter is a generalization of the delay line in which the relative efficiency of individual IDT fingers is varied so that the frequency response of the transducer can be tailored. The control is commonly achieved either by *apodization*, which consists of varying the individual finger lengths, or by *withdrawal weighting*, which involves selectively removing fingers. These techniques are illustrated in the device shown in Fig. 3.

In a first-order design process, each finger in an IDT is represented by a delta function whose magnitude is proportional to the length. The impulse response of the IDT is then a sequence of weighted delta functions separated by $\tau = p/2v$ seconds. This representation corresponds directly to the one commonly used for the design of finite-impulse-response (FIR) digital filters, for which there are extensive design tools. One of the most common of these tools is the Remez exchange algorithm, for which computer programs are readily available [2], but other optimization algorithms can also be used. Once the equivalent digital FIR filter has been designed, the SAW filter is obtained by making the finger lengths proportional to the tap weights of the digital filter. If the transducer has an impulse response that is symmetric, then its frequency response will exhibit a linear phase. This property is important in communications applications.

Care must be exercised when designing a SAW filter having two apodized transducers. Since in this case the acoustic beam generated by the first apodized transducer will not be uniform across acoustic aperture, the signal detected by each finger in the second transducer will seldom be proportional to its length. Because of the

Table 1. Common Substrates Used in Surface Acoustic Wave Devices

Substrate	Cut	Velocity v (m/s)	k^2 (%)	Temperature Coefficient (ppm/K)
Quartz	ST-X	3158	0.116	0
Lithium niobate	Y-Z	3488	4.82	+94
Lithium niobate	128°-X	3992	5.44	+75
Lithium tantalate	Y-Z	3230	0.66	+35

Source: Morgan [17].

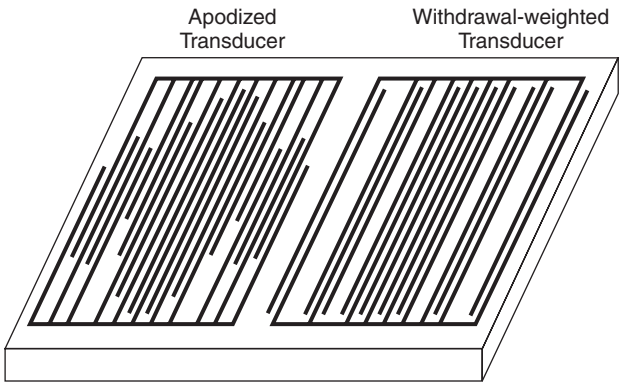

Figure 3. SAW device employing an apodized transducer and a withdrawal-weighted transducer.

difficulties that this behavior introduces in the design process, the second transducer is rarely apodized. In this case, withdrawal weighting is an attractive option.

3.3. Dispersive SAW delay line

Both the SAW delay line and transversal filter are usually designed to have a linear phase response. There are situations, however, where a nonlinear phase response is desirable. For example, a frequency-modulated ("chirp") impulse response is often used to improve the range and resolution of radar systems.

A dispersive SAW delay line can be made by varying the finger positions of a delay line. Alternatively, grooves of varying periodicity can be etched into the substrate, as shown in Fig. 4, to create a *reflective array compressor* (RAC) [3]. The various frequency components in the acoustic beam will be reflected efficiently in the region where the grooves have a periodicity equal to half the acoustic wavelength. The frequency components will thus travel different distances and will reach the output tranducer with differing delays. The phase response of the filter is obtained by integrating the radial frequency with respect to time, so a nonconstant delay can produce a desired nonlinear phase response.

3.4. Single-Mode SAW Resonator

An array of metal strips or grooves on the surface of the substrate can reflect SAW energy. If we place such arrays on the far sides of a one- or two-transducer device as shown in Fig. 5, we can create an acoustic resonant cavity. Resonance will occur, and the acoustic energy will be trapped in the cavity when the acoustic wave has a

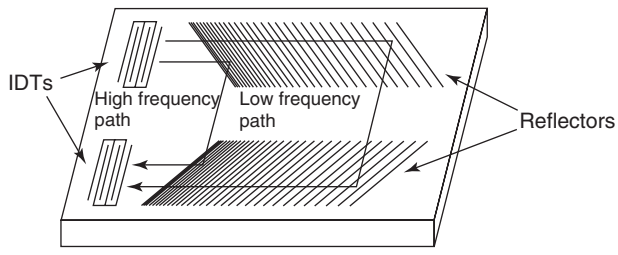

Figure 4. Reflective array compressor (RAC).

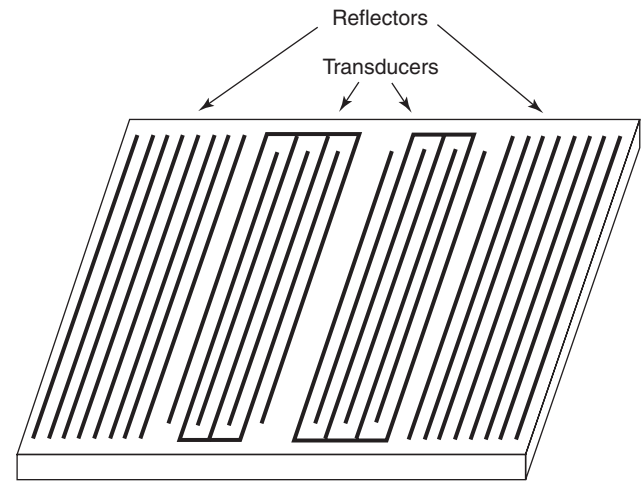

Figure 5. SAW resonator.

wavelength that is approximately equal to an even multiple of the reflector strip periodicity.

When properly designed, a SAW resonator can achieve a quality factor, measured as the inverse of the fractional bandwidth, equal to about 10,000. In addition, the SAW resonator usually has a low insertion loss because the acoustic energy is trapped in the cavity. An insertion loss of less than 2 dB is easily achievable.

3.5. Multimode SAW Resonator

If we allow the acoustic energy in two identical resonant cavities to couple, the resonant frequency of the combined structure will split into two resonant frequencies. This property is often used to produce resonators that exhibit a higher fractional bandwidth than do single-cavity resonators, while still maintaining their low insertion loss.

The resonators can be longitudinally coupled, in which case two acoustic cavities are placed in line and the reflector array that they share is shortened to allow the acoustic energy to "leak" into the adjacent cavity. This approach allows the designer to precisely control the coupling between the cavities. Alternatively, the cavity length can be increased sufficiently to permit two or more modes to exist within the single cavity. However, at frequencies not reflected by the reflector arrays, the SAW waves will be able to freely propagate between transducers in these inline structures. This leads to poor out-of-band rejection.

The resonators may also be transversely coupled. In this case the acoustic cavities are placed in parallel, with a very narrow gap (usually a grounded metal strip) between them. Acoustic energy is coupled between the cavities through the evanescent "tail ends" of the transverse energy distribution of each cavity. This approach gives limited control over the coupling between cavities, but leads to excellent out-of-band rejection, in the order of 60 dB.

3.6. Low-Loss Structures

The previous paragraphs have described many "first generation" SAW devices, which can be divided into high-loss filters with outstanding frequency response

characteristics, and low-loss narrowband resonant devices with responses over which the designer has limited control. A "second generation" type of device has emerged that can provide both low loss and control over the shape of the frequency response.

Designing transducers that launch acoustic energy primarily at one port can reduce the insertion loss. This is done by introducing wave reflections within each IDT that add in phase with waves propagating in the desired direction, but that add out of phase with waves propagating in the opposite direction. Since the standard IDT is symmetric, it cannot generate unsymmetric output unless the substrate is unsymmetrical. We must employ instead transducers that have multiple electrodes, often of varying width, per period. Several examples of structures, known as *single-phase unidirectional transducers* (SPUDTs), are given in Ref. 4. These devices require higher photolithographic resolution, and their fabrication presents difficulties at frequencies above 1 GHz.

A second approach to reducing the insertion loss is to employ multiple bidirectional transducers that are alternatingly connected to the input and output ports. Since each input transducer (unless located at the ends) has a receiving transducer at both acoustic ports, and since each output transducer (unless located at the ends) has a transmitting transducer at each port, very little acoustic energy is lost. These devices, known as *interdigitated interdigital transducers* (IIDTs), are not subject to the same fabrication limitations at high frequencies as the devices described in the previous paragraph, but they often exhibit severe ripples in the frequency response.

3.7. SAW Ladder Networks

One-port SAW resonators have been increasingly used as circuit elements in ladder networks [5]. These filters, known as *impedance element filters*, offer low insertion loss and high power-handling capability. They are therefore often used in the output stage of wireless transceivers.

The basic configuration for an impedance element filter is given in Fig. 6, which also shows the typical frequency response of the circuit elements. The resonant frequencies of the shunt and series elements are offset so that the antiresonant frequency of the shunt elements matches the resonant frequency of the series elements. The result is a filter with a wider bandwidth than achievable with individual resonators, with sharp transition bands and good close-in stopband suppression.

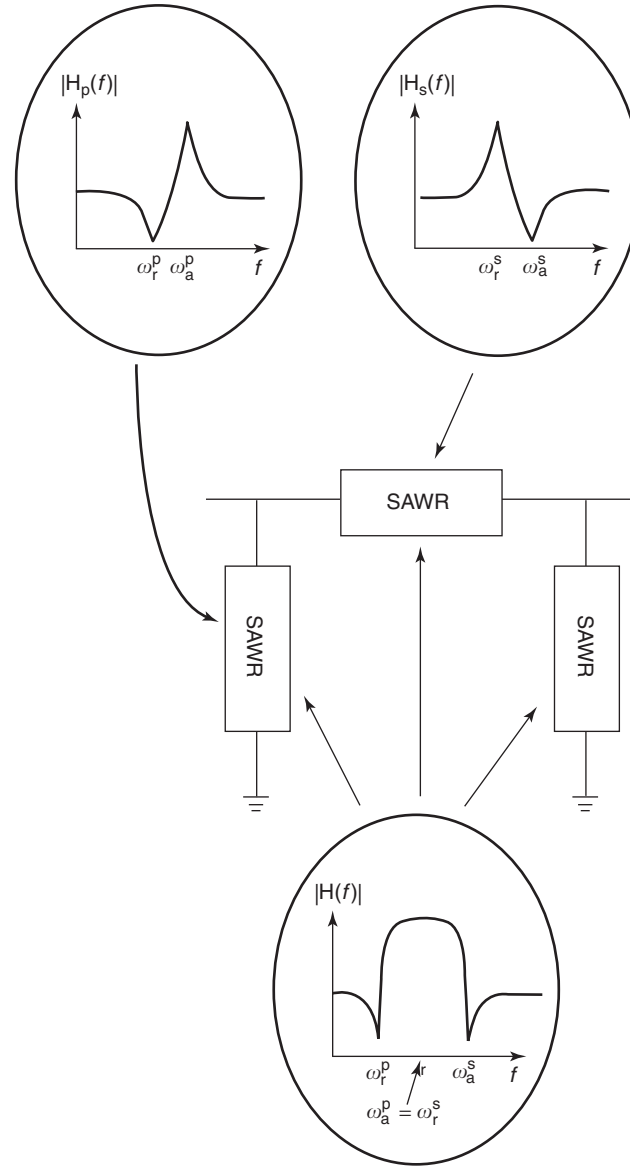

Figure 6. Configuration of impedance element filter employing SAW resonators.

4. SUBSTRATES

4.1. SAW Substrates

At low frequencies, most BAW devices employ a cylindrical quartz crystal that is polished on the two faces, on which are placed metal electrodes. Since the fundamental resonant frequency is inversely proportional to the distance between the two faces, the crystal becomes extremely thin at high frequencies, and impractical at microwave frequencies.

In the case of the FBAW, the thin-film piezoelectric substrate must be easily deposited and processed. The most commonly used materials are aluminum nitride (AlN) and zinc oxide (ZnO).

4.2. SAW Substrates

There are currently many substrates in use for SAW devices. The most common are lithium niobate ($LiNbO_3$), quartz (SiO_2), and lithium tantalate ($LiTaO_3$), which are cut at various angles to the crystalline axes. Table 1 summarizes the most important properties of some of the more common crystal cuts.

The phase velocity v of the wave, combined with the photolithographic resolution of device fabrication process, determine the maximum sampling frequency of the transducers. Clearly, since IDT electrodes must be at most half a wavelength apart, a high velocity is desirable at microwave frequencies.

The coupling coefficient k^2 provides an indication of the electromechanical coupling efficiency. It is computed by evaluating the fractional velocity difference between waves propagating under metallized and free surfaces. Filters built on substrates with a higher k^2 can achieve lower insertion loss and wider bandwidths.

The temperature coefficient determines the effect of temperature changes on the acoustic phase velocity. This parameter is particularly important in oscillator applications where the cost of controlling the substrate temperature is excessive.

In general, $LiNbO_3$ crystals are used for wideband devices such as transversal filters, where the device may be placed in a temperature-controlled environment, or where small passband shifts due to temperature variations are of minor concern.

Quartz is usually preferred for narrowband applications, such as for resonators to be used in oscillators, where minor frequency shifts due to temperature variations are of major concern. The ST-X cut of quartz, with its zero first-order temperature coefficient at room temperature, is ideal for this type of application.

$LiTaO_3$ is often selected as a compromise between the two other substrates. Its temperature coefficient is lower than that of $LiNbO_3$, but its coupling coefficient is higher than for quartz.

There has been considerable interest in the use of multilayer substrates. A substrate that shows great promise is diamond because of its hardness, which leads to a high acoustic velocity. Since it is not piezoelectric, the diamond substrate must be layered with a piezoelectric thin film such as zinc oxide (ZnO). Nakahata reported that a silicon substrate coated with diamond and ZnO films can support a SAW having a velocity of 10,500 m/s and an electromechanical coupling coefficient k^2 of 1.5% [6]. Commercial diamond-based SAW devices operating well above 2 GHz are now available.

5. APPLICATIONS

5.1. Nyquist Filter

Consider a communication system designed to transmit digital bits (assume that each bit is transmitted as a delta function for now) every T seconds. The frequency response of the transmitted information must be restricted to the available channel bandwidth, which makes the impulse response of the channel infinite in length. Unless special steps are taken, successive bits will produce intersymbol interference (ISI). The solution is usually to employ a Nyquist filter in the transmitter.

To minimize this interference, it is important that the channel's impulse response be zero at all sampling instances $t = T_0 + nT$, $n \neq 0$, where T_0 is the delay through the channel. A channel with an ideal rectangular frequency response and a bandwidth of $1/T$ Hz would have a sinc impulse response

$$\text{sinc}\left(\frac{t}{T}\right) = \frac{\sin(\pi t/T)}{\dfrac{\pi t}{T}} \tag{3}$$

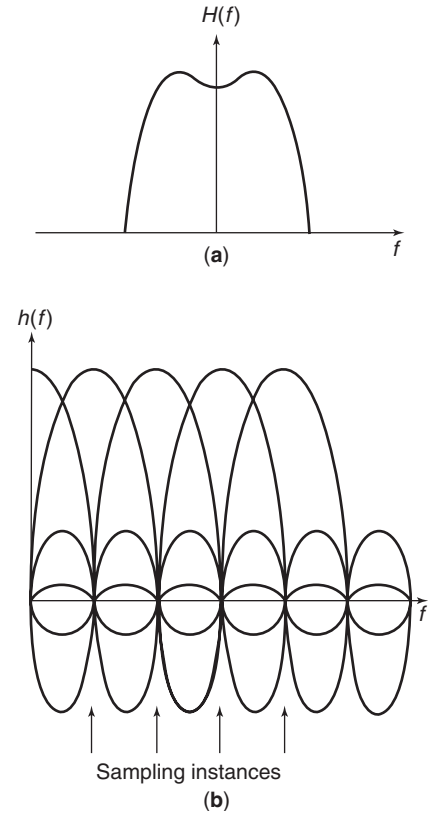

Figure 7. (a) Raised-cosine Nyquist filter frequency response; (b) impulse response of Nyquist filter.

which has the desired property. Other functions, such as the *raised-cosine function* [7], have the same property and are easier to realize. Any deviation from these precise frequency responses by the channel filter will quickly degrade the performance of the system.

The frequency response of the channel filter must be modified to account for the frequency response of the transmitted bit, which in practice cannot be a true delta function. If we assume a rectangular bit (with its sinc-shaped frequency response), a corresponding 1/sinc response must be superimposed on the frequency response of the channel filter. The resulting frequency response and its time-domain properties are illustrated in Fig. 7.

Because of their performance, reproducibility, and their ability to operate at intermediate frequencies (so that a single filter can operate on the combined in-phase and quadrature signals instead of requiring a baseband filter for each of these signals), SAW filters are often used in these applications [8].

5.2. Satellite Subchannelizers

Satellites usually have several transponders, and these are often leased to users. For example, the standard bandwidth of a C-band (6/4-GHz) satellite channel is 40 MHz, of which 36 MHz is usable because of the required guard bands between channels. In a conventional system, the user must lease the entire channel, regardless of whether the bandwidth is needed. The high cost of leasing the entire channel can be a major deterrent.

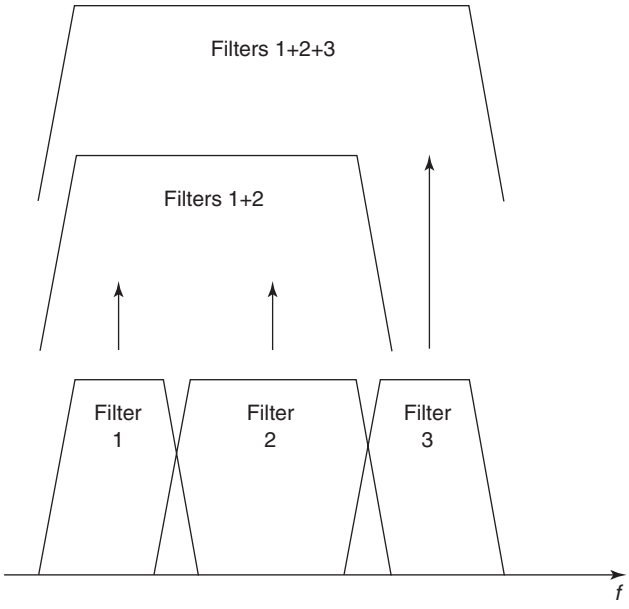

Figure 8. Filters in a SAW filter-bank seamlessly combine to dynamically vary channel bandwidth.

The high selectivity of SAW filters makes it possible to divide the satellite channel into three or more subchannels, possibly of varying bandwidth. Furthermore, if the magnitude and phase of these filters are carefully controlled, it is possible to combine two or more of these subchannels to form a contiguous channel of higher bandwidth, up to the full bandwidth of the transponder. Such a system is illustrated in Fig. 8. The Inmarsat-3 satellite uses this type of system to service its mobile users [9].

5.3. Wireless Handsets

Wireless communications systems require inexpensive, rugged, and compact components that consume very little power. Low-loss SAW devices excel in all four attributes, and have been widely adopted by all major manufacturers [10]. Cellular telephones are currently the largest market for SAW devices, at over 1 billion units per year.

SAW longitudinally coupled resonator filters are often used in the front end to remove out-of-band signal interference. A waveguide-coupled resonator filter is then used to select the desired channel. Figure 9 illustrates the possible uses of SAW components in a wireless handset.

5.4. SAW Oscillators

Stable oscillators require a narrowband device in their feedback path whose passband frequency can be precisely established. The frequency response of the device should also present a low insertion loss and be highly stable. Finally, for volume applications, the response must be easily reproducible.

SAW resonators meet all of these requirements, and are lightweight and rugged. When compared to other technologies, they can be manufactured at a low cost. For these

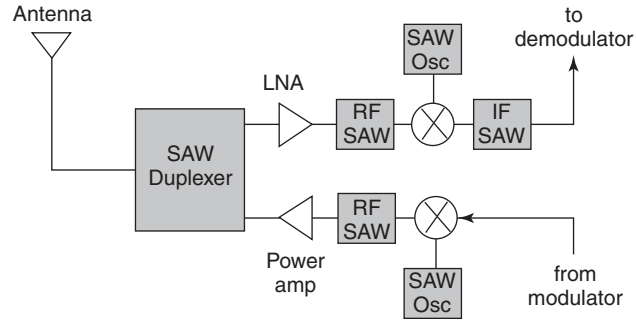

Figure 9. Block diagram of a wireless transceiver. Shaded blocks routinely use SAW devices.

reasons, SAW oscillators are widely used whenever signals in the range from 50 MHz to 2 GHz are required.

Oscillator stability is usually categorized as either short- or long-term. *Short-term stability* refers to output frequency variations lasting less than 1 s and caused by random thermal vibrations and the discrete nature of electric charge. *Long-term stability* encompasses effects due to temperature variations and component aging.

Short-term stability can be improved by selecting a high-Q feedback filter, an amplifier with low flicker noise and noise factor, and a clean power supply. In the case of SAW oscillators, it is also important to isolate the SAW device from mechanical vibrations, since the piezoelectric substrate can convert the vibrations to electrical signals. Short-term stability is usually measured in terms of single-sideband phase noise, which describes the oscillator output power density, normalized to the power of the carrier, at specific offset frequencies. A 500-MHz SAW oscillator, for example, is typically able to achieve phase noise levels of –130 dBc/Hz at 1 kHz offset from the carrier (dBc refers to decibels with respect to the carrier). The phase noise then typically drops to about –175 dBc/Hz at 100 kHz offset, and levels off [11].

Long-term stability can be improved by placing the oscillator in a temperature-controlled environment. Placing the SAW device in a package with thermal characteristics that are similar to those of the substrate also helps reduce mechanical stresses. Because component aging occurs predominantly early in its life, it is also important to "burn in" all oscillator components by subjecting them to high signal levels and high temperatures for an extended period of time. SAW oscillator long-term stability is usually measured in parts per million (ppm), and a good design can achieve 1 ppm per year at a fixed temperature or about 20 ppm over a temperature variation of 50 K.

5.5. SAW Chirp Fourier Transformer

The SAW chirp Fourier transformer is an analog circuit that is able to perform a finite-bandwidth windowed Fourier transform. The circuit is based on a simple algebraic manipulation of the formula for the Fourier transform $S(\omega)$ of a time signal $s(t)$:

$$S(\omega) = \int_{-\infty}^{\infty} s(t) e^{-j\omega t}\, dt \tag{4}$$

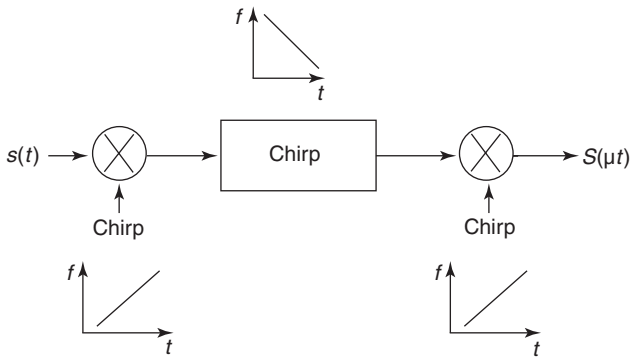

Figure 10. A multiply-convolve-multiply SAW Fourier transformer.

Substituting $-2\omega t = (t-\omega)^2 - t^2 - \omega^2$ and $\omega = \mu t$, we obtain

$$S(\omega) = S(\mu t) = e^{-j(\mu/2)t^2} \int_{-\infty}^{\infty} (s(\tau)e^{-j(\mu/2)\tau^2})e^{j(\mu/2)(t-\tau)^2}\, d\tau \quad (5)$$

This expression can clearly be represented by the circuit shown in Fig. 10, which involves a multiplication by a linear frequency-modulated (FM) signal, followed by a convolution with another FM signal having a frequency variation opposite that of the first. The output of the convolver is then multiplied by a third FM signal having the same frequency variation as that of the first signal. A similar transformation can show that the dual circuit, consisting of a convolve–multiply–convolve system, produces the same result.

In a practical system, the convolutions can be performed by feeding the signal into a SAW chirp filter having a linear group delay. The multiplying signals can be provided by impulsing SAW chirp filters, but are usually generated digitally because this approach makes it easier to compensate for imperfections in the convolving SAW chirp filters.

While the SAW chirp Fourier transformer has not been widely used in commercial applications, studies have shown that it could be very competitive in some communications satellite applications [12].

6. ACOUSTIC WAVE PROPAGATION

A solution to the acoustic wave propagation in a piezoelectric substrate requires that both Maxwell's and Newton's equations be solved simultaneously in a nonisotropic medium. These two sets of equations are linked through the piezoelectric relationships. The equations that rule the behavior are

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} = -\boldsymbol{\mu}\frac{\partial \mathbf{H}}{\partial t} \quad (6)$$

$$\nabla \times \mathbf{H} = \frac{\partial \mathbf{D}}{\partial t} = \frac{\partial}{\partial t}(\boldsymbol{\varepsilon}^T\mathbf{E} + \mathbf{dT}) \quad (7)$$

$$\nabla_s \mathbf{v} = \frac{\partial \mathbf{S}}{\partial t} = \frac{\partial}{\partial t}(\mathbf{d}'E + \mathbf{s}^E\mathbf{T}) \quad (8)$$

$$\nabla \cdot \mathbf{T} = \boldsymbol{\rho}\frac{\partial \mathbf{v}}{\partial t} \quad (9)$$

where

$\mathbf{B}$ = magnetic flux density vector
$\mathbf{d}$ = (3×6) piezoelectric strain coefficient matrix
$\mathbf{D}$ = electric flux density vector
$\mathbf{E}$ = electric field vector
$\boldsymbol{\varepsilon}^T$ = (3×3) electric permittivity matrix
$\mathbf{H}$ = magnetic field vector
$\boldsymbol{\mu}$ = (3×3) magnetic permeability matrix
$\mathbf{s}^E$ = (6×6) compliance coefficient matrix
$\mathbf{S}$ = strain vector
$\mathbf{T}$ = stress vector
$\boldsymbol{\rho}$ = diagonal (3×3) material density matrix
$\mathbf{v}$ = particle velocity vector = $\partial\mathbf{u}/\partial t$
$\mathbf{u}$ = particle displacement vector

Here, $\nabla\times$ represents the curl and the prime refers to the transpose of a matrix. Assuming the standard abbreviated subscript notation described in Ref. 13, we have

$$\nabla\cdot = \begin{bmatrix} \frac{\partial}{\partial x} & 0 & 0 & 0 & \frac{\partial}{\partial z} & \frac{\partial}{\partial y} \\ 0 & \frac{\partial}{\partial y} & 0 & \frac{\partial}{\partial z} & 0 & \frac{\partial}{\partial x} \\ 0 & 0 & \frac{\partial}{\partial z} & \frac{\partial}{\partial y} & \frac{\partial}{\partial x} & 0 \end{bmatrix} = (\nabla_s)' \quad (10)$$

$$\nabla\times = \begin{bmatrix} 0 & -\frac{\partial}{\partial z} & \frac{\partial}{\partial y} \\ \frac{\partial}{\partial z} & 0 & -\frac{\partial}{\partial x} \\ -\frac{\partial}{\partial y} & \frac{\partial}{\partial x} & 0 \end{bmatrix} \quad (11)$$

The wave solutions obtained by solving these equations, subject to boundary conditions, can be classified by their propagation properties. The most common types are bulk waves, Rayleigh waves, Bluestein–Gulyaev waves, and leaky waves.

6.1. Bulk Waves

Bulk acoustic waves are waves that propagate in the interior of the substrate, so that they are subject to the substrate boundary conditions only when they strike the boundaries. A bulk wave will in general have a particle motion that is composed of a superposition of three fundamental modes. These are known as the *fast longitudinal wave*, whose particle motion is in the same direction as the wave, and two *slower transverse waves*, whose particle motions are perpendicular to the wave. The latter are usually termed *fast-shear* and *slow-shear* waves, owing to their different phase velocities (in some crystal directions, these two waves could have the same velocity). Since these components travel independently, their relative magnitudes and phases will be determined by the launching conditions. In a piezoelectric substrate, each of these wave components will have a phase velocity that depends on its propagation direction.

6.2. Rayleigh Waves

Rayleigh waves satisfy the Maxwell and Newton equations in a piezoelectric half-space. Their motion is retrograde elliptical in the sagittal plane (defined by axes x_1, x_3 in Fig. 2), and their velocity is lower than that of all other waves. This slow velocity leads to very low propagation loss because the acoustic power is confined to within about 1 wavelength of the surface and does not leak into the substrate.

6.3. Bluestein–Gulyaev Waves

Bluestein–Gulyaev waves, also called *surface transverse waves* (STWs), contain particle motion only in the x_2 direction and can be generated with the traditional IDT structure. In general, the energy will propagate at a nonzero angle to the surface, which makes the wave lossy. However, if the surface is subjected to a periodic stress, the STW can be guided parallel to the surface so that it behaves very much like a surface wave; it is then called a *surface-skimming bulk wave* (SSBW). IDTs or reflector arrays built with a heavier or thicker metal film are usually used to guide the wave.

For particular substrate cuts, STW or SSBW can be the dominant acoustic modes. They have a higher velocity than do Rayleigh waves, so they are sometimes used instead of their Rayleigh counterparts in high-frequency devices.

6.4. Leaky Waves

For some substrates, it is possible to satisfy the surface boundary conditions with waves that travel at a velocity that is higher than that of the slow shear wave. Such waves are referred to as "leaky waves" because they are not confined to the surface and their acoustic energy leaks into the substrate. However, in some cases their electromechanical coupling coefficient is higher than that for Rayleigh waves and their propagation loss is small enough to make them practical. In addition, many of these substrates offer very small temperature coefficients. For these reasons, leaky waves are being increasingly used, particularly at high frequencies.

7. DEVICE MODELS

7.1. Introduction

Attempts to accurately model surface wave devices have met with varying success. The electromechanical interactions that are central to their operation require that both Maxwell's and Newton's equations be solved for the given boundary conditions. Until recently (as of 2003), the computational requirements to fully model even the simplest devices have been excessive. As a result, varying levels of simplification have been adopted in order to generate useful design tools. Effects that have not been predictable with these simplified models have been classified as "second-order effects," with several techniques used to minimize their effect on the desired behavior of the device [14].

7.2. Impulse Response Model

The impulse response model was first derived by Hartmann et al. [15] as an alternative to more complicated equivalent circuit approaches. It provides more information on a SAW device's performance than does the delta function model described by Eq. (1) because it includes information on electrical impedances and can cater to transducers with nonuniform electrode spacing.

The process of modeling a SAW device with the impulse response model involves three steps:

1. Each electrode is replaced with a half-cycle of a sine wave whose magnitude is proportional to the length of the electrode.
2. If electrode spacing is not uniform, then the magnitude of each ith half-cycle is further scaled by $f_i^{3/2}$, where f_i is the instantaneous frequency at that point in the transducer.
3. The frequency response is obtained by taking the Fourier transform of the resulting impulse response. This technique is illustrated in Fig. 11.

The input impedance of a transducer can be computed from the impulse response model through energy conservation arguments. The equivalent circuit consists of a radiation conductance, representing acoustic energy generation, in parallel with a radiation susceptance, corresponding to energy absorption and regeneration in the transducer, and with a static capacitance. The radiation conductance of an IDT with uniformly spaced electrodes is found to be

$$G_a(f) = 8k^2 C_s f_0 N^2 \left| \frac{\sin\left[\dfrac{N\pi(f-f_0)}{f_0}\right]}{\dfrac{N\pi(f-f_0)}{f_0}} \right|^2 \tag{12}$$

while the radiation susceptance is the Hilbert transform of $G_a(f)$ and is given by

$$B_a(f) = 8k^2 C_s f_0 N^2 \frac{\sin\left[\dfrac{2N\pi(f-f_0)}{f_0}\right] - \dfrac{2N\pi(f-f_0)}{f_0}}{2\left[\dfrac{N\pi(f-f_0)}{f_0}\right]^2} \tag{13}$$

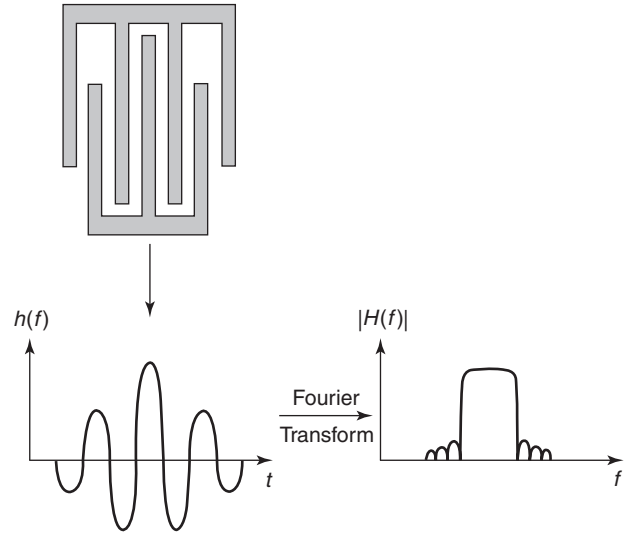

Figure 11. Impulse response model of a transducer.

The static capacitance for the transducer is

$$C_t = NC_s \tag{14}$$

In Eqs. (12) through (14), k^2 is the electromechanical coupling constant, C_s is the capacitance per finger pair, and N is the number of finger pairs in the transducer. The equivalent circuit values for transducers with nonuniformly spaced electrodes can be found in Ref. 15.

7.3. Coupling-of-Modes Model

The *coupling-of-modes* (COM) model is a phenomenological description of the behavior of propagating waves that are subjected to a periodic disturbance in their propagation medium. The technique is ideally suited to the computation of the behavior of SAW structures that contain a large number of equally spaced transducer fingers or reflector strips. The COM approach is very numerically efficient, but is only accurate over fractional bandwidths of about 10%. It also must be slightly modified to model devices that employ leaky waves.

Consider two sinusoidal waves having complex amplitudes $w^+(x)$ and $w^-(x)$ propagating in a transducer region in the $+x_1$ and $-x_1$ directions shown in Fig. 2, respectively. Because of reflections and acoustic generation at the electrodes, these waves will be coupled to each other so that

$$\begin{aligned}
\frac{\partial w^+(x)}{\partial x} &= -j\delta w^+(x) + j\kappa w^-(x) + j\alpha V \\
\frac{\partial w^-(x)}{\partial x} &= j\delta w^-(x) - j\kappa^* w^+(x) - j\alpha^* V \\
\frac{\partial I(x)}{\partial x} &= -2j\alpha^* w^+(x) - 2j\alpha w^-(x) + j\omega C_0 V
\end{aligned} \tag{15}$$

where κ is the distributed reflection coefficient, α is the distributed transduction coefficient, V is the applied voltage, ω is the radian frequency, C_0 is the static capacitance per unit length of the transducer, and δ is a measure of frequency deviation from the Bragg frequency given by

$$\delta = \beta - \frac{\pi}{a} \tag{16}$$

where β is the propagation constant and a is the electrode separation. The terms containing V and the equation for the incremental current $I(x)$ can be disregarded when dealing with reflector arrays.

If we write Eq. (15) in matrix form, we obtain

$$\begin{aligned}
\frac{\partial \mathbf{w}(x)}{\partial x} &= \mathbf{C}\mathbf{w}(x) + \mathbf{f}V \\
\frac{\partial I(x)}{\partial x} &= \mathbf{N}\mathbf{w}(x) + j\omega C_0 V
\end{aligned} \tag{17}$$

where

$$\mathbf{w}(x) = \begin{bmatrix} w^+(x) \\ w^-(x) \end{bmatrix}, \quad \mathbf{C} = \begin{bmatrix} -j\delta & j\kappa \\ -j\kappa^* & j\delta \end{bmatrix}, \quad \mathbf{f} = \begin{bmatrix} j\alpha \\ -j\alpha^* \end{bmatrix}$$

and $\mathbf{N} = [-2j\alpha^* \ -2j\alpha]$, the general solution for the waves is

$$\mathbf{w}(x) = \mathbf{V}_e\mathbf{E}(x)\mathbf{V}_e^{-1}\mathbf{w}(0) + (\mathbf{V}_e\mathbf{E}(x)\mathbf{V}_e^{-1} - \mathbf{II})\mathbf{C}^{-1}\mathbf{f}V \tag{18}$$

where $\mathbf{V}_e$ is the 2×2 matrix containing the eigenvectors of $\mathbf{C}$ in its columns. $\mathbf{II}$ is the 2×2 unit matrix, and

$$\mathbf{E}(x) = \begin{bmatrix} e^{\lambda_1 x} & 0 \\ 0 & e^{\lambda_2 x} \end{bmatrix} \tag{19}$$

for which λ_1 and λ_2 are the eigenvalues of $\mathbf{C}$ [16]. In the case of transducers, the solution requires an expression for the current, which is obtained by integrating the incremental current over the length of the transducer. For a transducer of length L_T, we get

$$\begin{aligned}
I = \mathbf{N}\mathbf{V}_e\mathbf{\Lambda}^{-1}(\mathbf{E}(L_T) - \mathbf{II})\mathbf{V}_e^{-1}\mathbf{w}(0) + \{\mathbf{N}[\mathbf{V}_e\mathbf{\Lambda}^{-1}(\mathbf{E}(L_T) - \mathbf{II})\mathbf{V}_e^{-1} \\
+ L_T\mathbf{II}]\mathbf{C}^{-1}\mathbf{f} + j\omega C_t\}V
\end{aligned} \tag{20}$$

where $C_t = xC_0$ is the total static capacitance of the transducer and

$$\mathbf{\Lambda} = \begin{bmatrix} \lambda_1 & 0 \\ 0 & \lambda_2 \end{bmatrix} \tag{21}$$

The admittance parameters for the device can be computed as

$$y_{ij} = \left.\frac{I_i}{V_j}\right|_{V_k = 0, k \neq j} \tag{22}$$

where the subscripts identify the transducers in the device. Scattering parameters are then obtained from the admittance parameters by using standard transformations.

7.4. Green's Function Model

The Green's function models for SAW devices were first developed in the 1970s, with many simplifications applied to make the numerical computations tractable with the resources available at that time. The most common assumption at that time was that the substrate interface was stress-free [17]. The technique has attracted considerable attention more recently because of its ability to model essentially all aspects of a SAW device's performance and to take into account all acoustic propagation modes.

A Green's function describes the behavior of a structure due to a point source. This source can be an electrical charge on the surface of the substrate, or a mechanical stress due to, for example, the mass of a surface electrode. In the k domain (corresponding to the Fourier transform of these terms), these relationships can be summarized as

$$\begin{bmatrix} \bar{u}_1(k_1) \\ \bar{u}_2(k_1) \\ \bar{u}_3(k_1) \\ \bar{\phi}(k_1) \end{bmatrix} = \begin{bmatrix} \bar{G}_{11}(k_1) & \bar{G}_{12}(k_1) & \bar{G}_{13}(k_1) & \bar{G}_{14}(k_1) \\ \bar{G}_{21}(k_1) & \bar{G}_{22}(k_1) & \bar{G}_{23}(k_1) & \bar{G}_{24}(k_1) \\ \bar{G}_{31}(k_1) & \bar{G}_{32}(k_1) & \bar{G}_{33}(k_1) & \bar{G}_{34}(k_1) \\ \bar{G}_{41}(k_1) & \bar{G}_{42}(k_1) & \bar{G}_{43}(k_1) & \bar{G}_{44}(k_1) \end{bmatrix} \times \begin{bmatrix} \bar{T}_5(k_1) \\ \bar{T}_4(k_1) \\ \bar{T}_3(k_1) \\ \bar{D}_3(k_1) \end{bmatrix} \tag{23}$$

where the overbar indicates a Fourier transform. G_{ij} are Green's functions, ϕ is the electric potential, and u_i, T_i, D_3 are elements of the displacement, stress, and electric flux density vectors, respectively.

A convenient method to evaluate all the Green's functions was proposed by Peach [18]. For an assumed x_1 component of the acoustic wavenumber given by k_1, the possible x_3 components can be evaluated by solving Eqs. (6)–(9). The solution can be written as an eighth-order eigenvalue problem, where the k_3 terms are the eigenvalues, and the eigenvectors are the partial waves that make up the solution. The boundary conditions determine the relative contributions of these partial waves. The $\bar{G}_{ij}(k_1)$ terms are then readily obtained.

The singular terms in the $\bar{G}_{ij}(k_1)$ functions must be quantified so that the spatial domain Green's functions $G_{ij}(x_1,\omega)$ can be obtained. This step is often the most time consuming, but it is necessary because these singular points determine the long-range effect of the sources. The spatial domain Green's functions are then convolved over all sources and the overall device behavior is obtained.

Recently, a periodic Green's function methodology was introduced that is well suited to the analysis of long periodic structures [19]. This approach limits the analysis to that of a single period, which greatly reduces the computation requirements.

7.5. Finite-Difference Time-Domain Model

The finite-difference time-domain (FDTD) method was first introduced by Yee for the simulation of electromagnetic wave propagation [20]. It involves the discretization of the wave equations in both time and space, which then leads to a numerical solution of the wave propagation problem. The technique's main benefits are that it permits the description of wave propagation in nonuniform and nonlinear media, and it can easily include a wide range of boundary conditions. The technique is particularly well suited to broadband analyses, because the spectral response can be computed from the structure's time response to a narrow Gaussian impulse excitation.

There has been some early work on the extension of the method to the propagation of ultrasonic waves through piezoelectric media [21]. Stability considerations require that a quasistatic approximation be imposed on Eqs. (6)–(9), so that they can be reduced to

$$\nabla_s \mathbf{v} = \hat{\mathbf{s}}^E \frac{\partial \mathbf{T}}{\partial t} \tag{24}$$

$$\nabla \cdot \mathbf{T} = \boldsymbol{\rho} \frac{\partial \mathbf{v}}{\partial t} \tag{25}$$

where the stiffened compliance matrix is defined as

$$\hat{\mathbf{s}}^E = \mathbf{s}^E - \mathbf{d}'(\boldsymbol{\varepsilon}^T)^{-1}\mathbf{d} = (\hat{\mathbf{c}}^E)^{-1} \tag{26}$$

In the saggital plane, the resulting time-stepping equations become

$$-\mathbf{V}\big|_{i+(1/2),\,j+(1/2)}^{n+(1/2)} = \mathbf{V}\big|_{i+(1/2),\,j+(1/2)}^{n-(1/2)} + \frac{\Delta t}{2\rho\Delta x}\,\hat{\mathbf{T}}\big|_{i+(1/2),\,j+(1/2)}^{n} \tag{27}$$

$$\mathbf{T}\big|_{i,j}^{n+1} = \mathbf{T}\big|_{i,j}^{n} + \frac{\Delta t}{2\Delta x}\,\hat{\mathbf{c}}^E \hat{\mathbf{v}}\big|_{i,j}^{n+(1/2)} \tag{28}$$

where the superscripts refer to the time instant and the subscripts indicate the gridpoint index. In Eqs. (27) and (28), we have

$$\hat{\mathbf{T}}\big|_{i+(1/2),\,j+(1/2)}^{n} = \begin{bmatrix} T_1|_{i+1,j+1}^{n} - T_1|_{i,j+1}^{n} + T_1|_{i+1,j}^{n} - T_1|_{i,j}^{n} \\ + \cdots + T_5|_{i+1,j+1}^{n} - T_5|_{i+1,j}^{n} + T_5|_{i,j+1}^{n} - T_5|_{i,j}^{n} \\ T_6|_{i+1,j+1}^{n} - T_6|_{i,j+1}^{n} + T_6|_{i+1,j}^{n} - T_6|_{i,j}^{n} \\ + \cdots + T_4|_{i+1,j+1}^{n} - T_4|_{i+1,j}^{n} + T_4|_{i,j+1}^{n} - T_4|_{i,j}^{n} \\ T_5|_{i+1,j+1}^{n} - T_5|_{i,j+1}^{n} + T_5|_{i+1,j}^{n} - T_5|_{i,j}^{n} \\ + \cdots + T_3|_{i+1,j+1}^{n} - T_3|_{i+1,j}^{n} + T_3|_{i,j+1}^{n} - T_3|_{i,j}^{n} \end{bmatrix} \tag{29}$$

$$\hat{\mathbf{v}}\big|_{i,j}^{n+(1/2)} = \begin{bmatrix} v_1|_{i+(1/2),\,j+(1/2)}^{n+(1/2)} - v_1|_{i-(1/2),\,j+(1/2)}^{n+(1/2)} + v_1|_{i+(1/2),\,j-(1/2)}^{n+(1/2)} - v_1|_{i-(1/2),\,j-(1/2)}^{n+(1/2)} \\ 0 \\ v_3|_{i+(1/2),\,j+(1/2)}^{n+(1/2)} - v_3|_{i+(1/2),\,j-(1/2)}^{n+(1/2)} + v_3|_{i-(1/2),\,j+(1/2)}^{n+(1/2)} - v_3|_{i-(1/2),\,j-(1/2)}^{n+(1/2)} \\ v_2|_{i+(1/2),\,j+(1/2)}^{n+(1/2)} - v_2|_{i+(1/2),\,j-(1/2)}^{n+(1/2)} + v_2|_{i-(1/2),\,j+(1/2)}^{n+(1/2)} - v_2|_{i-(1/2),\,j-(1/2)}^{n+(1/2)} \\ v_3|_{i+(1/2),\,j+(1/2)}^{n+(1/2)} - v_3|_{i-(1/2),\,j+(1/2)}^{n+(1/2)} + v_3|_{i+(1/2),\,j-(1/2)}^{n+(1/2)} - v_3|_{i-(1/2),\,j-(1/2)}^{n+(1/2)} \\ + \cdots + v_1|_{i+(1/2),\,j+(1/2)}^{n+(1/2)} - v_1|_{i+(1/2),\,j-(1/2)}^{n+(1/2)} + v_1|_{i-(1/2),\,j+(1/2)}^{n+(1/2)} - v_1|_{i-(1/2),\,j-(1/2)}^{n+(1/2)} \\ v_2|_{i+(1/2),\,j+(1/2)}^{n+(1/2)} - v_2|_{i-(1/2),\,j+(1/2)}^{n+(1/2)} + v_2|_{i+(1/2),\,j-(1/2)}^{n+(1/2)} - v_2|_{i-(1/2),\,j-(1/2)}^{n+(1/2)} \end{bmatrix} \tag{30}$$

Further development of the FDTD method for piezoelectric substrates is expected in the future.

7.6. Diffraction and Beamsteering

Surface acoustic waves are generated by sources of finite aperture and are therefore subject to diffraction effects. As is done in optics, the effects are classified as near-field (Fresnel) effects and far-field (Fraunhofer) effects. In SAW devices, the Fraunhofer region is of most interest.

Many of the techniques developed for optics can be applied to SAW, with the small modification that the velocity, and therefore the wavenumber, of the waves depend on the direction of propagation. The wave velocity in a specified direction is computed by solving the stiffened Christoffel equation, as outlined in Ref. 13.

A commonly used method of computing the effect of diffraction is known as the *angular spectrum of waves* (ASoW) technique. If we ignore any wave dependence in the x_3 direction, the amplitude of the surface wave ψ at a point (x,y) on the surface of the substrates can be written [22]

$$\psi(x,y) = \int_{-\infty}^{\infty} \Psi(k_y) e^{-j(k_x x + k_y y)}\, dk_y \tag{31}$$

where $\Psi(k_y)$ is the Fourier transform of the wave amplitude at a reference point $x = 0$, while k_x and k_y are x_1 and x_2 components of the wavenumber for a wave propagating at an angle ϕ to the x_1 axis shown in Fig. 2. The signal detected at the receiving transducer is calculated by integrating $\psi(x,y)$ over all receiving electrodes.

Because of the anisotropy of SAW substrates, the acoustic wavefront does not always propagate in the direction that is normal to the electrodes. This effect, known as *beamsteering*, must be considered when positioning the receiving transducer.

BIBLIOGRAPHY

1. R. M. White and F. W. Voltmer, Direct piezoelectric coupling to surface elastic waves, *Appl. Phys. Lett*. **7**(12):314–316 (1965).
2. J. H. McClellan, T. W. Parks, and L. R. Rabiner, A computer program for designing optimum FIR linear phase digital filters, *IEEE Trans. Audio Electroacoust*. **21**(6):506–526 (1973).
3. R. C. Williamson and H. I. Smith, The use of surface elastic wave reflection gratings in large time-bandwidth pulse compression filters, *IEEE Trans. Microwave Theory Tech*. **MTT-21**(4):195–205 (1973).
4. M. Solal, P. Dufilie, and P. Ventura, Innovative SPUDT based structures for mobile radio applications, *1994 IEEE Ultrason. Symp. Proc*., Cannes, France, 1994, pp. 17–22.
5. M. Hikita, N. Shibagaki, T. Akagi, and K. Sakiyama, Design methodology and synthesis techniques for ladder-type SAW resonator coupled filters, *1993 IEEE Ultrason. Symp. Proc*., Baltimore, MD, 1993, pp. 15–24.
6. H. Nakahata, K. Higaki, S. Fujii, A. Hachigo, K. Kitabayashi, K. Tanabe, Y. Seki, and S. Shikata, SAW devices on diamond, *1995 IEEE Ultrason. Symp. Proc*., Seattle, WA, 1995, pp. 361–370.
7. H. Stark and F. B. Tuteur, *Modern Electrical Communications*, Prentice-Hall, Englewood Cliffs, NJ, 1979.
8. J. C. B. Saw, T. P. Cameron, and M. S. Suthers, Impact of SAW technology on the system performance of high capacity digital microwave radio, *1993 IEEE Ultrason. Symp. Proc*., Baltimore, MD, 1993, pp. 59–65.
9. R. C. Peach, F. Z. Bi, and B. van Osch, The application of surface acoustic wave filters to communications satellite design, *Proc. AIAA 15th Int. Commun. Satellite System Conf*., San Diego, CA, 1994.
10. J. Machui, J. Bauregger, G. Riha, and I. Schropp, SAW devices in cellular and wireless phones, *1995 IEEE Ultrason. Symp. Proc*., Seattle, WA, 1995, pp. 121–130.
11. G. K. Montress, T. E. Parker, and D. Andres, Review of SAW oscillator performance, *1994 IEEE Ultrason. Symp. Proc*., Cannes, France, 1993, pp. 43–54.
12. P. M. Bakken and A. Rønnekleiv, SAW-based chirp Fourier transform and its application to analogue on-board signal processing, *Int. J. Satellite Commun*. **7**(4):283–293 (1989).
13. B. A. Auld, *Acoustic Fields and Waves in Solids*, 2nd ed., Vol. 1, Kruger, Malabar, FL, 1990.
14. C. K. Campbell, *Surface Acoustic Wave Devices*, Academic Press, Boston, 1998.
15. C. S. Hartmann, D. T. Bell, Jr., and R. C. Rosenfeld, Impulse response model design of acoustic surface-wave filters, *IEEE Trans. Microwave Theory Tech*. **MTT-21**(4):162–175 (1973).
16. Y. Xu and P. M. Smith, A theoretical and experimental study of coupled SAW resonator filters, *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **UFFC-42**(4):717–725 (1995).
17. D. P. Morgan, *Surface-Wave Devices for Signal Processing*, Elsevier, Amsterdam, 1991.
18. R. C. Peach, A general Green function analysis for SAW devices, *1995 IEEE Ultrason. Symp. Proc*., Seattle, WA, 1995, pp. 221–226.
19. V. P. Plessky and T. Thorvaldsson, Periodic Green's functions analysis of SAW and leaky SAW propagation in a periodic system of electrodes on a piezoelectric crystal, *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **UFFC-42**(2):280–293 (1995).
20. K. S. Yee, Numerical solution of initial boundary value problems involving Maxwell's equations in isotropic media, *IEEE Trans. Anten. Propag*. **AP-14**:302–307 (1966).
21. P. M. Smith and W. Ren, Finite-difference time-domain techniques for SAW device analysis, *2002 IEEE Ultrason. Symp. Proc*., Munich, Germany, 2002, pp. 313–316.
22. T. L. Szabo and A. J. Slobodnik, Jr., The effect of diffraction on the design of acoustic surface wave devices, *IEEE Trans. Sonics Ultrason*. **SU-20**(3):240–251 (1973).

ACTIVE ANTENNAS

ALAN MICKELSON
University of Colorado
Boulder, Colorado

1. INTRODUCTION TO ACTIVE ANTENNAS

A good place to start a discussion of active antennas might well be to define what we mean by an *active antenna* as is

done in two review articles on active integrated antennas [2,3]. An antenna is a structure that converts electromagnetic energy propagating in free space into voltage and current[1] in an electrical circuit and vice versa. In a transceiver system, the antenna is used to both receive and transmit free-space waves. At minimum, a transceiver then must consist of a signal source that serves to drive the antenna as well as a receiver circuit that reads out the signal from the antenna. Until relatively recently, practically all antenna systems operating in the microwave frequency regime (operation frequencies greater than 1 billion cycles per second, or 1 GHz) went to great lengths to isolate the antenna from the circuits—that is, to find ways to make system operation independent of the antenna's electrical characteristics. In contradistinction, an active antenna is one in which the antenna actually serves as a circuit element of either the driver or readout circuit. To really understand why this is different from conventional antenna driving or readout will require us to take a bit of a historical trip through the last century or so.

Actually, the first antenna of all time was an active one. Heinrich Hertz back in 1884 [4] was the first person to demonstrate that one could generate radiowaves and that they would propagate from a transmitter to a receiver at the speed of light. The apparatus used is schematically depicted in Fig. 1. The idea of the transmitter is that, by discharging an induction coil (a wire looped about a magnetic core such that the composite device can store significant amounts of magnetic energy) into a sparkgap, one can generate a current in the 5-mm-diameter wire. The voltage in the sparkgap induces a current in the wire, which in turn induces a voltage in the wires, and this voltage in turn induces current such that the voltage and current propagate along the two pieces of the wire to either side of the sparkgap as waves, appearing much like a one-dimensional slice through a water wave propagating away from the point where a pebble has struck the water's surface (the sparkgap). A wave will propagate rectilinearly until it encounters an obstruction, at which point it can suffer reflection and transmission from the barrier that the obstruction presents. There will then be reflections off the metal spheres on the ends of the wire. The spark will generate a broad spectrum of frequencies—that is, different lengths of waves. The reflections off the two ends, though, will tend to cancel each other except at certain special frequencies. The effect at these wrong frequencies is much like the effect of throwing a handful of pebbles into the pond and noting that, in between the points where the pebble struck, the waves are much less

[1]A recurring theme in this article will be that voltage and current can be independently measured only at low frequency. Active antennas are useful in the frequency regime where we cannot really operationally have independent voltage and current, but only a combination of the two that forms a wave. It would really be better to define an antenna as a structure that converts waves propagating in free space to waves propagating in a guiding structure and vice versa. Such wording is a bit overpowering and requires a bit too much qualification for the second sentence of an introduction.

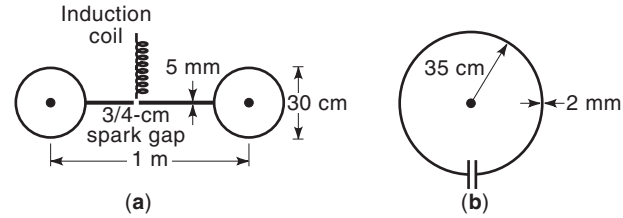

Figure 1. Hertz apparatus for (a) transmitting and (b) receiving radiowaves, where the transmitting antenna serves to choose a specific frequency of the sparkgap voltage to transmit to the receiving antenna, which also serves to pick out this special frequency from the free-space waveform and turn this electromagnetic disturbance into a voltage across the receiver antenna gap.

distinct than they are far from where the handful struck the surface. The special frequencies are ones that just fit into the region between the spheres. The current needs to be zero at the two ends in order to fit, whereas the voltage needs to be maximum at the ends. The current and voltage waves at the right frequency may appear as depicted in Fig. 2. The Hertz transmitter is the archetypical active antenna. The source is the sparkgap, which is actually placed in the antenna. The antenna then acts as a filter to pick the right frequency out of a large number of frequencies that could be launched from the sparkgap. The receiver is picked to be of a length to also select this primary frequency.

Hertz-style sparkgap transmitters, after further development and popularization by Marconi, were the primary ones in use for some 50 years after Hertz until they were banned for by the Federal Communications Commission (FCC). Indeed, sparkgap transmitters do exhibit some rather severe drawbacks. The main problem is that the simple resonant dipole antenna (i.e., a straight-wave antenna with a gap used to feed in current) is a pretty lousy frequency filter; that is, if one increases the frequency by 50%, there is 75% as much power transmitted at this frequency as at the first resonance, which is called the *fundamental*. There is a second resonance at twice the frequency of the first resonance and others at each integer multiple of the fundamental. Therefore, with increasing frequency the transmitted power decreases a little and then flattens out around the second resonance, decreases a little, flattens out at the third resonance, and so on, as is illustrated in Fig. 3. If the spark discharge is really broadband (i.e., if it really generates a large number of frequencies

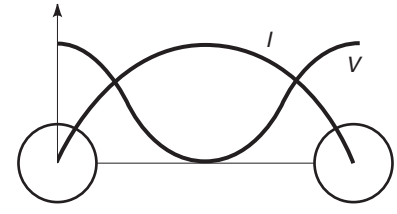

Figure 2. Current and voltage waveforms for the lowest-order (least number of zeros) waveform for the Hertz transmitter of Fig. 1a. The current must go to zero at the points where the wire ends, whereas the potential will be highest there.

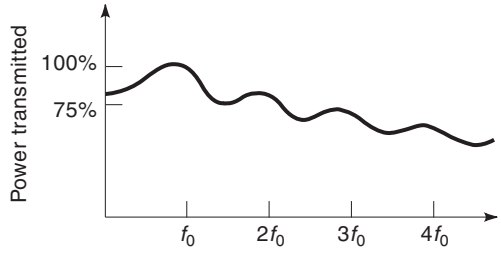

Figure 3. A sketch of what the transmission as a function of frequency might look like for the Hertzian dipole antenna of Figs. 1 and 2.

where the highest frequency may be many times the lowest), then what is transmitted by the antenna will also be broadband, albeit with somewhat higher transmission at the fundamental frequency and its harmonics than in between. In the very early days of radio, this was somewhat acceptable, although I would imagine that any information that one tried to impress on such a broadband carrier would be rather severely degraded on reception. However, the demise of the sparkgap transmitter was really instigated by the early success of radio, which caused the available frequency bands to begin to fill up rapidly. This band filling was a motivation for the formation of the FCC in 1934, which was then charged with allocation of frequency bands. That as allocation was necessary was in and of itself a justification for a (1934) ban on sparkgap transmitters, which were needlessly wasting bandwidth.

In a later experiment, Hertz noticed that the waves he was generating would tend to have a component that hugged the ground and could therefore travel over the horizon and, in fact, across the Atlantic Ocean, skimming along the surface of the water. Other researchers noticed that the effect became more pronounced at wavelengths longer than the roughly 2 m wavelength that Hertz originally used. (For the relation between frequency and wavelength for some important frequency bands, see Table 1.) In order for wave transmission to be useful, however, the transmitted signal needs to carry information. To impress information on the wave is said to be *modulating* the carrier. One can modulate either the heights (amplitudes) of the wave or the frequency of the wavetrain. The discovery of a technique to *amplitude-modulate* the waves coming off an antenna (in 1906) then led to the inception of AM radio in bands with wavelengths greater than 300 m, which corresponds to roughly 1 MHz. AM radio became commercial in 1920. By the 1930s, other researchers noted that waves with frequencies around 10 MHz, corresponding to a wavelength around 30 m, could be quite efficiently propagated over the horizon by bouncing the wave off the ionosphere. This led to the radio bands known as *shortwave*. In 1939, a researcher realized a technique to modulate the frequency of the wave. This realization led in the 1950s to FM radio, which was allocated the band around 100 MHz with a corresponding wavelength around 3 m. However, the FM technique was used first during World War II as a radar modulation technique. Radars today, as will be brought up in a subsequent paragraph, are at frequencies above roughly 1 GHz or wavelengths below 30 cm.

Table 1. A Listing of the Allocated Microwave and Millimeter-Wave Bands as Defined by the Frequency and Wavelength Range within Each Band

Band Designation	Frequency (GHz)	Wavelength
L	1–2	15–30 cm
S	2–4	7.5–15 cm
C	4–8	3.75–7.5 cm
X	8–12	2.5–3.75 cm
Ku	12–18	1.67–2.5 cm
K	18–26	1.15–1.67 cm
Ka	26–40	0.75–1.15 cm
Q	33–50	6–9 mm
U	40–60	5–7.5 mm
V	50–75	4–6 mm
E	60–80	3.75–5 mm
W	75–110	2.7–4 mm
D	110–170	1.8–2.7 mm
G	140–220	1.4–2.1 mm
Y	220–325	0.9–1.4 mm

There is a fundamental difference between circuits that operate at frequencies whose corresponding wavelengths are less than the maximum circuit dimension and those circuits that are large compared to the carrier wavelength. The effect is closely related to the concept of impedance. As was mentioned above, in the wire antenna, the voltage and current feed each other and thereby travel on the antenna as waves. The same effect takes place in a circuit. At any point along the path (line) in a circuit, one defines the ratio of voltage at one frequency to the current at the same frequency as the impedance at that frequency. If the impedance tends to preserve the phase relation (where the wave peaks lie, relatively), then we would say that the impedance is *resistive*. If the impedance tends to drive the voltage peaks forward with respect to the current peaks, we say that the impedance is *capacitive*; in the converse case we say that the impedance is *inductive*. In a small circuit, one generally tries to carefully craft passive components—resistors, capacitors, and inductors—such that they exhibit large local impedance; that is, large impedance within their physical dimension. The lines (wires) between them have little or no effect on the electromagnetic disturbance passing through the circuit, then, as the impedances in the wires are small and reasonably constant with length. When the circuit is large (compared to the highest frequency into which any signal handled by the circuit can be decomposed), the lines themselves become circuit elements, and they themselves must be carefully crafted in order to exhibit the proper impedances. To illustrate, consider the parallel-plate capacitor of Fig. 4. The capacitance is maximized by maximizing the permittivity ε (a material parameter that denotes the ratio of electrial displacement to applied electric field) and area A while minimizing the plate spacing d. However, that the capacitance depends on the plate spacing d is the important point here. Consider the circuit of Fig. 5. The only ground in the figure is the one on the battery, but the wires connecting the circuit elements together in essence form

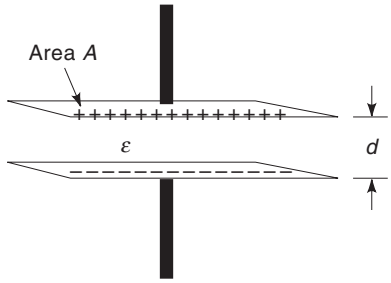

Figure 4. Schematic depiction of a parallel-plate capacitor in which the flow of a current will tend to change the upper plate, causing a voltage difference between upper and lower plates. The *capacitance* is defined as the ratio of the amount of change of the upper plate to the magnitude of the voltage this change induces between the plates.

at each point a capacitor, with a point on the wire that is carrying charge as the upper plate and the ground as the lower. This capacitance value changes as a function of position along the wire. For a small enough circuit (relative to the wavelength of the highest frequency carried by the circuit), the effect is not too important, as the wire–ground pair is not optimized for capacitance value and the position-varying effect is small. For a large circuit, the effect is disastrous, as we'll consider below.

Consider the circuit of Fig. 6. The idea is to discuss what happens when impedances aren't carefully controlled. Let's first say that the circuit is short (compared to wavelength). If the load resistor R_L is not matched to (i.e., isn't equal to) the resistance of the source R_S, some amount of reflection will occur at R_L, propagate back to R_S, be reflected with a minus sign times the reflection at R_L, propagate back to R_L, and so on. The reflections add up perfectly out of phase (i.e., simply subtract from one another) at the source and load, and the amount of power supplied to the load is less than optimal. In this limit of a small-circuit case, it is as if the load will not allow the source to supply as much power as it is capable of. Let's now say that the line is "nice" but long compared to a wavelength. Then the same argument applies to the reflections, but in this case the source doesn't know that the load is there until several wave periods have passed (several maxima and minima of the waveform have left the source), so the source supplies all the power it can. The power, though, is not allowed to be fully absorbed by the load, and some amount of the power will rattle around the line until it is radiated or absorbed. As we mentioned above, in a long enough circuit the wire itself becomes a distributed element—that is, one with an impedance of its own. If the distance to the nearest ground is not kept fixed

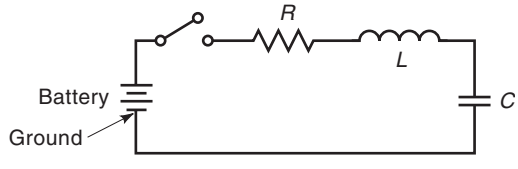

Figure 5. A circuit with lumped elements connected by wire segments.

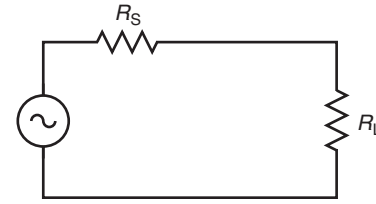

Figure 6. A circuit in which one is trying to supply power from a source with internal resistance R_S to a load with resistance R_L. The power transfer is maximized only when R_S and R_L are equal, in which case half the power supplied by the source is supplied to the load, the other half being dissipated in the source and causing it to heat.

along the line, this impedance becomes dependent on the position. In this case, we would have distributed reflections all along the line and the circuit would probably not work at all. This spatially variable impedance line is flexible, though, as illustrated by the drawing of a coaxial cable in Fig. 7. The idea is that, if the line brings along its own ground plane in the form of a grounded outer conductor, the impedance of the line can be kept constant with distance. The problem becomes the connection of the line to the source and load. A byproduct of this problem is a measurement reality. That reality is that a sufficiently high frequency one can no longer accurately sample voltage or current individually. Voltage sampling requires a measurement circuit that exhibits a high resistive impedance parallel to the impedance, which separates the sampling points of this composite voltage probe, whereas a current probe requires a small parallel impedance. Such probes are not impedance matched and disrupt the normal operation of the circuit under test. High-frequency circuit probes must use carefully impedance-matched termination, and thereby can only sample the power of waves propagating on the circuit's lines.

Before going on to discuss the "conventional" solution versus the "new" active-antenna solution, perhaps we should summarize a bit. In AM, shortwave, and FM applications, the wavelengths are greater than meters. If one considers typical receivers, the whole circuit will generally

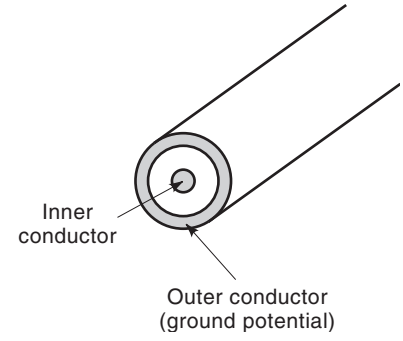

Figure 7. A coaxial cable in which signals are carried on an inner conductor and in which the grounded outer conductor serves to carry the ground plane along with the signal in order to give a constant impedance along the line.

be small compared to the carrier wavelength. This is also to say that in all of these cases, the antennas will be active in the sense that the antenna presents an impedance to the circuit. One needs pieces of line comparable to a wavelength to really match or isolate a component. However, from here on we won't be interested in the low-frequency case but rather in the well-above-1-GHz case. During World War II, radar was the application that drove the frequencies above 1 GHz (wavelength less than 30 cm). In a radar, one sends out a pulse and, from the return scattered wave, tries to infer as much as possible about the target. Target resolution is proportional to wavelength. There has been a constant drive to shorten wavelength. Therefore, as is indicated by Table 1, one notes that bands have been allocated out to 100 s of GHz. Presently, however, there are a plethora of nonmilitary drivers for pushing to higher frequencies. These relate to compactness and lower power dissipation. But as we'll see, the conventional solution, which was developed for radars, is really not conducive to compactness nor to the pressures of cost minimization of the commercial market.

A typical conventional transmitter may appear as that schematically depicted in Fig. 8. A main concept here is that the transmission lines and matching networks are being used to isolate the oscillator from the amplifier and the amplifier from the antenna, in contrast to the situation in an active antenna. There were a number of reasons why the conventional solution took on the form that it did. Among them was the urgency of World War II. Radar was developed rapidly in both Great Britain and the United States in the 1930s and 1940s. Rapid development required numerous researchers working in parallel. When operating frequencies exceeded 1 GHz (corresponding to 30 cm wavelengths), matching networks, whose main requirement is that they must consist of lines of lengths comparable to a wavelength, became convenient to construct (in terms of size) for ground-based radar. In this case, then, the oscillators could be optimized independently of the amplifiers, which in turn could be optimized independently of the antennas and the receiver elements. The impedances of the individual pieces didn't matter, as the matching networks could be used to effectively transform the effective impedances looking into an element into something completely different for purposes of matching pieces of the network to each other. There are costs associated with such a solution, though, such as total system size as well as the tolerances that components must satisfy. However, once the technique was in place, the industry standardized on the conventional solution and perfected it to the point where it was

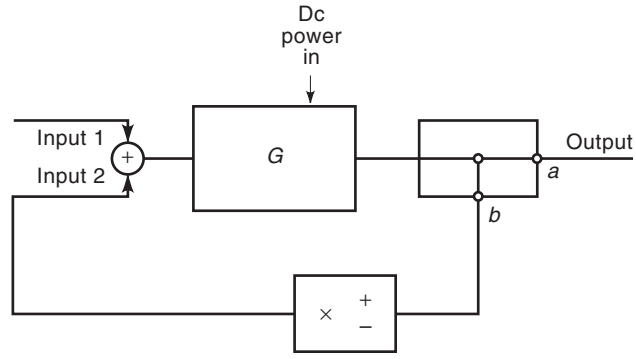

Figure 9. Schematic depiction of a feedback system that can operate as an oscillator when G is greater than 1, the feedback is positive, and there is a delay in feeding back the output to the input.

hard to challenge. The reemergence of the active solution really owes itself to two independent technologies, the emergence of high-frequency solid-state devices and the development of planar circuit and planar antenna technology.

A single frequency of electromagnetic energy must be generated in an *oscillator*—that is, a circuit that converts DC electrical power to AC electromagnetic power at the proper frequency. The basic operation of an oscillator can be described with respect to Fig. 9. What is shown here schematically is an amplifier in which a portion b (<1) of the output is fed back to the input with either a plus or a minus sign. When the feedback is off ($b=0$), then the signal out will be just G times the input. When the feedback is negative, the output will be less than G times the input. However, in the negative feedback mode, the stability to noise increases since fluctuations will be damped; that is, if the output fluctuates up, this lowers the effective input, whereas if the output fluctuates down, the output is driven up. The opposite is true in the positive-feedback case. In the positive-feedback case, if there were no fluctuation, any input would cause the output to increase until all the DC power in as well as all of the input signal would show up at the output. (This is all of the power that can show up at the output. This behavior is typical of unstable operation.) This would not be such an interesting case. However, there are always fluctuations of the input, and the positive feedback will cause these to grow. If there is a delay from output to input, then fluctuations with a period corresponding to this delay will be favored, as a rise in the input would show up as a rise in the output one period later, and rapidly all the DC power in would be converted to power out at this magic frequency. A real

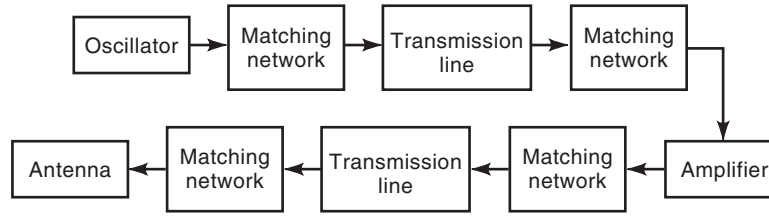

Figure 8. Schematic of a conventional RF microwave transmitter in which each individual element of the transmitter is matched to each other element.

circuit would operate a bit more interestingly than our ideal one. In a real circuit, as the fluctuations build up, the gain would be affected and some elements would absorb power, but the oscillations still would take place, although perhaps with a different frequency and amplitude from what one would have predicted from nondynamic measurements.

The transistor was first demonstrated in 1947, with publication in 1948 [5], with the diode not far behind [6]. Although the field-effect transistor (FET) was proposed in 1952 [7], it was not until the mid-1960s that the technology had come far enough that it could be demonstrated [8]. The high-electron-mobility transistor (HEMT) is a modification of the FET which allows for higher-frequency (and lower-noise) operation than the FET. The heterojunction bipolar transistor (HBT) is a more complex three-dimensional structured yet still integrated circuit (IC)-compatible semiconductor device that is now replacing the FET/HEMT in certain high-frequency applications. Two-terminal transferred electron devices (TEDs) were used before the FET for microwave applications and are still in use but tend to have a much lower wallplug efficiency, especially as the amplifying device of an oscillator. Radar systems, however, were already in use in the late 1930s. Essentially all of the microwave sources in radars up until the 1970s operated on principles that required that the source have physical dimensions larger than a wavelength, and perhaps many wavelengths. This fact almost required the use of conventional solution. Transistors, though, can have active areas with dimensions of micrometers; even packaged hybrid devices can have complete packages of dimensions smaller than a millimeter. The transistor can, therefore, act as an amplifier with dimensions much smaller than a wavelength and does not, therefore, need to be placed in a conventional solution design.

The last piece of our story of the new active-antenna era involves the development of printed-circuit technology, along with slot and patch antennas. The two most common planar "open waveguide" designs are microstrip line and coplanar waveguide (CPW). Depictions of these waveguide lines are given in Fig. 10. The idea behind the microstrip line is to propagate electromagnetic energy along the line by confining the electric field between the upper signal line and a lower ground plane. As the upper line carries current, a magnetic field encircles the upper line. As power flow takes place in a direction perpendicular to the electric and magnetic fields, the power flow is beneath the signal line in the dielectric. As we discussed before, on a low-frequency wire, the voltage and current waveforms couple to generate a wave. The coupling of the electric and magnetic fields in the microstrip is analogous to the coupling of voltage and current on the Hertz antenna wire, except that the microstrip line can be electrically long in the sense that the distance from the signal line to the ground plane is kept constant so that the impedance can be kept constant, as with the earlier-discussed coaxial cable. Lines that carry along their ground planes are generally referred to as *transmission lines*. Components (i.e., capacitors and inductors) can be built into the line by doing such things as changing the width or cutting gaps

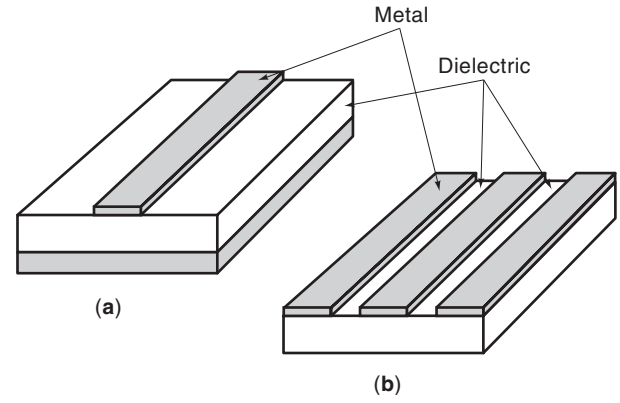

Figure 10. Views of (a) a microstrip and (b) a coplanar waveguide line. In the microstrip, the ground plane is the lower electrode, whereas in the coplanar waveguide the ground plane is placed on the surface of the dielectric substrate.

into the upper line or putting slits in the ground plane. In this sense, we can still describe transmission-line circuits by conventional circuit theory if we use a special circuit model for the line itself. The CPW line is quite similar to the microstrip line except that there the ground planes are on top of the dielectric slab. Either of these line types is reasonably easy to fabricate, as one needs only to buy a metal-coated dielectric plate and then pattern the needed shapes by photographically defining the patterns using a technique known as *photolithography*, a process common to all present-day circuit fabrication. These planar structures are quite compatible with transistor technology, as is indicated by the simple transistor oscillator circuit depicted in Fig. 11. The gap in the line on the drain side is there in order to provide the proper feedback for oscillation. In this case, the total oscillator linear dimension can be less than a wavelength.

In order to have an active antenna, one needs to have a radiating element—that is, a passive-antenna element in the active antenna. Certain antenna technologies are compatible with microstrip and CPW technologies, and these antenna types are illustrated in Fig. 12. The idea behind either of these antenna types is that the patch or slit is designed to have one of its dimensions in the plane match the operating wavelength such that the structure resonates (such as we had discussed in conjunction with the Hertz dipole antenna). In the case of fundamental mode operation of the patch antenna, the resonating direction is

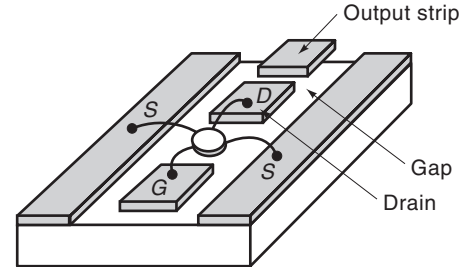

Figure 11. A simple transistor oscillator implemented in CPW technology.

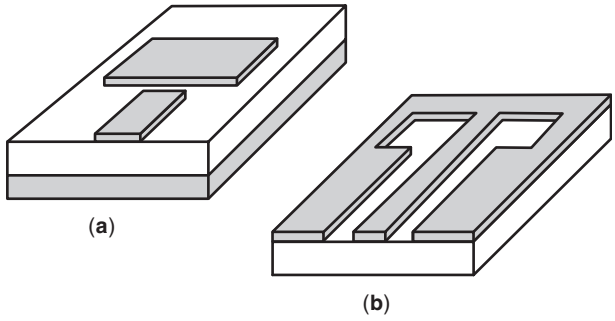

Figure 12. A depiction of (a) a patch antenna in a microstrip line and (b) a slot antenna in a CPW line.

the direction of the patch that lies along the direction of the feedline and extends from the end of the feedline to the end of the patch. The other dimension must be chosen such that it does not resonate, which requires that its dimension not correspond too closely to a resonance along that direction. A possible choice is to make this dimension smaller than the other so that its length is too short to resonate. However, square patches are also possible as the feedline will favor the resonance along the feed direction. Now, in a microstrip configuration, the electric field points primarily from the upper conductor to the ground plane. For the patch antenna, this configuration is illustrated in Fig. 13. The downward-pointing electric field component along the edges of the patch that are directed along the same direction as the input feedline (resonating direction) will then have a field pattern as sketched in Fig. 13a, and this downward component of the electric field along the edges perpendicular to the feedline direction (where it has been assumed that there is no resonance along this direction) will have a field pattern as sketched in Fig. 13b, with a composite sketch given in Fig. 13c. The important part of the sketches, however, is really the so-called fringing fields in Fig. 13a—that is, the fields that point neither up nor down but rather point across. Along the input *radiating edge*, that is, the edge that is perpendicular and connects to the input line, electric field lines point along the direction of the feedline extending from some distance out in the dielectric to the edge. Along the other *radiating edge*, the other edge that is perpendicular to the input feedline but at the other side of the patch, there is a field pointing out (i.e., in phase with the electric field of the input radiating edge) from the edge into the dielectric. These two stripes of field, in phase and a resonating distance apart, then combine together to create an upwardly radiating wave field. The non radiating edges, those that are along the direction of the input feedlines, do not give rise to fringe field contributions as well, but these fringe field contributions are out of phase with each other and thereby cancel and do not contribute to the radiation from the patch. The operation of a slot antenna can be explained by a similar argument if one notes that the radiating edges must be those edges that lie along the direction of the feedline that is the downward-pointing magnetic field (the dominant component of the magnetic field that rings the currents) that takes the part of the electric field in the slot antenna's operation.

We have now introduced all the pieces necessary to describe the new resurgence in active-antenna research. A possible active-antenna design could appear as in Fig. 14 [9], where the transistor is actually mounted right into the patch antenna element, and therefore the design can be quite compact; that is, the source plus oscillator plus antenna can all be fit into less than a wavelength area. The design of Fig. 14, which comes from R. Compton's group at Cornell, will be discussed further in the next section.

There are a number of advantages to the use of active antenna ideas. One is that an active antenna can be made compact. Compactness in itself is advantageous,

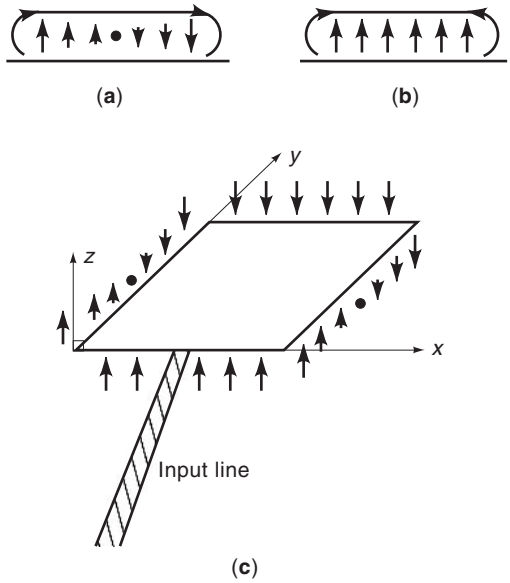

Figure 13. Illustration of the electric field directions along (a) the nonradiating edge and (b) the radiating edge, and (c) a schematic depiction of the edge fields around the patch.

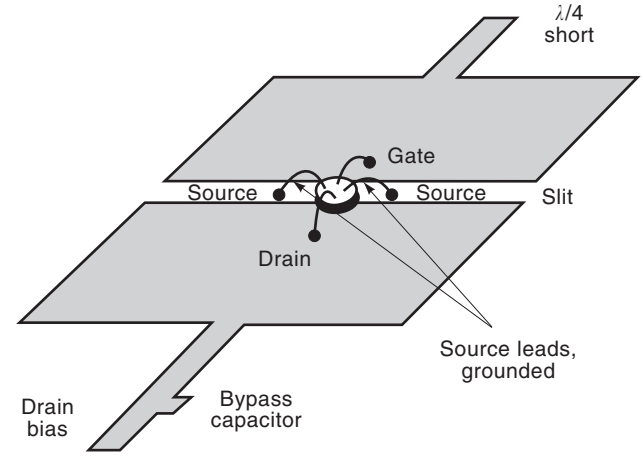

Figure 14. Depiction of the upper surface metallization of a microstrip active patch antenna discussed in Ref. 7. The short circuit on the gate together with the slit between gate and drain provides the proper feedback delay to cause oscillation.

as throughout the history of microelectronics, miniaturization has led to lowered costs. There are really two more advantages, though, that relate to compactness. One is that the power-handling capabilities of a device go down with increasing frequency. We would therefore like to find ways to combine the power from several devices. One can try to add together outputs from various oscillators in the circuit before feeding them to the elements, but this goes back to the conventional solution. A more advantageous design is to make an array of antennas, with proper spacing relative to the wavelength and antenna sizes, and add the power of the "locked" oscillators in the array quasioptically in free space.[2] The locking requires that the oscillators "talk" to each other such that the phases of all the array elements stay in a given relation. As will be discussed in more detail in the next section, however, an important problem at present in the active-antenna field relates to keeping elements locked yet still being able to modulate the output as well as steer the beam in order to be able to electronically determine on output direction. These issues will be discussed in Section 2 and in more detail in Section 3.

2. SOME QUANTITATIVE DISCUSSION OF ASPECTS OF ACTIVE ANTENNAS

Antennas are structures that convert free-space radiation to guided radiation and vice versa. In order to carry out this operation efficiently, antennas must have some dimension that is significant compared to a wavelength. Antenna design then must require a full treatment of the electromagnetic field, including its geometric structure to subwavelength accuracy and its polarization. Such analysis requires the full apparatus of Maxwell's field equations. An early motivation for the use of the active-antenna concept was that of using the field generating devices in proximity to the antenna such that the physical length of an electromagnetically small antenna could be augmented by the characteristics of the generating mechanism. Presently, attention has turned to higher frequencies, but the active-antenna concept that an antenna and a circuit be coupled such that the circuit can be used to alter the antennas characteristics is the same. An interesting point is that although the operating frequency of active antennas is usually high, that is, higher than the frequency regime at which integrated electronic circuits operate, the driving circuit tends to be small in total extent relative to the operating wavelength and therefore circuit theory concepts still apply to active-antenna design although these circuit theory concepts must be judiciously combined with electromagnetic theory. The usual formulation couples a high-frequency form of transmission-line theory with circuit theory as applied to microwave/millimeter-wave circuits. We will presently work from Maxwell's theory to high-frequency transmission-line theory as it applies to guidance and radiation. We will introduce the somewhat specialized circuit formulation, which includes transmission lines and planar antennas that is usually applied to the high-frequency integrated active-antenna problem.

Maxwell's equations are the basic defining equations for all electromagnetic phenomena, and they are expressible in MKSA units as [11]

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t}$$

$$\nabla \times \mathbf{H} = \mathbf{J} + \frac{\partial \mathbf{D}}{\partial t}$$

$$\nabla \cdot \mathbf{D} = \rho$$

$$\nabla \cdot \mathbf{B} = 0$$

where $\mathbf{E}$ is the electric field vector, $\mathbf{B}$ is the magnetic induction vector, $\mathbf{H}$ is the magnetic field vector, $\mathbf{D}$ is the electric displacement vector, $\mathbf{J}$ is the current density vector, and ρ is the volume density of charge. Each of these field quantities is a function of three spatial coordinates, which define a coordinate vector $\mathbf{r}$, and of the time t. The del operator ∇ and its associated operations of the curl $\nabla \times$ and the divergence $\nabla \cdot$ operate on these spatial coordinates. An additional important quantity is $\mathbf{S}$, the Poynting vector, defined by

$$\mathbf{S} = \mathbf{E} \times \mathbf{H}$$

If one is to take the divergence of $\mathbf{S}$, one finds

$$\nabla \cdot \mathbf{S} = \nabla \cdot (\mathbf{E} \times \mathbf{H})$$

where, if one assumes a free-space region

$$\mathbf{D} = \varepsilon_0 \mathbf{E}$$

$$\mathbf{B} = \mu_0 \mathbf{H}$$

where free-space implies current-free

$$\mathbf{J} = 0$$

and charge-free

$$\rho = 0$$

where ε_0 is the permittivity of free space and μ_0 is the permeability of free space, one can use vector identities and Maxwell's equations to obtain

$$\nabla \cdot \mathbf{S} = -\frac{\varepsilon_0}{2}\frac{\partial}{\partial t}(\mathbf{E} \cdot \mathbf{E}) - \frac{\mu_0}{2}\frac{\partial}{\partial t}(\mathbf{H} \cdot \mathbf{H})$$

Integrating this equation throughout a volume V and using Gauss' theorem

$$\int \nabla \cdot \mathbf{S}\, dV = \int \mathbf{S} \cdot \mathrm{d}\mathbf{A}$$

[2]An amplifier is an oscillator biased above threshold, but without feedback. An array of active antennas carefully designed to have no internal feedback can be used to amplify weak signals. This is an alternative to having the array itself generate the initial signal, and the design if such amplifiers is also a part of the field of quasioptical power combining. This topic is reviewed in Ref. 10.

where $d\mathbf{A}$ is the unit normal pointing out of the surface of the volume V, one finds that

$$\int \mathbf{S}\cdot d\mathbf{A} = -\frac{\partial}{\partial t} W_{\mathrm{e}} - \frac{\partial}{\partial t} W_{\mathrm{m}}$$

where W_{e} is the electric energy density

$$W_{\mathrm{e}} = \frac{\varepsilon_0}{2}\int \mathbf{E}\cdot\mathbf{E}\, dV$$

and W_{m} is the magnetic energy density

$$W_{\mathrm{m}} = \frac{\mu_0}{2}\int \mathbf{H}\cdot\mathbf{H}\, dV$$

The interpretation of these equations is that the amount of $\mathbf{S}$ flowing out of V is the amount of change of the energy within V. One therefore associates energy flow with $\mathbf{S} = \mathbf{E}\times\mathbf{H}$. This is important in describing energy flow in wires as well as transmission lines and waveguides of all types. As was first described by Heavyside [12], the energy flow in a wire occurs not inside the wire but around it; that is, as the wire is highly conductive, there is essentially no field inside it except at the surface where the outer layer of oscillating charges have no outer shell to cancel their effect. There is therefore a radial electric field emanating from the surface of the wire that combines with an azimuthal magnetic field that rings the current flow to yield an $\mathbf{E}\times\mathbf{H}$ surrounding the wire and pointing down its axis. Likewise, for a structure to radiate electromagnetic power upward from its surface requires that crossed components of $\mathbf{E}$ and $\mathbf{H}$ exist on an upward-pointing surface of the conductor.

Now, we would like to apply Poynting's theorem to the study of circuits that may contain antennas. A circuit, in general, will contain conductors that guide charges and currents, and these conductors will be surrounded by materials that are permeated by electromagnetic fields generated by the charges and currents in the conductors. It was Pocklington in 1897 [13] who made the formal structure of the fields around a wire a bit more explicit and, in the effort, also formed the basis for the approximation on which most of circuit and transmission-line theory rests, the quasistatic approximation. The result of his study of monochromatic (single-frequency) fields on wires could be summarized as follows. If one considers a small enough region around the axis of a wire conductor, one could construct an xyz Cartesian coordinate system where the axis of the wire is the z axis. As the fields close to the wire are stronger than those farther away, one can show that close enough to the wire all of the field quantities $\mathbf{f}(x, y, z, t)$ vary as

$$\mathbf{f}(x,y,z,t) = \Re\{\mathbf{f}(x,y)p(z,t)\}$$

where the propagation function $p(z, t)$ will generally take the form

$$p(z,t) = a_{\mathrm{f}}e^{i\beta z - i\omega t} + a_{\mathrm{b}}e^{-i\beta z - i\omega t}$$

where the a_f and a_b are complex constants, β a propagation constant and ω the angular frequency of the assumed field's source. That is, the above states that the fields consist of forward- and backward-propagating waves multiplied by a transverse field configuration. If one assumes that the velocity of propagation of the above-defined wave is $v = (\mu\varepsilon)^{-1/2}$, where the speed of light the speed of light $c = (\mu_0\varepsilon_0)^{-1/2}$ is generally reduced by materials that have μ and ε different from their free-space values, then one can write that

$$\beta = \frac{\omega}{v}$$

The result that $\mathbf{f}(x, y)$ is independent of z, when substituted into Maxwell's equations, results in the relations in which

$$\nabla_{\mathrm{t}}\times\mathbf{E}_{\mathrm{t}} = \rho$$

$$\nabla_{\mathrm{t}}\times\mathbf{H}_{\mathrm{t}} = J_z$$

where

$$\nabla_{\mathrm{t}} = \hat{e}_x\frac{\partial}{\partial x} + \hat{e}_y\frac{\partial}{\partial y}$$

is just the transverse, and therefore two-dimensional, gradient operator and the $\mathbf{f}_{\mathrm{t}}$ are the transverse field quantities. These equations are just the electro-and magnetostatic equations for the transverse fields, whereas the propagation equation above shows that these static transverse field configurations can be just propagated forward [if the wire is perfectly terminated such that the a_{b} of the $p(z, t)$ equation is zero but the a_{f}, the forward-going coefficient is nonzero] as if they corresponded to a propagating plane-wave field configuration. If the magnetic field is caused by the current in the wire, it rings the wire, whereas if the electric field is static, it must appear to emanate from charges in the wire and point outward at right angles to the magnetic field. The Poynting vector $\mathbf{S}$ then points along the direction of propagation, that is, along the wire. If the wire is somehow terminated, for example in an open or short circuit termination, then the dominant electric field may be along the direction of the wire's axis [this is the case where the a_{b} may be close to or equal to the a_{f} in the $p(z, t)$ equation], and the Poynting vector $\mathbf{S}$ may have a significant component at right angles to the propagation direction. In fact, in an antenna structure, one open-terminates a wire at a length (half-wavelength) from a feedpoint such that the electric field is strongly and homogenously pointing along the axis of the wire during each half of the wave period. As the current guided along the wire and also changes direction each half-period, the Poynting vector can be maintained in an upwardly pointing direction throughout the wave period. It is reasonably straightforward to generalize this thin wire theory to more general conductor shapes and non-Cartesian geometries, but always with the result that the conductors can be laid out in such manner that they can be used to control the electromagnetic energy flow through controlling the forward and backward excitation coefficients of transverse field configurations that closely resemble static field structures.

If we wish to guide electromagnetic energy along conductors and radiate energy by changing the guiding structure in a controlled manner, then one must design the guiding and radiating structures such that the quasistatic picture comes close to being the actual one. An approximate theory that is based on Pocklington's quasistatic

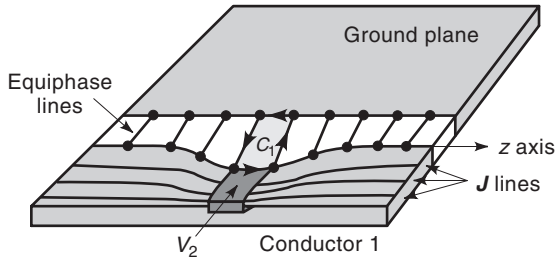

Figure 15. A sketch of a two-conductor transmission line where some equipotentials and some current lines are drawn in, as well as a volume V_1 with outward-pointing normal $d\boldsymbol{A}_1$. There is also an outward-pointing normal $d\boldsymbol{A}_2$ associated with the area bounded by contour C_2.

approximation is one called *transmission-line theory*. To derive this theory, first consider the two-wire transmission line of Fig. 15. If we are to have something that we can actually call a transmission line, then we would hope that we can find equiphase fronts of the electromagnetic disturbance propagating in the gap crossing the gap conductor and that we can find lines along which the current flows on the current-carrying conductor. Otherwise, if the equiphases closed on themselves and/or we had eddies in the current, it would be hard to think of the structure as any form of guiding structure. Let's say we form an area in the gap with two walls of the four-sided contour C_1 surrounding this area following equiphases an infinitesimal distance dz from each other. We could then write

$$\int \nabla \times \mathbf{E} \cdot \mathbf{dA}_1 = -\int \frac{\partial \mathbf{B}}{\partial t} \cdot \mathbf{dA}_1$$

where $\mathbf{dA}_1$ corresponds to an upward-pointing normal from the enclosed area. One generally defines the integral as

$$\int \mathbf{B} \cdot \mathbf{dA}_1 = \phi$$

where ϕ is the magnetic flux. We further often define the flux as the inductance of the structure times the current by

$$\phi = Li$$

The integral with the curl in it can be rewritten by Stokes' theorem as

$$\int \nabla \times \mathbf{E} \cdot \mathbf{dA}_1 = \oint_{C_1} \mathbf{E} \cdot \mathbf{d}\ell$$

where C_1 is the contour enclosing the area. If we define

$$v = \int \mathbf{E} \cdot \mathbf{d}\ell$$

on the two equiphase lines of the contour C_1, where v is an AC voltage (this is the main approximation shown above, as it is only strictly true for truly static fields), then, noting that v doesn't change along two of the boundaries of the contour (because they are the infinitesimal walls on constant voltage plates) and making the other two connecting lines infinitesimal, we note that the relation between the curl of $\mathbf{E}$ and the magnetic field reduces to

$$v(z+dz) - v(z) = \frac{\partial}{\partial t}(Li)$$

where it has been tacitly assumed that geometric deviations from rectilinear are small enough that one can approximately use Cartesian coordinates, which could be rewritten in the form

$$\frac{\partial v}{\partial z} = \ell \frac{\partial i}{\partial t} \tag{1}$$

where ℓ is an inductance per unit length, which may vary with longitudinal coordinate z if the line has longitudinal variation of geometry. A similar manipulation can be done with the second and third of Maxwell's equations. Taking

$$\nabla \cdot (\nabla \times \mathbf{H}) = \nabla \cdot \mathbf{J} + \frac{\partial}{\partial t} \nabla \cdot \mathbf{D}$$

and noting that the divergence of a curl is zero, substituting for $\nabla \cdot \mathbf{D}$ we find

$$\nabla \cdot \mathbf{J} + \frac{\partial \rho}{\partial t} = 0$$

which is the equation of charge conservation. Integrating this equation over a volume V_2 that encloses the current-carrying conductor whose walls lie perpendicular to the current lines gives

$$\int \underline{\nabla} \cdot \mathbf{J}\, dV_2 = -\frac{\partial}{\partial t} \int \rho dV_2$$

where the total change Q, given by

$$Q = \int \rho dV_2$$

is also sometimes defined in terms of capacitance C and voltage v by

$$Q = Cv$$

Noting that

$$\int \nabla \cdot \mathbf{J} dV_2 = \int \mathbf{J} \cdot \mathbf{dA}_2$$

where $\mathbf{dA}_2$ is the outward-pointing normal to the boundary of the volume V_2 and where one usually defines

$$i = \int \mathbf{J} \cdot \mathbf{dA}_2$$

and letting the volume V have infinitesimal thickness, one finds that

$$\int \mathbf{J} \cdot \mathbf{dA}_2 = i(z+dz) - i(z)$$

Putting this together with the equations above, we find

$$\frac{\partial i}{\partial z} = c \frac{\partial v}{\partial t} \tag{2}$$

where c is the capacitance per length of the structure, where longitudinal variations in line geometry will lead to a longitudinal variation of c. The system of partial differential equations for the voltage and current have a circuit representation, as schematically depicted in Fig. 16a. One can verify this by writing Kirchhoff's laws for the nodes

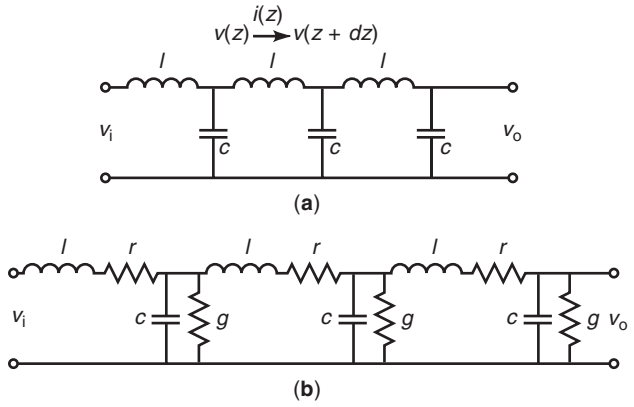

Figure 16. A circuit equivalent for (a) a lossless and (b) a lossy transmission line. The actual stages should be infinitesimally long, and the *l*s and *c*s can vary with distance down the line. In reality, one can find closed-form solutions for the waves in nominally constant l and c segments and put them together with boundary conditions.

with $v(z+dz)$ and $v(z)$ using the relations

$$v = \ell \frac{\partial i}{\partial t}$$

and

$$i = c \frac{\partial v}{\partial t}$$

Fig. 16b illustrates the circuit equivalent for a lossy (and therefore dispersive) transmission line, where the r represents the resistance encountered by the current in the metallization and where the g represents any conductance of the substrate material that might allow leakage to ground. A major point of the diagram is that the structure need not be uniform in order to have a transmission-line representation, although one may find that irregularities in the structure will lead to longitudinally varying inductances and capacitances.

Clearly, the solution to the circuit equations will have a wave nature that will exhibit propagation characteristics, which we discussed previously. In a region with constant ℓ and c, one can take a z derivative of Eq. (1) and a t derivative of Eq. (2) and substitute to obtain

$$\frac{\partial^2 v}{\partial z^2} - \ell c \frac{\partial^2 v}{\partial t^2} = 0$$

which is a wave equation with solutions

$$v(z,t) = v_f \cos(\omega t - \beta z + \phi_f) + v_b \cos(\omega t + \beta z + \phi_b) \qquad (3)$$

where v_f is the amplitude of a forward-going voltage wave, v_b is the amplitude of a backward-going voltage wave, and

$$\frac{\omega}{\beta} = \sqrt{\ell c}$$

Similarly, taking a t derivative of Eq. (1) and a z derivative of Eq. (2) and substituting gives

$$\frac{\partial^2 i}{\partial z^2} - \ell c \frac{\partial^2 i}{\partial t^2} = 0$$

which will have a solution analogous to the one in Eq. (3), but with

$$v_f = \sqrt{\frac{\ell}{c}} i_f$$

$$v_b = \sqrt{\frac{\ell}{c}} i_b$$

which indicates that we can make the identification that the line phase velocity v_p is given by

$$v_p \triangleq \frac{\omega}{\beta} = \sqrt{\ell c}$$

and the line impedance Z_0 is given by

$$Z_0 = \sqrt{\frac{\ell}{c}}$$

Often, we assume that we can write (the sinusoidal steady-state representation)

$$v(z,t) = \mathrm{Re}[v(z)e^{j\omega t}]$$

$$i(z,t) = \mathrm{Re}[i(z)e^{j\omega t}]$$

such that we can write that

$$\frac{\partial v}{\partial z} = -j\omega \ell i$$

$$\frac{\partial i}{\partial z} = -j\omega c v$$

with solutions

$$v(z) = v_f e^{-j\beta z} + v_b e^{j\beta z}$$

$$i(z) = i_f e^{-j\beta z} + i_b e^{j\beta z}$$

Let's say now that we terminate the line with a lumped impedance Z_ℓ at location ℓ. At the coordinate ℓ, then, the relations

$$Z_\ell i(\ell) = v_f e^{-j\beta\ell} + v_b e^{j\beta\ell}$$

$$Z_0 i(\ell) = v_f e^{-j\beta\ell} - v_b e^{j\beta\ell}$$

hold, and from them we can find

$$v_f = \frac{1}{2}(Z_\ell + Z_0) i(\ell) e^{j\beta\ell}$$

$$v_b = \frac{1}{2}(Z_\ell - Z_0) i(\ell) e^{-j\beta\ell}$$

which gives

$$v(z) = \frac{i(\ell)}{2}[(Z_\ell + Z_0)e^{j\beta(\ell - z)} + (Z_\ell - Z_0)e^{-j\beta(\ell - z)}]$$

$$i(z) = \frac{i(\ell)}{2Z_0}[(Z_\ell + Z_0)e^{j\beta(\ell - z)} - (Z_\ell - Z_0)e^{-j\beta(\ell - z)}]$$

allowing us to write

$$Z(z-\ell) = \frac{v(z-\ell)}{i(z-\ell)} = Z_0 \frac{Z_\ell + jZ_0 \tan\beta(z-\ell)}{Z_0 + jZ_\ell \tan\beta(z-\ell)} \qquad (4)$$

This equation allows us to, in essence, move the load from the plane ℓ to any other plane. This transformation can be

used to eliminate line segments and thereby use circuits on them directly. However, note that line lengths in which the line is at least comparable to a wavelength are necessary in order to significantly alter the impedance. At the plane $z = \ell$, then, we can further note that the ratio of the reflected voltage coefficient v_b and the forward-going v_f, which is the voltage reflection coefficient, is given by

$$\mathscr{R} = \frac{Z_\ell - Z_0}{Z_\ell + Z_0}$$

This is the reflection we discussed in the last section, which causes the difference between large and small circuit dimension.

One could question the utility of discussing Poynting vectors and transmission lines when the discussion was on active antennas. The answer really is that any antenna system, at whatever frequency or of whatever design, is a system for directing power from one place to another. To direct power from one place to another requires constantly keeping the Poynting vector pointed in the right direction. As we can surmise from the transmission-line derivation, line irregularities may cause the Poynting vector to wobble (with attendant reflections down the line due to attendant variations in the ℓ and c), but the picture must stay close to "correct" for power to get from one end of the system to another. For this reason, active antennas, even at very high (100 s of GHz) frequencies can still be discussed in terms of transmission lines, impedances, and circuit equivalents, although greater care must be used in applying these concepts at increasingly higher frequencies.

The next piece of an active antenna that needs to be discussed is the active element. Without too much loss of generality, we will take our device to be a field-effect transistor (FET). A field-effect transistor (FET) is a device first described by Schockley in 1952 [7], but the MESFET (metal semiconductor FET) was not realized until 1965 [8] when gallium arsenide (GaAs) fabrication techniques became more workable. It should be pointed out that the silicon MOSFET (metal oxide semiconductor FET) is the workhorse device of digital electronics and therefore the most common of all electronic devices presently in existence by a very large margin. The GaAs MESFET was an important structure in the development of discrete microwave components and was used in early development of monolithic microwave circuitry (MMIC). High-electron-mobility transistors (HEMTs) and heterostructure bipolar transistors (HBTs) in such material systems as InP now are replacing GaAs MESFETs as both discrete and integrated components. In the present, though, the FET (and for some characteristics, the GaAs MESFET) will be used as a prototype device as its characteristics are reasonably archtypical of solid-state microwave devices. A top view of an FET might appear as in Fig. 17. As is shown clearly in the figure, an FET is a three-terminal device with gate, drain, and source regions. A cross section of the active region (where the gate is very narrow) might appear as in Fig. 18. The basic idea is that the highly doped n region causes current to flow through the ohmic contacts from drain to source (i.e., electrons flow from source to drain), but the current is controlled in magnitude by the electric field generated by the reverse bias voltage applied to the

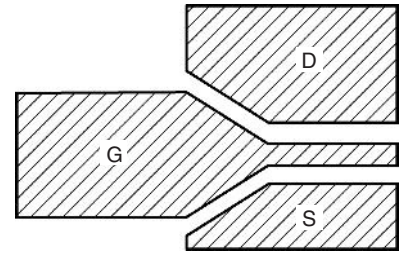

Figure 17. Schematic depiction of a top view of the metallized surface of an FET, where G denoted gate, D drain, and S source.

gate electrode. The situation is described a bit more in Fig. 19, where bias voltages are defined and a typical I–V curve for DC operation is given. Typically the bias would be supplied by a circuit such as that of Fig. 20. In what follows, we will simply assume that the biases are properly applied and isolated and consider the AC operation. An AC circuit model is given in Fig. 21. If one uses the proper number of circuit values, these models can be quite accurate, but the values do vary from device to device, even when the devices were fabricated at the same time and even on the same substrate. Usually, the datasheet with a device will, instead of specifying the circuit parameters, specify the device S parameters, which are defined as in Fig. 22 and can be measured in a straightforward manner by a network analyzer. The S parameters are defined by the equation

$$\begin{pmatrix} V_1^- \\ V_2^- \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} V_1^+ \\ V_2^+ \end{pmatrix}. \tag{5}$$

An important parameter is the transfer function of the transistor circuit, which can be defined as the ratio of the v_o to the v_i as defined in Fig. 21. To simplify further analysis, we will ignore the package parasitics R_g and R_d with respect to other circuit parameters, and thereby we will carry out further analysis on the circuit depicted in Fig. 23. The circuit can be solved by writing a simultaneous system of equations for the two nodal voltages v_i and v_o. These sinusoidal steady-state equations become

$$v_i = v$$

$$j\omega C_{gd}(v_o - v_i) + g_m v_i + j\omega C_{ds} v_o + \frac{v_o}{R_{ds}} + \frac{v_o}{Z_L} = 0$$

The system can be rewritten in the form

$$v_o\left[j\omega(C_{gd} + C_{ds}) + \frac{1}{R_{ds}} + \frac{1}{Z_L}\right] = v_i[-g_m + j\omega C_{gd}]$$

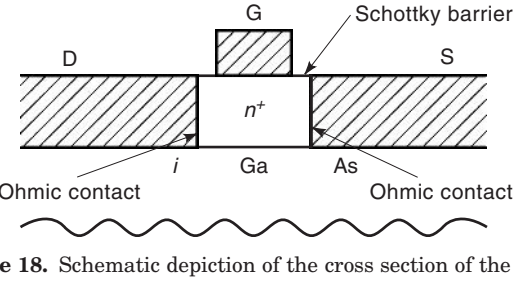

Figure 18. Schematic depiction of the cross section of the active region of a GaAs FET, Specific designs can vary significantly in the field-effect family.

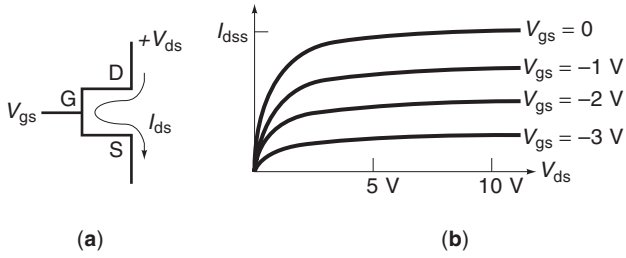

Figure 19. (a) Circuit element diagram with voltages and currents labeled for (b), where a typical *I–V* curve is depicted.

which gives us our transfer function T in the form

$$T = \frac{v_o}{v_i} = \frac{-g_m + j\omega C_{gd}}{j\omega(C_{gd} + C_{gs}) + \dfrac{1}{R_{ds}} + \dfrac{1}{Z_L}}$$

Often we are interested in open-circuit parameter—that is, the circuit transfer function when Z_L is large compared to other parameters. We often call this parameter G the *open-circuit gain*. We could write this open-circuit gain in the form

$$G = \left.\frac{v_o}{v_i}\right|_{oc} = \frac{-g_m R_{ds} + j\omega C_{gd} R_{ds}}{j\omega(C_{gd} + C_{gs})R_{ds} + 1}$$

It is useful to look at approximate forms. It is generally true that

$$C_{gd} \ll C_{ds}, C_{gs}$$

but for usual operating frequencies it is also generally true that

$$\frac{1}{\omega C_{ds}} \ll R_{ds}$$

Using both of the equations in our equations for T and G, we find

$$T = \frac{-g_m R_{ds}}{1 + \dfrac{R}{Z_L}}$$

$$G = -g_m R_{ds}$$

Clearly, one sees that the loaded gain will be less than the unloaded gain, as we would expect. Making only the first of our two approximations above, we can write these

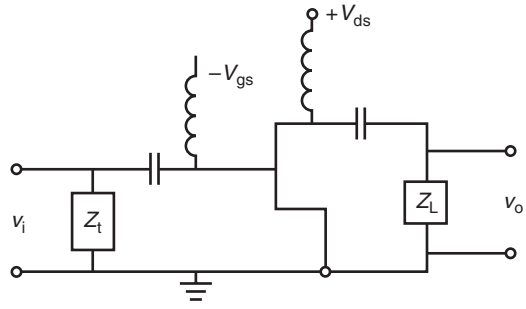

Figure 20. Typical FET circuit including the bias voltages v_{gs} and v_{ds} as well as the AC voltages v_i and v_0, where the conductors represent AC blocks and the capacitors DC blocks.

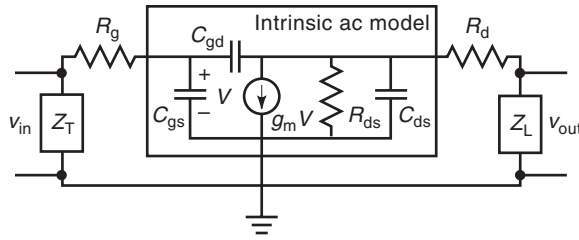

Figure 21. Intrinsic model for a common-source FET with external load and termination impedances and including gate and drain resistive parasitics, where Z_T is the gate termination impedance, R_g is the gate (metallization) resistance, C_{gs} is the gate-to-source capacitance, C_{gd} is the gate-to-drain capacitance, g_m is the channel transconductance, R_{ds} is the channel (drain-to-source) resistance, C_{ds} is the channel capacitance, R_d is the drain (metallization) resistance, and Z_L is the load impedance.

equations as

$$T = \frac{-g_m R_{ds}}{1 + j\omega\tau_{ds} + \dfrac{R_{ds}}{Z_L}}$$

$$G = \frac{-g_m R_{ds}}{1 + j\omega\tau_{ds}}$$

where the τ_{ds} is a time constant given by

$$\tau_{ds} = \frac{1}{C_{ds} R_{ds}}$$

We see that, in this limit, the high-frequency gain is damped. Also, an interesting observation could be that, at some frequency ω, an inductive load could be used to cancel the damping and obtain a purely real transfer function at that frequency. This effect is the one that allows us to use the transistor in an oscillator.

Let us now consider an oscillator circuit. The basic idea behind the oscillator circuit is illustrated in the one-port diagram of Fig. 24. The transistor's gain, together with feedback to the input loop through the capacitor C_{gd}, can give the transistor an effective negative input impedance that can lead to oscillation if the real and imaginary parts of the total impedance (i.e., Z_T in parallel with the Z_i of the transistor plus load) cancel. The idea is much like that illustrated in Fig. 25 of a feedback network. One sees that the output of the feedback network can be expressed as

$$v_o = G(j\omega)[v_i - H(j\omega)v_o]$$

or, by rearranging terms, one finds that

$$\frac{v_o}{v_i} = \frac{G(j\omega)}{1 + G(j\omega)H(j\omega)}$$

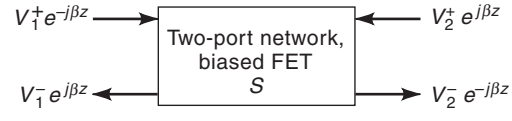

Figure 22. Schematic depiction of an FET as a two-port device that defines the quantities used in the S matrix of Eq. (5).

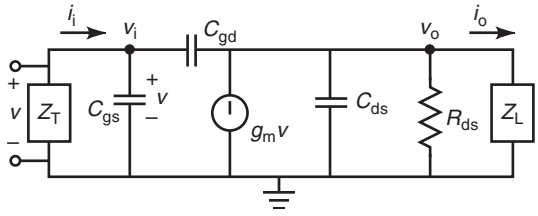

Figure 23. Simplified transistor circuit used for analyzing rather general amplifier and oscillator circuits, where the circuit parameter definitions are as in Fig. 22.

which clearly will exhibit oscillation—that is, have an output voltage without an applied input voltage—when

$$H(j\omega) = -\frac{1}{G(j\omega)}$$

What we need to do to see if we can achieve oscillation is to investigate the input impedance of our transistor and load seen as a one-port network. Clearly we can write the input current of Fig. 23 as

$$i_i = j\omega C_{gs} v_i + j\omega C_{gd}(v_i - v_o)$$

and then using the full expression for T to express v_o as a function of v_i, one finds

$$Z_i = \frac{i_i}{v_i} = j\omega C_{gs} + j\omega C_{gd}\left(1 + \frac{g_m - j\omega C_{gd}}{j\omega(C_{gd} + C_{ds}) + \dfrac{1}{R_{ds}} + \dfrac{1}{Z_L}}\right)$$

which can be somewhat simplified to yield

$$Z_i = j\omega C_{gs} + j\omega C_{gd}\left[\frac{g_m R_{ds} + 1 + j\omega\tau_{ds} + \dfrac{R_{ds}}{Z_L}}{1 + j\omega\tau_{ds} + \dfrac{R_d}{Z_L}}\right]$$

We can again invoke a limit in which $\omega\tau_{ds} \ll 1$ and then write

$$Z_i = j\omega C_{gs} + j\omega C_{gd}\left[\frac{Z_L(1 + g_m R_{ds} + R_{ds})}{R_{ds} + Z_L}\right]$$

Perhaps the most interesting thing about this expression is that one notes that if

$$Z_L = j\omega L$$

and

$$g_m R_{ds} \gg 1$$

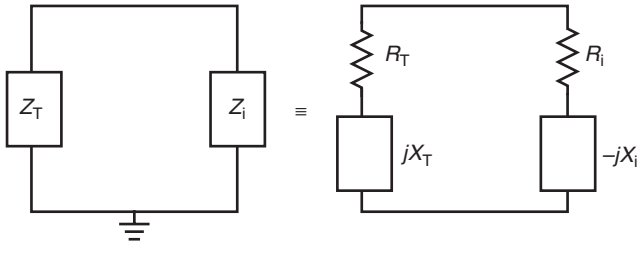

Figure 24. Diagram depicting the transistor and its load as a one-port device that, when matched to its termination so that there is no real or imaginary part to the total circuit impedance, will allow for oscillations.

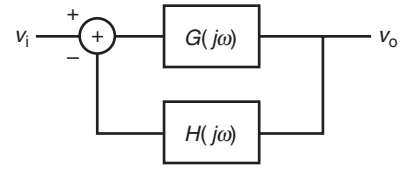

Figure 25. Depiction of a simple feedback network.

then clearly

$$R_i < 0$$

Whether X_i can be made to match any termination is another question that we will take up in the next paragraph.

As was mentioned earlier, generally the datasheet one obtains with an FET has plots of the frequency dependence of the S parameters rather than values for the equivalent-circuit parameters. Oscillator analysis is, therefore, usually carried out using a model of the circuit such as that depicted in Fig. 26, where the transistor is represented by its measured **S** matrix. The condition for oscillation in such a system can be expressed in either of the forms

$$\Gamma_i \Gamma_T = 1$$

or

$$\Gamma_o \Gamma_L = 1$$

where the Γs are as defined in the caption of Fig. 26. If both Z_T and Z_L were passive loads—that is, loads consisting of resistance, inductance, and capacitance, then we would have that

$$|\Gamma_T| < 1$$
$$|\Gamma_L| < 1$$

and the conditions for unconditional stability (nonoscillation at any frequency) would be that

$$|\Gamma_i| < 1$$
$$|\Gamma_o| < 1$$

Clearly, we can express Γ_i and Γ_o as series of reflections such that

$$\Gamma_i = S_{11} + S_{12}\Gamma_L S_{21} + S_{12}\Gamma_L S_{22}\Gamma_L S_{21}$$
$$+ S_{12}\Gamma_L S_{22}\Gamma_L S_{22}\Gamma_L S_{21} + \cdots$$
$$\Gamma_o = S_{22} + S_{21}\Gamma_T S_{12} + S_{21}\Gamma_T S_{11}\Gamma_T S_{12}$$
$$+ S_{21}\Gamma_T S_{11}\Gamma_T S_{11}\Gamma_T S_{12} + \cdots$$

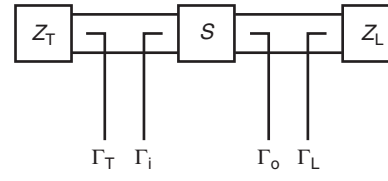

Figure 26. Schematic depiction of an oscillator circuit in which the transistor is represented by its S matrix and calculation is done in terms of reflection coefficients Γ_T looking into the gate termination, Γ_i looking into the gate source port of the transistor, Γ_o looking into its drain source port, and Γ_L looking into the load impedance.

Using the fact that

$$\sum_{n=0}^{\infty} x^n = \frac{1}{1-x}$$

we can reexpress the Γs as

$$\Gamma_{\mathrm{i}} = S_{11} + \frac{S_{12}S_{21}\gamma_{\mathrm{L}}}{1 - S_{22}\Gamma_{\mathrm{L}}}$$

$$\Gamma_{\mathrm{o}} = S_{22} + \frac{S_{12}S_{21}\Gamma_{\mathrm{T}}}{1 - S_{22}\Gamma_{\mathrm{T}}}$$

If we define the determinant of the **S** matrix to be Δ and be given by

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

and a transistor κ parameter by

$$\kappa = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}$$

then some tedious algebra leads to the result that stability requires

$$\kappa > 1$$

$$\Delta < 1$$

At frequencies where these condition are not satisfied, oscillation can occur if the load and termination impedances, Z_{L} and Z_{T}, respectively, are chosen properly. Oscillator design is discussed in various texts [11,14–16]. Generally, though, oscillator design involves finding instability points and not predicting the dynamics once oscillation is achieved. The next paragraph will discuss these dynamics.

If a transistor circuit is designed to be unstable, then as soon as the DC bias is raised to a level whereby the circuit achieves the set of unstable values, the circuit's output within the range of unstable frequencies rises rapidly and dramatically. The values that we took in the equivalent AC circuit, though, were small-signal parameters. As the circuit output increases, the signal will eventually no longer be small. The major thing that changes in this limit is that the input resistance to the transistor saturates, such that [17,18]

$$R_{\mathrm{i}} = -R_{\mathrm{i}\phi} + mv^2$$

where the plus sign on the nonlinearity is necessary, for if it were negative the transistor would burn up or else burn up the power supply. Generally, the m has to be determined empirically, as nonlinear circuit models have parameters that vary significantly from device to device. For definiteness, let's assume that the Z_{T} is resistive and the Z_{L} is purely inductive. At the oscillation frequency, the internal capacitance of the transistor then should cancel the load inductance, but to consider dynamics we need to put in both the C and L, as dynamics take place in the time domain. The dynamic circuit to consider is then as depicted in Fig. 27. The loop equation for this circuit in the time domain would be

$$L\frac{\partial i}{\partial t} + (R_{\mathrm{i}} + R_{\mathrm{T}})i + \frac{1}{C}\int i\,dt = 0$$

Recalling the equivalent circuit of Fig. 23 and recalling that

$$C_{\mathrm{gs}} \gg C_{\mathrm{gd}}$$

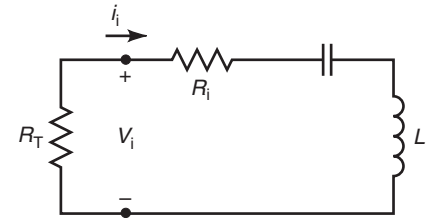

Figure 27. Circuit used to determine the dynamical behavior of a transistor oscillator.

we see that, approximately at any rate, we should have the relation between v_{i} and i_{i} that

$$i = C_{\mathrm{gs}}\frac{\partial v}{\partial t}$$

Using this $i - v$ relation in the preceding, we find that

$$\frac{\partial^2 v}{\partial t^2} - \frac{R_{\mathrm{i}} - R_{\mathrm{T}}}{L}\left(1 - \frac{mv^2}{R_{\mathrm{i}} - R_{\mathrm{T}}}\right)\frac{\partial v}{\partial t} + \frac{v}{LC} = 0$$

which we could rewrite in terms of other parameters as

$$\frac{\partial^2 v}{\partial t^2} - \varepsilon(1 - \gamma^2 v^2)\frac{\partial v}{\partial t} + \omega_0^2 v = 0$$

which is the form of Van der Pol's equation (see, e.g., Refs. 17 and 18), which is an equation that describes the behavior of essentially any oscillator.

Now that we have discussed planar guiding structures and at least one example of a dynamical element that we can insert into a planar circuit, the time has arrived to discuss the planar antenna structures. Perhaps the best way to gain understanding of the operation of a patch antenna is by considering a cavity resonator model of one. A good review of microstrip antennas is given in Carver and Mink [19] and is reprinted in Ref. 20. Let's consider a patch antenna and coordinate system as is illustrated in Fig. 28. The basic idea behind the cavity model is to consider the region between the patch and ground plane as a resonator. If the resonator were a perfect one, an idealized set of boundary conditions would be satisfied that would allow no exchange of energy between the resonator and its surroundings. In actual operation, it is the inaccuracy of the idealized boundary conditions that gives rise to the transduction mechanism whereby an antenna can convert

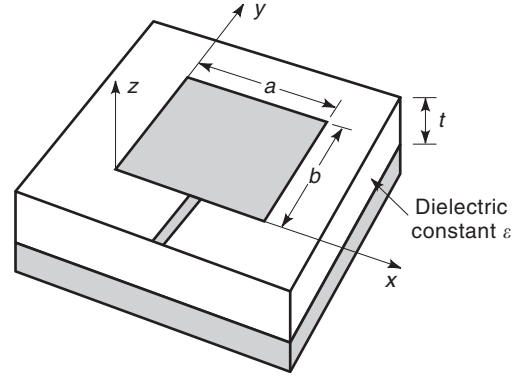

Figure 28. A patch antenna and Cartesian coordinate system.

guided waves to radiated a waves and vice versa. We will assume the idealized conditions that there is only a z-directed electric field underneath the patch and that this field achieves maxima on the edges (open-circuit boundary condition). The magnetic field will be assumed to have both and H_x and H_y components (only an H_x component in what we call the fundamental mode), and tangential components of these on the edges will be zero. (This boundary condition is the one consistent with the open circuit condition on the electric field and is exact as the thickness of the layer approaches zero, as there can be no component of current normal to the edge at the edge, and it would be the normal component of the current that generates the transverse **H** field.) The electric field satisfying the open circuit condition can be seen to be given by the modes

$$e_{mn} = \frac{\chi_{mn}}{\sqrt{\varepsilon abt}} \cos k_n x \cos k_m y$$

where

$$k_n = \frac{n\pi}{a}$$

$$k_m = \frac{m\pi}{b}$$

$$\chi_{mn} = \begin{cases} 1, & m = 0 \text{ and } n = 0 \\ \sqrt{2}, & m = 0 \text{ or } n = 0 \\ 2, & m \neq 0 \text{ and } n \neq 0. \end{cases}$$

The **H** field corresponding to the **E** field then will consist of modes

$$\mathbf{h}_{mn} = \frac{1}{j\omega\mu} \frac{\chi_{mn}}{\varepsilon abt} [\hat{e}_x k_m \cos k_n x \sin k_m y - \hat{e}_y k_n \sin k_n x \cos k_m y]$$

Now what we will call the fundamental mode is the one with $m = 1$ and $n = 0$. We can excite such a mode by choosing the dimension b to be resonant, that is, to correspond to a half of a wavelength in the structure. The dimension transverse to this must then be chosen to be nonresonant. This can be achieved by, for example, making this dimension less than a half-wavelength, but this is not the only way by any means. Now the basic transduction operation of the antenna must be due to the fact that the boundary conditions are not quite exact and the antenna can accept energy from the feedline and radiate it into free space. Let us consider this transduction operation in the antenna's fundamental mode. One might recall from the earlier argument that accompanied Fig. 13 that the z-directed field gives rise to a fringe field at the edges $y = 0$ and $y = b$ such that there are strips of y-directed electric field at the substrate surface for $y \leq 0$ and $y \geq b$. Because the boundary conditions are not quite correct on **H**, there will also be strips of x-directed magnetic fields in these regions. As the Poynting vector is given by $\mathbf{E} \times \mathbf{H}$, we note that these strips will give rise to a z-directed Poynting vector at each of these edges. As these edges are a half-wavelength apart and the fields are in phase and Poynting-vector-like directed, these radiating edges will give rise to an upward-radiated field. Similar arguments could be applied to the edges at $x = 0$ and $x = a$. However, the x-directed field at $x \leq 0$ has a change of sign at the middle of the edge and is pointwise oppositely directed from the x-directed electric field at $x \geq a$. These fields, therefore, only give rise to very weak radiation, as there is significant cancellation. Analysis of the slot antenna requires that we first interchange the role if the **E** and **H** fields and realize that the radiating edges in the case of the slot are the edges that are along the direction of the feedline structure. Thus, in the CPW structure, the dominant electric fields are in the gaps between the conductors while the dominant magnetic field in the gaps points into the substrate. The end of the center conductor splits the downward-pointing magnetic field into two phases, one to the right of the center conductor and one to the left, defining the radiating edges of the structure in terms of the null of the z-directed magnetic field.

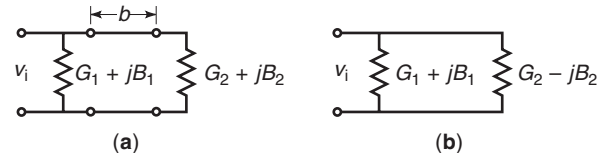

Figure 29. (a) A transmission-line model for a patch antenna, and (b) its circuital equivalent as resonance.

The picture of the patch antenna as two radiating strips allows us to represent it with a transmission line as well as a circuit model. The original idea is due to Munson [21]. The transmission line model is depicted in Fig. 29. The idea is that one feeds onto an edge with an admittance (inverse impedance) of $G_1 + jB_1$ and then propagates to a second edge with admittance $G_2 + jB_2$. When the circuit is resonant, then the length of transmission line will simply complex conjugate the given load [see Eq. (4)], leading to the circuit representation of Fig. 29b. The slot admittance used by Munson [21] was just that derived for radiation from a slit in a waveguide [22] as

$$G_1 + jB_1 = \frac{\pi a}{\lambda_0 Z_0} [1 - j0.636 \ln k_0 t]$$

where Z_0 is the impedance of free space of $377\Omega(\sqrt{\pi_0/\varepsilon_0})$, λ_0 is the free-space wavelength, and k_0 is the free-space propagation vector, and where a and t are defined as per Fig. 28. When the edges are identical (as for a rectangular patch), one can write

$$G_2 + jB_2 = G_1 + jB_1$$

to obtain the input impedance in the form

$$Z_i = \frac{1}{Y_i} = \frac{1}{2G_1}$$

We have now considered all of the pieces, and therefore it is time to consider a couple of actual active-antenna designs. Figure 30 depicts one of the early designs from Kai Chang's group at Texas A&M [23]. Essentially, the patch here is being used precisely as the feedback element of an amplifier circuit (as was described in combination with Fig. 9). A more compact design is that of Fig. 14 [9]. There, the transistor is actually mounted directly into the patch antenna. The slit between the gate and drain yields a

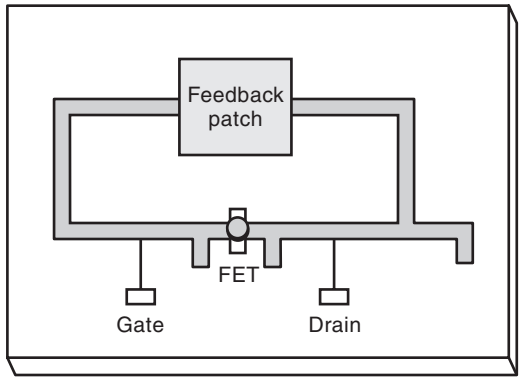

Figure 30. A design of a microstrip active radiating element.

capacitive feedback element such that the effective AC circuit equivalent of this antenna might well appear as depicted in Fig. 31. The capacitor/inductor pair attached to the gate lead form what is often referred to as a *tank circuit*, which (if the load were purely real) defines a natural frequency through the relation

$$\omega = \sqrt{\frac{1}{LC}}$$

As was discussed at some length in Section 1, a major argument for the use of active antennas is that they are sufficiently compact that they can be arrayed together. Arraying is an important method for free-space power combining, which is necessary due to the fact that, as frequency increases, the power-handling capability of active devices decreases. However, element size also decreases with increasing frequency such that use of multiple coherently combined elements can allow one to fix total array size and power more or less independently of frequency even though the number of active elements to combine increases. In the next paragraph, we'll consider some of the basics of arrays. The interested reader might also want to consult a relatively recent review article [10].

Consider a linear array such as is depicted in Fig. 32. Now let's say that the elements are nominally identical apart from phases that are set by the array operator at each of the elements. The complex electric field far from the nth element due to only the nth element would then be given by

$$\mathbf{E}_n = \mathbf{E}_e e^{i\phi_n}$$

where the $\mathbf{E}_e$ is the electric field of a single element. To find out what is radiated in the direction θ due to the whole array, we need to sum the fields from all of the radiators, giving each radiator the proper phase delay. Each element will get a progressive phase shift $kd \sin\theta$ due to its position (see Fig. 32), where k is the free-space propagation factor, given by

$$k = \frac{2\pi}{\lambda}$$

where λ is the free-space wavelength. With this, we can write for the total field radiated into the direction θ due to all n elements

$$\mathbf{E}_t(\theta) = \mathbf{E}_e \sum_{n=0}^{N-1} e^{-inkd\sin\theta} e^{i\phi_n}$$

The sum is generally referred to as the *array factor*. The intensity, then, in the θ direction is

$$I_t(\theta) = I_e \left| \sum_{n=0}^{N-1} e^{-inkd\sin\theta} e^{i\phi_n} \right|^2$$

One notes immediately that, if one sets the phases ϕ_n to

$$\phi_n = nkd\sin\theta$$

then the intensity in the θ direction is N^2 times the intensity due to a single element. This is the effect of coherent addition. One gets a power increase of N plus a directivity increase of N. To illustrate, let's consider the broadside case where we take all the ϕ_n to be zero. In this case, we can write the array factor in the form

$$\left| \sum_{n=0}^{N-1} e^{-ind\sin\theta} \right|^2 = \left| \frac{1 - e^{-iNkd\sin\theta}}{1 - e^{-ikd\sin\theta}} \right|^2$$

which in turn can be written as

$$\mathrm{AF} = \frac{\sin^2\left(N\frac{kd}{2}\sin\theta\right)}{\sin^2\left(\frac{kd}{2}\sin\theta\right)} \tag{6}$$

which is plotted in Fig. 33. Several interesting things can be noted from the expression and plots. One thing to note is that, for kd less than π, there is only one central lobe in the pattern. Another thing to note is that the pattern becomes increasingly directed with increasing N. This is just the directivity effect. If the array had a power-combining

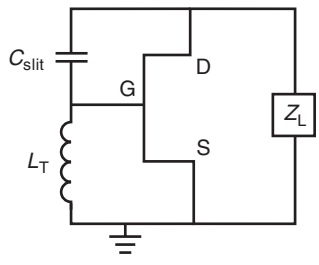

Figure 31. AC circuit equivalent of the active antenna of Fig. 14.

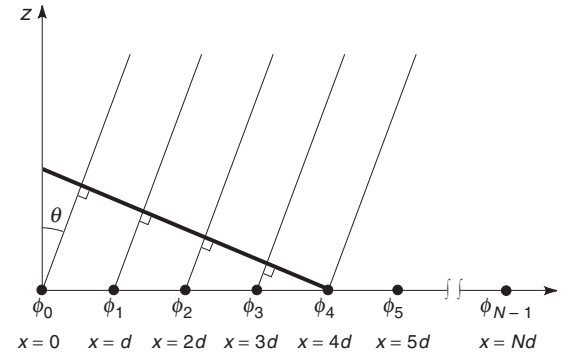

Figure 32. Depiction of a linear array of N identical radiating elements.

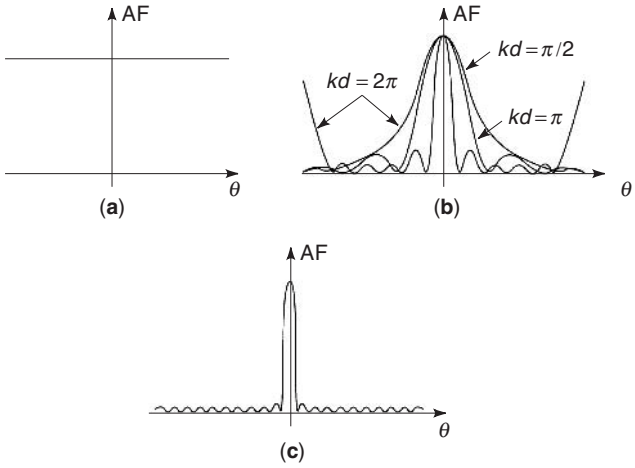

Figure 33. Plots of the array factor of Eq. (6), where (a) $N=1$, (b) $N=5$ and $kd=\pi/2$, π, and 2π, and (c) $N=10$ and $kd=\pi$.

efficiency of 100% (which we have built into our equations by ignoring actual couplings, etc.), then the total power radiated could only be N times that of a single element. However, it is radiated into a lobe that is only $1/N$ times as wide as that of a single element.

If we are to realize array gain, however, we need to be certain that the array elements are identical in frequency and have fixed phase relations in time. This can only take place if the elements are locked together. The idea of locking is probably best understood in relation to the Van der Pol equation [24–26], with an injected term, such that

$$\frac{\partial^2 v}{\partial t^2} - \frac{R_{i\phi} - R_T}{L}\left(1 - \frac{mv^2}{R_{i\phi} - R_T}\right)\frac{\partial v}{\partial t} + \omega_0^2 v = A\cos\omega_i t$$

where $R_{i\phi}$ is the input resistance of the transistor circuit as seen looking into the gate–source port and R_T is the external termination resistor placed between the gate and the common source. In the absence of the locking term, one can see that oscillation will take place with a primary frequency (and some harmonics) at angular frequency ω_0 with amplitude $\sqrt{R_{i0} - R_T/m}$ such that

$$v(t) \approx \sqrt{\frac{R_{i0} - R_T}{m}}\cos(\omega_0 t)$$

Without being too quantitative, one can say that, if ω_i is close enough to ω_0 and A is large enough, the oscillation will lock to ω_i in frequency and phase. If ω_i is not quite close enough and A not quite big enough (how big A needs to be is a function of how close ω_i is), then the oscillation frequency ω_0 will be shifted such that

$$v(t) = A_0\cos((\omega_0 + \Delta\omega)t + \phi)$$

where $\Delta\omega$ and ϕ are functions of ω_i and A. These ideas are discussed in a number of places, including Refs. 1,17,18, and 24–26. In order for our array to operate in a coherent mode, the elements must be truly locked. This locking can occur through mutual coupling or through the injection of an external signal to each of the elements.

Ideally, we would like to be able to steer the locked beam. A number of techniques for doing this are presently under investigation. A reasonably recent review article covering such techniques is [27]. Much of the thinking stems from the work of Stephan and coworkers [28–31]. One of the ideas brought out in these works was that, if the array were mutually locked and one were to try to inject one of the elements with a given phase, all the elements would lock to that phase. However, if one were to inject two elements at the locked frequency but with different phases, then the other elements would have to adjust themselves to these phases. In particular, if one had a locked linear array and one were to inject the two end elements with phases differing by ϕ, then the other elements would equally share the phase shift such that there would be a linear phase taper of magnitude ϕ uniformly distributed along the array. A different technique was developed by York [32,33] based on work he began when working with Compton [34,35]. In this technique, instead of injecting the end elements with the locked frequency and different phase, one injects the array with frequencies that are detuned from the desired center frequency. If the amplitudes of these injected frequencies are set to values that are not strong enough to lock the elements to these injected frequencies, then the elements would retain their "free-running" frequencies, but would obtain phase shifts from the injected signal as the oscillation within the element attempts to satisfy the contradictory operation instructions that are being fed to the element. If the elements of the array were locked because of mutual feedback, trying to inject either end of the array with "detuned" frequencies would then tend to give the elements a linear taper—that is, one in which the phase varies linearly with distance down the array—with much the same result as the technique of Stephan [28–31]. This will just linearly steer the mainlobe of the array off broadside and to a new direction. Such linear scanning is certainly what is needed for many commercial applications such as tracking or transmitting with minimum power to a given location. Another technique that again uses the locking-type ideas is the technique of changing the biases on each of the array's active devices [36–38]. Changing the bias of a transistor will alter the free-running frequency at which the active antenna wants to oscillate. For an element locked to another frequency, then, changing the bias will just change the phase. In this way one can individually set the phase on each element. There are problems with this approach (as with all the others to present, which is why this area is still one of active research). One is that addressing each bias line represents a great increase in the complexity that we were trying to minimize by using an active antenna solution. The other is that the maximum phase shift obtainable with this technique is $\pm\pi$ from one end of the array to the other, a limitation that is shared by the phase shifts at the ends technique. In many phased array applications, of which electronic warfare is a typical one, one wants to have "true time delay," which means that one would like to have as much as a π phase shift between adjacent elements. Essentially none of the techniques addressed to present can seem able to satisfy this requirement. Yet true time delay could open up a set new set of applications that could further drive work in this area. Work, however, continues. But already the

discussion has impinged on the topic of the next section, that of future application areas, and, therefore, now is a propitious time to begin this third section.

3. APPLICATIONS OF AND PROSPECTS FOR ACTIVE ANTENNAS

As was discussed earlier, active antennas were the first antennas of Hertz [4] although perhaps the greatest driver of more recent advances in this area has been power combining at high frequencies [10]. The power-combining area is becoming a subarea of high-power microwave/millimeter-wave devices by itself. However, there are numerous motivations other than simple power combining to pursue the study of active antennas. In this section, the aim is to run through a whole potpourri of past, present, and future applications. The applications to be touched on in this section are by no means exhaustive, but hopefully are representative.

Perhaps the earliest application of the active-antenna concept (following that of Hertz) was aimed at solving the small-antenna problem. As we recall, an antenna can be modeled (roughly) by a series *RLC* network with the *R* representing the radiation resistance. The input impedance of such a combination is given by

$$Z_{\mathrm{i}} = \frac{1 - \dfrac{\omega^2}{\omega_0^2} + j\omega RC}{j\omega C}$$

and so we see that, when the operation frequency ω is well below the resonant frequency

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

and the inverse of the *RC* time constant

$$\tau = RC$$

then the antenna appears as a capacitor and radiates quite inefficiently. The problem of reception is similar. Apparently, already in 1928 Westinghouse had a mobile antenna receiver that used a pentode as an inductive loading element in order to boost the amount of low-frequency radiation that could be converted to circuit current. In 1974, two works discussed transistor-based solutions to the short aerial problem [39,40]. In Ref. 40, the load circuit appeared as in Fig. 34. The idea was to generate an inductive load whose impedance varied with frequency, unlike a regular inductor, but so as to increase antenna bandwidth. The circuit's operation is not intuitively obvious. It is possible that most AM, shortwave, and FM receivers employ some short antenna solution regardless of whether the actual circuit designers are aware that they are employing active antenna techniques.

More recent efforts aimed at miniaturization have been concentrated on efficient amplification by single active-antenna elements rather than solving the small-antenna problem. For example, handheld wireless communication requires not only compact antenna elements but also compact and efficient amplification at the element. High-efficiency F class amplifiers were already under study in

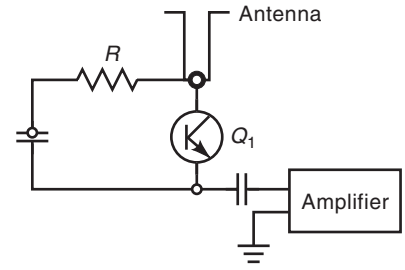

Figure 34. A circuit taken from Ref. 37 in which a transistor circuit is used to load a short antenna. Analysis shows that, in the frequency regime of interest, the loading circuit appears, when looking toward the antenna from the amplifier terminals, to cancel the strongly capacitive load of the short antenna.

1993 [41] followed by studies of lower-frequency class E amplifiers [42]. Efforts at fabricating integrated active-antenna elements employing high efficiency amplifiers have used resonant (if modified) patch elements, and have therefore in order to remain compact have carried out demonstrations at higher frequencies (S and C bands) where the resonant patches are more compact because of the smaller wavelengths, as is evidenced by work at Tatsuo Itoh's group at UCLA in [43,44]. Kalialakis et al. attempted to make the active antenna not only efficient but also duplex and thereby a candidate for a transceiver [45].

Another set of applications where active devices are used as loading elements is in the >100-GHz regime. Developments in this regime are reviewed in Refs. 1 and 46. To date, most work at frequencies greater than 100 GHz has involved radioastronomical receivers. A problem at such frequencies is a lack of components, including circuit elements so basic as waveguides. Microstrip guides already start having extramode problems at Ku band. Coplanar waveguides can go higher, although to present, rectangular metallic waveguides are the preferred guiding structures past about 60 GHz. In W band (normally narrowband, about 94 GHz—see Table 1), there are components, as around 94 GHz there is an atmospheric window of low propagation loss. However, waveguide tolerances, which must be a small percentage of the wavelength, are already severe in W band, where the wavelength is roughly 3 mm. Higher frequencies pretty much have to be handled in free space or, as one says, quasioptically. Receivers must therefore by nature be downconverting in this >100 GHz regime. Indeed, these types of solutions are the ones being demonstrated by the group at Michigan [46], where receivers will contain multipliers and downconverting mixers right in the antenna elements in order that CPW can be used to carry the downconverted signals to the processing electronics. Millimeter-wave/terahertz radioastronomy seems to be a prime niche for quasioptical active-antenna solutions.

The first applications of active antennas where solid-state components were used as gain elements were for power boosting [47–52]. By 1960, solid-state technology had come far enough that antennas integrated with diodes and transistors could be demonstrated. These early demonstrations of *antennafiers* [48] could be considered as the precursors of the high-efficiency integrated antennas we

mentioned in an earlier paragraph, but judging from the reference lists of these more recent works [43,44], there doesn't seem to be much of causal relationship. In fact, this early integrated active-antenna technology was to remain a laboratory curiosity per se until the 1980s, when further improvements in microwave devices were to render the technology more practical. The motivation at that point in time was primarily large gain. Large power gain, however, really requires combining the outputs of multiple solid-state devices. Power combining (see reviews in Refs. 10, 53, and 54), though, can be hard to achieve. There is a theorem that grew out of the early days of radiometry and radiative transfer (in the 1800s) known variously as the *brightness theorem*, the *Lagrange invariant*, or later the (later) *second law of thermodynamics*. (See, for example, Ref. 55 for some discussion of the Lagrange invariant.) The theorem essentially states that one cannot increase the brightness of a source by passive means. This theorem practically means that if one tries to combine two nominally identical but non-phase-locked sources by taking their outputs, and attempting to launch those two outputs into the same direction in space such that the two beams occupy the same spatial location in space, the resulting power density per steradian can be no greater than that of either of the nominally identical sources. Other power that was intended to go into this desired direction will have gone in some other direction. This seems to preclude any form of power combining. There is a proviso here, though. At the time the brightness theorem was first formulated, there were no coherent radiation sources. If one takes the output of a coherent radiation source, splits it in two, and adds it back together in phase, then the brightness, which was halved, can be restored. If two sources are phase locked, they are essentially one source. Therefore, locked sources can be coherently added if they are properly phased. A major portion of the power-combining field is therefore associated with techniques to lock individual radiating elements together into coherent sources and/or to amplify the output of weak sources in arrays of devices that lock to the source and to each other. It turns out that a powerful method with which to carry out such power combining employs the techniques that are generally referred to as *free-space power combining*.

A number of groups are working on developing compact elements for free-space power combining. Examples of free-space power-combining schemes have already appeared in Fig. 14 [9] and 30 [22]. In designs where the elements are spatially packed tightly enough, proximity can lead to strong enough nearest-neighbor coupling so that an array will lock to a common frequency and phase. Closeness of elements is also desirable in that arrays with less than $\lambda/2$ spacing will have no sidelobes sapping power from the central array beam. In designs that don't self-lock, one must either inject a locking signal on bias lines or spatially from a horn to try to lock to all elements simultaneously. A method for carrying out power combining in a self-locking array is to use the so-called *grid oscillator* solution [56,57]. The actual structure of a grid appears as in Fig. 35. The operating principle of the grid is actually quite a bit different from that of the arrays of weakly coupled individual elements. Note that there is no ground

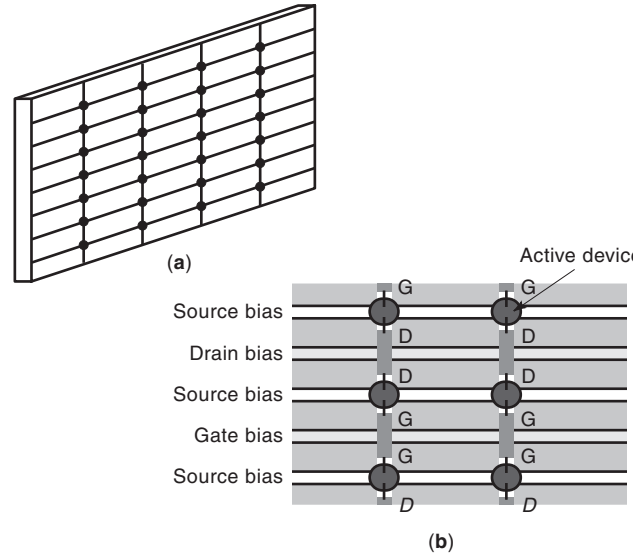

Figure 35. Schematic depiction of (a) the active surface of a grid oscillator and (b) a breakout of an internal region of the grid showing the active device placement relative to the bias lines.

plane at all on the back, and there is no ground plane either, per se, on the front side. Direct optical measurements of the potentials on the various lines of the grid [58], however, show that the source bias lines act somewhat as AC grounds. In this sense, either a drain bias line, together with the two closest source biases, or a gate bias line together with the two horizontally adjacent bias lines appears somewhat like CPW. The CPW lines, however, are periodically loaded ones with periodic active elements alternated with structures that appear like slot antennas. The radiating edges of the slots are, for the drain bias lines, the vertical AC connection lines between drain and drain or, for the gate bias CPW, the horizontal AC gate-to-gate convection lines. Indeed, the grid is known to lock strongly along the rows and more weakly between columns. As adjacent-row elements are sharing a patch radiator, this should be expected behavior. In a major sense, this strong locking behavior of the grid is both an advantage and a disadvantage. It is advantageous that the grid is compact (element spacing can be $\leq \lambda/6$) and further that it is easy to get the rows to lock to each other. However, the compactness is also a disadvantage in that it is quite hard to get any more functionality on the grid. Much effort has been given in this area to generate functionality by stacking various grid-based active surfaces such as amplifying surfaces, varactor surfaces for frequency shifting and modulation, or doubling surfaces. A problem with stacking is, of course, diffraction as well as alignment. Alignment tolerance adds to complexity. Diffraction tends to ease alignment tolerance, but in an inelegant manner. A 100-transistor array with $\lambda/6$ spacing will have an extent of roughly 1.5λ per side. As the diffraction angle is something like the wavelength divided by the array diameter, the diffraction angle for such an array is a major portion of a radian. One can say that grids are quasioptical, but in optics one seldom uses apertures too much smaller than a millimeter, for which the diffraction angle

would be roughly a thousandth of a radian. As far as pure combining efficiency goes, grids are probably the optimal solution. However, more functionality may well be hard to obtain with this solution. But then, as was previously mentioned, free-space power combining is itself becoming a subarea of high-power microwave/millimeter-wave sources as is evidenced by a review article [10].

Another application area of active antennas is that of proximity detection [59]. The idea is that an oscillator in an antenna element can be very sensitive to its nearby (within several wavelengths) environment. As was discussed previously, variation in distances to ground planes change impedances. The proximity of any metal object will, to some extent, cause the oscillator to be aware of another ground plane in parallel with the one in the circuit. This will change the impedance that the oscillator sees and thereby steer the oscillator frequency. The active antenna of Ref. 59 operated as a self-oscillating mixer; that is, the active element used the antenna as a load, whereas the antenna also used a diode mixer between itself and a low-frequency external circuit. The antenna acted both as a transmitting and receiving antenna. If there were something moving near the antenna, the signal reflected off the object and rereceived might well be at a different frequency than the shifting oscillator frequency. These two frequencies would then beat in the mixer, be downconverted, and show up as a low-frequency beat note in the external circuit. If such a composite device were to be used in a controlled environment, one could calibrate the output to determine what is occurring. Although Navarro and Chang [1, p. 130] mention such applications as automatic door openers and burglar alarms, I personally don't know how far the technology has gone into such commercial application. The original paper [59], though, seemed to have a different application in mind, as the term *Doppler sensor* appeared in the title. If one were to carefully control the immediate environment of the self-oscillating mixer, then reflections off more distant objects received by the antenna would beat with the stable frequency of the oscillator. The resulting beat note of the signals would then be the Doppler shift of the outgoing signal on reflection off the surface of the moving object, and from it one could determine the normal component of the object's velocity. It is my understanding that some low-cost radars operate on such a principle. As with other applications, though, the active-antenna principle, if due only to size constraints, becomes even more appealing at millimeter-wave frequencies, and at such frequencies power constraints favor use of arrays.

An older field that seems to be going through an active-antenna renaissance is that of retroreflection. A retroreflector is a device that, when illuminated from any arbitrary direction, will return a signal directly back to the source. Clearly, retroreflectors are useful for return calibration as well as for various tracking purposes. An archetypical passive retroreflector would be a corner cube. Another idea for a passive reflector is a Van Atta array [60]. Such an array uses wires to interconnect the array elements such that the phase progression of the incident signal is conjugated and thereby returned in the direction of the source. As was pointed out by Friis in the 1930s, though, phase conjugation is carried out in any mixer in which the local oscillator frequency exceeds the signal frequency [61]. This principle was already being exploited in 1963 for implementing retroreflection [62]. This work didn't seem to catch on, perhaps due to technology. A review in 1994 [63] and designs for such arrays were demonstrated and presented at the 1995 International Microwave Symposium [64,65]. For a more recent demonstration, a group of UCLA researchers borrows from the term *phase conjugation* from the optics literature in order to describe their work [66]. Work in this area of retrodirective arrays continues [67].

Although much has been done in the area of active antennas in general and active integrated antennas in particular, much remains to be done, and the area remains an active one at this point in time. Although the field of active antennas began with the field of radiofrequency, it still seems to be a field in its infancy and one that should continue to grow and change with advances in technology.

BIBLIOGRAPHY

1. J. A. Navarro and K. Chang, *Integrated Active Antenna and Spatial Power Combining*, Wiley, New York; 1995.
2. K. Chang, R. A. York, P. S. Hall, and T. Itoh, Active integrated antennas, *IEEE Trans. Microwave Theory Tech*. **50**:937–944 (March 2002).
3. Y. Qian and T. Itoh, Progress in active integrated antennas and their applications. *IEEE Trans. Microwave Theory Tech*. **46**:1891–1900 (Nov. 1998).
4. H. Hertz, *Electric Waves*, Macmillan, 1983.
5. J. Bardeen and W. Brittain, The transistor: A semiconductor triode, *Phys. Rev.* **74**:435 (1948).
6. W. Schockley, The theory of p-n junctions in semiconductors and p-n junction transistors, *Bell Syst. Tech. J.* **28**:435 (1949).
7. W. Schockley, A unipolar field-effect transistor, *Proc. IEEE* **40**:1365–1376 (1952).
8. C. A. Mead, Schottky-barrier gate field-effect transistor, *Proc. IEEE* **54**:307–308 (1966).
9. R. A. York, R. D. Martinez, and R. C. Compton, Active patch antenna element for array applications, *Electron. Lett*. **26**:494–495 (March 1990).
10. M. P. DeLisio and R. A. York, Quasi-optical and spatial power combining, *IEEE Trans. Microwave Theory Tech*. **50**:929–936 (March 2002).
11. K. Chang, *Microwave Solid-State Circuits and Applications*, Wiley, New York, 1994.
12. See, for example, Chap. 3 of B. J. Hunt, *The Maxwellians*, Cornell Univ. Press, Cornell, NY, 1991.
13. H. C. Pocklington, Electrical oscillations in wires, *Proc. Cambridge Phil. Soc*. 324–333 (1897).
14. D. M. Pozar, *Microwave Engineering*, Addison-Wesley, Reading, MA, 1990.
15. P. E. Gray and C. L. Searle, *Electronic Principles, Physics, Models and Circuits*, Wiley, New York, 1967.
16. R. E. Collin, *Foundations for Microwave Engineering*, 2nd ed., MacGraw-Hill, New York, 1992.
17. K. Y. Chen, P. D. Biernacki, A. Lahrichi, and A. R. Mickelson, Analysis of an experimental technique for determining Van der Pol parameters of a transistor oscillator. *IEEE Trans. Microwave Theory Tech*. **MTT-46**:914–922 (1998).

18. B. Van der Pol, Forced oscillations in a circuit with a nonlinear resistance, *Phil. Mag.* **3**:65–80 (Jan. 1927).
19. K. R. Carver and J. W. Mink, Microstrip antenna technology, *IEEE Trans. Anten. Propag.* **AP-29**:2–24 (Jan. 1981).
20. D. M. Pozar and D. H. Schauber, eds., *Microstrip Antennas*, IEEE Press, Piscataway, NJ, 1995.
21. R. E. Munson, Conformal microstrip antennas and microstrip phased arrays. *IEEE Trans. Anten. Propag.* **AP-22**:74–78 (1974).
22. R. F. Harrington, *Time Harmonic Electromagnetic fields*, McGraw-Hill, New York, 1961 (the equation in question is on p. 276).
23. K. Chang, K. A. Hammer, and G. K. Gopalakrishnan, Active radiating element using FETsource integrated with microstrip patch antenna, *Electro. Lett.* **24**:1347–1348 (Oct. 1988).
24. R. Adler, A study of locking phenomena in oscillators, *Proc. IRE* **34**:351–357 (June 1946).
25. R. Adler, A study of locking phenomena in oscillators, *Proc. IEEE* **61**:1380–1385 (Oct. 1973).
26. K. Kurokawa, Injection locking of microwave solid-state oscillators, *Proc. IEEE* **61**:1386–1410 (Oct. 1973).
27. R. A. York and T. Itoh, Injection and phase-locking techniques for beam control, *IEEE Trans. Microwave Theory Tech.* **46**:1920–1929 (Nov. 1998).
28. K. D. Stephan, Inter injection locked oscillators for power combining and phased arrays, *IEEE Trans. Microwave Theory Tech.* **34**:1017–1025. (Oct. 1986).
29. K. D. Stephan and W. A. Morgan, Analysis of inter-injection-locked oscillators for integrated phased arrays, *IEEE Trans. Anten. Propag.* **35**:771–781 (July 1987).
30. K. D. Stephan and S. L. Young, Mode stability of radiation-coupled inter-injection-locked oscillators for integrated phased arrays. *IEEE Trans. Microwave Theory Tech.* **36**:921–924 (May 1988).
31. W. A. Morgan and K. D. Stephan, An X-band experimental model of a millimeter-wave inter-injection-locked phased array system, *IEEE Trans. Anten. Propag.* **36**:1641–1645 (Nov. 1988).
32. R. A. York, Nonlinear analysis of phase relationships in quasi-optical oscillator arrays, *IEEE Trans. Microwave Theory Tech.* **41**:1799–1809 (Oct. 1993).
33. P. Liao and R. A. York, A new phase-shifterless beam scanning technique using arrays of coupled oscillators, *IEEE Trans. Microwave Theory Tech.* **41**:1810–1815 (Oct. 1993).
34. R. A. York and R. C. Compton, Quasi-optical power combining using mutual synchronized oscillator arrays, *IEEE Trans. Microwave Theory Tech.* **39**:1000–1009 (June 1991).
35. R. A. York and R. C. Compton, Coupled-oscillator arrays for millimeter-wave power-combining and mode-locking, *IEEE MTT-S Int. Microwave Symp. Digest*, June 1992, pp. 429–432.
36. P. S. Hall and P. M. Haskins, Microstrip active patch array with beam scanning, *Electron. Lett.* **28**:2056–2057 (Oct. 1992).
37. P. S. Hall, I. L. Morrow, P. M. Haskins, and J. S. Cahele, Phase control in injection-locked microstrip active antennas, *IEEE MTT-S Int. Microwave Symp. Digest*, 1994, pp. 1227–1230.
38. A. Zarrang, P. S. Hall, and M. Cryan, Active antenna phase control using subharmonic locking, *Electron. Lett.* **31**:842–843 (1995).
39. T. S. M. Maclean and P. A. Ransdale, Short active aerials for transmission, *Int. J. Electron.*, **36**:261–269 (Feb. 1974).
40. P. K. Rangole and S. S. Midha, Short antenna with active inductance, *Electron. Lett.*, **10**:462–463 (Oct. 1974).
41. C. Duvanaud, S. Dietsche, G. Paraut, and J. Obregon, High-efficiency class F GaAsFETamplifiers operating with very low bias voltages for use in mobile telephones at 1.75 GHz, *IEEE Microwave Guided Wave Lett.*, **3**:268–270 (Aug. 1993).
42. T. B. Mader and Z. B. Popović, The transmission-line-high-efficiency class-E amplifier, *IEEE Microwave Guided Wave Lett.*, **5**:290–292 (Sept. 1995).
43. V. Radišić, Y. Qian, and T. Itoh, Novel architectures for high-efficiency amplifiers for wireless application, *IEEE Trans. Microwave Theory Tech.* **46**:1901–1909 (Nov. 1998).
44. W. R. Deal, V. Radišić, Y. Qian, and T. Itoh, Integrated-antenna push-pull power amplifier, *IEEE Trans. Microwave Theory Tech.*, **47**:1418–1425 (Aug. 1999).
45. C. Kalialakis, M. J. Cryan, P. S. Hal, and P. Gardner, Analysis and design of integrated active circulator antennas, *IEEE Trans. Microwave Theory Tech.* **48**:1017–1023 (June 2000).
46. G. M. Rebeiz, Millimeter-wave and terahertz integrated circuit antennas, *Proc. IEEE* **80**:1748–1770 (Nov. 1996).
47. A. D. Frost, Parametric amplifier antennas, *Proc. IRE* **48**:1163–1164 (June 1960).
48. J. R. Copeland and W. J. Robertson, Antenna-verters and antennafiers, Electronics 68–71 (Oct. 1961).
49. M. E. Pedinoff, The negative conductance slot amplifier, *IRE Trans. Microwave Theory Tech.* **9**:557–566 (Nov. 1961).
50. W. J. Robertson, J. R. Copeland, and R. G. Verstraete, Antennafier arrays, *IEEE Trans. Anten. Propag.* **2**:227–233 (March 1964).
51. K. Fujimoto, Active antennas: Tunnel-diode-loaded dipole, *Proc. IEEE* **53**:174 (Feb. 1964).
52. H. H. Meinke, Tunnel diodes integrated with microwave antenna systems, *Radio Electron. Eng.* **31**:76–80 (Feb. 1966).
53. K. J. Russell, Microwave power combining techniques, *IEEE Trans. Microwave Theory Tech.* **27**:472–478 (May 1979).
54. K. Chang and C. Sun, Millimeter-wave-power-combining techniques, *IEEE Trans. Microwave Theory Tech.* **31**:91–107 (1983).
55. M. Born and E. Wolf, *The Principles of Optics*, 5th ed., Pergamon Press, New York, 1975.
56. Z. B. Popovic, M. Kim, and D. B. Rutledge, Grid oscillators, *Int. J. Infrared Millimeter Waves* **9**:647–654 (July 1988).
57. Z. B. Popovic, R. M. Weikle, M. Kim, and D. B. Rutledge, A 100-MES FETplanar grid oscillator, *IEEE Trans. Microwave Theory Tech.* **39**:193–200 (Feb. 1991).
58. K. Y. Chen, P. D. Biernacki, S. Bucheit, and A. R. Mickelson, Noninvasive experimental determination of charge and current distributions on an active surface, *IEEE Trans. Microwave Theory Tech.* **44**:1000–1009 (1996).
59. B. M. Armstrong, R. Brown, F. Rix, and J. A. C. Stewart, Use of microstrip impedance-measurement technique in the design of BARITT piplex Doppler sensor, *IEEE Trans. Microwave Theory Tech.* **28**:1437–1442 (Dec. 1980).
60. E. D. Sharp and M. A. Diab, Van Atta reflector array, *IRE Trans. Anten. Propag.* **8**:436–438 (July 1960).
61. H. T. Friis and C. Feldman, A multiple-unit steerable antenna for short-wave reception, *Bell Sys. Tech. J.* **16**:337–419 (1937).
62. C. Y. Pon, Retrodirective array using the heterodyne technique, *IEEE Trans. Anten. Propag.* **12**:176–180 (1964).
63. B. S. Hewitt, The evolution of radar technology into commercial systems, *IEEE MTT-S Int. Microwave Symp. Digest*, 1994, pp. 1271–1274.
64. C. W. Poblanz and T. Itoh, A conformal retrodirective array for radar applications using a heterodyne phase scattering

element, *IEEE MTT-S Int. Microwave Symp. Digest*, 1995, pp. 905–908.

65. Y. Chang, D. C. Scott, and H. R. FETterman, Microwave phase conjugation using antenna coupled nonlinear optically pumped surface, *IEEE MTT-S Int. Microwave Symp. Digest*, 1995, pp. 1303–1306.
66. Y. Chang, H. R. Fetterman, I. L. Newberg, and S. K. Panaretos, Microwave phase conjugation using antenna arrays, *IEEE Trans. Microwave Theory Tech.*, **46**:1910–1919 (Nov. 1998).
67. S. L. Karode and V. F. Fusco, Self-tracking duplex communication link using planar retrodirective antennas, *IEEE Trans. Anten. Propag.* **47**:993–1000 (June 1999).

ACTIVE FILTERS: OVERVIEW OF ACTIVE-FILTER STRUCTURES

LAURENT BILLONNET
BERNARD JARRY
IRCOM University of Limoges
Limoges, Cedex, France

1. INTRODUCTION

Telecommunication services and products fueled by Internet, mobile, and space markets, have grown spectacularly since the early 1990s with no signs of slowing down. The use of microwave, millimeter-wave, and more generally high-frequency circuits, for today's applications, concerns at the same level detection systems (radars, intrusion sensors, etc.), the medical domain, and also various communication systems (e.g., telephone, PCS, data transfer, Internet by satellite, military applications, WLAN, Bluetooth). Such systems employ different RF functions or subsystems. Basic blocks can be divided into two categories. The first category concerns passive blocks or functions such as multiplexers, delays, couplers, isolators and connection sections (e.g., transmission lines). The second category focuses instead on active blocks, that is, blocks that use basic active components (transistors) or more complex subsystems. Basic subsystems to consider in this case are amplifiers, mixers, oscillators, and filters. Amplifiers are generally used to extract the information signal from noise in a front-end receiver or to increase the signal level in a transmitter chain. Mixers are used to upconvert or downconvert (modulate or demodulate) the working frequency of a signal to enable its transmission through a particular media (e.g., for hertzian transmission) or in a particular dedicated frequency band (e.g., in a given channel between a base station and a satellite or as a relay between two satellites). Oscillators are frequency sources most often used in association with mixers. The frequencies generated drive the up- or downconversion during a modulation/demodulation process. Finally, another essential block in a communication system is a filter. What is a filter [1]? A filter performs an electrical function used for a frequency selection process. This process can consist in preserving a frequency band. We then speak either of lowpass, bandpass, or highpass filters. These filters are used to process a signal that must be transmitted to another part of a chain. The process can also consist in rejecting frequency bands. We speak in this case of bandstop filters. These filters are used to eliminate the effect or influence of a parasitic signal next to the frequency of a working signal. Note that lowpass or highpass filters may be considered, depending on their use (selection or rejection) as rejecting filters.

With the need of compact size and light weight for new satellite and PCS applications, the translation from classical waveguide-type technologies to planar integrated processes has become unavoidable. If passive filters solutions are first considered, reducing insertion losses and, as a result, increasing battery life and noise performance, the use of high-Q volumic resonators is needed. The latter cannot be reached by use of conventional planar MIC or MMIC technologies where unloaded Q factor does not exceed 200–300 and rapidly decreases with increasing frequency. The solution cannot then be found on the basis of conventional frequency selective passive circuits. One well-known limitation is the ratio between insertion loss and bandwidth. Their product is a constant for a given realization of passive filtering structure.

One promising way that naturally comes to mind to overcome these drawbacks, and specifically losses compensation, is the integration of passive filters with active components or devices. As we show it in this article, on the basis of this idea, different configurations of microwave active filters (MAFs) have been developed, and new types are under intensive search and study nowadays.

The key features of MAFs are:

- Gain control without distortion of the frequency response
- Frequency tuning capability (in Hz)
- Frequency agility for fast-tuned filters (in Hz/s)
- Capability of modifying specified poles to improve response selectivity
- Possibility of implementing automatic frequency control techniques
- Easy use of MIC/MMIC and integrated technologies
- Small filter dimensions and weight

However, in comparison to purely passive structures, implementation of active devices is accompanied with undesirable factors to take into account, such as:

- Noise figure increase
- Critical power-handling behavior
- Dynamic range reduction
- Electrical stability
- Stability of active parts under variations of external mechanical, climatic, optical, or electromagnetic conditions

In the design of microwave active filters, first task of researchers has then been to deal with imperfect active devices and lossy passive components [2]. The situation was

similar to that encountered before the advent of high-performance op- amps (operational amplifiers) in the 1950s and 1960s, when audiofrequency active *RC* filter designs were attempted. By adapting some of the active solutions used at lower frequency, investigators have then devised a number of interesting circuits. In this section, we first talk about the different families of filters. We evaluate different ways of classifying MAFs and show that two main categories can be finally considered. For the first category, we describe, from a general point of view, various compensation techniques and detail more specifically filters based on the use of gyrators and negative-impedance converters (NICs). At this step, we emphasize different problems that must be faced by RF and microwave designers in comparison to low-frequency classical designs. The second category is based on filters resulting from the application of methods and concepts used primarily at low frequency. As an example, this section sums up the different ways of considering and implementing recursive and transversal (R&T) filters for the microwave purpose.

2. MAF CLASSIFICATION

Most MAFs can be classified into several levels of a consideration depending on their basic topology structure, type of passive and active elements used, resonator configurations, guiding structures, application domain, working frequency band, and other factors. Major problem for MAF classification resides in the fact that there is still no systematic method to predict which active solution is the best to fit given specific functional requirements.

From our point of view, active filter structures at microwaves can be divided into two main categories:

- Active filters resulting from the improvement of classical microwave passive structures (category 1)
- Active filters resulting from the application, in the microwave domain, of methods and concepts primarily used at low frequency (category 2)

In fact, active-filter categories can, using the same approach, be defined by considering how the active components or functions improve the basic passive structures:

- If the active parts are used as correction blocks (e.g., for loss compensation), then the corresponding active filter belongs more to the first category;
- If the improvement is done through the benefit of a typical active property (except compensation, e.g., through nonreciprocity, unilaterality, or gain), then the second category is indicated.

Depending on the way the active parts contribute to the response improvement, the resulting filter can belong to one or the other category. As an example, consider the simple case of a classical *LC* filter for which the response improvement is realized through the use of an "active inductance":

- If the active inductance consists in a classical passive inductance in which losses are compensated with a NIC (a negative resistance), the global filter rather belongs to the first category.
- On the other hand, if the active inductance results from the capacitive load of a gyrator (which specific role, as we will see later, is to invert an impedance), then the global filter is of the second category.

Most realizations to date use the compensation principle and then belong to category 1 [3–6]. However, as it will be shown further, original approaches now tends to design circuits of category 2.

3. COMPENSATION TECHNIQUES

Referring to filter category 1, we show here various approaches to compensate (from a general point of view) the response of filter structures. Considering circuits using either distributed elements (in microstrip or coplanar technology) or lumped elements (using, e.g., monolithic integrated processes), compensation can be done in three basic ways.

3.1. Amplifiers for Loss Compensation

A first solution is used for resonator-based planar or volumic structures. It consists in compensating for the passive losses of one or more resonator thanks to the feedback of an amplifier. In terms of the compensation, the two-port amplifier is equivalent to a one-port negative resistance, as will be shown below. Following this principle, an example of a three-pole filter realized on a duroïd substrate is given in Fig. 1 [7]. In this case, only the central resonator losses are directly compensated by the amplifier of adequate phase and gain values. These values are calculated to maintain the electrical stability (see Active filters: tools and techniques for active-filter design, Section 2). Input and output coupling values have been chosen to perform a 400 MHz bandwidth at 12 GHz. Figure 2 shows the improvement provided by the amplifier. Measurements of the filter in Fig. 3 show a perfect loss compensation within the passband. Poor input matching is due to a nonperfect matching of the amplifier. The same approach has been applied to volumic structures [8] for a third-order dielectric resonator (DR) filter for which the central resonator is compensated by an active loop [9].

3.2. Active Matching Approach

This active matching technique has already been successfully used and described at lower frequencies for broad-

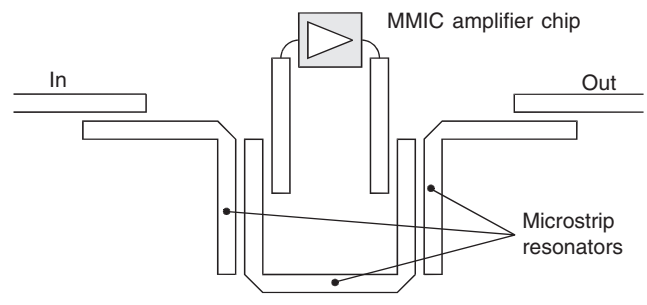

Figure 1. Topology of a third-order planar active filter.

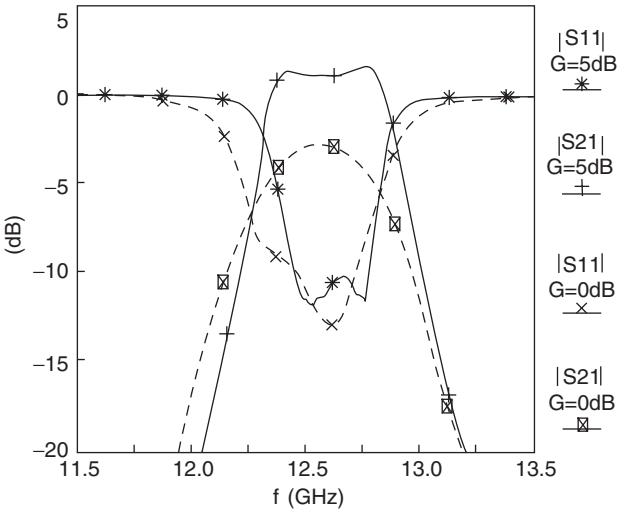

Figure 2. Simulated passive and compensated third-order planar filter responses.

band matching [10,11]. As an example, the filter consists here of a cascade association of three sections (Fig. 4) [12]. First and last sections act respectively as input and output matching networks. PHEMT active devices in common-gate and common-drain configurations have been used instead of passive elements to achieve wideband matching simultaneously as gain performances. The bandpass filter response is obtained by the intermediate section composed of a passive lumped-element network that sets the filter center frequency. The main goals of the common-gate and common-drain stages are to improve selectivity, compensate for the passive network losses, and match the filter to 50 Ω external impedances.

At high frequencies, the common-gate configuration is unilateral, whereas the common-drain configuration becomes nonunilateral, thus being capable of achieving both input and output matchings to 50 Ω impedances. It can be shown [13] that the voltage transfer function of the passive section realizes a bandpass filter response. Replacing the common-gate and common-drain transistors in Fig. 4 by their equivalent models, it can be demonstrated that S_{21} is proportional to the voltage transfer function, thus realizing a bandpass filter response. Figure 5 shows the layout of the monolithic microwave integrated circuit (MMIC) using ED02Ah GaAs process from OMMIC [14]. Dimensions of the chip are $1.5 \times 1\,\text{mm}^2$. Total DC power consumption is 80 mW. Figure 6 shows a comparison between computer-simulated and measured results. The active filter operates at 31.825 GHz with 0.5 dB gain and 1.5 GHz with –3 dB bandwidth. Active matching approach appears to be suitable to achieve broadband performance with $|S_{ii}| < -12$ dB. At the central frequency, the noise factor of the filter is equal to the minimum noise factor of 4 dB. The –1 dB compression point occurs for an input power of + 3 dBm. Noise performance and power-handling capabilities are discussed in the article on active-filter design tools and techniques, cited above (in Section 3.1).

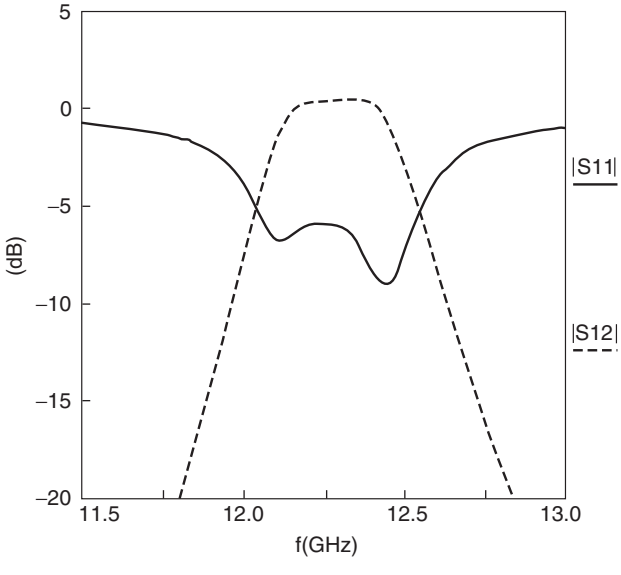

Figure 3. Measured third-order planar filter response.

3.3. Filtering/Matching Approach with Gain

The method is derived from classical lumped matching technique but it differs in the fact that a preliminary matching step is performed on the active part. This alternative method combines amplification and filtering functions based on the use of an active element with cascaded passive lumped filtering sections also contributing to the matching of the active part. A circuit example using this approach is presented in Fig. 7 [12]. The basic methodology first consists in simply doing a preliminary matching of a single transistor at the central frequency thanks to two inductances at the input and output. Wideband matching and filtering principles are then simultaneously realized by lumped passive filtering sections placed either before or after the preliminary matched active device while maintaining gain in the passband.

In comparison to a classical method, the preliminary matching using only two components achieves a significant reduction in the number of elements of the matching sections that can then be achieved much more simply. The chip size is only 1.5×1 mm. Total DC power consumption is 20 mW. Figure 8 shows a comparison between computer-simulated and measured results. This filter operates at 14.12 GHz. The gain is near 0 dB, and the –3 dB bandwidth is 1.77 GHz. Good performances are obtained, especially for the input matching ($|S_{11}| = -17.26$ dB). Simulated noise factor is equal to 2.7 dB at the center frequency.

3.4. Gyrators and NICs

The last compensation approach consists in using gyrators or NICs. Gyrators (impedance inverters) and NICs are functions initially used at low frequency. Their role is to build a given impedance through an intermediate load impedance. Thus, the impedance at a gyrator input is inversely proportional to the load impedance of the gyrator. In the NIC case, the input impedance is proportional to the negative of the load impedance of the NIC.

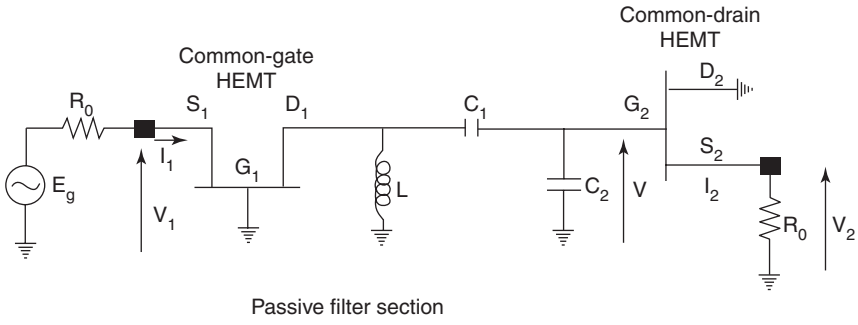

Figure 4. Actively matched passive lumped filter.

In most cases, NICs are dedicated to the compensation of losses and of resistive parts. However, overcompensation has already been used for oscillator design [15,16]. Gyrators are more classically used for high-value reactance design (in particular, for inductances) and for ideal inductances [17,18].

3.4.1. Design Problems at Microwaves. A large number of gyrators and NICs topologies have been investigated. Most of them come from the low frequency domain, where transistors and op amps can be considered as ideal transconductances and amplifiers with infinite gain, respectively.

At microwaves, gyrators and NICs topologies can be divided into two categories. As an example, we consider the NIC case here:

- In Fig. 9, high-gain transistors are considered as high-value transconductances. Input impedance of the global circuit then depends only on the three load impedances Z_1, Z_2, Z_3, and is given by:

$$Z_{\text{in}} = -\frac{Z_1 Z_2}{Z_3}$$

- For the second category, transistors are modeled as finite-value transconductances. In Fig. 10, input impedance depends not only on a load impedance Z but also on the two transconductances g_1 and g_2, and is given by:

$$Z_{\text{in}} = -\frac{1}{g_1 g_2 Z}$$

However, whatever category is considered, investigator has to face some problems inherent to the microwave domain:

- Transconductances values cannot be infinite.
- Transistors cannot be modeled as simply as at low frequency, even in the linear regime.
- Passive components are not ideal and present losses or unwanted distributed effects.
- Interconnecting elements (in general transmission-line sections) lead to nonnegligible effects on the whole circuit response.

Considering the example of Fig. 10 at microwaves, when loaded with a pure resistance R, the circuit can provide a complex input impedance, even with a positive real part. Therefore, even if the idea of a simple transposition of low-frequency concepts to microwaves is promising, more complex compensation means must be considered.

3.4.2. Design Methodologies. In many cases, for negative-resistance circuits, designers just try to fit the negative real part of the desired impedance and accommodate as best as possible with the parasitic or unwanted imag-

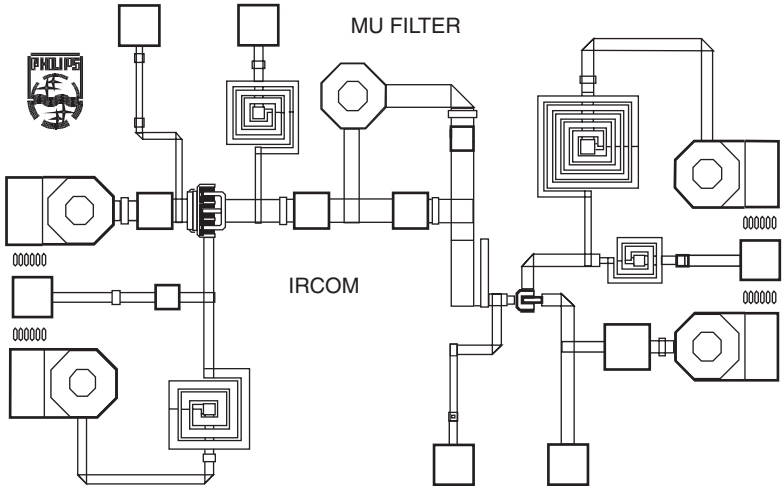

Figure 5. Layout of the actively matched passive lumped filter.

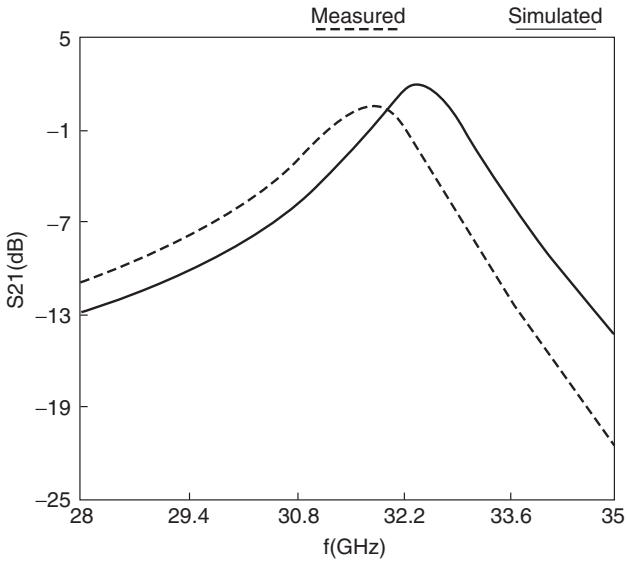

Figure 6. Comparison between simulated and measured S_{21} parameter of the actively matched passive lumped filter.

inary part when associating it to the rest of the filter [19,20]. This is the same for active inductances when designers try to fit only the imaginary part without sufficiently factoring in the parasitic real part, thus leading to poor-Q-factor inductances. Most part of the time, this tendency is only due to the lack of a systematic procedure. Some researchers have derived interesting methodologies to overcome these problems. Among all the attempts, one of the most interesting and simplest has been done by Sussman-Fort [21].

To explain the method, we come back to the topology of Fig. 10. Consider now the two-port NIC represented by its chain matrix (classically four parameters: A, B, C, and D) and loaded with an impedance Z. The input impedance is given by:

$$Z_{\text{in}} = \frac{AZ + B}{CZ + D} \tag{1}$$

Considering that a pure load resistance R at port 2 does not lead to $-R$ at the input at microwaves, the question we now consider is whether the corresponding Z_{in} can still be made to be a negative resistance by choosing a special load impedance Z. To answer this, we set $Z_{\text{in}} = -R$ in (1) and solve for the required Z as follows:

$$Z = -\frac{DR + B}{CR + A} = -Z' \tag{2}$$

Referring to (2), Z may be interpreted as the negative of the impedance Z' looking into port 2 when port 1 (the input) is terminated with the negative of the desired input impedance (here R is the negative of $-R$).

The design approach then simply consists in terminating the input of the circuit with the negative of the desired impedance, and to synthesize the negative of the impedance seen at port 2 under this condition. In our example, we then first load the input with R, look at the resulting impedance Z' at port 2, and try to synthesize $-Z'$, that is, Z.

A restriction must, however, be emphasized in the fact that the real part of Z must be positive to lead to a passive network to synthesize at port 2. If not, the procedure turns to a nonsense approach since a negative resistance will still have to be synthesized at port 2.

Note that this general procedure can also be applied for the design of ideal inductance. In that case, the procedure leads to synthesize the negative of the impedance seen at port 2 when the input is loaded by a negative inductance. The procedure applies for NICs as well as for gyrators. In any case, the impedance needed at port 2 can be synthesized using any adequate CAD software based, for example, on the real frequency technique.

To further facilitate the design, additional preliminaries can be applied before using this technique:

- In the case of infinite transconductance NICs or gyrators, each transistor can be replaced by a cascade association of two or more transistors to emulate as close as possible an infinite transconductance value [22].
- In the case of a finite-value transconductance NIC or gyrator, each transistor can be substituted with two transistors in a cascade configuration [21]. The desired effect here is to reduce the parasitics of the transistors.

However, in both cases, the synthesis steps cannot be skipped and are not sufficient to get close enough to the ideal case. Moreover, the cascade approach increases power consumption and degrades the power-handling capabilities (and in particular the compression point).

Another interesting design approach [23] can be associated with the Sussman-Fort basic approach for the complex load impedance synthesis. It relies on an original assisted visual representation of the design process.

Until now, there have been two main approaches to synthesize broadband matching and compensation networks for microwave active circuits. The first approach is based on the analytic theory by Fano [24] and Youla [25]; the second is the use of the already mentioned real frequency

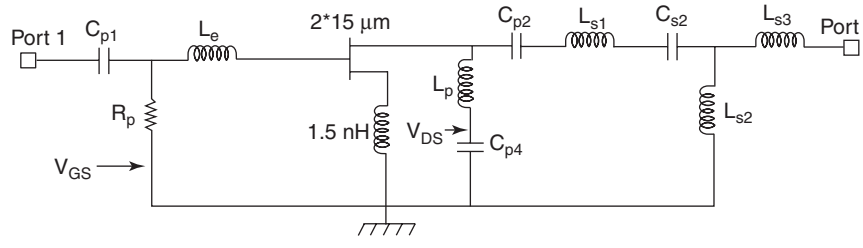

Figure 7. Schematic of the preliminary matched filter structure.

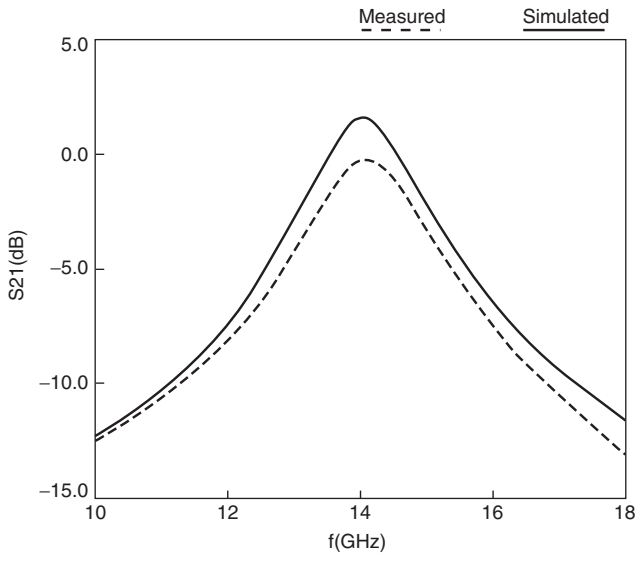

Figure 8. Simulated and measured S_{21} parameter of the preliminary matched filter.

technique (RFTs) by Carlin and Yarman [26]. Unfortunately, these approaches involve several limitations:

- It is difficult to apply them directly for the design of complex active circuits (i.e., circuits with several matching/compensation networks).
- With the synthesis techniques above, network configurations and elements result from fully formalized, complicated numerical procedures. Therefore, the designer has only very limited possibilities to control these configurations and elements.
- If distributed-element matching networks have to be designed, both the analytical procedures and RFTs lead to networks made from commensurate transmission lines. However, in practice, it may be preferable to employ networks consisting of noncommensurate lines, or mixed lumped/distributed-element networks.

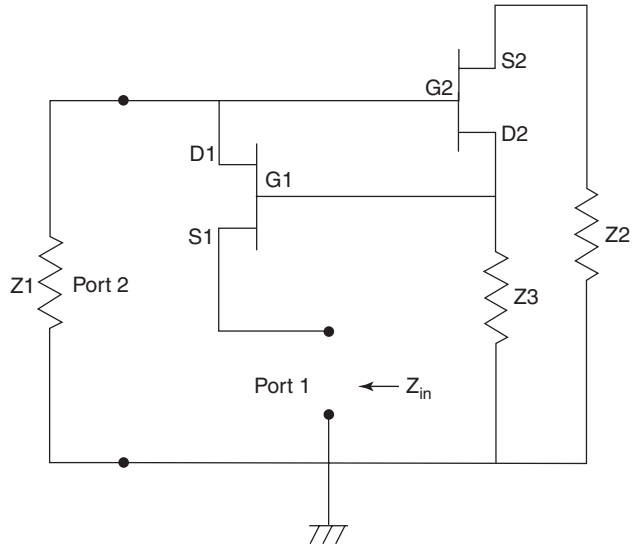

Figure 9. Example of a high-transconductance NIC topology.

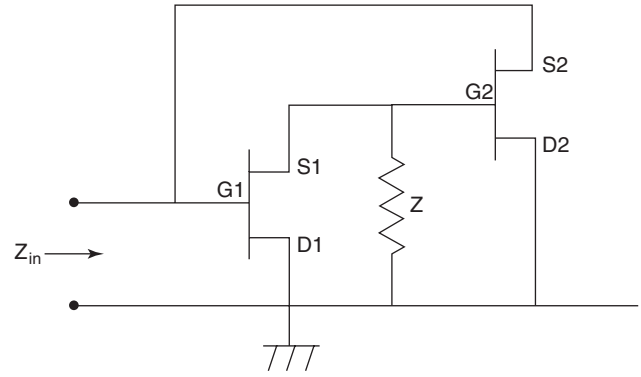

Figure 10. Example of a finite-value transconductance NIC topology.

To overcome these limitations, a new decomposition synthesis approach has been introduced for designing linear and nonlinear active circuits with passive matching/compensation networks. This method supposes that the design of active circuit is accomplished in two steps:

- Determination of acceptable regions of the matching/compensation networks immitances at sample frequencies over a frequency band of interest, according to a set of circuit specification ranges (noise, gain, matching levels)
- Synthesis of matching/compensation networks based on the acceptable immitance regions.

This technique allows the user to select a suitable network configuration and to directly control all the network elements for successful fabrication. Lumped, distributed noncommensurate line and mixed (lumped/distributed) networks of moderate complexity can then be designed. The approach is implemented in the software tool LOCUS, offering simple and fast means to produce solutions

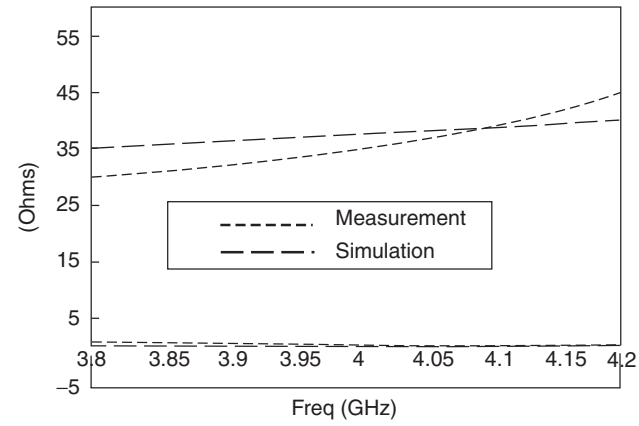

Figure 11. Simulated and measured imaginary part of the 1.5 nH active inductance.

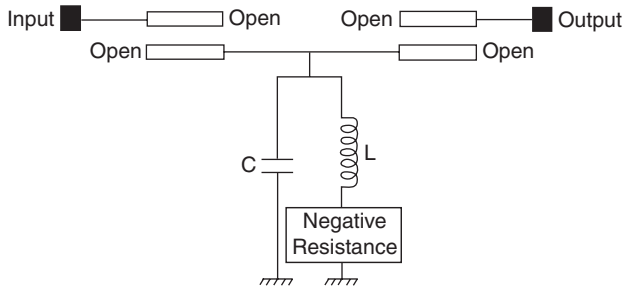

Figure 12. Basic *LC* shunt bandpass filter topology.

without the need for complicated circuit theory and mathematics. Other approaches have been developed by Yarman [27].

3.4.3. Circuit Examples. We give here three application examples of the compensation principle. The first example concerns the design of an ideal inductor in the 3.8–4.2 GHz band for a high-Q filter at 4 GHz [28]. Here, a spiral MMIC inductor is cascaded with a negative-impedance converter to obtain a high-Q inductor. Topology used is of infinite transconductance NIC type. The circuit has been drawn with the elements of the HB200 UMS (United Monolithic Semiconductors) process [29]. The size of the MMIC chip is 2.2×1.8 mm. Figure 11 shows simulated and measured results. The imaginary part is close to the expected value and losses are perfectly compensated.

The active inductance can then be used to design selective band-pass filters. Basic topology is presented in Fig. 12 [28]. Coupled lines are used at the input and output of the circuit to decouple the *LC* resonator and control the filter selectivity. Response of the filter achieves a Q factor of 1000 with a perfect loss compensation at the center frequency. A photograph of the filter is given in Fig. 13. Note the input and output coupling elements and the capacitance in parallel with the compensated spiral inductor.

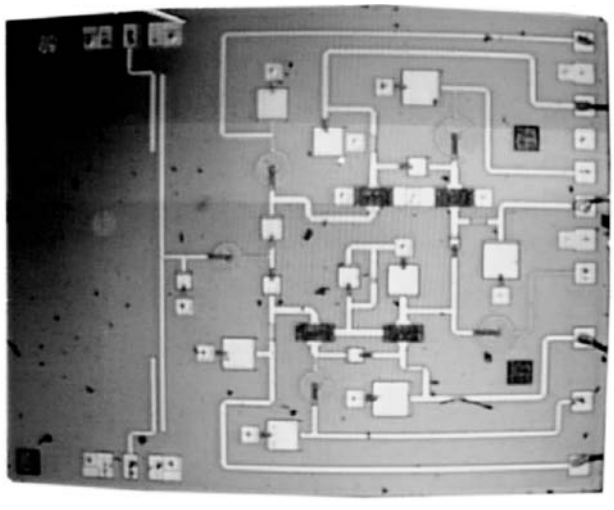

Figure 13. Photograph of the actively compensated *LC* shunt bandpass filter.

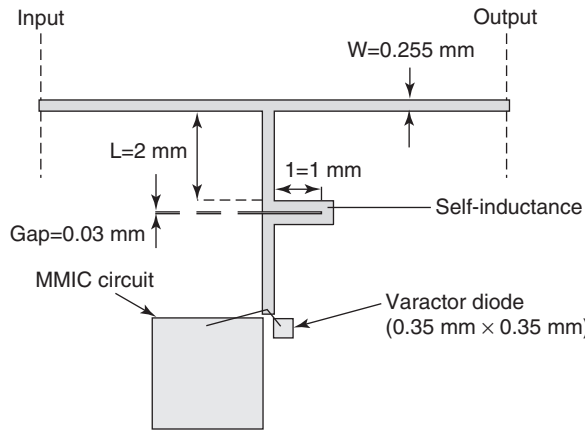

Figure 14. Layout of the tunable compensated bandstop filter.

The second example focuses on an active tunable bandstop filter using lumped elements [28]. We use here pseudolumped inductors built and synthesized in microstrip technology. Center frequency is optimized at 2 GHz. This filter can be tuned in frequency by using a varactor diode. Losses of the microstrip inductors and of the varactor diode are compensated by the negative-resistance circuit of Fig. 10. In a first step, characteristics of lumped inductors are studied according to the different geometric dimensions to determine an electrical equivalent schematic. This study is realized thanks to classical EM-CAD software packages. We use here an alumina substrate ($\varepsilon_r = 9.8$; $h_s = 635\,\mu$m). For this filter, the inductor chosen is realized with a single meander of length 1 mm, gap 30 μm, and strip width 255 μm. Layout of the filter including the MMIC chip is shown in Fig. 14. Measurements are shown in Fig. 15. Note that this bandstop filter is tunable in frequency over a wide band (nearly one octave). Tunability is also one interesting capability of active filters. It gives the property of being reconfigurable in frequency. Other examples of response tunability will be given and commented in the next sections. In this case, the tuning range varies from 1.3 to 2.6 GHz (66% of center frequency). The losses are well compensated as intended.

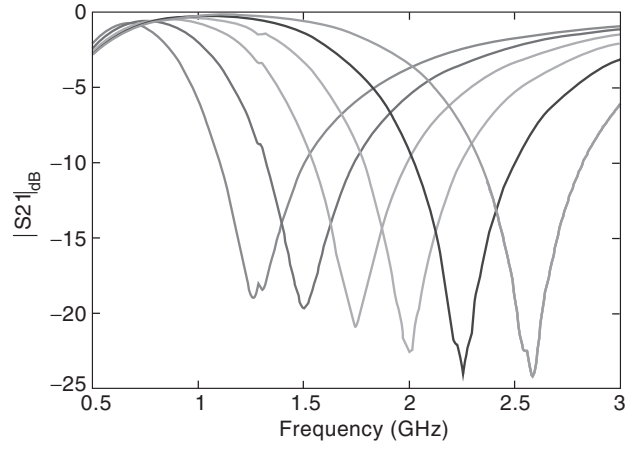

Figure 15. Measured tuned response of the compensated bandstop filter.

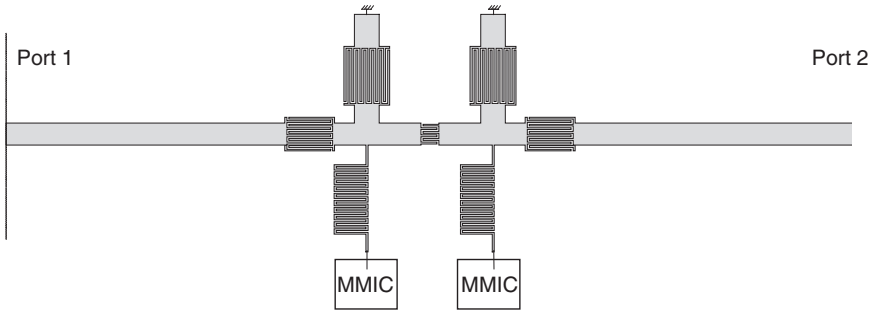

Figure 16. Layout of the two-pole active bandpass filter.

In the third example, we use the same type of NIC chip to compensate for the losses of a two-pole microstrip bandpass filter [30]. Interdigital capacitors and meander inductors are used to obtain a center frequency at 1.6 GHz. Compensation is made at one end of the inductors as shown in Fig. 16. Figure 17 shows the simulated response of the filter using the measured results of the MMIC chip. This figure also illustrates the response that would be obtained at the same frequency (due to the imaginary part of the MMIC impedance) without the negative real part of the MMICs. As can be seen, the difference of level obtained at the center frequency is more than 16 dB.

4. LOW-FREQUENCY CONCEPTS AT MICROWAVE APPLICATION TO RECURSIVE FILTER DESIGN

This section focuses on filters of category 2: active filters resulting from the application, in the microwave domain, of methods of filtering and concepts firstly used at low frequency.

4.1. Theoretical Background

Active filters have, for many years, focused at low frequency on operational amplifier approaches because of the abilities of such components to compensate for the intrinsic losses of passive components, and for the overall amplification also provided. Although the physical constraints are strongly different, these advantages carry over to microwave frequencies, thus showing an increasing interest in adapting low-frequency techniques for use in microwave systems. One of these techniques includes the design of recursive and transversal filters. Application of such concepts to filtering structures clearly must employ MMIC technology [31].

Recursive and transversal filters are governed by the following time-domain (3) and frequency-domain (4) equations, where $x(t)$ [$y(t)$] is the input [output] of the system:

$$y(t) = \sum_{k=0}^{N} a_k x(t - k\tau) - \sum_{p=1}^{P} b_p y(t - p\tau) \tag{3}$$

$$H(f) = \frac{Y(f)}{X(f)} = \frac{\sum_{k=0}^{N} a_k e^{-2j\pi f k\tau}}{1 + \sum_{p=1}^{P} b_p e^{-2j\pi f p\tau}} \tag{4}$$

Implementation of the corresponding (N : P)-order filter requires multiple constant delay increments τ, amplitude weighting elements $\{a_k\}$ and $\{b_p\}$, and a mean of combining the elementary delayed signal components.

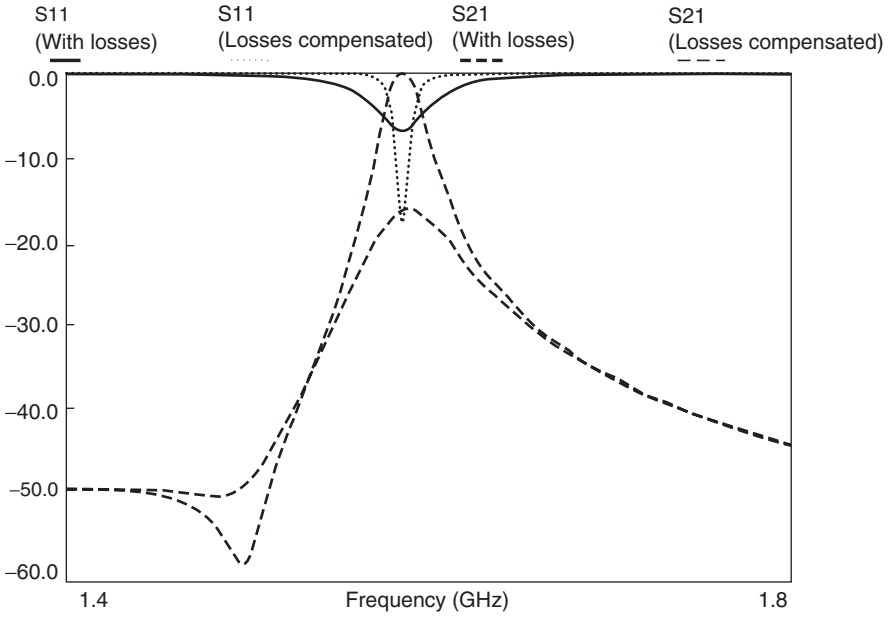

Figure 17. Influence of the negative real part of the MMIC on loss compensation of the two-pole bandpass filter.

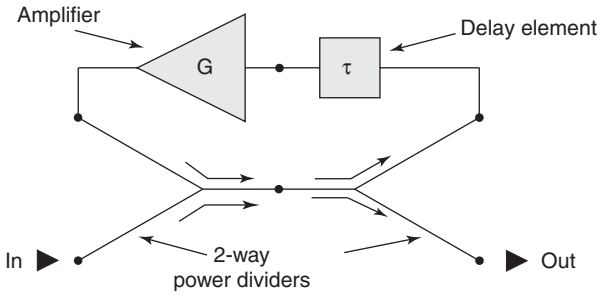

Figure 18. Topology of the first-order microwave recursive filter.

4.2. Power Matching Approach

Several approaches have been investigated to implement recursive responses. A first approach [31,32] consists in identifying a transversal filter with a distributed amplifier to get a ladder-type structure. However, this technique impose respectively a lowpass filter and a highpass filter before and after each transistor of the structure, to simultaneously realize the necessary delay time τ, and contribute to the response selectivity.

Another simple solution consists in considering combiners at microwaves, as power dividers/combiners [33]. This approach enables filter branches to be easily associated and then to be designed separately, each of them matched to the same impedance (in general, 50 Ω), naturally leading to the identification of the weighting parameters as microwave amplifiers [34–36].

Following these principles for MMIC design purpose, we consider here a first-order recursive filter, shown in Fig. 18 [37]. Power dividers/combiners are built in MMIC technology with lumped-element cells in order to minimize the size of the final device. Each power divider/combiner requires five lumped components. Delay time τ is built with a lowpass T cell. A one-stage pseudoresistive amplifier, including two *RL* series circuits for the matching of a single FET, is chosen here [38], thus again reducing the dimensions of the resulting circuit. For electrical stability reasons that we discuss in the article on active-filter design tools and techniques (cited above, in Section 3.1), the amplifier gain is adjusted to obtain the ratio $|S_{21}|_{\max}/|S_{21}|_{\min} = 10$ (20 dB) in the 7.5–12.5 GHz range. Figure 19 shows the layout of the filter, following OMMIC MMIC process design rules [14]. The circuit is implemented on an 100-μm-thick GaAs substrate. Dimensions of the chip are 2.0×1.5 mm. Perfect agreement between simulated and measured results is shown in Fig. 20.

4.3. Voltage Matching Approach

Considering that voltage matching and input/output signals combination can be more easily obtained over wider frequency bands than power matching, an alternative technique consists in synthesizing the filter responses owing to the use of voltage-matched devices [13]. At a last step, the whole circuit is matched to 50 Ω external impedances using FETs as described in Section 3.2. The classical recursive flow graph can be identified to the idealized series–shunt feedback model where an ideal adder is used to loop a unilateral forward active path $\mu(j\omega)$ with a passive path $\beta(j\omega)$. Under these assumptions, the overall transfer function can be identified as the transfer function of a first-order recursive filter if $\mu(j\omega) = 1$ and $\beta(j\omega) = -b_1 e^{-j\omega\tau}$.

The design procedure begins by first determining the circuit that realizes the voltage summation function at the input of the feedback. Then, the passive feedback device must provide the necessary delay time imposed by the

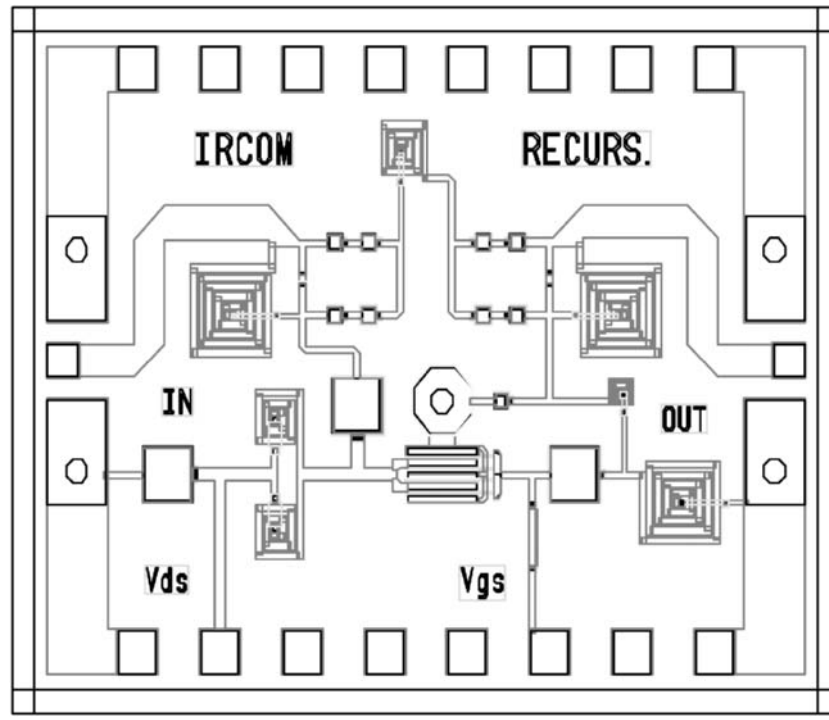

Figure 19. Layout of the first-order microwave recursive filter.

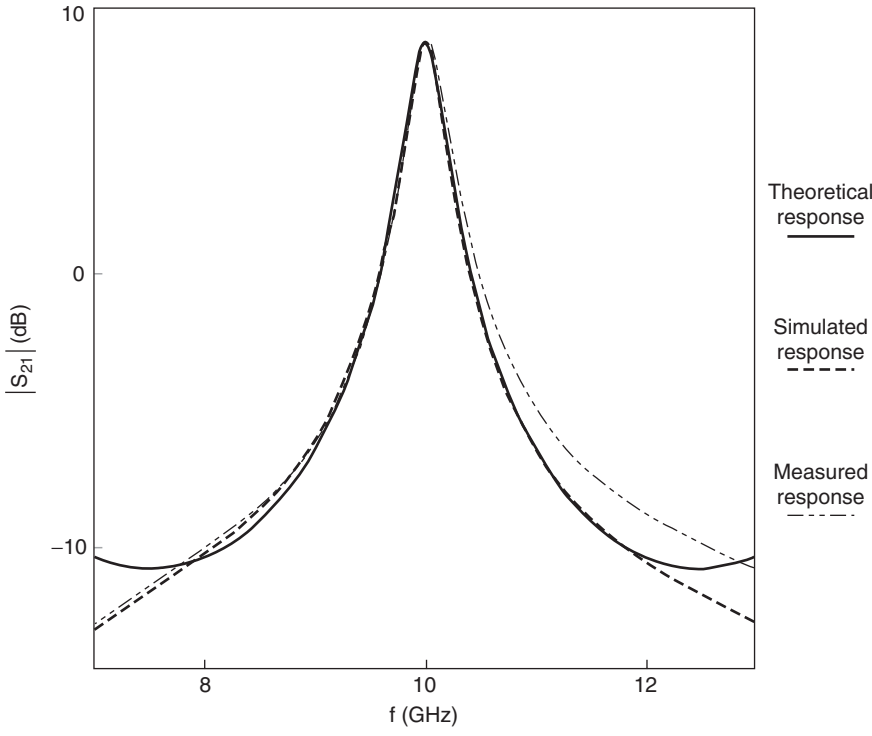

Figure 20. Theoretical, simulated, and measured response of the first-order recursive filter.

recursive process. Finally, a unilateral microwave active device must be employed in the forward branch in order to allow the feedback scheme to operate as intended. By verifying adequate relations between the impedances of the different blocks within the structure [13], the filter voltage gain appears to be of the recursive type:

$$G_V = K\left(\frac{\mu}{1-\mu e^{-j\omega\tau}}\right)$$

Finally, for integration in microwave systems, two impedance transformers are required to match the filter to 50 Ω external impedances: a common-gate MESFET at the input and a common-drain MESFET at the output (Fig. 21), which must simultaneously provide a voltage matching of the loop and a power matching of the complete structure. Moreover, an attracting outstanding feature is the capability of the common-gate stage T_1 to produce power gain, making it a significant factor in the composition of the overall noise figure of the filter. The loop gain can be controlled by the bias voltage of the common drain amplifier T_2 placed within the feedforward branch of the loop. A conventional lumped highpass cell and a lowpass cell are used to provide the necessary delay time τ for the desired filter center frequency. The filter has been fabricated using a 0.2-μm-gate-length PHEMT foundry process (ED02Ah from OMMIC [14]), and implemented on a 100-μm-thick GaAs substrate. Dimensions of the corresponding MMIC chip are $1 \times 1.5\ \text{mm}^2$. Total DC power consumption of the filter is 30 mW. Figure 22 shows a comparison between measured and simulated responses of the filter.

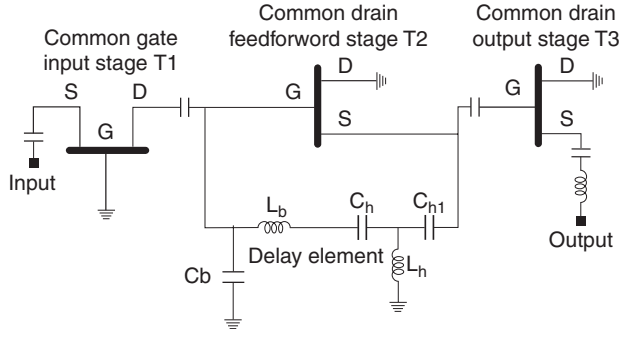

Figure 21. Electrical schematic of the voltage-matched first-order recursive filter.

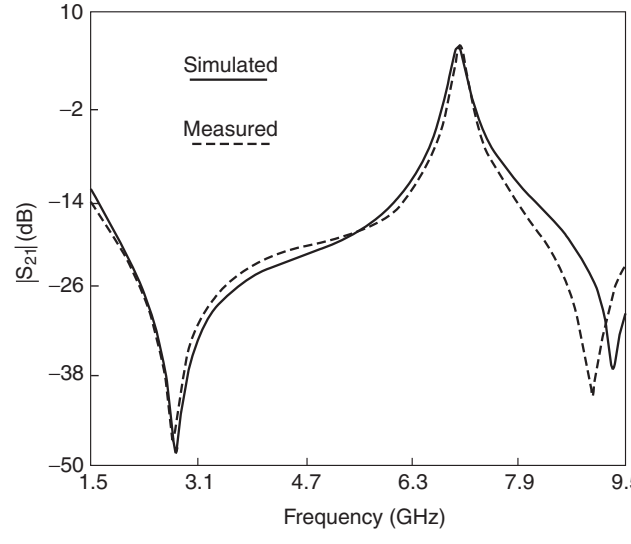

Figure 22. Simulated and measured voltage-matched first-order recursive filter response.

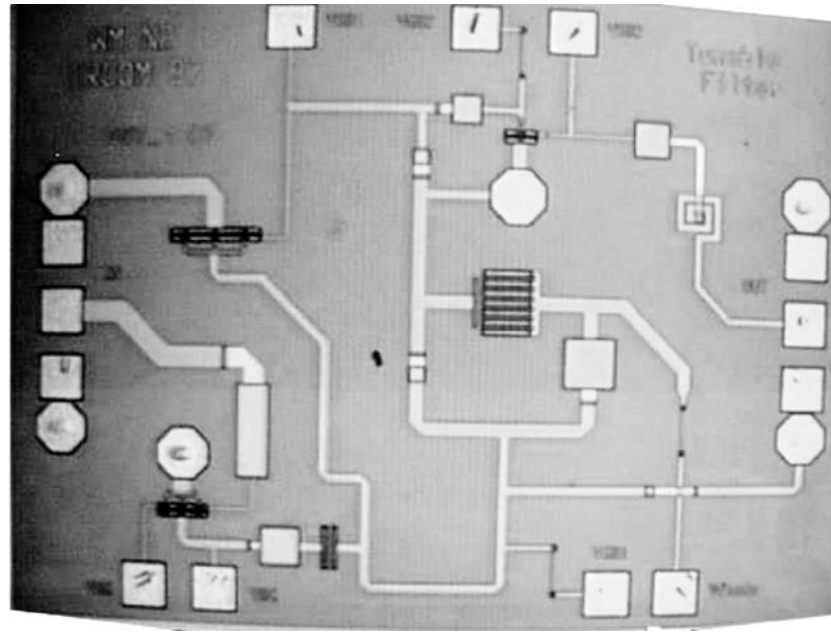

Figure 23. Photograph of the MMIC varactor-tuned first-order recursive filter.

The circuit is operating at 7 GHz with 5.1 dB gain at the center frequency and 140 MHz at 3 dB bandwidth. The out-of-band rejection is better than 20 dB, with 2 GHz from passband edges. The measured –1 dB compression point occurs for an input power of -15 dBm, and the simulated noise figure is 5.5 dB at the center frequency.

4.4. Frequency Tunable Recursive Filters

Recursive and transversal filters can simply provide tunable responses because of arbitrary analog phase shifter structures. As an example, we present the expression of a recursive transfer function shifted over a frequency band noted Δf:

$$H(f-\Delta f)=\frac{\sum_{k=0}^{N} a_k e^{-2j\pi(f-\Delta f)k\tau}}{1+\sum_{p=1}^{P} b_p e^{-2j\pi(f-\Delta f)p\tau}} = \frac{\sum_{k=0}^{N} a_k e^{-2j\pi fk\tau} e^{jk\phi}}{1+\sum_{p=1}^{P} b_p e^{-2j\pi fp\tau} e^{jp\phi}} \tag{5}$$

with $\phi = 2\pi\Delta f\tau = 2\pi\Delta f/f_0$. This expression clearly shows that recursive responses can be tuned by the introduction of a variable phase shift in each branch of the filter. Consequently, many "recursivelike" filter structures can take advantage of this concept to be turned into tunable versions.

For most applications, 10% of tuning range is not sufficient and emphasizes the need for a real phase shifter function. A phase shifter structure for "recursivelike" filter purpose is proposed in Ref. 39. Maximum phase shift measured is 55°. Gain is near 7.5 dB in the 3–5 GHz frequency band. Noise factor of the phase shifter is 4.5 dB at 4 GHz.

Another tunable filter example is based on the design concepts outlined in Section 4.3. A tunable filter is realized by introducing a phase shift into the feedback loop of a voltage-matched recursive structure [13]. Filter tuning at the desired center frequency is accomplished through variation of the equivalent capacitor of a varactor diode that replaces a capacitance of the initial delay-time section. Correct adjustment of the bias point of the transistor T_2 (see Fig. 21) ensures a constant gain level over the frequency tuning range when the series diode resistance varies with the bias voltage.

A photograph of the filter is shown in Fig. 23. Dimensions of the MMIC chip are $2 \times 1.5\,\text{mm}^2$. The measured transmission parameter of the filter is shown in Fig. 24. A frequency shift from 7.03 to 9.5 GHz (30% of relative

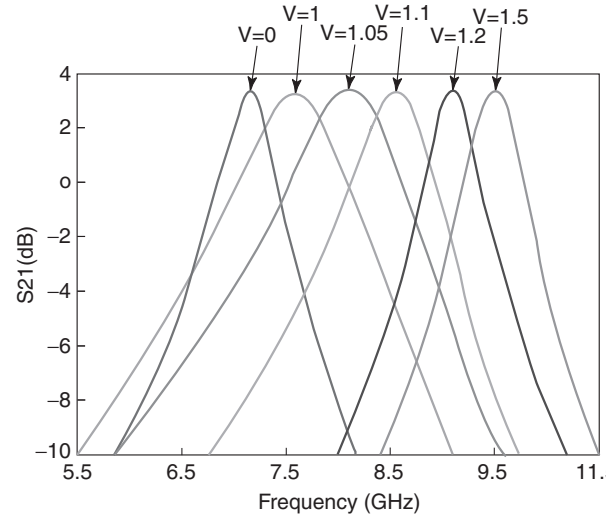

Figure 24. Measured S_{21} parameter of the tunable first-order recursive filter.

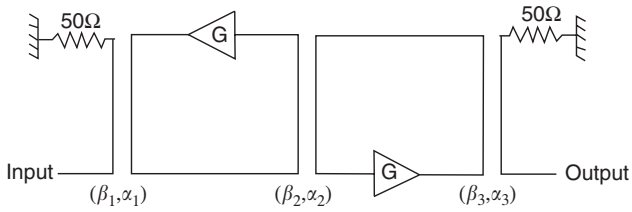

Figure 25. Second-order ring resonator active recursive filter.

tuning band) is achieved with a constant gain level of 3.5 dB across the tuning band. Moreover, the filter exhibits a good 50 Ω matching over the 2.5-GHz tuning band ($S_{ii} < -10\,\text{dB}$; $i = 1,2$). The expected noise figure is 5 dB at center frequencies. The measured -1 dB compression point occurs for an input power of -10 dBm. Maximum total DC power consumption is 46 mW.

4.5. High-Order Recursive Filters

For high-order filter design, a first alternative approach consists in coupling microstrip planar ring resonators, each resonator realizing a pole of the recursive transfer function.

The general transfer function of these ring resonator filters, where K and $\{K_n\}$ are functions of the coupling values and the amplifier gains can be expressed as:

$$S_{21}(f) = \frac{Ke^{-j\pi(f/f_0)}}{1 + \sum_{n=1}^{N} K_n e^{-2n\pi(f/f_0)}}$$

We give here an example of a second-order filter implemented in coplanar technology [40]. Many studies have shown that, in most cases, coplanar waveguides can be a good alternative to microstrip lines because of greater ease and flexibility in the design [41,42]. Because all conductors are located on the same plane, the ground connections for the active chips through via holes or ground report are eliminated, thus leading in more ease for connecting the active parts (here the amplifiers/phase shifters) and in more compact designs. Another advantage of coplanar technology is that each element characteristic can be adjusted and improved through additional geometric parameters. According to this degree of freedom, high-directivity couplers can then be easily achieved by minimizing the difference between the phase velocities of the two normal modes [43].

In our example, we consider three pairs of parallel coupled lines with up to two amplifiers within each passive ring resonator to achieve a second-order structure. The considered topology is shown in Fig. 25. With a methodology discussed in the article on active-filter design tools and techniques alluded to above, the noise performance of such structures can be analytically optimized. We use here the same amplifier/phase shifter as in Section 4.4. The

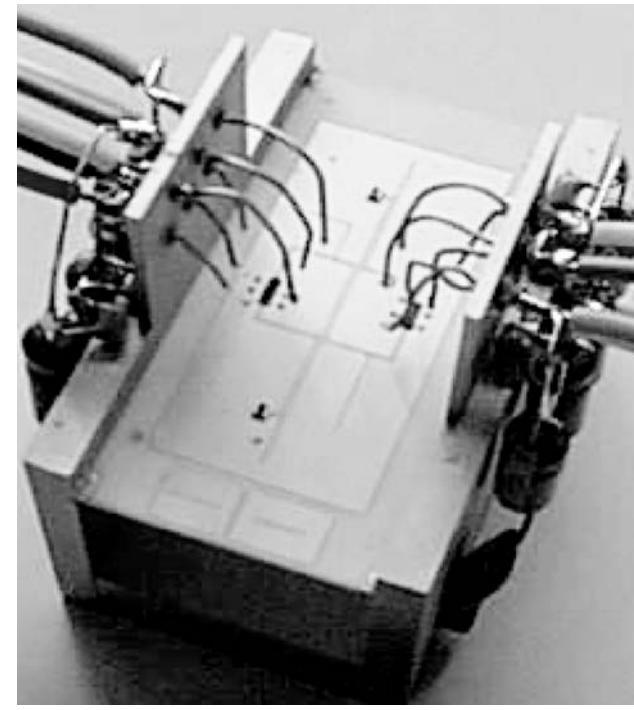

Figure 27. Photograph of the two-pole ring resonator recursive filter on its test fixture.

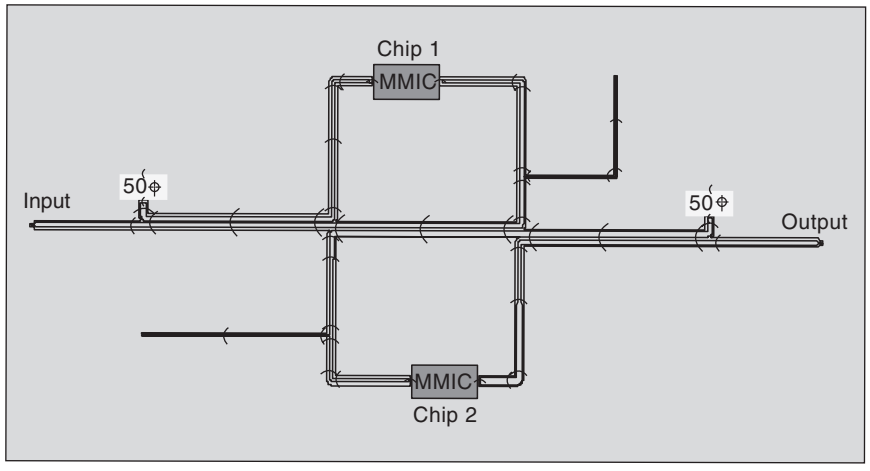

Figure 26. Two-pole ring resonator recursive filter layout in coplanar technology.

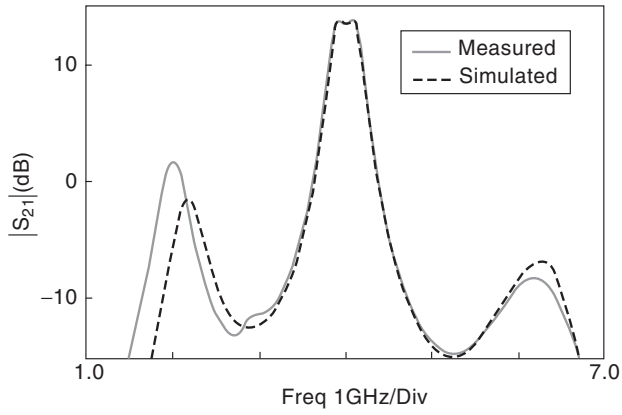

Figure 28. Comparison between simulation and measurements of the two-pole active ring resonator filter.

objective is to achieve a bandwidth $\Delta f = 120\,\text{MHz}$ with a ripple $\delta = 0.2\,\text{dB}$ within the passband. With $|G| = 2.2$, $F_A = 4.5$ at 4 GHz, the center frequency, we obtain $|S_{21}| = 13.7\,\text{dB}$, $|S_{ii}| < -12\,\text{dB}$. The noise figure is estimated to 6.5 dB. Figure 26 shows the layout of the active filter implemented on a 635-μm-thick alumina substrate ($\varepsilon_r = 9.6$). Dimensions of the filter are $38 \times 18\,\text{mm}$. A photograph of the circuit on its test fixture is given in Fig. 27.

Figure 28 shows a perfect agreement between simulated and experimental results. The gain of the filter is equal to 13.6 dB at 4 GHz. At center frequency, S_{11} and S_{22} are less than $-10\,\text{dB}$. Power consumption is about 24 mW.

A second alternative for high-order filter design resides on the fact that classical "ladder type" high-order recursive filter design can become greatly complex considering the n-way dividers/combiners and the stability analysis of such multifeedback structures.

In the proposed approach [44], classical recursive filter concepts are extended by decomposing the response as a set of unitary terms. Each of these corresponds to a first-order function characterized by its own weighting coefficients $\{a_i, b_i\}$ and delay-time parameters τ_i. The obvious advantage of this approach is a more flexible way to

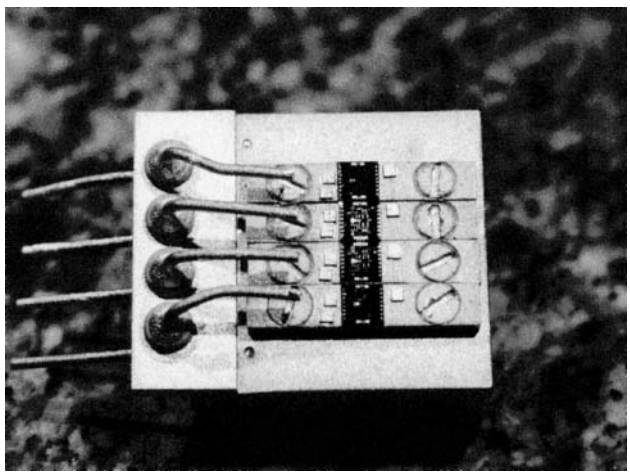

Figure 29. Test fixture of the four-cell filter configuration.

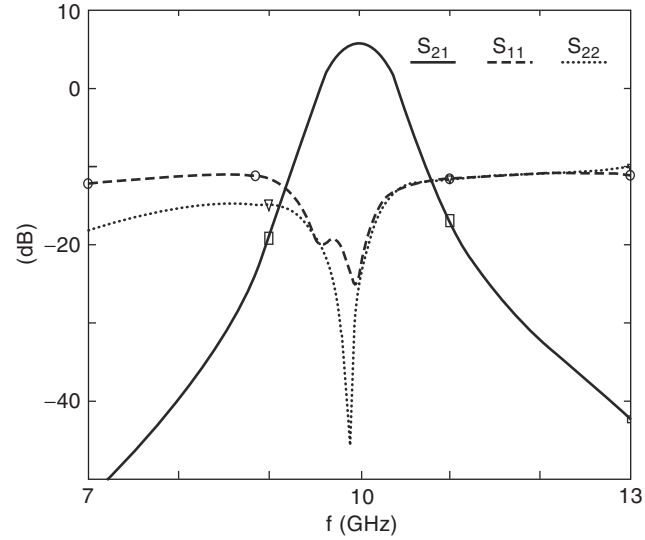

Figure 30. Measured S_{21} parameter of the four-cell filter with pairs of pole at 9.7 and 10.3 GHz.

individually control each pole frequency, selectivity, and also stability, thus simultaneously maintaining the global filter stability when cascading n unitary cells for a nth-order response. This also enables a tuning of the bandwidth and of the center frequency, whereas the classical approach does not give such flexibility. At least by cascading several elements of the same type, this approach also takes great advantage of MMIC technology reproducibility.

A physical implementation is shown in Fig. 29. Four $2 \times 2\,\text{mm}$ first-order tunable version of the chip of Fig. 19 are cascaded. Various response shapes can be obtained in terms of gain and bandwidth by adjusting center frequencies of the individual poles. Figure 30 shows excellent results obtained in the 4-chip configuration when two poles are located at 9.7 GHz and two at 10.3 GHz. Gain at center frequency is near 6 dB for a 670 MHz bandwidth. Good matching of the structure and $-40\,\text{dB}$ out-of-band rejection can also be noted in this case.

BIBLIOGRAPHY

1. R. V. Snyder, All the world is a filter, *IEEE MTT-S Newsl.* 5–10 (Fall 1990).
2. S. E. Sussman-Fort, Design concepts for microwave GaAs FET active filters, *IEEE Trans. Microwave Theory Tech.* **MTT-37**(9): 1418–1424 (1989).
3. H. Trabelsi and C. Cruchon, A varactor-tuned active microwave bandpass filter, *IEEE Microwave Guided Wave Lett.* **2**(6): 231–232 (1992).
4. S. R. Chandler, I. C. Hunter, and J. G. Gardiner, Active varactor tunable bandpass filter, *IEEE Microwave Guided Wave Lett.* **3**(3): 70–71 (1993).
5. U. Karacaoglu, I. D. Robertson, and M. Guglielmi, Microstrip bandpass filters using MMIC negative resistance circuits for loss compensation, *IMS'94, IEEE MTT-S Int. Microwave Symp. Digest*, 1994, pp. 613–616.

6. B. Hopf, I. Wolff, and M. Guglielmi, Coplanar MMIC active bandpass filters using negative resistance circuits, *IMS'94, IEEE MTT-S Int. Microwave Symp. Digest*, 1994, pp. 1183–1185.
7. A. Brucher, C. Cenac, M. Delmond, F. Delpino, B. Madrangeas, Ph. Meunier, V. Madrangeas, L. Billonnet, and B. Jarry, Several methodologies for active filter design at microwaves, *Int. J. RF Microwave Comput. Aided Eng.* **7**(3): 250–267 (1997).
8. F. Delpino, V. Madrangeas, L. Billonnet, B. Jarry, and P. Guillon, Dual mode dielectric resonator microwave active filters, *Microwave Opt. Technol. Lett.* **7**: 330–332 (1994).
9. B. Madrangeas, B. Jarry, P. Guillon, J. Larroque, B. Theron, and D. Parise, Three-pole DR microwave bandpass active filter, *IEE Proc. H.* **139**(2): 205–207 (1992).
10. K. B. Niclas, Active matching with commun gate MESFET, *IEEE Trans. Microwave Theory Tech.* **MTT-33**(6): 492–499 (1996).
11. R. S. Pengelly, J. R. Suffolk, J. R. Cockrill, and J. A. Turner, A comparison between actively and passively matched S-band GaAs monolithic FET amplifiers, *IEEE MTT-S Int. Microwave Symp. Digest*, 1981, pp. 367–369.
12. J. Tissier, W. Mouzannar, L. Billonnet, B. Jarry, and P. Guillon, Novel alternative design methods based upon combined amplification, matching and filtering approaches in MMIC technology, *IMS'2000, IEEE MTT-S Int. Microwave Symp. Digest*, 2000, Vol. 1, pp. 409–412.
13. W. Mouzannar, L. Billonnet, B. Jarry, and P. Guillon, A new design concept for wideband frequency-tunable and high-order MMIC microwave active recursive filters, *Microwave Opt. Technol. Lett.* **24**(6): 380–385 (2000).
14. ED02Ah monolithic process, *OMMIC, ED02Ah Design Manual*, GaAs Foundry and ASIC Design Center, *http://www.ommic.fr* (2000).
15. V. M. T. Lam and P. C. L. Yip, Microwave oscillator phase noise reduction using negative resistance compensation, *Electron. Lett.* **29**(4): 379–380 (1993).
16. A. V. Grebennikov, Stability of negative resistance oscillator circuits, *Int. J. Electric. Eng. Ed.* **36**: 242–254 (1999).
17. S. El Khoury, The design of active floating positive and negative inductors in MMIC technology, *IEEE Microwave Guided Wave Lett.* **5**(10): 321–323 (1995).
18. G. F. Zhang and J. L. Gautier, Broad-band, lossless monolithic microwave active floating inductor, *IEEE Microwave Guided Wave Lett.* **3**(4): 98–100 (1993).
19. U. Karacaoglu and I. D. Robertson, A MMIC active bandpass filter with FET negative resistance elements, *Microwave J.*, **7**: 76–79 (1996).
20. A. Brucher et al., Negative resistance monolithic circuits for microwave planar active filter losses compensation, *Proc. EuMC'95, 25th European Microwave Conf.* 1995.
21. S. E. Sussman-Fort, An NIC-based negative resistance circuit for microwave active filters, *Int. J. Microwave Millimeter Wave Comput. Aided Eng.* **4**(2): 130–139 (1994).
22. S. E. Sussman-Fort and L. Billonnet, Microwave, biquadratic, active-RC filter development, *Int. J. RF Microwave Comput. Aided Eng.* **2**(8): 102–115 (1998).
23. L. I. Babak, and M. V. Cherkashin, Interactive "visual" design of matching and compensation networks for microwave active circuits, *IMS'2001, IEEE MTT-S Int. Microwave Symp. Digest*, 2001.
24. R. M. Fano, Theoretical limitations on the broadband matching of arbitrary impedances, *J. Franklin Inst.*, **249**(1): 57–83, (Jan. 1950), **249**(2): 39–154 (Feb. 1950).
25. D. C. Youla, A new theory of broadband matching, *IEEE Trans. Circuit Theory*, **CT-11**(1): 30–50, (Mar. 1964).
26. B. S. Yarman and H. J. Carlin, A Simplified "Real Frequency" technique applied to broad-band multistage microwave amplifiers, *IEEE Trans. on Microwave Theory Techniques*, **MTT-30**(12): 2216–2222 (Dec. 1982).
27. A. Aksen and B. S. Yarman, A computer aided design technique for hybrid and monolithic microwave amplifiers employing distributed equalizers with lumped discontinuities, *IMS'2001, IEEE MTT-S Int. Microwave Symp. Digest*, 2001.
28. F. Biron, J. Ph. Plaze, L. Billonnet, D. Cros, B. Jarry, and P. Guillon, Design procedure for loss compensation of planar microwave filters using negative resistances for tunable bandstop and bandpass applications, *Proc. GAAS'2000, 8th European Gallium Arsenide and Related III-V Compounds Applications Symp.*, 2000, pp. 443–447.
29. HB200 monolithic process, UMS United Monolithic Semiconductors, *www.ums-gaas.com*.
30. J. Ph. Plaze, L. Billonnet, B. Jarry, and P. Guillon, A 2-pole bandpass filter assisted by a MMIC impedance for losses compensation and frequency control, *Proc. EuMC'2001, 31th European Microwave Conf.*, 2001.
31. C. Rauscher, Microwave active filters based on transversal and recursive principles, *IEEE Trans. Microwave Theory Tech.* **MTT-33**(12): 1350–1360 (1985).
32. M. J. Schindler, and Y. Tajima, A novel MMIC active filter with lumped and transversal elements, *IEEE Trans. Microwave Theory Tech.* **MTT-37**(12): 2148–2153 (1989).
33. L. Billonnet, B. Jarry, and P. Guillon, Theoretical and experimental analysis of microwave tunable recursive filters using power dividers, *IMS'93, IEEE MTT-S Int. Microwave Symp. Digest*, 1993, Vol. 1, pp. 185–188.
34. L. Billonnet et al., Design concepts for microwave recursive and transversal filters using Lange couplers, *IMS'92, IEEE MTT-S Int. Microwave Symp. Digest*, 1992, Vol. 2, pp. 925–928.
35. M. Danestig, H. Johansson, A. Ouacha, and S. Rudner, Low-noise active recursive MMIC filters, *IMS'97, IEEE MTT-S Int. Microwave Symp. Digest*, 1997.
36. R. Malmqvist, M. Danestig, S. Rudner, and C. Svensson, Analysis of intermodulation and noise performance for recursive active microwave integrated filters, *Proc. EuMC'99, 29th European Microwave Conf.*, 1999, pp. 60–63.
37. M. Delmond, L. Billonnet, B. Jarry, and P. Guillon, Microwave tunable active filter design in MMIC technology using recursive concepts, *IMS'95, IEEE MMWMC-S Microwave and Millimeter-Wave Monolithic Circuits Symp. Digest*, 1995, pp. 105–108.
38. P. K. Ikäläien, An RLC matching network and applications in 1–20 GHz monolithic amplifier, *IEEE MTT-S Int. Microwave Symp. Digest*, 1990, pp. 503–506.
39. A. Cenac, L. Nénert, L. Billonnet, B. Jarry, and P. Guillon, MMIC broadband analog phase shifter and gain circuit for frequency-tunable microwave planar multipole active filter categories, *Microwave Opt. Technol. Lett.* **25**(5): 311–318 (2000).
40. L. Nénert, L. Billonnet, B. Jarry, P. Guillon, C. Quendo, E. Rius, and G. Tanné, Compact high-order planar ring-resonator filters optimized in noise in coplanar technology,

IMS'2001, IEEE MTT-S Int. Microwave Symp. Digest, 2001, Vol. 3, pp. 1441–1444.

41. M. Houdart, Coplanar lines: application to broadband microwave integrated circuits, *Proc. EuMC'76, 6th European Microwave Conf.*, 1976, pp. 49–53.
42. L. Nenert, A. Cenac, L. Billonnet, B. Jarry, P. Guillon, C. Quendo, E. Rius, and G. Tanne, Use of coplanar technology advantages for tunable active planar looped filter structures optimised in noise, *Proc. EuMC'2000, 30th European Microwave Conf.*, 2000.
43. E. Rius, T. Le Gouguec, K. Hettak, J. Ph. Coupez, and S. Toutain, Broadband high directivity 3 dB coupler using coplanar waveguide technology, *IMS'95, IEEE MTT-S Int. Microwave Symp. Digest*, 1995, pp. 671–674.
44. M. Delmond, L. Billonnet, B. Jarry, and P. Guillon, High-order monolithic active recursive filter based upon multicellular approach, *IMS'96, IEEE MTT-S Int. Microwave Symp. Digest*, 1996, Vol. 2, pp. 623–626.

ACTIVE FILTERS: TOOLS AND TECHNIQUES FOR ACTIVE-FILTER DESIGN

LAURENT BILLONNET
BERNARD JARRY
BRUNO BARELAUD
University of Limoges
Limoges Cedex, France

1. INTRODUCTION

Whatever the application is, all communications systems—whether cellular, PCS, cable or satellite—require, in increasing quantity, a range of microwave filters with near-ideal characteristics to maximize communication capacity and signal processing efficiency and thus lower system costs. To satisfy these demands, engineers try to come up with design innovations and improved manufacturing processes of new filtering devices to reduce the cost of high-frequency communications. Since the early 1990s, engineers have also been increasingly interested in using active techniques for their compatibility with planar integrated monolithic technologies. Since the first microwave circuit was designed using a GaAs-based process, more and more attempts have been done nowadays to switch to silicon-based processes because of the resulting compact size and low-cost aspects.

We follow and gradually illustrate this tendency in this article. We first discuss the use of CAD tools for microwave and RF filter design, focusing particularly on optimization tools. We emphasize that, without any strong microwave design background and experience, this kind of tool unavoidably leads to nonreproducible and nonsystematic solutions. We then show the necessary implementation of analytical procedures to set and verify some essential characteristics of low-noise active devices, with examples of electrical stability criteria and noise performance calculation, prediction, and optimization. These two examples are illustrated through many integrated filter designs and measurements.

Section 3 deals with the description of tools and techniques for filter improvements. We first begin with an extended consideration of compensation techniques based not only on loss compensation but also on response selectivity and circuit dimensions. The technique is illustrated with the design of a one-pole interdigital filter and a two-pole coplanar filter in which response and size have been improved using this approach. We then generalize this principle to the "active-impedance profile" (AIP) technique and present an example application to multistandard and pseudomultipole filters.

In Section 4, novel approaches and new technologies for new microwave and RF communications needs are detailed. We first discuss the new application constraints driven by new communication standards. We then discuss GaAs processes to silicon-based technologies, emphasizing the differences between the two technologies in terms of processes themselves, and in terms of CAD tools, component implementation, compactness, relative size, and cost with two basic circuit examples. Migration to silicon-based processes also involves novel implementation approaches among which differential circuits. This last approach is illustrated with experimental results.

2. ANALYTICAL TOOLS AND PROCEDURES FOR ACTIVE FILTER DESIGN

2.1. Numerical CAD Optimization Tools

Since 1980, scientific production on microwave filters has grown extensively. This extension finds its sources from a technical perspective in:

- A permanent growth in device complexity
- A constant objective of reduction in size and weight
- The use of new materials and new technologies (superconductor materials, MEMs, planar monolithic technologies, etc.)

However, any experimented engineer knows that this growth of production is fueled mostly by novel modern computing systems and by the extraordinarily growing computation capabilities.

Without this computation power, many application would still be only perspectives:

- The development of precise electromagnetic simulation methods for planar (2D or 2.5D) or volumic (3D) circuits, such as the finite-element method, method of lines, or modal analysis
- The development of numerical synthesis methods taking into account a larger number of parameters such as losses or process limitations
- Global analysis methods simultaneously coupling in a single step various sorts of analysis that are sometimes very different