Data Conversion

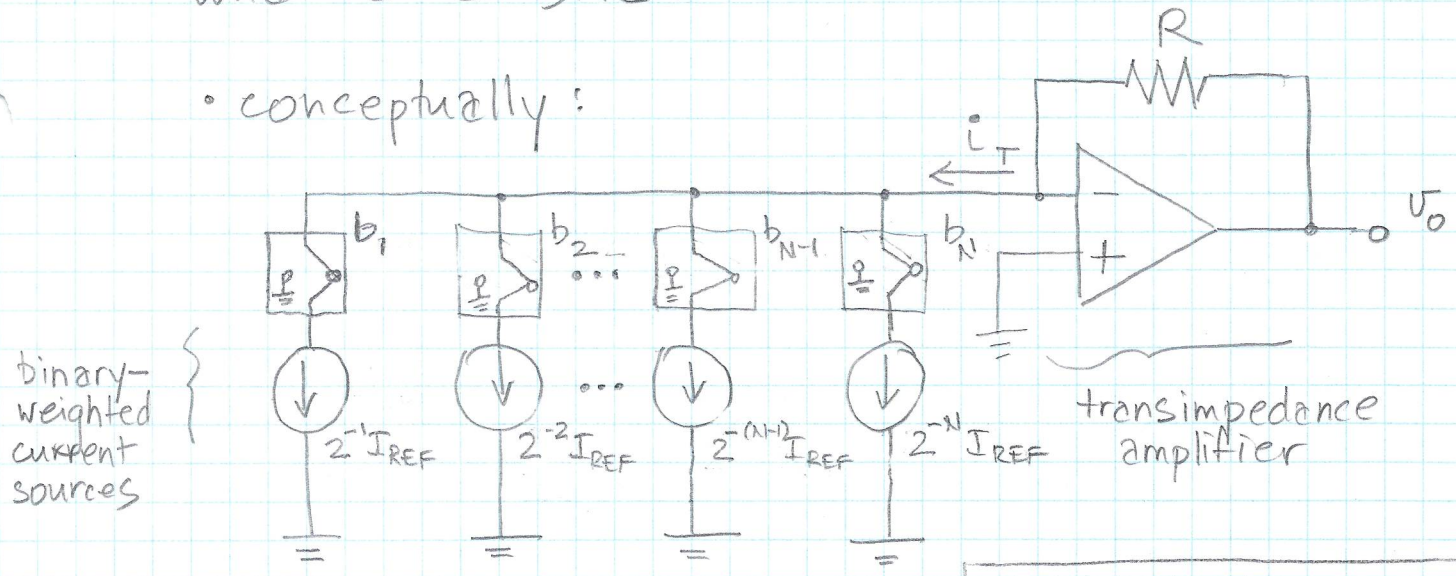
- ADCs & DACs aka A/Ds & D/As
- conceptual/theoretical foundation
- "Nyquist-Rate" & "Oversampled" architectures

D/A Conversion

- fundamental building block in data conversion

  → every ADC has a DAC inside it!

- what is a DAC?
  - conceptually:



$$v_o = R\, i_T \quad \text{(Ohm's Law)}$$

$$\cdots b_2 b_1 b_0 \bullet \underbrace{b_1 b_2 b_3 \cdots b_{N-1} b_N}_{\text{DAC implements this}}$$

$$\therefore \quad v_o = R \sum_{i=1}^{N} 2^{-i} I_{REF}\, b_i \quad \text{(KCL)}$$

$$\therefore \quad \boxed{v_o = (I_{REF} R) \sum_{i=1}^{N} 2^{-i} b_i = V_{REF} \sum_{i=1}^{N} 2^{-i} b_i}$$

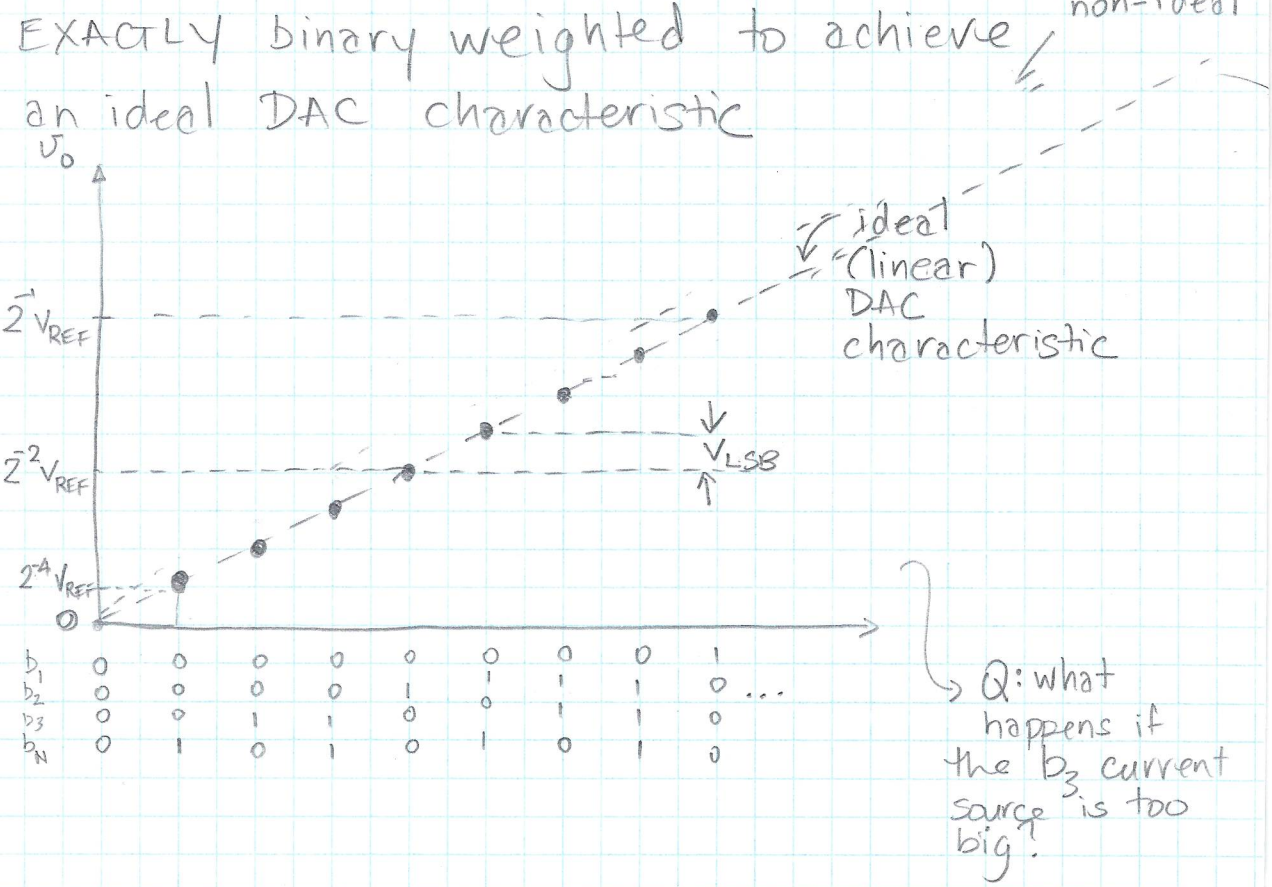
$$\text{where } V_{REF} = I_{REF} R$$

- so conceptually, DACs map a binary quantity (a fraction of the form $.b_1 b_2 b_3 \ldots b_N$) specified by binary values b_1 to b_N, into an analog voltage; although not evident from the diagram, we presume that the binary inputs are clocked since most digital systems operate according to a uniform clock

Element Size Mismatch

- major challenge with the DAC is the accuracy with which the binary-weighted elements are constructed

→ current sources above must be EXACTLY binary weighted to achieve an ideal DAC characteristic



- DAC linearity is often given in spec sheets and is important for SNR and dynamic range performance

- note the voltage associated with the least significant bit (LSB):

$$V_{LSB} = V_{REF}\, 2^{-N}$$

which defines the smallest allowable change in the DAC characteristic.

→ errors are often cast in terms of LSB; in fact the true accuracy of a DAC is determined in terms of V_{LSB}.

→ suppose $|v_{o,error}| = 0.01\, V_{REF}$

what is the corresponding V_{LSB}?

$$0.01\, V_{REF} = V_{REF}\, 2^{-N}$$

$$2^{-N} = 0.01$$

take $\log_2(\cdot)$ of both sides:

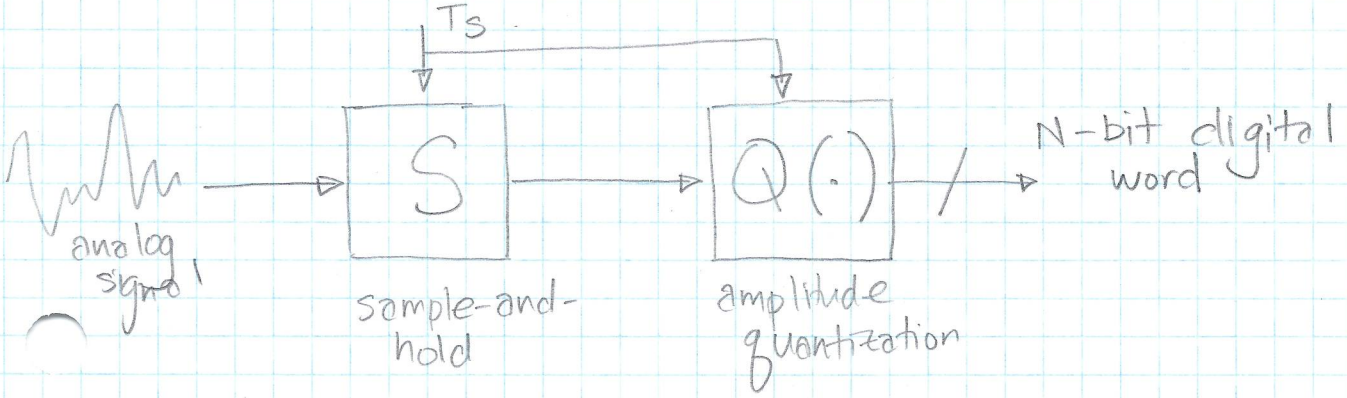
$$-N = \log_2 10^{-2} = -2\log_2(10) \doteq -2(3.322)$$

$$\therefore N = 6.64 \quad (6 \text{ bits of accuracy})$$

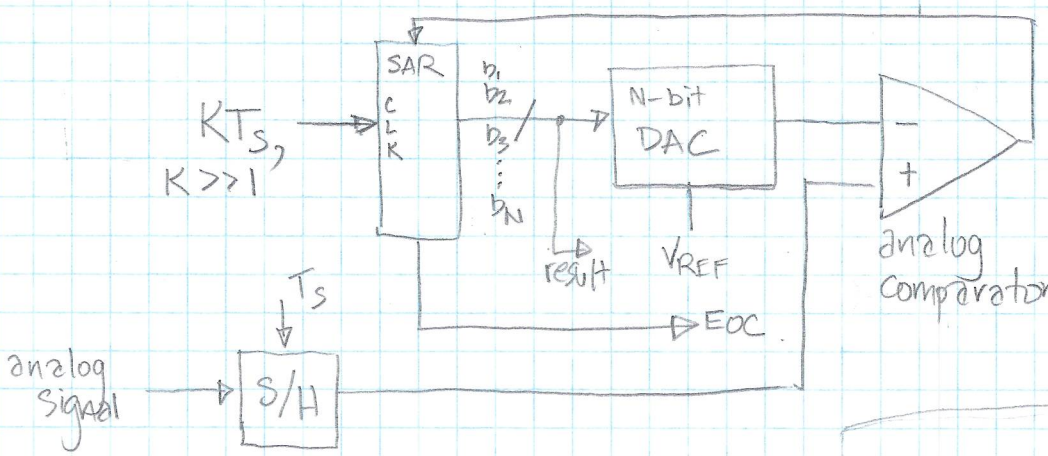
- Q: what's the maximum error I can have for 10-bit accuracy?

A/D Conversion

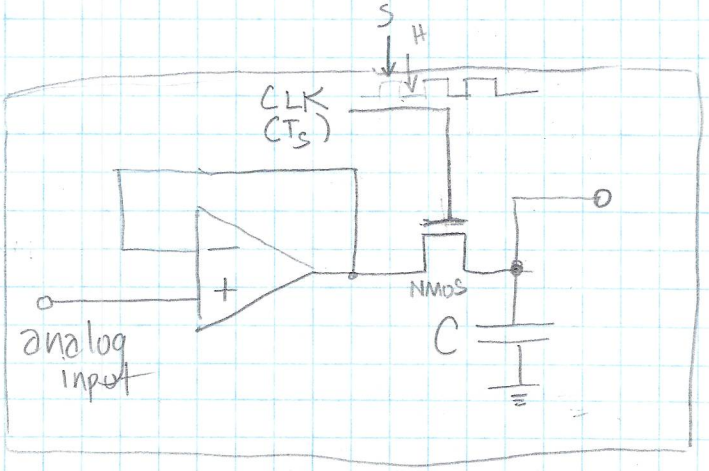
- a two-stage process (conceptually):



Successive-Approximation



sample-and-hold: circuit



- also: flash, pipelined Nyquist-Rate ADCs

  and: Δ-Σ Modulator Oversampled ADCs.