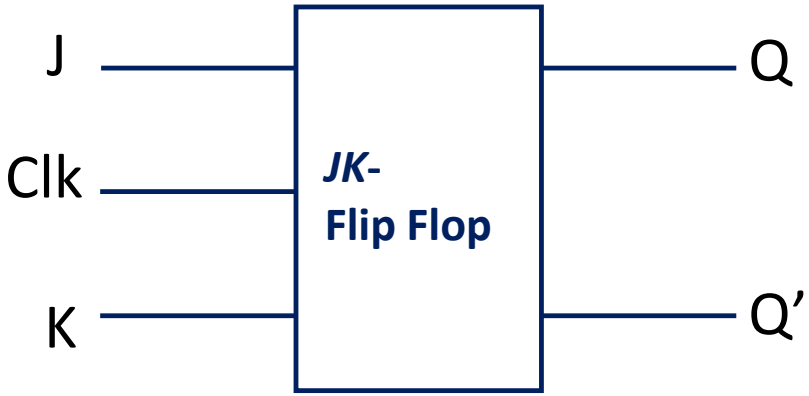
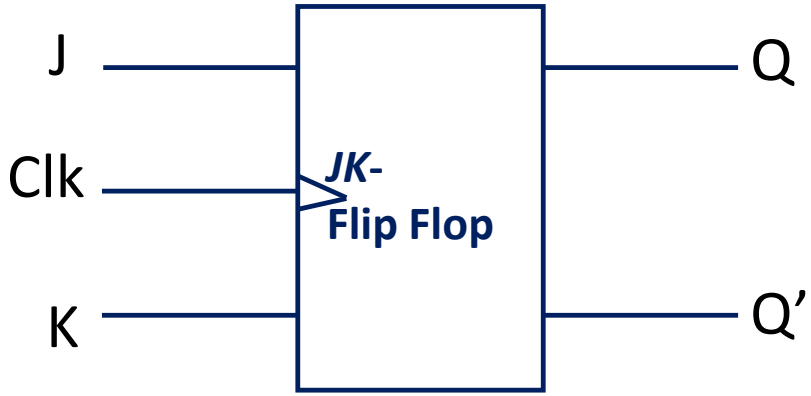
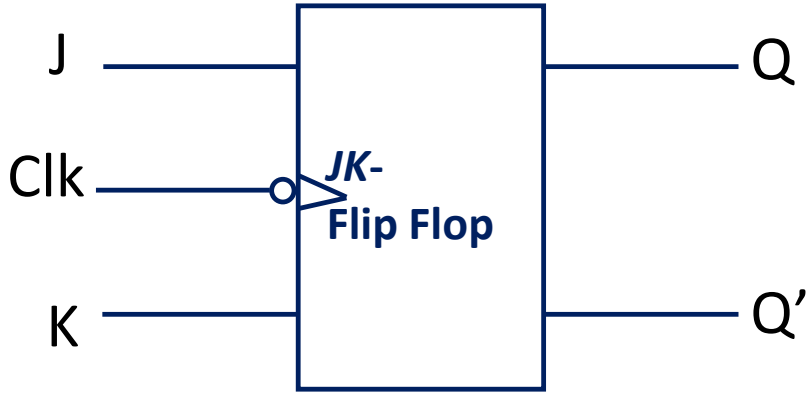
Triggering



Level triggering

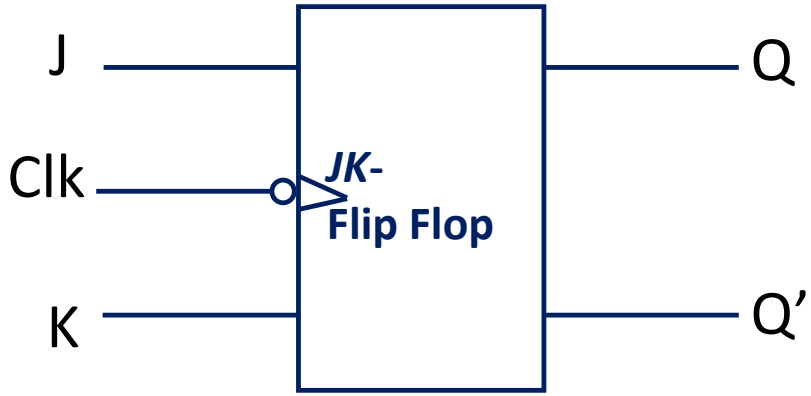


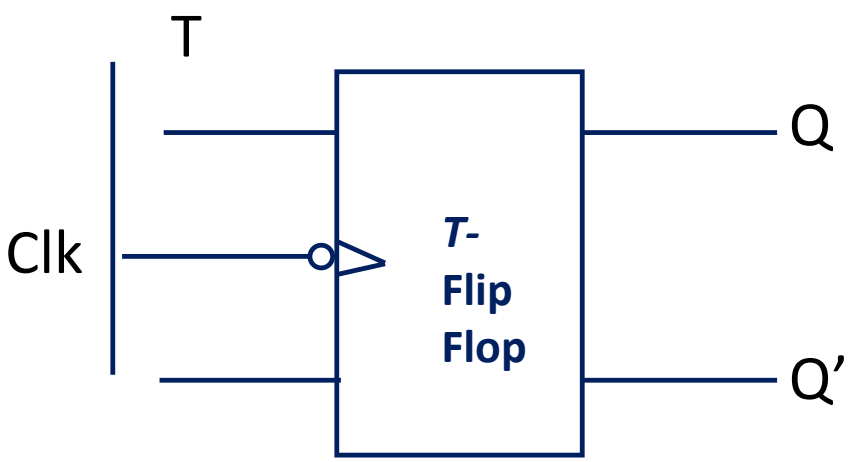
Positive edge- triggering

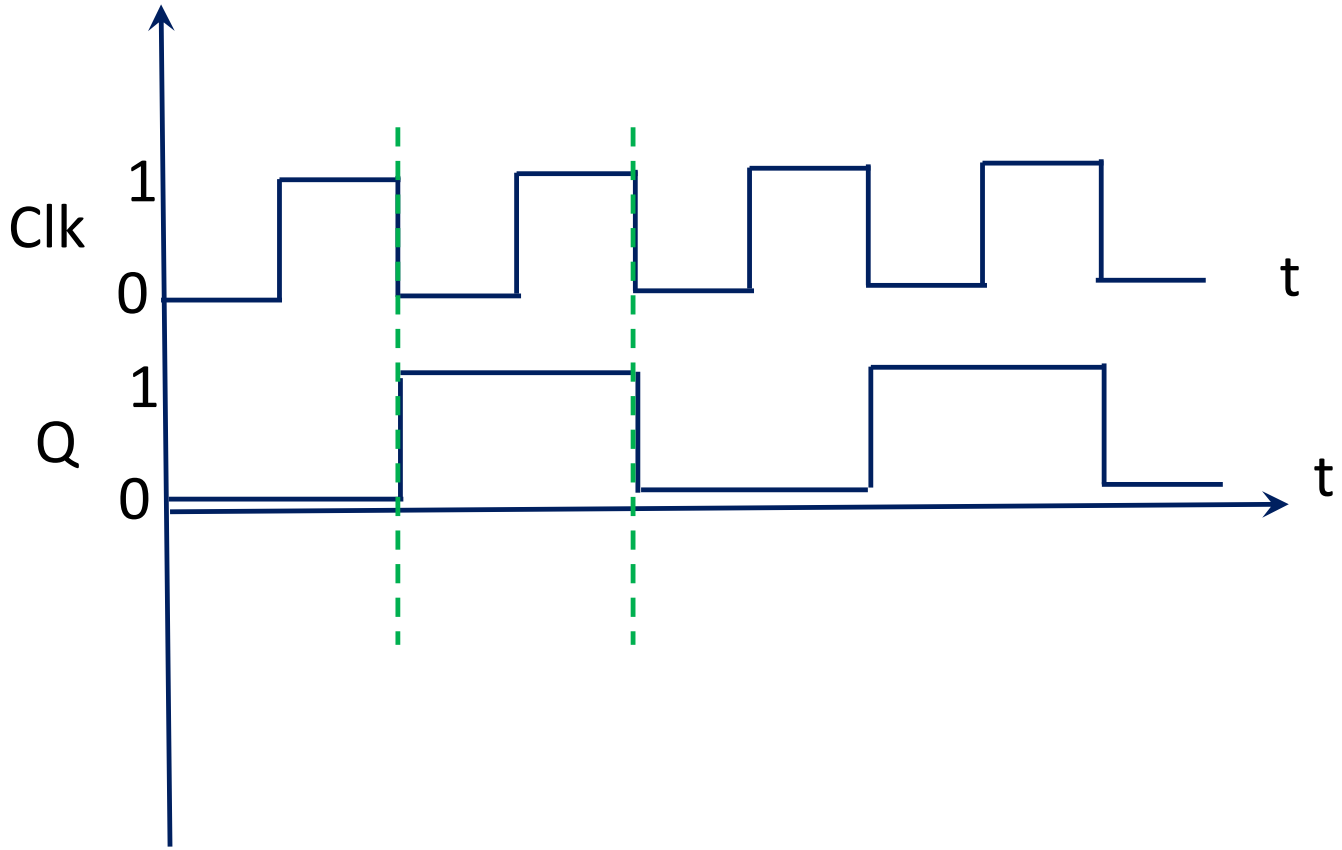


Negative edge- triggering

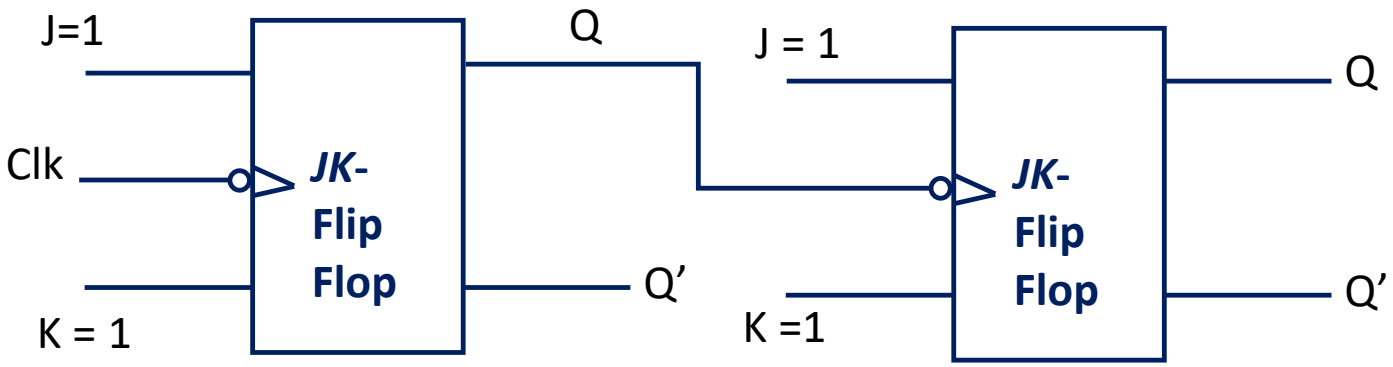
Toggle flipflop- Divide by 2 circuit



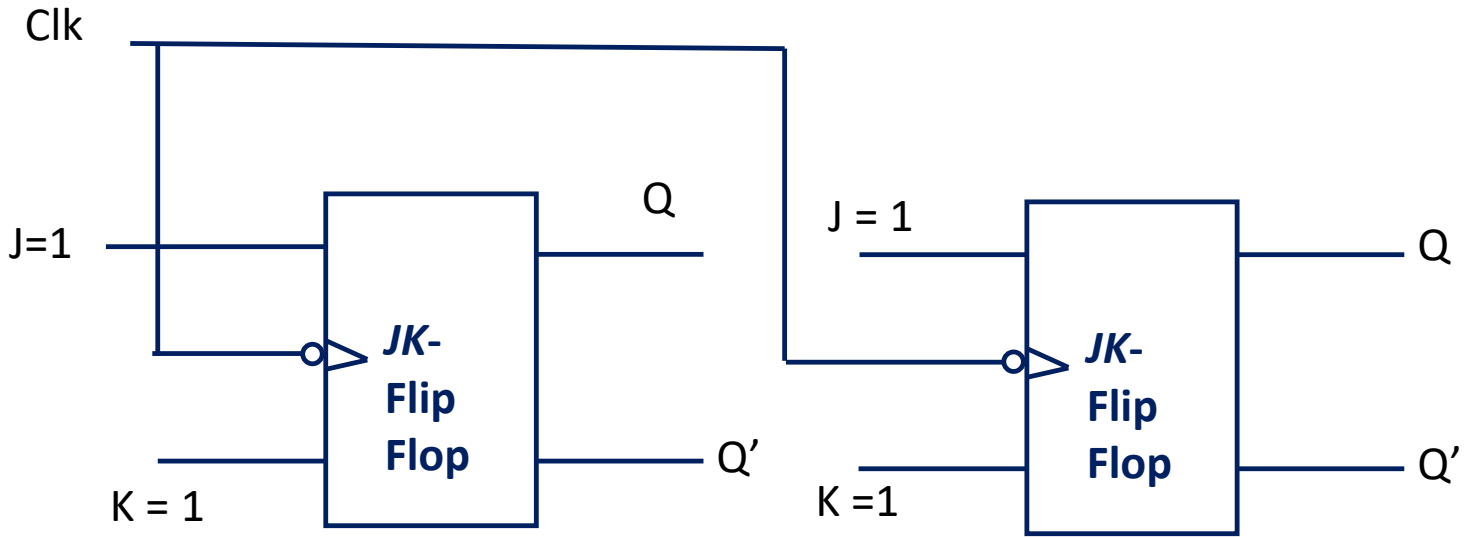




Synchronous and Asynchronous/ Ripple Counter

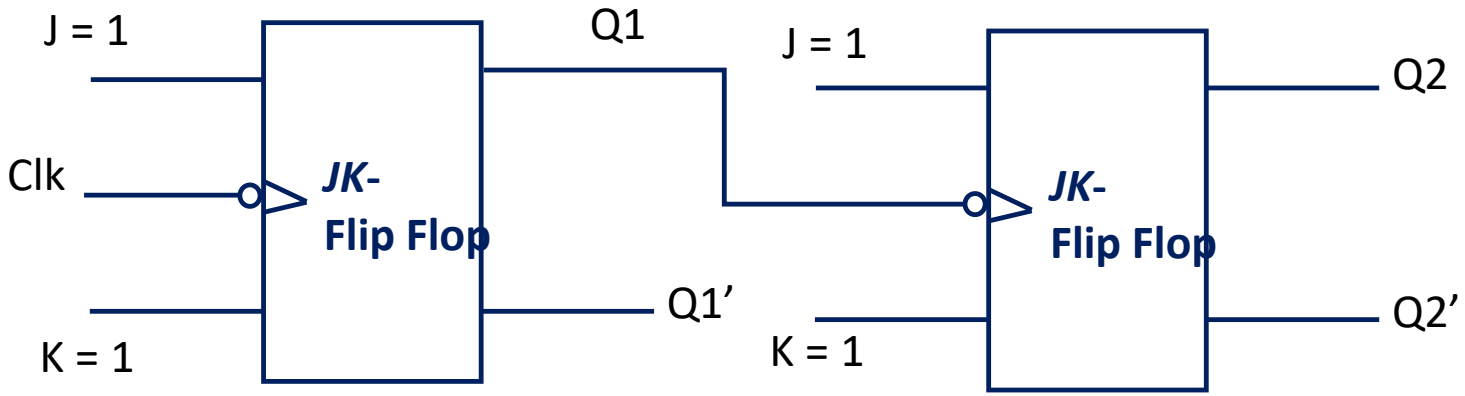


Asynchronous/ Ripple



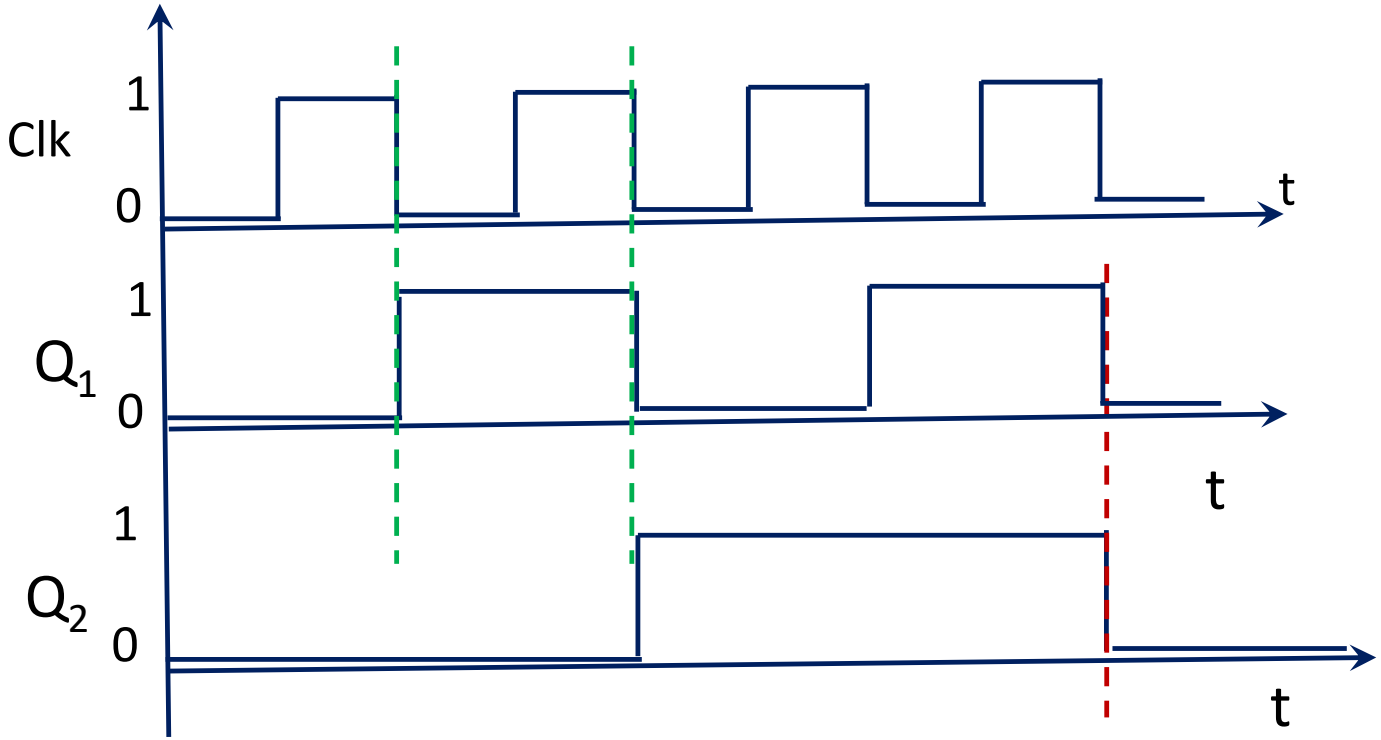
Synchronous

Asynchronous/ Ripple Counter

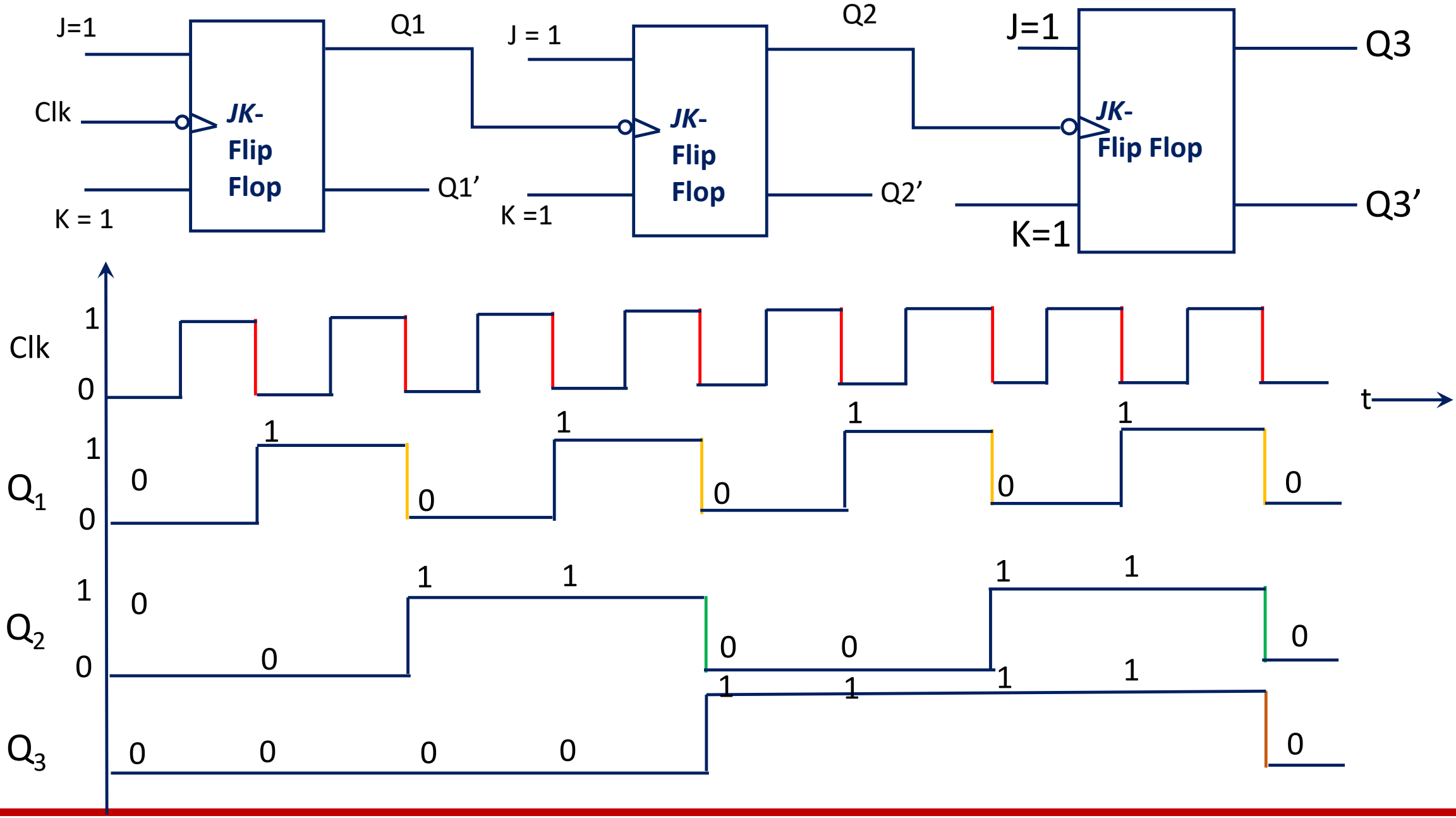


- *n* number of flipflops divide the input clock by 2^n.

clk	Q2	Q1
0	0	0
1	0	1
2	1	0
3	1	1



3-bit binary Ripple Counter



Asynchronous Down Counter

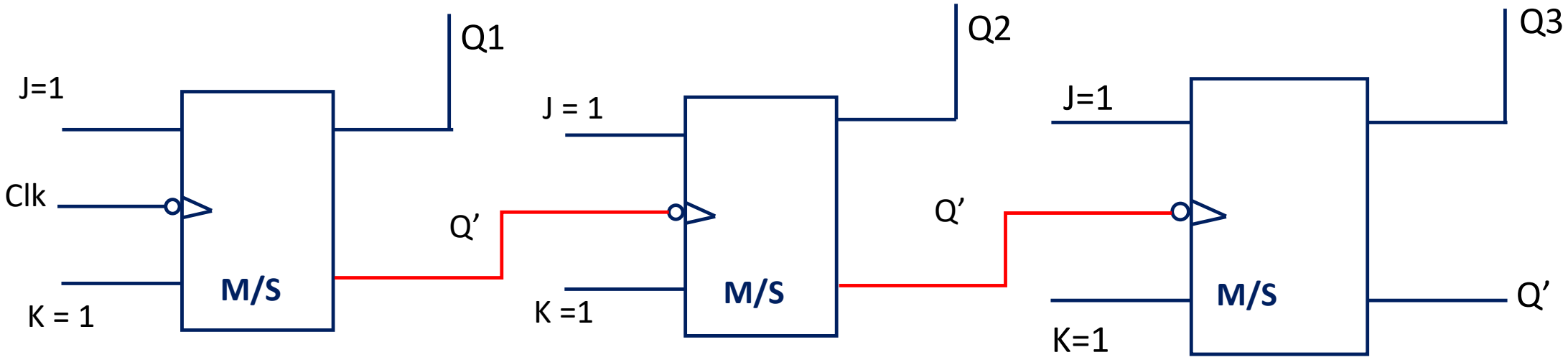
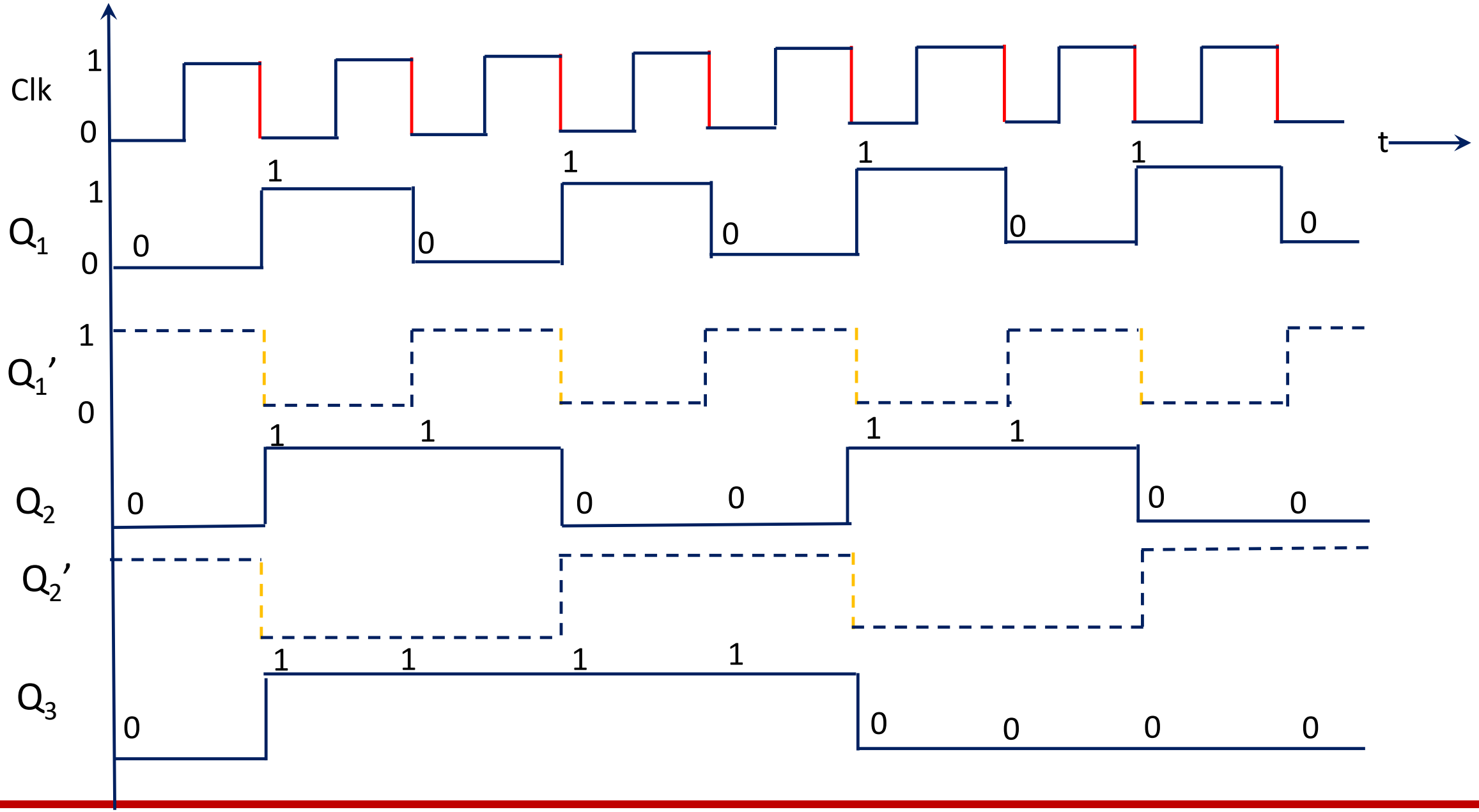


Fig. A

Asynchronous Down Counter Fig. A



Asynchronous Down Counter

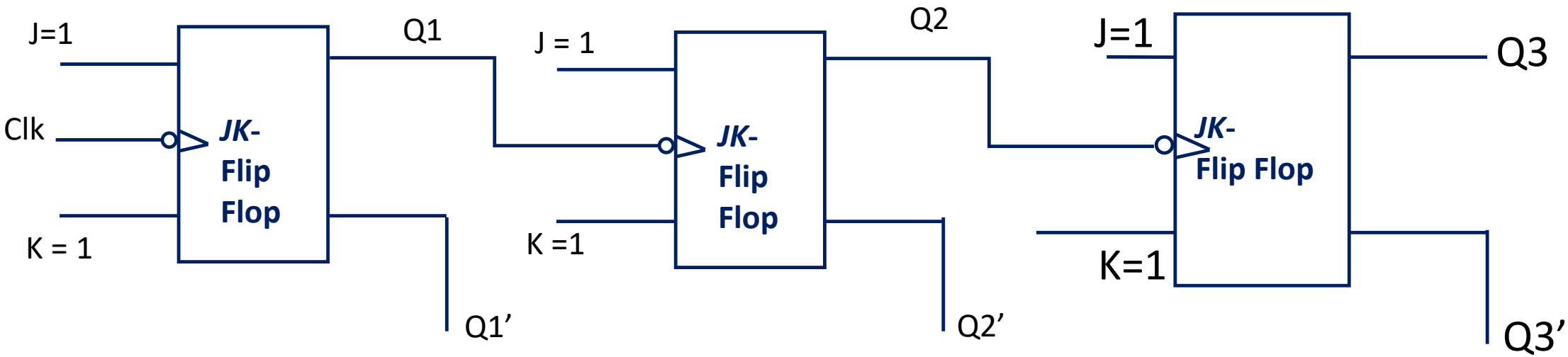
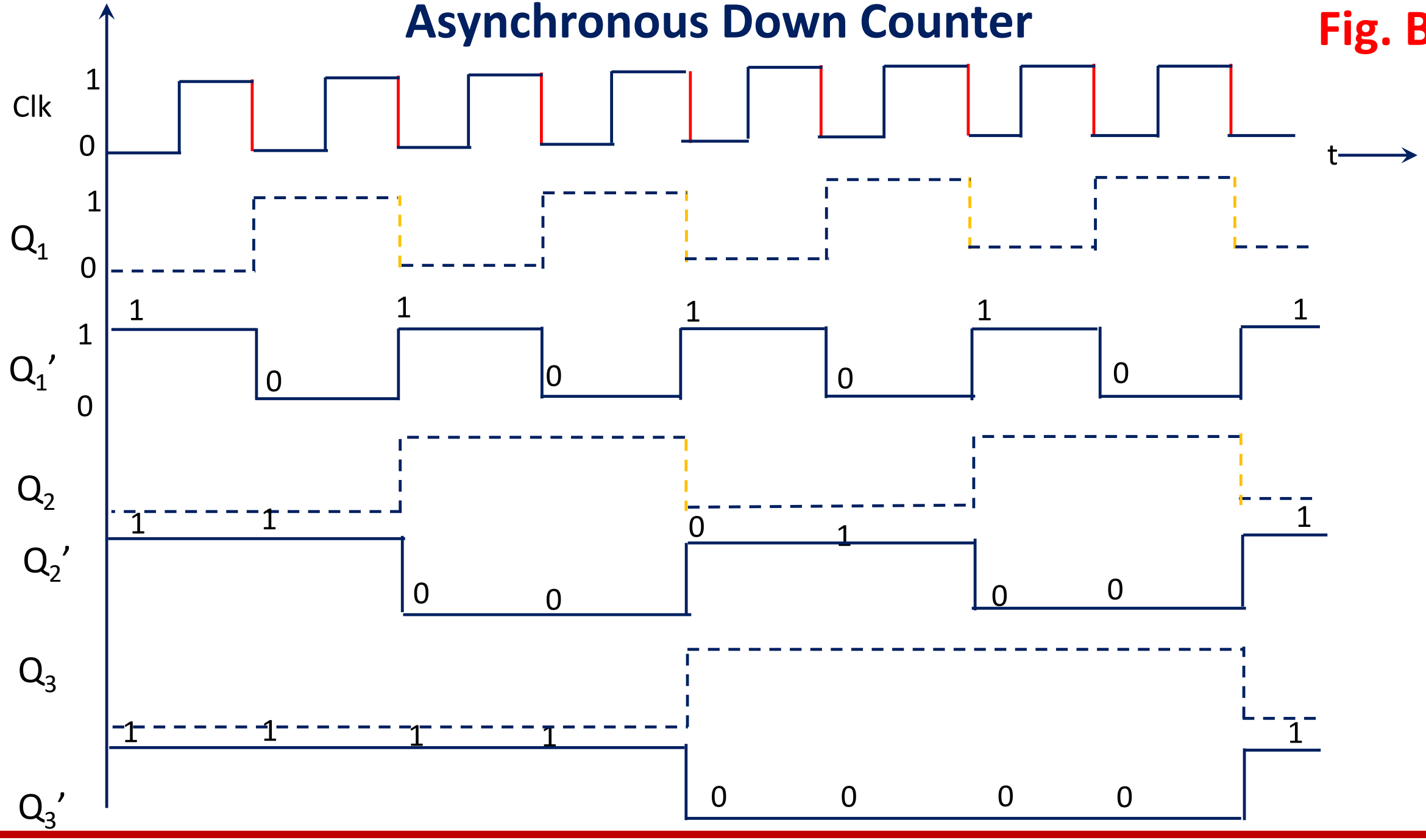


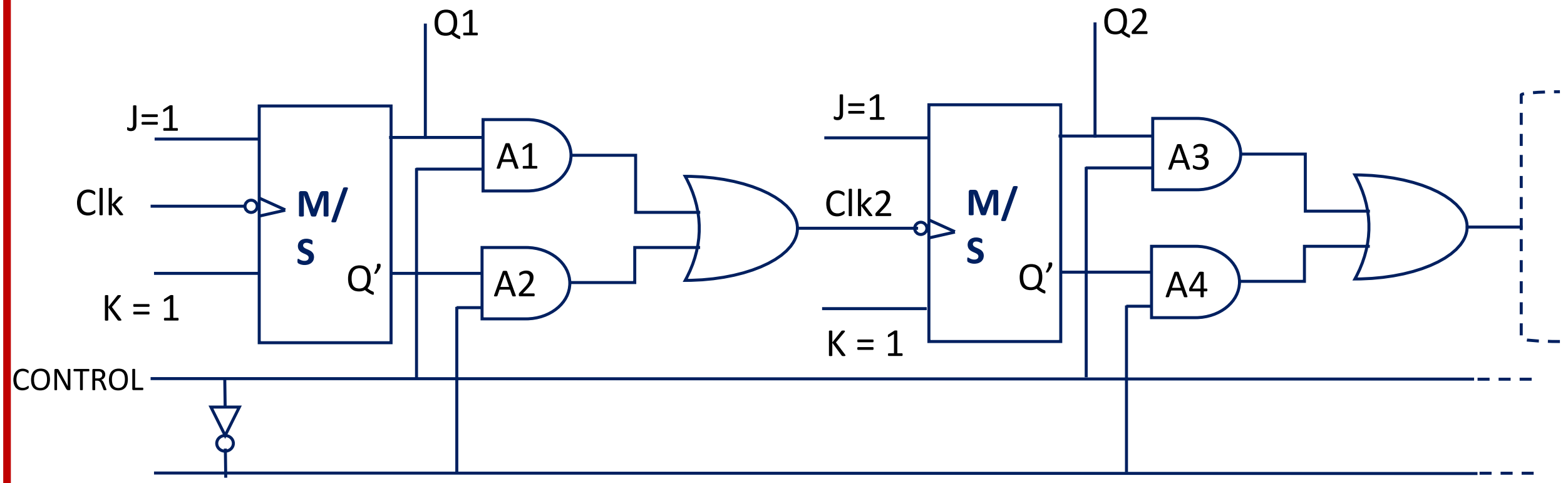
Fig. B

Asynchronous Down Counter

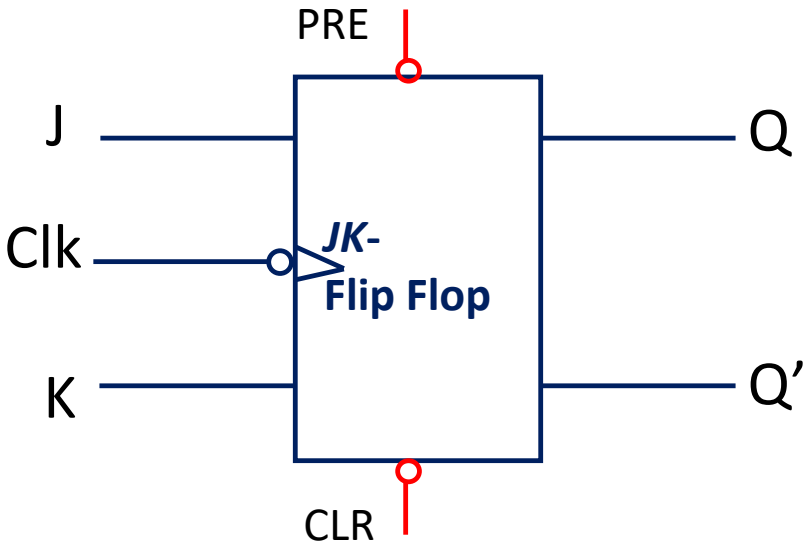
Fig. B



Asynchronous Up- Down Counter



- Propagation delay is larger because of additional AND-OR gates included in the circuit.



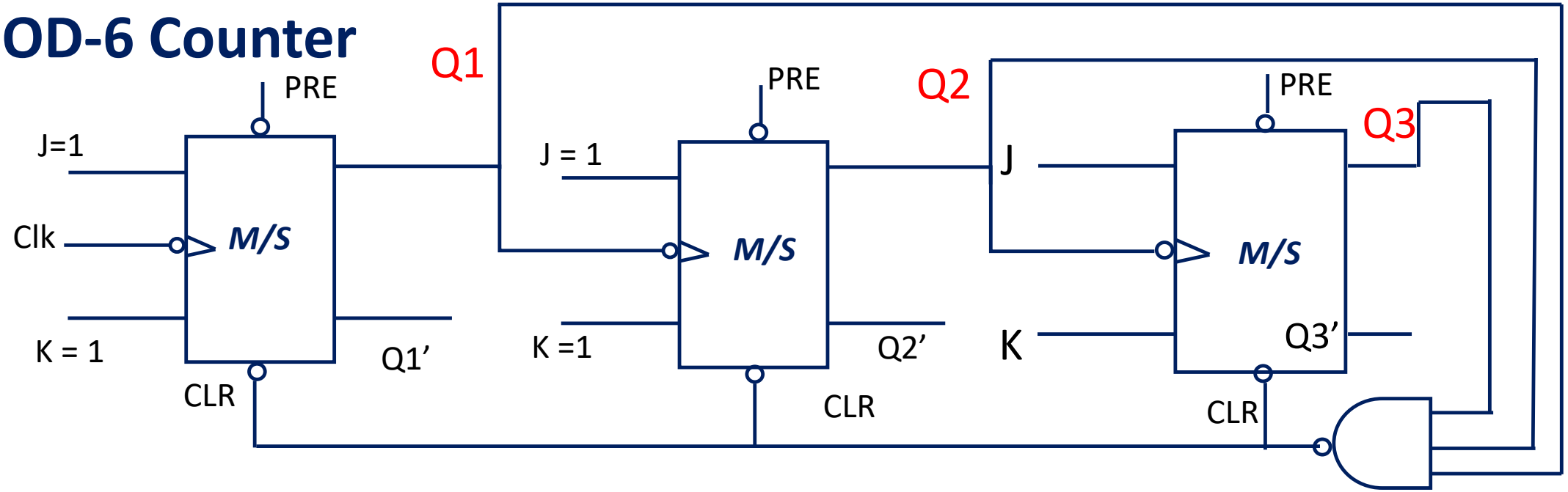
PRE	CLR	Q
0	1	1
1	0	0
1	1	Normal
0	0	Not allowed

- Preset and Clear inputs are active Low inputs i. e. Overriding inputs.
- Preset = 0, Q =1 i.e. PRE = 0, Sets the FF.
- Clear = 0, Q =0 i.e. CLR = 0, Resets the FF.
- PRE = 1 and CLR = 1, FF works normally.

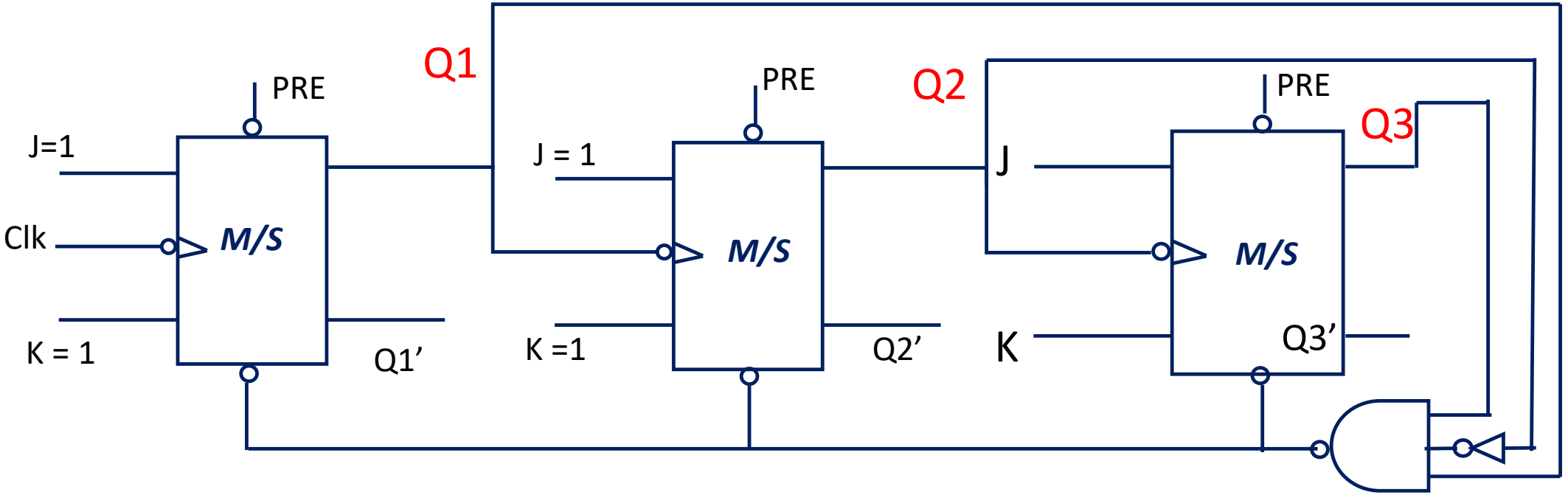
Counters with feedback

- A counter consisting of *n* flip flops can run through 2^n distinct states.
- Counters with moduli of 2,4,8, 16, 32 etc. can be constructed with appropriate number of flip flops.
- Counters with moduli different from 2,4,8,16, 32 etc. can be constructed by skipping desired number of states from larger modulus counter.
- Skipping of states is done by incorporating feedback in the counter circuit.

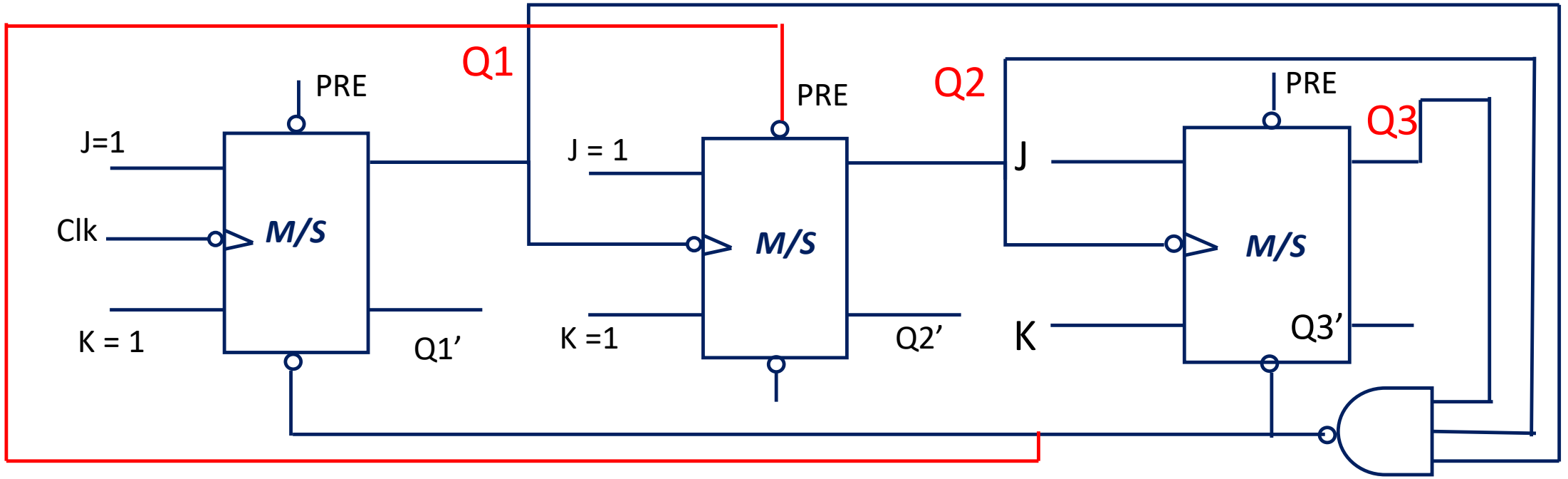
MOD-6 Counter



MOD-5 Counter



Ex. Counting from 2 to 6



Q3	Q2	Q1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0

Parallel or Synchronous Counter