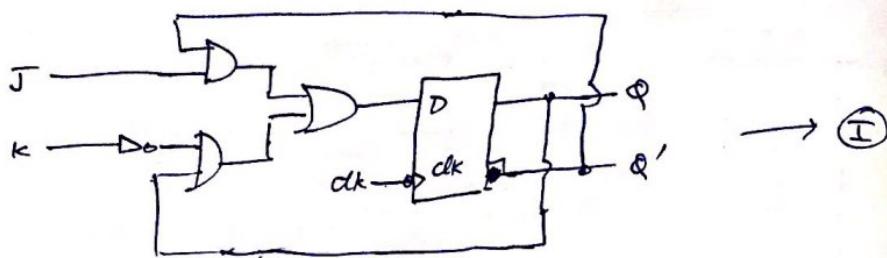


construction of flip flops using D-flip flops



		Next state		
D.	Q(t)	D	Q(t+1)	D
0	0	0	0	Q(t+1)
1	1	1	1	Q'(t+1)

$\Rightarrow D = \underline{Q(t+1)}$ $\rightarrow \textcircled{1}$

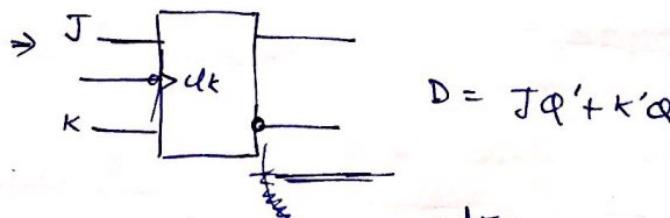
J	K	Q	Q'
0	0	0	No change
0	1	0	1
1	0	1	0
1	1	Toggle	Toggle

J	K	Q(t+1)
0	0	Q(t)
0	1	Q'(t)
1	0	Q(t)
1	1	Q'(t)

$$\Rightarrow Q(t+1) = JQ'(t) + K'Q(t) \quad \rightarrow \textcircled{2}$$

from $\textcircled{1} \& \textcircled{2}$: $D = JQ'(t) + K'Q(t)$

Therefore, this expression can be implemented by circuit $\textcircled{1}$.



T-flip flop:

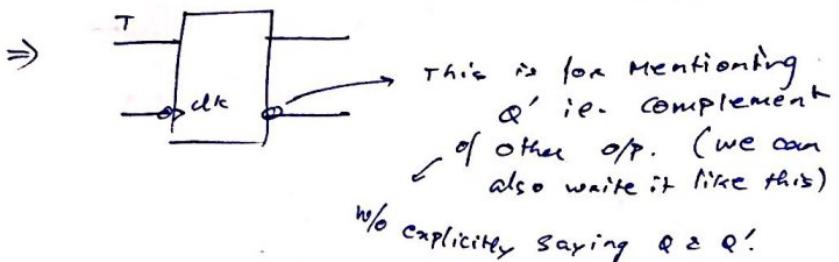
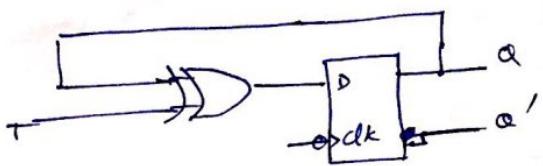
T	Q	Q'
0	Memory (No change)	
1	Toggles	

T	Q(t+1)
0	Q(t)
1	Q'(t)

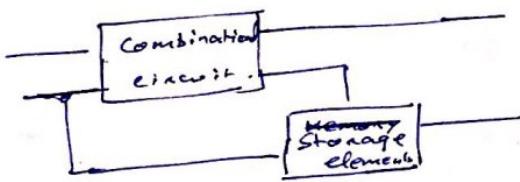
$$\Rightarrow Q(t+1) = TQ'(t) + T'Q(t)$$

$$= T \oplus Q(t)$$

$$\Rightarrow D = T \oplus Q(t)$$



Sequential circuit:



The next state depends on the current state of ~~the~~ Storage element & given i/p to combinational circuit

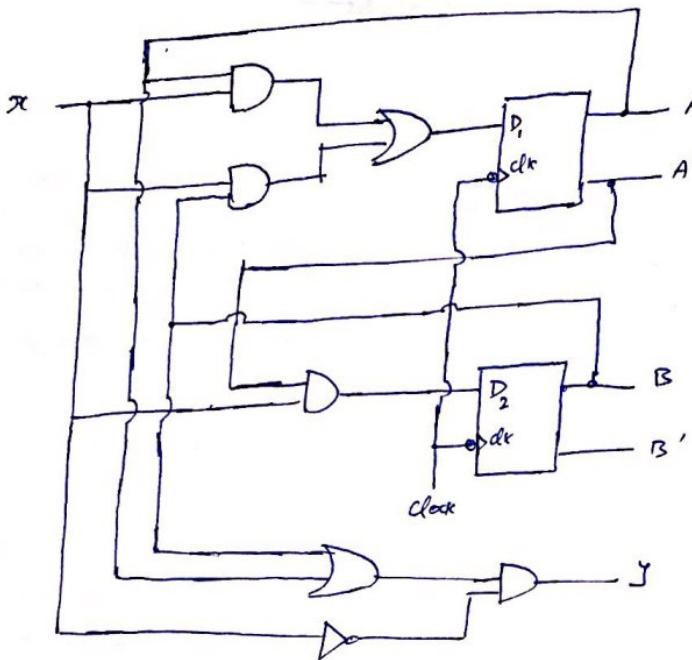
Analysis of Clocked sequential Circuits:

- Counters we designed go through a fixed sequence of states and have no i/p other than clock pulse that causes state to change
- Consider sequential circuits that have additional i/p's.
- In general, sequence of o/p's & sequence of flip flop states for such circuits will depend on the i/p sequence which is applied to the circuit.
- Given a sequential circuit & an i/p sequence, we can analyse circuit to determine flip-flop state sequence & o/p sequence by tracing 0 & 1 signals through circuit.
- Signal tracing is adequate for small circuits
- For large circuits, it is better to construct state graph or State table which represents behaviour of the circuit.

State Equations:

- A state eqn (also called transition eqn) specifies next state as a function of present state and i/p's

Eg:



- Consider two D-flip flops $A \& B$, an i/p x and an o/p y .
- Since D i/p of flip flop determines value of next state, it is possible to write a set of state eqns for circuit.

$$D_1 = A(t) \cdot x(t) + B(t) \cdot x'(t)$$

Since $A(t+1) = D_1 \Rightarrow A(t+1) =$

$$\therefore A(t+1) = \underline{A(t) \cdot x(t) + B(t) \cdot x'(t)} \rightarrow \textcircled{1}$$

$$\text{Similarly } B(t+1) = D_2 = \underline{A'(t) \cdot x(t)} \rightarrow \textcircled{2}$$

$$y(t) = x'(t) \cdot [A(t) + B(t)]$$

LHS of eqn $\textcircled{1}, \textcircled{2}$. with $(t+1)$ denotes next state of flip flop one clock edge later.

$$A(t+1) = Ax + Bx'$$

$$B(t+1) = A'x.$$

• Boo
gal
Since
S
• By
eq

- Flip F

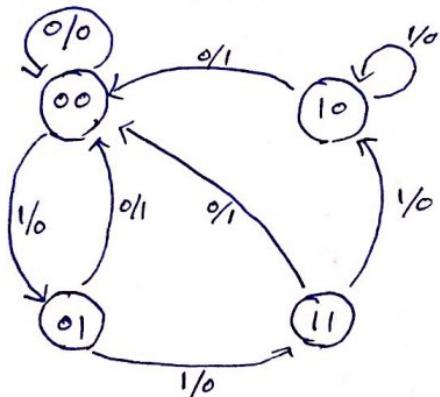
- Boolean exp for state eqns can be derived directly from gates that form combinational part of sequential circuits. Since D values of combinational circuit determines next state.

- By removing symbol (t) for present state, o/p boolean eqn:

$$y = (A+B)x'$$

State Table \rightarrow lists time sequence
of i/p, o/p
of flip flop
states

Present State	i/p		Next State		o/p y	
	$A(t)$	$B(t)$	x	$A(t+1)$	$B(t+1)$	
0 0	0	0	0	0	0	0
0 0	0	1	0	1	1	0
0 1	0	0	0	0	0	01
0 1	0	1	1	1	1	0
1 0	0	0	0	0	0	01
1 0	0	1	1	0	0	0
1 1	0	0	0	0	0	01
1 1	0	1	1	0	0	0

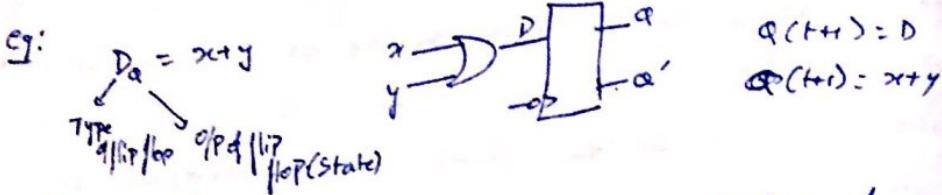


// Arrow directed from present state to next state.
Indication on arrows is input / output
ie. x/y .

This is called State diagram.

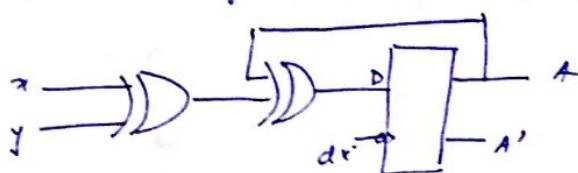
- Flip Flop input equations:

- Logic diagram of sequential circuit consists of flip flops & gates
- Interconnections among gates form a combinational circuit and may be specified with Boolean expressions
- Part of combinational circuit that generates external o/p's is described algebraically and is called o/p eqns.
- Part of circuit that generate i/p to flip flop is described algebraically and is called flip flop i/p eqn (excitation eqn)



- D flip flop eqns constitute a convenient algebraic form for specifying logic op.
- The letter is to specify which type of flip flop.

Eq: $D_x = A \oplus x \oplus y$



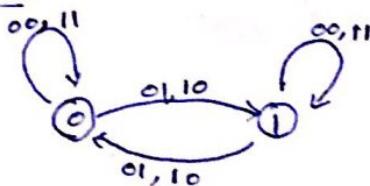
Next State values are obtained from state eqn.

$$A(t+1) = A \oplus x \oplus y.$$

State table:

Present State	I/P.	Next State
A(t)	x y	A(t+1)
0	0 0	0
0	0 1	1
0	1 0	1
0	1 1	0
1	0 0	1
1	0 1	0
1	1 0	0
1	1 1	1

State diagram:

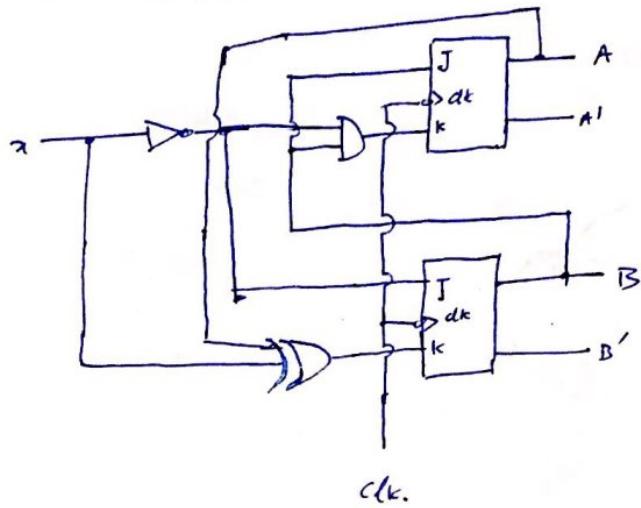


Analysis with JK flip-flops:

- For D-type flip flop, State eqn is same as I/P eqn.
- For other types, it's necessary to refer corresponding characteristic values.

For JK flip flop: $Q(t+1) = JQ'(t) + K'Q(t)$

eg:



- Circuit has no o/p; ∴ State table does not need an o/p column.
(o/p of flip flop may be considered as o/p in this case)
- Circuit is specified by flip flop i/p eqns.

$$J_A = B \quad K_A = Bx'$$

$$J_B = x' \quad K_B = x \oplus A$$

Next state for JK flip flop $\Rightarrow Q(t+1) = JQ(t) + K'Q(t)$

Present State		i/p.	Next State	
A	B	x	$A(t+1)$	$B(t+1)$
0	0	0	0	1
0	0	1	0	0
0	1	0	1	1
0	1	1	1	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1

$$Q(t+1) = JQ'(t) + K'Q(t)$$

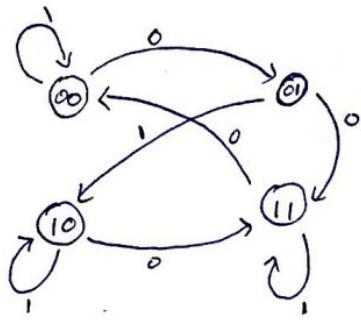
$$A(t+1) = J_A A'(t) + K'_A A(t)$$

$$= J_A A' + \underline{K'_A A}$$

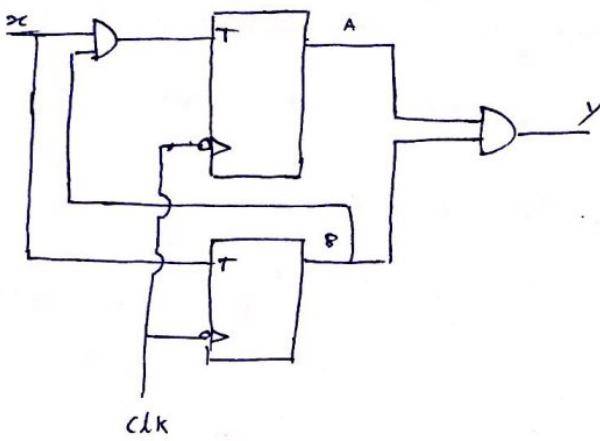
$$\text{II}^H B(t+1) = J_B B' + K'_B B.$$

J_A	K_A	J_B	K_B
0	0	1	0
0	0	0	1
1	1	1	0
1	0	0	1
0	0	1	1
0	0	0	0
1	1	1	1
1	0	0	0

State Diagram:



e.g:



$$T_A = x_1 B$$

~~A $\oplus B$~~

$$T_B = x$$

$$Q(t+1) = T \oplus Q(t)$$

$$A(t+1) = T_A \oplus A$$

$$= x_1 B \oplus A = (x_1 B)' A + x_1 B A'$$

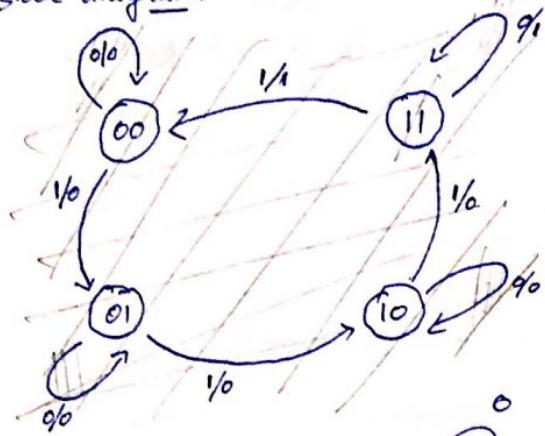
$$B(t+1) = T_B \oplus B = (x_1' B') A + x_1 B A'$$

$$= x_1 \underline{\oplus} B = x_1' B + x_1 B'$$

$$Y = \underline{A \cdot B}$$

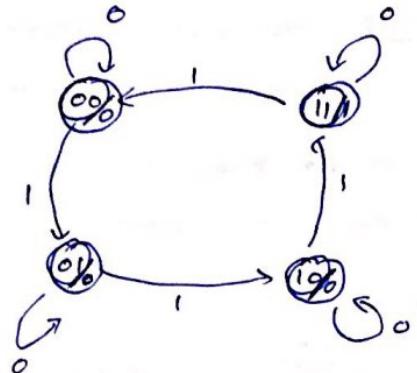
Present state		I/P	Next state		O/P
<u>A(t)</u>	<u>B(t)</u>	<u>x</u>	<u>A(t+1)</u>	<u>B(t+1)</u>	<u>y</u>
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
01	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1

State diagram:



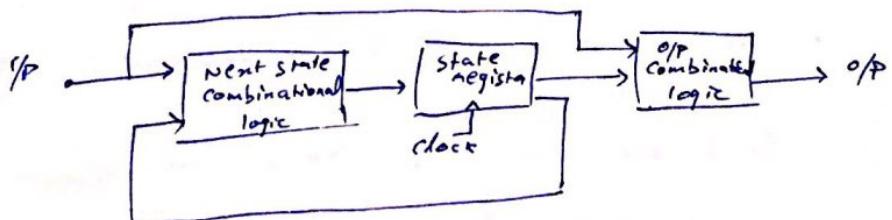
Since o/p is
state dependent alone
and hence is drawn
inside the state circles.

Since each circle
gives out same
o/p so it can
be ~~written~~ drawn
as
and o/p
is state
dependent
hence o/p
can be
drawn in
the circle.



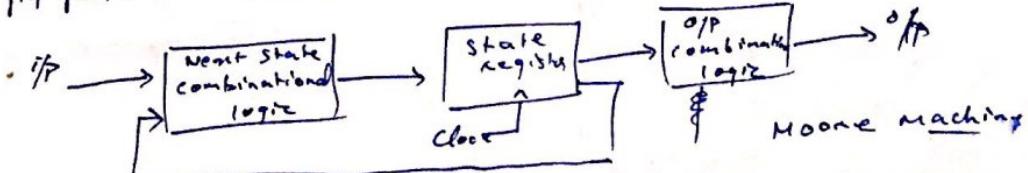
- Mealy and Moore Models of Finite State Machines:

- 2 TYPES of clocked sequential circuits - Mealy machine and Moore machine.
- Circuit in which o/p depends on both present state of flip flops and the value of circuit i/p's \rightarrow Mealy machine.



Mealy machine

- Circuit in which o/p depends only on present state of flip flops \rightarrow Moore machine



Moore machine

- 2 models of sequential circuits are referred as finite state machine (FSM)

- In Moore model, o/p of sequential circuit are synchronized by clock, \therefore they depend only on flip flop o/p that are synchronized by clock.

state Table
Present

\Rightarrow State reduction & Assignment

- Analysis of sequential circuits starts from circuit diagram & concludes in state table/diagram
- Design (synthesis) of sequential circuit starts from set of specifications and ends in logic diagram
- Certain prop of sequential circuits that may simplify a design by reducing no. of gates and flip flops it uses.
In general, reducing no. of flipflops reduces costs.
- State Reduction:
 - Reduction in no. of flip flops in sequential circuit is referred to State reduction problem.
 - Only i/p-o/p sequences are important; internal states are merely used to provide required sequences.
For that reason, states marked inside circles are denoted by letter symbols instead of binary values.
 - This is in contrast to binary counter, wherein binary value sequence of states themselves is taken as o/p.
 - There are infinite no. of i/p sequences that may be applied to circuit.

They
are
equivalent

//
ALU De

ALU:

Arithm

ADD

A_0 — [
 B_0 —]

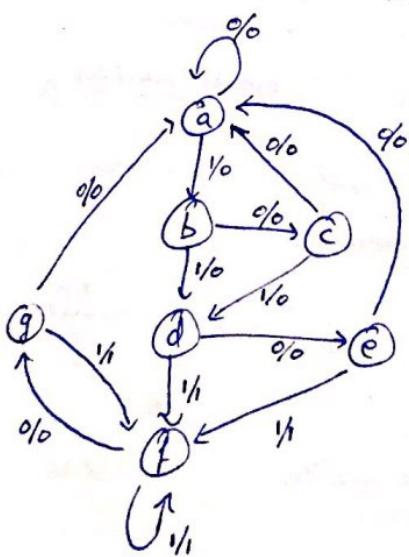
$A-B$

A_0
 B_0' —

Sele

Each results in unique o/p Sequence

e.g.:



state Table:

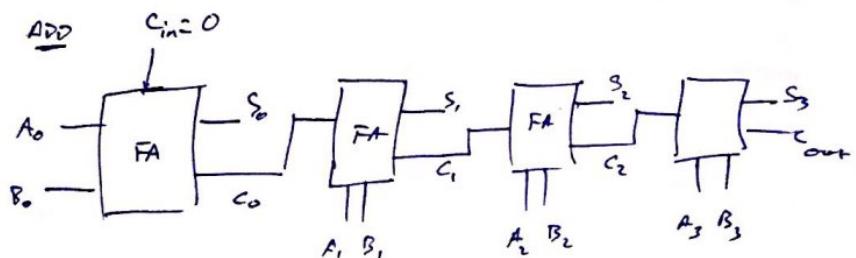
Present State	Next State		O/P	
	$x=0$	$x=1$	$x=0$	$x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

They
are
equivalent

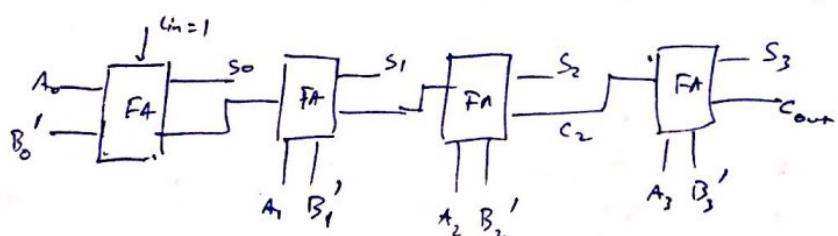
ALU Design:

ALU: Arithmetic and Logic unit

Arithmetic: ADD, ADC, SUB, SBB, INC, DEC



$$A - B = A + B'$$



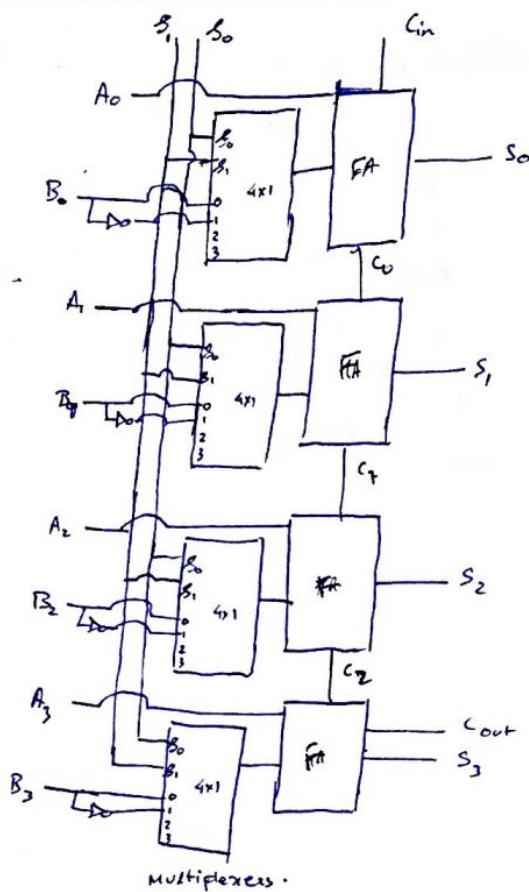
Selection to make the full adder allow us to choose:

$A_0, B_0, C_{in}=1 \rightarrow$ Add with carry

$A_0, B_0, C_{in}=1 \rightarrow$ Subtraction

$A_0, B_0, C_{in}=0 \rightarrow$ subtraction with borrow. i.e. $A_0 + B_0'$

$A_0, B_0, C_{in}=0 \rightarrow$ Add.



controls:
 Address:
 State
 I/P
 O/P

From +
 output
 So w/
 each c

✓
 Equivalen

Redu
 :- Sta
 n

Given initial state and I/P, we find output.

Control: Given initial state s_0
Start: State: $a \ a \ b \ c \ d \ e \ f \ f \ g \ f \ g \ a$
State: ~~$a \ a \ b \ c \ d \ e \ f \ f \ g \ f \ g \ a$~~

i/p 0 1 0 1 0 1 1 0 1 0 0 → i/p Sequence
o/p 0 0 0 0 0 1 1 0 1 0 0 → o/p sequence

Present State

From the State table, 'e' and 'g' & gives the same output ~~for~~ and next state for same input.

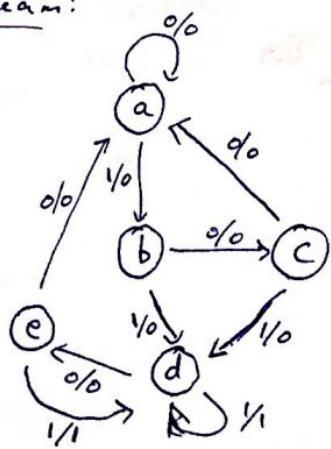
So whenever we find 'e' or 'g' we ^{can} replace it with each other.

<u>Present State</u>	<u>Next State</u>		<u>O/P:</u>	
	$x=0$	$x=1$	$x=0$	$x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	e	0	1

Equivalent.

<u>Present state</u>	<u>Next state</u>		<u>O/P:</u>	
	$x=0$	$x=1$	$x=0$	$x=1$
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1

Reduced
∴ State diagram:



→ Reduced State Table

Now, we check if this reduced state diagram matches with the given i/p and o/p sequence.

<u>state</u>	a a b c d e d d e a
i/p:	0 1 0 1 0 1 1 0 1 0 0
o/p:	0 0 0 0 0 1 1 0 1 0 0

Sequence det
c

If we

X~~xx~~. It holds true.

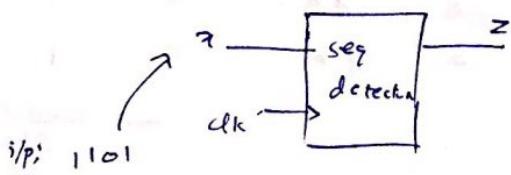
State Assignment:

<u>State</u>	Assignment 1 <u>Binary</u>	Assignment 2 <u>Gray code</u>	Assignment 3 <u>One-hot</u>
a	000	000	00001
b	001	001	00010
c	010	011	00100
d	011	010	01000
e	100	110	10000

cg:
Des
mon

Sequence Detection:

- Suppose we wish to design a circuit that detects a sequence in a string of bits coming through an input line (i.e. input is serial bit stream)



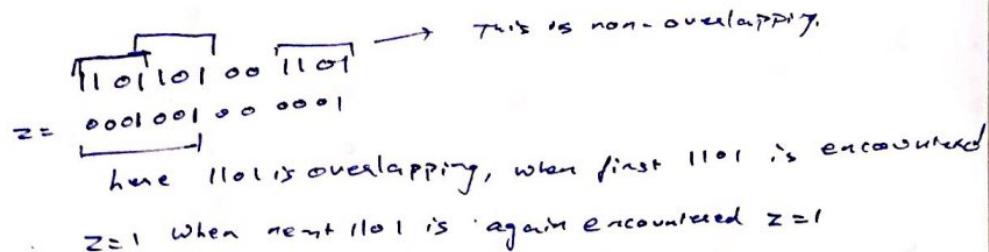
We start from MSB:

$$\begin{array}{llll} x=1 & x=1 & z=0 & z=1 \\ z=0 & z=0 & z=0 & z=1 \end{array}$$

→ complete of sequence will give $z = 1$.

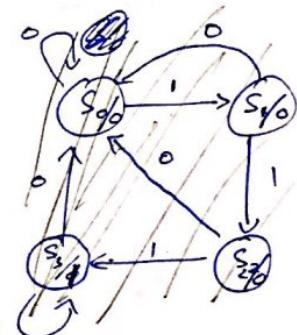
Sequence detector has two types:
overlapping and non-overlapping

If we need to detect 1101 sequence.



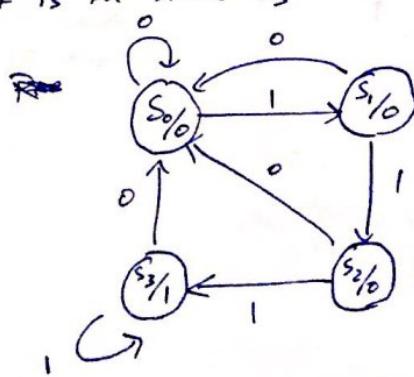
Q9: Design a circuit which detects sequence of three or more consecutive 1's in a string of bits.

- It is derived by starting with state S_0 , reset state. If i/p is 0, circuit stays in S_0 , if it's 1, it goes to S_1 to indicate that 1 has detected.
- If next i/p is 1, change is to S_2 to indicate arrival of 2 consecutive 1's, but if i/p is 0, state back to S_0 .
- Third consecutive 1 sends circuit to S_3 . If more 1's are detected, circuit stays in S_3 .
- Any i/p 0 sends circuit back to S_0 .



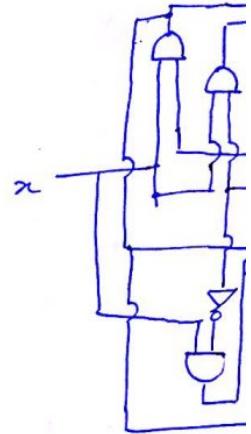
In this way, circuit stays in S_3 as long as there are three or more consecutive 1's received.

- This is meone sequential circuit, since o/p is 1 when circuit is in state S_3 and is 0 otherwise.



Present State			i/p x	Next State	o/p.	
	A	B			A	B
$S_0 \{ 0 0$	0	0	0	0 0	0	
	0	0	1	0 1	0	
$S_1 \{ 0 1$	0	1	0	0 0	0	
	0	1	1	1 0	0	
$S_2 \{ 1 0$	1	0	0	0 0	0	
	1	0	1	1 1	1	
$S_3 \{ 1 1$	1	1	0	0 0	0	
	1	1	1	1 1	1	

(by State Assignment)
Binary



$$\text{Since } D_A = A(t+1) \quad D_B = B(t+1)$$

$\cancel{D_A = \sum(3, 5, 7)}$	x	AB	D			
			00	01	11	10
	0		0	0	0	0
	1		0	1	1	1

$$D_A = A\bar{x} + Bx$$

$\cancel{D_B = \sum(1, 5, 7)}$	x	AB	A			
			00	01	11	10
	0		0	0	0	0
	1		1	0	1	1

$$D_B = A\bar{x} + B'x$$

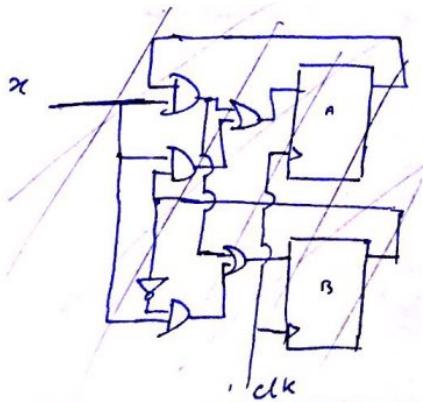
$$\therefore A(t+1) = A(t)x + B(t)\bar{x}$$

$$B(t+1) = A(t)x + B'(t)\bar{x}$$

$$Y = \sum(5, 7)$$

A	$B\bar{x}$	x			
		00	01	11	10
0	0	0	0	0	0
1	0	1	1	1	0

$$Y = A\bar{x}$$

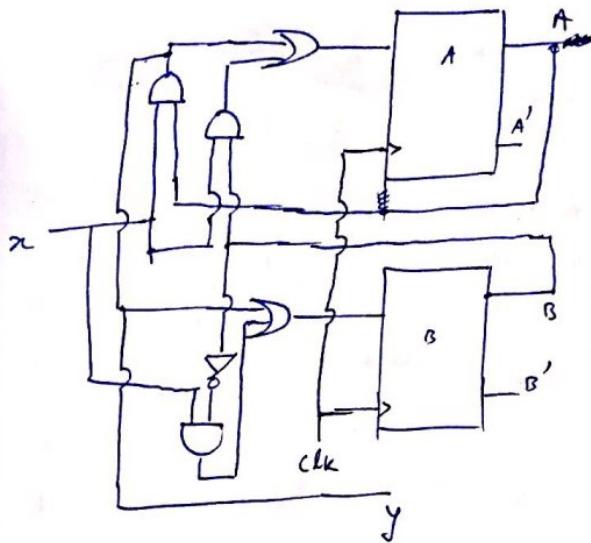


- Synthesis
Registers
J
Q CH

J
0
0
1

α C^t

T flip



- Synthesis using JK flip flop:

Recall:

JK flip flop:

$$Q(t+1) = JQ'(t) + K'Q(t)$$

<u>JK</u>	<u>$Q(t+1)$</u>
0 0	memory
0 1	Reset
1 0	Set
1 1	Toggle

<u>J</u>	<u>K</u>	<u>$Q(t)$</u>	<u>$Q(t+1)$</u>
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

<u>$Q(t)$</u>	<u>$Q(t+1)$</u>	<u>JK</u>
0	0	0 X
0	1	1 X
1	0	X 1
1	1	X 0

Called Excitation table.

T flip flop:

<u>T</u>	<u>Q</u>
0	memory
1	Toggle

<u>T</u>	<u>$Q(t)$</u>	<u>$Q(t+1)$</u>
0	0	0
0	1	1
1	0	1
1	1	0

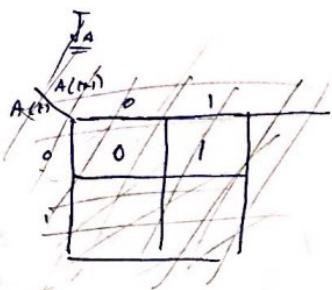
<u>$Q(t)$</u>	<u>$Q(t+1)$</u>	<u>T</u>
0	0	0
0	1	1
1	0	1
1	1	0

→ Excitation Table

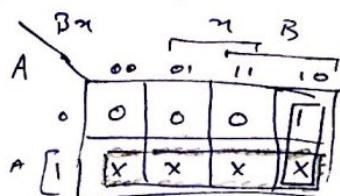
e.g:

Given Table:

Present State $A(t)$ $B(t)$	i/p x	Next state $A(t+1)$ $B(t+1)$		F _{t+1} or f ₁ or i/p eqns	
		$A(t+1)$	$B(t+1)$	J_A	K_A
0 0	0	0 0	0 0	0	X 0
0 0	1	0 1	0 1	0	X 1
0 1	0	1 0	1 0	1	X X 1
0 1	1	0 1	0 1	0	X X 0
1 0	0	1 0	1 0	X 0	0 X
1 0	1	1 1	1 1	X 0	1 X
1 1	0	1 1	1 1	X 0	X 0
1 1	1	0 0	0 0	X 1	X 1

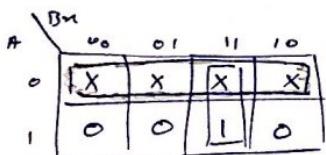


$J_A:$



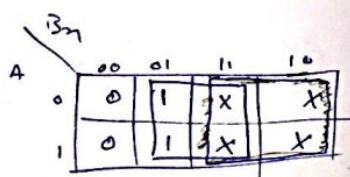
$$J_A = ABx'$$

$K_A:$



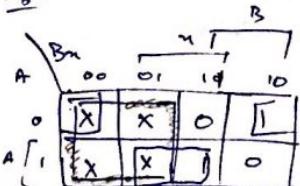
$$K_A = Bx'$$

$J_B:$



$$J_B = x'$$

$K_B:$



$$K_B = A\bar{x} + A'\bar{x}'$$

$$= (A \oplus x)'$$

$$\Rightarrow J_A = Bx' \quad K_A = B\bar{x}$$

$$J_B = x' \quad K_B = (A \oplus x)'$$

\therefore From the obtained expressions, we can draw the circuit.

Synthesis

00 0
00 1
01 0
01 1
10 0
10 1
11 0
11 1

cons

Pres

$A(t)$

0

0

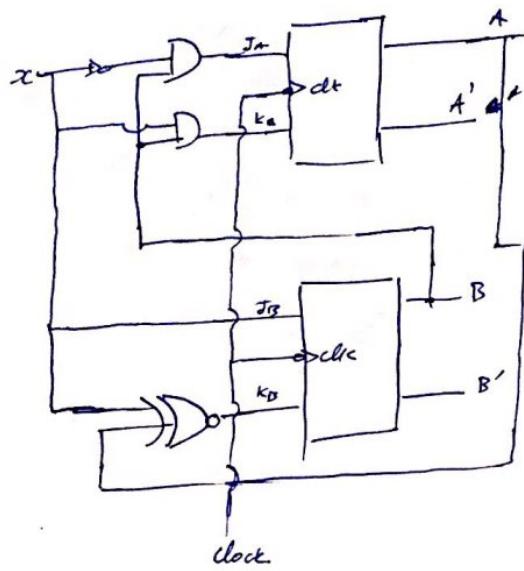
0

1

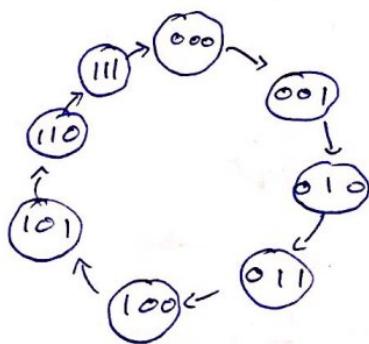
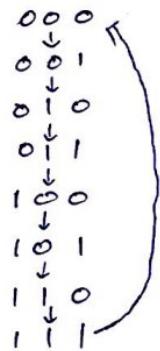
1

1

1



• Synthesis of 3-bit counter using T-flip flop

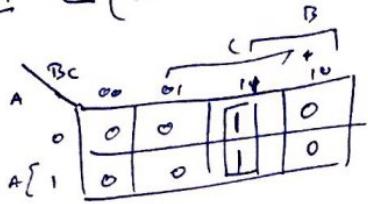


consider A, B, C are three different flip flops.

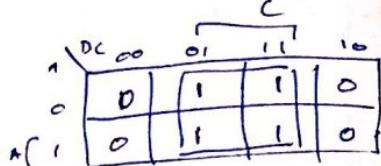
Present State A(t) B(t) C(t)	Next State A(t+1) B(t+1) C(t+1)			T_A	T_B	T_C
	A(t+1)	B(t+1)	C(t+1)			
0 0 0	0 0 1			0	0	1
0 0 1	0 1 0			0	1	1
0 1 0	0 1 1			0	0	1
0 1 1	1 0 0			1	1	1
1 0 0	1 0 1			0	0	1
1 0 1	1 1 0			0	1	1
1 1 0	1 1 1			0	0	1
1 1 1	0 0 0			1	1	1

$$T_B = \sum(1, 3, 5, 7)$$

$$T_A = \sum(3, 7)$$



$$T_A = BC$$



$$T_B = C$$

$$T_C = \sum(0, 1, 2, 3, 4, 5, 6, 7)$$

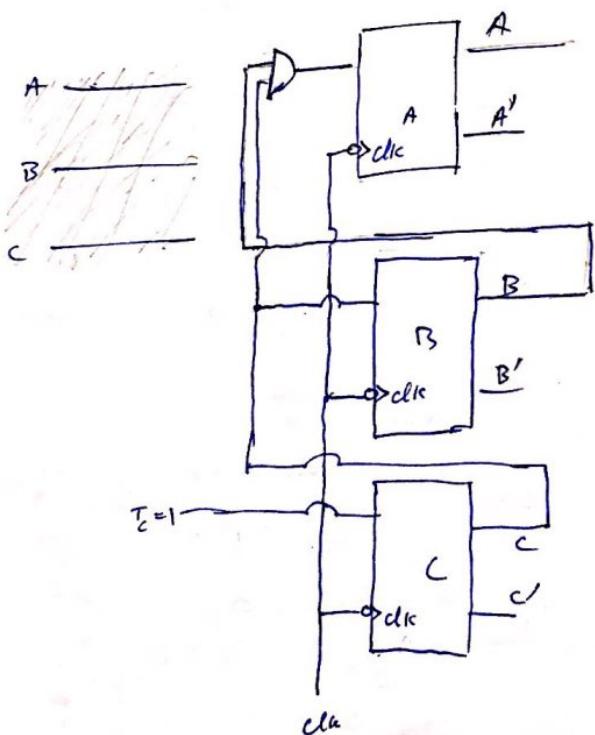
$$T_C = 1$$

\therefore I/P eqns:

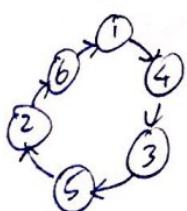
$$T_A = BC$$

$$T_B = C$$

$$T_C = 1$$



Q: Design a counter with arbitrary sequence
1, 4, 3, 5, 2, 6



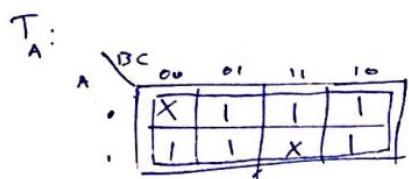
Present	
A(t)	B(t)
0	0
0	0
0	0
1	1
1	1
1	1

T_A:

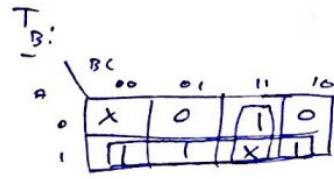
T_C:

T_A = 1

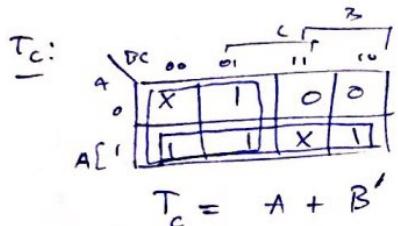
Present State			Next State			T_A	T_B	T_C
$A(t)$	$B(t)$	$C(t)$	$A(t+1)$	$B(t+1)$	$C(t+1)$			
0	0	0	X	X	X	X	X	X
0	0	1	1	0	0	1	0	1
0	1	0	1	1	0	1	0	0
0	1	1	1	0	1	1	1	1
1	0	0	0	1	1	1	1	1
1	0	1	0	1	0	1	1	1
1	1	0	0	0	1	1	1	1
1	1	1	X	X	X	X	X	X



$$T_A = 1$$



$$T_B = BC + A$$

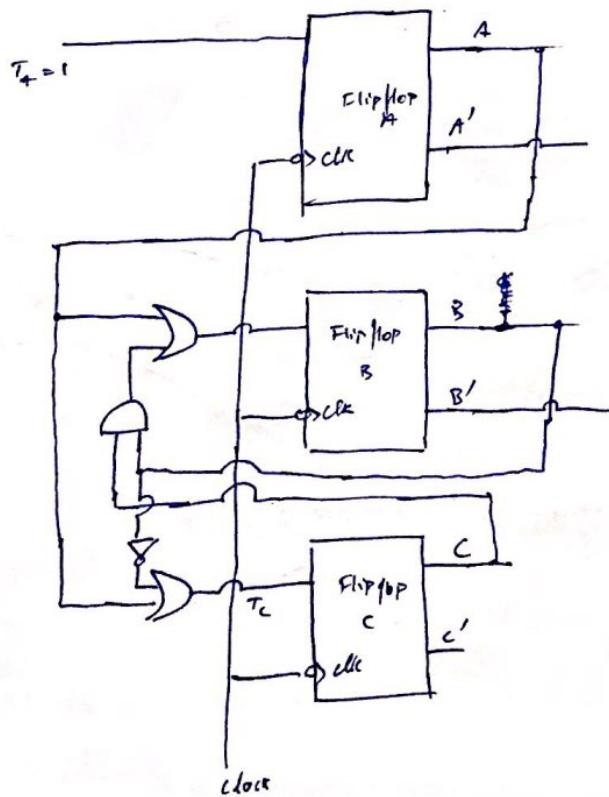


$$T_C = A + B'$$

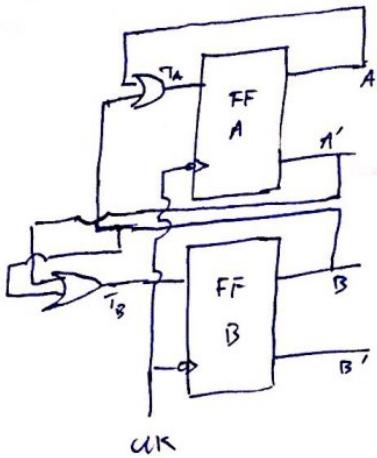
$$T_A = 1$$

$$T_B = BC + A$$

$$T_C = A + B'$$



eg: Find what sequence will this circuit count?



Draw state diagram and state table.
Determine the sequence for this circuit

$$T_A = A + B$$

$$T_B = A' + B$$

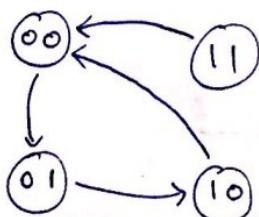
$$\Rightarrow A(t+1) = T_A \oplus A \\ = (A+B) \oplus A$$

$$B(t+1) = T_B \oplus B \\ = (A'+B) \oplus B$$

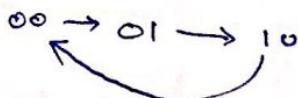
State Table:

Present State:		Next State:		T_A	T_B
$A(t)$	$B(t)$	$A(t+1)$	$B(t+1)$		
0	0	0	1	0	1
0	1	1	0	1	1
1	0	0	0	1	0
1	1	0	0	1	1

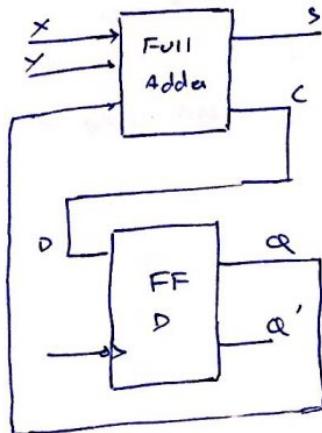
State Diagram:



The sequence is



eg:



Draw state table and state diagram.

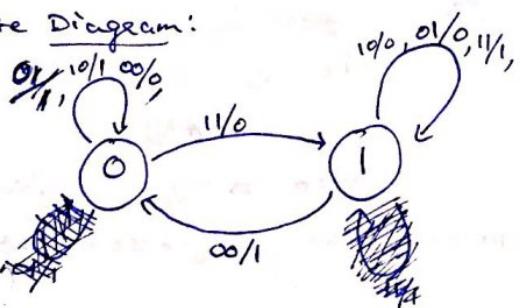
$$T_D = Q(X \oplus Y) + XY$$

$$Q(t+1) = T_D = Q(t)[X \oplus Y] + XY$$

State Table:

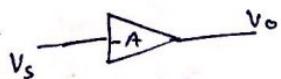
Present State $Q(t)$	Input		Next State $Q(t+1)$	O/P S
	X	Y		
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

State Diagram:



→ Operational Amplifiers: (OPAMP)

- Operational Amplifiers are amplifiers which can perform addition, subtraction, multiplication and division.
- It can have one or 2 i/p.

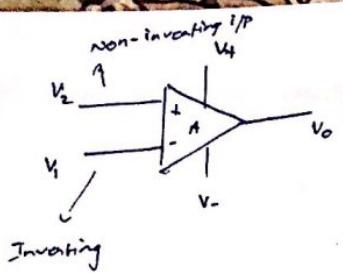


$$\text{In this case } V_o = -AV_s$$

A is called gain.

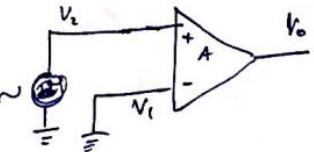
open loop gain A_{OL}

It is called open loop since there is no feedback from o/p to i/p.

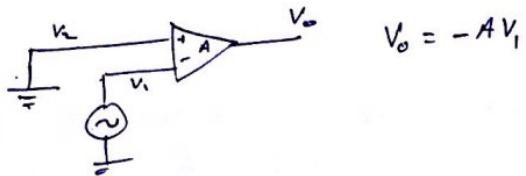


$$V_0 = A(V_2 - V_1)$$

V_+ and V_- are called Supply Voltages.



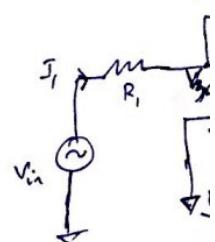
$$V_0 = AV_2$$



$$V_0 = -AV_1$$

In order either for o/p to no

• Inverting



Virtual c

• Ideal OPAMP:

i/p resistance $R_i = \infty$

o/p resistance $R_o = 0$.

Band width $BW = \infty$.

gain $A = \infty$.

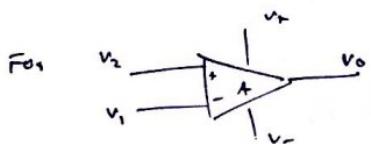
Units:

MΩ

Ω

-

$10^3 - 10^6$

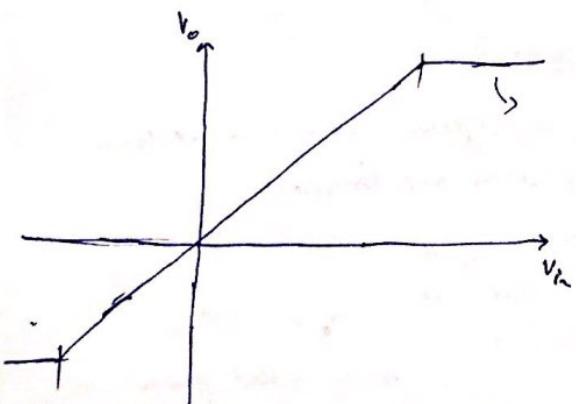


when $V_2 = V_1$

$$\text{i.e. } V_0 = A(V_2 - V_1) \\ = A V_d$$

$$V_d = 0 \Rightarrow V_0 = 0 \text{ (ideally.)}$$

however, we will get some o/p V_0



$$V_0 = AV_{in}$$

$$A = \frac{V_0}{V_{in}}$$

$$\text{consider } A = 10^6$$

$$V_{in} = 1 \text{ mV}$$

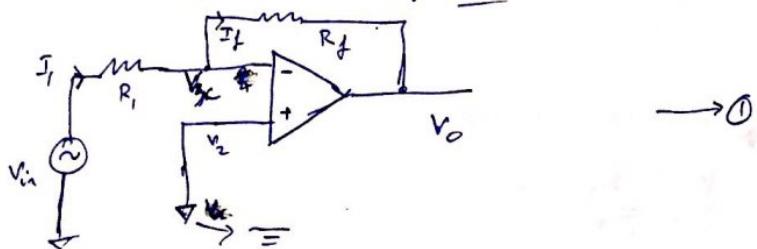
$$\Rightarrow V_0 = 10^3 \text{ V}$$

Practically it is not possible, it cannot exceed the supply voltages'

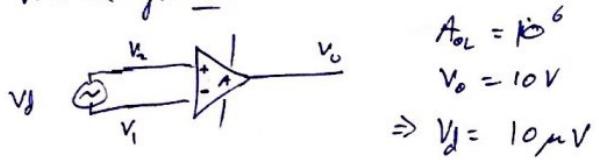
Hence graph doesn't give linear anymore

In order to give it linearly, it can be done in two ways.
either feedback from op to inverting ip or feedback from o/p to non-inverting ip.

- Inverting OPAMP configuration:



Virtual ground:



$$A_{OL} = 10^6$$

$$V_o = 10V$$

$$\Rightarrow V_d = 10\mu V$$

$$V_2 - V_1 = 10\mu V \approx 0$$

$$\Rightarrow V_2 = V_1$$

\therefore ~~From~~ (1) : \rightarrow
By Virtual ground.

$$V_2 = V_1 = V_x =$$

~~but $V_x \neq 0$, $V_x \approx 0$~~

For ideal OPAMP.

$$R_i = \infty$$

$$\Rightarrow I_1 = I_f$$

$$\Rightarrow \frac{V_{in} - V_x}{R_1} = \frac{V_x - V_o}{R_f}$$

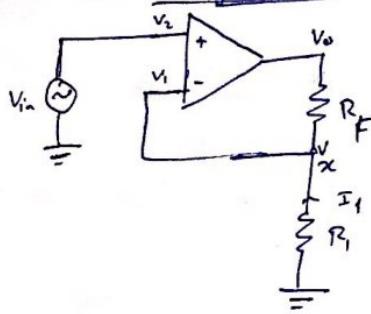
but $V_x = V_2$ (Virtual ground)
and $V_2 = 0$.
 $\therefore V_x = 0$

$$\Rightarrow \frac{V_{in}}{R_1} = -\frac{V_o}{R_f}$$

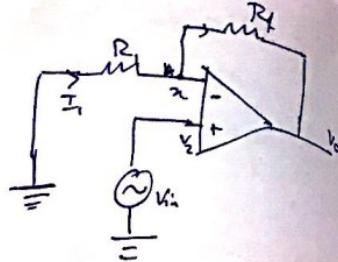
$$\Rightarrow \frac{V_o}{V_{in}} = -\frac{R_f}{R_1} = A_{in}$$

$$\therefore A_{in} = -\frac{R_f}{R_1}$$

• Non-Inverting OP AMP Configuration.



(obtained from)



By Voltage division method;

$$V_x = \frac{R_1}{R_1 + R_F} \cdot V_o$$

$$V_x = V_i = V_2 = V_{in} \quad (\text{virtual ground})$$

$$\Rightarrow V_{in} = \frac{R_1}{R_1 + R_F} V_o$$

$$\Rightarrow \frac{V_o}{V_{in}} = \frac{R_1 + R_F}{R_1} = \left(1 + \frac{R_F}{R_1}\right)$$

$$\Rightarrow \underline{A_{CL} = 1 + \frac{R_F}{R_1}} \quad \text{for non-inverting configuration}$$

Subtractor:
Subtractor

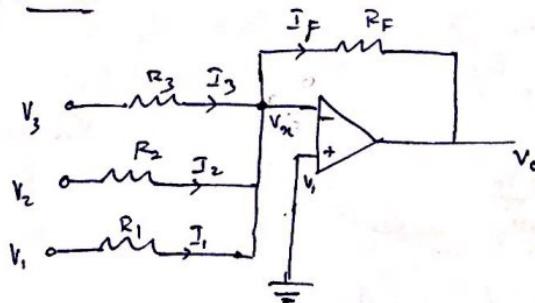
Note:



$$\therefore A_{CL} = 1 + \frac{R_F}{R_1} \quad \text{for non-inverting}$$

$$\underline{A_{CL} = -\frac{R_F}{R_1}} \quad \text{for inverting}$$

Adder:



$$V_i = V_x = 0 \quad (\text{virtual ground})$$

$$\Rightarrow \frac{-V_o}{R_F} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

$$\underline{I_1 + I_2 + I_3 = I_F}$$

$$\Rightarrow \frac{V_1 - V_x}{R_1} + \frac{V_2 - V_x}{R_2} + \frac{V_3 - V_x}{R_3} = \frac{V_x - V_o}{R_F}$$

$$\begin{aligned} I &= \\ \Rightarrow V &= \end{aligned}$$

$$\Rightarrow V_o = -R_F \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

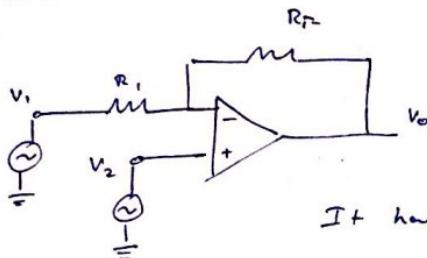
$$= - \left[\frac{R_F}{R_1} V_1 + \frac{R_F}{R_2} V_2 + \frac{R_F}{R_3} V_3 \right]$$

$$\text{If } R_1 = R_2 = R_3 = R_F$$

$$\Rightarrow V_o = - \underline{\underline{(V_1 + V_2 + V_3)}}$$

Subtraction:
Subtraction:

Note:



It has both inverting and Non-inverting configuration

$$\text{i.e. } A_{CL} = -\frac{R_F}{R_1}$$

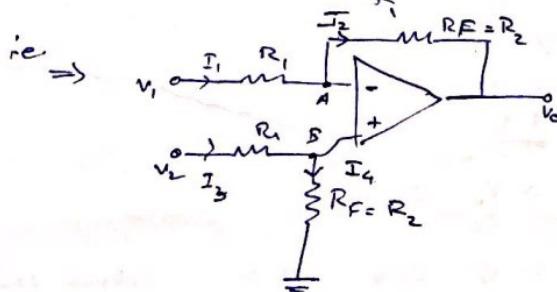
$$A_{CL} = 1 + \frac{R_F}{R_1}$$

$$\Rightarrow \frac{R_F}{R_1} = 1 + \frac{R_F}{R_1} = \frac{R_1 + R_F}{R_1}$$

Multiply ~~both~~ by $\frac{R_F}{R_1 + R_F}$

$$\frac{R_1 + R_F}{R_1} \cdot \frac{R_F}{R_1 + R_F} = \frac{R_F}{R_1}$$

Since they both are on same amplifier, so they have to be equal. For that, we need to make some modification/add to the circuit in order to make it equal



so that

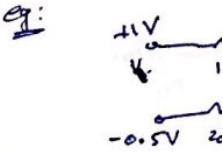
A_{CL} is equal for both configurations

$$I_1 = I_2$$

$$\Rightarrow \frac{V_1 - V}{R_1} = \frac{V - V_o}{R_1 R_2}$$

$$\Rightarrow \frac{V_i - V}{R_1 R_2} = \frac{V}{R_2} - \frac{V_o}{R_2}$$

$$\Rightarrow \frac{V_i}{R_1} = V \left(\frac{1}{R_1} + \frac{1}{R_2} \right) - \frac{V_o}{R_2} \rightarrow ①$$



Also $I_3 = I_4$

$$\Rightarrow \frac{V - V}{R_1} = \frac{V - 0}{R_2} \Rightarrow \frac{V_2}{R_1} - \frac{V}{R_1} = \frac{V}{R_2}$$

$$\Rightarrow \frac{V_2}{R_1} = V \left(\frac{1}{R_1} + \frac{1}{R_2} \right) \rightarrow ②$$

From ① & ②:

$$\Rightarrow \frac{V_i}{R_1} = \frac{V_2}{R_1} - \frac{V_o}{R_2}$$

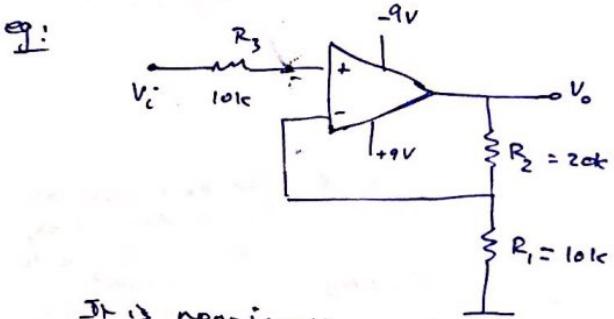
$$\Rightarrow V_o = \underline{\underline{\frac{R_2}{R_1} (V_2 - V_i)}}$$

calcul

$V_A =$

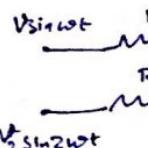
$V_B =$

$V_C =$



Calculate o/p voltage if
 $V_i = 0.5V, 2V$ and
 $4V.$

Q:



It is non-inverting configuration with R_3 which can be neglected (Ref: [non-invert](#))

$$A_{cl} = \frac{V_o}{V_i} = 1 + \frac{R_2}{R_1}$$

$$\Rightarrow V_o = \frac{R_1 + R_2}{R_1} V_{in} = \frac{30k}{10k} V_{in} = 3V_i$$

When $V_i = 0.5V$

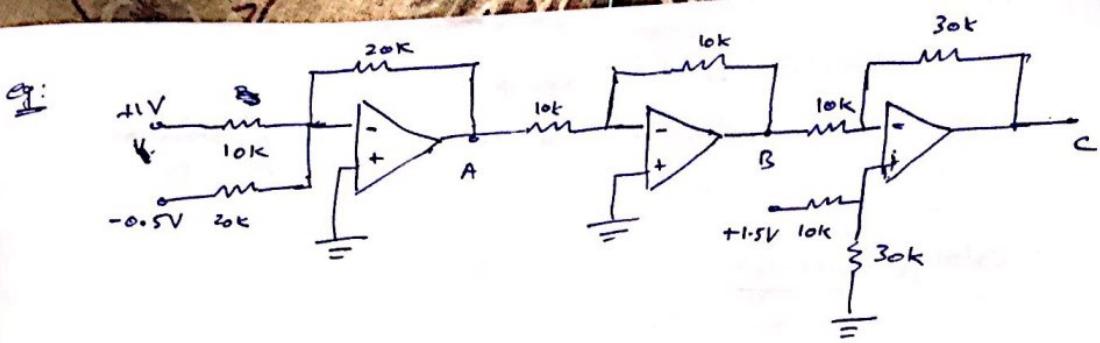
$$V_o = \underline{\underline{1.5V}}$$

$$V_i = 2V \Rightarrow V_o = \underline{\underline{6V}}$$

$V_i = 4V \Rightarrow V_o = 12V$ however, output should not exceed supply voltages
 $\therefore V_o = \underline{\underline{9V}}$ for $V_i = 4V.$

Voltage

V_i
(V)



Calculate the voltages at pts A, B, C.

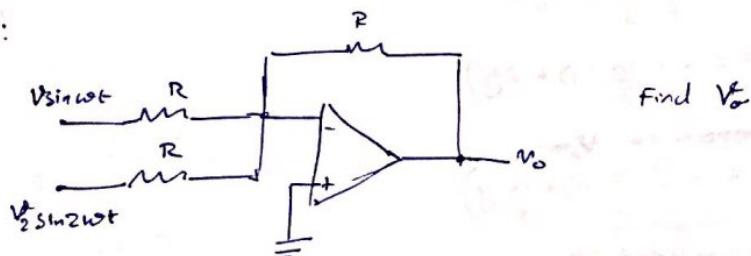
$$V_A = -R_F \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} \right) \quad (\text{Adder configuration})$$

$$= -20k \left(\frac{1}{10k} + \frac{-0.5}{20k} \right) = -\frac{20}{30} \left(2 + -0.5 \right) \\ = -1.5 \text{ V}$$

$$V_B = -\frac{R'_F}{R'_1} \cdot V_A = -\frac{10}{10} \cdot (-1.5) = 1.5 \text{ V} \quad (\text{Inverting configuration})$$

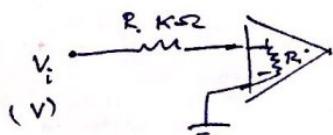
$$V_C = \frac{R''_F}{R''_1} (V_2 - V_B) = \frac{30}{10} (1.5 - 1.5) = 0 \text{ V} \quad (\text{Subtractor configuration})$$

eg:



$$\begin{aligned} V_o &= -(V_{1 \sin \omega t} + V_{2 \sin 2\omega t}) \\ &= -(V \sin \omega t + 2V_2 \sin \omega t \cos \omega t) \\ &= -\underline{\underline{V \sin \omega t}} (V + 2V_2 \cos \omega t) \end{aligned}$$

Voltage inversion



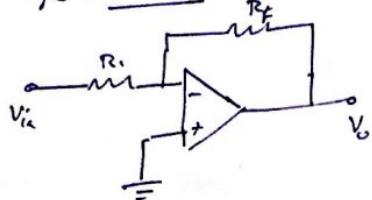
ideally $R_i = \infty$
practically $i_r \gg i_s$ in M-S2

$$\therefore R_{\text{series}} = M\Omega.$$

$$\therefore I = \frac{V}{M\Omega} = mA. \quad \therefore \text{through } K_{S2} \Rightarrow V = mV.$$

which is so low compared to V_i
 \therefore we neglect resistance (like in previous example)

- Voltage Inverter:



$$A_{in} = \frac{V_o}{V_i} = -\frac{R_F}{R_i}$$

When $R_F = R_i$

$$\Rightarrow V_o = -V_i$$

Q: Design an ~~opamp~~ OPAMP which finds the solution of

$$\begin{aligned} 3x + 6y - 10 &= 0 \quad \rightarrow \textcircled{1} \\ 2x - y - 8 &= 0 \quad \rightarrow \textcircled{2} \end{aligned}$$

$$\textcircled{1} \Rightarrow 3x + 6y - 10 = 0$$

$$3x = 10 - 6y$$

$$x = \frac{10}{3} - 2y$$

$$x = -\left(\frac{-10}{3} + 2y\right)$$

$$\Rightarrow x = -\left(\frac{10}{3}(-1) + 2y\right)$$

In correspond to V_o

$$x = -\left(\frac{10}{3}(-1) + \frac{10}{5}y\right)$$

In correspond to

$$V_o = -\left(\frac{R_F}{R_i}V_1 + \frac{R_F}{R_2}V_2\right)$$

$$\Rightarrow R_F = 10k\Omega$$

$$R_i = 3k\Omega$$

$$V_1 = -1V$$

$$R_2 = 5k\Omega$$

$$V_2 = y$$

$$\textcircled{2} \Rightarrow 2x - y - 8 = 0$$

$$y = 2x - 8$$

$$= -(8 + 2(-x))$$

$$y = -\left(\frac{2}{1}(4) + \frac{2}{1}(-x)\right)$$

In correspond to

$$V_o' = -\left(\frac{R'_F}{R'_i}V'_1 + \frac{R'_F}{R'_2}V'_2\right)$$

$$\Rightarrow R'_F = 2k\Omega$$

$$R'_i = R'_2 = 1k\Omega$$

$$V'_1 = 4V$$

$$V'_2 = -x$$

