HIGH PERFORMANCE CIRCUIT DESIGN

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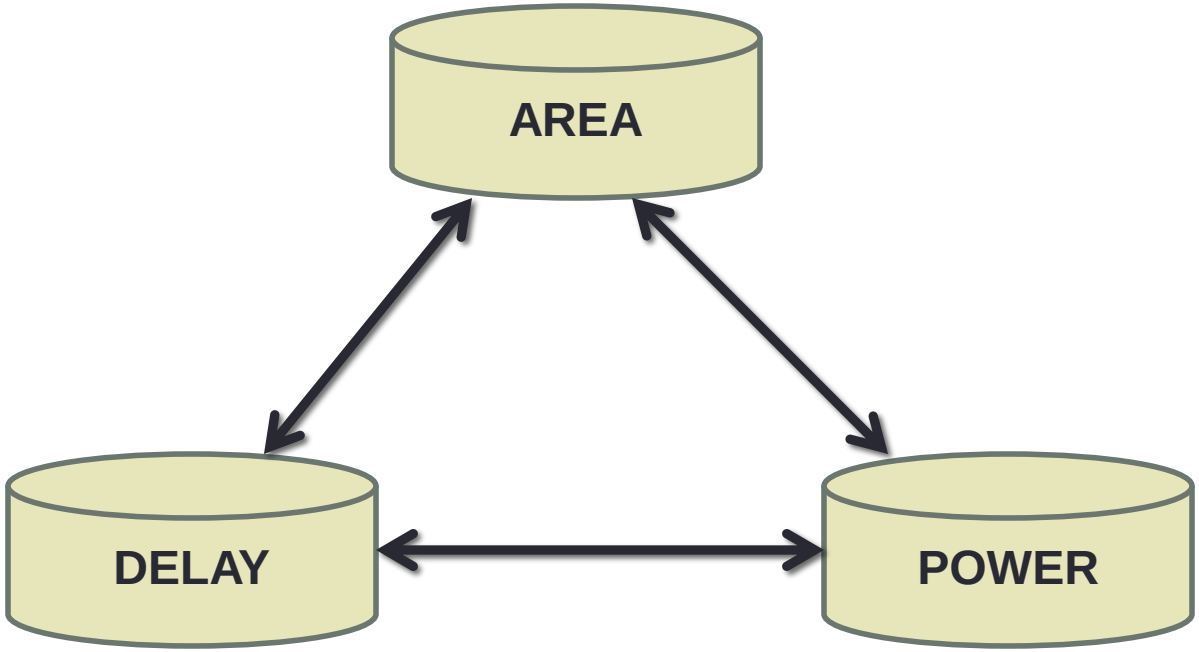
Hprcse

High Performance Circuit Design



Delay Optimization

- Parallel processing
- Control and data path separation
- Pipelining

Parallel Processing

R(i)=A(i)*B(i);
i is varied from 0 to 99

Conventional processing
Time taken = Tc

R(i)=A(i)*B(i);
i is varied
from 0 to 25

R(i)=A(i)*B(i);
i is varied
from 25 to 49

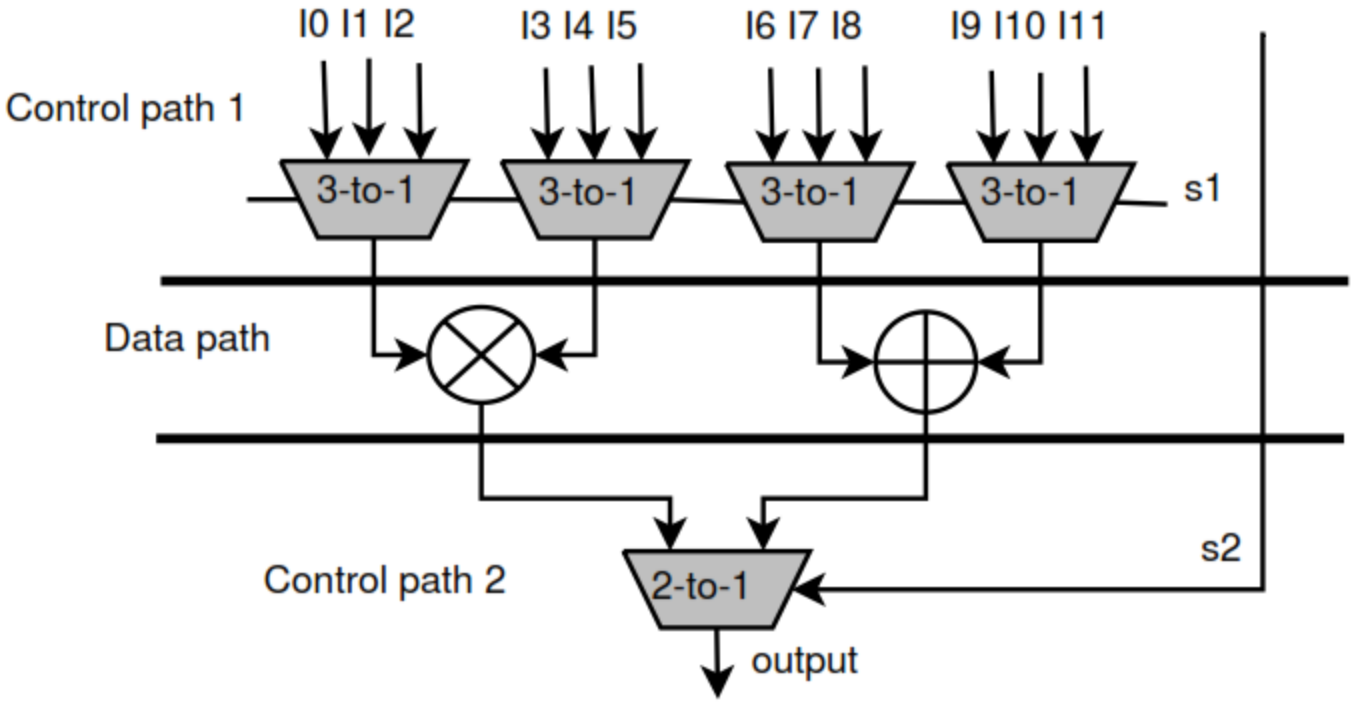
R(i)=A(i)*B(i);
i is varied
from 50 to 74

R(i)=A(i)*B(i);
i is varied
from 75 to 99

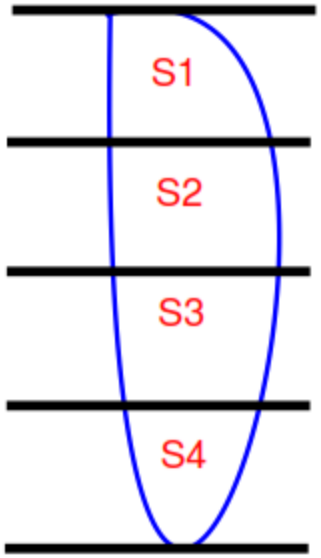
Parallel processing Time taken = Tc/4

Control and Data Path Separation

- Data path - Collection of functional units (arithmetic/ logical)
- Control path - It commands the data path and memory according to the instructions



Pipelining



Clock	1	2	3	4	5	6	7
Task1	S1	S2	S3	S4			
Task2		S1	S2	S3	S4		
Task3			S1	S2	S3	S4	
Task4				S1	S2	S3	S4

Total time = $(K + n - 1)T_c$

K= No. of segments

n= No. of tasks

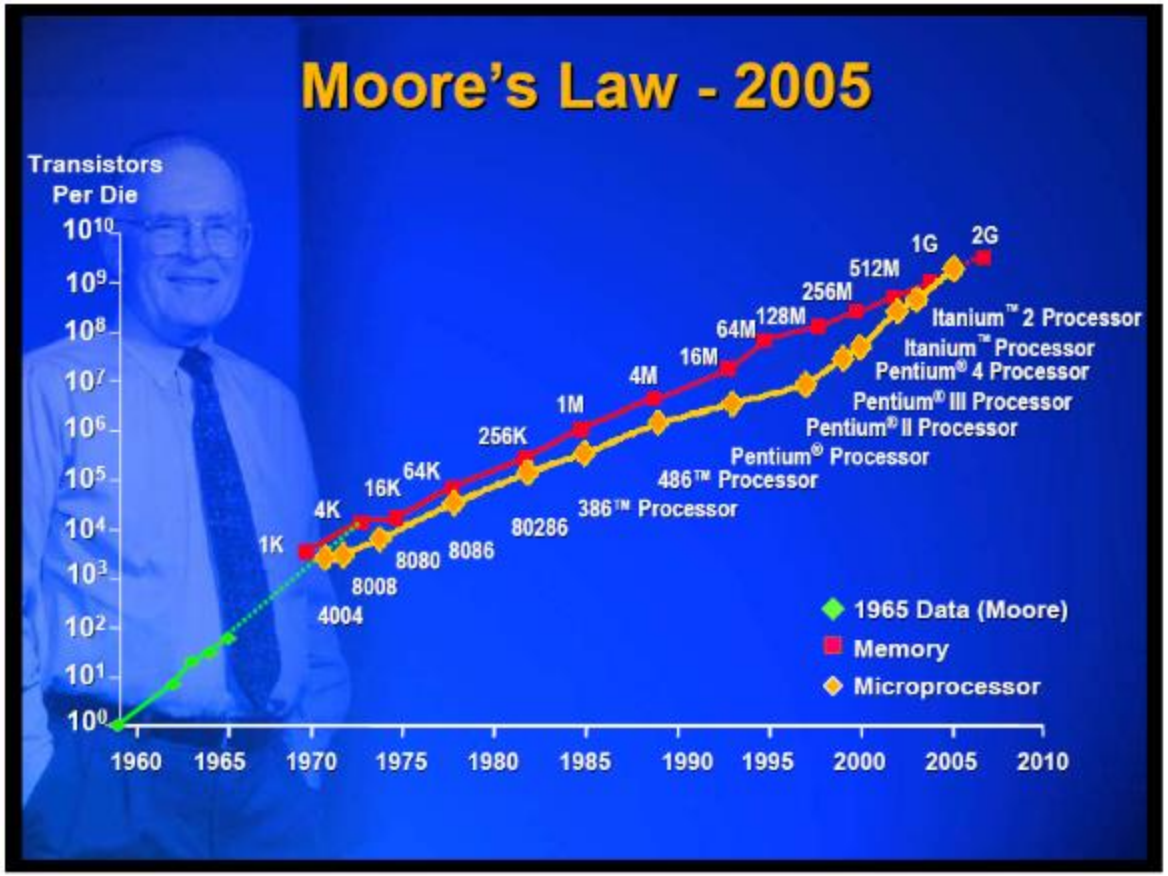
T_c = Clock period

Area optimization

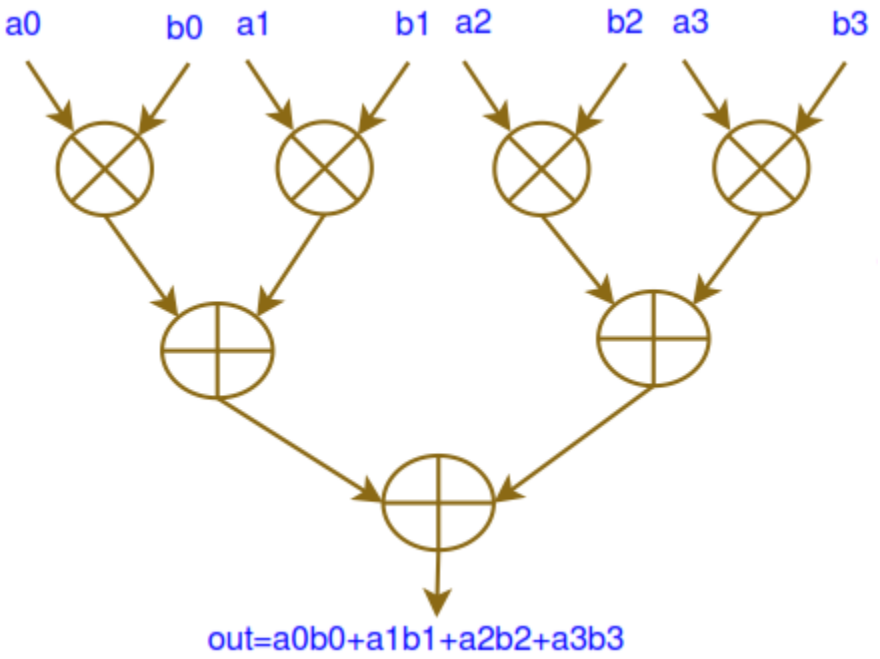
- Hardware reuse

Moore's law

- The number of transistors in a integrated circuit doubles approximately every two years

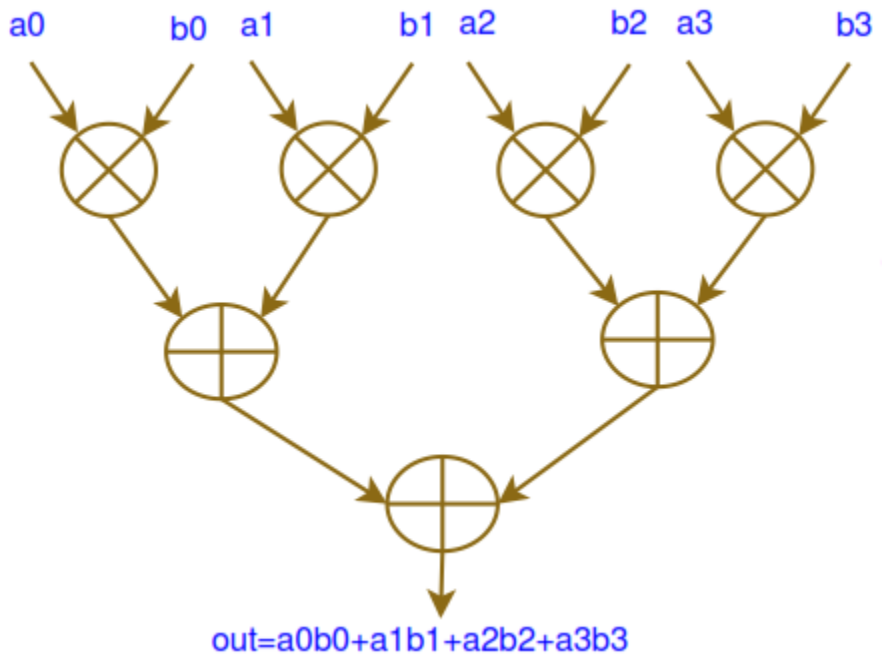


Hardware Reuse



Conventional design
No. of multipliers - 4
No. of adders - 3
No. of cycles - 1

Hardware Reuse



Conventional design
No. of multipliers - 4
No. of adders - 3
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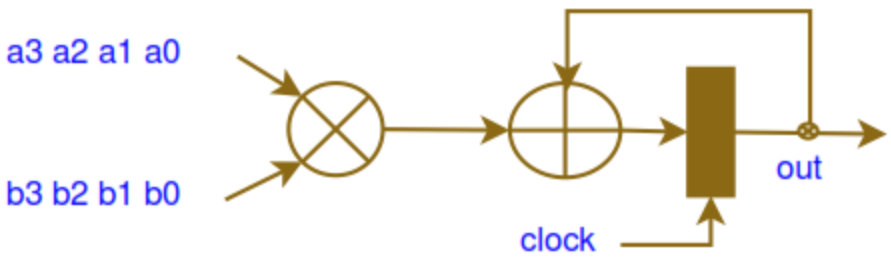


Hardware reuse design
No. of multipliers - 1
No. of adders - 1
No. of cycles - 4

Hprcse

Power optimization

- Dynamic Power

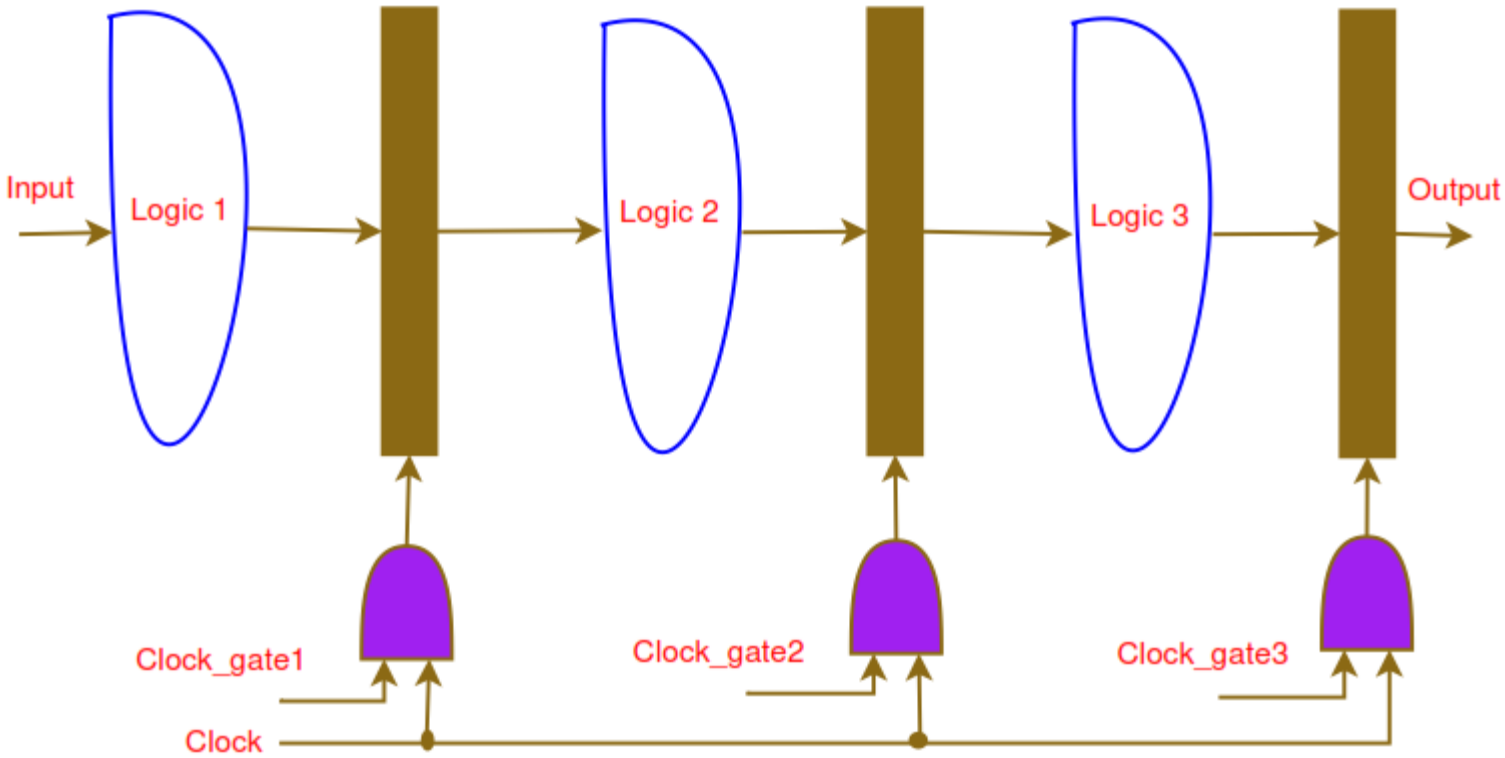
$$P_{\text{switching}} = \alpha C V_{DD}{}^{2} f$$

Try to minimize:

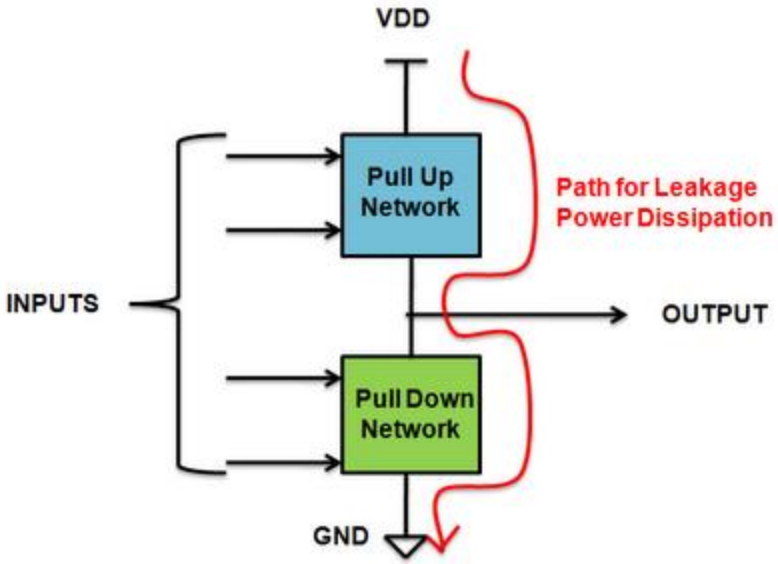
- Activity factor
- Capacitance
- Supply voltage
- Frequency

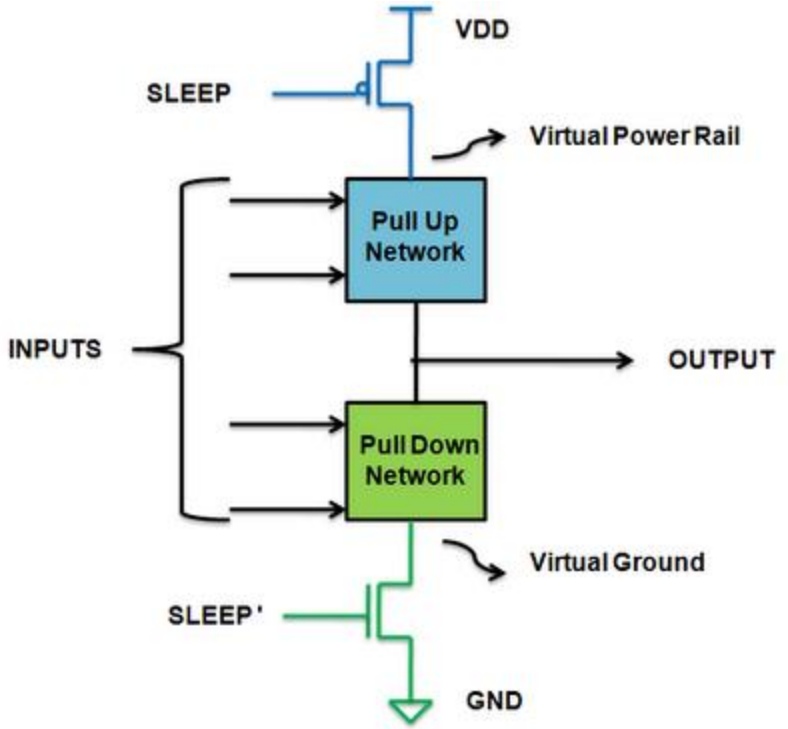
- Clock gating

Clock Gating



Power Gating





- SLEEP=0 Normal Operation
- SLEEP=1 Low Power, PMOS and NMOS are OFF, No Leakage Power