Indian Institute of Information Technology Design and Manufacturing (IIITDM) Kancheepuram Chennai - 600 127

COM304 Computer Architecture - End Semester (Open Book) Exam

Date: 2 July 2020 Duration: 3 hours Max. Marks: 40

- *Answers the ALL the following questions* $[5 \times 8Marks = 40Marks]$
- *Write on the White or ruled Paper.*
- *Usage of laptops and other electronics materials are allowed.*
- *Discussions among the students is NOT allowed.*
- *Student and His/her parent/gaurdian has to endorse each and every page of the answersheet. Followed the rules of online examination.*

1. A spacecraft design company gave the following specifications to the processor design company.

   - The processor has to perform all integer, floating-point, logical, and shift operations.
   - All the basic I/O processing has to be on the processor chip. Only IO pins should be available externally.
   - The I/O pins that are available on the processor chip will directly drive the devices that are connected to it.
   - The main objective of this processor is for control and management purposes.
   - All the development related to hardware and software should be on the single-chip only.

   (a) You are requested to architect the processor, memory, storage on single chip.
   (b) Ensure the proposed architecture will give higher throughput.
   (c) Compare your design with respect to the superscalar processor in terms of speed of execution, cost, and throughput.
   (d) Among these two (Proposed and Super-scalar) architectures which will give higher performance? Justify?
   (e) How do you maintain the operating system and application programs on the single-chip?
   (f) Specify the type of memory that you are going to use to store the OS and Application programs? Justify?
   (g) How do you organize the cache memory? Justify?

2. A processor design company has explored the following options of the storage interface to the processor?

   (a) Storage implemented as flash memory. The Flash memory device is directly connected to the processor.
   (b) Processor with the on-chip cache memory and then connected to flash memory device as storage.
   (c) Processor with on-chip cache and off-chip cache of flash memory type and then connected to flash memory device as storage.
   (d) Processor with on-chip L1 cache contains Data and Instruction cache, and followed by L2 Cache and flash memory device as storage.
   (e) Processor with on-chip L1 and L2 Caches contains Data and Instruction Caches and followed by flash memory devices as storage.

Provide your analysis on each of the above in terms of per-bit cost, speed of execution. Which one will perform better among all, justify your answer? You can propose a better memory hierarchy, which will give better performance than above. Justify your answers?

3. A processor design company has opted for the following two architectures for their processor design.

   - **TYPE A**: A processor with integer, floating-point, and load-store units in parallel. The processor is designed using out-of-order execution, where each functional unit executes in parallel and independently. The processor uses statistical and dynamic instruction scheduling.
   - **TYPE B**: A processor with integer, floating-point, and load-store units in parallel. The processor is designed with VLIW architecture, where each functional unit executes in parallel and independently. The processor uses the statistical and assumes that it supports even dynamic instruction scheduling.

   (a) The functional units that are used in both the processor will have the same number of pipeline stages. Then which will have a higher speed. Justify your answer?

   (b) What are the limitations of Type A and Type B? Justify?

   (c) Discuss your view about multiple thread support?

   (d) State the best-suited applications for each processor type that will give higher performance? Justify?

   (e) Provide your analysis about opting for multiple cores on each chip for type A and type B separately. State the limitations and how to overcome the limitations.

4. (a) How do you overcome the register spill problem in the hardware? Propose your hardware solution and justify your answer?

   (b) One of the major limitations to ILP is Register renaming. Propose your architectural solution and justify your answer?

   (c) A processor manufacturing company has designed Processor A with super-scalar out-of-order execution single core on a chip, Processor B with four cores on-chip. What is the operating speed of Processor A and Processor B. What is the performance difference between each other. What are the modifications that you recommend such a way that processor B will perform 4 times better than processor B?

   (d) A processor design company had tied up with one of semiconductor manufacturing for five years. Initially, whatever the design that the processor design company gives it used to manufacture without any fault. The processor design company typically manufactures a superscalar processor with out-of-order execution. After 2 years the manufacturing company has reported to a processor design company, that they can not manufacture the integer multiplication unit in the superscalar processor successfully, but they can able manufacture other processor elements (adders, SDRAM cell, load, and store, etc.,) successfully. Now breaking contact with manufacturing companies and executing contact with other manufacturing units may cause a huge loss to the processor design company. What is the architectural change that you propose to overcome to this issue and to continue the contract with the old manufacturing company?

5. (a) Propose the architectural changes to support simultaneous multi-threading efficiently for out-of-order execution processor.

   (b) How one can go for multiple instruction issue and multiple commits on top it.

   (c) How multi-core architecture will support thread-based execution efficiently.

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