INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, DESIGN AND MANUFACTURING, KANCHEEPURAM

Course **:** VLSI Design Practice

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AIM:

Implementation of Universal Shift Register performing SISO, PIPO, SIPO, PISO using Verilog.

INTRODUCTION TO SHIFT REGISTERS:

Shift Registers are sequential logic circuits, capable of storage and transfer of data. They are made up of Flip Flops which are connected in such a way that the output of one flip flop could serve as the input of the other flip-flop, depending on the type of shift registers being created.

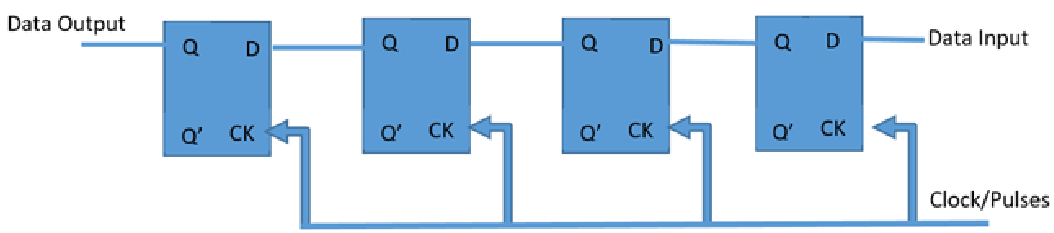


Fig.1 shows the basic shift register made out of flipflops

Shift registers are basically a type of register which have the ability to transfer ("shift") data.

Registers are generically storage devices which are created by connecting a specific number of flip flops together in series and the amount of data (number of bits) which can be stored by the register is always directly proportional to the number of flip flops, as each flip flop is capable of storing only one bit at a time.

When the flip-flops in a register are connected in such a way that the output of one flip flop, becomes the input of the other, a shift register is created.

DIFFERENT TYPES OF SHIFT REGISTERS:

Shift registers are categorized into types majorly by their mode of operation, either serial or parallel. There are six (6) basic types of shift registers which are listed below although some of them can be further divided based on direction of data flow either shift right or shift left.

1. Serial in – Serial out Shift Register (SISO)
2. Serial In – Parallel out shift Register (SIPO)
3. Parallel in – Parallel out Shift Register (PIPO)
4. Parallel in – Serial out Shift Register (PISO)
5. Bidirectional Shift Registers
6. Counters

Serial In - Serial Out Shift Register (SISO):

Serial in – Serial out shift registers are shift registers that streams in data serially (one bit per clock cycle) and streams out data too in the same way, one after the other.

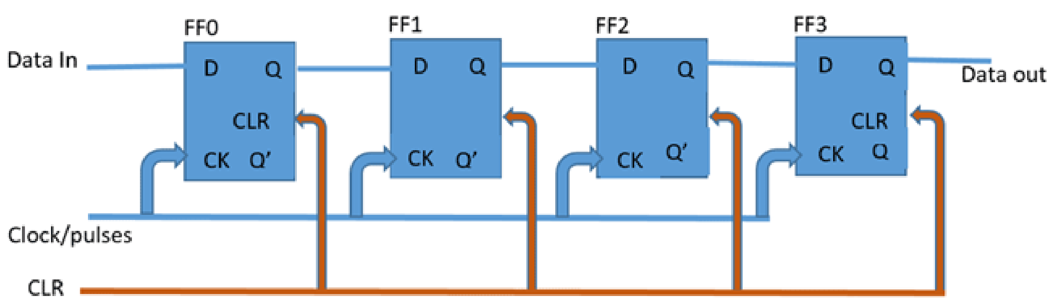


Fig.2 Serial In – Serial Out (SISO) 4 – Bit shift register

As shown in Fig.2, the register consists of 4 flip flops and the breakdown of how it works is explained. On startup, the shift register is first cleared, forcing the outputs of all flip flops to zero, the input data is then applied to the input serially, one bit at a time.

Serial In – Parallel Out Shift Register (SIPO):

The second type of shift register we will be considering is the Serial in – Parallel out shift register. These types of shift registers are used for the conversion of data from serial to parallel. The data comes in one after the other per clock cycle and can either be shifted and replaced or be read off at each output. This means when the data is read in, each read in bit becomes available simultaneously on their respective output line (Q0 – Q3 for the 4-bit shift register shown below).

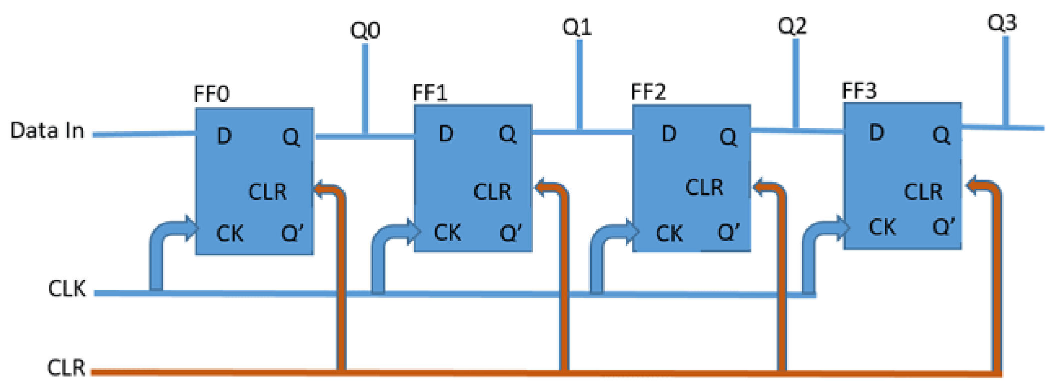


Fig.3 4 – Bit Serial In – Parallel Out (SIPO) shift register

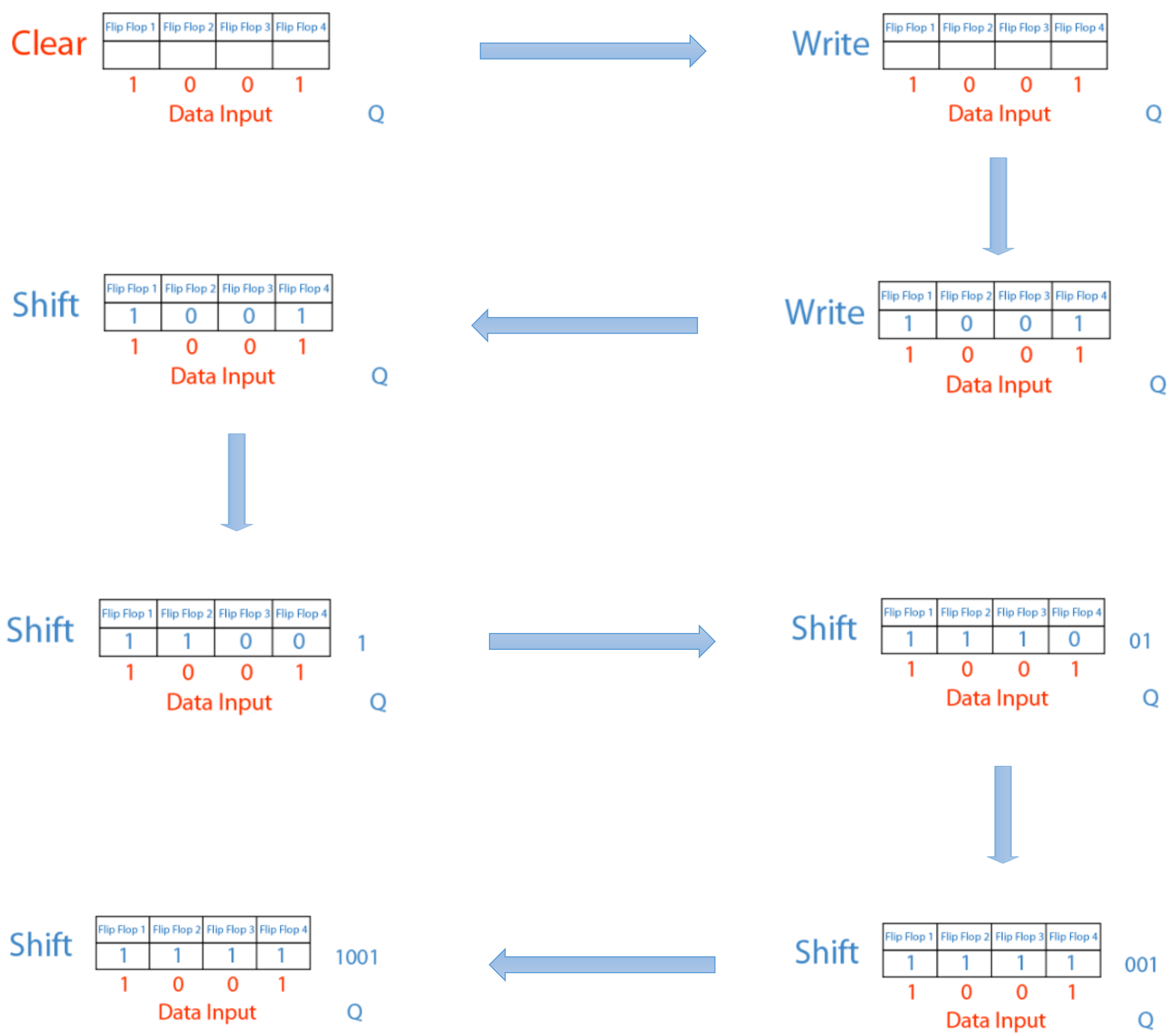
Table 1: A table showing how data gets shifted out of Serial In – Parallel Out 4 – bit shift register, with the Data In as 1001.

Clear	FF0	FF1	FF2	FF3
1001	0	0	0	0
	1	0	0	0
	0	1	0	0
	0	0	1	0
	1	0	0	1

Parallel In – Serial Out Shift Register (PISO):

This configuration has the data input on lines D1 through D4 in parallel format, D1 being the most significant bit. To write the data to the register, the Write/Shift control line must be held LOW. To shift the data, the W/S control line is brought HIGH and the registers are clocked. The arrangement now acts as a PISO shift register, with D1 as the Data Input. However, as long as the number of clock cycles is not more than the length of the data-string, the Data Output, Q, will be the parallel data read off in order.

Fig.4 The following diagrams shows the operation of PISO:



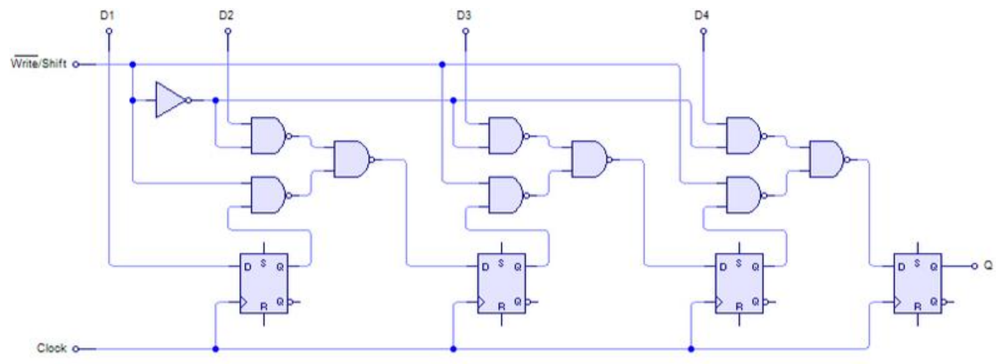


Fig.5 4 – Bit Parallel In – Serial Out (PISO) shift register

Parallel In – Parallel Out Shift Register (PIPO):

For parallel in – parallel out shift register, the output data across the parallel outputs appear simultaneously as the input data is fed in.

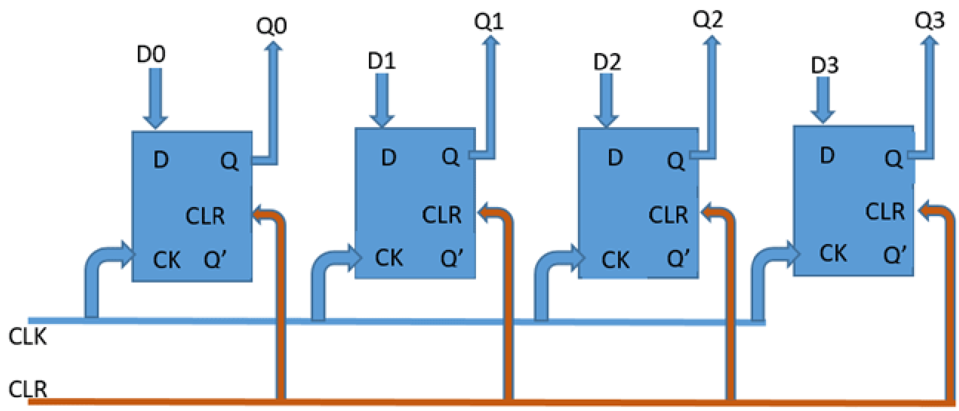


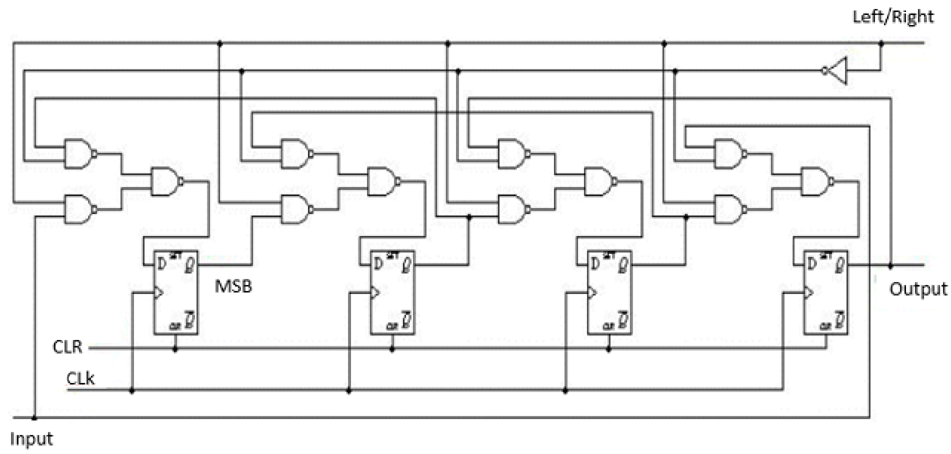
Fig.6 4 – Bit Parallel In – Parallel Out (PIPO) shift register

The input data at each of the input pins from D0 to D3 are read in at the same time when the device is clocked and at the same time, the data read in from each of the inputs is passed out at the corresponding output (from Q0 to Q3).

Bidirectional Shift Registers:

Shift registers could either perform right or left data shift, or both depending on the kind of shift register and their configuration. In right shift operations, the binary data is divided by two. If this operation is reversed, the binary data gets multiplied by two. With suitable application of combinational logic, a serial shift register can be configured to perform both operations.

Fig.7 4 – Bit Bi – Directional shift register

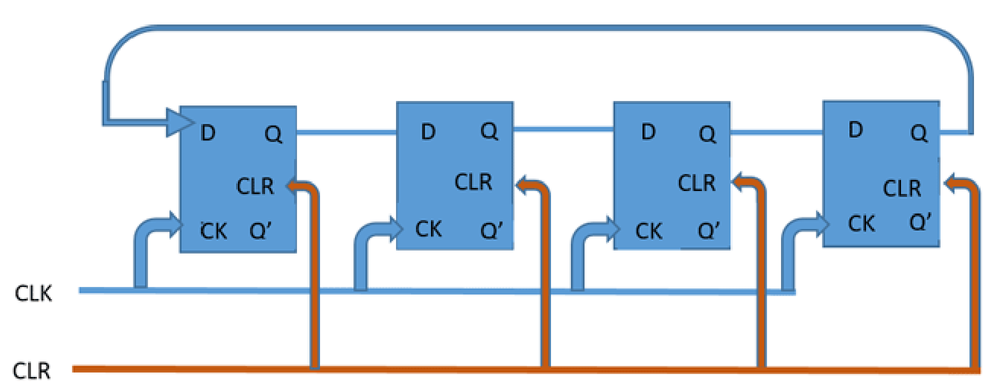


Counters:

Counters, sometimes called rotate shift register are basically shift registers with their outputs fed back into the device as inputs in such a way that it creates a particular pattern. These kinds of registers are referred to as counters because of the pattern and sequence they exhibit.

This most popular type of shift register counters are the Ring Counters.
Ring counters are basically a type of counter in which the output of the most significant bit is fed back as an input to the least significant bit.

Fig.8 4 – Bit Ring Counter



BASIC WAYS OF SHIFTING DATA:

There are two basic ways of shifting data out through a shift register:

- Destructive Readout
- Non-destructive Readout

Destructive Readout:

For destructive readouts, the data is completely lost as the flip flop just shifts the information through. Assuming for the 4-bit shift register above, we want to send the word “1101”. After clearing the shift register, the output of all the flip flops becomes 0, so during the first clock cycle as we apply this data (1101) serially, the outputs of the flip flops look like the table below.

First clock cycle:

FF0	FF1	FF2	FF3
1	0	0	0

Second clock cycle:

FF0	FF1	FF2	FF3
0	1	0	0

Third Clock Cycle:

FF0	FF1	FF2	FF3
1	0	1	0

Fourth Clock Cycle:

FF0	FF1	FF2	FF3
1	1	0	1

Non – Destructive Readout:

Non - Destructive readout based, shift registers always have a read/write mode of operation with an extra line added to allow the switch between the read and write operational modes.

When the device is in the "write" operational mode, the shift register shifts each data out one bit at a time behaving exactly like the destructive readout version and data is thus lost, but when the operational mode is switched to "read", data which are shifted out at the input goes back into the system and serve as input to the shift register. This helps ensure that the data stays longer (as long as it stays in read mode).

APPLICATIONS OF SHIFT REGISTERS:

Registers are used in digital electronic devices like computers as

- Temporary data storage
- Data transfer
- Data manipulation
- As counters.

Shift registers are used in computers as memory elements. All the digital systems need to store large amount of data, in an efficient manner; there we use storage elements like RAM and other type of registers.

Many of the digital system operations like divisions, multiplications are performed by using registers. The data is transferred through serial shift registers and other type.

Counters are used as Digital clocks, Frequency counters, Binary counters etc.

- Serial In – Serial Out (SISO) registers are used for time delays.
- Serial In – Parallel Out (SIPO) registers are used for converting the data from serial form to parallel form. So, these are also called **"***Serial to Parallel converters***".**
- Parallel In – Serial Out (PISO) registers are used for converting the data from parallel form to serial form. So, these are also called **"***Parallel to Serial converters***".**

INTRODUCTION TO UNIVERSAL SHIFT REGISTER:

Universal Shift Register is a register which can be configured to load and/or retrieve the data in any mode (either serial or parallel) by shifting it either towards right or towards left. In other words, a combined design of unidirectional (either right- or left-shift of data bits as in case of SISO, SIPO, PISO, PIPO) and bidirectional shift register along with parallel load provision is referred to as universal shift register.

It means that, the universal shift register can store the data in parallel and can transmit the data in parallel. In the same manner the data can stored and transmitted by serial path through shift left and shift right operations.
Simply, the universal shift register will load the data either in serial/parallel and will produce output as we require i.e. either in serial/parallel. It is called Universal Shift Register as it can be used for left shift, right shift, serial to serial, serial to parallel, parallel to serial and parallel to parallel operations.

CONSTRUCTION OF UNIVERSAL SHIFT REGISTER:

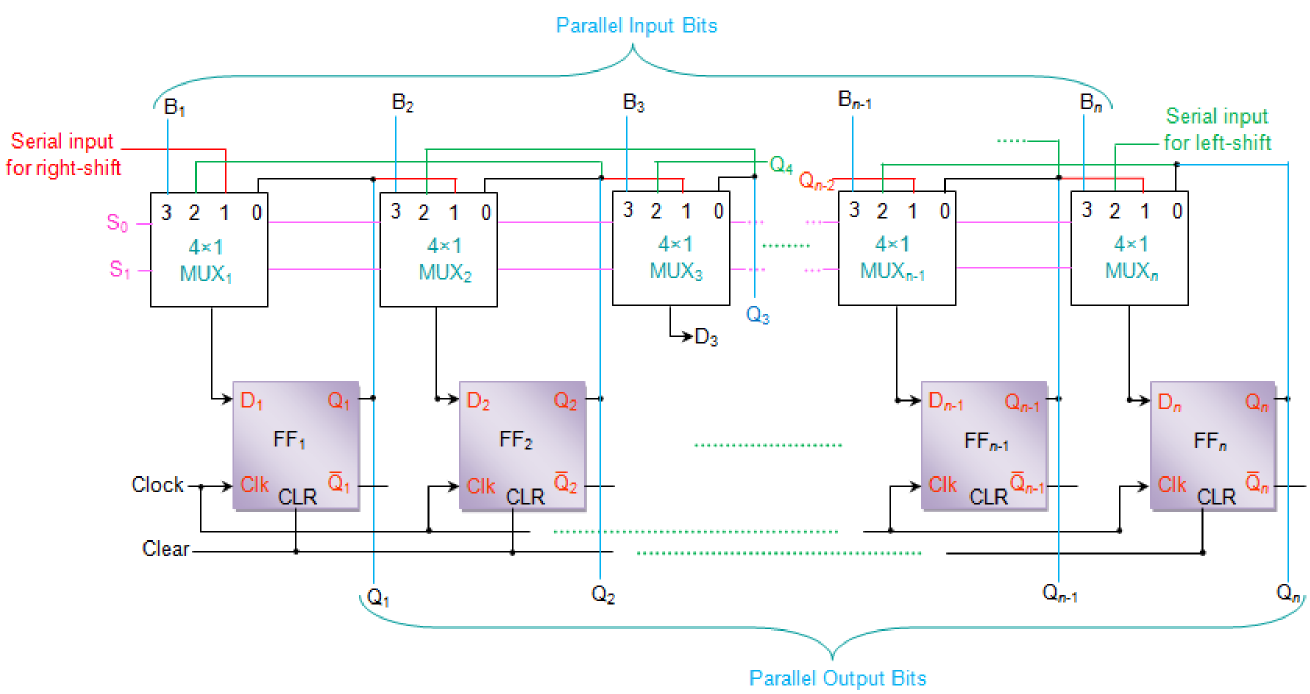


Fig.9 n – Bit Universal Shift Register

OPERATION AND WORKING OF USR:

The design shown by Figure uses n - 4×1 multiplexer to drive the input pins of n flip-flops in the register which are also connected to clock and clear inputs. All of the multiplexers in the circuit share the same select lines, S1 and S0 (pink lines in the figure), in order to select the mode in which the shift registers operate. It is also seen that the MUX driving a particular flip-flop has its

First input (Pin Number 0) connected to the output pin of the same flip-flop i.e. zeroth pin of MUX1 is connected to Q1, zeroth pin of MUX2 is connected to Q2, … zeroth pin of MUXn is connected to Qn.

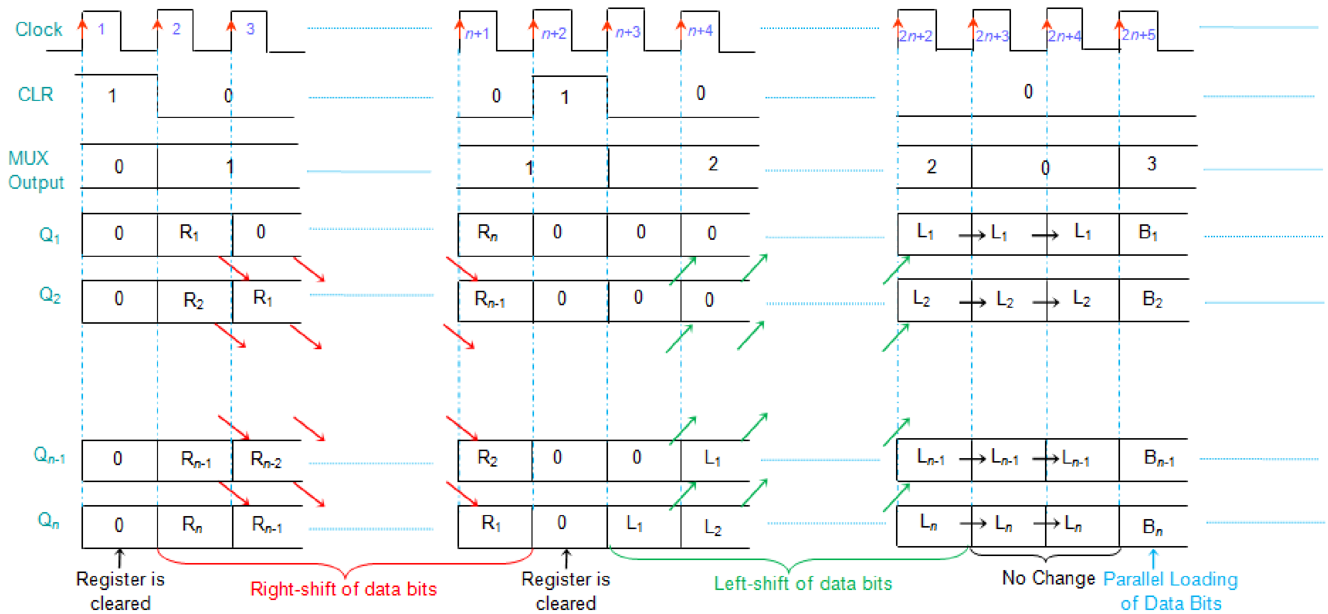
Second input (Pin Number 1) connected to the output of the very-previous flip-flop (except the first flip-flop FF1 where it acts like a serial-input to the input data bits which are to be shifted towards right) i.e. first pin of MUX2 is connected to Q1, first pin of MUX3 is connected to Q2, … first pin of MUXn is connected to Qn-1.

Third input (Pin Number 2) connected to the output of the very-next flip-flop (except the first flip-flop FFn where it acts like a serial-input to the input data bits which are to be shifted towards left) i.e. second pin of MUX1 is connected to Q2, second pin of MUX2 is connected to Q3… second pin of MUXn-1 is connected to Qn.

Fourth input (Pin Number 3) connected to the individual bits of the input data word which is to be stored into the register, thus providing the facility for parallel loading.

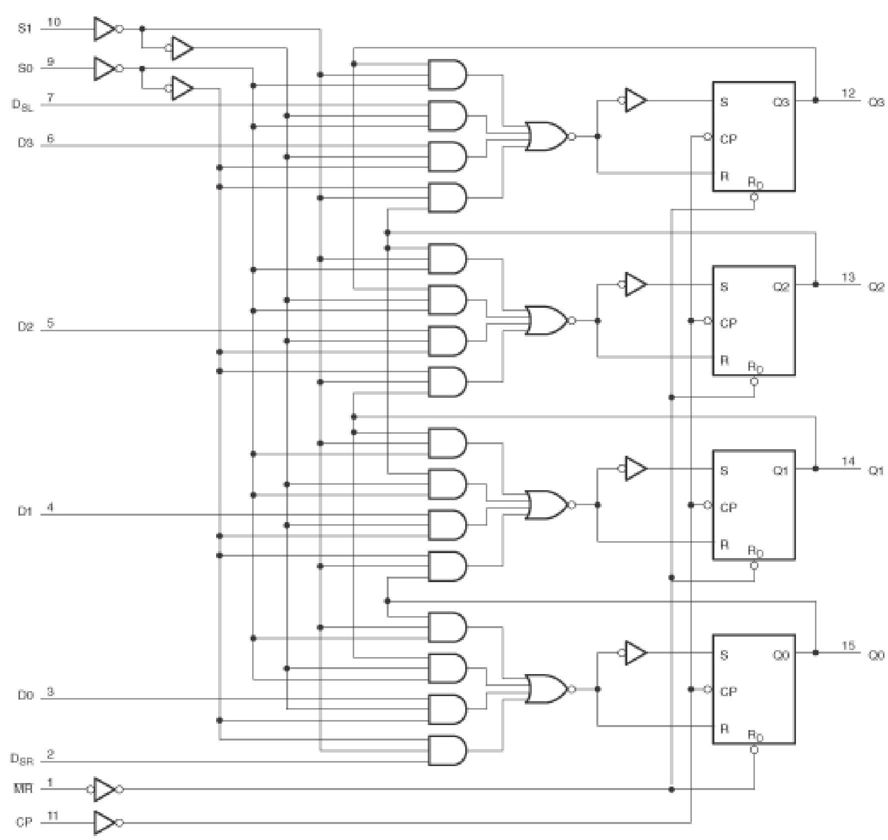
Table 2: The working of this shift register is explained by the Table and the Fig.10 wave forms are given by respectively.

Select Lines		Functionality
S_0	S_1	
0	0	No change for any number of clock cycles as the outputs of the flip-flops are back-fed to themselves
0	1	Data bits within the register shift right for each clock tick with the serial input bits being provided at D_1 via MUX_1
1	0	Data bits within the register shift left for each clock tick with the serial input bits being provided at D_n via MUX_n
1	1	Bits of the data word to be stored are fed in parallel format through Pin Number 3 of each MUX at the rising edge of the clock



CIRCUIT IMPLEMENTATION:

Fig.11 4 – Bit Bi – Directional Universal Shift Register



REFERENCES:

1. https://en.wikipedia.org/wiki/Shift_register
2. https://www.electronicshub.org/shift-registers/
3. https://circuitdigest.com/tutorial/what-is-shift-register-types-applications
4. https://www.allaboutcircuits.com/textbook/digital/chpt-12/introduction-to-shift-registers/
5. https://www.electrical4u.com/universal-shift-registers/