1916/AD485

Assignment   3-ECE-2   ①

1. Define microprocessor.

A clock driven electronic integrated circuit processes the data based on the instructions called a microprocessor.
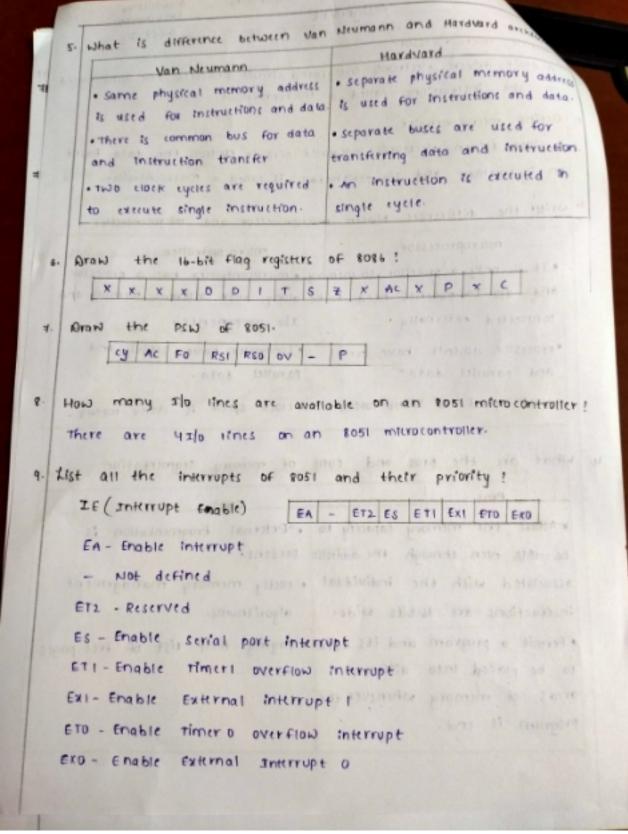
2. Define microcontroller.

A clock driven electronic integrated circuit controls the data based on instructions and I/o peripherals is called a microcontroller.

3. Write the differences b/ween microprocessor and microcontroller

microprocessor	microcontroller
• It is only a processor. So memory and I/o components need to be connected externally.	• microcontroller has a processor along with internal memory and I/o components.
• processor doesn't have serial and parallel data.	• controller have serial and parallel data.
• clock speed is 5MHz - 10MHz.	• clock speed is 1MHZ - 10MHZ.

4. What are the pros and cons of memory segmentation

Pros	Cons
• Allow the memory capacity to be 1MB even through the address associated with the individual instructions are 16-bits wide.	• External fragmentation is present.
	• costly memory management algorithms.
• Permit a program and its data to be placed into different areas of memory whenever the program is end.	• paging keep list of free pages.

5. What is difference between Van Neumann and Hardvard archi...

Van Neumann	Hardvard
• Same physical memory address is used for instructions and data	• Separate physical memory address is used for instructions and data.
• There is common bus for data and instruction transfer	• Separate buses are used for transferring data and instruction.
• Two clock cycles are required to execute single instruction.	• An instruction is executed in single cycle.

6. Draw the 16-bit flag registers of 8086 !

x	x	x	x	O	D	I	T	S	Z	x	AC	x	P	x	C

7. Draw the PSW of 8051.

cy	AC	F0	RS1	RS0	OV	-	P

8. How many I/o lines are available on an 8051 microcontroller !

There are 4 I/o lines on an 8051 microcontroller.

9. List all the interrupts of 8051 and their priority !

IE (Interrupt Enable)

EA	-	ET2	ES	ET1	EX1	ET0	EX0

EA - Enable interrupt

- - Not defined

ET2 - Reserved

ES - Enable serial port interrupt

ET1 - Enable Timer1 overflow interrupt

EX1 - Enable External interrupt 1

ET0 - Enable Timer0 overflow interrupt

EX0 - Enable External Interrupt 0

IP (Interrupt priority):

—	—	PT2	PS	PT1	PX1	PT0	PX0

- — Not implemented
- — Not implemented

PT2 - Reserved

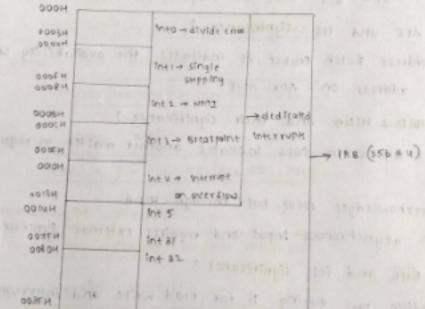PS - Priority of serial port interrupt

PT1 - Priority of timer 1

PX1 - Priority of External interrupt 1

PT0 - Priority of timer 0

PX0 - Priority of External interrupt 0

10. Draw the IVT of 8086

Address		
0000H		
0003H	Int0 → divide error	
0004H		
0007H	Int1 → Single stepping	
0008H		
000BH	Int2 → NMI	→ dedicated interrupts
000CH	Int3 → Breatpoint	
000FH		→ IRB (256 × 4)
0010H		
0013H	Int4 → Interrupt on overflow	
0014H	Int 5	
03F8H	Int 61	
03F8H	Int 62	
03FCH		
03FFH	Int 255	

11. What is the difference blween a packed and unpacked BCD?

- Packed BCD represented as first 4bits and last 4bits in a byte.

  $75 → 01110101$

- Unpacked BCD is each number is represented by it own byte

  $75 → 00000111\ 00000101$

12. Write the formula to compute physical/effective address of a sou...
for 8086 ?

   OA → offset address
   $PA = 10H \times SA + OA$ SA → segment address

13. List various flag manipulation instructions of 8086.

   CLC - clear carry flag
   CMC - complement carry flag
   STC - set carry flag
   CLD - clear directional flag
   STD - set directional flag
   CLI - clear interrupt flag
   STI - set interrupt flag

14. What is ALE and its significance ?

   ALE is address Latch Enable, it indicates the availability of
   the valid address on $AD_0 - AD_{15}$

15. What is HOLD & HLDA and their significance ?

   It is 30 & 31 pins in 8086 indicates another master in requesting
   local bus.
   → processor acknowledges local bus through HLDA
   → HOLD is an asynchronous input and requires external synchronization.

16. What is $\overline{BHE}$ and its significance ?

   • $\overline{BHE}$ is active low during T_1 for read, write and interrupt
   acknowledge cycles.
   • status information is available during $T_2, T_3 \& T_4$
   • Becomes tristated during hold.

what is the difference blween a array and a string ?

An array is a data structure while a string is a object. Arrays can hold any datatypes, which strings hold any data types, while strings hold only char data types. Array have fixed length while strings do not.

18. Why the crystal frequency of a microcontroller must be a minimum frequency specified by the vendor ?

crystal frequency of a microcontroller must be a minimum frequency specified by the vendor to get the standard baud rates for UART communication.

19. Draw SCON register

SMO	SMI	SM2	REN	TB8	RB8	TI	RI

20. Draw TCON register

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

21. Draw PCON register

SMOD	-	-	-	GF1	GF0	PD	IDL

22. Draw IP register

-	-	PT2	PS	PT1	PX1	PT0	PX0

23. Draw TMOD register

Gate	C/T	M1	M0	Gate	C/T	M1	M0

24. What does TEST instruction perform ?

TEST is 23pin examined by a WAIT instruction
• If low, execution will continue else the processor will remain in idle state.

25. Draw the Instruction format of a typical 8086 instruction:

W	D	S	V	Z	REG

26. What are the various components of assembly language instruction

Basic elements of assembly language instruction are

- Directives
- Labels
- comments
- operands

27. What is the size of ARM instruction?

32-bit

28. What is the size of thumb instruction?

16-bit

29. What is the size of Jazzle instruction?

8-bit

30. A constant cannot be a destination operand in 8086 (T/F)?

True

31. What are different datatypes of an ARM processor.

Byte - 8-bit

Halfword - 16-bit

word - 32-bit

Long word - 64-bit

32. Status of 8086 SP after push and pop operations.

push : stack pointer decremented by 2

POP : stack pointer incremented by 2

33. Status of 8051 SP after push and pop operations

push : stack pointer incremented by 1

POP : stack pointer decremented by 1

Why is the instruction byte queue size of 8086 is 6 bytes?

Longest instructions can be possible upto 6 bytes hence instructions queue has size of 6-bytes in 8086

35. Operating frequency of 8086 is ?

5MHz. to 10MHz

36. UART full form.

Universal Asynchronous Receiver and Transmitter

37. Difference b/ween minimum and maximum modes of 8086

Minimum mode	maximum mode
• there can be only one processor	• There can be multiple processor
• circuit is simpler	• circuit is more complex.
• multiprocessing cannot be performed	• multiprocessing can be performed
• performance is lower	• High performance.

38. What various versions of ARM cortex based on Applications.

ARM-cortex : A- series [Advanced computing applications]

ARM-cortex : R-series [used for real time applications]

ARM-cortex : M-series (microcontroller based applications]

39. Expand OMAP.

open multimedia application processor

40. What is the difference b/ween a microprocessor and DSP?

Microprocessor	DSP
• Instructions are executed in single cycle of the clock	• multiple clock cycles are required for execution.
• parallel execution is possible	• Execution of instruction is always sequential.

41. List the segment registers of 8086.

        code segment (cs)
        data segment (DS)
        Stack segment (SS)
        Extra segment (ES)

42. List out bit-wise logical instructions of 8051.

    ANL, ORL, XRL, CLR, CPL, RL, RLC, RR, RRC, SWAP

43. List the conditional branching instructions of 8051.

        CALL - Acall, Lcall
        RET - Return
        RETI - Return from an interrupt subroutine
        Jump - Ajmp, Ljmp, Sjmp ,Jz, Jnz, gnc, djne

44. Write a short note on dptr.

   • DPTR is a 16-bit register has not any internal address
   • DPTR has two 8-bit register DPH & DPL these are addressable registers
   • DPTR points to program.

45. Write short note on ARM instructions B and BL.

   B :- The B instruction causes a branch to label

   BL :- The BL instruction copies the address of the next instruction in R14(-LR), and causes a branch to label.

46. How do you reset 8086 ?

The reset pin of 8086 and other processors will be cause the cs:IP to point to FFFF:0000 which is the lowest 16 bytes of memory. In that location only is a jump instruction to somewhere in the memory space to initialize the processor.

How could you reset 8051?

The 8051 is reset by holding the RST high for atleast two machine cycles and then returning it low.

48. SP content of 8051 when it is reset?

If SP is resets then it sets to 07H, it can be changed to any internal address.

49. I/o port buffer content when 8051 is reset?

When I/O port is resets then it sets to FFH.

50. List the index registers of 8086.

  i. Source index register

  ii. destination index register

51. List the pointer registers of 8086

  i. Stack pointer register

  ii. Base pointer register

52. What are the addressing modes supported by 8051 instructions?

  i. Immediate addressing mode

  ii. Register addressing mode

  iii. Direct addressing mode

  iv. Indirect addressing mode.

53. What is NMI?

Pin no: 17 - NMI (Non maskable interrupt)

• It is an edge-triggered i/p causes a Type-2 interrupt

• Input is internally synchronised.

54. How do you compute the address of ISR in 8086?

The vector address for an 8086 interrupt is obtained from a vector table implemented in the first 1KB memory space

$$CS:IP = 4 bytes = 256 \times 4 = 1024 = 2^{10} = 1KB \ [00000H - 03FFFH].$$

55. What are different 8051 timer modes?

TMOD, TCON, TL0, TH0, TL1, TH1

56. What are different 8051 serial communication modes?

SCON
SBUF
PCON

57. Write short note on $\overline{WR}$ and $\overline{RD}$.

$\overline{RD}$:- RD indicates that the 8086 is performing a read of data of the IO bus.

• It only shows T_2, T_W, T_3 of any read cycle.

$\overline{WR}$:- The 8086 switches WR to logic 0 to signal external device that valid write, or output data on the bus.

58. What is the principle of even & odd address banks?

• The organisation of memory into two banks and providing bank select signals allows the programmer to read/write the byte operand in any memory address through 16-bit data bus.

• Byte data with an even address transferred on $D_7 - D_0$
• Byte data with an odd address transferred on $D_{15} - D_8$

59. What is long multiplication in ARM?

Long byte multiplication length is of 64-bit in ARM.

60. What is accumulation in ARM multiplication operations?

Multiplication in ARM can be performed as only multiplication and multiply & accumulation

• where the result can be stored as 32-bit/64-bit.

61. List various barrel shifter operations?

LSL   ASR   ROX
LSR   ROR

What is difference blween packed BCD and unpacked BCD numbers?

• Packed BCD represented as first 4bits and last 4bits in a byte.

$$75 \rightarrow 01110101$$

• unpacked BCD represented its each number by its own byte

$$75 \rightarrow 00000111 \ 00000101$$

63. What is difference between Mov, Move, Movx 8051 instructions?

• MOVX :- This instruction is used to transfer data between external RAM and internal register 'A'.

• MOVC :- This instruction is a data transfer instruction blween accumulator and program code.

• Mov :- This instruction is an internal data which transfers blween the internal Registers.

64. What is Sjmp and Ljmp?

• Sjmp :- It is short jump, relative address is 8-bit it support 132 location forward

• It uses 8-bit address, It is an 2 byte instruction.

• Ljmp :- It is long jump, xange is 64KB

• It uses 16 bit address, it is an 3 byte instruction.

65. What is cjne and Djnz?

• cjne :- cjne instruction compares the first two operands and branches to specified destination if their values are not equal. If the values are the same, execution continues with the next instruction.

• DJnz :- Djnz instruction decrements the byte indicated by the first operand and, if the resulting value is not zero, branches to the address specified in the second operand.

66. How is load a constant into a segment register of 8086?

We can load a data into a segment register, first loading it into a general purpose register and then we have to move it from this geneneral register to the segment register.

67. What is the size of each logical segment of 8086 memory?

each logical segment has 64KB of memory and each type DS, CS, ES, SS have 256KB of memory.

68. 8051 ROM has 4 address banks (T/F) :

True

69. 8051 RAM has program code (T/F) :

False

70. 8051 timers are 16-bit (T/F) :

True.

71. Define coprocessor.

An ARM core can have one or more coprocessors to extend the availability of instructions configurable registers and I/O peripherals interfacing.

72. List any 4 conditional execution opcodes of ARM ?

MI : minus/Negative

PL : positive logic

VS : over flow

VC : VC no overlow

What is the difference b/ween a signed and unsigned numbers?

• signed numbers use sign flag or can be distinguish between negative values and positive values.

• whereas unsigned numbers stored only positive numbers but not negative numbers.

#4 write any 4 8086 Assembler directives !

    dB : define byte

    Assume

    offset

    label

#5. What is the difference b/ween a procedure and macro ?

• procedure :- set of instructions which can be called repetitively that performs a specific task.

• Requires less memory.

• Macro :- Sequence of instructions that is written within the macro definition to support programming.

• Requires more memory.

#6. write a short note on LDS and LES ?

• LDS/LES : load pointer to DS/ES.

• loads DS, ES are instructions for specified destination. content of 5000H.

#7. What is the size of SBUF ?

    8-bit of size.
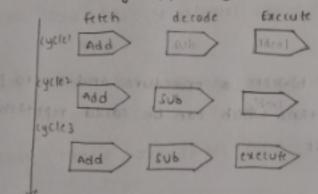
78. How many timing cycles an 8086 clock has?

cycles: (5) T₁, T₂, T₃, Tw, T4 in write mode

cycles: (4) T₁, T₂, T₃, T4 in read mode

79. How many timing cycles an 8051 clock has?

Each machine cycle in 8051 has 12 clock cycles.

80. Draw a 4 stage pipelining.

	fetch	decode	Execute
cycle1	Add	sub	Mrol
cycle2		Add	Sub	Mrol
cycle3		Add	Sub	execute

———— X ————