

D-A and A-D Converters

Introduction:-

- * In real-world, the physical quantities such as voltage, current, temperature, pressure and time etc. are available in analog form.
- * It is difficult to store, process or transmit the analog signals. and it also affects with noise.
- * For processing, transmission and storage purpose, it is often convenient to express these variables in digital form.
 - * It gives better accuracy and reduces noise.
 - * The operation of any digital communication system is based upon analog to digital (A/D) & digital to analog (D/A)

Conversion:-

- * Both ADC and DAC are also known as data converters and are available in IC form.

DAC [Digital to Analog Converter] :-

A digital to analog converter (DAC) converts a digital signal to an analog voltage or current output.

$$100101 \Rightarrow \boxed{\text{DAC}} \Rightarrow \text{Analog Output}$$

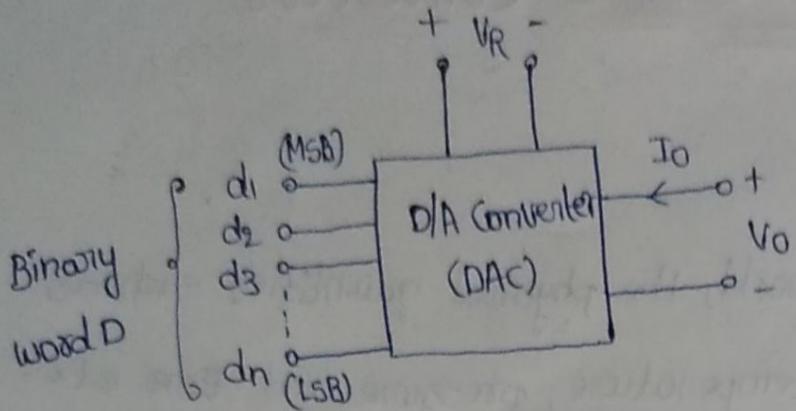


fig:- schematic of DAC

→ The ip is an n-bit binary word D and it is combined with a reference voltage VR to give an analog signal.

→ The op of a DAC can be either a voltage or current.

→ For a voltage op DAC, the D/A converter is mathematically

described as,

$$V_O = K V_{FS} \left(d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \dots + d_n 2^{-n} \right)$$

where,

V_O = output voltage

V_{FS} = full scale output voltage

K = scaling factor usually adjusted to unity.

d_1, d_2, \dots, d_n = n-bit fractional word.

d_1 = MSB

d_n = LSB

* DAC core available in many types:

1. Binary weighted Resistor DAC

2. R-2R Ladder DAC

3. Inverted R-2R Ladder DAC

1. Binary Weighted Resistor DAC :-

- * It utilizes a summing op-amp circuit
- * weighted resistors are used to distinguish each bit from the most significant to the least significant.
- * Transistors are used to switch between V_{ref} and ground [bit high or low]

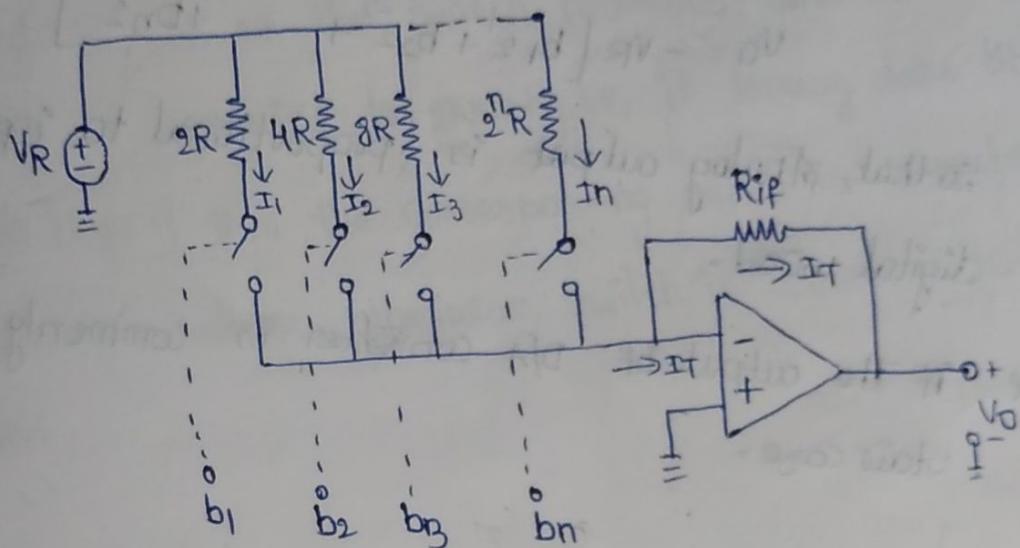


fig:- circuit diagram for weighted resistors DAC.

* FOR ON-Switch $I = VR/R$

Here, $b_1 = \text{MSB}$

$b_n = \text{LSB}$

* FOR OFF-Switch $I = 0$

$$I_T = \text{total current} = I_1 + I_2 + I_3 + \dots + I_n$$

$$I_T = \frac{VR}{2R} b_1 + \frac{VR}{2^2 R} \cdot b_2 + \frac{VR}{2^3 R} \cdot b_3 + \dots + \frac{VR}{2^n R} \cdot b_n \quad \text{--- (1)}$$

Here, $I_1 = \frac{VR}{2R} b_1$

$$I_2 = \frac{VR}{2^2 R} b_2$$

$$I_n = \frac{VR}{2^n R} \cdot b_n$$

$$I_T = \frac{VR}{R} \left[\frac{1}{2^1} b_1 + \frac{1}{2^2} b_2 + \dots + \frac{1}{2^n} b_n \right]$$

\therefore The o/p voltage,

$$V_O = -I_T \cdot R_{if}$$

$$V_O = -\frac{VR}{R} \times R_{if} \left[\frac{1}{2^1} b_1 + \frac{1}{2^2} b_2 + \dots + \frac{1}{2^n} b_n \right]$$

when $R_{if} = R$, V_O is given as,

$$V_O = -VR \left[b_1 \frac{1}{2^1} + b_2 \frac{1}{2^2} + \dots + b_n \frac{1}{2^n} \right]$$

so that, Analog output is proportional to input digital word.

* * The output of D/A converter is commonly a staircase.

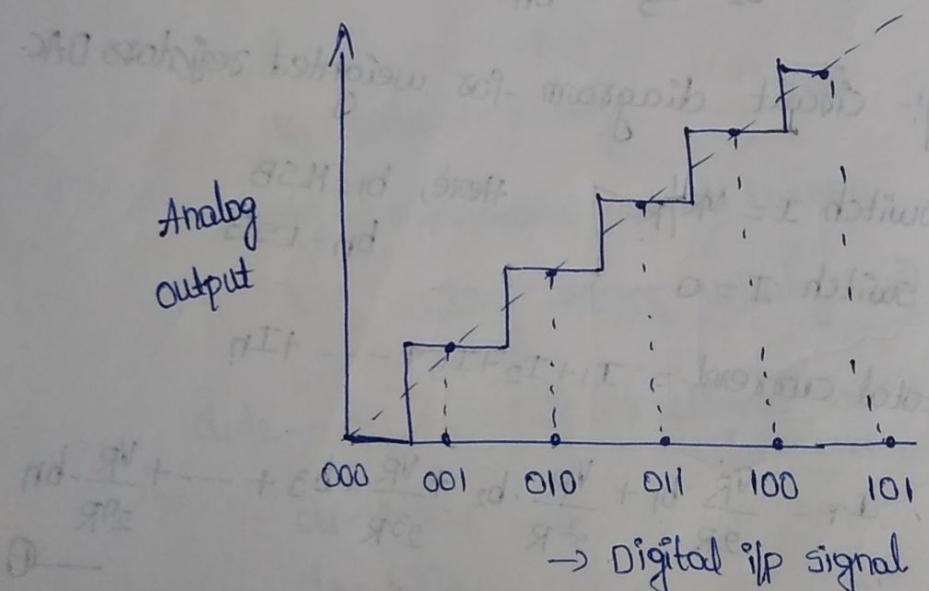


Fig:- DAC Response

Advantages:-

* simple construction and Analysis is easy.

* Fast conversion.

Disadvantages:-

- * Requires large range of resistors.
- * Requires low switch resistances in transistors.
- * Can be expensive. Therefore, usually limited to 8-bit resolution.

R-2R Ladder DAC:-

In this R-2R Ladder DAC, Reference voltage V_R is applied to one of the switch positions, and other switch position is connected to ground. i.e., if binary data bit is high [logic 1] then the corresponding switch is connected to reference voltage. otherwise, switch is connected to ground.

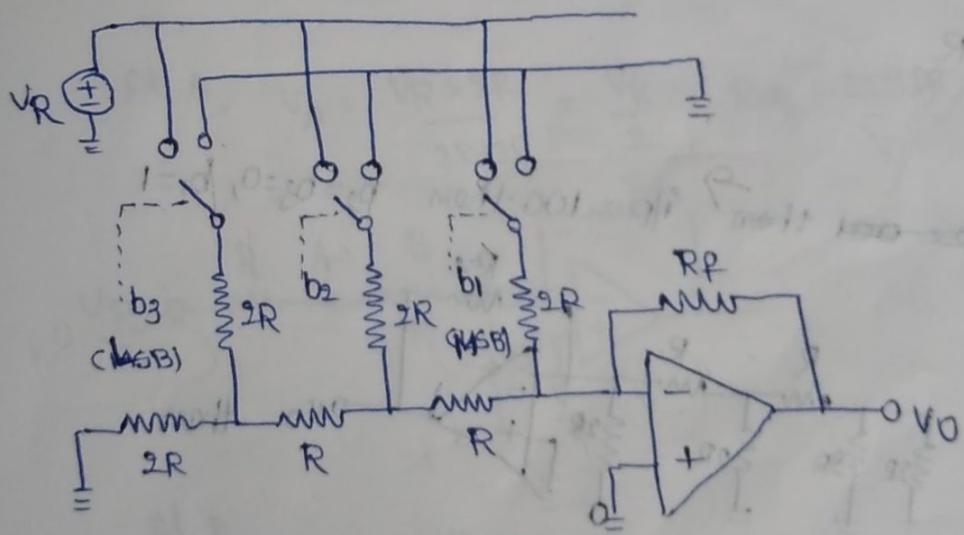


fig:- R-2R Ladder DAC.

Here, b_0 = LSB

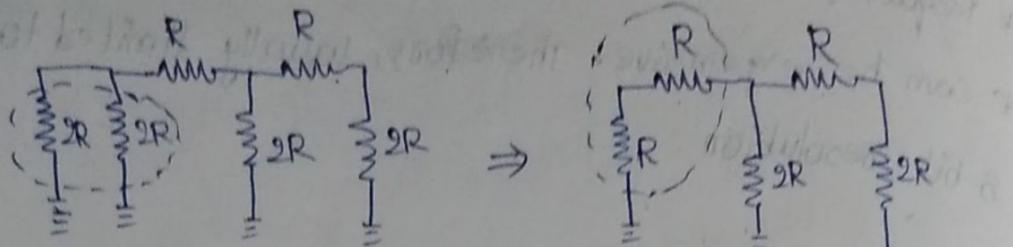
b_1 = MSB

* It uses only two values of Resistor ($R \& 2R$).

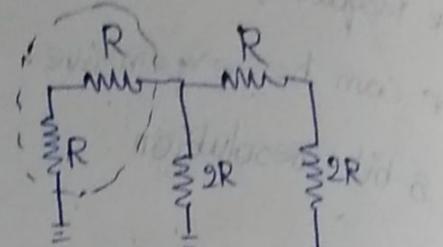
Hence easy and accurate fabrication can be done.

- * It is easy to scale with respect to no. of bits.
- * Impedance of Network is R , regard less of no. of bits.

i.e,



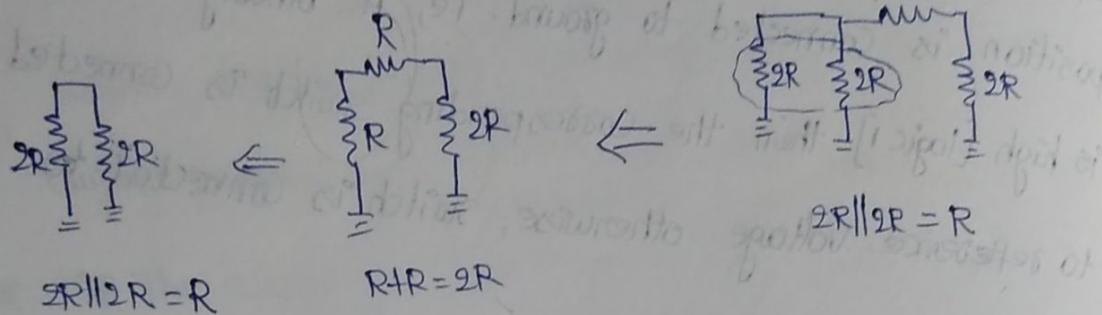
\Rightarrow



$$2R \parallel 2R$$

$$R+R = 2R$$

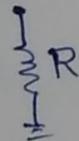
$$Req = \frac{2R \times 2R}{2R + 2R} = \frac{4R^2}{4R} = R$$



$$2R \parallel 2R = R$$

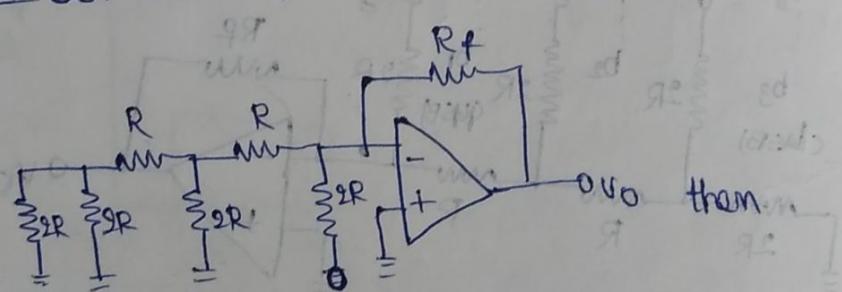
$$R+R = 2R$$

\Downarrow

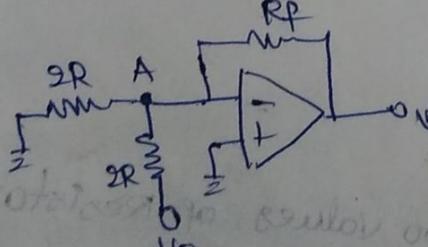


if ~~if~~ then $I_{IP} = 100$ then $b_2 = b_3 = 0, b_1 = 1$

then

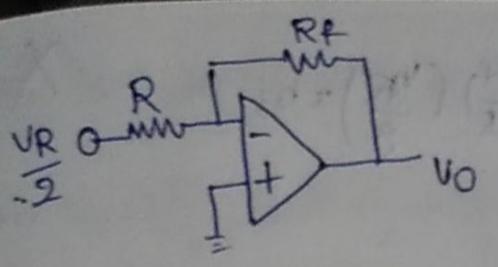


\Downarrow



$$VA = \frac{VR \times 2R}{2R + 2R} = \frac{VR}{2}$$

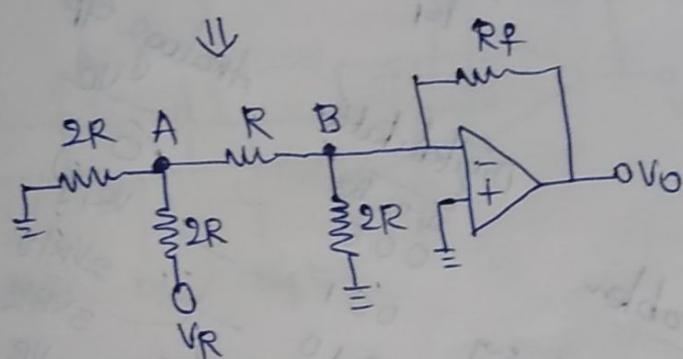
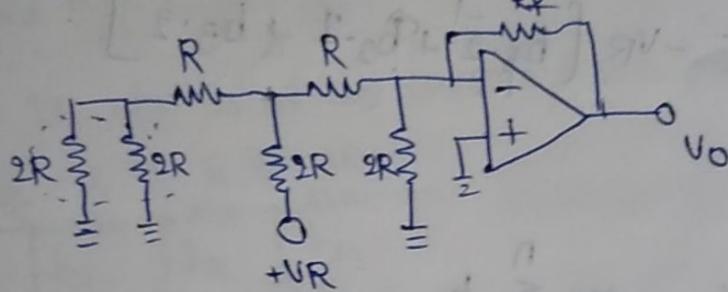
$$Req = R$$



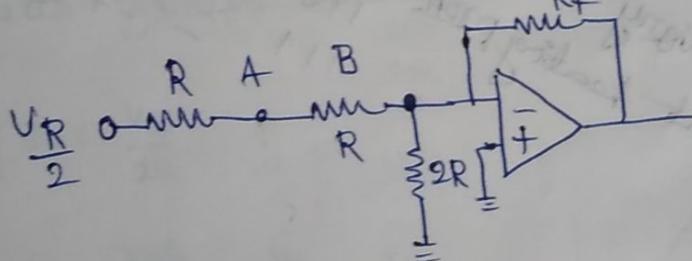
$$\therefore V_O = -\left(\frac{R_F}{R}\right) \cdot \left(\frac{V_R}{2}\right) \Rightarrow V_O = -\left(\frac{R_F}{R}\right) \frac{V_R}{2} \times b_1$$

Here $b_1 = 1$

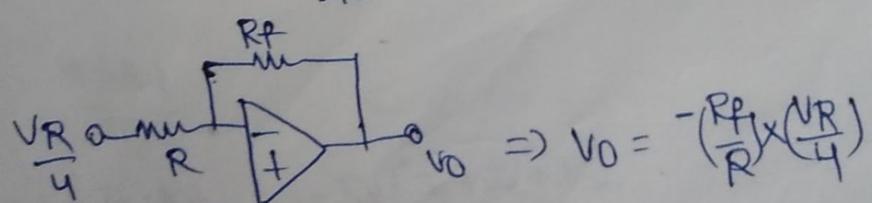
If $b_2 = 1, b_1 = b_3 = 0$ then if $p = 010$ then



$$\text{At } A, V_A = \frac{V_R \times 2R}{2R+2R} = \frac{V_R}{2}, \quad \text{Req} = 2R||2R = R$$



$$\text{At } B, V_B = \frac{V_R \times 2R}{2R+2R} = \frac{V_R}{4} \quad \text{Req} = 2R||2R = R$$



$$\Rightarrow V_O = -\left(\frac{R_F}{R}\right) \times \frac{V_R}{4} \times b_2$$

Here $b_2 = 1$

$$\text{like, } b_3=1, b_1=b_2=0 \Rightarrow V_O = -\left(\frac{R_f}{R}\right) \left(\frac{V_R}{8}\right) \cdot b_3$$

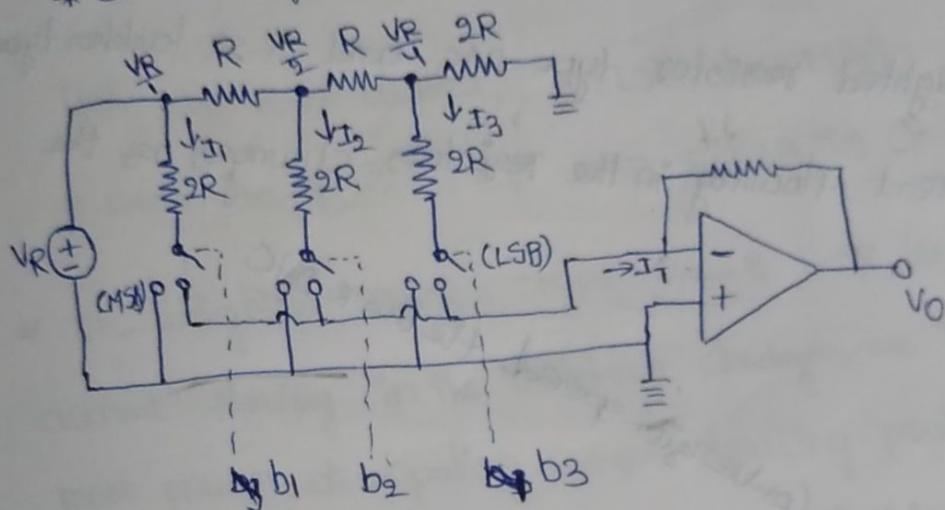
$$\rightarrow V_O = \left(\frac{R_f}{R}\right) V_R \left[\frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \dots \right]$$

If $R_f = R$ then

$$V_O = -V_R \left[b_1 \frac{1}{2} + b_2 \frac{1}{2} + b_3 \frac{1}{2} + \dots \right]$$

Inverted R-2R Ladder DAC:-

* It is also called as current mode R-2R ladder D/A converter



$$\text{Here, } b_1 = \text{MSB} \quad b_1 = \text{MSB}$$

$$b_3 = \text{LSB} \quad b_3 = \text{LSB}$$

* Switch connects between the Ground or virtual ground.

$$I_1 = \frac{V_R}{2R}$$

$$I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R} = \frac{I_1}{2}$$

$$I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R} = \frac{I_1}{4}$$

Like,

$$I_n = \frac{V_R/2^n}{2R}$$

$$\therefore V_O = -I_T \cdot R_f = -R_f (I_1 + I_2 + I_3)$$

$$\therefore V_O = -R_f \left[b_1 \cdot \frac{V_R}{2R} + b_2 \cdot \frac{V_R}{4R} + b_3 \cdot \frac{V_R}{8R} \right] \text{ for above circuit.}$$

$$\therefore V_O = - \left[b_1 \cdot \left(\frac{I}{2}\right) + b_2 \cdot \left(\frac{I}{4}\right) + b_3 \cdot \left(\frac{I}{8}\right) \right] R_F$$

$$I = \frac{V}{R}$$

$$V_O = - \left[b_1 \cdot \frac{-1}{2} + b_2 \cdot \frac{-2}{4} + b_3 \cdot \frac{-3}{8} \right] \cdot \frac{V_R \cdot R_F}{R}$$

For n-bits,

$$V_O = - \left[b_1 \cdot \frac{-1}{2^1} + b_2 \cdot \frac{-2}{2^2} + b_3 \cdot \frac{-3}{2^3} + \dots + b_n \cdot \frac{-n}{2^n} \right] \cdot \frac{V_R \cdot R_F}{R}$$

Here, b_1 = MSB

b_n = LSB in inverted R-2R ladder.

But, In R-2R Ladder, b_1 = LSB, b_n = MSB.

* Here the position of MSB & LSB is interchanged.

* In weighted register type DAC & R-2R ladder type DAC.

* In weighted register type DAC the current flowing in the resistors changes as i/p data. But more power dissipation causes heating problem.

* Inverted R-2R ladder DAC can be avoided heating problem completely.

* When switch is at logic '0' then current through 2R resistor flows to the ground. [+ve terminal of op-amp].

* When the switch is at logic '1', then current through 2R resistor sinks to the virtual ground [-ve terminal of op-amp].

Advantages -

* Only two resistor values (R & $2R$).

* Does not require high precision resistors.

* No. of bits can be expanded by adding more sections of same R/2R values.

IC 1408 :- (8 Bit - R-2R ladder DAC)

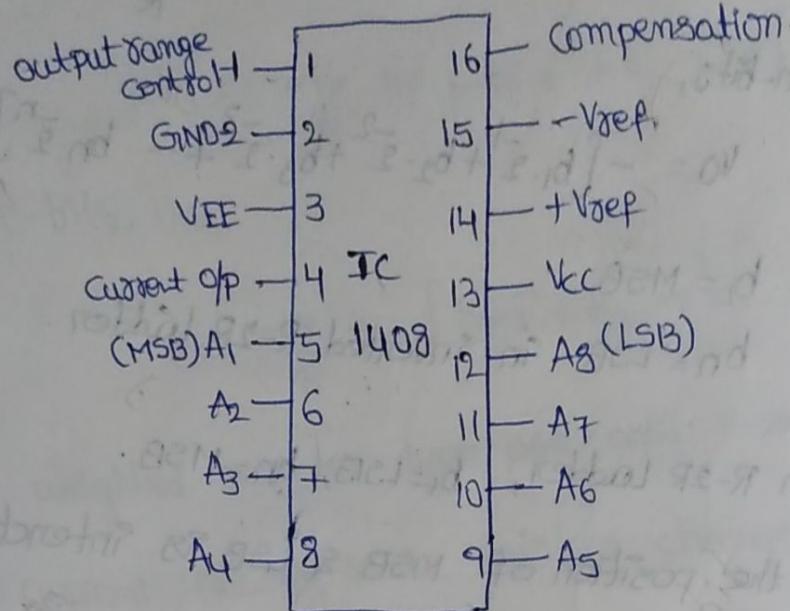


fig:- pin diagram

- * It is also called 8-bit R-2R ladder, Digital to analog converter.

- * It provides current output.

- * Current can be converted into voltage using I-V.

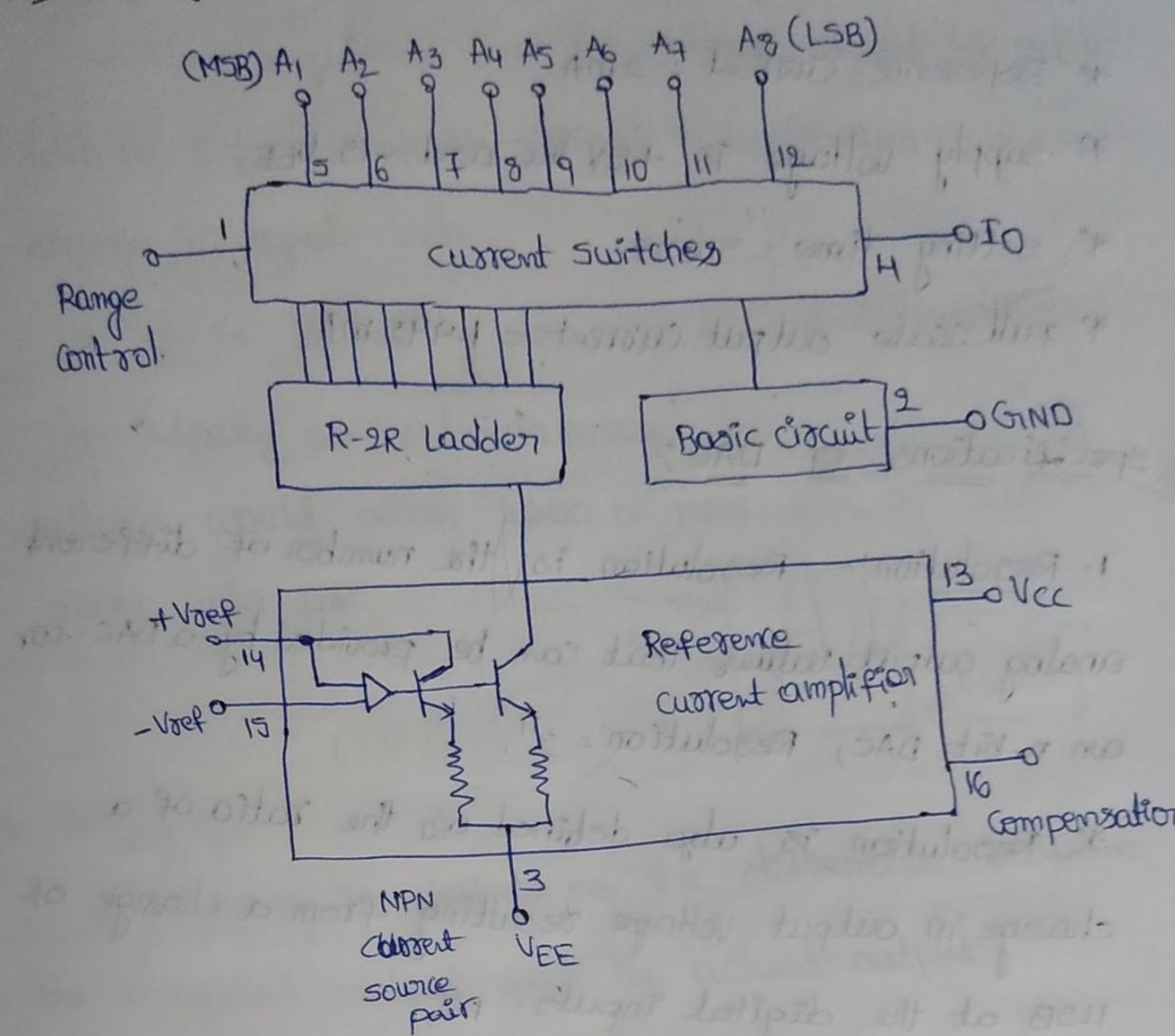
- * Compatible with both CMOS & TTL logics.

- * Here, A₁ = MSB & A₈ = LSB.

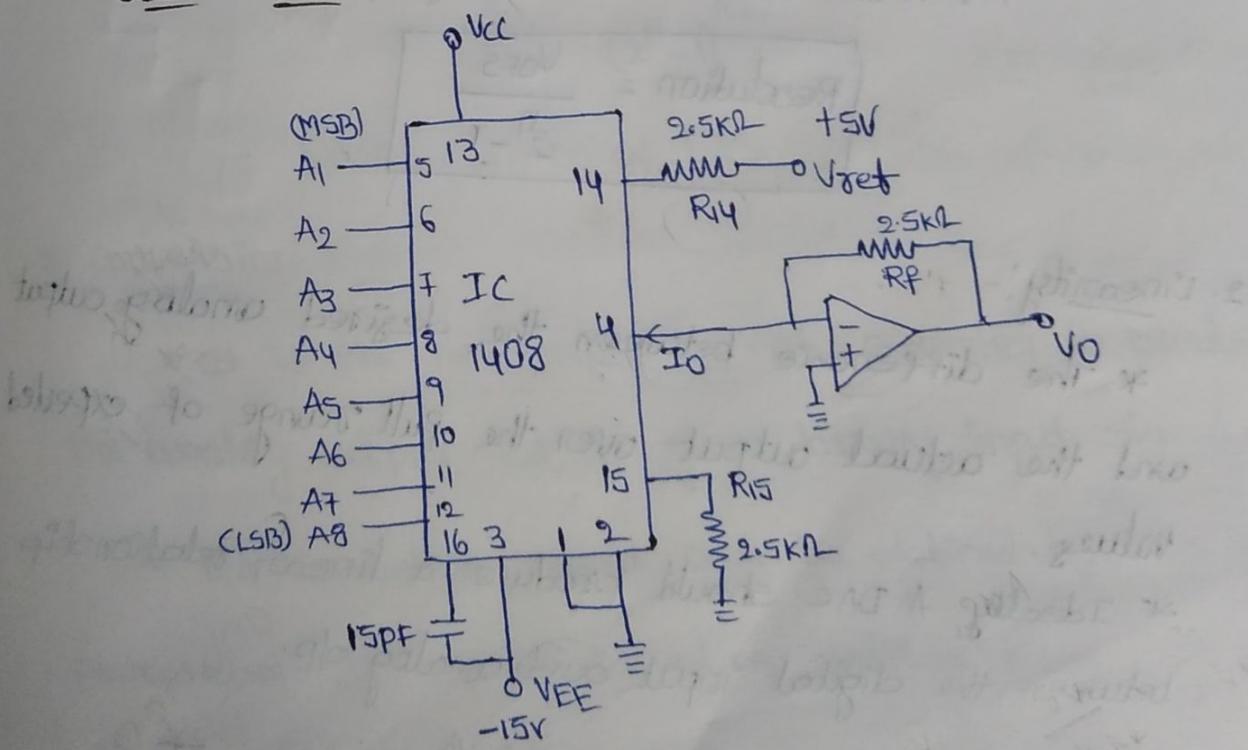
- * Output current is given as,

$$I_O = \frac{V_{ref}}{R_{14}} \left[\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right]$$

Block diagram:



Typical circuit:-



characteristics:-

- * Reference current = 2mA
- * supply voltage is +5V V_{CC} and -15 V_{EE}
- * setting time = 300ns
- * full scale output current = 1.992 mA

specifications of DAC:-

1. Resolution:- Resolution is the number of different analog output values that can be provided by a DAC. For an n-bit DAC, Resolution = 2^n .

* Resolution is also defined as the ratio of a change in output voltage resulting from a change of 1LSB at the digital inputs.

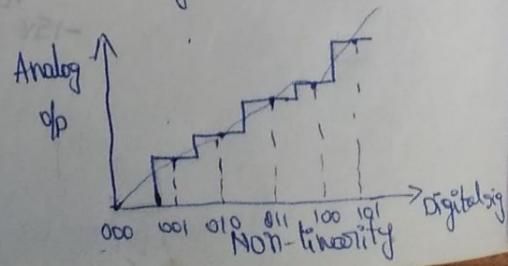
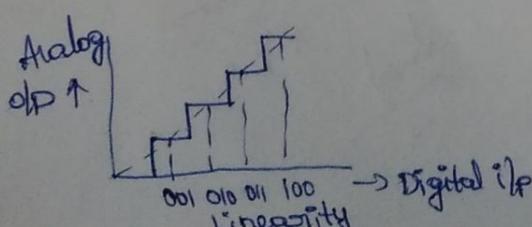
For n-bit DAC, it can be given as,

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1}$$

2. Linearity:-

* The difference between the desired analog output and the actual output over the full range of expected values.

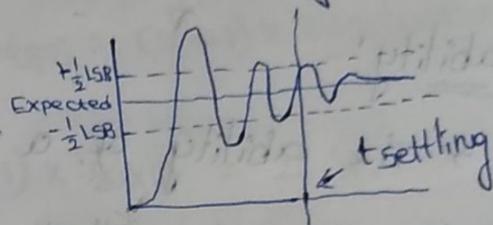
* Ideally, A DAC should produce a linear relationship between the digital input and analog o/p.



3 settling time:-

* Time required for the output signal to settle with in $\pm \frac{1}{2}$ LSB of its final value after a given change in input scale.

- * It is limited by slew rate of output amplifier.
- * Ideally, an instantaneous change in analog voltage would occur when a new binary word enters into DAC.



4. Accuracy:-

* Accuracy is defined as the difference between the measured output and the actual output.

$$\therefore \text{Accuracy} = \frac{V_{\text{ref}}}{(2^N - 1)^2}$$

where, N = no. of bits.

5. Conversion time:-

* It is the time taken for D/A converter to produce the analog output for the given binary input signal.

* D/A converters speed can be defined by this parameter. It is also called as settling time.

Monotonicity:-

- * A digital-to-analog converter is said to be monotonic, if the analog output increases for an increase in the digital input.
- * When DAC converter doesn't satisfy the condition described above, then, the output voltage may decrease for an increase in the binary input. i.e. non-monotonicity.

stability:-

- * The ability of a DAC to produce a stable output all the time is called as stability.
- * The performance of a converter changes with drift in temperature, aging and power supply variations.

Types of errors:-

1) Gain error:- It occurs when the slope of the

* The gain error is defined as the difference between the calculated gain of the current to voltage converter and the actual gain achieved.

2) Offset error:- Offset error is defined as the

* non-zero level of the output voltage when all inputs are zero.

3) Linearity error:- The linearity error is defined as the amount

by which the actual output differs from the ideal straight line output characteristic of DAC.

problems:

1. * The LSB of a 10-bit DAC is 20 mV.

i) what is its percentage resolution?

ii) what is its full-scale range?

iii) what is the output voltage for an input 1011001101?

Sol:-

$$\text{i) percentage resolution} = \frac{20 \times 10^{-3}}{2^{10}} \times 100 = 1\%$$

$$\text{ii) full-scale range } V_{OFS} = (2^n - 1) \times \text{resolution}$$

$$\therefore V_{OFS} = (2^{10} - 1) \times 20 \times 10^{-3} = 20.46 \text{ V}$$

$$\text{iii) output voltage } V_o = \frac{\text{Resolution}}{(2^n - 1)} \times (1011001101)_2 = 717 \times \frac{20 \times 10^{-3}}{1023} \text{ V}$$

$$V_o = 717 \times 20 \times 10^{-3} = 14.34 \text{ V}$$

2. what output voltage will be produced by 4 bit D/A converter

whose output range is 0V to 10V and whose input

binary is 0110?

Sol:-

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1} = \frac{10}{2^4 - 1} = 0.667 \text{ V}$$

$V_o = \text{Resolution} \times \text{Binary data}$.

$$V_o = 0.667 \times (0110)_2 = 0.667 \times 6 = 4 \text{ V}$$

$$V_o = 4 \text{ V}$$

③ The LSB of a 6-bit D/A converter represents 0.1V. what voltage value will be represented by the following binary words?

i) 101010 iii) 110110

Sol: Given that,

for a 6-bit D/A converter, $n=6$

LSB of 6-bit = resolution = 0.1V

i) Given binary word is 101010.

$$\text{output voltage } V_o = \text{Resolution} \times \text{Binary data}$$

$$= (0.1) \times (101010)_2$$

$$V_{D/A} = 0.1 \times (1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 0 \times 2^0)$$

$$= (0.1) (32 + 0 + 8 + 0 + 2 + 0)$$

$$\therefore V_o = 0.1 \times 42 = 4.2V$$

iii) Given binary word = 110110

$$\text{output voltage } V_o = 0.1 \times (110110)_2$$

$$= 0.1 \times 54 = 5.4V$$

④ LSB of a 6-bit DAC is represented 0.1mV. what is the full scale reading of this DAC?

Sol: Resolution = $\frac{V_{oFS}}{2^n - 1}$

$$\therefore V_{oFS} = (\text{Resolution}) \times (2^n - 1) = 0.1 \times (2^6 - 1) \times 10^{-3}$$

$$\therefore V_{oFS} = 6.3 \text{ mV}$$

$$= 6.3 \times 10^{-4} = 6.3 \text{ mV}$$

⑤ the basic step of 4-bit DAC is 10.3 mV . If 100000000 represents OR, what output voltage for the IP is 101101111 ?

Sol:-

$$\text{The o/p voltage} = 10.3 \times (101101111)_2 \times 10^{-3}$$

$$= 10.3 \times [10^{-3}] \times [1 \times 2^8 + 0 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 \times 1 \times 2^2 \times \\ 1 \times 2^1 + 1 \times 2^0]$$

$$= 10.3 \times 10^{-3} \times (367)$$

$$V_o = 3.78 \text{ V}$$

⑥ A 12-bit DAC has full scale range of 15 V . Its maximum differential linearity error is $\pm \frac{1}{2} \text{ LSB}$.

i) What is the % resolution?

ii) What are the minimum & maximum possible values of the increment in its o/p voltage?

Sol:-

Given that,

For 12-bit DAC, $n = 12$.

$$\text{full scale voltage } V_{FS} = 15 \text{ V}$$

$$\text{i) \% Resolution} = \frac{V_{FS}}{2^n - 1} \times 100 = \frac{15}{2^{12} - 1} \times 100 = 0.366\%$$

$$\text{ii) MSB} = \frac{V_{FS}}{2} = \frac{15}{2} = 7.5 \text{ V}$$

$$\text{LSB} = \frac{V_{FS}}{2^n} = \frac{15}{2^{12}} = 3.66 \times 10^{-3} \text{ V}$$

$$\text{LSB} = 3.66 \text{ mV}$$

Analog to Digital converters (ADC):

- * The A/D conversion is a quantizing process where an analog signal is converted into equivalent binary word.

* this A/D converter is exactly opposite function to that of the D/A converter.

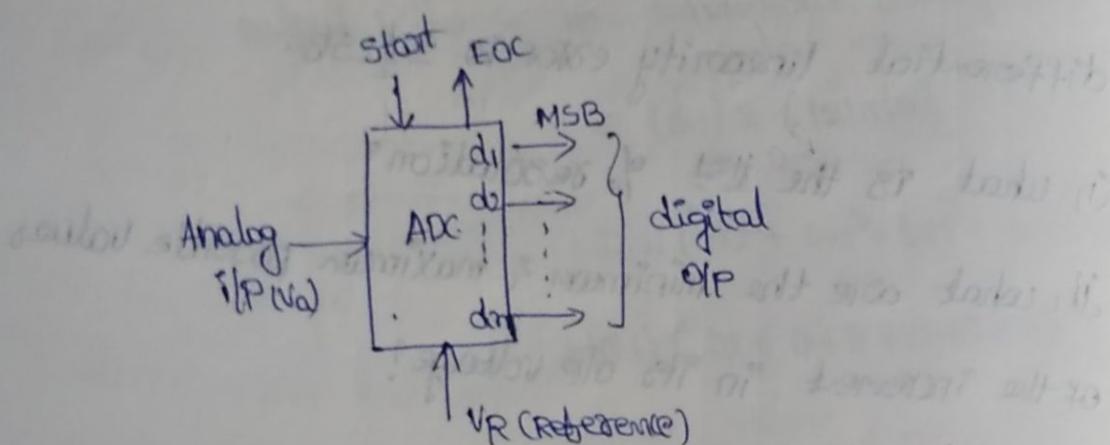
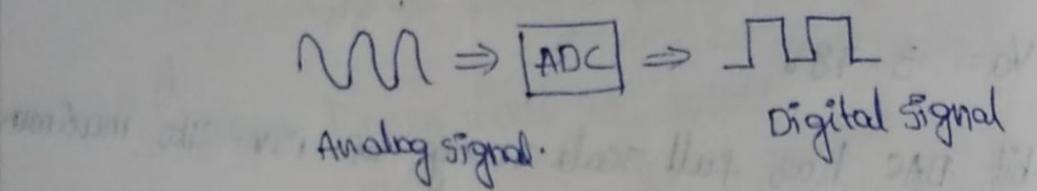


fig:- functional diagram of ADC.

- * It accepts an analog input voltage V_A & produces an output binary word $d_1, d_2, d_3, \dots, d_n$ of functional value D , so that

$$P = d_1 z^{-1} + d_2 z^{-2} + \dots + d_n z^{-n}$$

where, $d_1 = \text{MSB}$

$$dn = LSA$$

- * An ADC usually has two additional control lines
 - "start" input to tell ADC when to start the conversion
 - "Eoc" output to announce when the conversion is complete

* ADCs are classified broadly into two groups according to their conversion technique.

1. Direct type ADC

2. Integrating type ADC (indirect ADC)

1. Direct type ADCs:- It compare a given analog signal with the internally generated equivalent signal.
- this group includes:

1. parallel / flash (comparator) type converters.

2. counter type converters.

3. successive approximation type converters.

2. Integrating type ADCs! It perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to a digital code.

* Dual slope ADC is one of the integrating type ADC.

1. parallel comparator / flash type ADC:-

* It consist of comparators, each one comparing the input signal to a unique reference voltage.

* The Comparator outputs connect to the inputs of a priority encoder circuit, which produces a binary output.

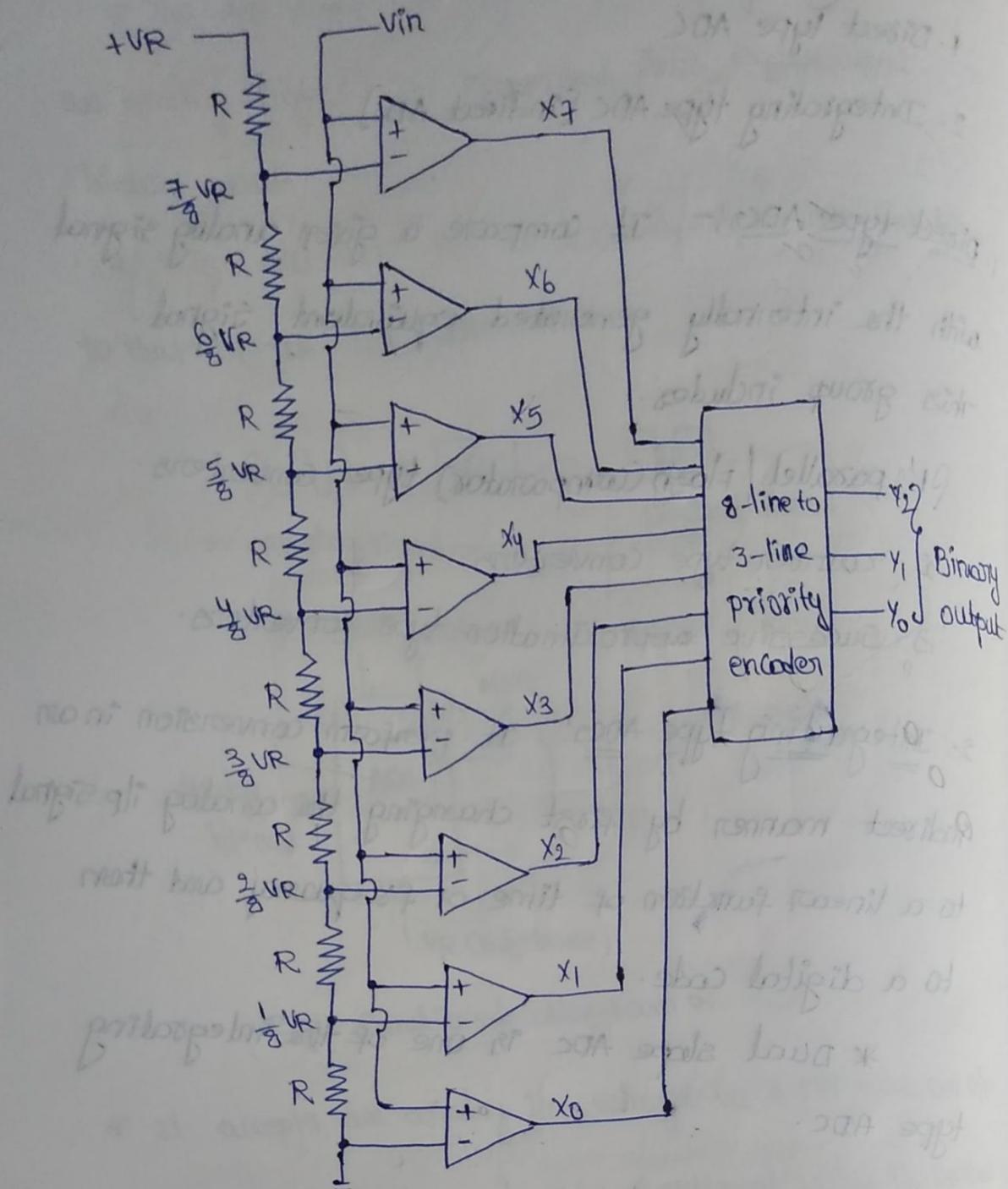


fig:- flash type ADC

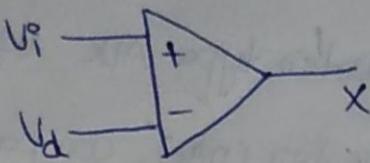
- * It is simplest A/D Converter and fastest A/D also.
- * In this we are using 8 op-amps (Comparators) and one 8-3 priority encoder.
- * Here VR is divided equally through resistors.

operating conditions:-

$$1. V_i > V_d ; x = 1$$

$$2. V_i < V_d ; x = 0$$

$$3. V_i = V_d ; x = \text{previous state}$$



* Encoder compares the code resulting from the comparators into binary code.

Input voltage (V_i)	x_7	x_6	x_5	x_4	x_3	x_2	x_1	x_0	y_2	y_1	y_0
0 to $\frac{V_R}{2}$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V_R}{2}$ to $\frac{3V_R}{2}$	0	0	0	0	0	0	1	1	0	0	1
$\frac{3V_R}{2}$ to $\frac{5V_R}{2}$	0	0	0	0	0	1	1	1	0	1	0
$\frac{5V_R}{2}$ to $\frac{7V_R}{2}$	0	0	0	0	1	1	1	1	0	1	1
$\frac{7V_R}{2}$ to $\frac{9V_R}{2}$	0	0	0	1	1	1	1	1	1	0	0
$\frac{9V_R}{2}$ to $\frac{11V_R}{2}$	0	0	1	1	1	1	1	1	1	0	1
$\frac{11V_R}{2}$ to $\frac{13V_R}{2}$	0	1	1	1	1	1	1	1	1	1	0
$\frac{13V_R}{2}$ to V_R	1	1	1	1	1	1	1	1	1	1	1

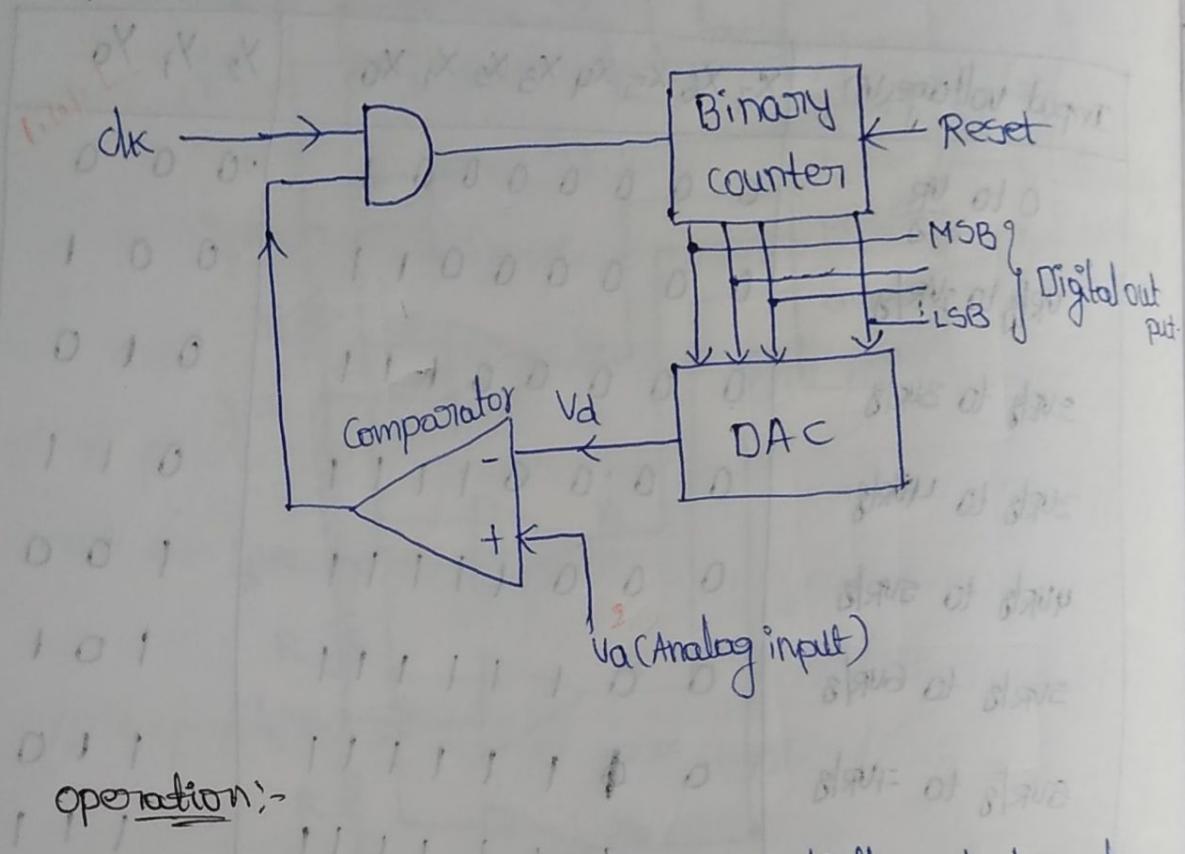
fig:- Truth table for flash type A/D converter

* The purpose of the circuit is to compare the analog input voltage V_{in} with each of the node voltages.

counter type ADC (ADC using DAC):-

* A counter-type ADC uses a binary counter, Digital-to-Analog converter (DAC), comparator and AND gate.

Basic principle:- The linear ramp can be produced by connecting the output of a counter to the input of a DAC.



Operation:-

* The n-bit binary counter is initially set to 0 by using reset command.

* Therefore, the digital output is zero and $V_d = 0V$.

* The clock pulses are allowed to go through AND gate and are counted by the binary counter.

* The D-to-A converter (DAC) converts the digital output to an analog voltage and applied as the

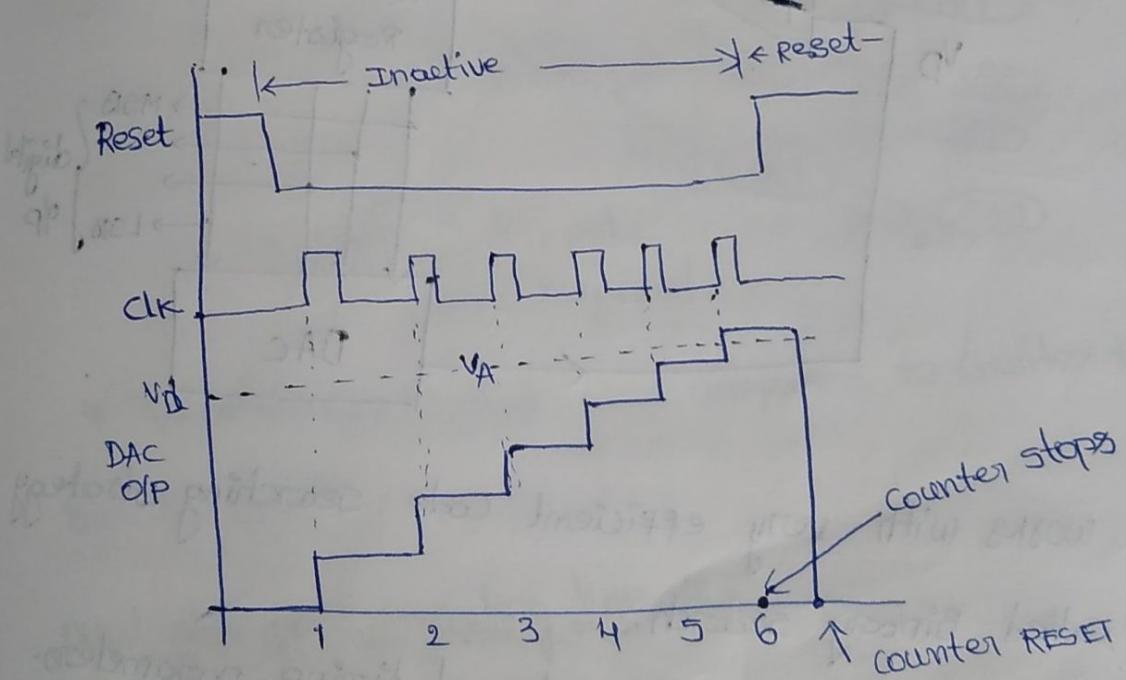
inverting input to the comparator.

- * the number of clock pulses increases with time and the analog input voltage V_d is a rising staircase waveform.

- * The counting will continue until the DAC output $V_d > V_A$.

- * Then the comparator output becomes low and thus disables the AND gate from passing the clock.

- * the counting stops at the instance $V_d < V_A$, and at that instant the counter stops its progress and the conversion is said to be complete.



- * The numbers stored in the n -bit counter is the

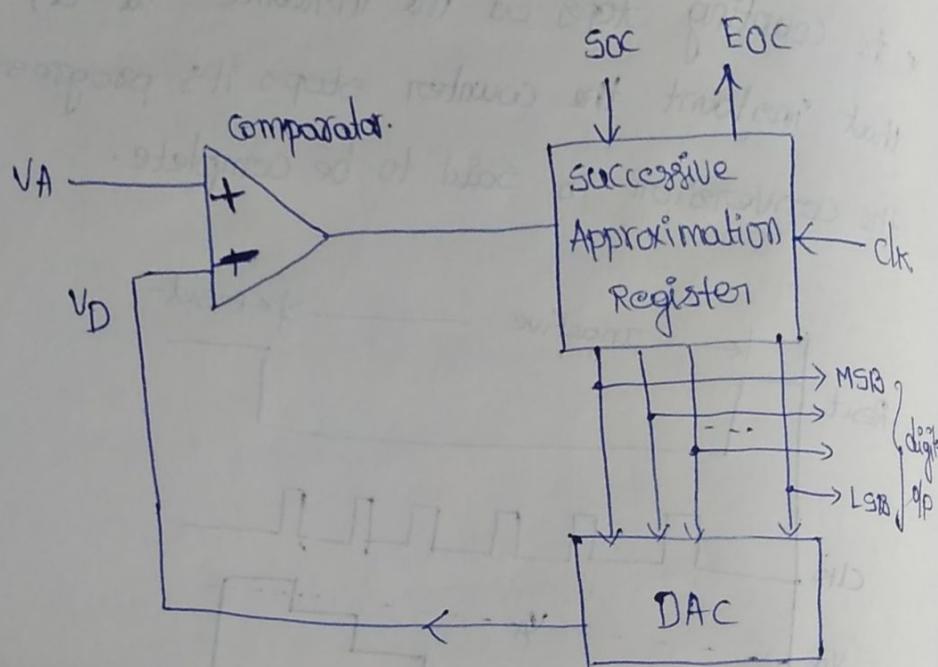
equivalent n -bit digital data for the given V_A .

- * Low speed is the most serious drawback of this method.

- * the conversion time can be as long as $(2^n - 1)$ clock periods depends upon the magnitude of input voltage V_A .

Successive Approximation Converter-

- * The successive approximation technique uses a very efficient to convert analog to digital output.
- * It consists of a DAC, a Comparator and Successive Approximation Register (SAR), the external clock clk sets the internal timing parameters. The $\text{start of conversion}$ signal starts initiates an A/D conversion & end of conversion (EOC) is obtained when the conversion is completed.



- * Works with very efficient code searching strategy called Binary search.
- * External clock sets the internal timing parameters.
- * The SOC initiates the process of search.
- * The SAR sets - MSB bit ($\text{MSB} = 1$)
- * The corresponding V_D generates by DAC.

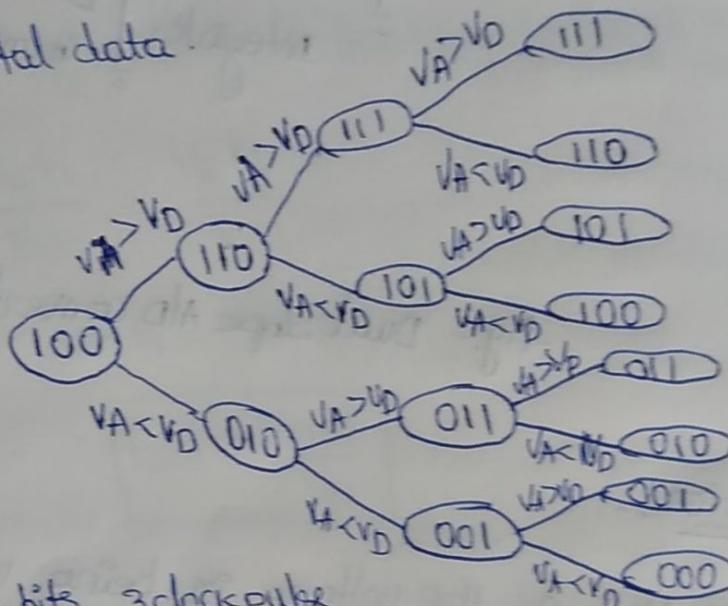
- * if $V_A > V_D$, then next significant bit will be set (1).
- * if $V_A < V_D$, then MSB = 0, next significant bit will be set to 1 by the SAR and then the process will be repeated.
- * The comparator changes its state whenever the DAC crosses V_A and this activates the EOC.

for example:-

For 3-bit digital data.

initially

At S0C,



For 3-bits, 3 clock pulse required.

* The conversion is fast when compared to counter type ADC.

But is complex.

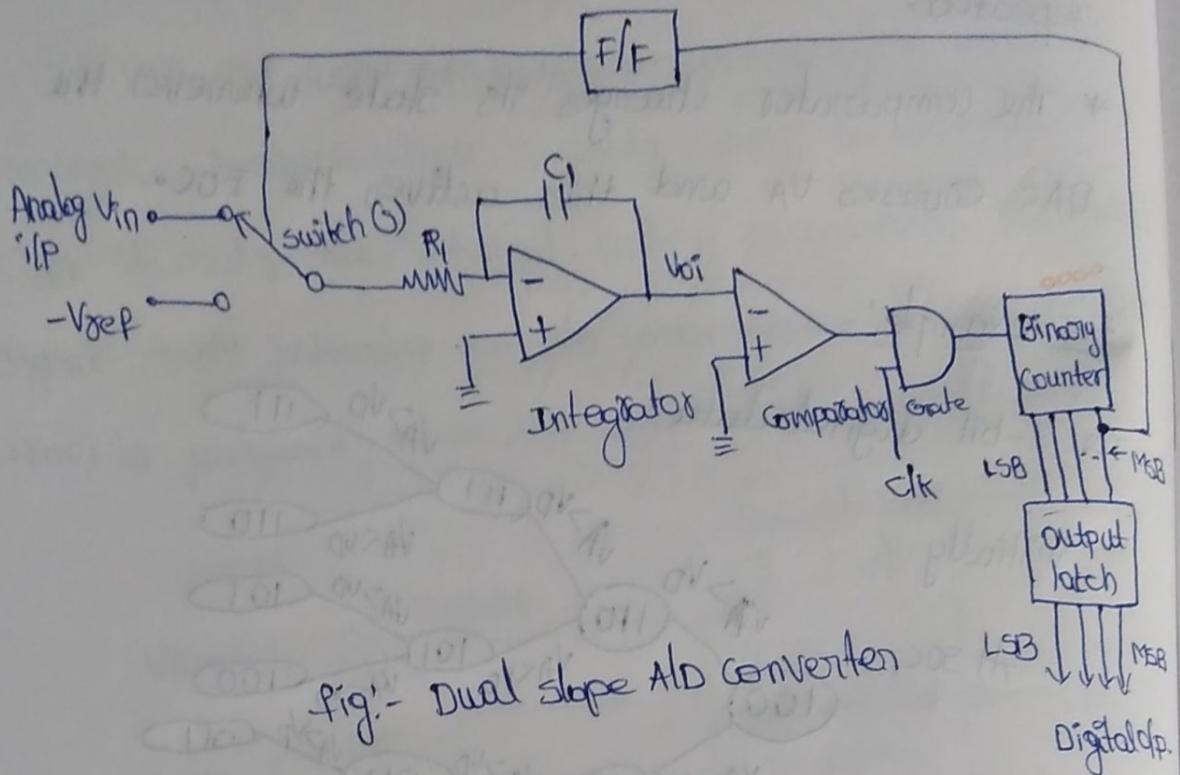
Dual slop or Integrating type ADC:-

* It is Indirect method of ADC conversion.

* Ref Voltage is converted into time periods by an integrator & then measured by Counter.

* Speed of conversion is ~~fast~~ slow. But accuracy is high.

- * The Ramp generator input - switched between V_i and a negative reference voltage $-V_{ref}$



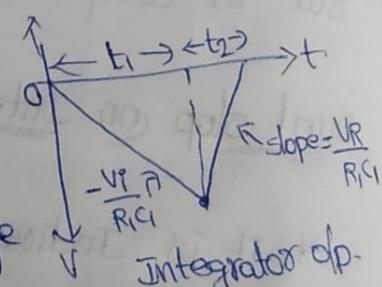
operation:-

- * When MSB=0, the voltage is being measured is connected to the ramp generator input.
- * When MSB=1, the negative reference voltage is connected to the ramp generator.

- * At time, $t=0$, analog switch S is connected to the analog input voltage V_{in} , so that the analog input voltage V_{in} .

Integration begins, the output of integrator is given as

$$V_{oi} = -\frac{1}{R_1 C_1} \int_0^t V_{in} dt = \frac{-V_{in} t}{R_1 C_1}$$



- * Here, $R_1 C_1$ is time constant & V_{in} is constant.
- * At the end of 2^N clock periods MSB goes high.
- * So, output of flip-flop goes high, which causes the switch S to be switched from V_i to $-V_{ref}$.
- * Therefore, integrator output is +ve.
- * When o/p reaches to 0, comparator o/p goes low.
- * Which disables the AND gate & counter stops.
- * If the charge voltage & discharge voltages are equal.

$$\frac{V_{int1}}{R_1 C_1} = \frac{V_R t_2}{R_1 C_1}$$

$$V_{int1} = V_R t_2.$$

$$\therefore t_2 = \frac{V_{int1}}{V_R}$$

$$\text{digital output} = \left(\frac{\text{counts}}{\text{second}} \right) \times t_2.$$

$$\therefore \text{digital output} = \frac{\text{counts}}{\text{second}} \times \frac{V_{int1}}{V_R}$$

problems:

- * For a particular dual slope ADC, t_c is 83.33ms and the reference voltage is 100mV. Calculate the t_2 if reference voltage is 100mV.

(i) $V_{in} = 100\text{mV}$ (ii) $V_{in} = 200\text{mV}$.

Sol:-

(i) Given that, $V_{in} = 100\text{mV}$, $V_{ref} = 100\text{mV}$; $t_1 = 83.33\text{ms}$.

$$\therefore t_2 = \frac{V_{in}}{V_{ref}} \times t_1 = \frac{100}{100} \times 83.33 \stackrel{\sqrt{10}}{=} 83.33\text{ms}.$$

$$(iii) V_m = 200 \text{ mV}$$

$$t_2 = \frac{200}{100} \times 83.33 \times 10^{-3} = 166.6 \text{ ms}$$

$$t_2 = 166.6 \text{ ms}$$

Specifications of ADC:-

1. Resolution:- The resolution refers to the finest minimum change in the signal which is accepted for conversion, and it is decided with respect to number of bits is 2^n .

* Resolution can also be defined as the ratio of change in the value of input voltage V_i , needed to change the digital output by 1 LSB. It is given as,

$$\text{Resolution} = \frac{V_{IFS}}{(2^n - 1)}$$

V_{IFS} = Input Full-scale input voltage.

2. Conversion time:- It is defined as the total time required for an A/D converter to convert an analog signal to digital output. It depends on the conversion technique and propagation delay of the circuit components.

3. Analog error:- An error occurring due to the variations in RC switching point of the comparators, resistors, reference voltage source, ripples and noises introduced by the circuit components is termed as Analog error.

4. Linearity error:-

It is defined as the measure of variation in voltage step size. It indicates the difference between the transitions for a minimum step of input voltage change. This is normally specified as fraction of LSB.

problem!

* A 8-bit ADC outputs all 1's when $V_i = 5.1V$. Find its
 (a) Resolution (b) digital output when $V_i = 1.28V$.

Sol:-

Given that, $V_{IFS} = 5.1V$

No. of bits $n = 8$

$$(a) \text{Resolution} = 2^8 = 256.$$

$$\text{Resolution in Volts} = \frac{V_{IFS}}{2^n - 1} = \frac{5.1}{2^8 - 1} = 20 \text{ mV / LSB}$$

(b) Input voltage $V_i = 1.28V$.

Digital output D = ?

$$D = \frac{1.28}{20 \text{ mV / LSB}} = 64 \text{ LSB}$$

The binary equivalent of 64 is $(0100\ 0000)_2$.