Code No: 153AN **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, October - 2020
DIGITAL SYSTEM DESIGN
(Electronics and Communication Engineering)

Time: 2 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
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1.a) Convert the following to Binary and then to gray code:
i) $(AB33)_{16}$ ii) $(3323)_8$
b) Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend.
i) 11010 – 10010 ii) 100 – 110000. [7+8]

2.a) Derive Boolean expression for a 2 input Ex-NOR gate to realize with two input NOR gates, without using complemented variables and draw the circuit.
b) Implement the function F with the following two level forms
i) NAND-AND
ii) AND-NOR
F(A,B,C,D) = P(0,1,2,3,4,8,9,12). [7+8]

3. For the given function F(A, B, C, D, E) =Σ(0,1, 2, 3, 4, 5, 9, 10, 16, 17, 18, 19, 20, 22, 25, 26)+ Σd (7, 11, 12, 13, 15, 23, 27, 28, 29, 30).
Obtain minimal SOP expression using K-Map. [15]

4.a) Implement the multiple output combinational logic circuit using a 4 line to 16 line decoder.
f1 = Σm(1, 2, 4, 7, 8, 11, 12, 13, 14, 15) f2 = Σm(0, 1, 3, 5, 8, 9, 15)
f3 = Σm(2, 3, 4, 7) f4 = Σm(0, 1, 3, 4, 7, 9)
b) Design a 32:1 Multiplexer using two 16:1 and 2:1Multiplexers. [8+7]

5.a) Design a 4 bit universal shift resister and draw the circuit with the given mode of operation table.

S_1	S_0	Operation
0	0	Shift left
0	1	Shift right
1	0	Parallel
1	1	Inhibit clock

b) Explain how a T Flip-Flop is converted to J-K Flip-Flop. [8+7]

6.a) Using the method of flip flop conversion carry out S-R to T conversion.
b) Design and implement a MOD-7 synchronous counter using T flip-flops. [7+8]

7.a) Design a Mod-6 synchronous counter using J-K flip flops.
b) Explain the design of a serial binary adder. [8+7]

8.a) Draw and explain the circuit diagram of a diode OR gate for positive logic.
b) Draw the circuit diagram of diode-transistor logic NOR gate and explain its operation. [7+8]

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