Code No: 09A50201 **R09** **Set No. 2**

III B.Tech I Semester Examinations,December 2011
IC APPLICATIONS
Common to Electronics And Telematics, Electronics And Communication Engineering, Electrical And Electronics Engineering

Time: 3 hours **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the difference between Analog to Digital converter and Digital to Analog converters through underlying equations.
   (b) Illustrate one application each of Analog to Digital and Digital to Analog converters. [5+10]
2. (a) With the help of logic diagram explain 74×157 multiplexer.
   (b) Design a full subtractor with logic gates?
   (c) Using the above subtractor design a 8-bit ripple subtractor. [8+3+4]
3. (a) Design a conversion circuit to convert a T flip-flop to J-K flip-flop?
   (b) Write short notes on:
      i. Edge triggered flip-flop
      ii. Master slave flip flop. [7+8]
4. (a) What is a level translator circuit? Why it is used with the cascaded differential amplifier?
   (b) What is a cascode amplifier? List the characteristics of the cascode amplifier. [8+7]
5. (a) Design a fourth order Butter worth low pass filter having upper cut off frequency 1 KHz and pass band gain of 10.
   (b) Write about frequency transformation in active filter. [10+5]
6. (a) Describe the application of 555 timer as pulsing buzzer.
   (b) What are the functions of threshold and control voltage pins in 555 timer IC? [10+5]
7. Consider the circuit shown in figure 1:

   Determine the following when, $V_1 = 1V$ & $V_2 = 2V$

   (a) I_x
   (b) V_A
   (c) V_B
   (d) Expression for V_A & V_B in terms of V_1 & V_2. [15]

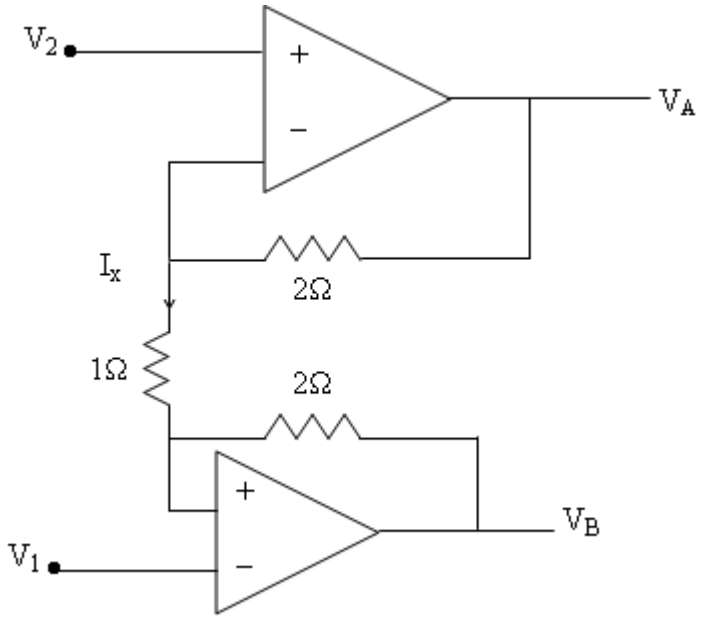

Figure 1:

8. (a) Design a CMOS transistor circuit with the functional behavior $f(X) = \left(A + \bar{B}\right)\left(C + \bar{D}\right)$

   (b) Distinguish between static and dynamic power dissipation of a CMOS circuit? Derive the expression for dynamic power dissipation? [8+7]

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Time: 3 hours **Max Marks: 75**

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1. (a) Using two 74×138 decoders design a 4 to 16 decoder?
   (b) Realize the following expression using 74×151 IC?
   f (X) = $\bar{A}BC + A\bar{B}C + AB\bar{C}$ [7+8]

2. (a) With a neat diagram explain about triangular wave generator.
   (b) With a neat diagram, Explain about Sawtooth. Wave form generator. [7+8]

3. (a) What are the parameters that are necessary to define the electrical characteristics of CMOS circuits? Mention the typical values of a CMOS NAND gate.
   (b) Design a CMOS 4-input AND-OR-INVERT gate. Draw the logic diagram and function table. [7+8]

4. (a) Write a note on multiplying DACs.
   (b) Compare and contrast R-2R ladder type and weighted resistor type DACs.
   (c) List the specifications of a Digital-to-Analog converter IC, 1408. [5+5+5]

5. (a) Design a 4-bit binary synchronous counter using 74×74.
   (b) Design a modulo-60 counter using 74×163 ICs. [7+8]

6. (a) How an symmetrical wave form generator can be constructed using 555 timer?
   (b) If R_A = 6.8 kΩ, R_B = 3.3 kΩ, c = 0.1 μF in 555 astable multivibrator. Calculate:
      i. t_{high}
      ii. t_{low}
      iii. Free running frequency
      iv. Duty cycle. [5+10]

7. (a) Explain the various techniques used to compensate for thermal drift in Op-Amps.
   (b) Explain the effects of time on input-Offset voltage and input-offset current. [8+7]

8. (a) Explain what the circuit does as shown in figure 2 and explain its working.

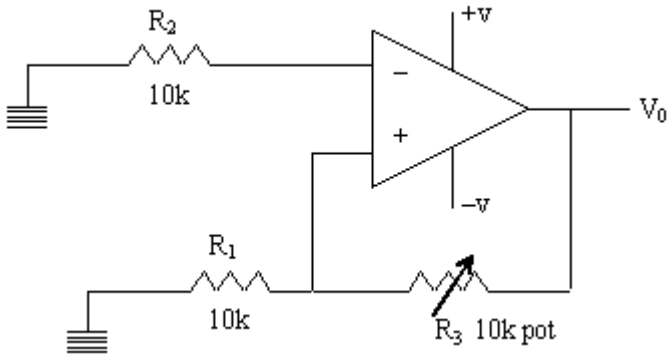

Figure 2:

(b) What is the maximum value for V_{in} when the potentiometer is set to its maximum resistance? [10+5]

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Code No: 09A50201 **R09** **Set No. 1**

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Time: 3 hours **Max Marks: 75**

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1. (a) Explain the role of negative feedback in operational amplifiers.
   (b) How does negative feedback affect, the performance of an inverting amplifiers?
   (c) What are the three operating temperature ranges of the IC? [7+4+4]
2. (a) Explain the operation of parallel comparator type ADC with the help of a neat diagram.
   (b) The LSB of a 6-bit D/A converter represents 0.1V. What voltage value will be represented by the following binary words?
      i. 101010
      ii. 110110 [10+5]
3. (a) Define the conditions on the feed back circuit of an amplifier to convert it into an oscillator.
   (b) What is VCO? Give two applications of it.
   (c) Design a 60 Hz Active LPF. [4+4+7]
4. (a) Explain how LF 398 can be used as sample and hold circuit?
   (b) Draw the wave forms of inverting and non-inverting comparator. [9+6]
5. (a) Give the logic diagram of 74×139? Explain with the help of truth table? Using this device design a 3 to 8 decoder and provide the truth table?
   (b) Design a 16-bit comparator using 74×85 ICs? [8+7]
6. (a) Explain the effect of floating inputs on CMOS gate.
   (b) Explain how a CMOS device is destroyed.
   (c) What is the difference between transmission time and propagation delay? Explain these two parameters with reference to CMOS logic. [4+4+7]
7. (a) Design a 3-bit LFSR counter using 74×194? List out the sequence assuming that the initial state is 10.
   (b) Design a Modulo-12 ripple counter using 74×74. [8+7]
8. What are passive loop filters in PLL consider the PLL shown in figure 3? [15]

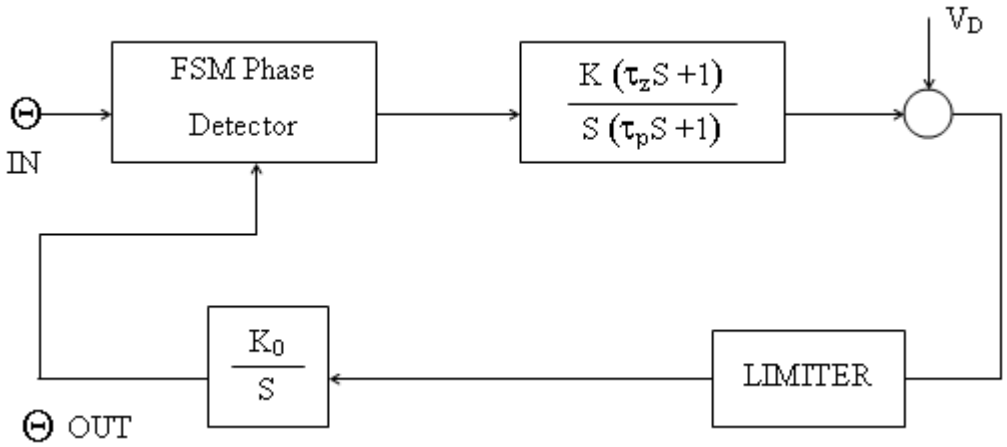

Figure 3

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1. (a) Explain the operation of a Successive Approximation type analog to digital converter.
   (b) Calculate the number of bits required to represent a full scale voltage of 10V with a resolution of 5mV approximately. [10+5]
2. (a) Draw the D flip flop and T flip flop and explain the operation with truth table.
   (b) Draw the J-K flip-flop and explain its operation with truth table. [8+7]
3. (a) Draw the circuits of NAND and NOR gates using CMOS logic and explain their operation with truth tables.
   (b) Compare the performance of various logic families with reference to power dissipation, propagation time delay, Fan in and Fan out. [7+8]
4. (a) Calculate:
      i. maximum output offset voltage caused by the input offset voltage V_{ios}
      ii. maximum output offset voltage caused by the input bias current I_B. For an inverting amplifier with $R_1 = 100\ k\Omega$ & $R_f = 10\ k\Omega$. Here 741 OP-Amp is used with $V_{ios} = 6$ mV $I_B = 500$ nA.
   (b) Draw and explain the practical circuit for offset voltage measurement of OP Amps. [8+7]

5. (a) Write about voltage controlled frequency shifter using 555 timer.
   (b) For the frequency shifter calculate:
      i. The charge current I for input E = OV
      ii. The centre frequency when E = OV
      iii. The frequency shift fout for E = ± 1V. [7+8]

6. (a) Draw the CMOS circuit diagram of tri-state buffer. Explain the circuit with the help of logic diagram and function table.
   (b) Design a CMOS transistor circuit that realizes the following Boolean function. f (a) = $\overline{\left(P+\bar{Q}\right).(Q+R)}$ Also explain its functional operations. [7+8]

7. Design and Second Order IGMF band pass filter with the following specifications. f_O = 500 Hz, gain at resonance = -5 and band width = 50 Hz. Use the circuit shown in figure 4 assume necessary data. [15]

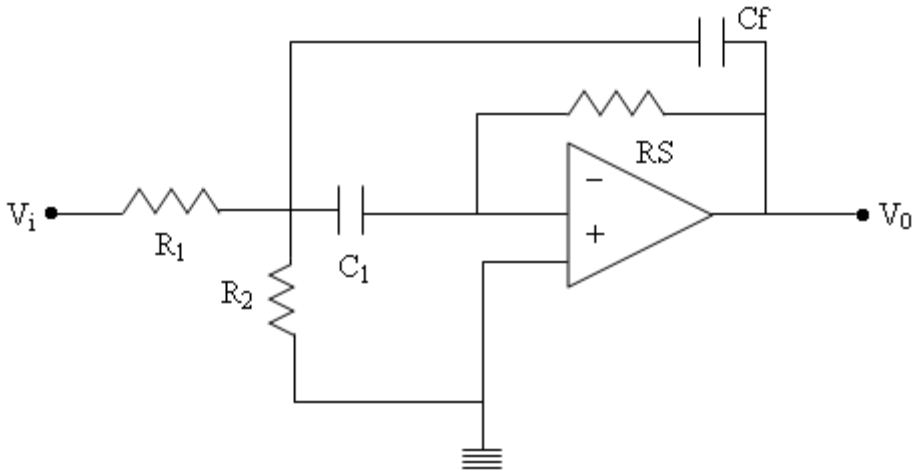

Figure 4:

8. Consider the circuit shown in figure 5.
   (a) Calculate the output voltages of the circuit.
   (b) Explain the effect of C' on stability of the OP-Amp connection. [10+5]

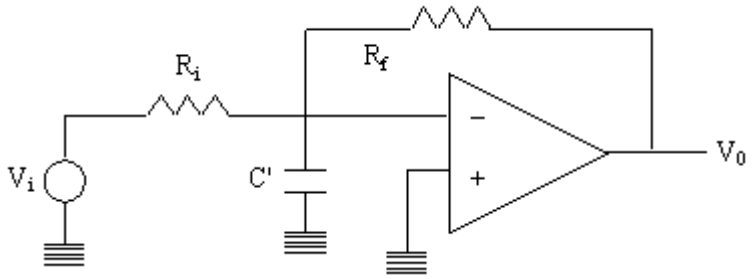

Figure 5

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