Tristate Inverter

Tristate TTL because it allows three possible output states

- High ✓
- Low ✓
- High impedance ✓

Q_3 ON → when o/p high (V_{OH})

Q_4 ON → when o/p low (V_{OL})

High impedance state → Both Q_3 & Q_4 OFF, as a result o/p is open, it is neither High nor Low.

Normal inverter

when Enable input high → normal inverter

diode D_2 open circuited.

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low at Enable forward bias D_2

High impedance state

which shunt current away from base of

when Enable input Low → Q_1 FB (ON), Q_L (OFF)

and Q_4 (OFF)

Q_3, making OFF

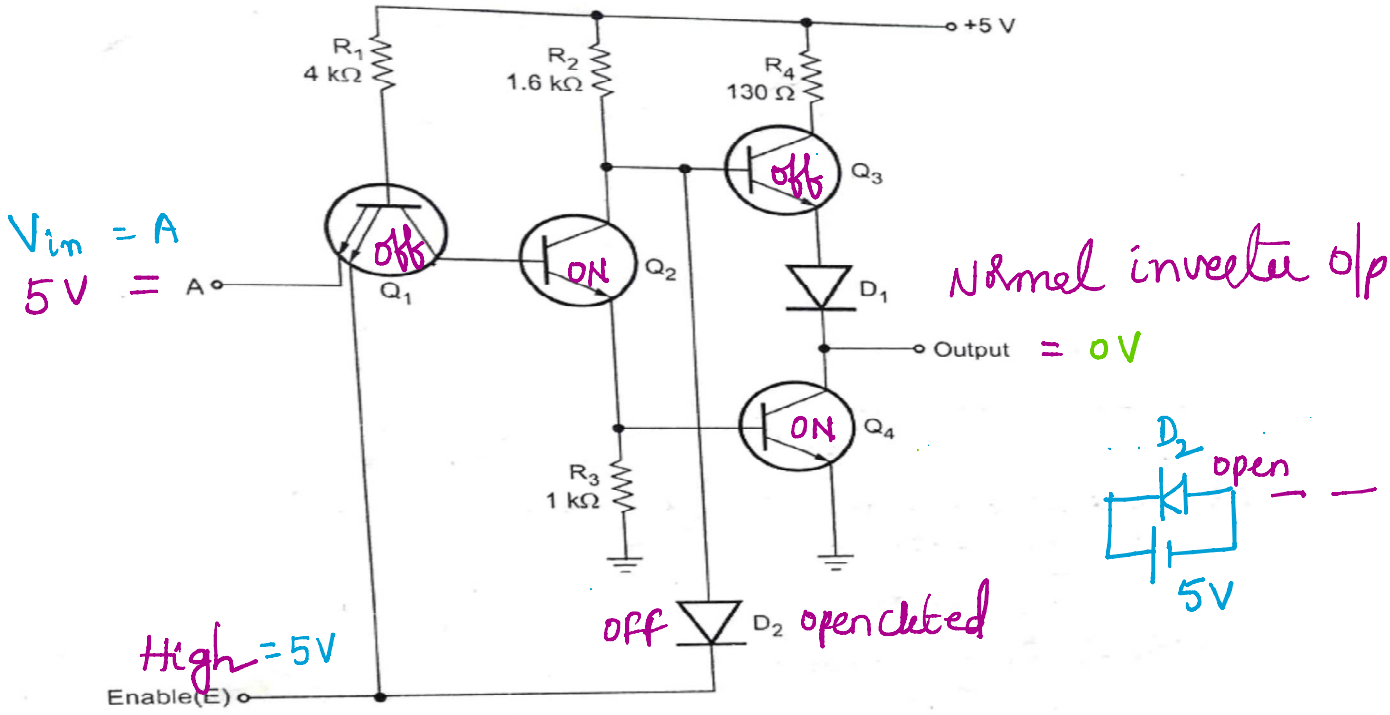

Fig. 7.24 Tristate TTL inverter

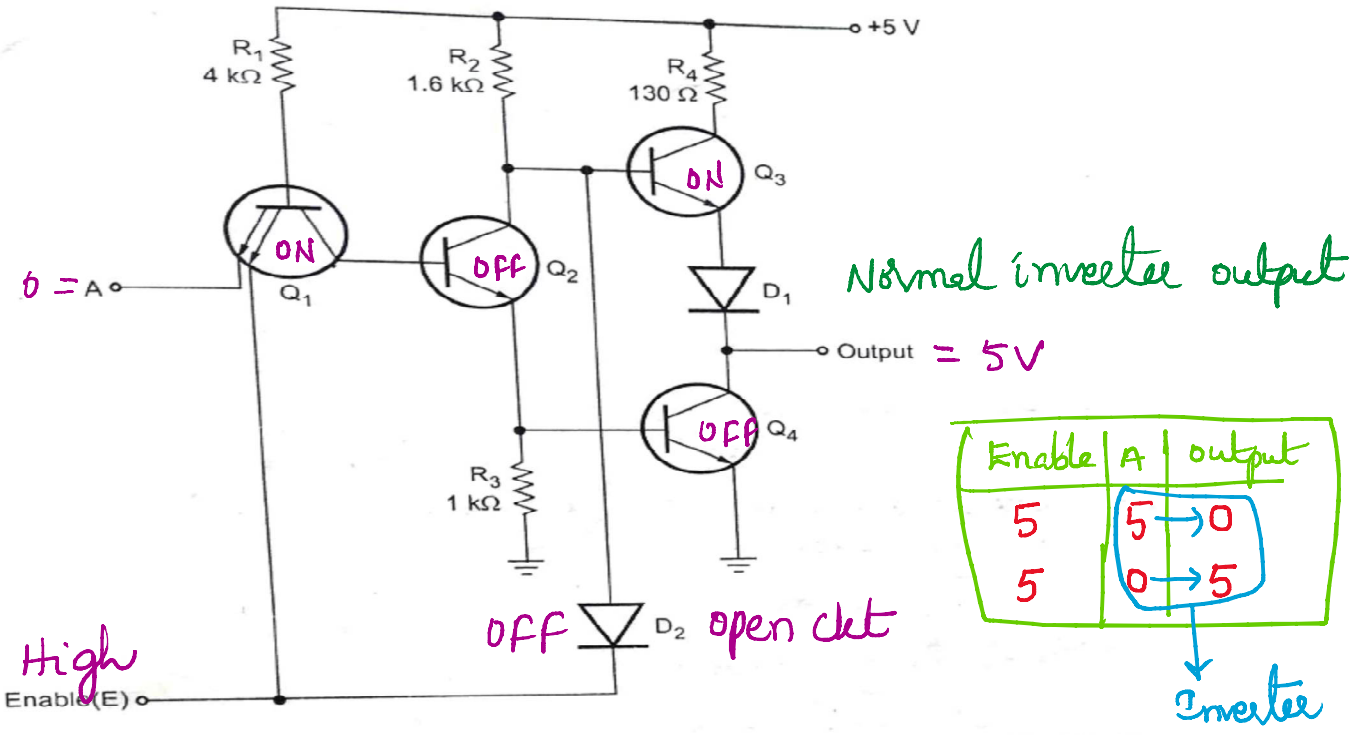

Fig. 7.24 Tristate TTL inverter

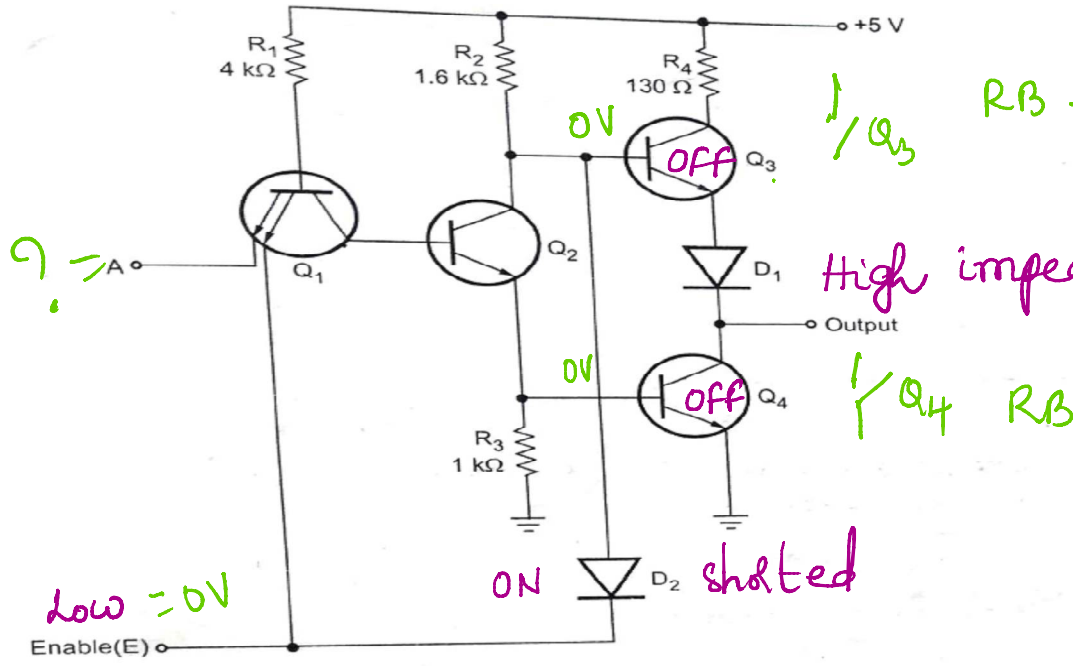

Fig. 7.24 Tristate TTL inverter

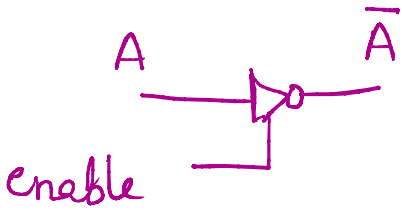

fig: Active high enable inverter

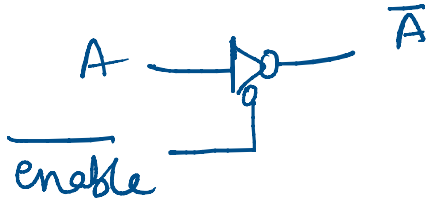

fig: Active Low enable inverter

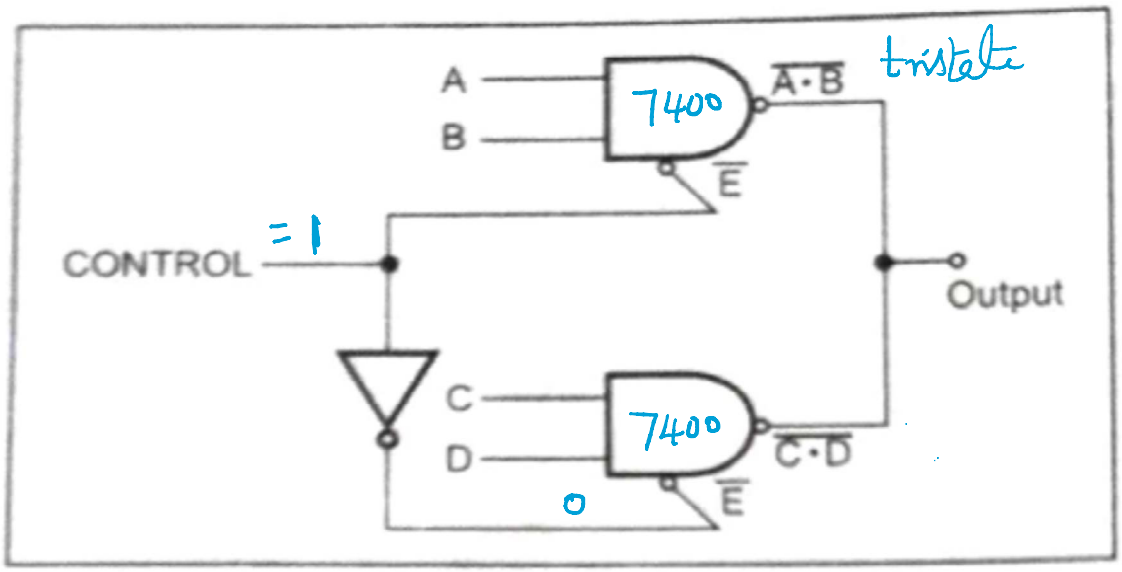

Fig. 7.26 Tristate outputs connected together

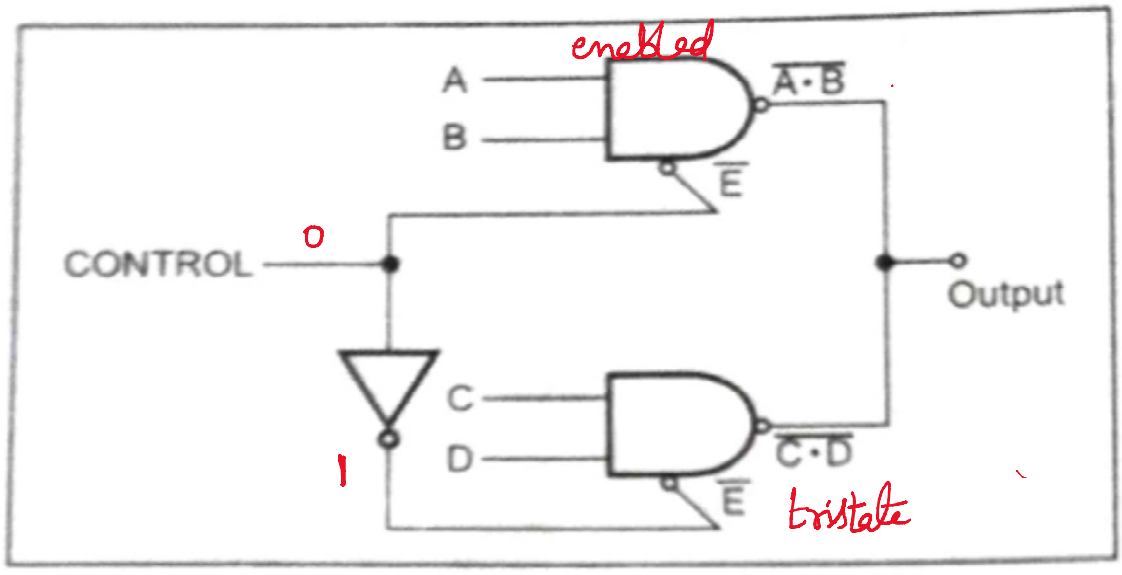

Fig. 7.26 Tristate outputs connected together