

- * one of the most versatile integrated ckt in the 555 IC.
- * Signetics corporation first introduced this device as the SE/NE 555 in early 1970.
- * The device has been used in a number of novel and useful applications.

Applications

- ① Monostable multi
- ② Astable multi
- ③ dc-dc converter
- ④ digital logic probes
- ⑤ waveform generators
- ⑥ analog freq meters
- ⑦ tachometers
- ⑧ temp measurement and control
- ⑨ infrared transmitters
- ⑩ burglar and toxic gas alarms
- ⑪ voltage regulators



- * The 555 is a monolithic timing ckt that can produce accurate and highly stable time delays or oscillation.

- * The Timer basically operates in one of the three modes.

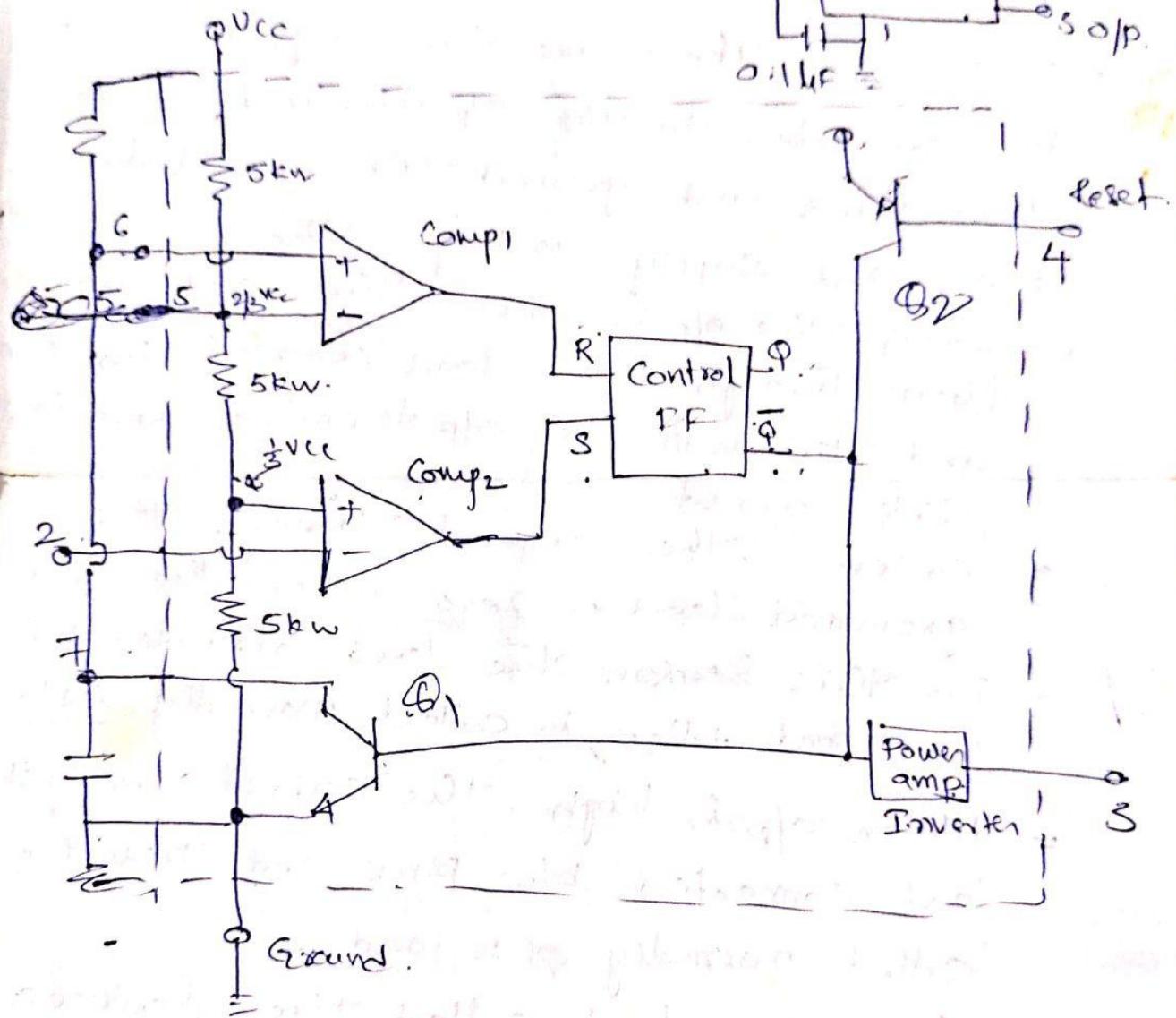
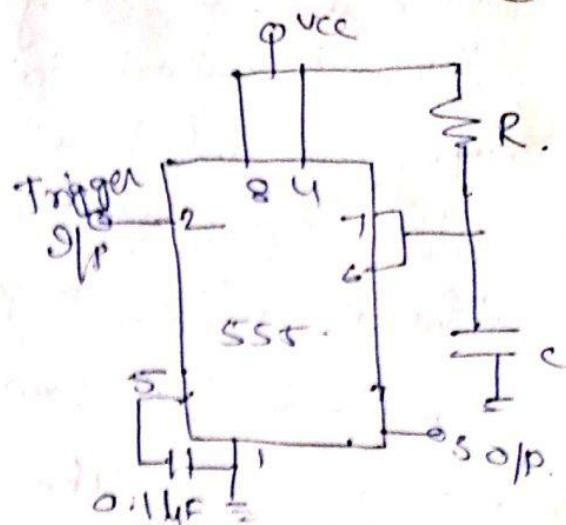
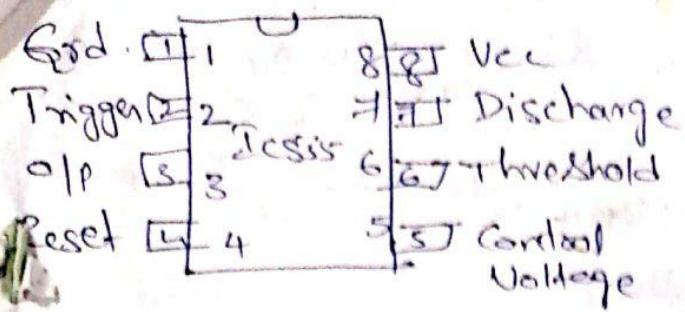
either as monostable (one-shot) mult or an astable mult

The device is available as an 8-pin metal can, and 8-pin mini DIP, or a 14 pin DIP

- * Figure shows the connection dia of NE/SE 555

- * The device is available on an 8-pin metal can, an 8-pin min DIP, or a 14pin Dip.
 - * The 556 timer contains two 555 timers and is a 14-pin DIP.
 - * There is also available counter timer such as Exar's XR-2240 which contains a 555 plus a programmable binary counter in a single 16-pin package.
 - * The SE555 is designed for the operating temp range from -55° to $+125^{\circ}$ C.
 - * While NE555 operates over a temp range of 0° to $+70^{\circ}$ C.
- * ① The important features of the 555 timer are these ; it operates on +5V to +18V supply voltage in free-running (astable) and one shot mode.
- * ② It has adjustable duty cycle.
- * ③ It can sink or source 200mA.
- * ④ The o/p can drive TTL or it is compatible with both TTL and CMOS logic ckt.
- ⑤ Like general purpose op-amp, the 555 is reliable, easy to use and low

(2)



in₁: Ground : All voltages are measured w.r.t this pin.

in₂: Trigger : The o/p of the timer depends on the amp of the external trigger pulse applied to this pin. The o/p is low if the voltage at this pin is greater than 2V_{DD}.

when a -ve going pulse of amp larger than $\frac{1}{3}V_{cc}$ is applied to this pin, the comparators O/P goes low, which in turn switches the O/P of the timer high.

The O/P remain high as long as the trigger terminal is held at a low voltage.

- * Pins. O/P There are two ways a load can be connected to the O/P terminal. either b/w pins 3 and ground (pin 1) or between pins 3 and supply voltage $+V_{cc}$.
 - * When the O/P is low, the load current flows through the load connected b/w pins 3 and $+V_{cc}$ into the O/P terminal and is called sink current.
 - * However, the current through the grounded load is zero when the O/P is high.
 - * For this reason the load connected b/w pins 3 and $+V_{cc}$ is called normally ON load.
 - * When O/P is high, the current through the load connected b/w pins 3 and ground is called normally OFF load.
- * This current is called the source current. The O/P terminal supplies current to the normally off load.
- * This current is called the source current. The maximum value of sink or source current is 200mA.

(5)
In 4 is Reset, the timer can be reset (disabled) by applying a low pulse to this pin. When the Reset function is not in use, this Reset terminal should be connected to +ve via a diode to avoid any possibility of false triggering.

Pins 5: An external voltage applied to this terminal changes the threshold as well as the trigger voltage. By imposing a voltage on this pin or by connecting a pot b/w this pin and ground.

Pins threshold: This is the non inverting input terminal of Comp 1, which monitors the voltage across the external capacitor. The voltage at this pin is \geq Threshold when the voltage at the pin is \geq $\frac{2}{3}V_{cc}$, the o/p of Comp 1 goes high which in turn switches the timer low.

n.7. Discharge: This pin is connected internally to the collector of transistor Q₁. When open, the o/p is high, Q₁ is off and acts as ~~an~~ ckt to the external capacitor connected across it.

When the o/p is low, Q₁ is saturated and acts as a short, shorting external capacitor C to ground.

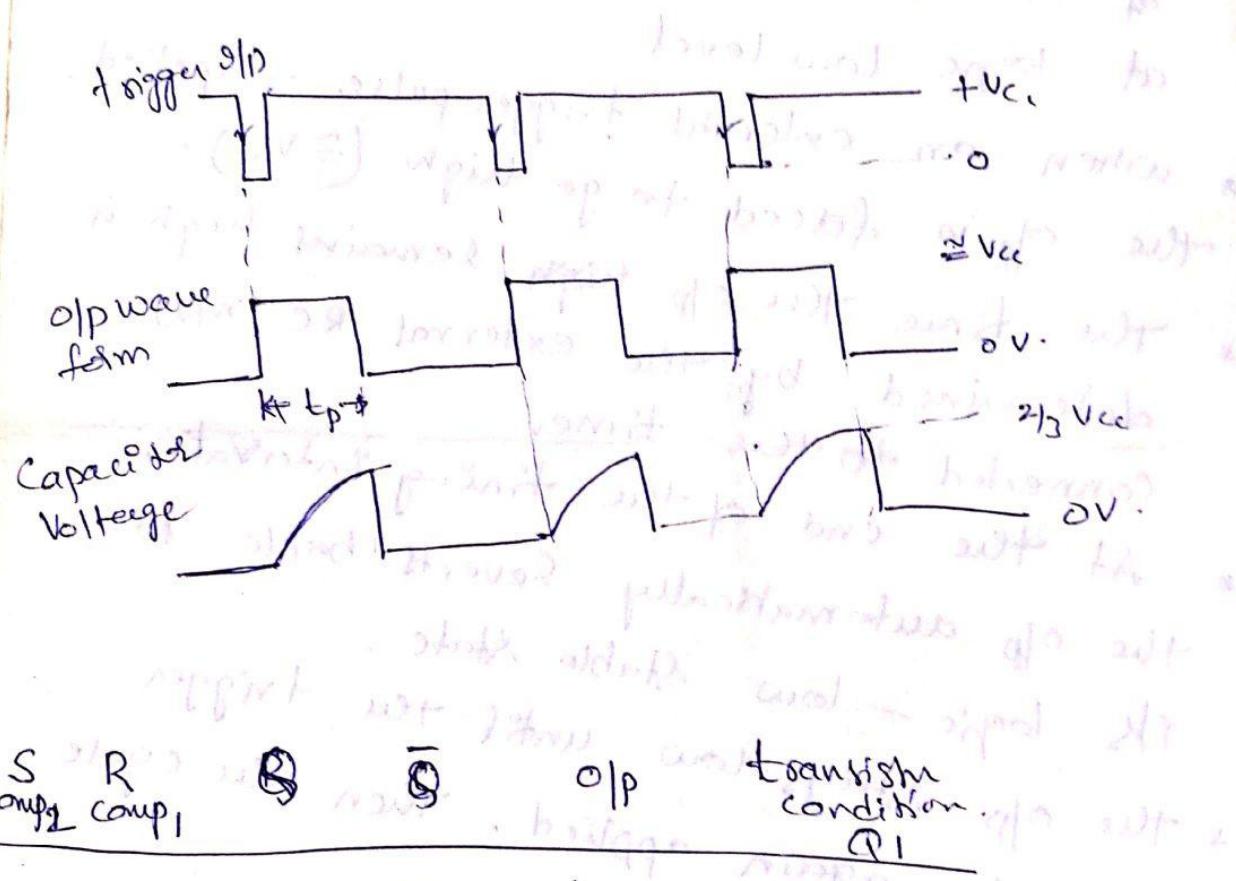
8: +U_{cc} The supply voltage of +5V to +18V

Applied to this pin w.r.t. to ground.

Monostable operation. :- (One shot multivibrator)

- * It is a pulse generating ckt in which duration of the pulse is determined by the RC network connected externally to the 555 timer.
- * In a stable or stand-by state the o/p of the ckt is approximately zero. or it is logic-low.
- * When an external trigger pulse is applied, the o/p is forced to go high ($\approx V_{CC}$).
- * The time the o/p remains high is determined by the external RC network connected to the timer.
- * At the end of the timing interval, the o/p automatically reverts back to its logic-low stable state.
- * The o/p stays low until the trigger pulse is again applied.
- * Then the cycle repeats.
- * The monostable ckt has only one stable state (o/p low), hence the name monostable.
- * Normally, the o/p of the monostable multivibrator is low.

Initially when the o/p is low, i.e. the ckt is in a stable state, transistor Q₁ is on and the capacitor C is shorted out to ground. However on the application of a negative trigger pulse on to pin 2, transistor Q₁ is turned off, which releases the short across the external capacitor C and drives the o/p high.



S	R	\bar{Q}	o/p	transistor condition
comp ₂	comp ₁			Q ₁
Low	High	Low	High	Low
High	Low	Low	High	ON

The capacitor 'C' now starts charging up toward V_{cc} through R_A.

However, when the voltage across the capacitor equals $2/3 V_{CC}$, comp 1's output goes from low to high, which in turn drives the op to its low state via the o/p of the flip flop.

At the same time, the o/p of the flip flop turns transistor Q₁ ON, and hence capacitor C rapidly discharges through the transis-

- * Following the monostable remains low until a triggered pulse is again applied, then the cycle repeats.

* The pulse width of the trigger input must be smaller than the expected pulse width of the flip flop waveform.

* The trigger pulse must be a full going o/p signal with an amplitude larger than $\frac{1}{3} V_{CC}$.

~~The time during the o/p remaining high given by~~

$$V_C = V_{CC} \left(1 - e^{-t/R_C}\right)$$

If we At $t = t_p$ $V_C = 2/3 V_{CC}$

$$\frac{2}{3} V_{CC} = V_{CC} \left(1 - e^{-t_p/R_C}\right)$$

$$-\frac{t_p}{R_C} = \ln \frac{1}{3}$$

$$e^{-t_p/R_C} = 1 - \frac{2}{3} = \frac{1}{3}$$

$$t_p = 1.1$$

The voltage across the capacitor is given by.

$$V_c = V_{cc} \left(1 - e^{-t/Rc} \right)$$

At $t = t_p$ $V_{ce} = \frac{2}{3} V_{cc}$

$$\frac{2}{3} V_{cc} = V_{cc} \left(1 - e^{-tp/Rc} \right)$$

$$tp = 1.1 R_c$$

* The timing interval is independent of the supply voltage.

* Once triggered, the o/p remains in the high state until time T_p elapses.

which depends upon R and C .

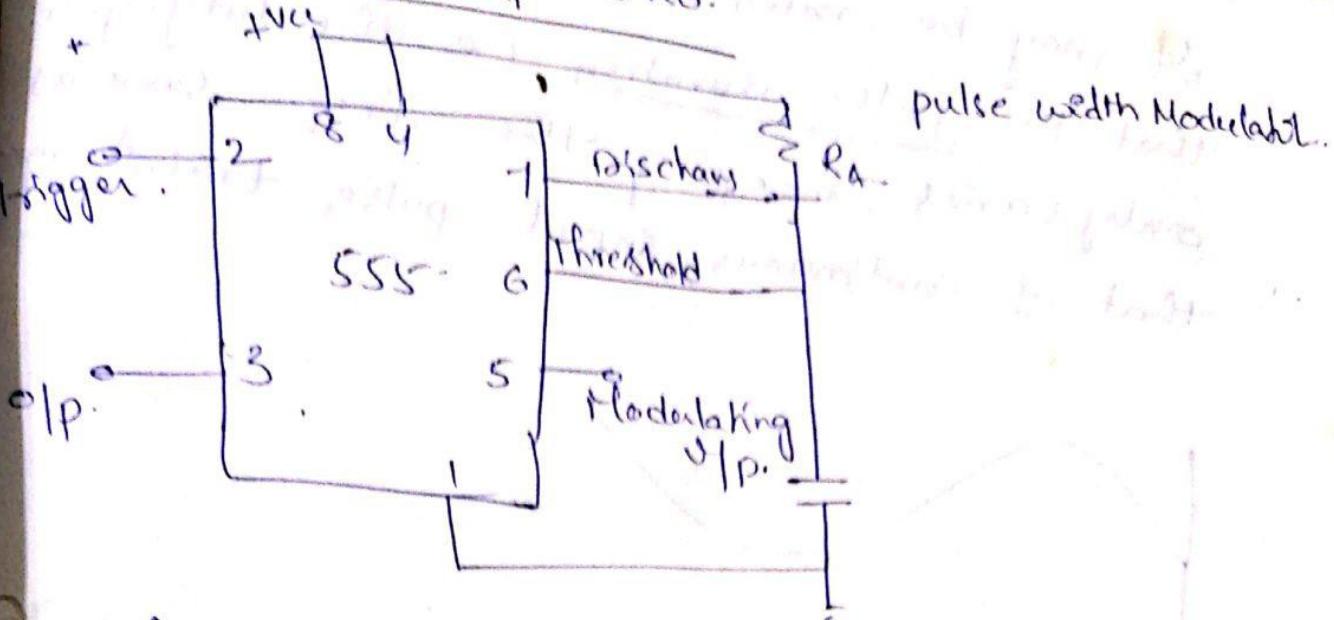
Any additional trigger pulse coming during this time will not change the state of the o/p.

* If a $-ve$ going pulse is applied to the set terminal of Q_1 , it will reset the o/p.

shown in fig is applied to the timing cycle, during the timing cycle, Q_2 goes off, Q_1 becomes on and the capacitor C is immediately discharged. The o/p returns to ground potential.

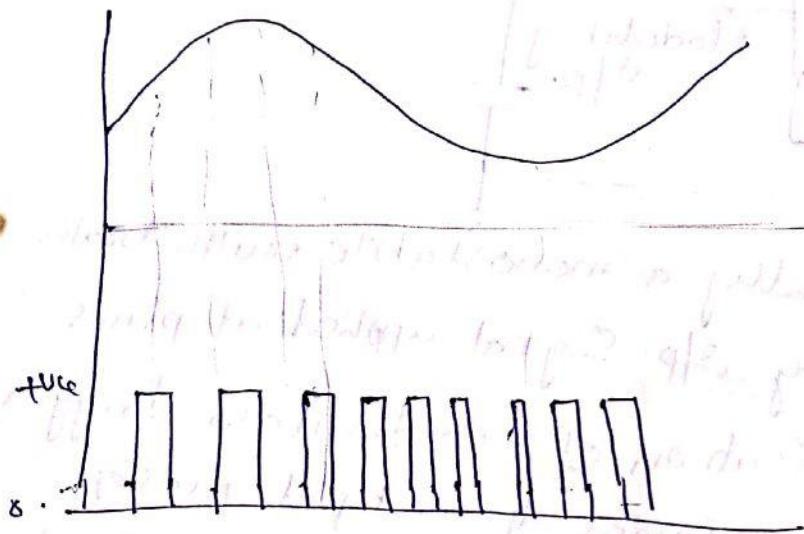
Even if the set is cleared, the o/p will still remain low until a $-ve$ going trigger pulse is again applied at pin 2.

Applications of Mono. Multivibrator



- * This is basically a monostable multivibrator with modulating S/p Signal applied at pin-5.
- * By the application of continuous trigger at pin 2, a series of output pulses are obtained, the duration of which depends on the modulating S/p at pin-5.
- * The modulating signal applied at pin-5 gets superimposed upon already existing voltage $\frac{2}{3} V_{cc}$ at the inverting S/p terminal of UC. This in turn changes the threshold level of UC and the output pulse width modulation takes place.
- * The Modulating Signal and the S/p waveform are shown in Fig.

It may be noted from the op wave form that the pulse duration i.e. the duty cycle only varies, keeping the freq same, that of continuous input pulse train.

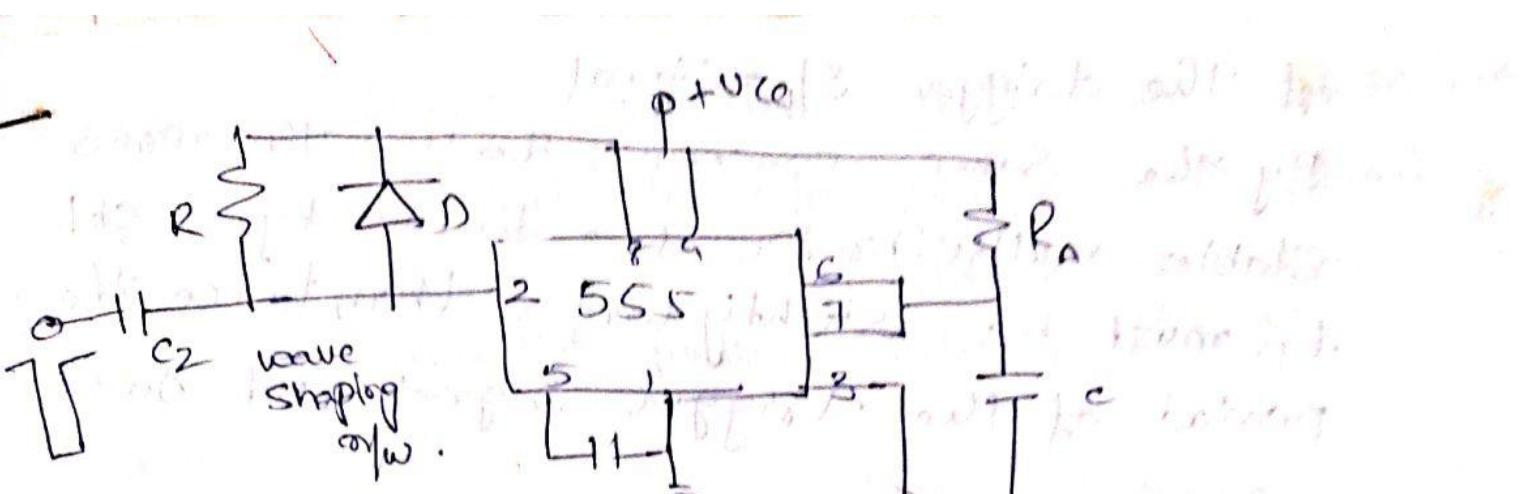


pulse width Modulated waveform

② frequency divider.

The Monostable multi can be used as a freq. divider by adjusting the length of the timing cycle t_p with respect to the time period T of the trigger dip signal applied to pin 2.

- * To use the monostable multivibrator as a divide-by-2 ckt, the timing internal t_p must be slightly larger than the time period T of the trigger dip signal



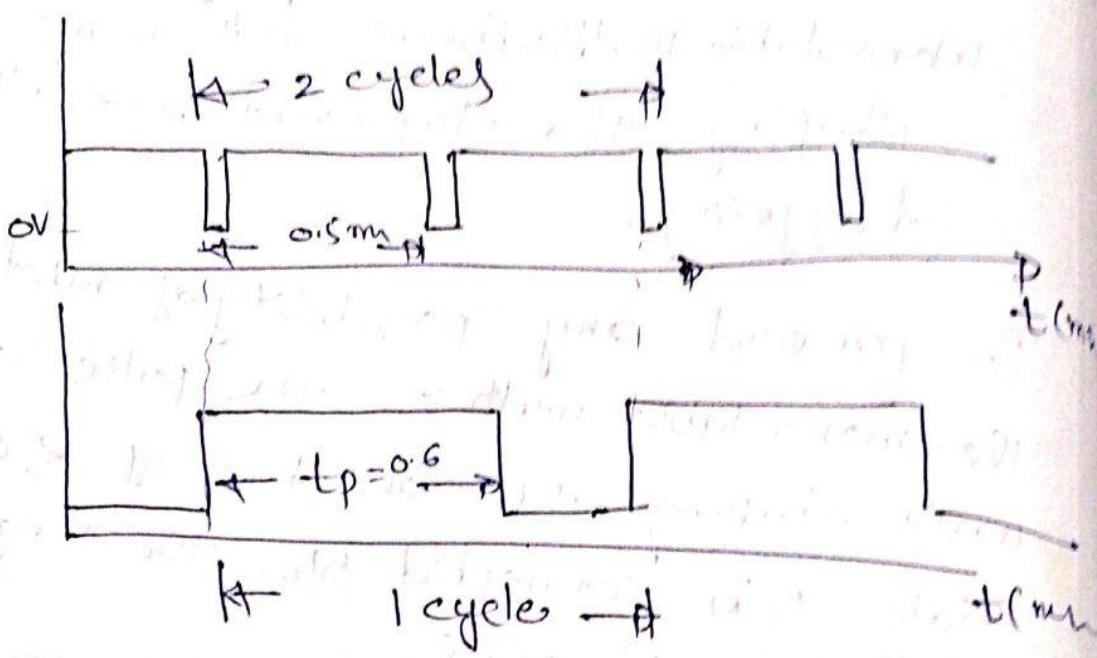
Monostable Multivibrator with wave shaping m/w to prevent +ve pulse edge triggering.

To prevent any possibility of mistriggering the monostable multivibrator pulse edges, a wave shaping ckt consisting of R, C_2 and diode D is connected b/w the trigger I/p pin 2 and V_{CC} pin 8.

* The values of R and C_2 should be selected so that the time constant RC_2 is smaller than the o/p pulse width t_p .

of the trigger Op signal

By the same concept, we use the mono-stable multivibrator as a divide-by-3 cell. t_p must be slightly larger than twice the period of the trigger signal and so,



Op and $\text{O}'\text{p}$ wave forms of mono stable

Multi as a divide-by-2 m/w.

prob.

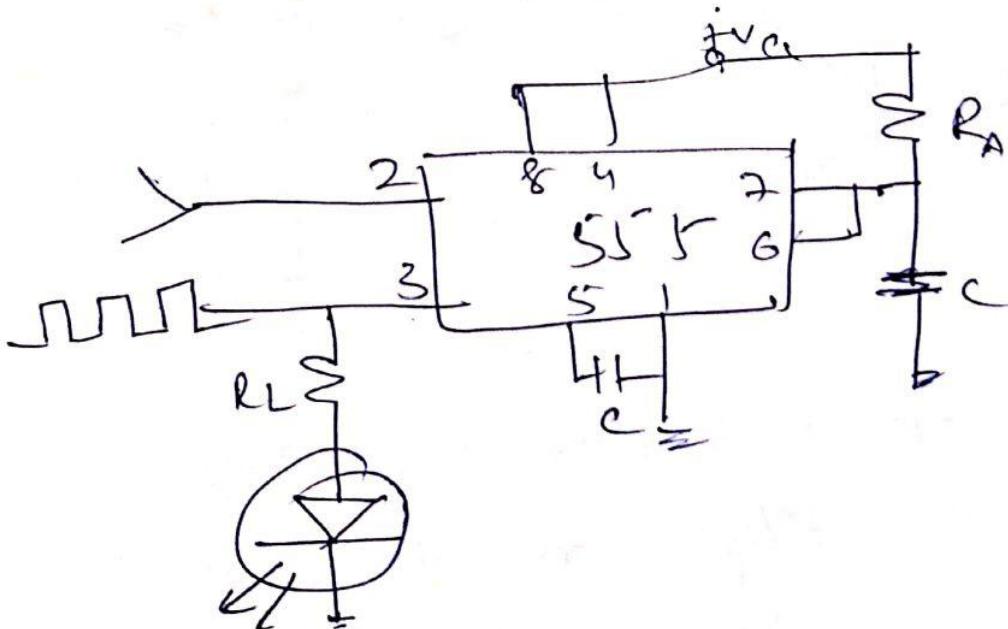
The ckt shown in the fig is to be up a divide-by-2 m/w. The freq of the Op signal is 2kHz . If the value of $C = 0.01\mu\text{F}$, what should be the value of R ?

Pulse Stretcher : This application makes use of the fact that the O/P pulse width (timing interval) of mono is of longer duration than the negative pulse width of the S/I trigger.

As such the O/P pulse width of mono can be viewed as a stretched version of the narrow S/I pulse. Hence the name pulse stretcher.

- * often narrow-pulse width signals are not suitable for driving an LED display mainly because of their very narrow pulse widths. The LED may be flashing but is not visible to eye because its on time period is small compared to its off time.

The 555 pulse stretcher can be used to remedy this problem

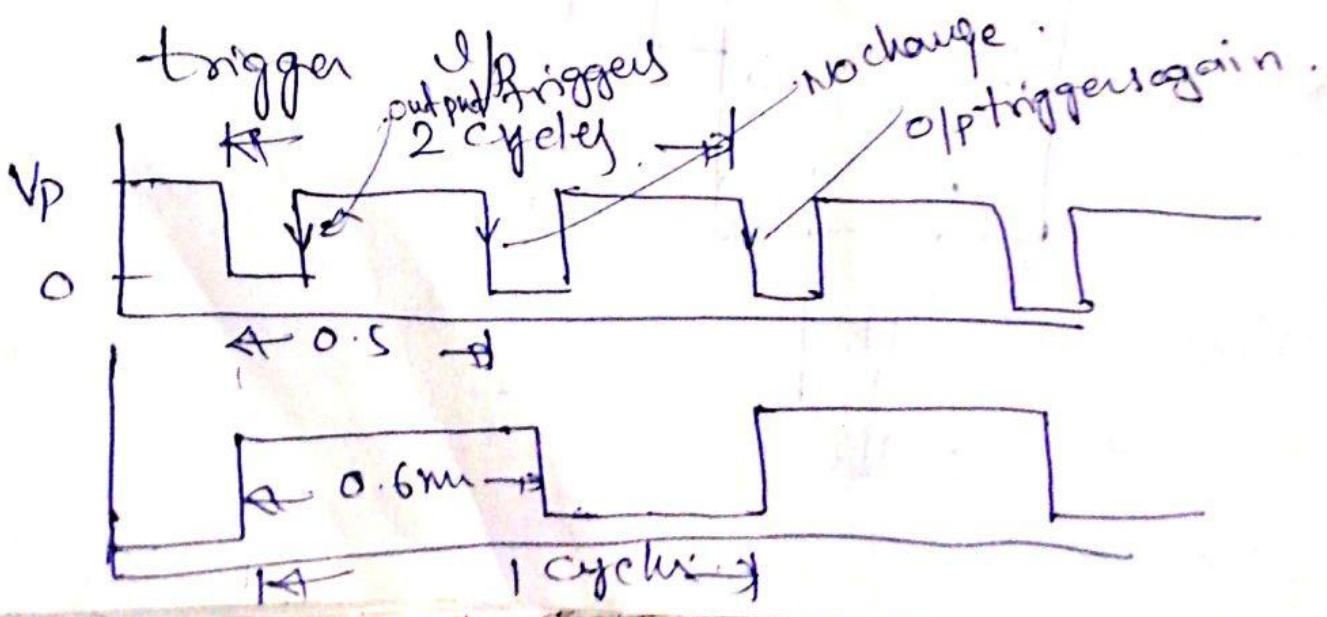


10k_{on} 100k_{on} 1M_{on} 10n 10n 10n 10n 10n

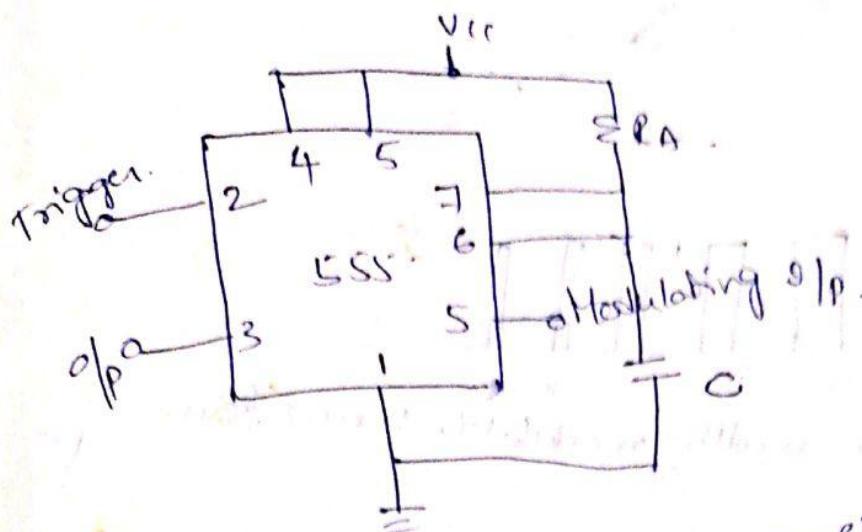
Mono stable multivibrator app

Freq divider, it can be used as freq divider by adjusting the length of timing cycle t_p wrt time period T_{op} of the trigger I/p signal applied to pin 2.

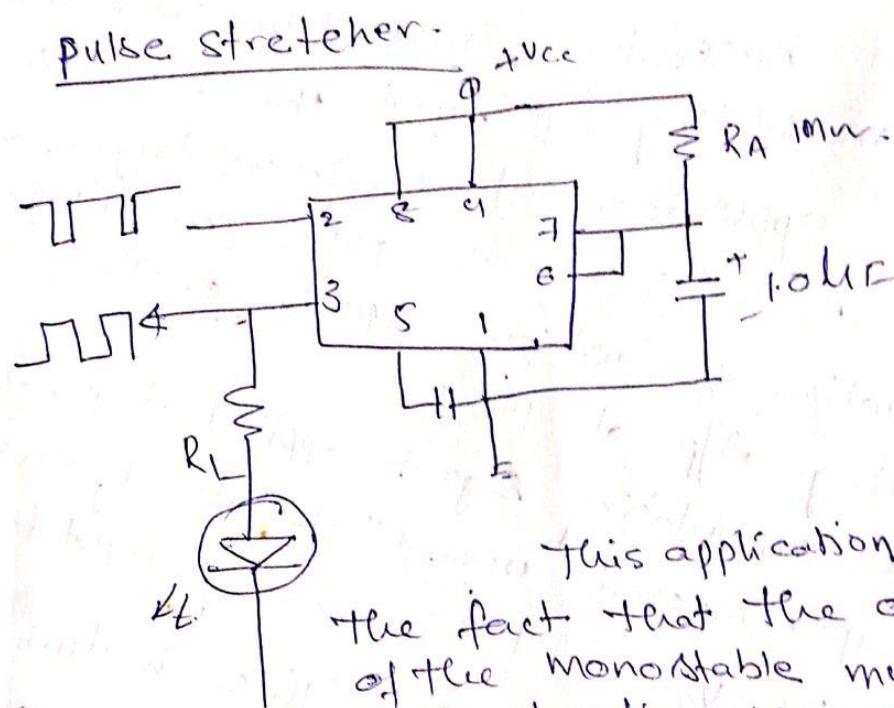
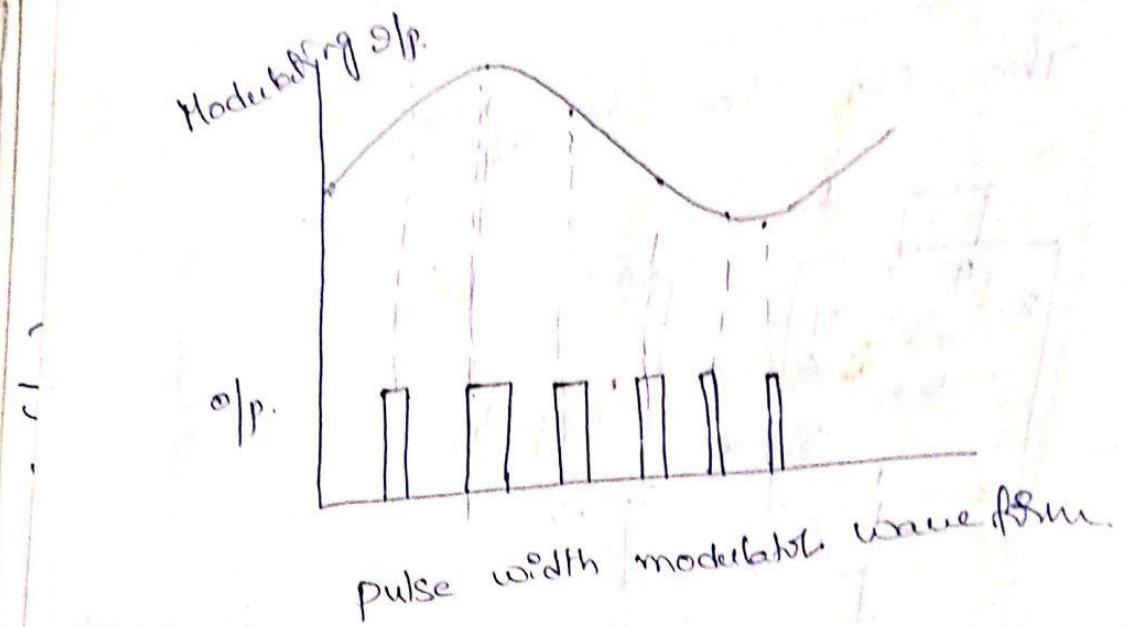
To use it as a divide-by-2 clk the timing interval t_p must be slightly larger than the time period T_{op} of the trigger I/p signal.



The ckt shown in Fig (c).



This is basically a monostable multivibrator with a modulating S/p signal applied at pin-5. By the application of continuous trigger at pin-2, a series of o/p pulses are obtained, the duration of which depends on the modulating S/p at pin-5. The modulating signal applied at pin-5 gets superimposed upon the already existing voltage $(\frac{2}{3}) V_{cc}$ at the inverting input terminal of the upper comparator. This in turn changes the threshold level of the o.c. and of the upper compensation. This in turn changes the width modulation of the o/p waveform. The modulating signal and the o/p waveform are shown in Fig. It may be noted from the o/p waveform that the pulse duration i.e. the duty cycle only varies, keeping the freq. same as that of the continuous S/p pulse train triggered at pin-2.



This application makes use of the fact that the o/p pulse of the monostable multivibrator is longer duration than the width of the S/p trigger. As such the o/p pulse width of the monostable multivibrator can be viewed as a stretched version of the narrow S/p pulse, hence the name pulse stretcher.

Narrow-pulse width signals are not suitable for driving an LED display mainly because of their very narrow pulse widths. The LED may be flashing but is not visible to the eye because its on time is infinitesimally small compared to its off time.

① Design a monostable multivibrator using 555 timer to produce a pulse width of 100ms. Verify the values of R and C obtained from the graph.

② The monostable multivibrator is used as a divide-by-3 network. The freq. of the S/I trigger is 15 kHz. If the value of C = $\frac{9.6}{+000} \mu F$, calculate the value of resistor R.

$$t_p > 2T$$

$$t_p = 1.2 (2T)$$

$$= 1.2 (2) (15) \times 10^3$$

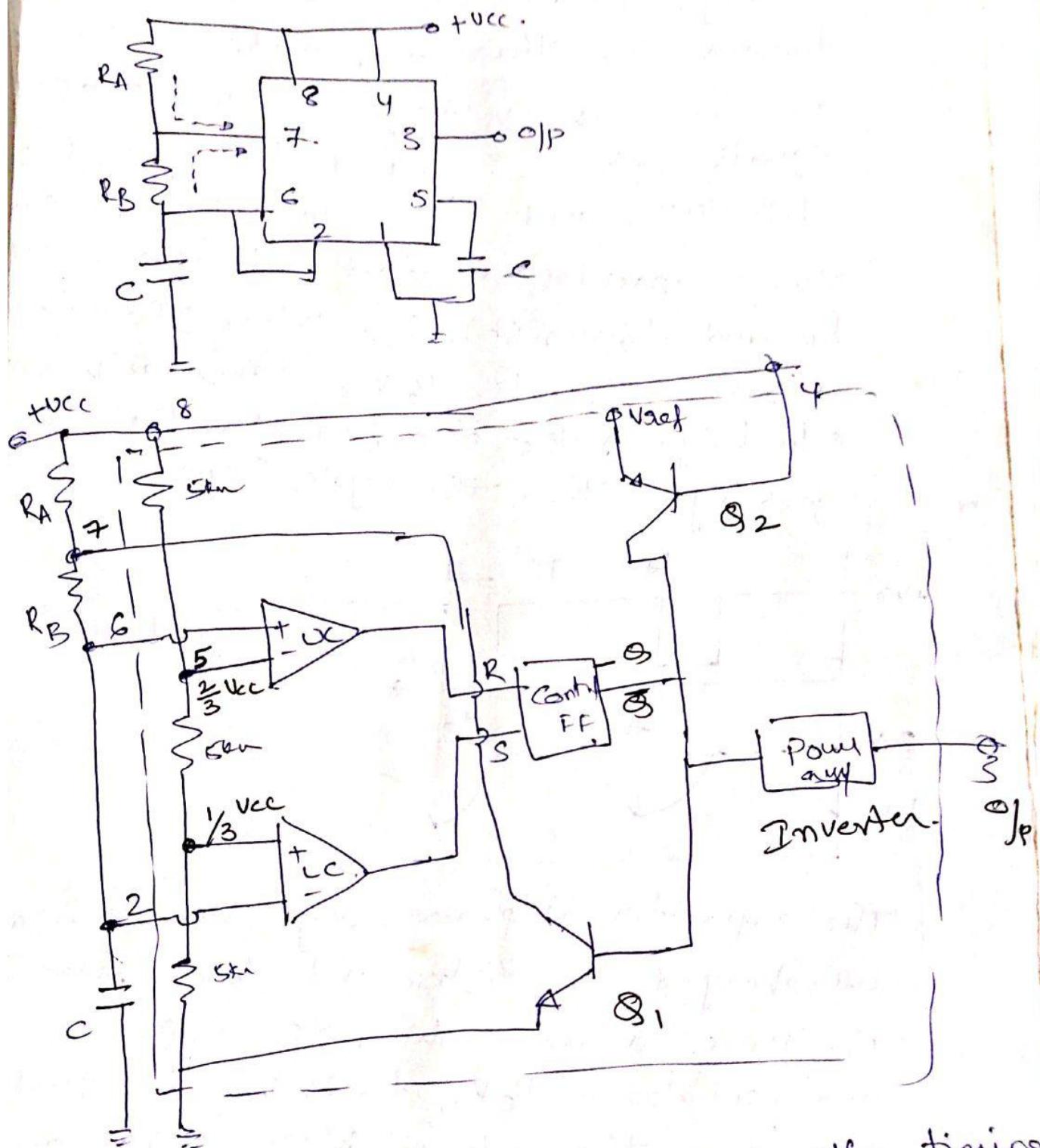
$$= 1.2 \times 30 \times 10^3$$

$$\boxed{t_p = \underline{\underline{36 \text{ kHz}}}}$$

$$t_p = 1.1 \times R \times C$$

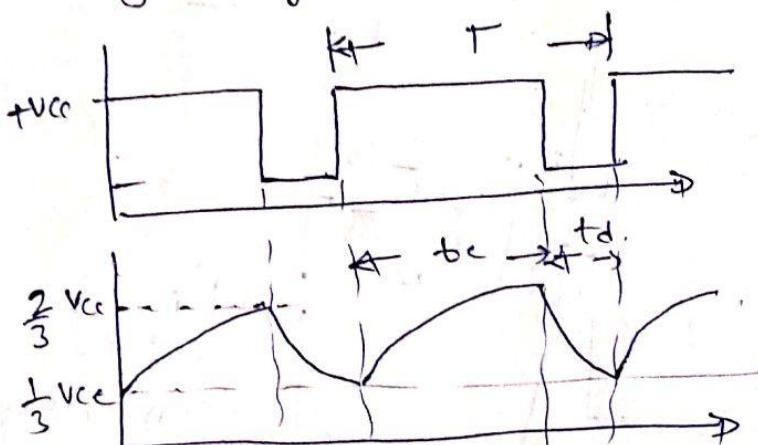
$$R = \frac{36 \times 10^3}{0.01 \times 10^{-6}}$$

Astable operation



Comparing with mono stable operation, the timing resistor is now split into two sections R_A and R_B . Pin 7 of discharge transistor Q_1 is connected to the junction of R_A and R_B .

* Initially assumed that o/p of multivibrator is in high state. capacitor starts charging towards V_{CC} through R_A and R_B . As soon as voltage across the cap equals $\frac{2}{3}V_{CC}$, comp 1 triggers the flip-flop, and the o/p switches low. Now capacitor C starts discharging thru R_B and transistor Q_1 . When the voltage across C equals $\frac{1}{3}V_{CC}$ comparator 2's o/p triggers the flip-flop and the o/p goes high. Then the cycle repeats.



The capacitor is periodically charged and discharged b/w $\frac{2}{3}V_{CC}$ and $\frac{1}{3}V_{CC}$. The time during which the capacitor changes from $\frac{1}{3}V_{CC}$ to $\frac{2}{3}V_{CC}$ is equal to the time the o/p is high and is given by

$$t_C = 0.69 (R_A + R_B) C$$

The time during which the capacitor discharges from $\frac{2}{3}V_{CC}$ to $\frac{1}{3}V_{CC}$ is equal to the time the o/p is low and is given by

$$t_d = 0.69 (R_B) C$$

$$T = L_C + t_d = 0.67 (R_A + 2R_B) C$$

$$f_0 = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B) C}$$

leaving the
0/p in high

$$\frac{L_C}{T} = \frac{R_A + R_B}{R_A + 2R_B}$$

In the astable multivibrator $R_A = 2.2 \text{ k}\Omega$, $R_B = 3.9 \text{ k}\Omega$,
 and $C = 0.1 \mu\text{F}$. Determine the positive pulse width t_p and
 negative pulse width t_n and free running frequency.

The capacitor voltage for a low pass
RC ckt subjected to a step I/P of

V_{cc} voltage is given by

$$V_c = V_{cc} (1 - e^{-t/RC})$$

The time t₁ taken by the ckt to charge from
0 to $\frac{2}{3} V_{cc}$ is.

$$\frac{2}{3} V_{cc} = V_{cc} (1 - e^{-t_1/RC})$$

$$t_1 = 1.09 RC$$

and the time t₂ to charge from 0 to $(\frac{1}{3})V_{cc}$

$$\frac{1}{3} V_{cc} = V_{cc} (1 - e^{-t_2/RC})$$

$$t_2 = 0.405 RC$$

So the time to charge from $\frac{1}{3} V_{cc}$ to $\frac{2}{3} V_{cc}$

is

$$t_{HIGH} = t_1 - t_2$$

$$= 1.09 RC - 0.405 RC$$

$$= 0.69 RC$$

So for the given ckt

$$t_{HIGH} = 0.69 (R_A + R_B) C$$

period $T = t_{ON} + t_{OFF}$.

$$D\% = \frac{R_A + R_B}{R_A + 2R_B} \times 100.$$

$$f = \frac{1}{T} = \frac{1}{0.69(R_A + 2R_B)C} = \frac{1.45}{(R_A + 2R_B)C}$$

$$f = \frac{1.45}{(R_A + 2R_B)C}$$

The op is low while the capacitor discharges from $\frac{2}{3} V_{cc}$ to $\frac{1}{3} V_{cc}$ and voltage across the capacitor is given by

$$\frac{1}{3} V_{cc} = \frac{2}{3} V_{cc} e^{-t/RC}$$

$$t = 0.69 R C.$$

for the given ckt

$$t_{low} = 0.69 R_B C$$

Notice that both R_A and R_B are in the charge path but only R_B is in the discharge path.

\therefore the total time

$$T = t_{high} + t_{low}$$

$$T = 0.69 (R_A + 2R_B) C$$

$$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B) C}$$

The duty cycle D of a ckt is defined as the ratio of ON time to the total time

period $T = t_{ON} + t_{OFF}$

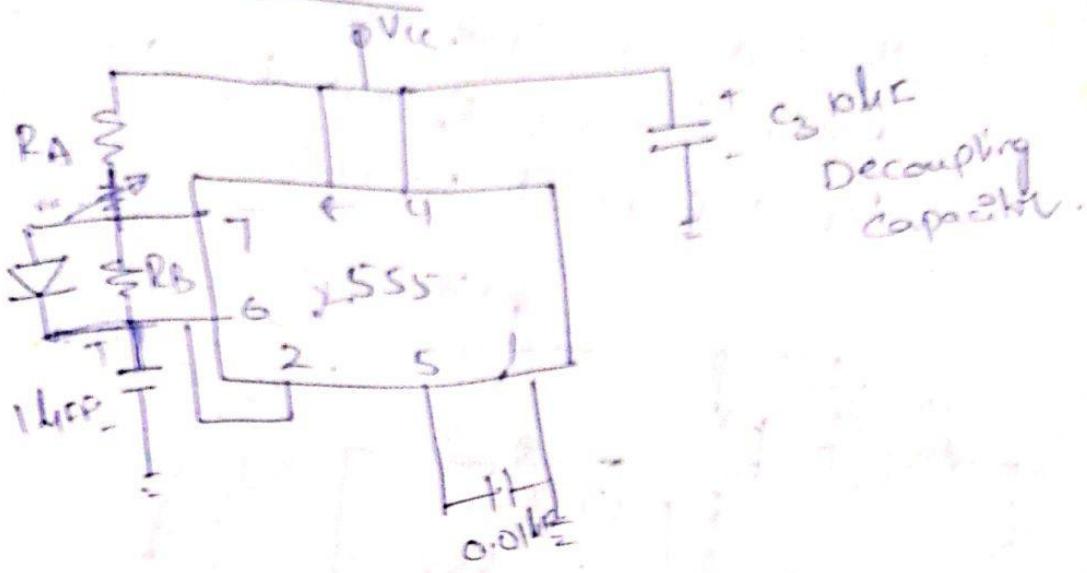
$$D\% = \frac{R_A + R_B}{R_A + 2R_B} \times 100$$

$$f = \frac{1}{T} = \frac{1}{0.69(R_A + 2R_B)C} = \frac{1.45}{(R_A + 2R_B)C}$$

$$f = \frac{1.45}{(R_A + 2R_B)C}$$

Applications of Astable Multivibrator.

① Square wave gen.



with out reducing $R_A = \infty$, the astable multivibrator can be used to produce a squarewave o/p simply by connecting diode D across resistor R_B . The capacitor C charges through R_A and diode D to approximately $\frac{2}{3} V_{cc}$ and discharge through R_B and terminal 7 until the capacitor voltage equals approximately $\frac{1}{3} V_{cc}$ then the cycle repeats.

To obtain a square wave o/p (50% duty cycle) R_A must be a combination of a fixed resistor and potentiometer so that the potentiometer can be adjusted for the exact square wave.

During the charging portion of the cycle, diode D₁ is forward biased effectively short circuiting R_B so that

$$t_{\text{high}} = 0.69 R_A C$$

During discharging portion of the cycle transistor S₁ becomes ON, thereby grounding pin 7 and hence the D₁. D₁ is reverse biased

$$t_{\text{low}} = 0.69 R_B C.$$

$$T = t_{\text{high}} + t_{\text{low}} = 0.69 (R_A + R_B) C.$$

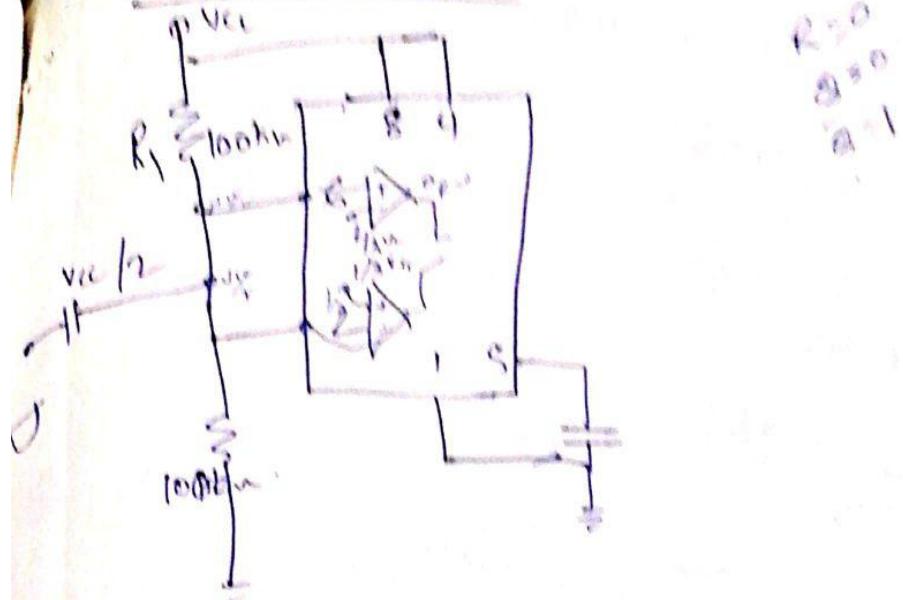
$$f = \frac{1.45}{(R_A + R_B)C}$$

and duty cycle

$$D = \frac{R_B}{R_A + R_B}$$

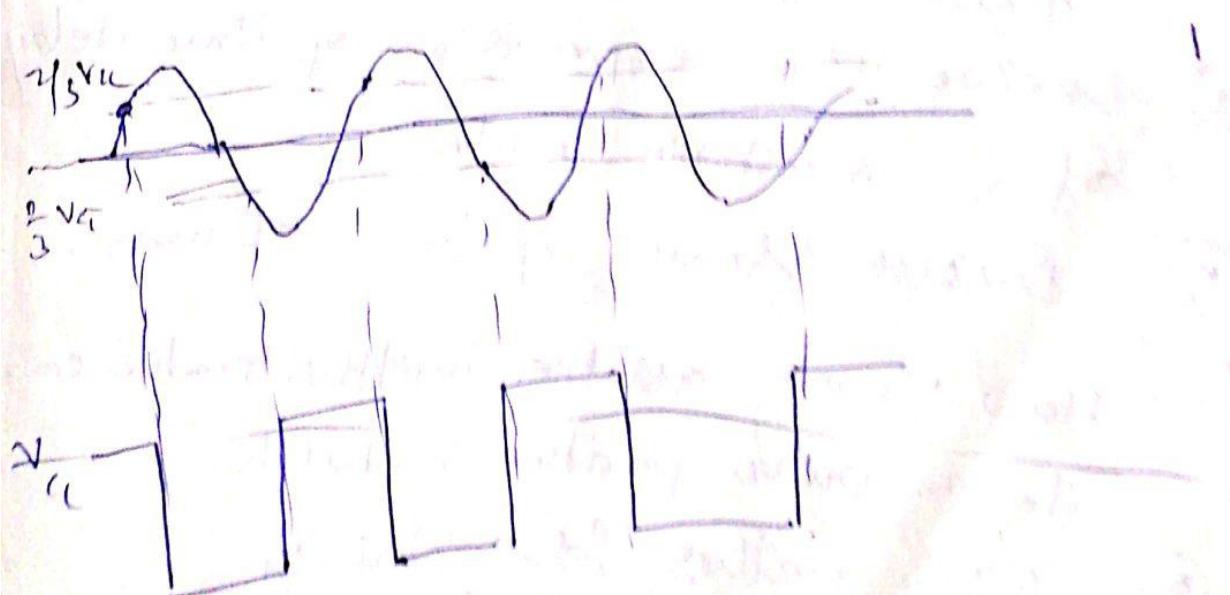
Resistors R_A and R_B could be made variable to allow adjustment of freq and pulse width. A series resistor of at least 100Ω should be added to each R_A and R_B. If R_A made equal to R_B the 50% duty cycle is achieved.

Schmitt trigger



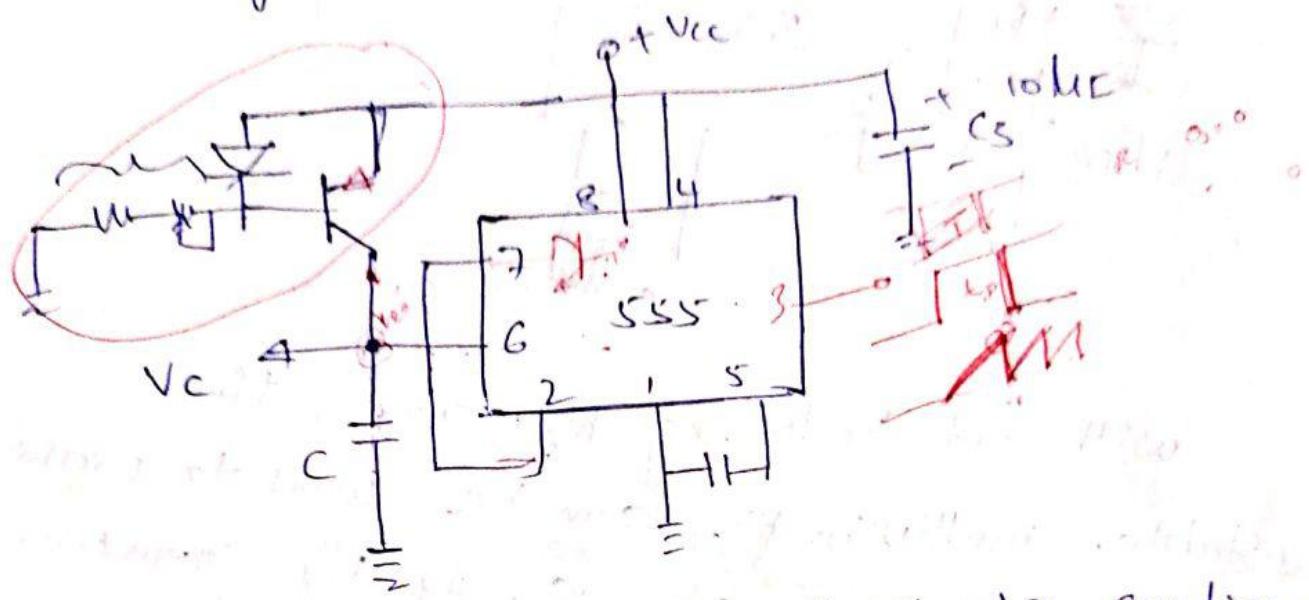
The two internal comparators are tied together and externally biased at $\frac{V_{cc}}{2}$ through R_1 and R_2 . Since the upper comparator will trip at $\frac{2}{3}V_{cc}$ and lower comparator at $\frac{1}{3}V_{cc}$ the bias provided by R_1 and R_2 is centered with in these two thresholds.

Thus a sine wave of sufficient amp > $\frac{V_{cc}}{6}$ ($\frac{2V_{cc}}{3} - \frac{V_{cc}}{2}$) to exceed the reference levels causes the internal flip-flop to alternately set and reset, providing a square wave of fm.



② Free-running ramp generator

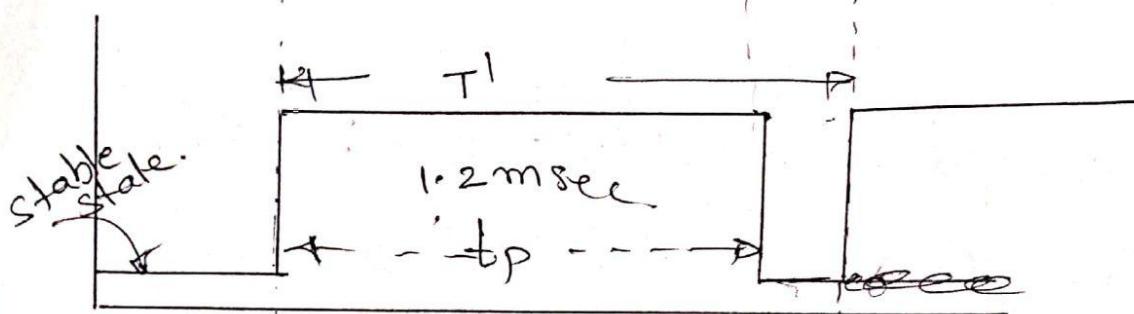
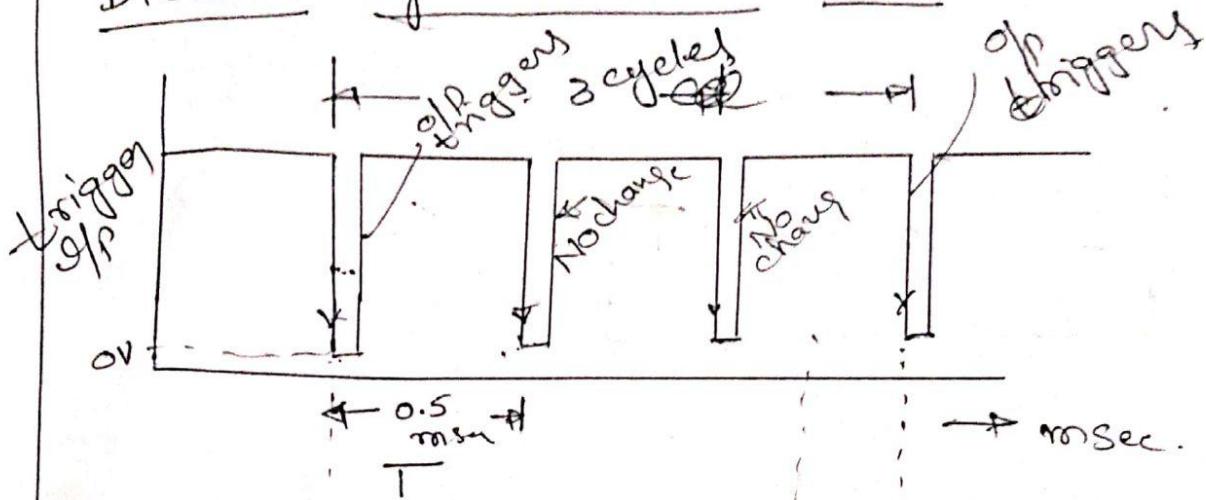
The astable multivibrator can be used as a free running ramp gen when resistors R_A and R_B are replaced by a current mirror.



Show an astable multivibrator configured to perform this function.
 This current mirror starts charging capacitor C toward V_{CC} at a constant rate.
 When voltage across C equals $2/3 V_{CC}$, Comp 1 turns transistor Q_1 on, and C rapidly discharges through transistor Q_1 . However, when the discharge voltage across C is app.

①

Divide - By - three circuit



$$t_p > 2T$$

Op Frequency is
 ~~$f = 1/T$~~ $f = 2 \text{ KHz}$
 $T = 0.5 \text{ msec}$

choose $t_p = (1.2)(2T)$. $= 0.96 \text{ msec}$

$$= (1.2)(2)(0.5)(10^{-3})$$

$t_p = 1.2 \text{ msec}$

T_1 is the op wave form time period.

To design Now take $t_p = 1.2 \text{ msec}$

choose $C = 0.01 \mu F$

$$t_p = 1.1RC$$

cd R $\therefore R = \frac{t_p}{1.1 \times C} = \frac{1.2 \times 10^{-3}}{1.1 \times 0.01 \times 10^{-6}}$

$$R = 10^9 \text{ k}\Omega$$

(2)

So to design Divide by 'n'

circuit we have to choose, gear
stable state time period

$$t_p > (n-1)T$$

(2)

The monostable multivibrator is used as a divide-by-3 network.

The frequency of the Ip trigger is 15 kHz. If the value of $C = 0.01 \mu F$. cal the value of resistance R .

$$t_p > 2T$$

$$f = 15 \text{ kHz}$$

$$T = \frac{66}{66} \text{ msec}$$

$$t_p = (1.2)(2)(66) \times 10^{-3}$$

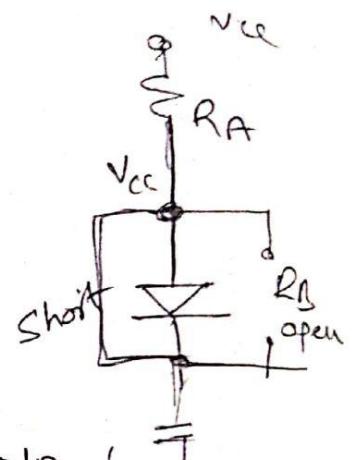
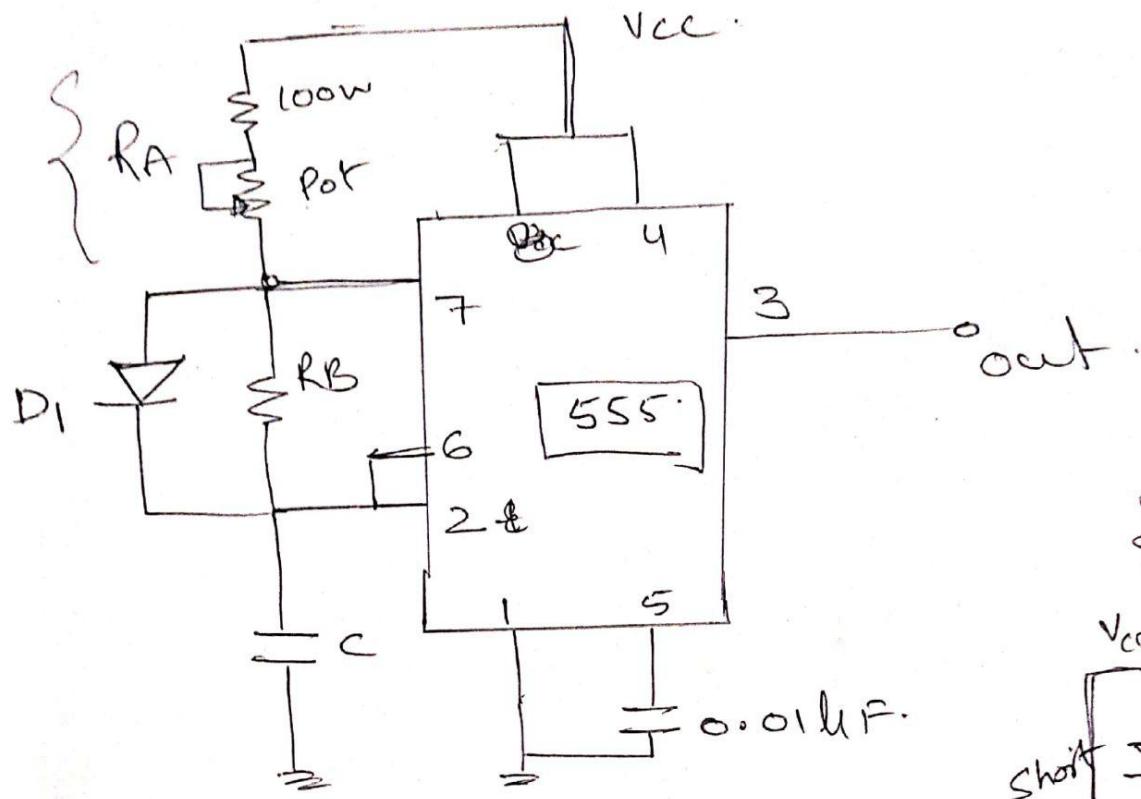
$$t_p = \underline{\hspace{2cm}}$$

$$t_p = 1.1 \times R \times C$$

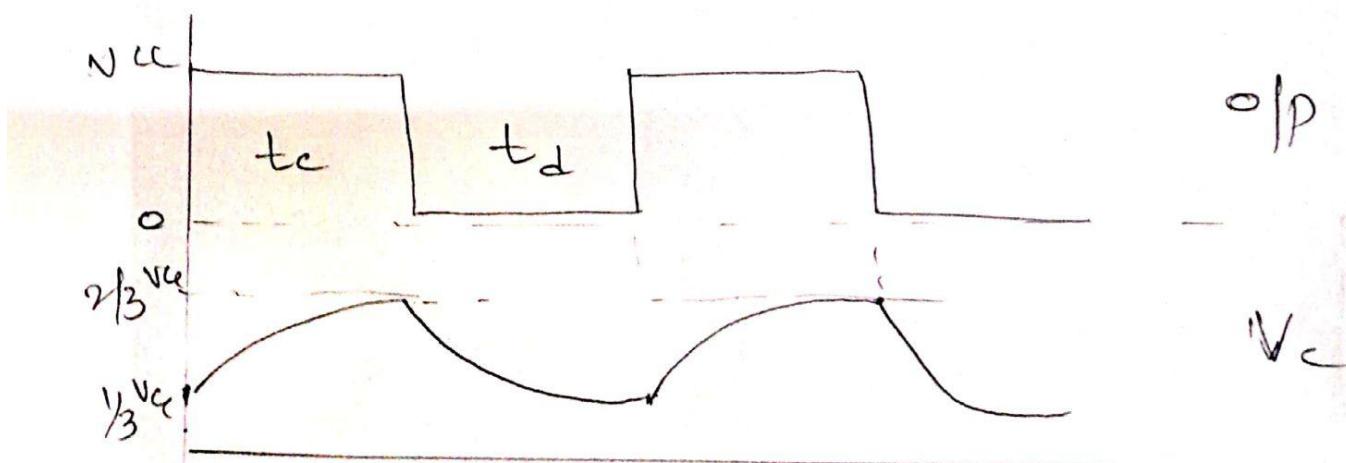
$$R = \frac{t_p}{1.1 \times 0.01 \mu F} = \underline{\hspace{2cm}}$$

(3)

Square wave generator.



A	7 pin.	Q_1	O/P
(short) ON.	$\approx V_{cc}$	OFF	1
(open) OFF	≈ 0	ON	0



$$t_c = 0.69 R_A C \quad (4)$$

$$t_d = 0.69 R_B C$$

$$T = t_c + t_d = 0.69 (R_A + R_B) C$$

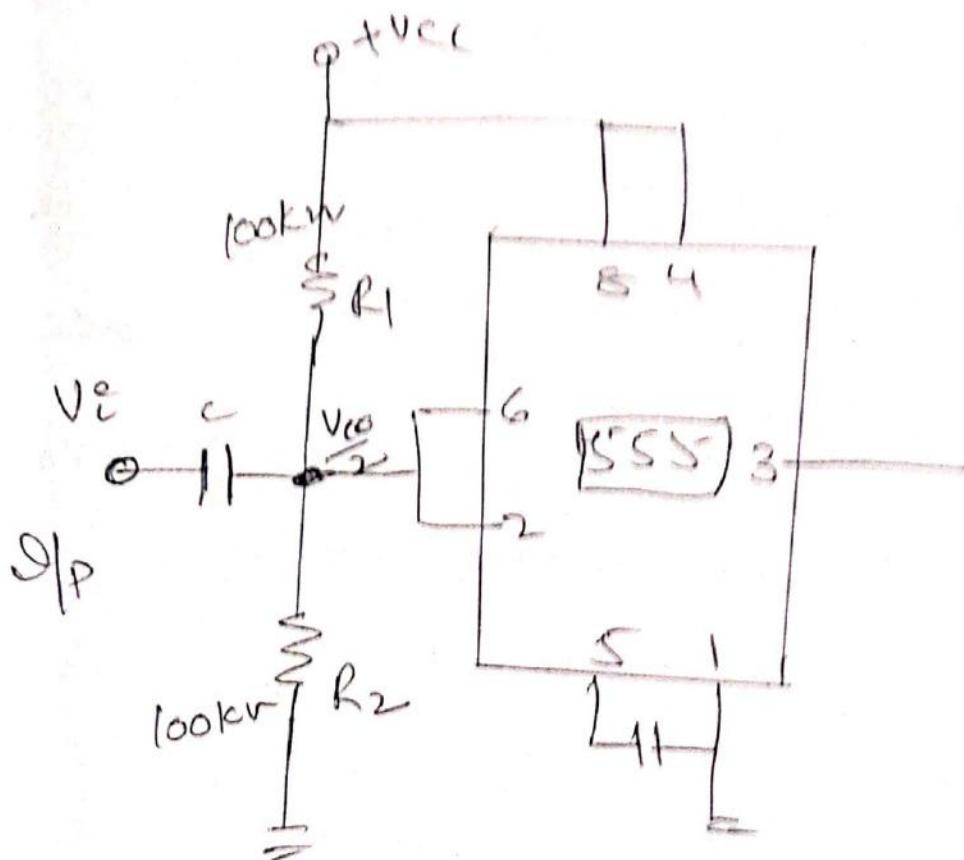
$$f = \frac{1.45}{(R_A + R_B) C}$$

and duty cycle = $\frac{R_B}{R_A + R_B}$

if R_A is made equal to R_B

then 50% duty cycle is
achieved.

Schmitt trigger.



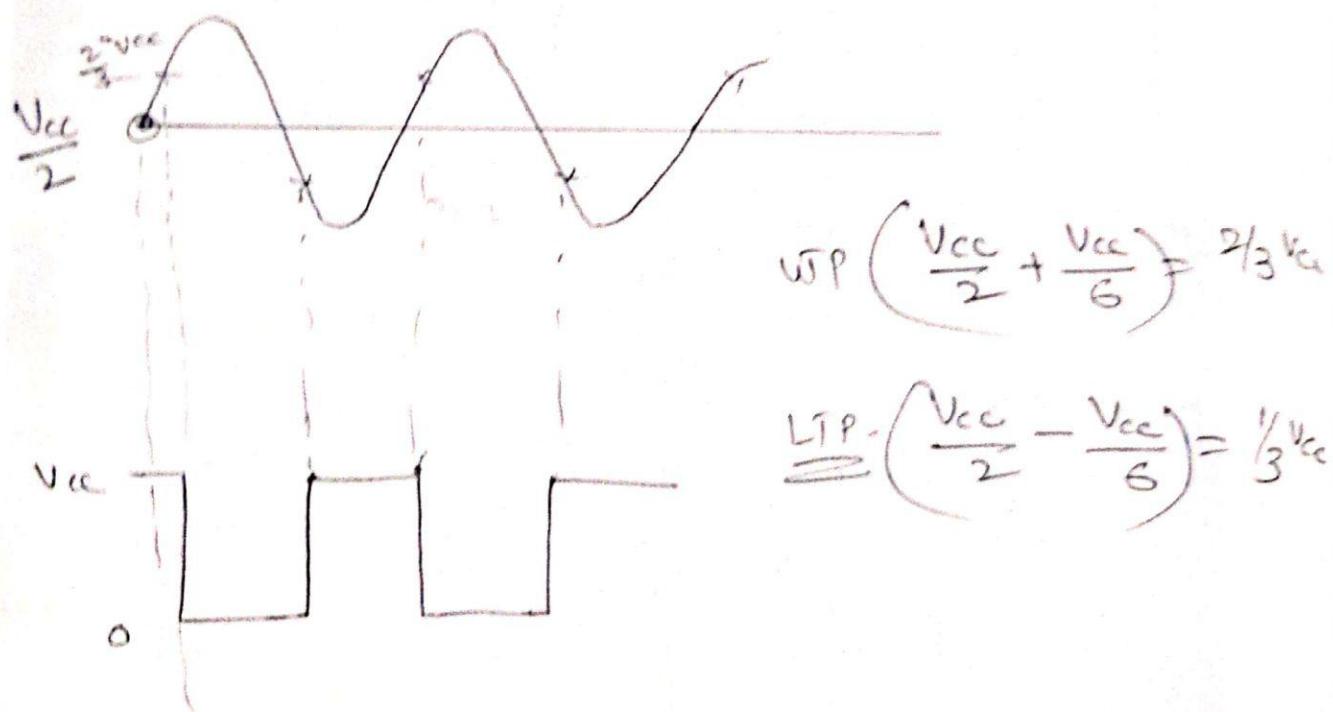
The two internal comparators are tied together and externally biased at $\frac{V_{cc}}{2}$ through R_1 and R_2 .

Since the upper comparator will trip at $(\frac{2}{3}) V_{cc}$ and lower comparator at $(\frac{1}{3}) V_{cc}$ the bias provided by R_1 and R_2 is centered with in these two thresholds.

Thus a sine wave of sufficient amplitude ($>\frac{V_{cc}}{6} = \frac{2}{3}V_{cc} - \frac{V_{cc}}{2}$)

to exceed the Ref levels causes the internal op to alternately set and reset, providing a square wave o/p.

No freq division is taking place and freq of square wave remains the same as that of Ipp signal.

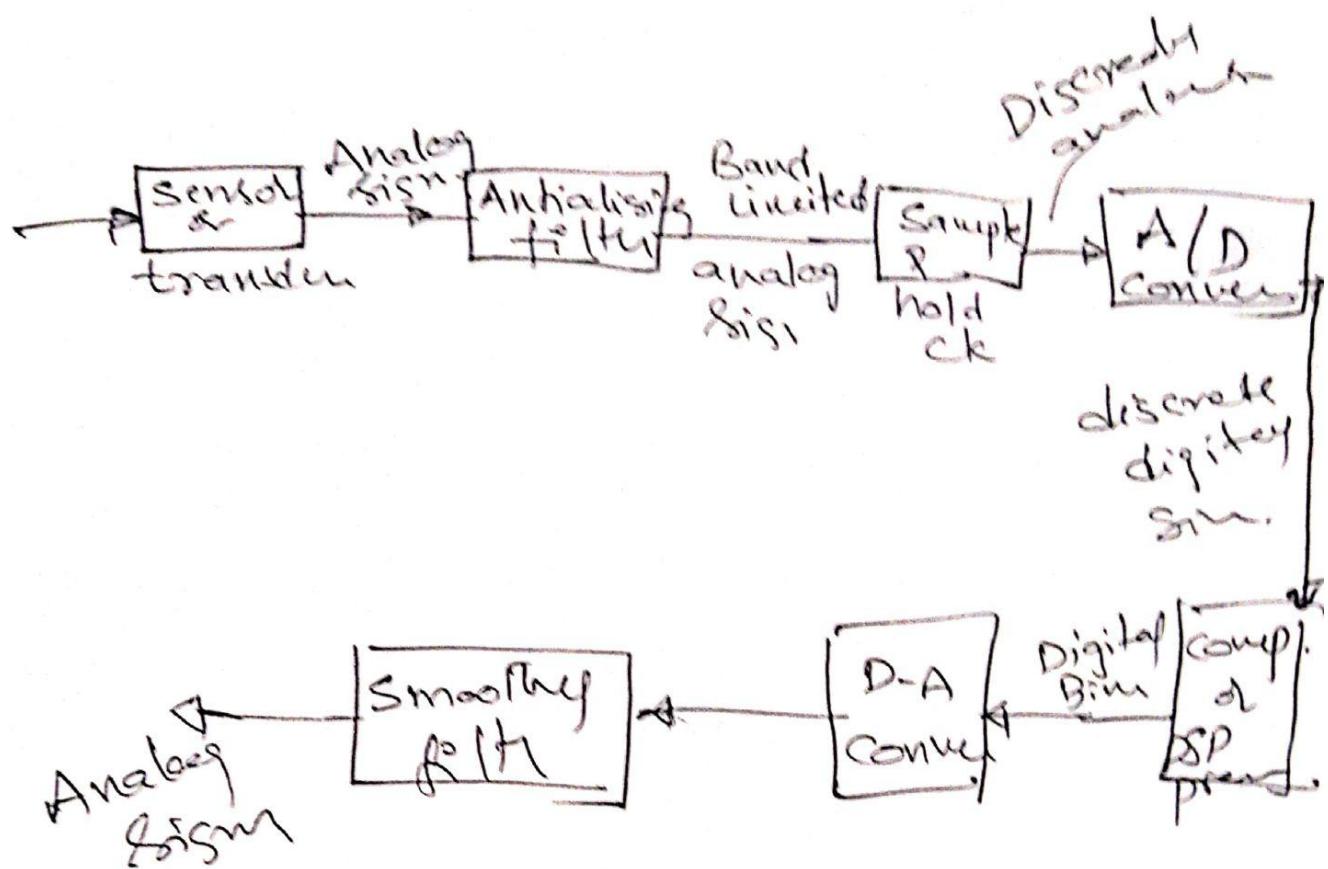


$$V_{IP} \left(\frac{V_{cc}}{2} + \frac{V_{cc}}{6} \right) = \frac{2}{3}V_{cc}$$

$$V_{LP} \left(\frac{V_{cc}}{2} - \frac{V_{cc}}{6} \right) = \frac{1}{3}V_{cc}$$

Ipp and o/p waveform of Schmitt trigger.

D-A AND A-D converters.



Applications of A/D and D/A

Conver.

①

Basic DAC Technique.

The schematic of DAC is shown in Fig. The input is an n -bit binary word D and is combined with a ref. voltage V_R to give an analog o/p signal. The o/p of a DAC can be either a voltage or current. For a voltage output DAC, the D/A converter is mathematically described as

$$V_o = k V_{FS} \left(d_1 \bar{2}^1 + d_2 \bar{2}^2 + \dots + d_n \bar{2}^n \right)$$

V_o = output Voltage.

V_{FS} = full scale output voltage

k = scaling factor usually adjusted to 1.

d_1, d_2, \dots, d_n = n bit binary word with

d_1 = Most Significant (MSB) with a

$$\frac{V_{FS}}{2}$$

d_n = Least Significant bit (LSB)

with a weight of $\frac{V_{FS}}{2^n}$

(2)

There are various ways to implement.

1. weighted resistor DAC.
2. R-2R Ladder.
3. Inverted R-2R ladder.

Weighted Resistor DAC.

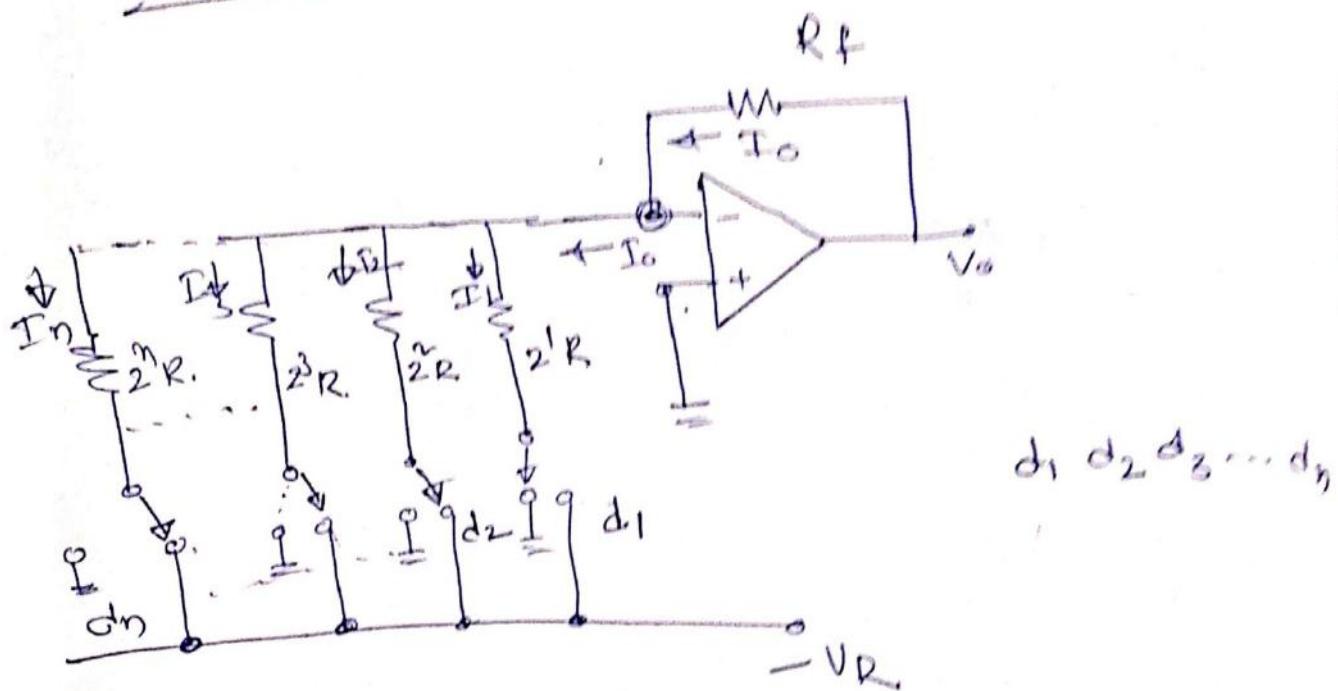
- * It uses a summing amplifier with a binary weighted resistor network.
- * It has n -electronic switches d_1, d_2, \dots, d_n controlled by binary I/p w/d.
- * These switches are single pole double throw (SPDT) type
- * If the binary I/p to a particular switch is 1, it connects the resistance to the reference voltage ($-V_R$).
- * If the I/p bit is '0', the switch connects the resistor to the ground.

From the fig the output current

I_o for an ideal op-amp can be written as

(2)

weighted resistor DAC



$$I_o = I_1 + I_2 + I_3 + \dots + I_n.$$

$$I_o = \frac{V_R}{2^1 R} d_1 + \frac{V_R}{2^2 R} d_2 + \dots + \frac{V_R}{2^n R} d_n.$$

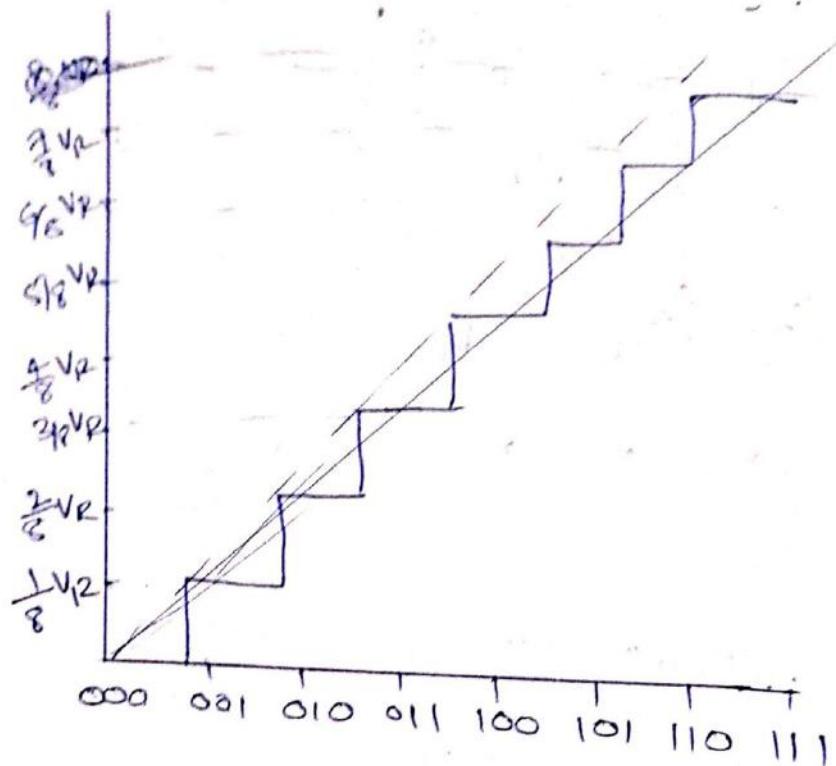
$$= \frac{V_R}{R} \left[d_1 \bar{2}^1 + d_2 \bar{2}^2 + \dots + d_n \bar{2}^n \right]$$

The output voltage

$$V_o = I_o R_f = V_R \cdot \frac{R_f}{R} (d_1 \bar{2}^1 + d_2 \bar{2}^2 + \dots + d_n \bar{2}^n)$$

if $\frac{R_f}{R} = R_k$, $k=1$ and $V_{fs} = V_R$.

(4)



(b) Transfer characteristics of a
3-bit DAC.

The ckt shown in fig. is a 5-bit DAC. In reference to the analog opp voltage is reference. The state can be shown in fig. therefore the state can be shown in fig. therefore the state can be shown in fig. therefore the state can be shown in fig.

For a 3-bit weighted resistor DAC.

It may be noted that

(i) Fig (a) is connected in inverting mode.
It can also be connected in non-inverting mode.

(ii) The op amp is simple working as a current to voltage converter.

(iii) The polarity of the reference voltage is chosen in accordance with the type of the switch used. For ex. if TTL compatible switches, the ref voltage should be +5V and the op voltage will be -5V.

* The accuracy and stability of a DAC depends upon the accuracy of the resistive track.

(6)

Limitations / & Disadvantages of Weighted Resistor DAC are

In this resistor divider (or) Binary weighted resistor DAC

1. Each resistor in the network has a different value.

2. The resistor used for the MSB

is required to handle a much greater current than that used for the LSB resistor.

For better resolution, the word length has to be increased. Thus as the number of bits increases, the range of resistor values increase.

For 8-bit DAC, the resistor

required are $2^0 R, 2^1 R, \dots, 2^7 R$

The largest resistor is 128 times the smallest one. for 8-bit DAC

For a 12-bit DAC, the largest resistor required is 5.12 mA if smallest is 2.5 kΩ.

(5)

The fabrication of such a large resistor value has I_C is not practical. Also the voltage drop across such a large resistor due to the bias current would also effect the accuracy.

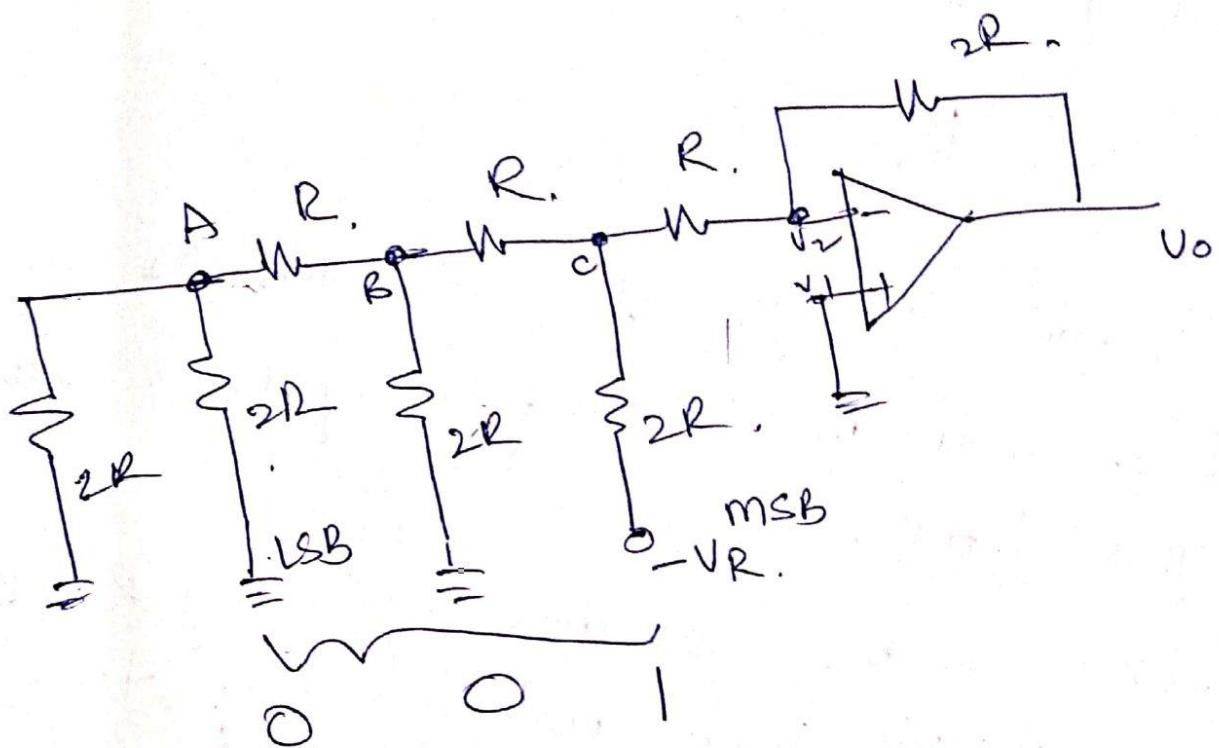
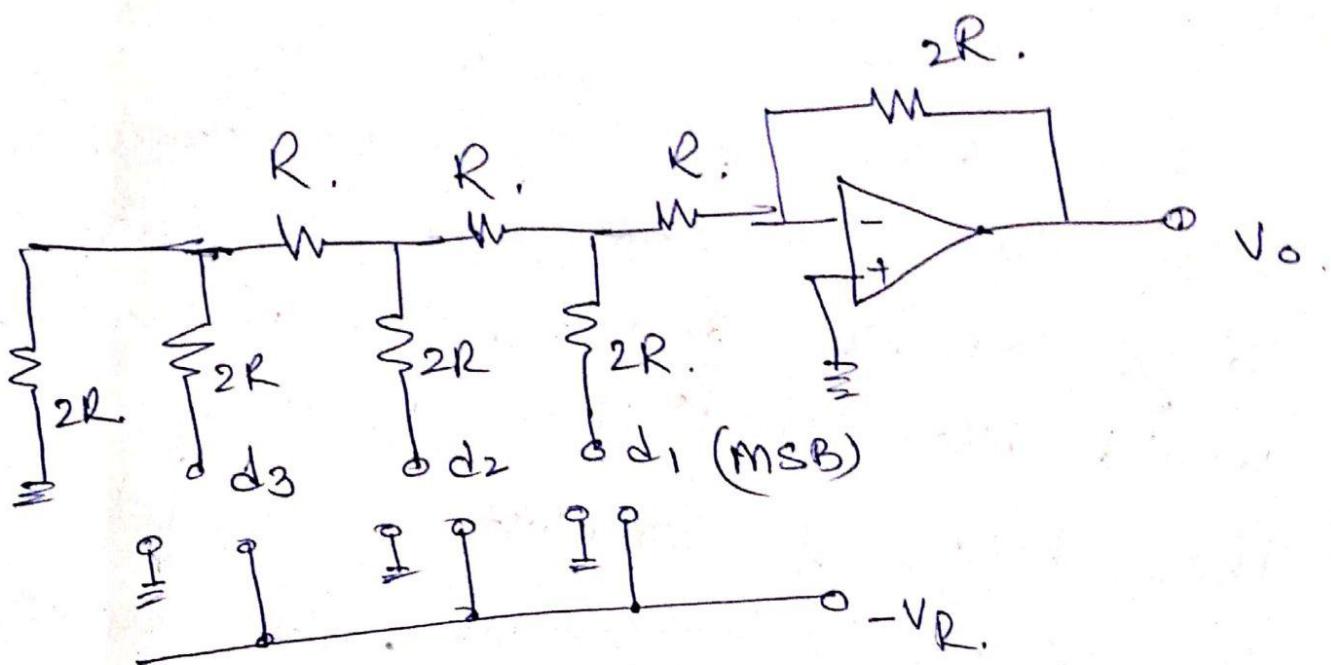
The choice of smallest resistor value as $2.5\text{ k}\Omega$ is reasonable, otherwise loading effect will be there.

R-2R Ladder DAC

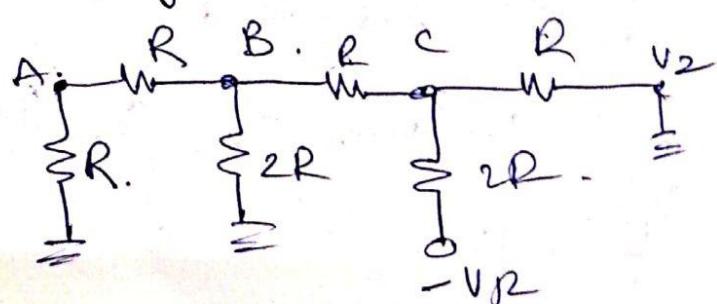
* wide range of resistors are required in binary weighted resistor type DAC.

This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. It is well suited for IC realization. The typical values of R ranges from $2.5\text{ k}\Omega$ to $10\text{ k}\Omega$.

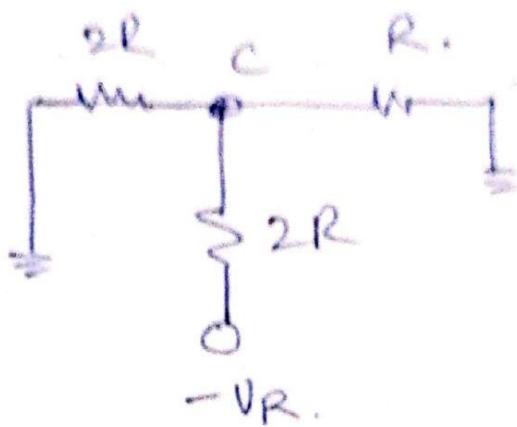
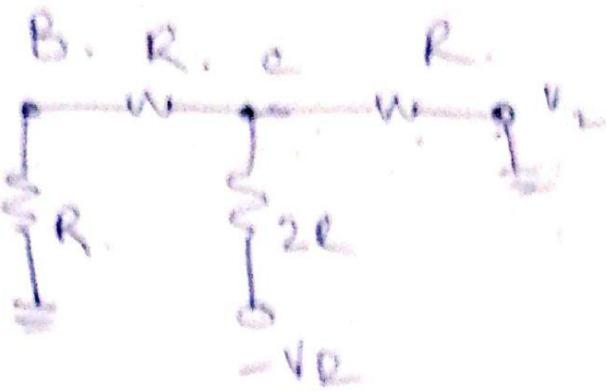
6



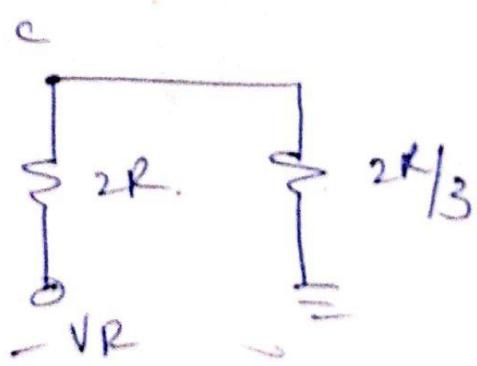
The Voltage at mode C



(7)



$$\frac{(2R)(CR)}{2R+R} = \frac{2R}{3R} = \frac{2R}{3}$$



$$\frac{2R}{2R+6R} = \frac{2R}{8R} = \frac{1}{4}$$

Voltage at node 'c' is

$$= -V_R \times \frac{\frac{2R}{3}}{\frac{2R}{3} + 2R} = -\frac{V_R}{4}$$

(8)

The output Voltage

$$V_o = \left(\frac{-2R}{R} \right) \left(-\frac{V_R}{4} \right) = \frac{V_R}{2} = \frac{V_{PS}}{2}$$

In a similar fashion we can
calc the voltages for

$$010 \rightarrow \frac{V_{PS}}{4} \rightarrow \frac{V_{PS}}{2^2}$$

$$001 \rightarrow \frac{V_{PS}}{8} \rightarrow \frac{V_{PS}}{2^3}$$

$$\begin{aligned} 111 &\rightarrow \frac{V_{PS}}{2} + \frac{V_{PS}}{4} + \frac{V_{PS}}{8} \\ &= \frac{4+2+1}{8} = \frac{7}{8} V_{PS} \approx V_{GS} \end{aligned}$$

Mono lithic DAC

(9)

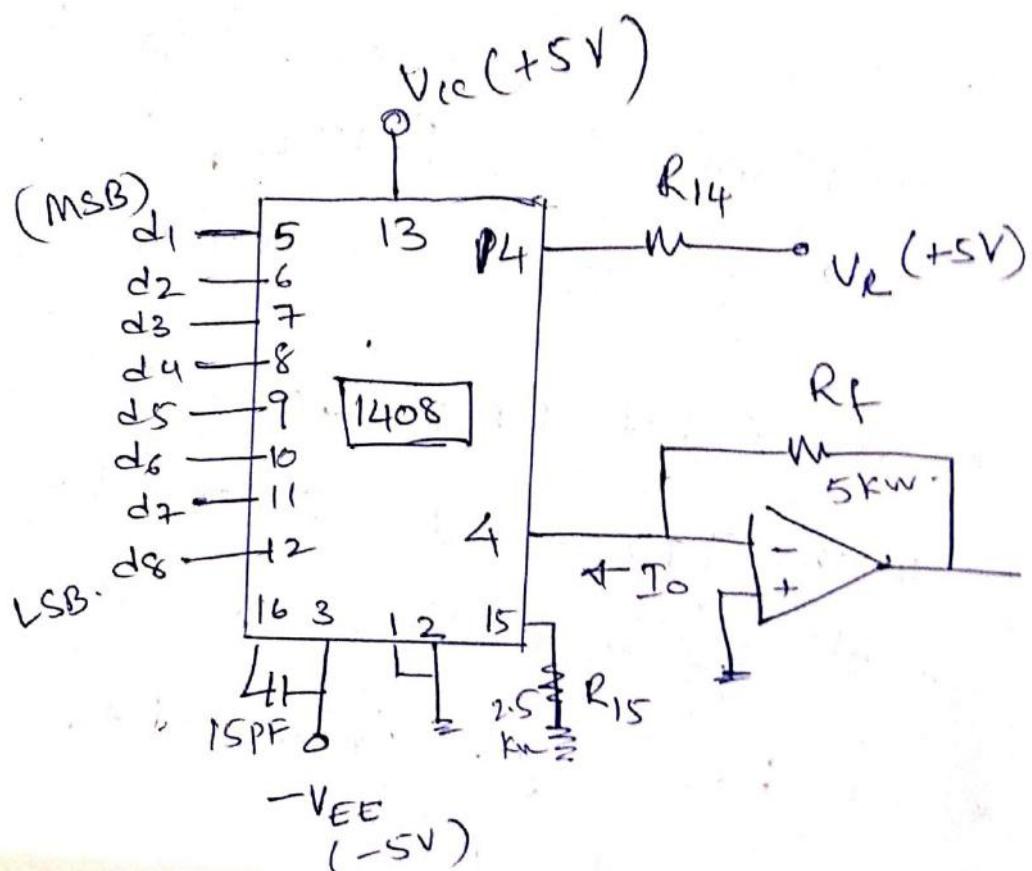
- * Mono lithic DAC's consists of R-2R ladder, switches and the R_R resistor are available for 8, 10, 12, 14 and 16 bit resolution from various manufacturers.
- * The MC 1408 L is a 8-bit DAC with current output.
- * There are hybrid D/A converter available in DATEL DAC-H-2 series for current as well as voltage output.
- * A 8-bit DAC 1408 is compatible with TTL and CMOS logic with settling time around 300 nsec.
- * It has eight input data lines d₇(MSB) through d₀ (LSB).
- * It requires 2mA reference current for full scale I_f and two power supplies V_{cc} = +5V and V_{EE} = -5V

10

The total reference current source is determined by resistor R_{14} and voltage reference V_R and equal to

$$\frac{V_R}{R_{14}} = \frac{5V}{2.5k\Omega} = 2mA.$$

- * The resistor $R_{15} = R_{14}$ match the input impedance of the reference source.



The output current I_o is cal. of

$$I_o = \frac{V_R}{R_{14}} \left(\sum_{i=1}^8 d_i 2^i \right) \quad d_1 = 0 \text{ or } 1$$

For full scale I/P (i.e. ds through
 $d_1 = 1$)

$$I_O = \frac{5V}{2.5k\Omega} \left[\sum_{i=1}^8 1 \times \bar{z}_i \right]$$

$$= 2mA \left(\frac{255}{256} \right) = \underline{\underline{1.992 \text{ mA}}}$$

MSB LSB \rightarrow Full Scale.

1 1 1 1 1 1 1 1

$$\left(\frac{1}{2} + \frac{1}{2^2} + \frac{1}{2^3} + \frac{1}{2^4} + \frac{1}{2^5} + \frac{1}{2^6} + \frac{1}{2^7} + \frac{1}{2^8} \right)$$

$$\frac{2^7 + 2^6 + 2^5 + 2^4 + 2^3 + 2^2 + 2^1 + 1}{2^8} = \frac{255}{256}$$

The output is 1 LSB less than the full scale reference current of 2mA.

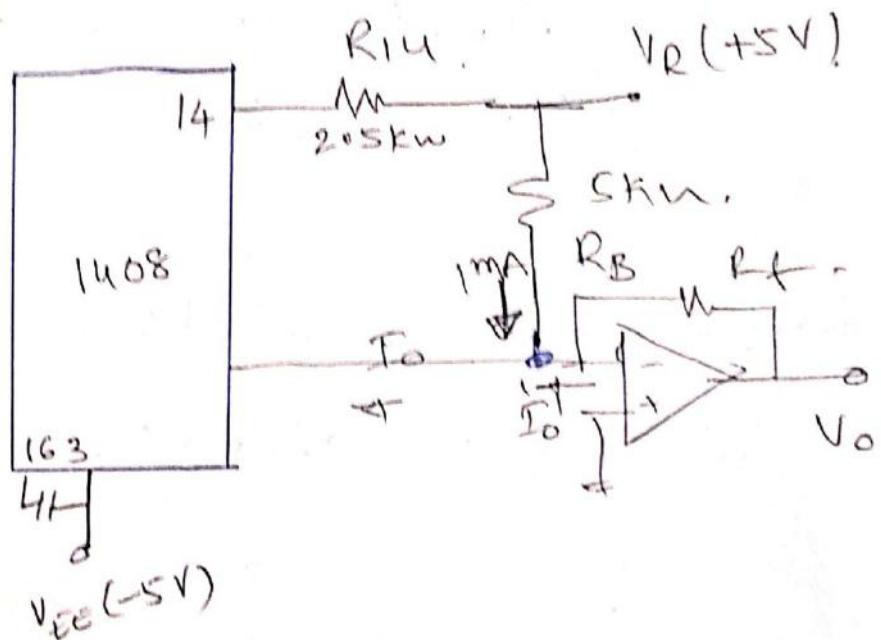
So, the output voltage V_o for the full scale I/P is -

$$V_o = 2mA \left(\frac{255}{256} \right) \times 5k\Omega = 9.961V.$$

In general the output Voltage
V_O is given by

$$V_O = \frac{V_R}{R_m} R_f \left[\frac{d_1}{2} + \frac{d_2}{4} + \frac{d_3}{8} + \dots + \frac{d_8}{256} \right]$$

The 1408 DAC can be calibrated
for bipolar range from -5V to +5V
by adding resistor R_B (5kΩ) between
V_R and op-amp Pin 4.



The resistor R_B supplies I_{mA} ($\frac{V_R}{R_B}$)

current to the output in the opposite
direction of the current generated by I/P

$$\begin{aligned} I_o' &= I_o - \left(\frac{V_R}{R_B} \right) \\ &= \left(\frac{V_R}{R_{IN}} \right) \left(\sum_{i=1}^d d_i \frac{1}{2^i} \right) - \frac{V_R}{R_B}. \end{aligned}$$

For the Binary S/p word 00000000
i.e zero S/p, the output becomes

$$\begin{aligned} V_o &= I_o' R_f \\ &= \left(I_o - \frac{V_R}{R_B} \right) R_f \\ &= \left(0 - \frac{5V}{5kW} \right) 5kW. \end{aligned}$$

$$V_o = \underline{-5V} \quad \text{for } \underline{00000000}$$

For binary input word 10000000
the V_o becomes

$$\begin{aligned} V_o &= \left(I_o - \frac{V_R}{R_B} \right) R_f \\ &= \left(\frac{V_R}{R_{IN}} \left(\frac{d_1}{2} \right) - \frac{V_R}{R_F} \right) R_f \\ &= \left(\frac{5}{205kW} \left(\frac{1}{2} \right) - \frac{5V}{5kW} \right) 5kW = \underline{0V} \end{aligned}$$

$$(1\text{mA} - 1\text{mA}) \times 5\text{k}\Omega = 0\text{V.}$$

(14)

For Binary D/p word = 1111 1111
The output voltage becomes.

$$V_o = \left[\frac{VR}{R_{14}} \left(\frac{255}{256} \right) - 1\text{mA} \right] R_F$$

$$= (1.992 \text{ mA} - 1\text{mA}) \times 5\text{k}\Omega.$$

$$V_o = 0.992 \text{ mA} \times 5\text{k}\Omega = \underline{\underline{4.960\text{V}}}.$$

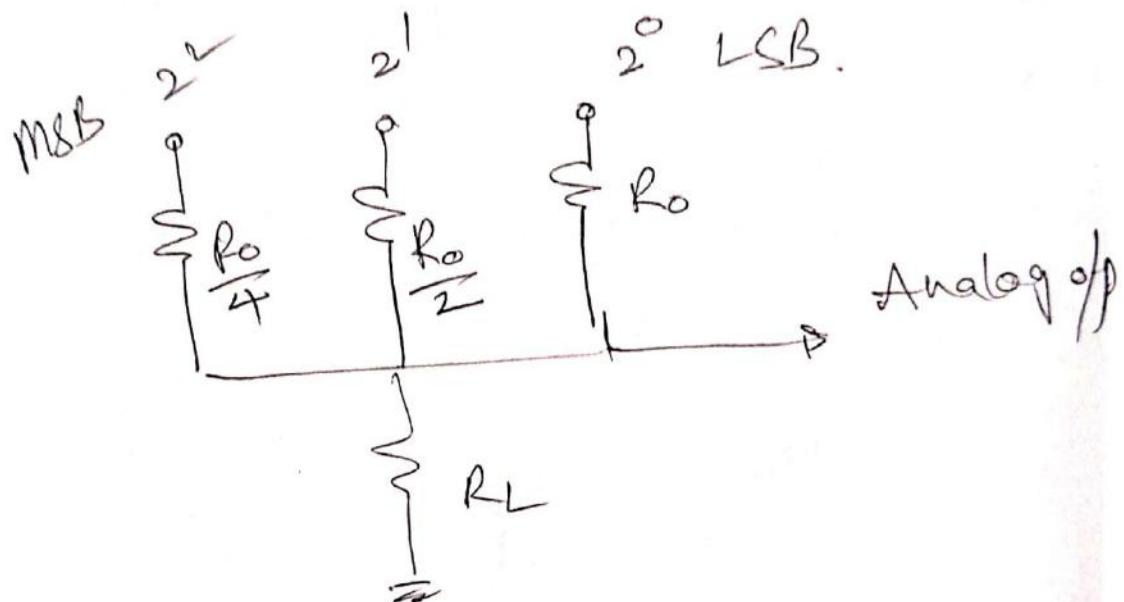
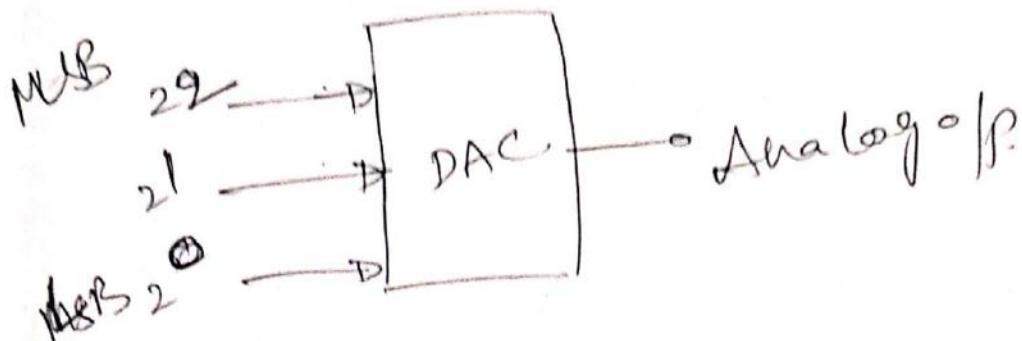
For 1111 1111

0000 0000 $\xrightarrow{-5\text{V}}$

1 000 0000 $\xrightarrow{0\text{V}}$

1.111 1111 $\xrightarrow{4.960\text{V}} \approx +5\text{V}$.

Resistive N/w.

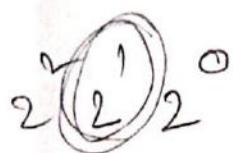


0 0 0	0 V
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	4
1 0 1	5
1 1 0	6
1 1 1	7 V

1 in the 2⁰ position will cause

$$+7 \times \frac{1}{7} = 1V \text{ at the o/p.}$$

$$2^1 = 2 \text{ and } 2^0 = 1$$

 2¹ 2² 2⁰

$$7 \times \frac{2}{7} = 2V.$$

In twice

$$7 \times \frac{4}{7} = \underline{\underline{4V}}.$$

$$\frac{V_{R_1}}{2^0 - 1} = \frac{V_O}{7}$$

Bit	weight
2 ⁰	$\rightarrow \frac{1}{7}$

$$2^1 \rightarrow \frac{2}{7}$$

$$2^2 \rightarrow \frac{4}{7}$$

$$\text{Sum} \rightarrow \frac{7}{7}$$

3-bit

Bit	weight
2 ⁰	$\frac{1}{15}$
2 ¹	$\frac{2}{15}$
2 ²	$\frac{4}{15}$
2 ³	$\frac{8}{15}$
	$\rightarrow \underline{\underline{\frac{15}{15}}}$
4-bit	

Assignment on 555 IC timer:

UNIT-IV

- ① Design a Monostable multivibrator using 555 IC timer to produce a pulse width of 100 msec.
- ② The monostable multivibrator is used as a divide - by - 3 n/w. The freq. of the I/p trigger is 15 kHz. If the value of $C = 0.01 \mu F$, calculate the value of resistance R .
- ③ In Astable multivibrator $R_A = 2.2 k\Omega$ and $C = 0.01 \mu F$. Calculate $R_B = 6.8 k\Omega$ and
i) t_{high} ii) t_{low} iii) Free running frequency iv) Duty cycle 'D'.
- ④ Design a Astable multivibrator of frequency 100 Hz and duty cycle of 75%.

- ⑤ Design a Symmetrical Square wave generator (i.e 50% duty cycle) of 10 KHz.
- ⑥ what are the important features of 555 IC timer and draw its pin diagram and functional diagram.
- ⑦ How a monostable multivibrator can generate pulses. Explain. And derive the expression of time delay (Q)
the expression of pulse width of Monostable multivibr.
- ⑧ Explain the operation of 555 timer in Astable mode and derive the expressions for free running freq and duty cycle.
- ⑨ Discuss the applications of Monostable mult using 555 IC timer.
⑩ a) Frequency divider b) Pulse width modulator.
- ⑩ Discuss the applications of Astable mult using 555 IC Timer.
⑩ a) Schnitt trigger b) Pulse position modulator
c) Square wave generation.

①

Voltage controlled oscillator (VCO)

A common type of VCO is available in IC form i.e. Signetics NE/SE 566. The pin configuration and basic block diagram of 566 VCO are shown in Fig. A tuning capacitor C_T is linearly charged or discharged by constant current source. The amount of current can be controlled by changing the voltage V_C applied at the modulating input (pin 5) or by changing the tuning resistor R_T external to IC chip.

The voltage at pin 6 is held at the same voltage as pin 5. Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.

(2)

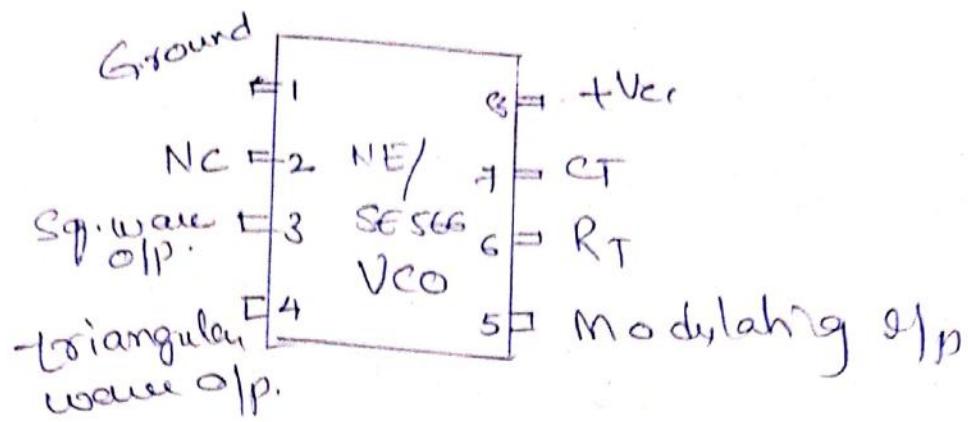


Fig (a)

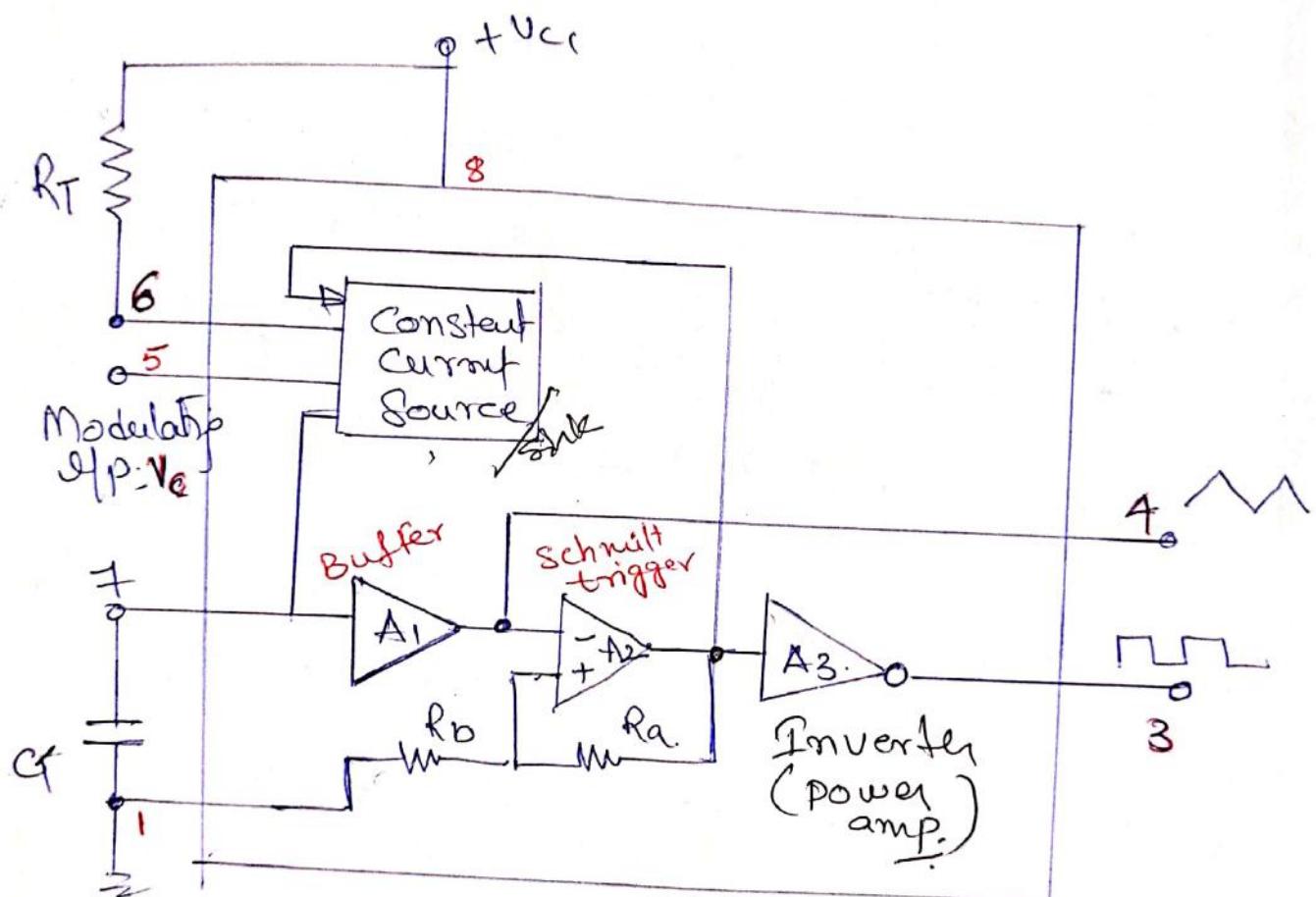


Fig (b)

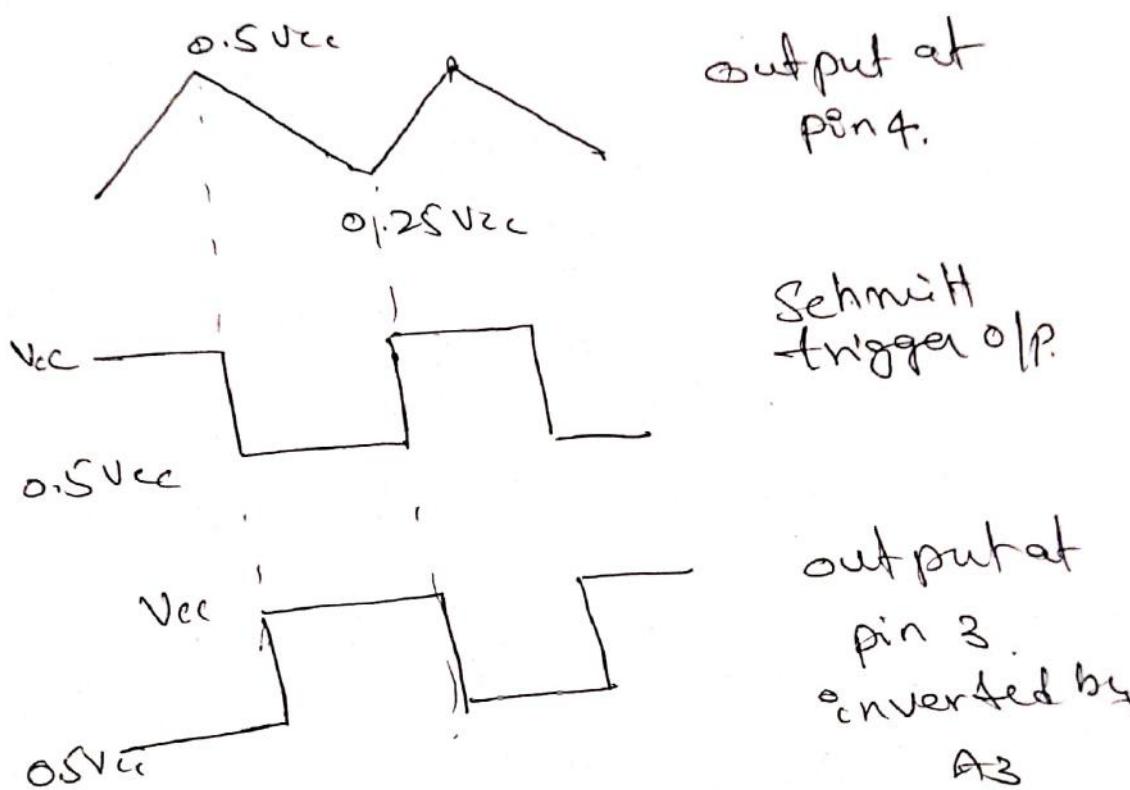
Voltage controlled oscillator (a) Pin configuration

(b) Block diagram.

- * The voltage across the capacitor C_T in ③ applied to the inverting input terminal of Schmitt trigger A_2 via buffer amplifier A_1 ,
- * The output voltage swing of the Schmitt trigger is designed to V_{cc} and $0.5V_{cc}$.
- * If $R_a = R_b$ in the positive feedback loop, the voltage at the non inverting input terminal of A_2 swings from $0.5V_{cc}$ to $0.25V_{cc}$.
- * When the voltage on the capacitor C_T exceeds $0.5V_{cc}$ during charging, the output of the Schmitt trigger goes low ($0.5V_{cc}$).
- * The capacitor now discharges and when it is at $0.25V_{cc}$, the output of Schmitt trigger goes HIGH (V_{cc}).
- * Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time.
- * This gives a triangular voltage wave form across C_T which is also available at pin 4.

(4)

The square wave output of the Schmitt trigger is inverted by inverter A₃ and is available at pin 3. The output waveforms are shown in Fig.



The output frequency of the VCO can be calculated as follows.

The total voltage on the capacitor changes from $0.25 V_{cc}$ to $0.5 V_{cc}$.

$$\text{Thus } \Delta V = 0.25 V_{cc}.$$

The capacitor charges with a constant current source.

(5)

$$\text{So } \frac{\Delta V}{\Delta t} = \frac{i}{C_T}$$

$$\frac{0.25 V_{cc}}{\Delta t} = \frac{i}{C_T}$$

$$\Delta t = \frac{0.25 V_{cc} \cdot C_T}{i} \quad \rightarrow (1)$$

The time period 'T' of the triangular waveform = $2 \Delta t$. The freq. of oscillation f_0 is

$$f_0 = \frac{1}{T} = \frac{1}{2 \Delta t}$$

$$f_0 = \frac{\cancel{0.25 V_{cc} C_T}}{2 \times 0.25 V_{cc} \cdot C_T} \quad \rightarrow (2)$$

$$f_0 = \frac{i}{0.5 V_{cc} C_T}$$

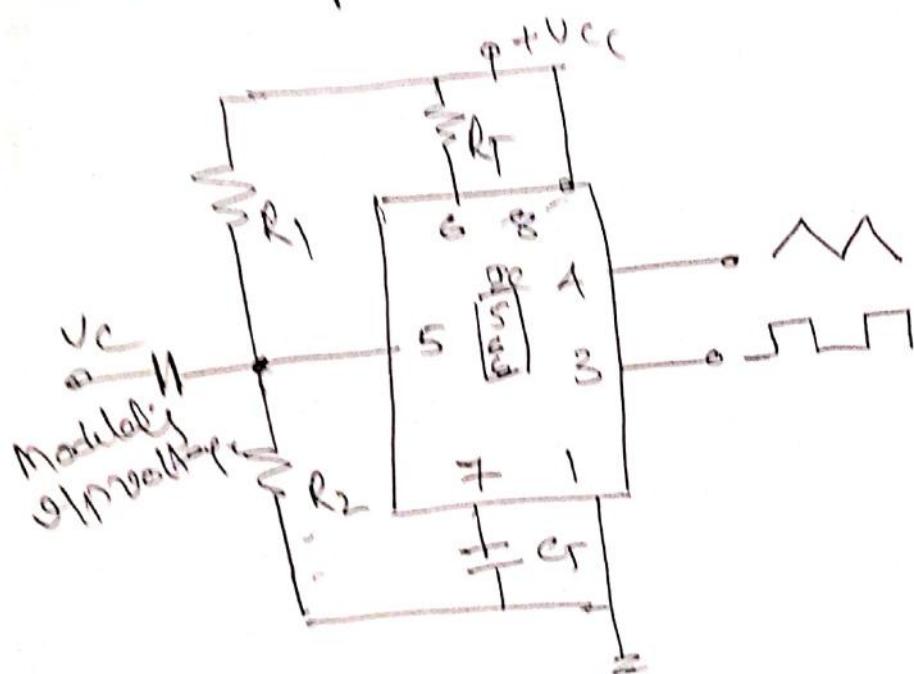
$$\text{But } i = \frac{V_{cc} - V_c}{R_T}$$

where V_o is the Voltage at pin 5. (6)

$$\therefore f_o = \frac{2(V_{cc} - V_o)}{C_F R_F V_{cc}} \quad (3)$$

The output frequency of the VCO can be change by (i) R_F (ii) C_F or (iii) the Voltage V_o at the modulating I/P terminal Pin 5.

The Voltage V_o can be varied by connecting a $R_1 R_2$ circuit as shown in Fig.



Typical connection diagram.

The components R_T and C_F are first selected so that VCO output frequency lies in the center of the operating frequency band.

Now the modulating S/p voltage is usually varied from $0.75 V_{cc}$ to V_{cc} which can produce a freq variation of about 10 to 1.

With no modulating S/p signal, if the voltage at pin 5 is biased at $(7/8) V_{cc}$

So from eq ③

$$f_0 = \frac{2 \left[V_{cc} - (7/8) V_{cc} \right]}{C_T R_T V_{cc}}$$

$$f_0 = \frac{1}{4 R_T C_T} = \frac{0.25}{R_T C_T} \quad \rightarrow ④$$

Voltage to Frequency Conversion Factor

A parameter of importance for VCO is voltage to frequency conversion factor k_V and is defined as

$$k_V = \frac{\Delta f_0}{\Delta V_c}$$

Here ΔV_c is the modulation voltage required to produce the freq shift Δf_0 , for a VCO. If we assume they are original freq f_0 and the new

in f_1 then.

(8)

$$\Delta f_o = f_1 - f_0.$$

$$= \frac{2(V_{ce} - V_c + \Delta V_c)}{C_F R_T V_{ce}} - \frac{2(V_{ce} - V_c)}{C_F R_T V_{ce}}$$

$$= \frac{2 \Delta V_c}{C_F R_T V_{ce}}$$

$$\Delta V_c = \frac{\Delta f_o \cdot C_F R_T V_{ce}}{2}$$

putting the value of $C_F R_T$ from eq(4)

$$\boxed{f_0 = \frac{1}{4 C_F R_T}}$$

$$\Delta V_c = \frac{\Delta f_o \cdot V_{ce}}{8 f_0}$$

$$K_V = \frac{\Delta f_o}{\Delta V_c} = \frac{8 f_0}{V_{ce}}$$

$$\boxed{K_V = \frac{8 f_0}{V_{ce}}}$$

Phase - Locked Loops.

(9)

Introduction :-

The phase-locked loop (PLL) is an important building block of linear systems. Electronic phase-locked (PLL) came into vogue in the 1930s when it was used for radar synchronisation and communication applications. The high cost of realizing PLL in discrete form limited its use earlier. Now with the advances in IC technology, PLLs are available as inexpensive monolithic ICs.

This technique for electronic frequency control is used in satellite communications, air borne navigational systems, FM communication systems, computers etc.

Basic principle :-

- ① Phase detector / comparator.
- ② A LPF.
- ③ An error amplifier.
- ④ A Voltage Controlled Oscillator (VCO).

- * The VCO is a free running multivibrator and operates at a free frequency f_0 called free running frequency.
- * This freq_v is determined by an external tuning capacitor and an external resistor.
- * It can also be shifted to either side by applying a dc control voltage V_c to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a 'Voltage Controlled Oscillator' or VCO.
- * If an input signal V_s of the freq_s is applied to the PLL, the phase detector compares the phase and freq_v of the incoming signal to that of the output V_o of the VCO.
- * If the two signals differ in freq_v and/or phase, an error voltage V_e is generated. The phase detector is basically a multiplier and produces

(11)

the sum ($f_s + f_o$) and difference ($f_s - f_o$) components at its outputs. The high freq component ($f_s + f_o$) is removed by the LPF and the difference frequency component is amplified and then applied as control voltage V_c to VCO.

The signal V_c shifts the VCO freq. in a direction to reduce the freq. difference between f_s and f_o . Once this action starts, the signal is in the capture range.

The VCO continues to change freq. till its output freq. is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency f_o of VCO is identical to f_s except for a finite phase difference ϕ . This phase difference generates a corrective control voltage V_c to shift the VCO frequency from f_o to

fs. and thereby maintain the lock, once locked, PLL tracks the frequency changes of the input signal.

Thus PLL goes through three stages.

- (i) Free running
- (ii) Capture
- (iii) Locked or tracking.

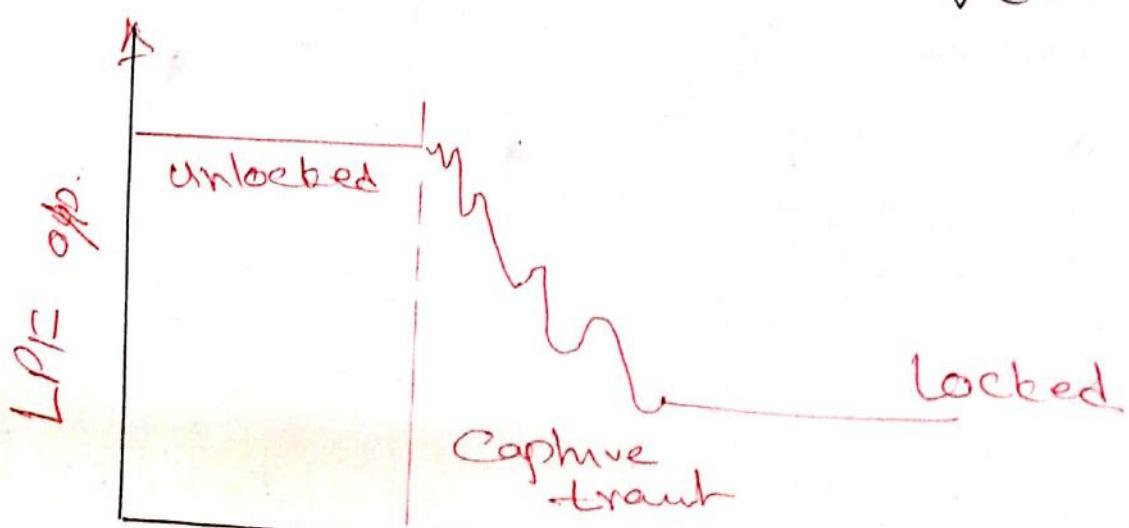
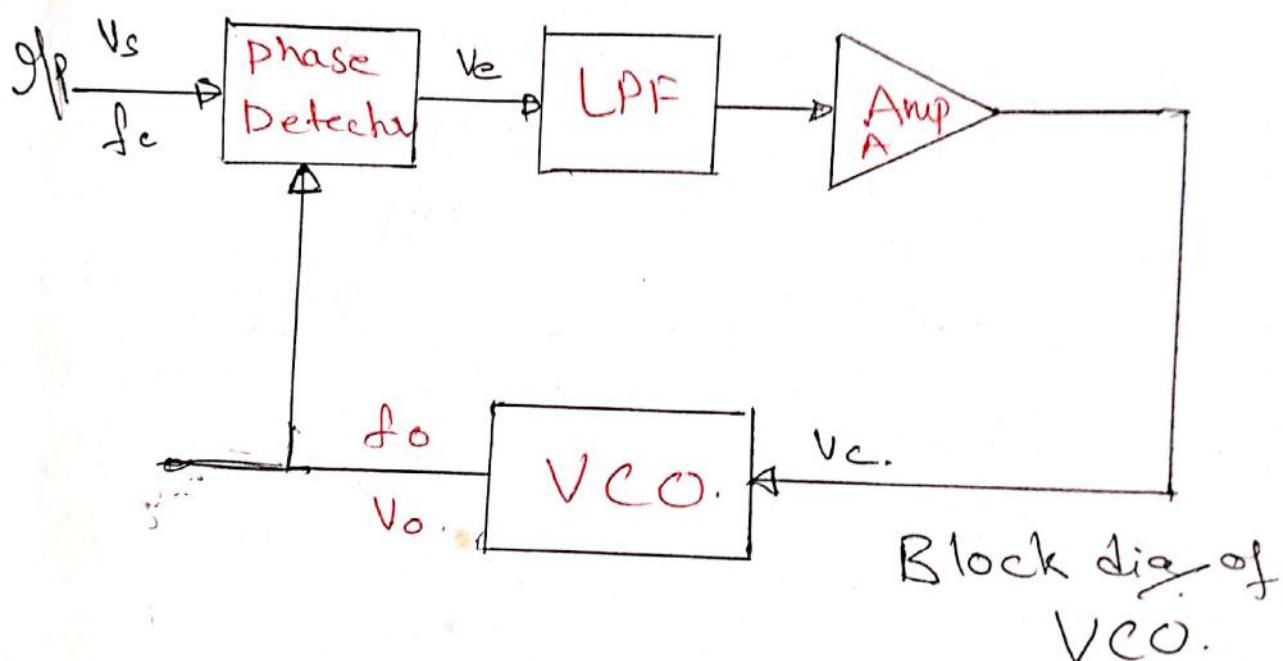


Fig: The capture train. Input f in gray

Fig shows the capture transient.

- * As capture starts, a small sine wave appears. This is due to the difference frequency between the VCO and the input signal. The dc component of the beat drives the VCO towards lock.
- * Each successive cycle causes the VCO frequency to move closer to the input signal frequency.
- * The difference in frequency becomes smaller and a larger dc component is passed by the filter, shifting the VCO frequency further.
- * The process continues until the VCO locks on to the signal and the difference freq is dc.
- * The LPF controls the capture range. If VCO freq is far away the beat freq will be too high to pass through the filter and the PLL will not respond. we say the the signal is out of the capture band. However once locked, the filter no longer

restricts the PLL. The VCO can track the signal well beyond the capture band.

Thus tracking range is always larger than the capture range.

Lock-in Range

once the PLL is locked, it can track freq changes in the incoming signals. The range of freq over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range.

The lock range is usually expressed as a percentage of f_0 , the VCO freq.

The lock range f_L is given by

$$f_L = \pm \frac{8f_0}{V} \text{ Hz}$$

Capture Range - The range of freqs over which the PLL can acquire lock with an s/p signal is called the capture range. This parameter is also expressed as

$$f_c = \pm \left[\frac{f_L}{(k_1)(3.6)(10^3)(C_2)} \right]^{1/2} \quad (15)$$

pull-in time

The total time taken by the PLL to establish lock is called pull in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

Phase detector / Comparator

The phase detector is the most important part of the PLL system. There are two types of phase detectors used. Analog and digital.

The phase detector compares the input frequency and the VCO frequency and generates a dc voltage that is proportional to the phase diff between the two frequencies. Depending on whether the analog or digital phase detector is used the PLL is called

either an analog or digital type. 14

A double-balanced mixer is an example of an analog phase detector.

The examples of digital phase detector, are

1. Exclusive-OR phase detector
 2. Edge-triggered phase detector.
 3. Monolithic phase detector (4049)
-
-
-
-
-

Exclusive-OR phase detector uses an

ex-OR gate such as CMOS type 4070.

The output of x-OR gate is high only when f_s or f_o is high.

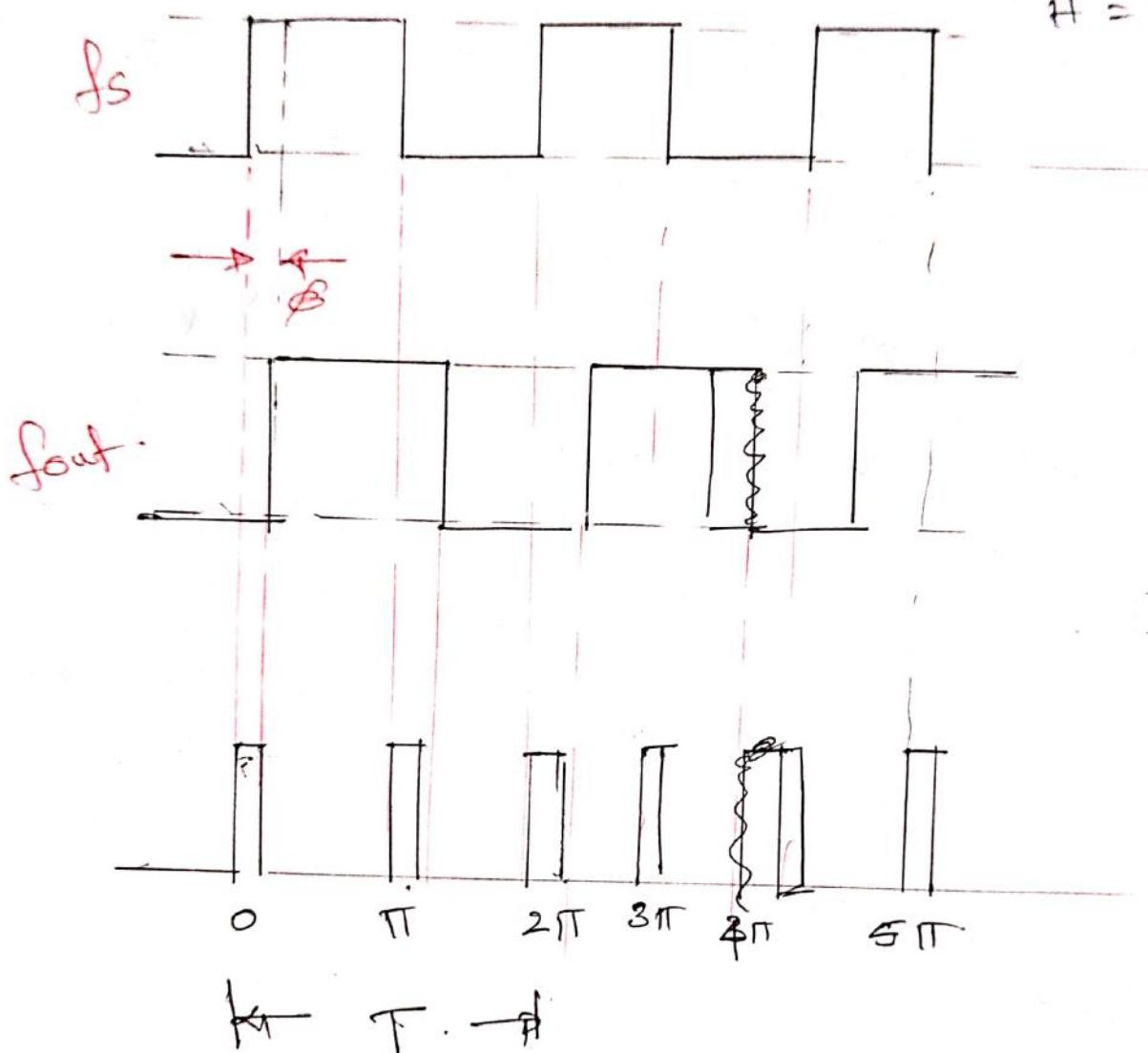
In this fig., f_s is leading f_o by ϕ' degree. i.e. the phase difference between f_s and f_o is ϕ degrees.

The dc o/p voltage of the ex-OR phase detector is a function of the phase difference between its two inputs.

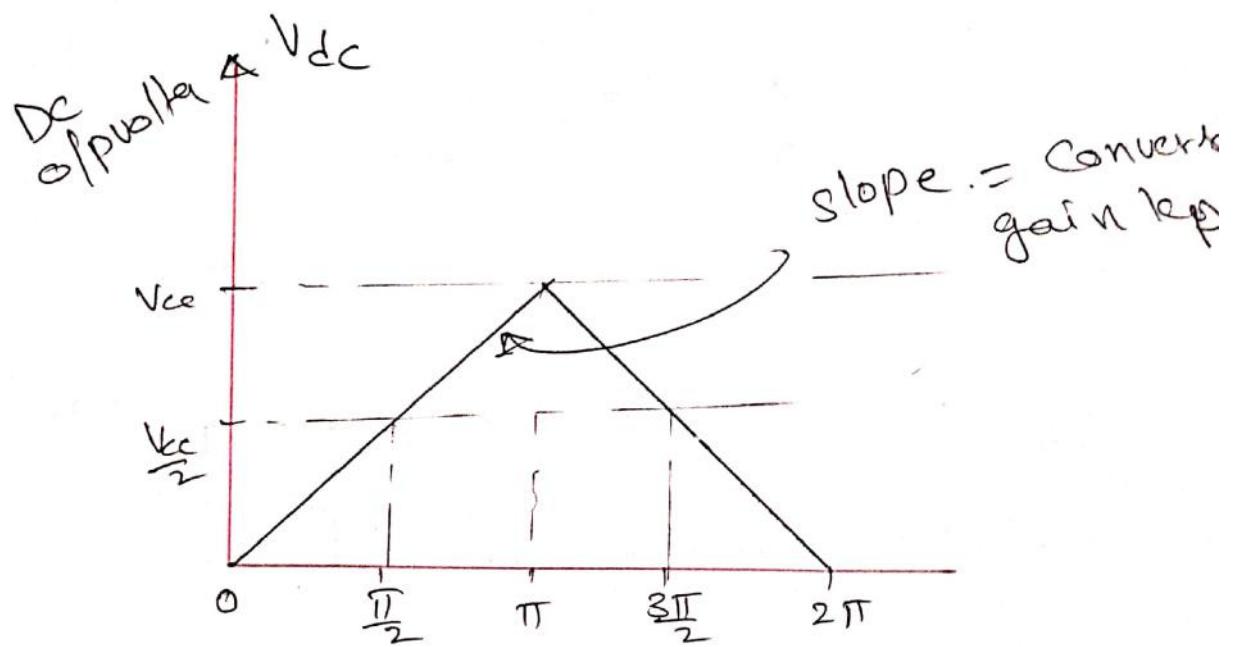


Inputs		Op
A	B.	Y
L	L	L
L	H	H
H	L	H
H	H	L

L = Low
H = High.



(18)



phase difference (ϕ). between
 f_H and f_{out}

①

Fixed Voltage Series Regulators.

78xx series are three terminal positive fixed voltage regulators.

- * There are seven output voltage options available such as 5, 6, 8, 12, 15, 18 and 24 V.
- * In 78xx the last two numbers xx indicate the output voltage.
- * Thus 7815 represents a 15V regulator.
- * There are also available 79xx series of fixed op-, -ve voltage regulators which are complements to the 78xx series devices.
- * There are two extra voltage options of -2V and -5.2V available in 79xx series.

(2)

These regulators are available in
few types of packages.

* metal package (To-3 type)

* plastic package (To-220 type)

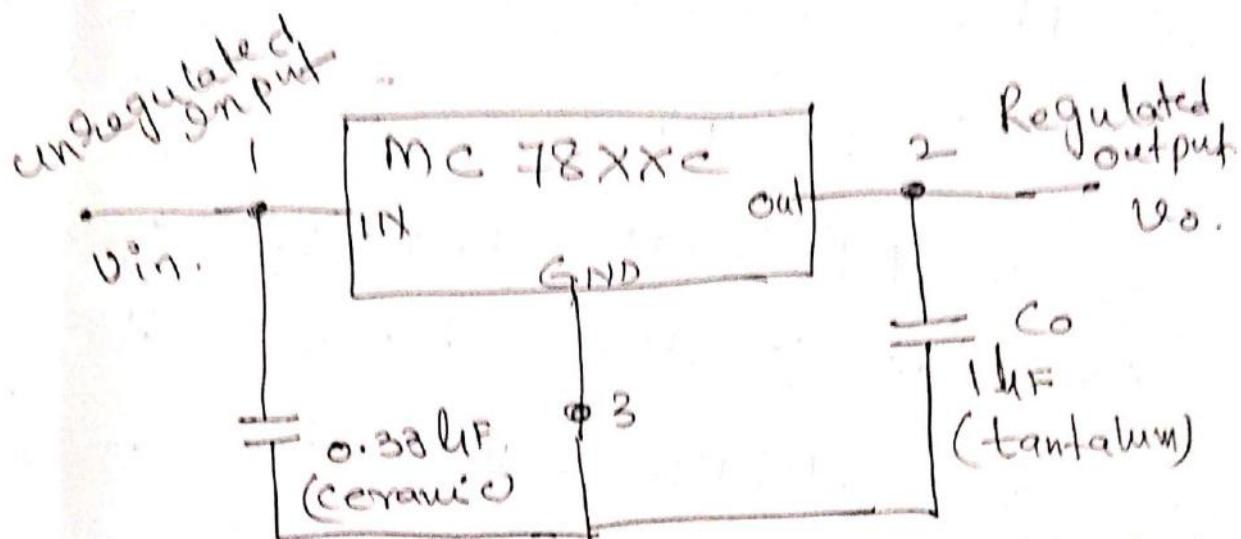


Fig:1
Standard representation of a 3-terminal positive monolithic regulator.

A capacitor C_1 ($0.33 \mu F$) is usually connected b/w Input terminal and Ground to cancel the inductive effects due to long distribution leads.

The output capacitor C_2 ($1 \mu F$) improves the transient response.

National Semiconductor also produce ^③ three terminal voltage regulators in LM Series. There are three being available for different operating temperature ranges.

LM 100 Series -55°C to $+125^{\circ}\text{C}$

LM 200 Series -25°C to $+85^{\circ}\text{C}$

LM 300 Series 0°C to 70°C

The popular series are LM 340 positive regulator and LM 320 negative regulator with output ratings comparable to 78xx/79xx series.

characteristics.

There are four characteristics of three terminal IC regulators which must be mentioned.

Absolute maximum rating

Input voltage (5V through 15V) 35V

24

40V.

Internal power dissipation

(4)

Internally limited

Storage temp range

-65°C to +150°C

operating junction temp range.

LM 7800

-55°C to +150°C

LM 7800C

0°C to 125°C

1. V_o : The regulated o/p voltage is fixed at a value as specified by manufacturer.

There are number of models available for different o/p voltages, for ex, 78xx series has o/p voltage at 5, 6, 8 etc.

2. $|V_{in}| \geq |V_o| + 2 \text{ Volts}$

The unregulated o/p voltage must be at least 2V more than the regulated o/p voltage. For ex $V_o = 5V$, then $V_{in} = 7V$.

(5)

③ $I_{O(\max)}$: The load current may vary from 0 to rated maximum o/p current.
The I_C is usually provided with a heat sink, otherwise it may not provide the rated max o/p curr.

④ Thermal shutdown:

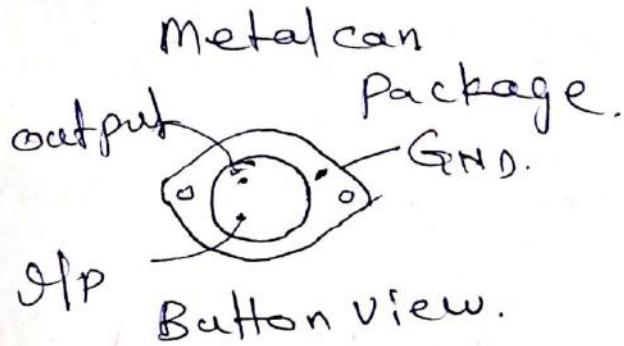
The I_C has a temperature sensor (built-in) which turns off the I_C when it becomes too hot (usually 125°C to 150°C). The output current will drop and remain there until the I_C has cooled significantly.

Line / Input Regulation:

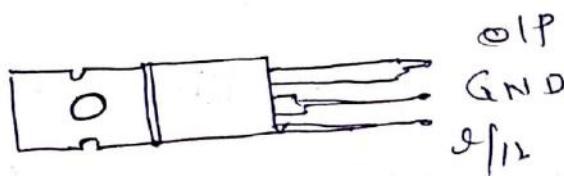
It is defined as the percentage change in the o/p voltage for a change in the i/p voltage.
It is usually expressed in millivolt or as a percentage of the o/p voltage.

Typical value of the line regulation

6



plastic package.

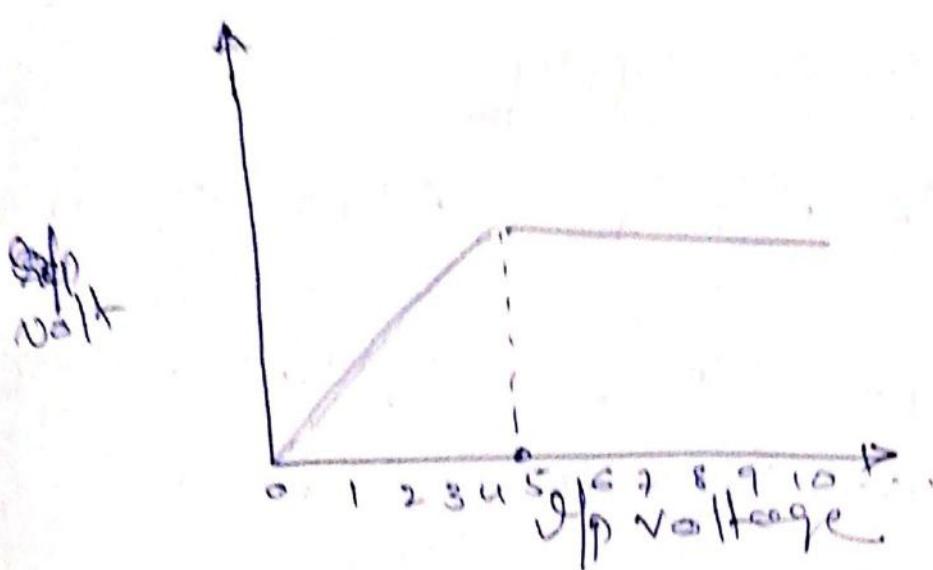


from data sheet of ~~38~~ 7805 in
3mV.

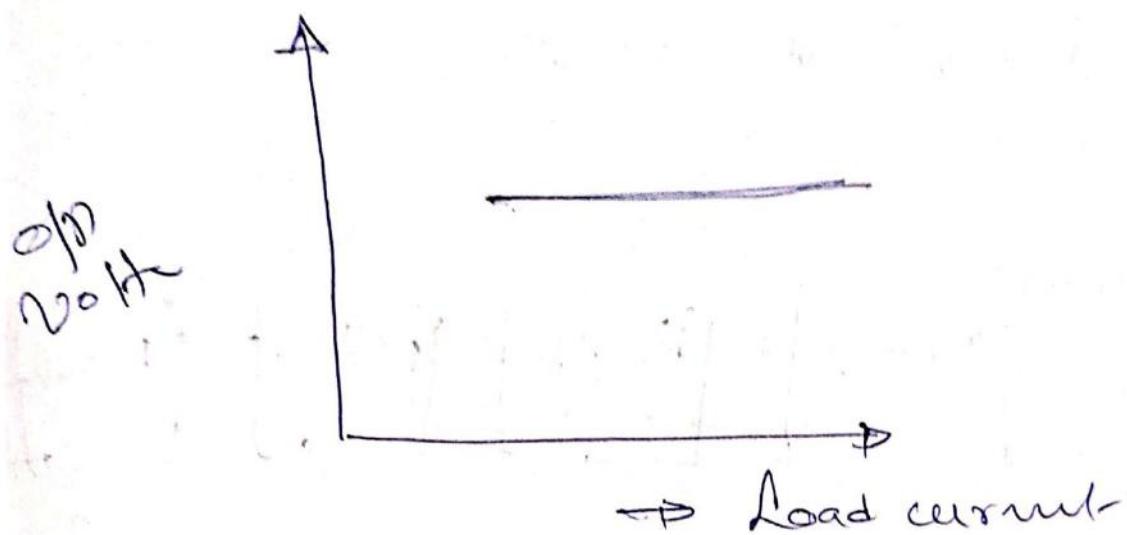
Load Regulation

It is defined as the change in o/p voltage for a change in load current and is also expressed in millivolts or as percentage of V_o .

7



Rise Regulation.

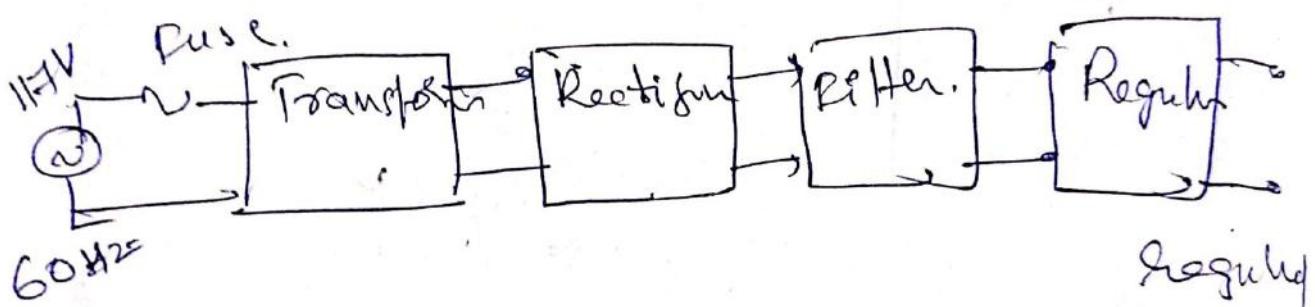


(8)

Power Supply.

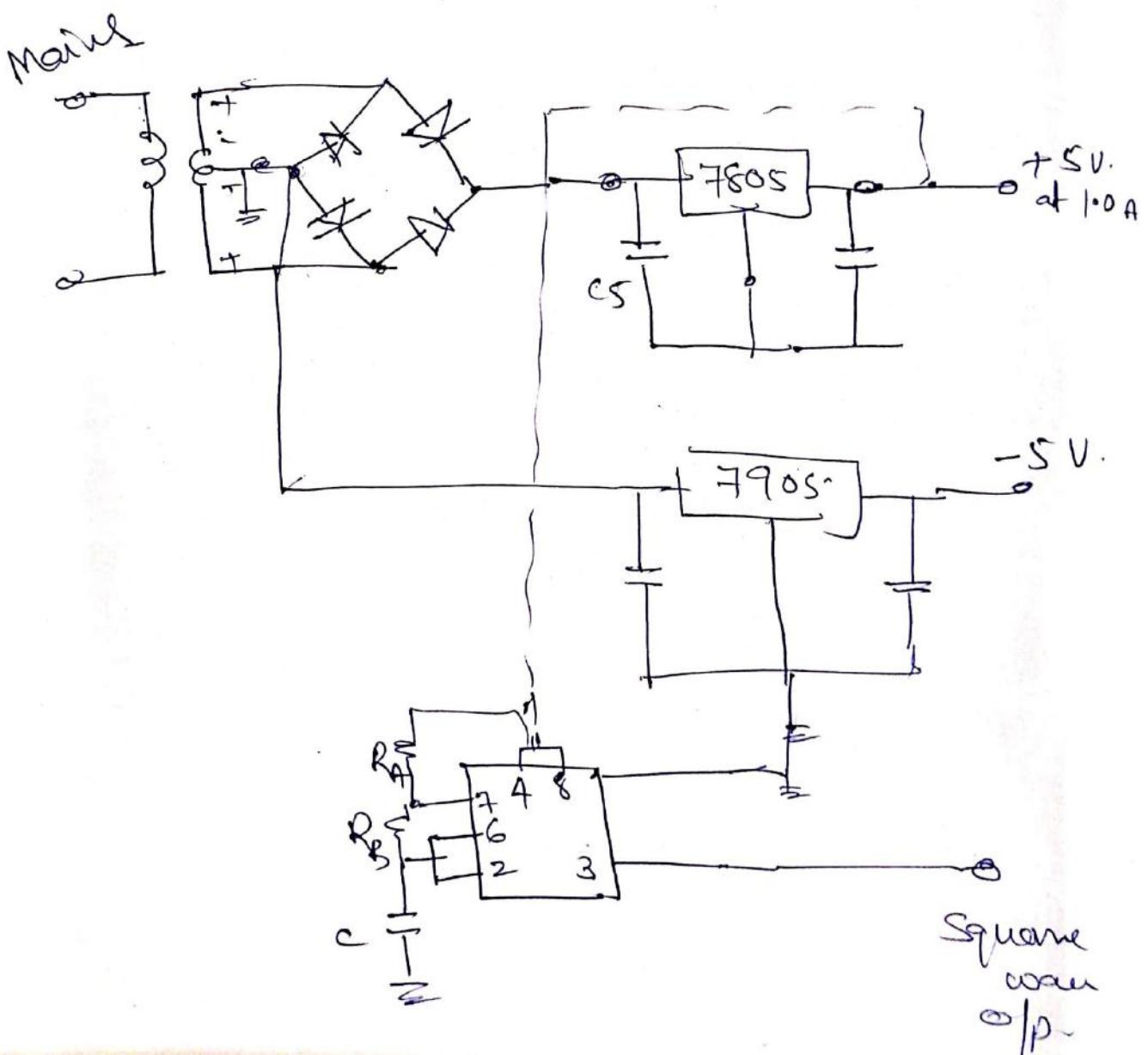
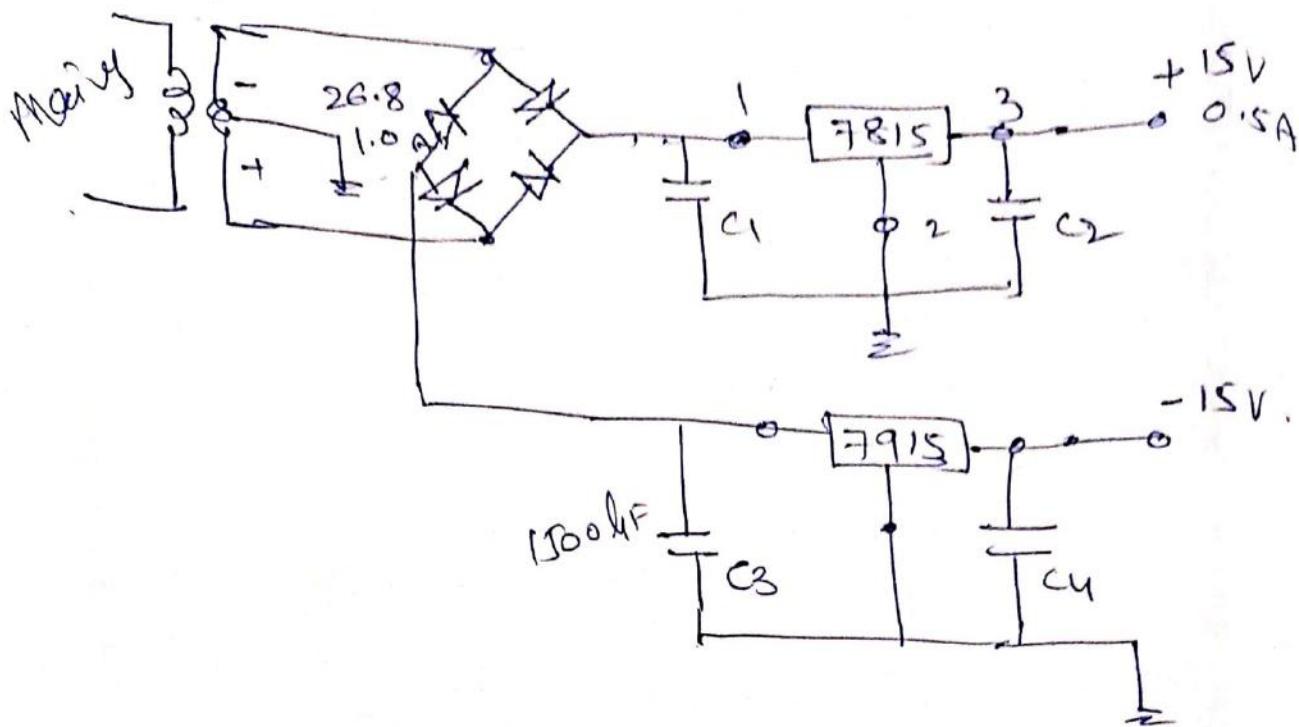
Application of voltage regulator.

Design voltage regulator which can generate +15V, -15V, +5V, -5V and Square wave o/p.
 $\pm 5V$ at 1.0 A and.
 $\pm 15V$ at 0.5 A.



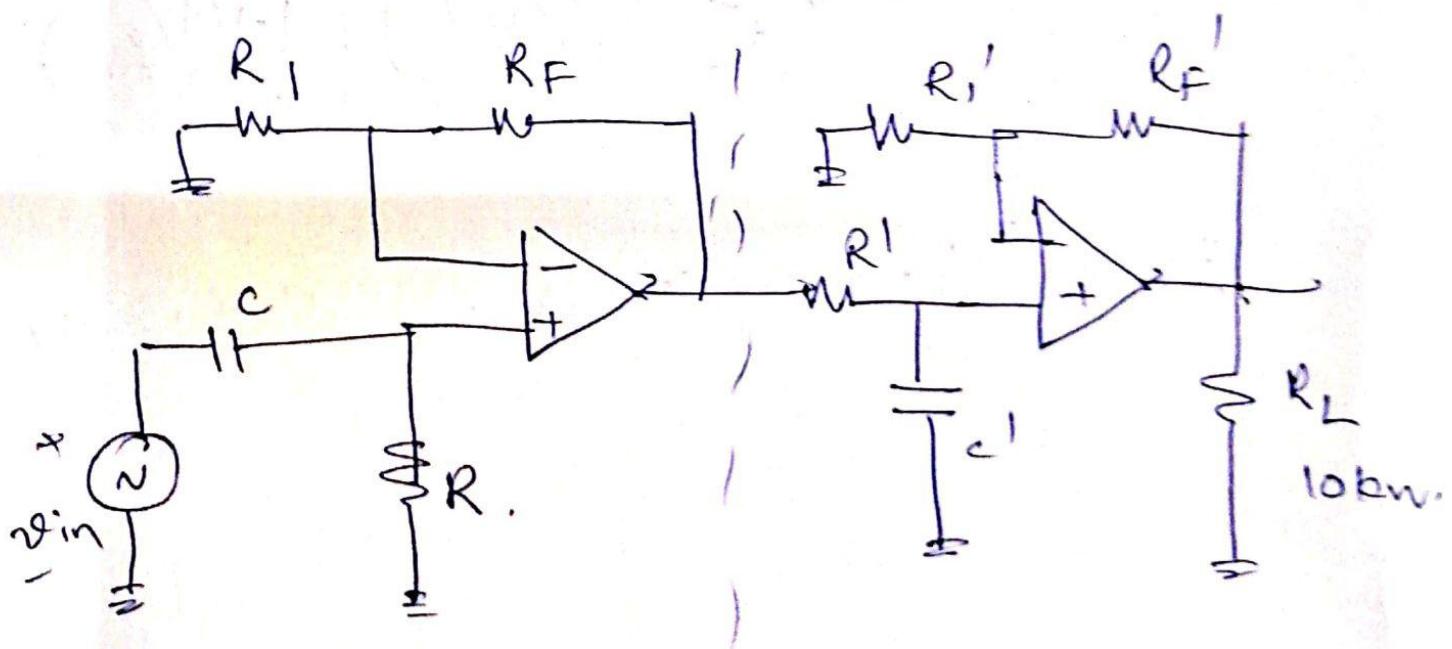
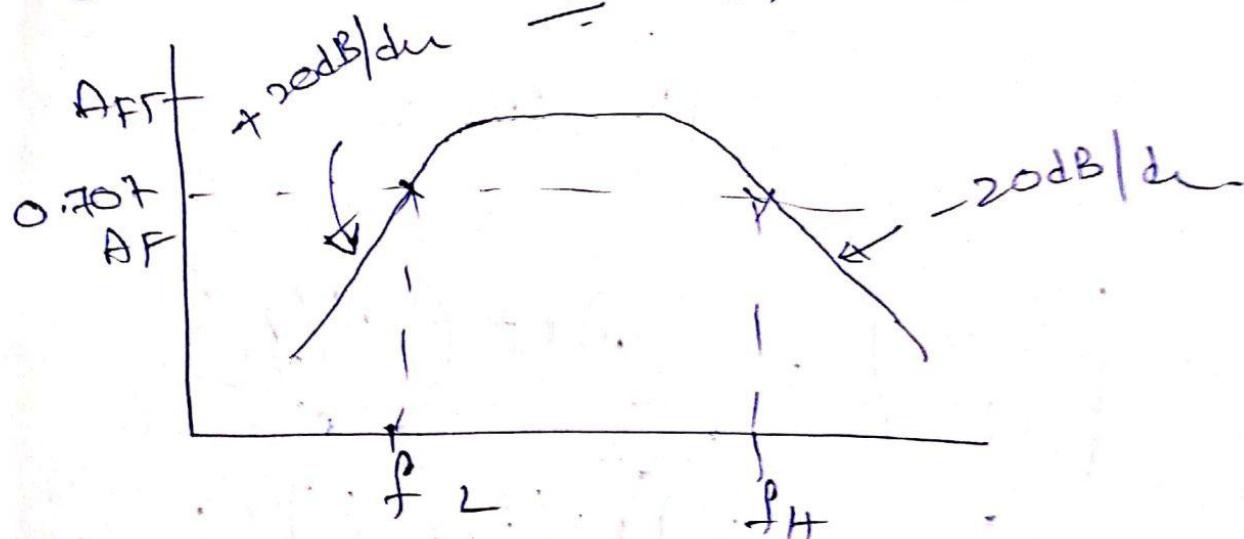
Block dia of a power Supply

9



(18)

- ② Design a Butterworth Active
 First
decomⁿ order Band pass filter
 whose higher and lower cutoff
freq are $f_L = 200\text{Hz}$, $f_H = 1\text{kHz}$
and pass band gain = 4.
 Draw the freq response.



First order \rightarrow HPF First order \rightarrow LPF

Design Case

$$1. f_L = 200 \text{ Hz}$$

$$\text{Let } C = 0.05 \mu\text{F}$$

$$\text{Then } R = \frac{1}{2\pi f_L C} = \frac{1}{2\pi (200)(5)(10^{-6})} \\ = 15.9 \text{ k}\Omega.$$

$$③ \left| \frac{V_o}{V_{in}} \right| = \frac{A_{FF}(f/f_L)}{\sqrt{\left[1 + \left(\frac{f}{f_L}\right)^2\right] \left[1 + \left(\frac{f}{f_m}\right)^2\right]}}$$

$$f_c = \sqrt{(1000)(200)} = 447.2 \text{ Hz.}$$

freq

Response

10¹ Hz

Gain

$$\frac{V_o}{V_m}$$

gain mag (dB)

20 log ($\frac{V_o}{V_m}$)

20

50

100

200

[f_L]

f_H

Voltage Regulator.

①

The function of a voltage regulator is to provide a stable dc voltage for powering other electronic circuits. A voltage regulator should be capable of providing substantial output current.

- * Series regulator: (a) linear regulator
- * switching regulator:

- * Series regulators use a power transistor connected in series between the unregulated input and the load.
- * The output voltage is controlled by the continuous voltage drop taking place across the series pass transistor.
- * Since the transistor conducts in the active or linear region, these regulators are also called linear regulators.
- * Linear regulators may have fixed or variable output voltage and could be positive or negative.
- * The schematic, important characteristics, data sheet, short circuit protection,

(2)

current fold-back, current boosting techniques for linear voltage regulation such as 78xx Series, 723 Ic are discussed.

Series op-amp Regulator

A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature and ac line voltage variations.

Fig shows a regulated power supply using discrete components. The circuit consists of following four parts

1. Reference Voltage circuit.

2 Error amplifier.

3 Series pass transistor

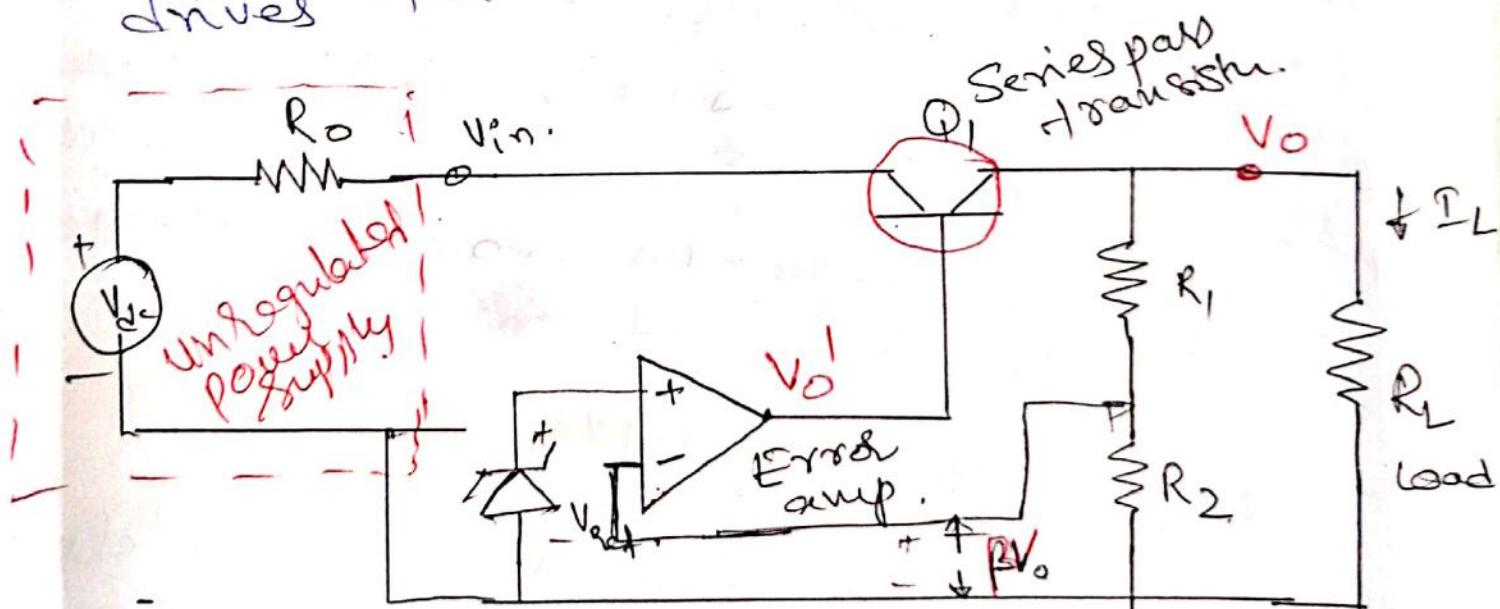
4. Feed back network.

The power transistor Q₁ is in series with the unregulated dc voltage V_{in} and the regulated output voltage V_o , so it must absorb the difference between these two voltages whenever any fluctuation in output voltage V_o .

(3)

The transistor Q_1 is also connected as an emitter follower and therefore provides sufficient current gain to drive the load.

The output voltage is sampled by the $R_1 - R_2$ divider and fed back to the (-) op-amp terminal of the op-amp error amplifier. This sampled voltage is compared with the reference voltage V_{ref} (usually obtained by a zener diode). The output V'_o of the error amplifier drives the series transistor Q_1 .



$$\beta = \frac{R_2}{R_1 + R_2}$$

(4)

if the output voltage increases, due to variation in load current, the sampled voltage βV_o also increases where

$$\beta = \frac{R_2}{R_1 + R_2}$$

This in turn, reduces the output voltage V_o' of the differen amp due to the 180° phase differen provided by the op-amp amplifier. V_o' is applied to the base of Q_1 , which is used as an emitter follower. So V_o follows V_o' , that is V_o also decreases. Hence the increase in V_o is nullified. Similarly, reduction in output voltage also gets regulated.

IC Voltage Regulators.

With the advent of micro-electron it is possible to incorporate the complete circuit on a monolithic silicon chip. This gives low cost, high reliability, reduction in size and excellent performance.

Examples of monolithic regulators are 78XX/79XX Series and 723 general purpose regulators.

J23 General purpose Register

The three terminal regulators have the following limitations.

1. No short circuit protection.
 2. output Voltage is fixed ($+ve$ or $-ve$).

These limitations have been overcome in the μ 23 general purpose regulators, which can be adjusted over a wide range of both positive or negative regulated voltages.

- * The limitation of 723 is that it has no in-built thermal protection.

* It has no short circuit current limit.

The Zener diode, a constant current source and reference amplifier produce a fixed voltage of about 7 V

at the terminal V_{ref} .

The constant current source forces the Zener to operate at a fixed point so that the Zener outputs a fixed voltage.

The other section of the IC consists of an error amplifier, a series pass transistor Q_1 , and a current limit transistor Q_2 .

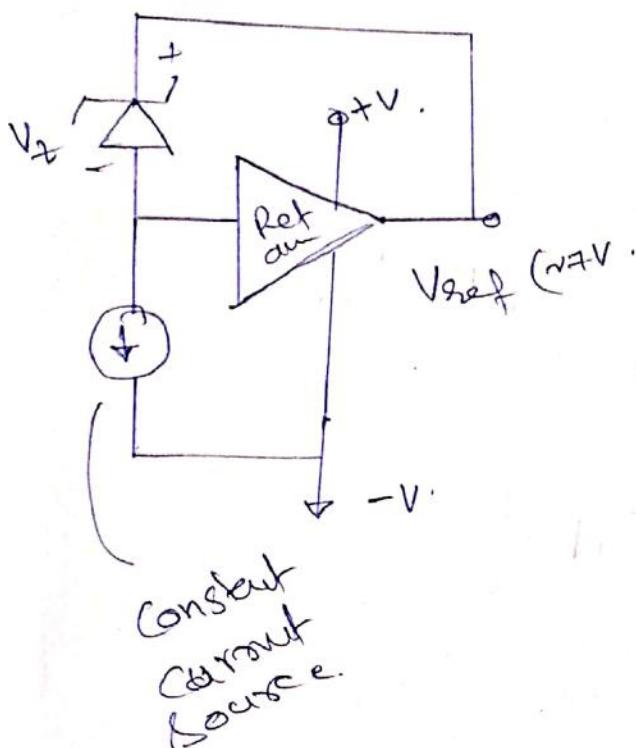
The error amplifier compares a sample of the output voltage applied at the INV input terminal to the ref voltage applied at the NI input terminal.

* The error signal controls the condition of Q_1 .

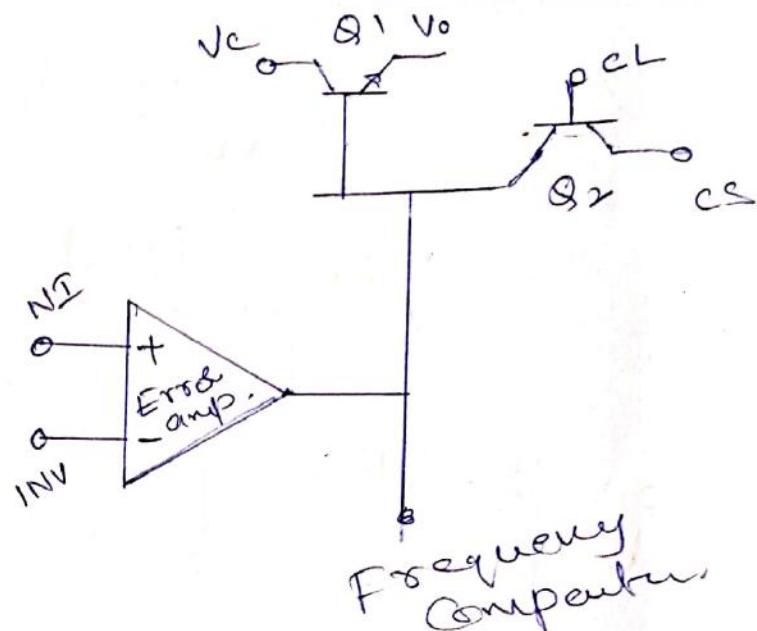
* These two sections are not internally connected but the various points are brought out on the IC package.

#23 regulator IC is available in a 14-pin dual-in-line package or 10-pin metal can shown in Fig

Functional block diagram of 723 regulator

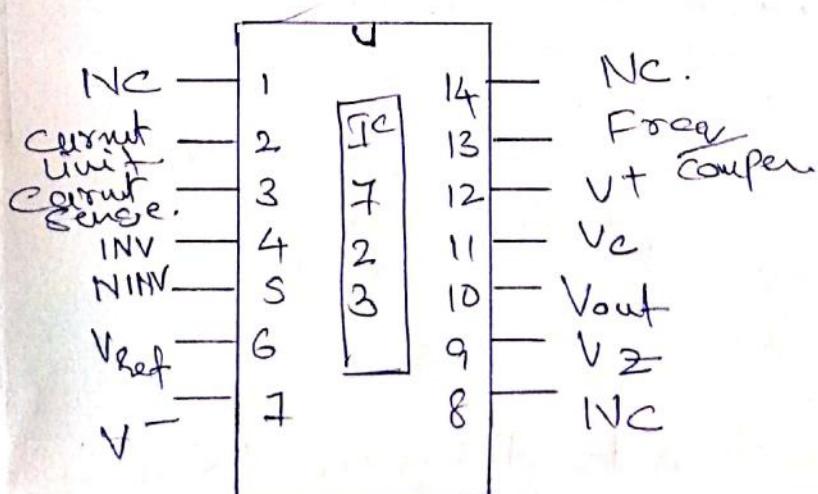


(Section 1)



(Section 2)

Functional block diagram of 723 regulator



8

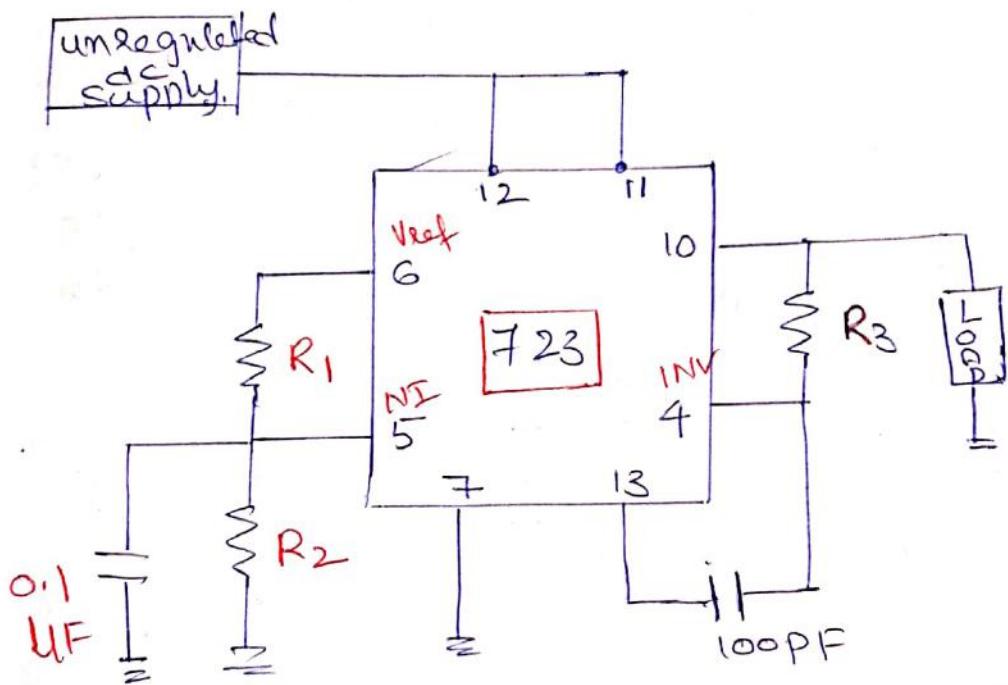


Fig :-(a) A Low Voltage Regulator Using 723 IC.

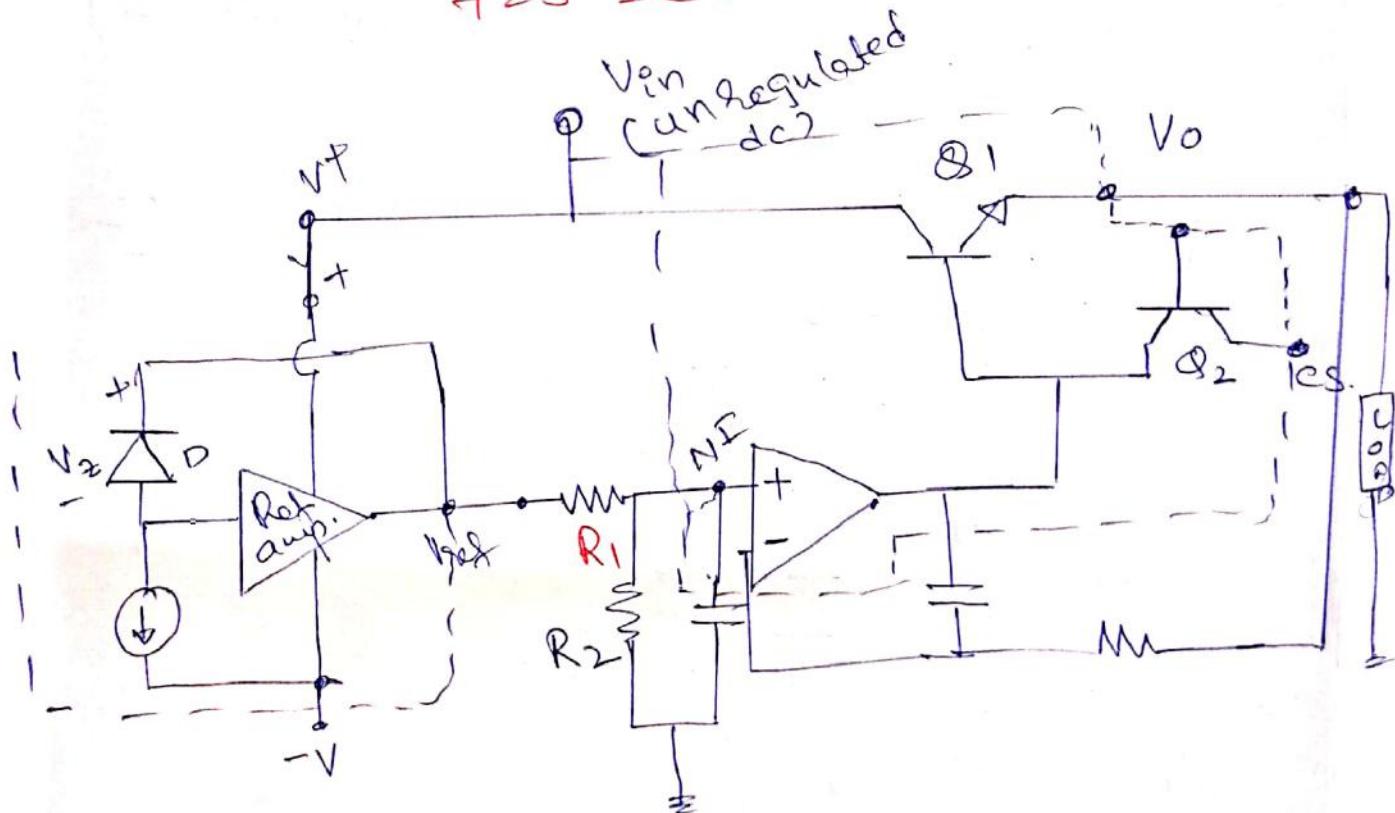


Fig: (b) Functional diagram for a low voltage regulator.

(9)

A simple low voltage (2V to 7V) regulator can be made using 723 as shown in Fig.

The voltage at the NI terminal of the error amplifier due to $R_1 R_2$ divider is

$$V_{NI} = V_{ref} \cdot \frac{R_2}{R_1 + R_2}$$

The difference V_{NI} and the output voltage V_o which is directly fed back to the INV terminal is amplified by the error amplifier.

The output of the error amplifier drives the pass transistor Q_1 , so as to minimize the difference between the NI and INV inputs of error amplifier since Q_1 is operating as an emitter follower.

$$V_o = V_{ref} \cdot \frac{R_2}{R_1 + R_2}$$

If the output voltage becomes low, the voltage at the INV terminal of error amplifier also goes down. This makes the output of the error amp

more positive, thereby driving transistor Q₁ more into conduction.

This ~~decreases~~ ^{reduces} the voltage across Q₁ and drives more current into the load causing voltage across load to increase. So the initial drop in the load voltage has been compensated. Similarly, any increase in the load or changes in the I/P voltage get regulated.

The reference voltage is typically 7.15V. So the output voltage V_O

$$\therefore V_O = 7.15 \times \frac{R_2}{R_1 + R_2}$$

which is always less than 7.15V. So the circuit shown in Fig(a) is used as a low voltage regulator (< 7V).

It is desired to produce regulated output voltage greater than 7V, then the circuit shown in Fig(c) is used.

(11)

The NI terminal is connected directly to V_{ref} through R_3 . So the voltage at the NI terminal is V_{ref} . The erod amplifier operates as a Non-Inverting amplifier with a voltage gain of

$$A_V = 1 + \frac{R_1}{R_2}$$

So the o/p voltage for the ckt is

$$V_o = 7.15 \left(1 + \frac{R_1}{R_2} \right)$$

