

7.1 Introduction

Digital circuits are invariably constructed with integrated circuits. An integrated circuit (abbreviated as IC) is a small silicon semiconductor crystal, called a chip, containing electrical components such as transistors, diodes, resistors and capacitors. The digital integrated circuits operate with binary signals and are made up of interconnected digital gates.

Now-a-days digital integrated circuits are most commonly used in the modern digital system. They provide following advantages.

ICs pack a lot more circuitry in a small package, so that the overall size of almost any digital system is reduced.

- The cost of ICs is very low, which makes them economical to operate.
- They have high reliability against failure, so the digital system needs less repair.
- Their reduced power consumption makes the digital system more economical to operate.
- The operating speed is higher, which makes them suitable for high-speed operations.
- The use of ICs reduces the number of external wiring connections because many of them are internal to the package.

With the widespread use of ICs, it becomes necessary to know and understand the electrical characteristics of the most common IC logic families such as TTL (Transistor-Transistor Logic), ECL (Emitter Coupled Logic), MOS (Metal-Oxide Semiconductor), CMOS (Complementary Metal-Oxide Semiconductor) and I²L or I²L (Integrated-Injection Logic). These logic families differ in the major components that they use in their circuitry. TTL and ECL use bipolar transistors as their major circuit element; MOS and CMOS use unipolar MOSFET transistors as their principle component. Because of the use of different principle component their characteristics are different.

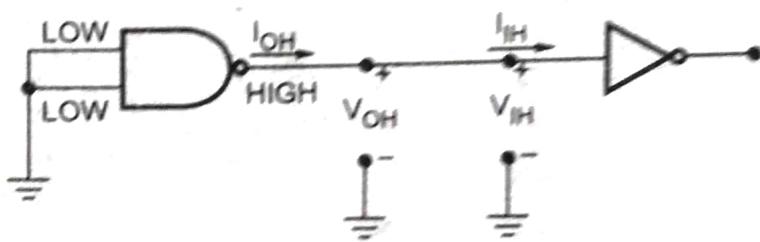
In this chapter we will study the important characteristics of DTL, RTL, TTL, CMOS, I²L and ECL families and their subfamilies.

7.2 Definition of Parameters

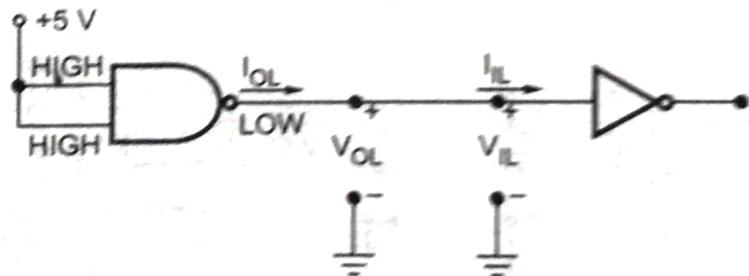
We know that there are various logic families. This logic families can be categorised as saturated and non-saturated logic families. In saturated logic families transistor (switching element) is driven into saturation. In non-saturated logic families transistor (switching element) is prevented to drive into saturation. Saturated logic families consume low power but they are slower. On the other hand non-saturated logic families are faster but their power consumption is more. Before going to discuss them, we see the nomenclature and terminologies used by them, and the most useful terms related to them.

7.2.1 Current and Voltage Parameters

$V_{IH(min)}$ - High-Level Input Voltage : It is the minimum voltage level required for a logical 1 at an input. Any voltage below this level will not be accepted as a HIGH by the logic circuit.



(a)



(b)

Fig. 7.1 Currents and voltages in the two logic states

$V_{IL(max)}$ - Low-Level Input Voltage : It is the maximum voltage level required for a logic 0 at an input. Any voltage above this level will not be accepted as a LOW by the logic circuit.

$V_{OH(min)}$ - High-Level Output Voltage : It is the minimum voltage level at a logic circuit output in the logical 1 state under defined load conditions.

$V_{OL(max)}$ - Low-Level Output Voltage : It is the maximum voltage level at a logic circuit output in the logical 0 state under defined load conditions.

I_{IH} - **High-Level Input Current**: It is the current that flows into an input when a specified high-level voltage is applied to that input.

I_{IL} - **Low-Level Input Current**: It is the current that flows into an input when a specified low-level voltage is applied to that input.

I_{OH} - **High-Level Output Current**: It is the current that flows from an output in the logical 1 state under specified load conditions.

I_{OL} - **Low-Level Output Current**: It is the current that flows from an output in the logical 0 state under specified load conditions.

Note : The current directions shown in the Fig. 7.1 may be opposite to those shown depending on the logic family.

7.2.2 Fan Out

In a digital system, we typically find many types of digital ICs interconnected to perform various functions. In these situations, the output of a logic gate may be connected to the inputs of several other similar gates. The maximum number of inputs of several gates that can be driven by the output of a logic gate is decided by the parameter called fan-out. In general, the fan-out is defined as the maximum number of inputs of the same IC family that the gate can drive maintaining its output levels within the specified limits. For example, a logic gate with fan-out 10 can drive maximum 10 logic inputs from the same family.

7.2.3 Noise Margin

In digital circuits, the binary 0 and 1 are represented by a pair of voltage levels. Each logic family has a different standard. The Table 7.1 shows the voltages used by several families.

Family	Logic 0	Logic 1
TTL	0 V	+ 5 V
ECL	- 1.7 V	- 0.9 V
CMOS	0 V	3 – 15 V

Table 7.1

These are the ideal voltage levels. But in practice, it is difficult to get these ideal voltages. Stray electric and magnetic field can induce voltages on the connecting wires between logic circuits. These unwanted signals are called noise, and can sometimes cause the voltage at the input to a logic circuit to drop below $V_{IH(min)}$ or rise above $V_{IL(max)}$, which could produce unpredictable operation. The noise immunity of a logic circuit refers to the circuit's ability to tolerate the noise without causing spurious changes in the output voltage. To avoid this problem due to noise, voltage level $V_{IH(min)}$ is kept a few fraction of

volts below $V_{OH(\min)}$ and voltage level $V_{IL(\max)}$ is kept above $V_{OL(\max)}$, at the design time. This is illustrated in Fig. 7.2.

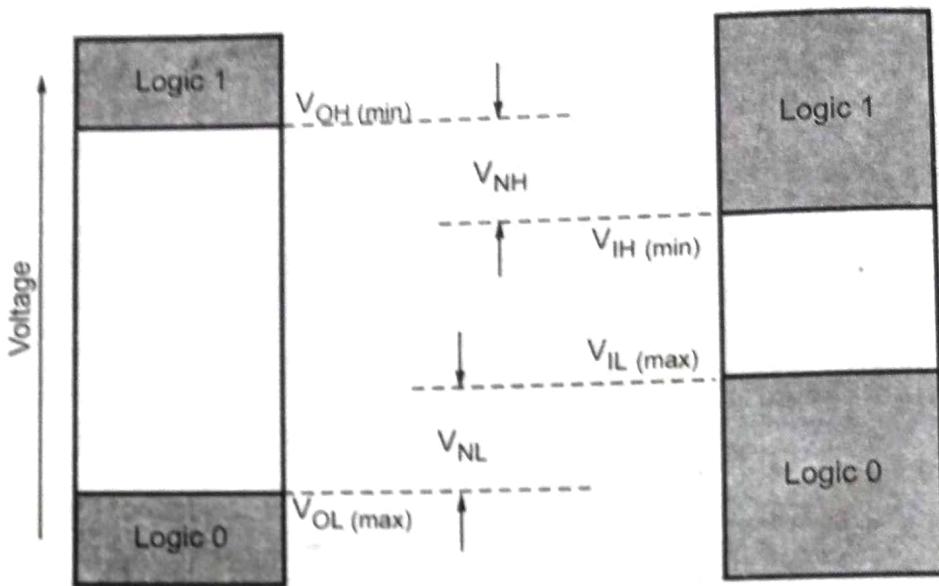


Fig. 7.2 Noise margins

As shown in Fig. 7.2, V_{NH} is the difference between the lowest possible HIGH output, $V_{OH(\min)}$ and the minimum voltage, $V_{IH(\min)}$ required for a HIGH input. This voltage difference, V_{NH} is called high-state noise margin. Similarly, we have low-state noise margin. It is the voltage difference between the largest possible low output, $V_{OL(\max)}$ and the maximum voltage, $V_{IL(\max)}$ required for a LOW input.

In short we can write as,

$$V_{NH} = V_{OH(\min)} - V_{IH(\min)} \text{ and}$$

$$V_{NL} = V_{IL(\max)} - V_{OL(\max)}$$

The noise margin allows the digital circuit to function properly if noise voltages are within the limits of V_{NH} and V_{NL} for a particular logic family.

7.2.4 Propagation Delay

The propagation delay of a gate is basically the time interval between the application of an input pulse and the occurrence of the resulting output pulse. The propagation delay is a very important characteristic of logic circuits because it limits the speed at which they can operate. The shorter the propagation delay, the higher the speed of the circuit and vice-versa. There are two propagation delays associated with logic gates.

1. t_{PLH} :It is the delay time measured when output is changing from logic 0 to logic 1 state (LOW to HIGH)
2. t_{PHL} : It is the delay time measured when output is changing from logic 1 to logic 0 state (HIGH to LOW).

Fig. 7.3 illustrates these propagation delay times for both inverted and non-inverted outputs.

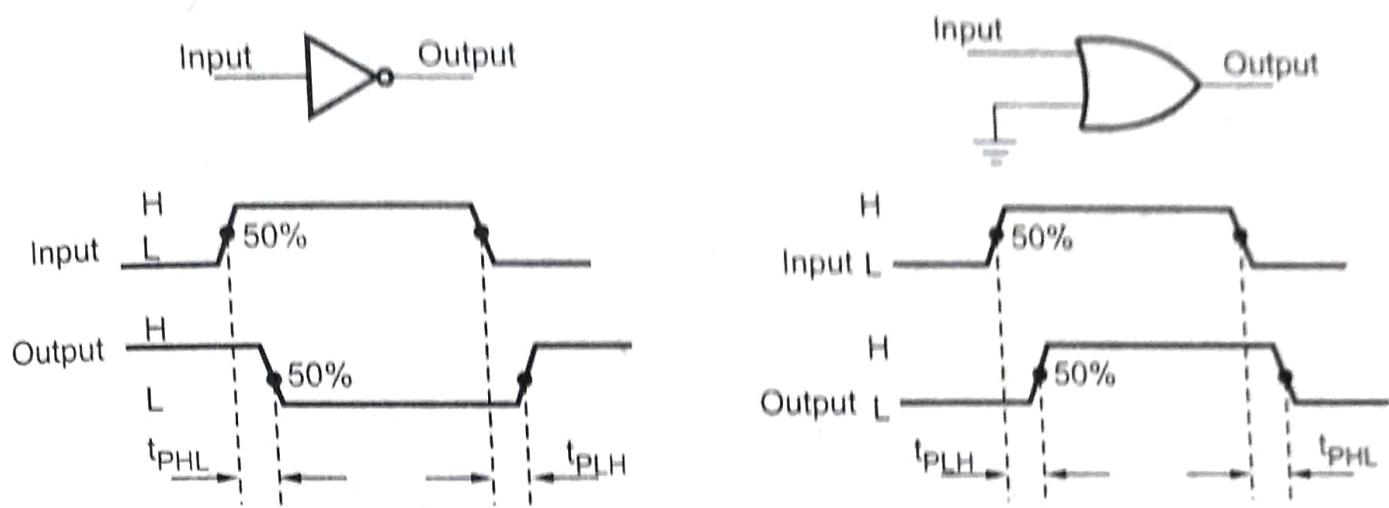


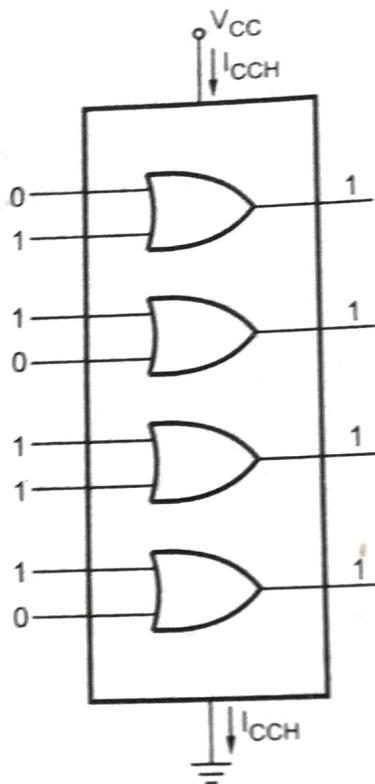
Fig. 7.3 Propagation delay times

As shown in the Fig. 7.3 propagation delays are measured between the 50 percent points on the input and output transitions. The values of propagation times t_{PHL} and t_{PLH} may not be same and both will vary depending on the capacitive load conditions. When t_{PHL} and t_{PLH} are not equal, the larger value is considered as a propagation delay time for that logic gate.

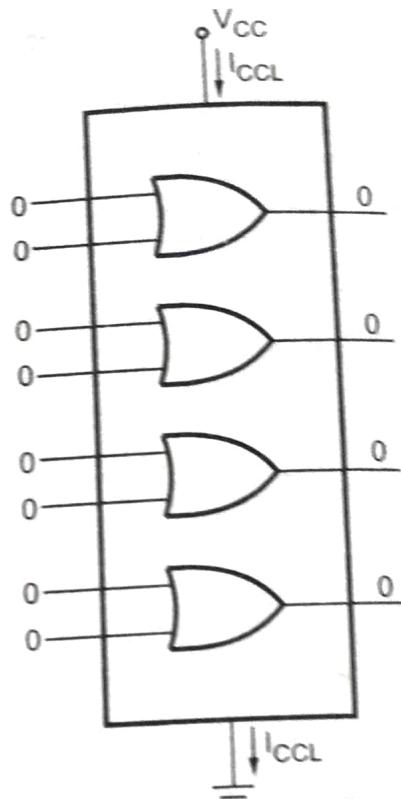
7.2.5 Power Dissipation

Every IC requires a certain amount of electrical power to operate. This power is supplied by one or more power-supply voltages connected to the power pin(s) on the chip. The amount of power that an IC dissipates is determined by the average supply current, I_{CC} , that it draws from the V_{CC} supply. It is the product of I_{CC} and V_{CC} . For many ICs, the value of I_{CC} for a LOW gate output is higher than for a HIGH output. Therefore the current drain on the supply depends on the logic states of the circuits on the chip. For example, Fig. 7.4 (a) shows an OR gate chip where all the gate outputs are HIGH. The current drain on the V_{CC} supply for this case is called I_{CCH} . Similarly, Fig. 7.4 (b) shows the current drain when all the gate outputs are LOW. This current is called I_{CCL} . The manufacturer's data sheet usually specifies values for I_{CCH} and I_{CCL} . The average I_{CC} is determined based on the 50% duty cycle operation of the gate (LOW half of the time and HIGH half of the time).

$$I_{CC(\text{avg})} = \frac{I_{CCH} + I_{CCL}}{2}$$



(a)



(b)

Fig. 7.4 Currents I_{CCH} and I_{CCL}

This can be used to calculate average power dissipation as

$$P_{D(\text{avg})} = I_{CC(\text{avg})} \times V_{CC}$$

Ex. 7.1 : A certain gate draws 1.8 mA when its output is HIGH and 3.2 mA when its output is LOW. What is its average power dissipation if V_{CC} is 5 V and it is operated on a 50% duty cycle?

Sol. : The average I_{CC} is given as

$$\begin{aligned} I_{CC(\text{avg})} &= \frac{I_{CCH} + I_{CCL}}{2} \\ &= \frac{1.8 + 3.2}{2} \\ &= 2.5 \text{ mA} \end{aligned}$$

Then average power dissipation is given as

$$\begin{aligned} P_{D(\text{avg})} &= I_{CC(\text{avg})} \times V_{CC} \\ &= 2.5 \text{ mA} \times 5 \text{ V} \\ &= 12.5 \text{ mW} \end{aligned}$$

7.2.6 Speed Power Product (Figure of Merit)

In general, for any digital IC, it is desirable to have shorter propagation delays (higher speed) and lower values of power dissipation. There is usually a trade-off between switching speed and power dissipation in the design of a logic circuit i.e. speed is gained at the expense of increased power dissipation. Therefore, a common means for measuring and comparing the overall performance of an IC family is the **speed-power product (SPP)**. It is also called **Figure of Merit**.

Actually, the speed-power product is computed as the product of propagation delay and average power dissipation, so the smaller the product, the better the overall performance. Notice that the product of propagation delay in seconds and power dissipation in watts (joules per second) has the units of energy - i.e. joules (J).

$$\therefore \text{Speed-power product (J)} = \text{Propagation delay (Seconds)} \times \text{Power dissipation (Joules/seconds)}$$

Ex. 7.2 : For a certain IC family, propagation delay is 10ns with an average power dissipation of 6 mW. What is its speed power product ?

Sol. : The speed-power product is given as

$$\begin{aligned} \text{SPP} &= \text{propagation delay} \times \text{average power dissipation} \\ &= 10 \text{ ns} \times 6 \text{ mW} \\ &= 60 \text{ pico joules (pJ)} \end{aligned}$$

In this section we have seen definition of various parameter/characteristics of logic families. In the next sections we are going to study various logic families.

7.3 Resistor - Transistor Logic (RTL)

We begin our discussion of logic gates by considering the resistor-transistor-logic (RTL) gate. Although RTL has become obsolete now, because of its simplicity and for historical reasons, it is proper to devote some attention to it and develop concepts useful in connection with all types of gates.

7.3.1 RTL Circuit

RTL circuits consist of resistors and transistors. Fig. 7.5 shows 2-input RTL NOR gate. As shown in the Fig. 7.5, emitters of both the transistors are connected to a common ground and collectors of both transistors are tied through a common collector resistor R_C to a supply voltage V_{CC} . The resistor R_C is commonly known as **passive pull-up resistor**.

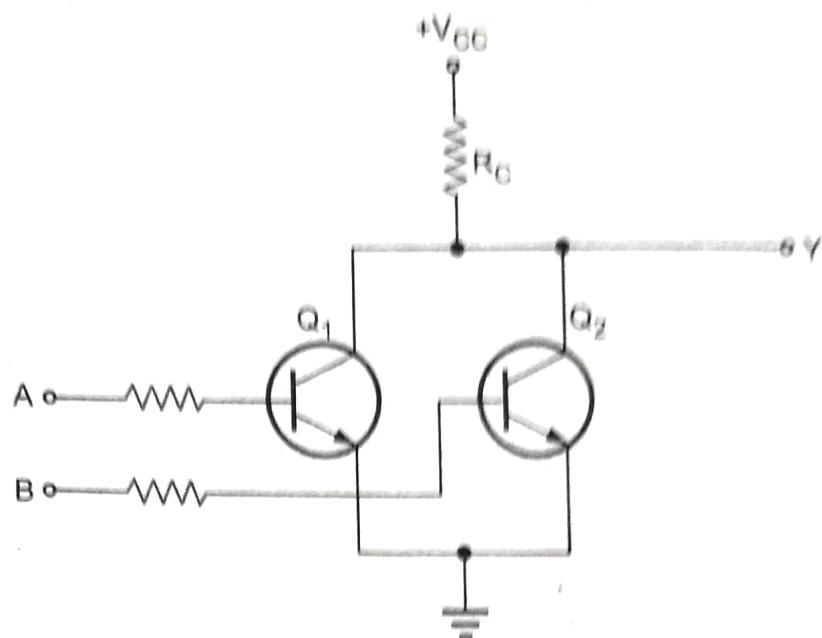


Fig. 7.5 2-input RTL NOR gate

7.3.2 Circuit Operation

Inputs representing logic levels are applied at A and B terminals. In the RTL gate the input voltage corresponding to LOW level is required to be low enough for the corresponding transistor to be cut off. Similarly, the input voltage corresponding to HIGH level should be high enough to drive the corresponding transistor to saturation.

When both the inputs are Low, transistors Q_1 and Q_2 are cut-off and the output is HIGH. A HIGH level on any input drives the corresponding transistor to saturation causing the output to go LOW. Table 7.2 shows the truth table for 2-input NOR gate.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Table 7.2 Truth table for 2-input NOR gate

We know that, the saturation voltage, $V_{CE(sat)}$ for transistor is approximately 0.2 V. Therefore, for RTL gates the LOW level output voltage is 0.2 V. In RTL a HIGH level output voltage depends on the number of gates connected to the output. As number of gates connected to the output increases, output voltage decreases. This is the deciding

factor for the fan-out of the gate. The number of gates connected to the output also affects the propagation delay time.

7.3.3 Specifications

The table 7.3 gives the specifications for RTL gate.

Parameter	Value
Propagative Delay	12 nsec
Power Dissipation	30-100 mW
Noise Margin	0.2 volts
Fan-out	4

Table 7.3 Specifications for RTL gate

From above specifications we can say that RTL gates have poor noise margin, poor fan-out capabilities, low speed and high power dissipation.

7.3.4 Wire-AND Connection

The RTL has a capacity called **wire - AND**. Since the output is effectively a transistor, two outputs can be wired together. This is illustrated in Fig. 7.6.

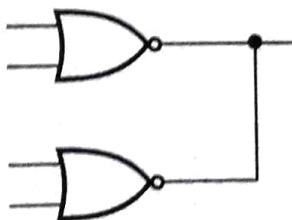


Fig. 7.6 Wired AND RTL NOR gates

7.4 Diode-Transistor Logic (DTL)

The diode - transistor logic, DTL is somewhat more complex than RTL but because of its greater fan-out and improved noise margins it has replaced RTL.

7.4.1 DTL Circuit

The Fig. 7.7 shows a discrete circuit for DTL NAND gate. It consists of input diodes and resistor R_D forming an AND gate and following them is transistor inverter.

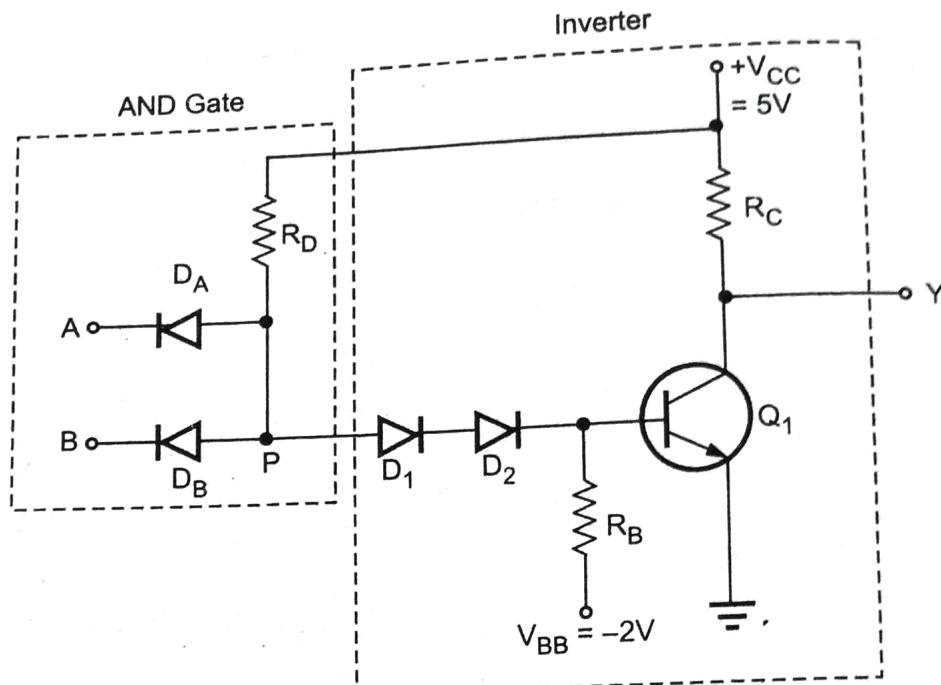


Fig. 7.7 2-input DTL NAND gate

7.4.2 Circuit Operation

When both inputs are LOW, diode D_A and D_B conduct resulting 0.7 volts at point P. This 0.7 voltage at point P is not sufficient to drive transistor Q_1 . Therefore, Q_1 is cut off giving output voltage $V_O = V_{CC}$ logic 1. A LOW level on any input cause corresponding diode to conduct resulting voltage at point P = 0.7 V.

This causes transistor to remain in cut-off and the output voltage is equal $V_{CC} = \text{logic 1}$. When both inputs are logic HIGH, diodes D_A and D_B are reversed biased. This causes the base current of transistor Q_1 to flow through R_D , D_1 , D_2 and the base of the transistor Q_1 . This drives transistor Q_1 in saturation giving output voltage = $V_{CE(\text{sat})} = 0.2 \text{ V} = \text{logic 0}$.

For driving transistor Q_1 is saturation we require more than $2.1 \text{ V} (V_{D_1}(0.7) + V_{D_2}(0.7) + 0.7(V_{BE}))$ at point P to drive transistor in saturation. Therefore, we can say that due to diodes D_1 and D_2 we need increased voltage level to drive transistor in saturation. This improves the noise margin for DTL gate.

When A and B inputs are HIGH, transistor Q_1 is driven in saturation and its base to emitter junction capacitance is charged. Now if any of the input goes low, voltage at point P becomes 0.7 V and transistor Q_1 will try to come out of saturation. To drive transistor from saturation to cut-off it is necessary to discharge the stored charge on the internal capacitance. The resistance, R_B provides a discharge path for the charged stored in the transistor. Resistor R_B is connected to the -2V supply to increase the rate of discharge.

7.4.3 Specifications

Table 7.4 gives the specifications for DTL gate

Parameter	Value
Power dissipation	60 mW
Propagation Delay	30 nsec
Noise Margin	0.7 volts
Fan out	8

Table 7.4 Specification for DTL gate

From the above specifications we can say that the DTL has the advantage of greater fan-out and improved noise margins, but it suffers from somewhat lower speed.

7.4.4 Wire-AND connection

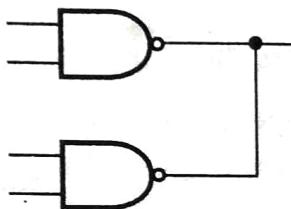


Fig. 7.8 Wired AND DTL NAND gates

Like RTL, the DTL also has a capacity called wire-AND. In DTL two outputs can be connected together as shown in the Fig. 7.8.

7.4.5 Modified Integrated DTL NAND Gate

To increase the fanout of DTL gate the base current of T_1 has to be increased. It is increased by replacing diode D_1 by a transistor, as shown in the Fig. 7.9(a). (See Fig on next page)

7.5 High-threshold Logic (HTL)

High-threshold logic (HTL) is an improved version of DTL logic. The improvement is done to handle the noise levels in the industrial environment such as presence of electric motor, on-off control circuits, high voltage switches and so on. The DTL gate discussed in the previous section is redesigned with a higher supply voltage 15 V instead of 5 V, the diode D_2 has been replaced by a zener diode with a zener breakdown voltage of 6.9 V and the resistance have been modified so that approximately the same currents are obtained as in DTL.

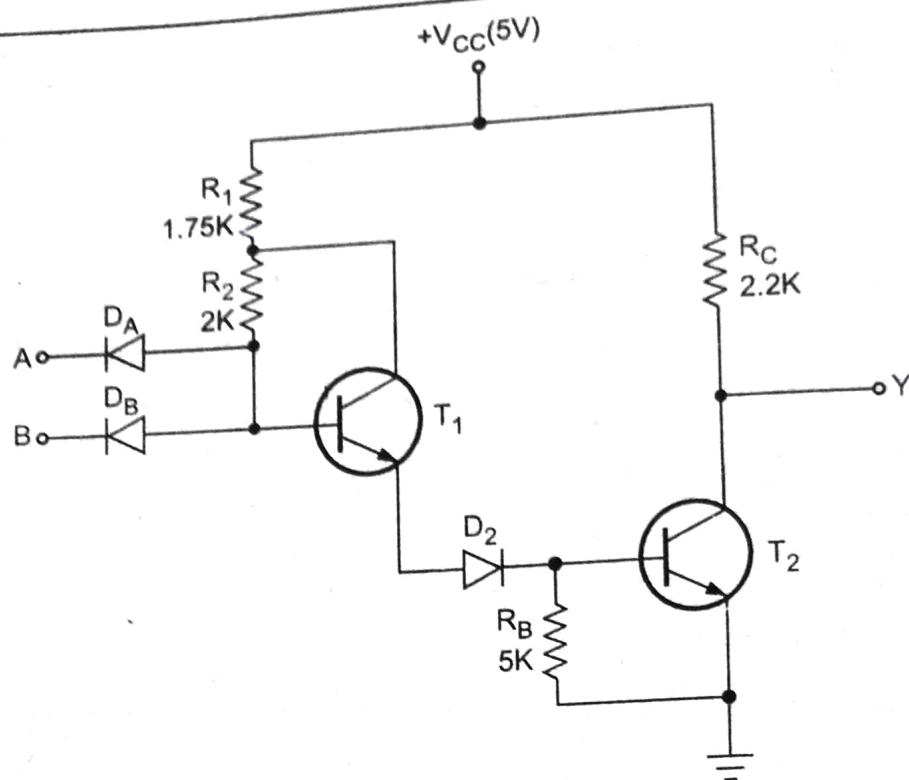


Fig. 7.9 (a) Modified 2-input DTL NAND gate

Because of the use of high resistance values the propagation delay of HTL family is high. It is as high as hundreds of nano-seconds. However, the temperature sensitivity of the HTL gate is considerably less than that of DTL. Fig. 7.9(b) shows the HTL NAND gate.

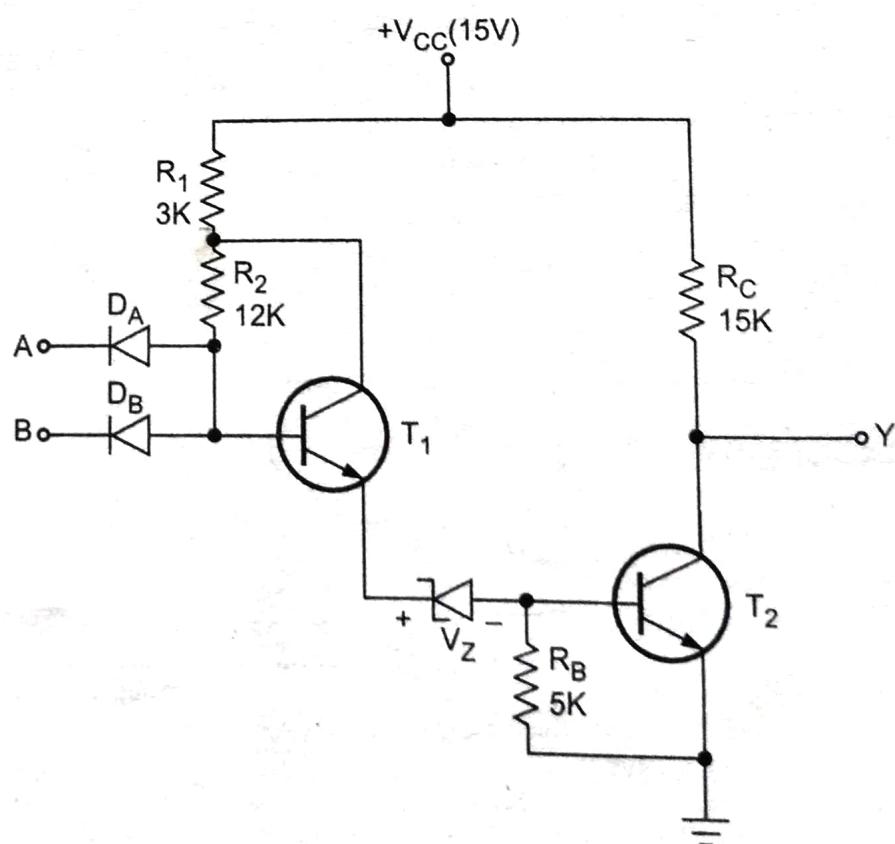


Fig. 7.9 (b) HTL NAND gate

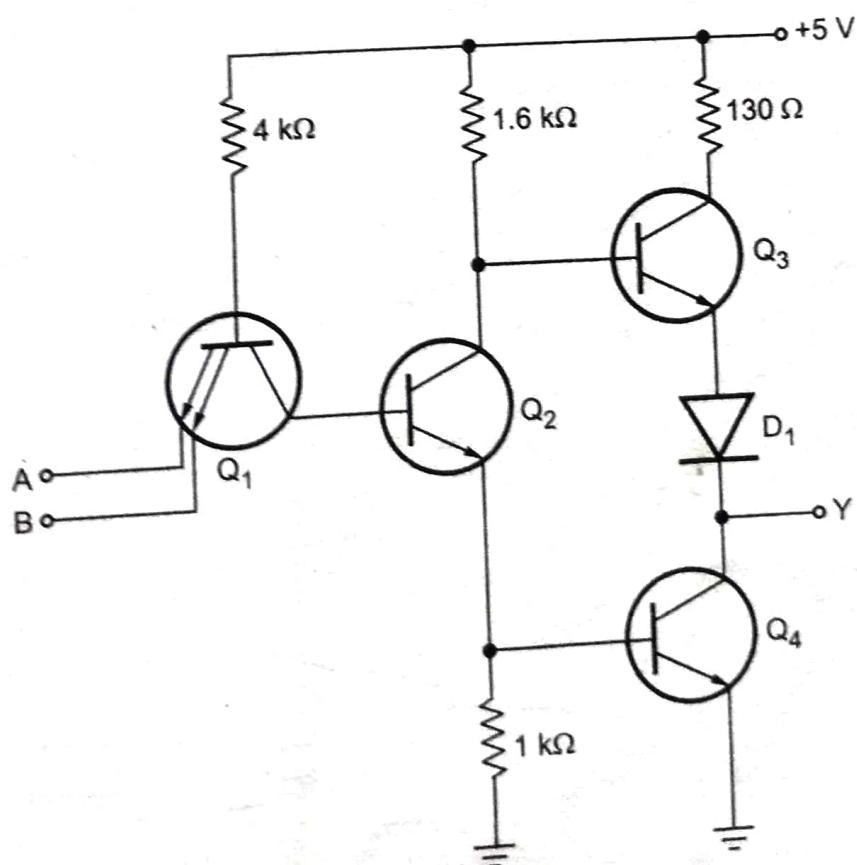
7.6 TTL

Transistor-transistor logic, TTL, is named for its dependence on transistors alone to perform basic logic operations. The first version, which is now known as standard TTL, was developed in 1965 and is rarely used in today's systems. Through the years, the basic design has been modified to improve its performance in several respects, and as a consequence, a number of subfamilies have evolved. In this section we are going to study the basic transistor configurations in TTL and its subfamily circuits along with their characteristics.

Fig. 7.10 (a) shows a transistor configuration for the standard TTL circuit. In particular, this configuration is a two input NAND gate.

7.6.1 Multiple-Emitter Transistor

Looking at the Fig. 7.10 (a) it can be noticed that Q_1 is an NPN transistor having two emitters, one for each input to the gate. Although this circuit looks complex, we can simplify its analysis by using the diode equivalent of the multiple-emitter transistor Q_1 , as shown in Fig. 7.10 (b). Diodes D_2 and D_3 represent the two E-B junctions of Q_1 and D_4 is the collector-base (C-B) junction.



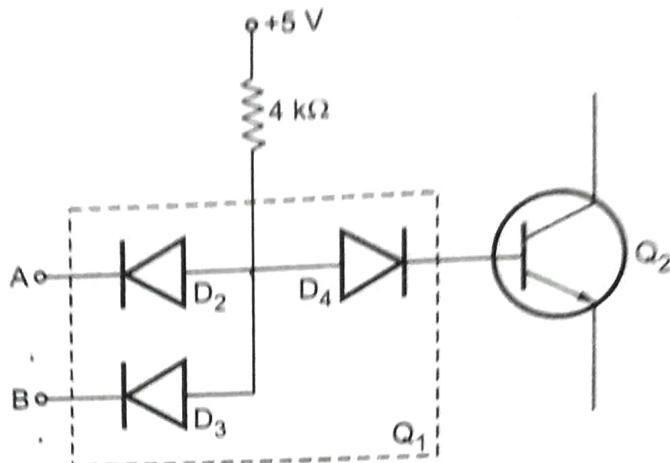


Fig. 7.10 (b) Diode equivalent for Q_1

The input voltages A and B are either LOW (ideally grounded) or HIGH (ideally 5 volts). If either A or B or both are low, the corresponding diode conducts and the base of Q_1 is pulled down to approximately 0.7 V. This reduces the base voltage of Q_2 to almost zero. Therefore, Q_2 cuts off. With Q_2 open, Q_4 goes into cutoff, and the Q_3 base is pulled HIGH. Since Q_3 acts as an emitter follower, the Y output is pulled up to a HIGH voltage. On the other hand, when A and B both are HIGH, the emitter diodes of Q_1 are reversed biased making them off. This causes the collector diode D_4 to go into forward conduction. This forces Q_2 base to go HIGH. In turn, Q_4 goes into saturation, producing a low output. Table 7.5 summarizes all input and output conditions.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Table 7.5 Truth table for 2-input NAND gate

Without diode D_1 in the circuit, Q_3 will conduct slightly when the output is low. To prevent this, the diode is inserted; its voltage drop keeps the base-emitter diode of Q_3 reverse-biased. In this way, only Q_4 conducts when the output is low.

7.6.2 Totem-Pole Output

Fig. 7.11 shows an high lighted output configuration. Transistor Q_3 and Q_4 form a totem-pole. Totem-pole transistors are used because they produce a LOW output impedance. Either Q_3 acts as an emitter follower (HIGH output), or Q_4 is saturated (LOW output). When Q_3 is conducting, the output impedance is approximately 70Ω ; when Q_4 is saturated, the output impedance is only 12Ω . Either way, the output impedance is low.

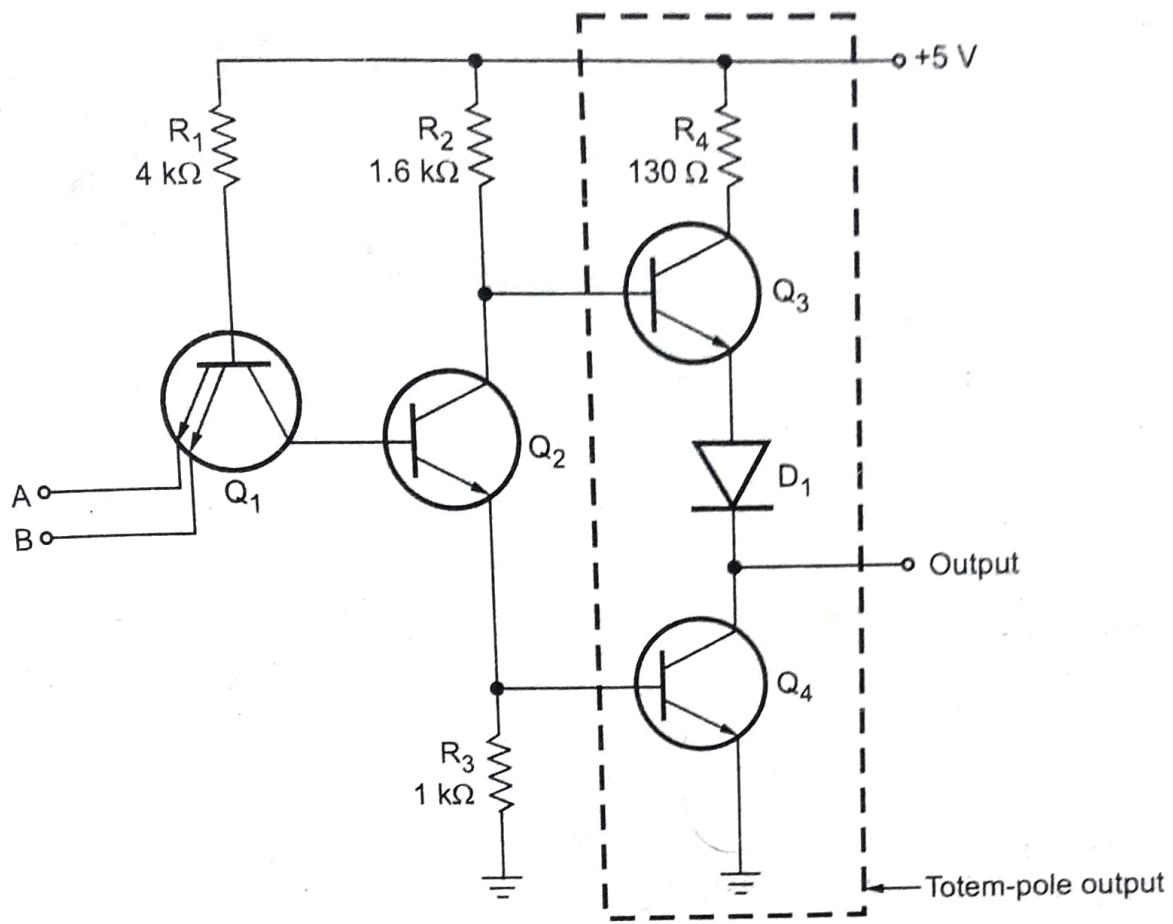


Fig. 7.11 Two input NAND gate with totem-pole output

This means that the output voltage can change quickly from one state to the other because any stray output capacitance is rapidly charged or discharged through the low output impedance.

Fig. 7.12 shows static analysis of one gate in a 7400 quad 2-input NAND gate, including the totem-pole output. Here diodes D_2 and D_3 have been added at the input terminals. These diodes protect the circuit from large negative transients on input lines. If an input attempts to go more than about 1 V negative, the protective diode conducts like a short circuit to ground.

Here, $A = 0V$ and $B = +5V$. This makes Q_1 to conduct and Q_2 to switch off. Since Q_2 is like an open switch, no current flows through it. Instead, current flows through the $1.6\text{ k}\Omega$ resistor and into the base of Q_3 , turning it on. Q_4 remains off because there is no path through which it can receive base current. The equivalent switches in the totem pole under these conditions are shown in the Fig. 7.12 (a). The output current, I_L flows through R_4 (130Ω) and diode D_1 . Therefore, the HIGH output voltage is given as

$$V_{OH} = V_{CC} - V_{CE(sat)} - V_D - I_L \times (130\Omega)$$

where V_D is the forward drop across diode D_1 , about 0.7 V.

$V_{CE(sat)}$ is the saturation voltage of Q_3 , about 0.1 V.

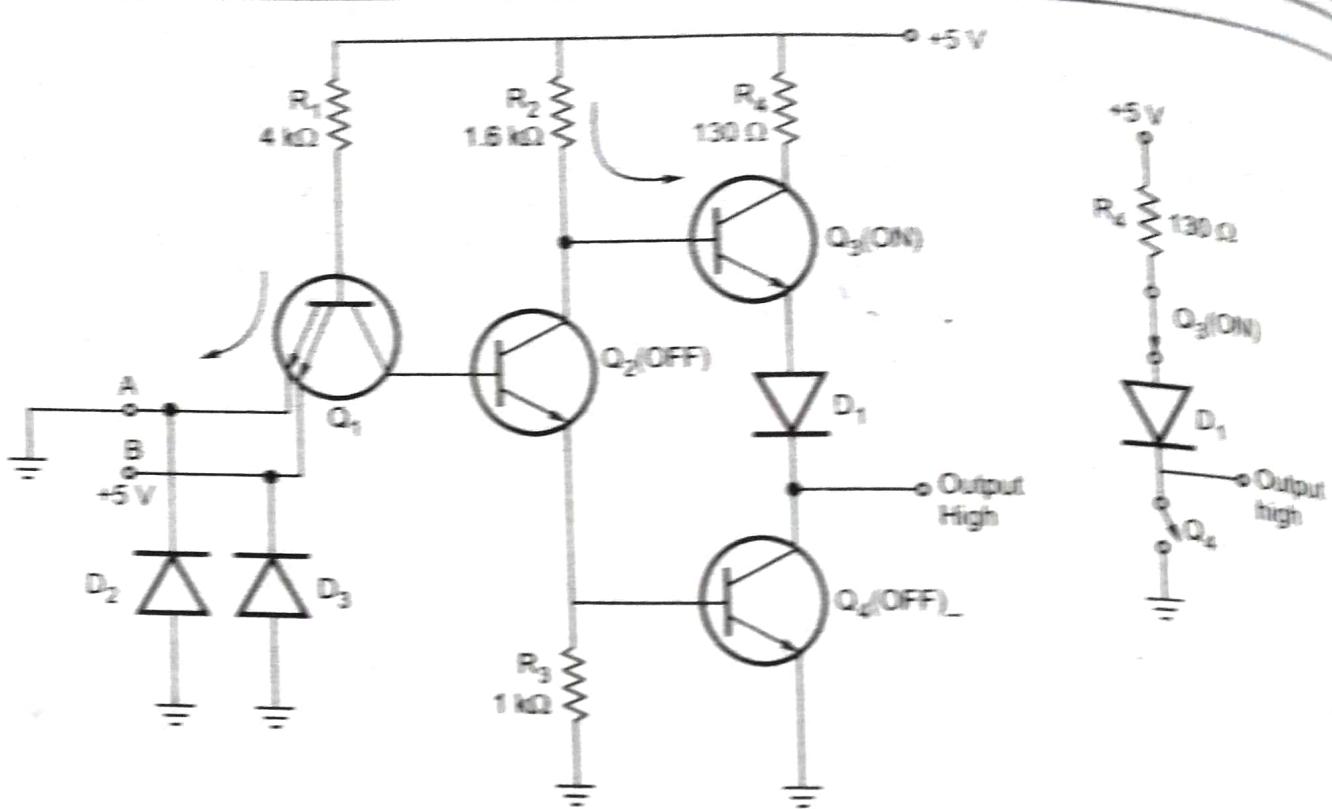
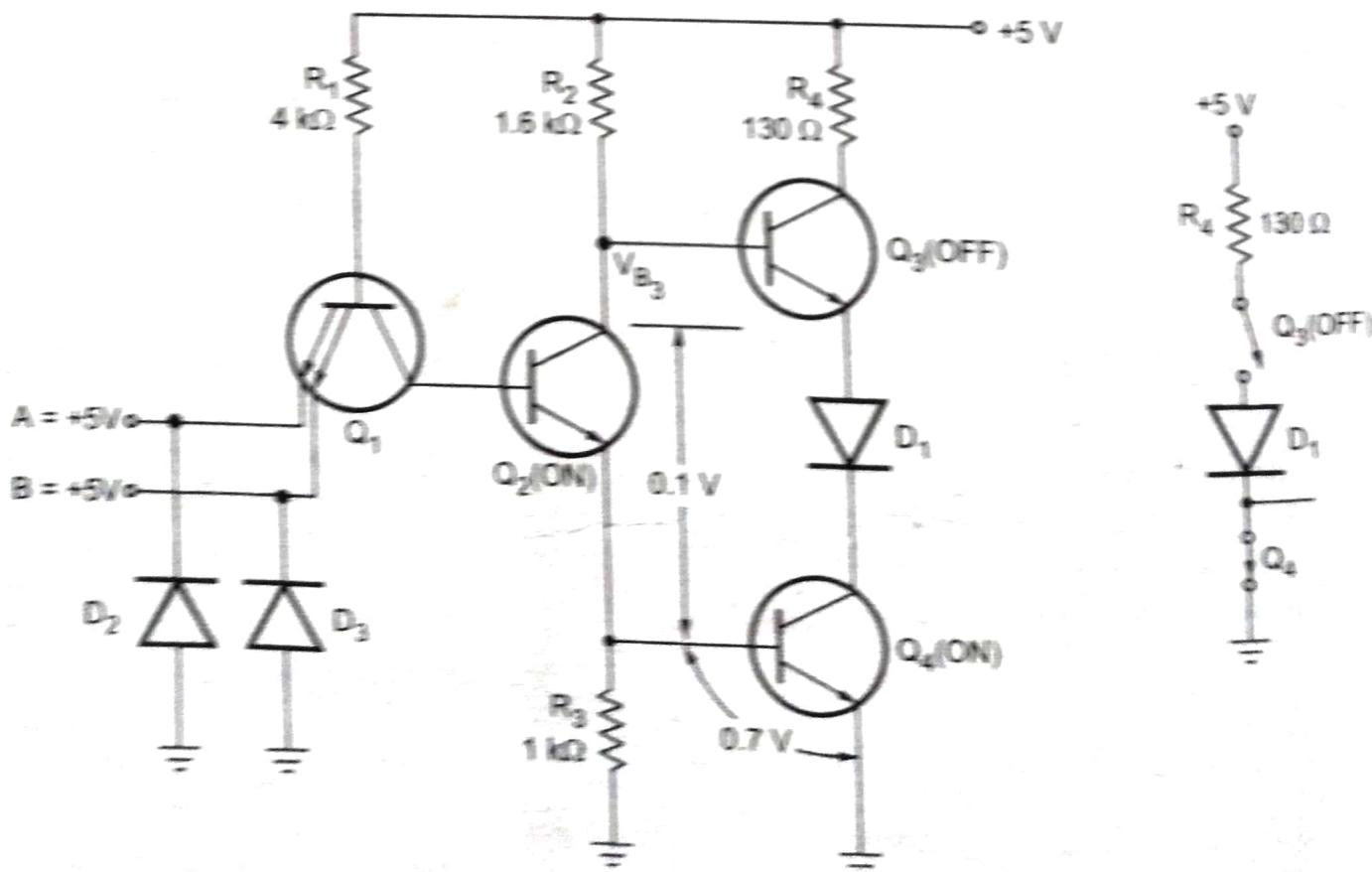


Fig. 7.12 (a) Static analysis when output is HIGH

We have seen that when both inputs are HIGH Q₂ is ON and it drives Q₄ turning it ON. Note that in this condition the voltage at the base of Q₃ equals the sum of the base-to-emitter drop of Q₄ and the V_{CE(on)} of Q₂.



$$\begin{aligned} V_{B_3} &= V_{BE}(Q_4) + V_{CE(sat)}(Q_2) \approx 0.7 \text{ V} + 0.1 \text{ V} \\ &= 0.8 \text{ V} \end{aligned}$$

Now we can easily understand the purpose of diode D_1 . It does not allow base-emitter junction of Q_3 to be forward-biased and thus ensures that Q_3 remains off when Q_4 is on.

Ex. 7.3 : A two input NAND gate has $V_{CC} = +5 \text{ V}$ and $1 \text{ k}\Omega$ load connected to its output. Calculate the output voltage

(a) when both input are LOW

(b) when both input are HIGH

Sol. : a) When both inputs of NAND gate are LOW, the output is HIGH and it is given as

$$\begin{aligned} V_{OH} &= V_{CC} - V_{CE(sat)} - V_D - I_L \times (130\Omega) \\ &= 5 - 0.1 - 0.7 - I_L (130\Omega) \\ &= 4.2 \text{ V} - I_L (130\Omega) \end{aligned} \quad \dots(1)$$

where the load current is

$$\begin{aligned} I_L &= \frac{V_{OH}}{R_L} \\ &= \frac{V_{OH}}{1\text{k}\Omega} \end{aligned}$$

Substituting for I_L in the equation 1 we get,

$$V_{OH} = 4.2 \text{ V} - \frac{V_{OH}}{1\text{k}\Omega} (130\Omega)$$

$$\therefore V_{OH} + \frac{130 V_{OH}}{1000} = 4.2$$

$$\therefore 1130 V_{OH} = 4200$$

$$\begin{aligned} V_{OH} &= \frac{4200}{1130} \\ &= 3.716 \text{ V} \end{aligned}$$

b) When both inputs of NAND gate are HIGH, the output is LOW and it is given as

$$V_{OL} = V_{CE(sat)} \approx 0.1 \text{ V}$$

7.6.3 Input and Output Currents- Fanout

We have seen that TTL output stage is a totem pole. It consists of two transistors Q_3 and Q_4 . When Q_3 is ON, the output is HIGH and it supplies current I_{IH} to drive the load. Hence Q_3 is called a pull-up transistor. When Q_4 is ON, the output is low and it draws current from the load to pull the load voltage down. Hence transistor Q_4 is called a pull-down transistor.

Since current flows out of the totem pole when the output is HIGH, Q_3 acts as a current source to a load. When the output is low, current flows into Q_4 , and we say that Q_4 is a current sink. Fig. 7.13 shows the output stage of the TTL driver connected to the input stage of the TTL load. In Fig. 7.13 (a) the driver output is low and Q_4 sinks current from the forward biased base-emitter junction of the input transistor of the load. This current is approximately 1.6 mA, and is designated I_{OL} at the output and I_{IL} at the input.

In Fig. 7.13 (b) the driver output is HIGH and Q_3 source current to the load. It is small leakage current supplied to the reverse biased emitter base junction of the input transistor of the load. It is approximately 40 μ A. This current is designated as I_{OH} at the output and I_{IH} at the input. By convention current flowing into a device is positive and current flowing out is negative. Therefore, manufacturers specify negative values for I_{OH} and I_{IL} .

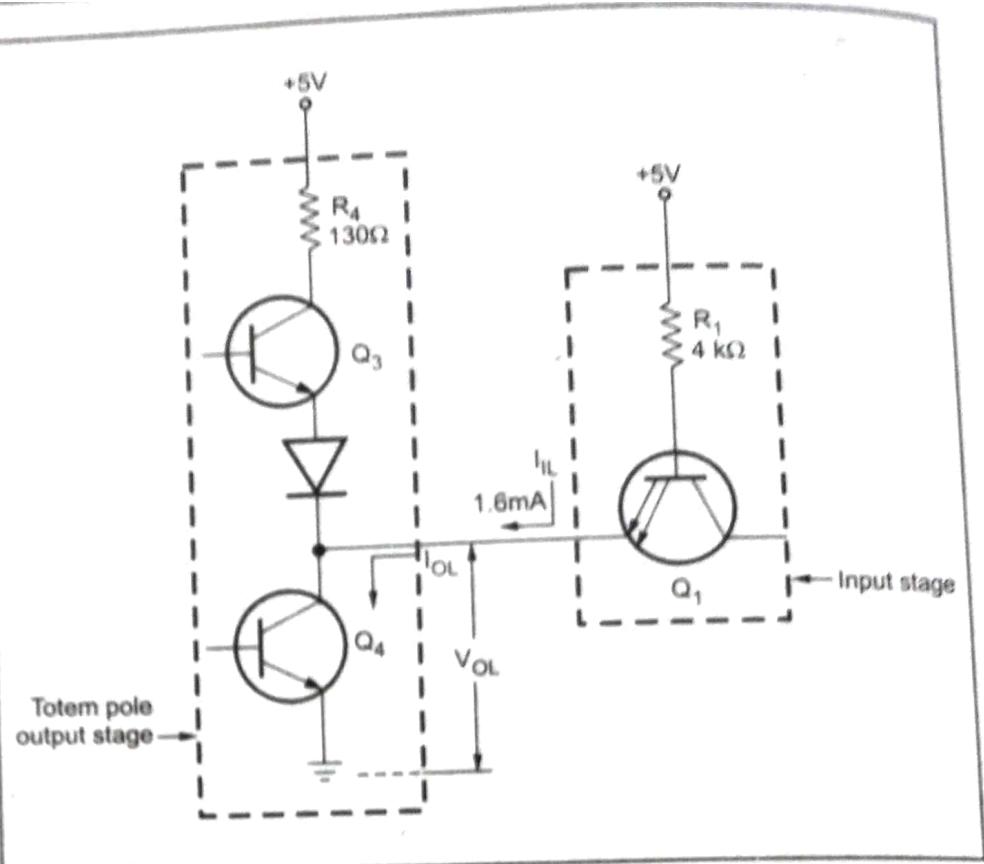


Fig. 7.13 (a) Q_4 acting as a current sink when output is LOW

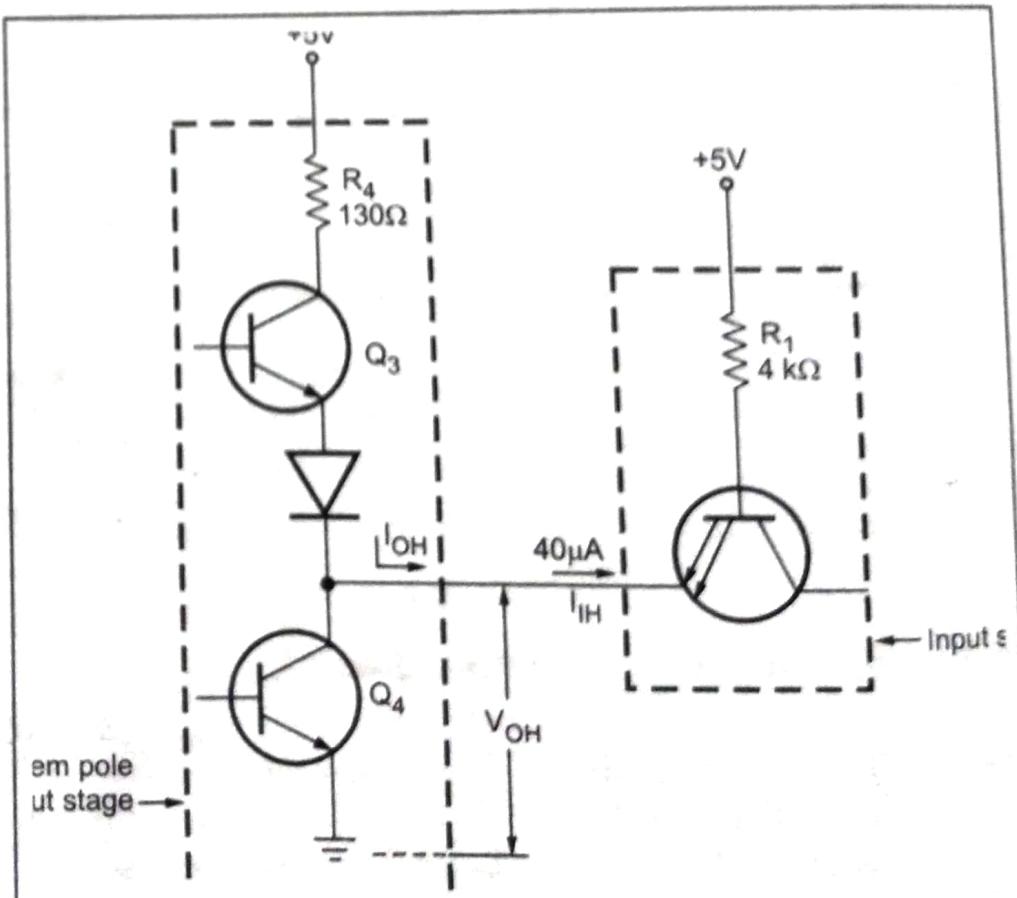


Fig. 7.13 (b) Q_3 acting as a current source when output is HIGH

Fig. 7.14 shows a TTL output connected to the several TTL loads. When the output is HIGH, it is necessary to supply load current (I_{IH}) to each TTL load, so Q_3 must be capable of sourcing the sum of these currents.

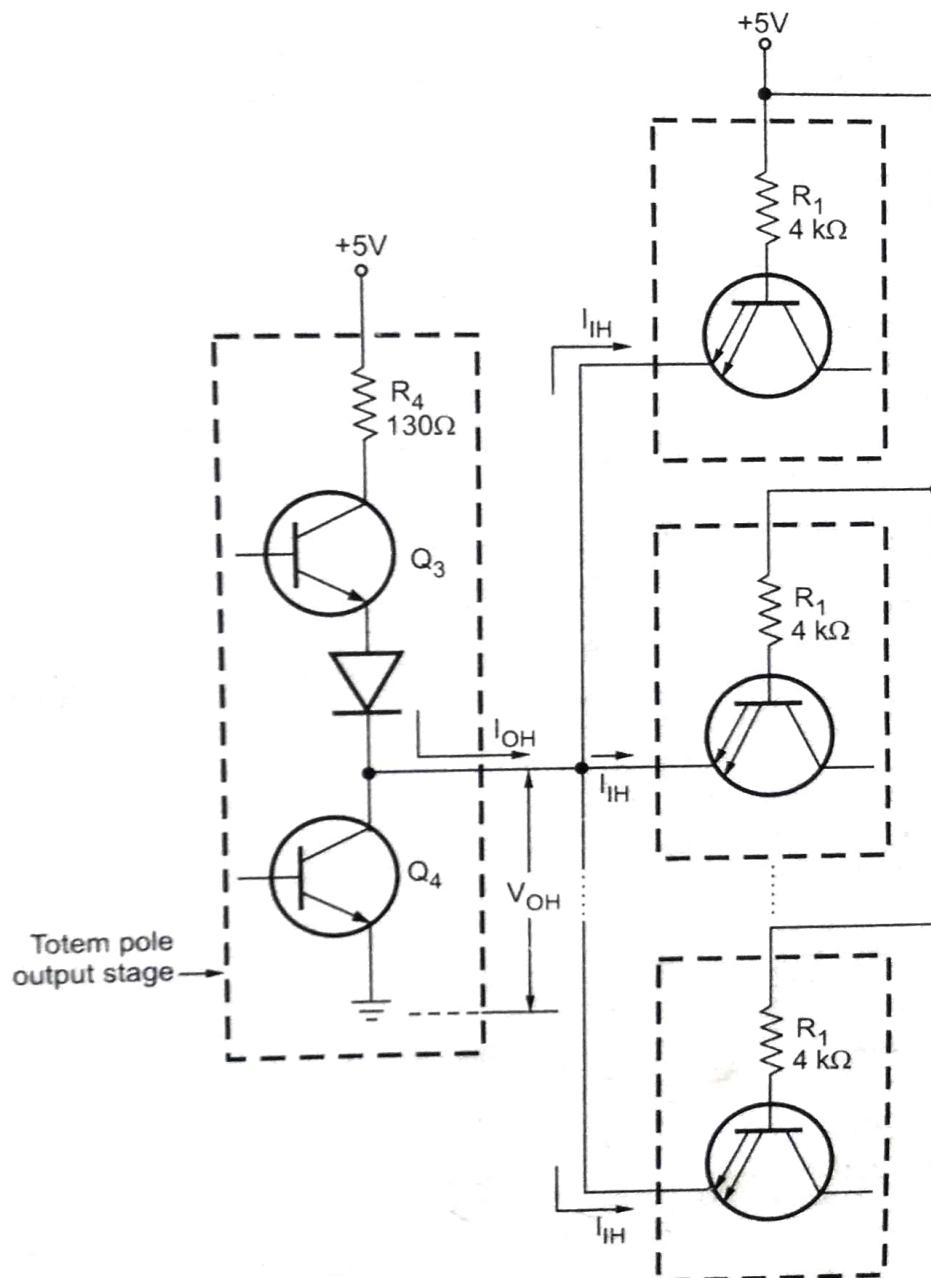


Fig. 7.14 (a) When output is HIGH

We know that, fanout is the maximum number of loads belonging to same family that a logic gate can drive,

so

$$\text{fanout} = \frac{|I_{OH(\max)}|}{I_{IH(\max)}}$$

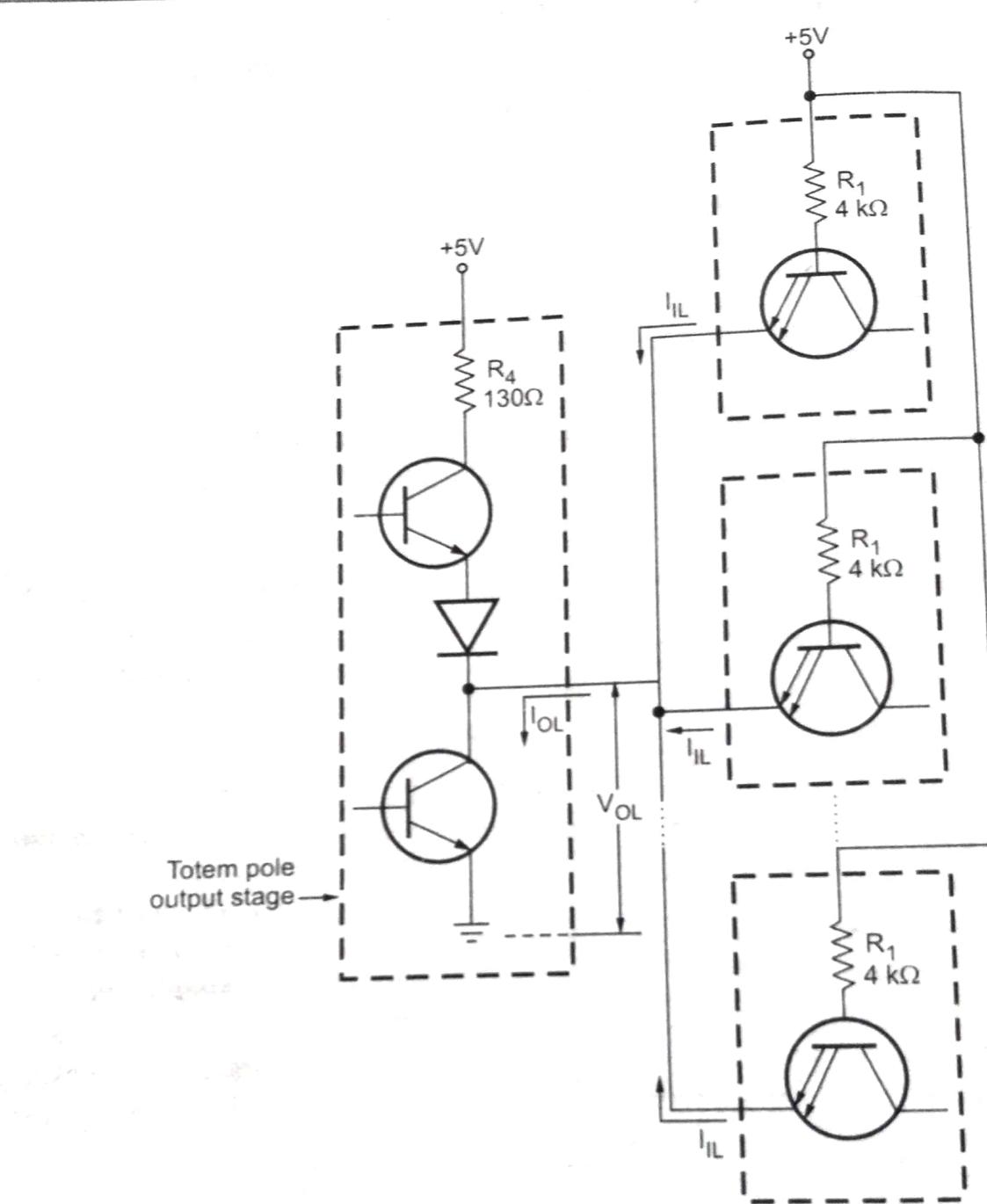


Fig. 7.14 (b) When output is LOW

For standard TTL, $I_{OH(\max)} = -400\text{ }\mu\text{A}$ and $I_{IH(\max)} = 40\text{ }\mu\text{A}$.

Therefore,

$$\text{fanout} = \frac{|-400\text{ }\mu\text{A}|}{40\text{ }\mu\text{A}}$$

$$= 10$$

Similarly, when the output is low, each load supplies current to the totem pole, so Q_4 must be capable of sinking the sum of these currents. In this case, fanout is defined as

$$\text{fanout} = \frac{|I_{OL(\max)}|}{|I_{IL(\max)}|}$$

For standard TTL,

$$I_{OL(\max)} = 16 \text{ mA} \text{ and } I_{IL(\max)} = -1.6 \text{ mA}$$

Therefore,

$$\text{fanout} = \frac{16 \text{ mA}}{|-1.6 \text{ mA}|} = 10$$

We have seen that fanout can be determined in two ways. Here, in both cases fanout is 10. But if they differ, the actual fanout is always the smaller of the two computations.

7.6.4 Standard TTL Characteristics

In 1964 Texas Instruments Corporation introduced the standard TTL ICs, 54/74 series. There are several series/ subfamilies in the TTL family of logic devices. We first examine the electrical characteristics of the standard 74 series. Later we introduce the other TTL series and compare their characteristics with those of the standard series.

Supply voltage and temperature range :

Both the 74 series and 54 series operate on supply voltage of 5V. The 74 series works reliably over the range 4.75 V to 5.25 V, while the 54 series can tolerate a supply variation of 4.5 to 5.5 V. The 74 series devices are guaranteed to work reliably over a temperature range of 0 to 70° C where as 54 series devices can handle temperature variations from - 55 to +125° C. From the above values we can say that 54 series devices have greater tolerance of voltage and temperature variations. Hence, these devices are used where it is necessary to maintain reliable operation over an extreme range of conditions. For example, in military and space application. The only disadvantage of these devices is that they are expensive.

Voltage Levels and Noise Margin :

Table 7.6 shows the input and output logic voltage levels for the standard 74 series. The minimum and maximum values shown in the Table 7.6 are for worst case conditions of power supply, temperature and loading conditions.

Voltages	Minimum	Typical	Maximum
V_{OL}	-	0.2	0.4
V_{OH}	2.4	3.4	-
V_{IL}	-	-	0.8
V_{IH}	2.0	-	-

Table 7.6 Voltage levels

Looking at the Table 7.6 we can say that, in the worst case, there is difference of 0.4 V between the driver output voltages and the required load input voltages. For instance, the worst-case low values are

$$V_{OL(\max)} = 0.4 \text{ V driver output}$$

$$V_{IL(\max)} = 0.8 \text{ V load input}$$

Similarly, the worst-case high values are

$$V_{OH(\min)} = 2.4 \text{ V driver output}$$

$$V_{IH(\min)} = 2 \text{ V load input}$$

In either case, the difference is 0.4 V. This difference is called *noise margin*. For TTL, Low state noise margin, V_{NL} and high state noise margin, V_{NH} both are equal and 0.4 V. This is illustrated in Fig. 7.15. It provides built-in protection against noise. It ensures reliable operation of the device for induced noise voltages less than 0.4 V.

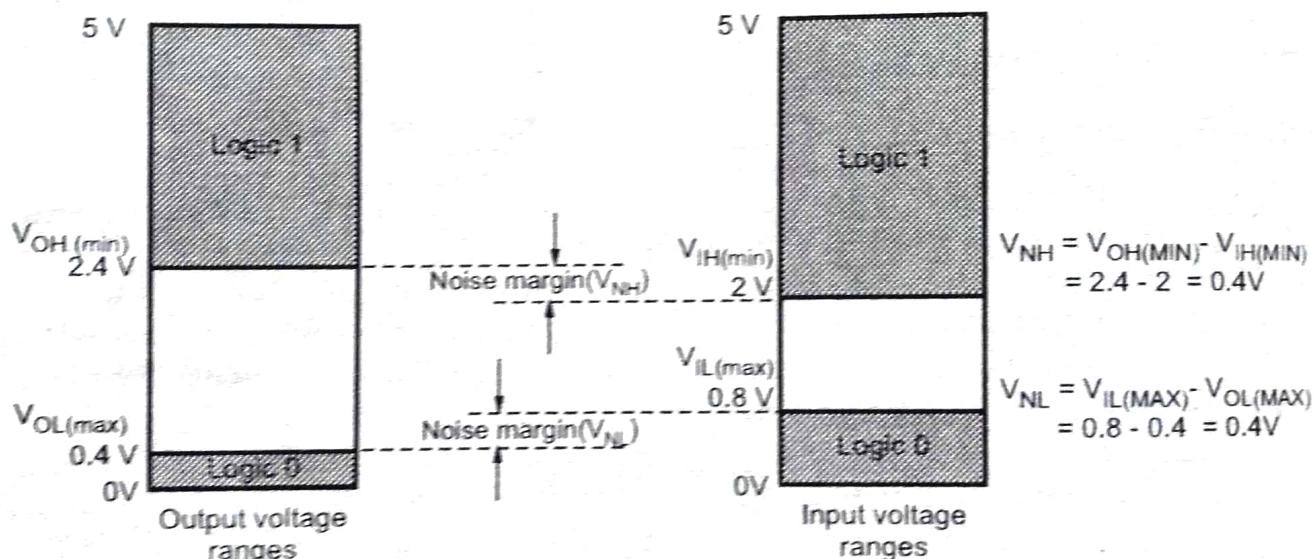


Fig. 7.15 TTL logic levels and noise margin

Power Dissipation and Propagation Delay

A standard TTL gate has an average power dissipation of about 10 mW. It may vary from this value because of signal levels, tolerances, etc. We know that, the propagation delay time is the time it takes for the output of a gate to change after the inputs have changed. The propagation delay time of a TTL gate is approximately 10 nanoseconds.

Fan-Out

A standard TTL output can typically drive 10 standard TTL inputs. Therefore, standard TTL has fanout 10.

Table 7.7 summarizes the characteristics of standard TTL.

Characteristics	Values
Supply voltage	For 74 series - (4.75 to 5.25) volts For 54 series - (4.5 to 5.5) volts
Temperature range	For 74 series - (0°C to 70°C) For 54 series - (-55° to 125° C)
Voltage levels	$V_{OL(max)} = 0.4 \text{ V}$ $V_{OH(max)} = 2.4 \text{ V}$ $V_{L(max)} = 0.8 \text{ V}$ $V_{H(min)} = 2.0 \text{ V}$
Noise margin	0.4 V
Power dissipation	10 mW per gate
Propagation delay	Typically 10 ns
Fanout	10

Table 7.7 Standard TTL characteristics

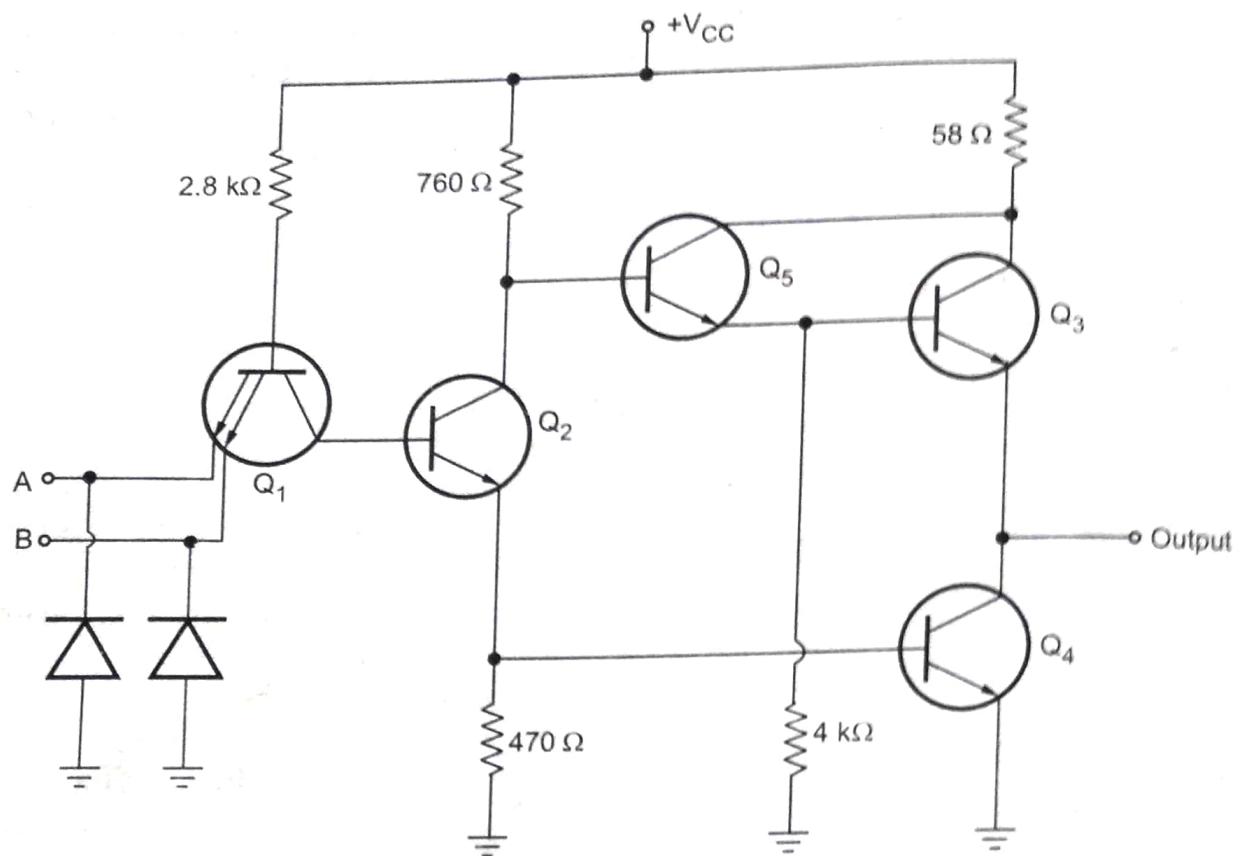
7.6.5 Improved TTL Series

The standard TTL series of ICs offer a wide variety of devices. But these devices are rarely used in new system designs because over the years newer TTL series with improved performance have been developed. These other TTL series-often called 'TTL-subfamilies'- provide wide range of speed and power capabilities. In the following sections we are going to study characteristics of TTL-subfamilies.

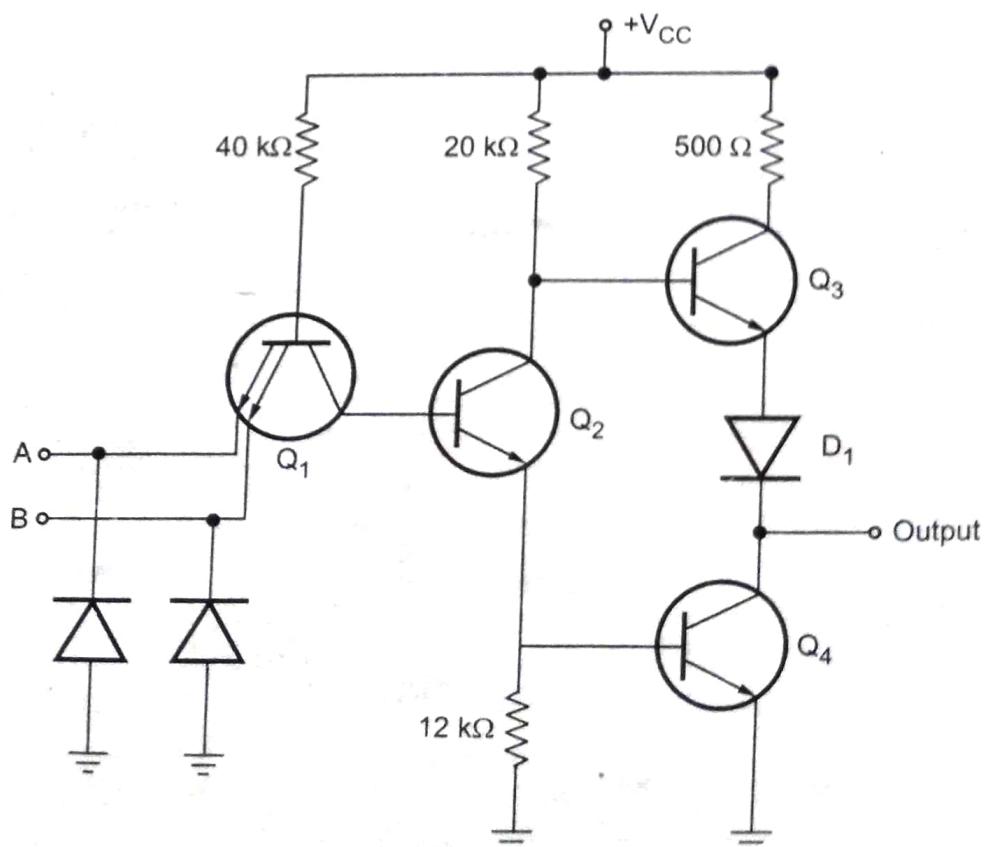
7.6.6 High-Speed (H) and Low-Power (L) TTL

The 74L and 74H series were developed to provide low-power and high-speed version of TTL, respectively. Both have the same basic circuit as the standard 74 series, but differences in circuit component values and one or more additional component give these two series their different characteristics.

Fig. 7.16 (a) shows 2-input high speed TTL NAND gate. Besides smaller resistance values, the only difference between this gate and the standard version is the additional transistor Q_5 . This transistor acts as a driver for Q_3 . Actually Q_3 and Q_5 form a darlington pair, which has much more current gain. This results in higher switching speed of the output from low to high. The switching time is also reduced due to low resistance values. However, due to reduced resistance values power consumption is more. It is important to note that the base-emitter junctions of Q_3 and Q_5 raise the threshold level at the base of Q_5 to 1.4 V and therefore, the darlington connection eliminates the need for a diode in the totem pole.



(a) 2-input high speed NAND gate



(b) 2-input low power NAND gate

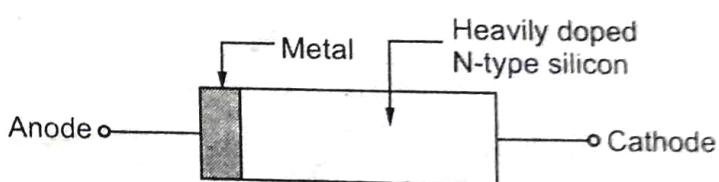
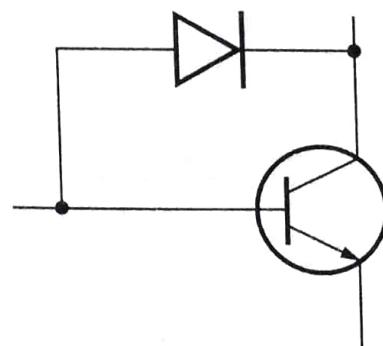
Fig. 7.16 74H00 and 74L00 NAND gates

Fig. 7.16 (b) shows 2-input low power TTL NAND gate. The only difference between this gate and the standard version is the much larger resistance values, which reduce power consumption at the expense of switching speed. The low-power series consumes less power of the order of 1 mW with longer propagation delay around 33 ns. On the other hand high-speed series has a reduced propagation delay of about 6 ns at the cost of higher power consumption around 32 mW.

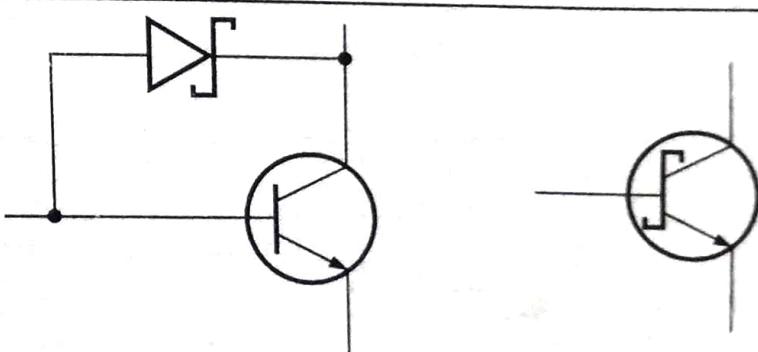
7.6.7 The Schottky Clamp

With standard TTL, high-speed TTL, and low-power TTL, when transistors are ON, they are driven into hard saturation. This causes a surplus of carriers to be stored in the base. This excess charge carriers in the base region must be removed before the transistors is switched from ON to OFF. The time required to remove these carriers, called storage time, is responsible for high propagation delays or low switching times. One way to counter this problem is to prevent the transistor from going into deep saturation when it is turned ON i.e. to restrict the forward bias of its base-to-collector junction to few tenths of a volt. This can be accomplished by connecting a diode across the base-to-collector junction, as shown in the Fig. 7.17 (a). The diode does not allow to increase the forward bias voltage at base-to-collector junction above its cut-in voltage. In other words, it clamps base-to-collector voltage upto its small cut-in voltage. As a result the junction cannot be heavily forward biased and the transistor is kept out of deep saturation.

We know that germanium diodes have less cut-in voltage but they cannot be fabricated in silicon integrated circuits. The Schottky diode, consisting of a silicon-metal junction with a cut-in voltage of 0.3 to 0.4 volts is ideal for this purpose. Fig. 7.17 (b) and (c)



(a) Transistor with clamping diode (b) Schottky diode construction



(c) Schottky diode symbol (d) Schottky clamped transistor (e) Symbol for Schottky clamped transistor

Fig. 7.17

show the construction, and Fig. 7.17 (d) and (e) show schottky clamped NPN transistor and its symbol.

Another important parameter of Schottky diode is that it has very little capacitance and fast recovery time. So it can be switched rapidly without storage time delays.

7.6.8 Schottky (s) and Low-Power Schottky (LS) TTL

Fig. 7.18(a) shows 2-input Schottky NAND gate. Looking at the Fig. 7.18(a), we can notice that it uses smaller resistor values to help improve switching times. This increases the device average power dissipation to about 20 mW, about the same as for 74H series. Note that all the transistors used are Schottky clamped transistors, except Q_3 , which does not saturate. This series also use a darlington pair (Q_1 and Q_5) to provide shorter output rise time when switching from OFF to ON. One more transistor (Q_6) is used in this series. This regulates the current flow into the base of Q_4 and helps in turning Q_4 off rapidly.

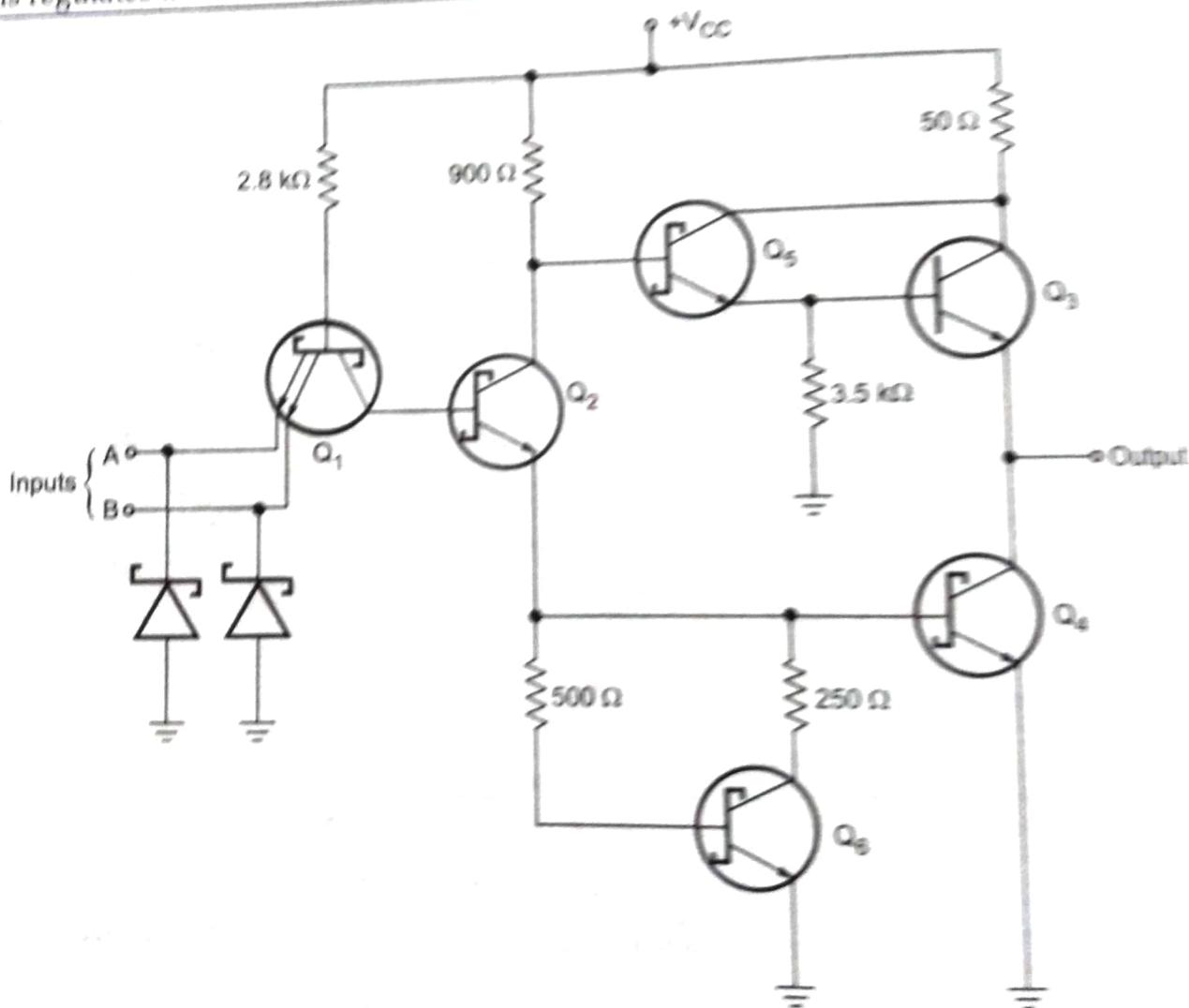


Fig. 7.18 (a) 2-input Schottky NAND gate

The 74LS series is a lower-powered, slower speed version of the 74S series. It uses the Schottky clamped transistors, but with larger resistor values than the 74S series. The larger resistor values reduce the circuit power requirement, but at the expense of an increase in

switching times. Fig. 7.18(b) shows 2-input low power Schottky NAND gate. Here, multi-emitter transistor is replaced by 2 diodes D₁ and D₂. Transistors Q₁, Q₂, and 20 kΩ resistor forms a two input AND gate, as discussed in section 7.3.2. Transistors Q₃, Q₄ and 4 kΩ resistor, so the output at the collector represents NAND function. The remaining circuitry, including the totem-pole output, is similar to that of 74S series, except for large resistance values, as mentioned earlier. The additional components, diodes D₁, D₂, and 4 kΩ resistor connected at the output helps in charging and discharging load capacitance when Q₁ and Q₂ are changing states.

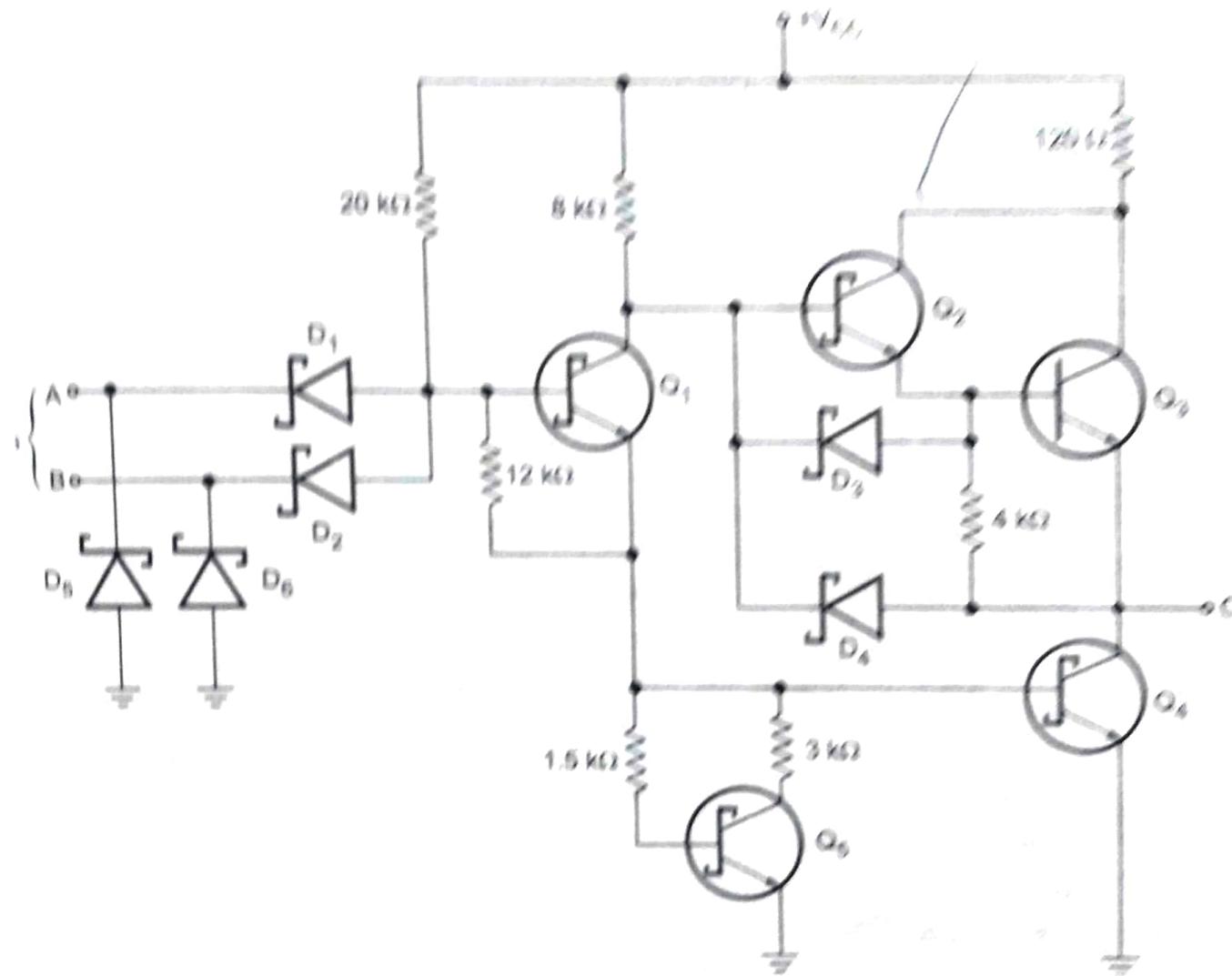


Fig. 7.18(b) 2-input low power schottky NAND gate

7.6.9 Advanced Schottky (AS) and Advanced Low-Power (ALS) Schottky TTL

74AS and 74ALS are recent enhancements in Schottky TTL circuitry. The 74AS series provides a considerable improvement in speed over the 74S series at a much lower power requirement. This is achieved by improvement in the doping and isolation techniques. These advanced Schottky devices are fabricated with ion implantation doping technique instead of diffusion and Schottky clamped transistors are isolated using oxide instead of P-material. These enhancements reduce capacitance and thus improve switching times.

These devices have few additional active components which further improve switching speeds, reduce power consumption, and increase fanout. The 74ALS series offers an improvement over the 74LS series in both speed and power dissipation. The 74ALS series has the lowest speed-power product of all the TTL series.

7.6.10 Fast (F) TTL

This is the latest TTL series. It uses a new integrated-circuit fabrication technique to reduce inter-device capacitances. This results low propagation delays. A typical fast TTL NAND gate has an average propagation delay of 3 ns and a power consumption of 6 mW.

7.6.11 Comparison of TTL Series Characteristics

Table 7.8 shows the typical values of characteristics of all the TTL series. All of the performance ratings, except for maximum clock rate, are for a NAND gate in each series.

Parameter	74	74S	74LS	74AS	74ALS	74F
Propagation delay (ns)	9	3	9.5	1.7	4	3
Power dissipation (mW)	10	20	2	8	1.2	6
Speed-power product (pJ)	90	60	19	13.6	4.8	18
Max. clock rate (MHz)	35	125	45	200	70	100
Fan-out	10	10 (Low level leads) 20 (high level leads)	20	40	20	33
Voltage parameters:						
$V_{OH(min)}(V)$	2.4	2.7	2.7	2.5	2.5	2.5
$V_{OL(max)}(V)$	0.4	0.4	0.5	0.5	0.4	0.5
$V_{IH(min)}(V)$	2.0	2.0	2.0	2.0	2.0	2.0
$V_{IL(max)}(V)$	0.8	0.8	0.8	0.8	0.8	0.8

Table 7.8

7.6.12 Open Collector Outputs

Until now we have seen totem pole output. One problem with totem pole output is that two outputs cannot be tied together. See the Fig. 7.19, where the totem pole outputs of two separate gates are connected together at point X. Suppose that the output of gate A is high (Q_{3A} ON and Q_{4A} OFF) and the output of gate B is low (Q_{3B} OFF and Q_{4B} ON). In this situation transistor Q_{4B} acts as a load for Q_{3A} . Since Q_{4B} is a low resistance load, it draws high current around 55 mA. This current might not damage Q_{3A} or Q_{4B} immediately, but over a period of time can cause overheating and deterioration in performance and eventual device failure.

Some TTL devices provide another type of output called open collector output. The outputs of two different gates with open collector output can be tied together. Fig. 7.20 shows a 2-input NAND gate with an open-collector output eliminates the pull-up transistor Q_3 , D_1 and R_4 . The output is taken from the open collector terminal of transistor Q_4 .

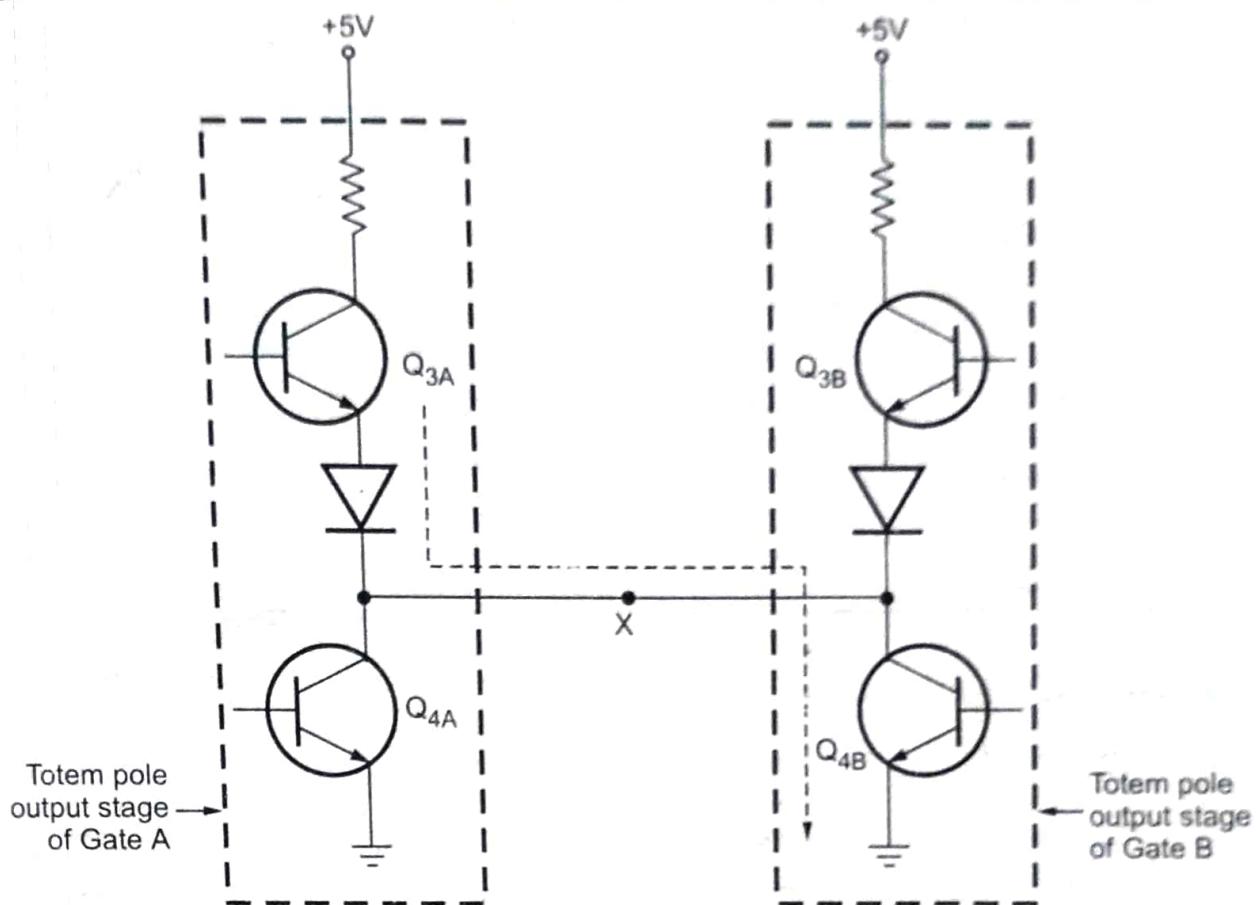


Fig. 7.19 Totem-pole outputs tied together can produce harmful current through Q_{3A} and Q_{4B}

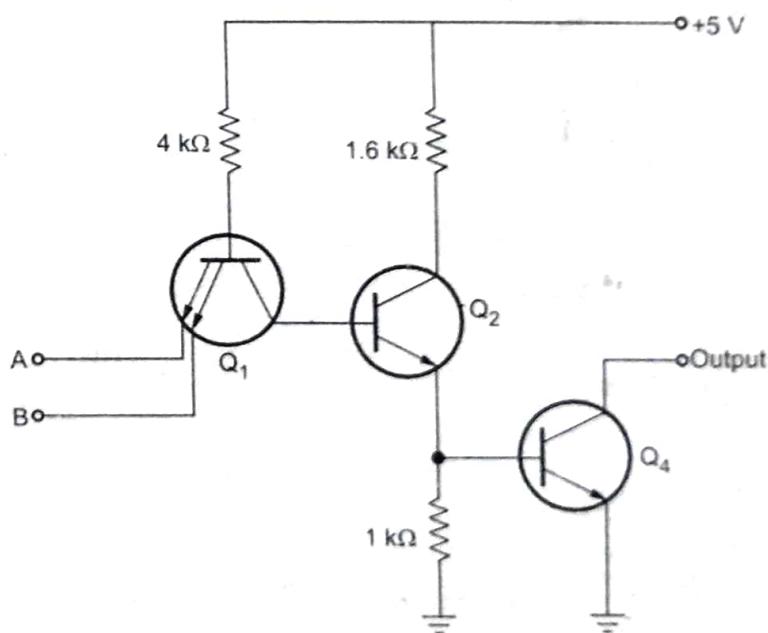


Fig. 7.20 Open collector 2-input TTL NAND gate

Because the collector of Q₄ is open, a gate like this will not work properly until you connect an external pull-up resistor, as shown in Fig. 7.21. When Q₄ is ON, output is low and when Q₄ is OFF output is tied to V_{CC} through an external pull up resistor.

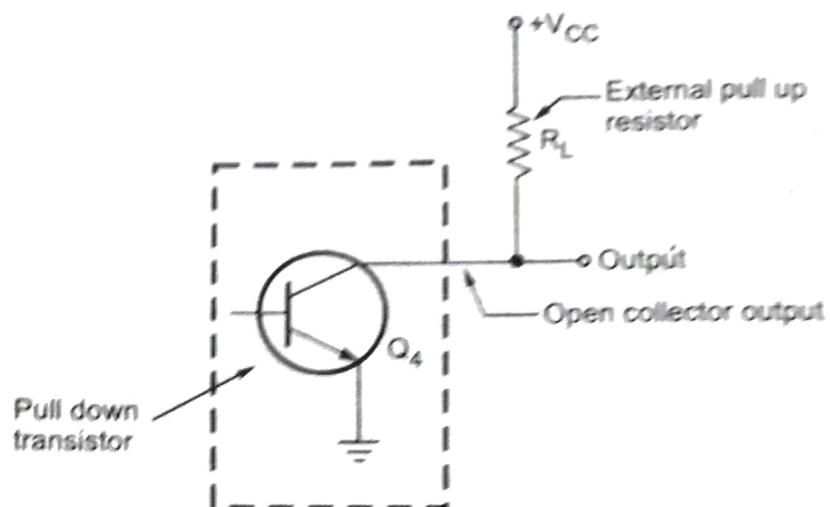


Fig. 7.21 Open collector output with pull-up resistor

7.6.13 Wired AND Connection

As mentioned earlier, the open collector outputs of two or more gates can be connected together, as shown in the Fig. 7.22 (a). The connection is called a wired AND and represented schematically by the special AND-gate symbol as shown in Fig. 7.22 (b).

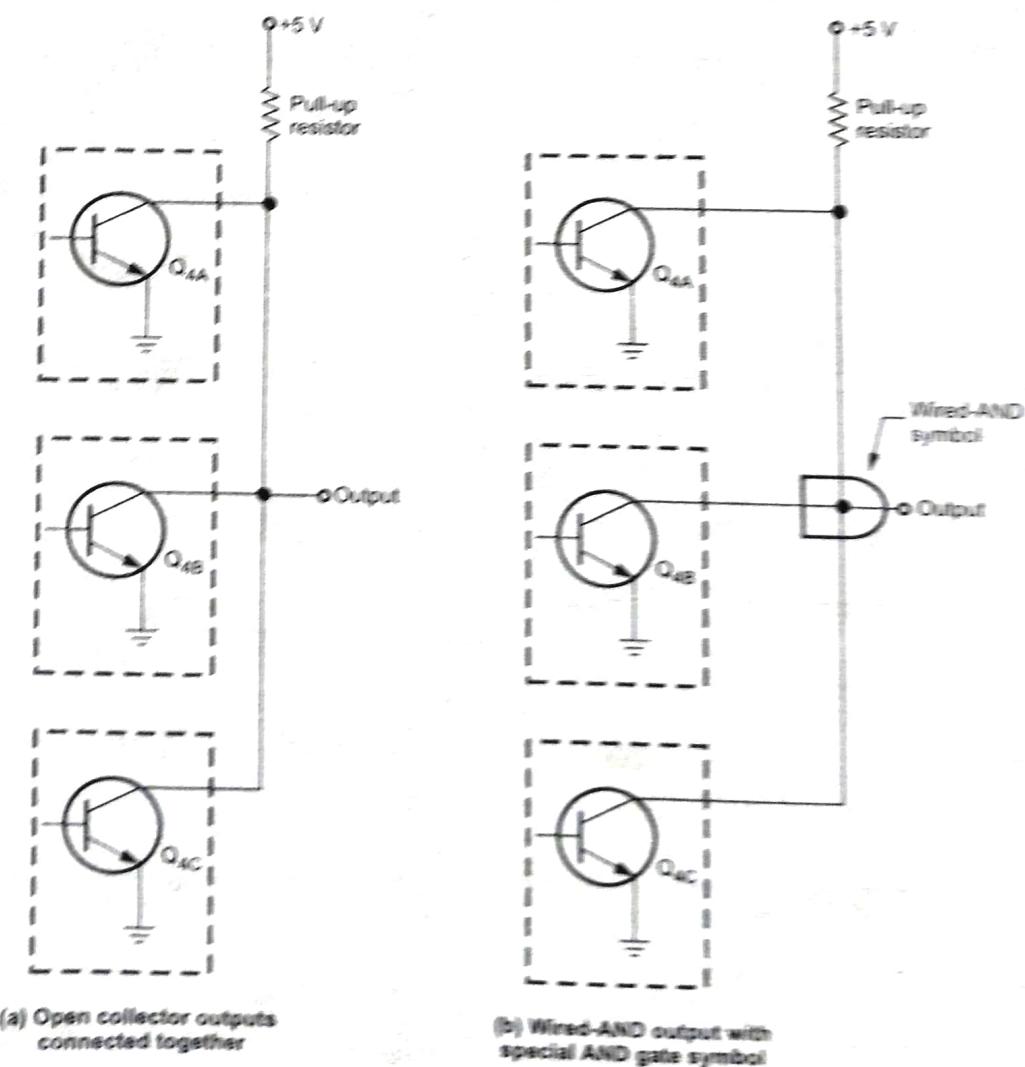


Fig. 7.22

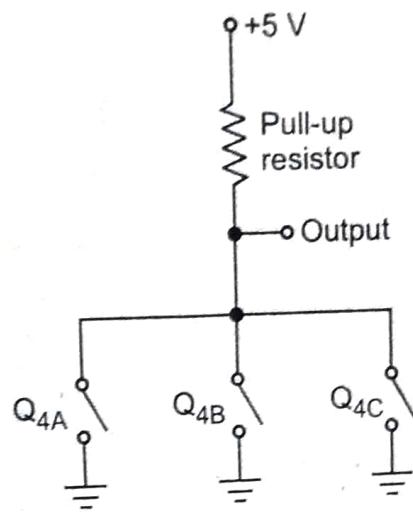
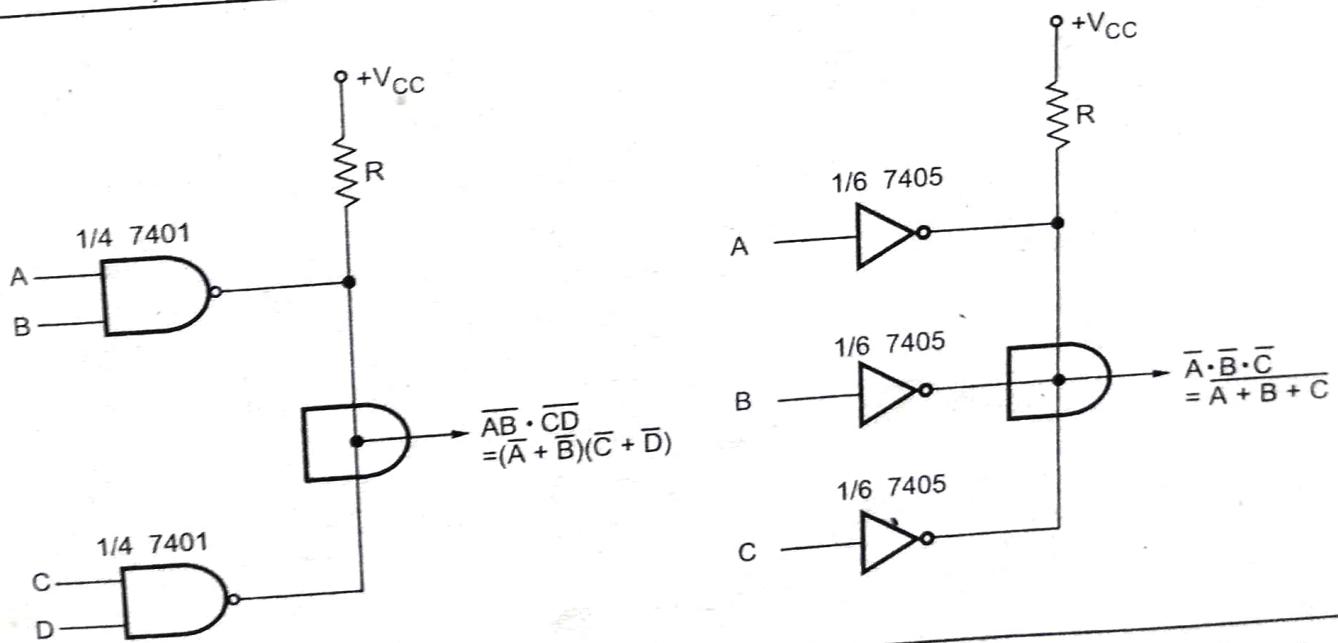


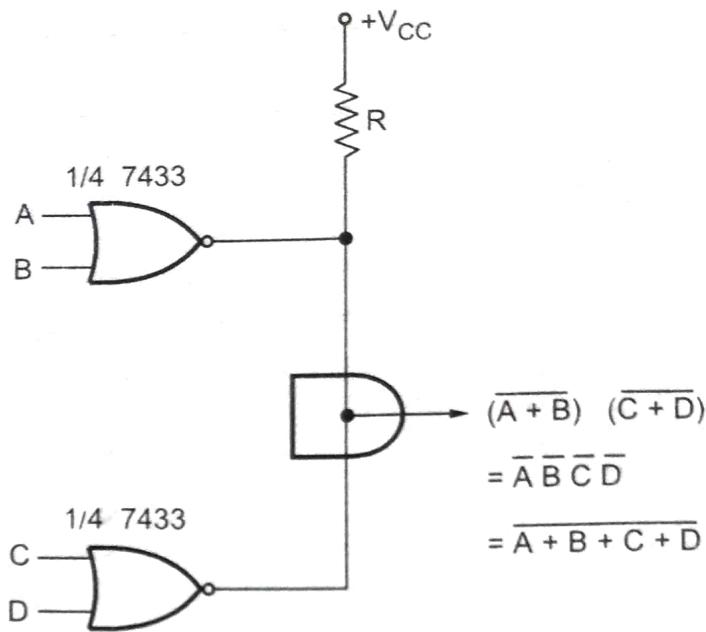
Fig. 7.22 (c) Electrical equivalent circuit for Fig. 7.22 (a) and (b)

Fig. 7.22 (c) shows the electrical equivalent circuit for Fig. 7.22 (a) and (b). It shows that the output is high only when all switches are open- i.e. only when output of each stage is HIGH . Thus, the output is the logical AND operation of the logic function performed by the gates. Fig. 7.23 shows wire ANDing of inverter, NAND and NOR gates.

The big disadvantage of open-collector gates is their slow switching speed. This is because the value of pull-up resistor is in kΩ, which results in a relatively long constants.



(a) Wire-ANDED output of NAND gates Fig. 7.23 (b) Wire-ANDED output of inverters



(c) Wire-ANDED output of NOR gates

Fig. 7.23 The wired-AND connections

7.6.14 Comparison Between TOTEM Pole and Open Collector Output

Table 7.9 summarizes the difference between totem pole and open collector outputs.

Totem Pole	Open Collector
1. Output stage consists of pullup transistor (Q_3), diode resistor and pull down transistor (Q_4)	1. Output stage consists of only pull down transistor
2. External pull-up resistor is not required	2. External pull-up resistor is required for proper operation of gate
3. Output of two gates cannot be tied together	3. Output of two gates can be tied together using wired AND technique
4. Operating speed is high	4. Operating speed is low

Table 7.9 Comparison of totem pole and open collector output

7.6.15 Tri-State Logic, Buffers and Bus Drivers

The tristate configuration is a third type of TTL output configuration. It utilizes the high-speed operation of the totem-pole arrangement while permitting outputs to be wired-ANDED (connected together). It is called tristate TTL because it allows three possible output stages : HIGH, LOW and high-impedance. We know that transistor Q_3 is ON when output is HIGH and Q_4 is ON when output is LOW. In the high impedance state both transistors, transistors Q_3 and Q_4 in the totem pole arrangement are turned OFF. As a result, the output is open or floating, it is neither LOW nor HIGH.

Fig. 7.24 shows the simplified circuit for tristate inverter. It has two inputs A and E.

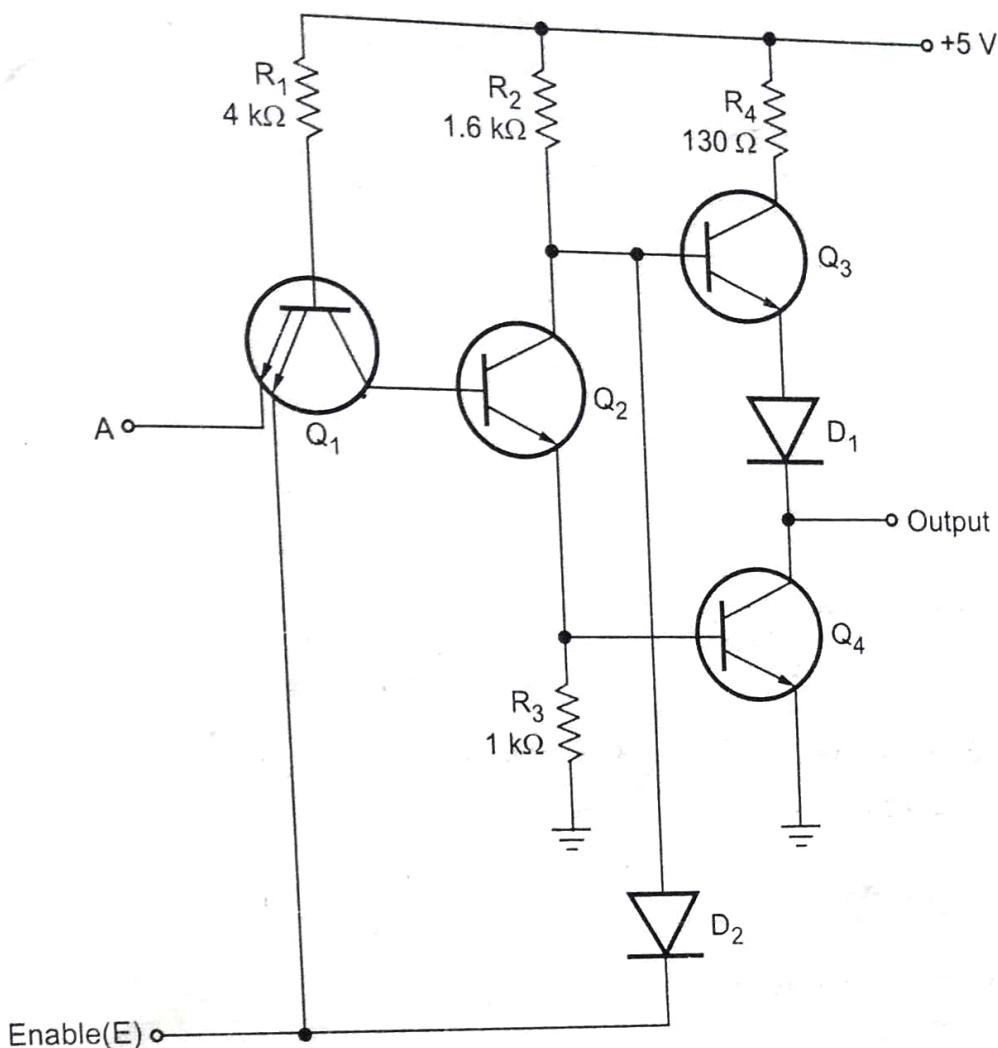
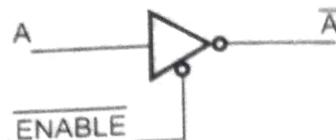
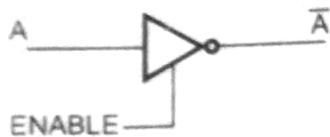


Fig. 7.24 Tristate TTL inverter

A is the normal logic input whereas E is an ENABLE input. When ENABLE input is HIGH, the circuit works as a normal inverter. Because when E is HIGH, the state of the transistor Q₁ (either ON or OFF) depends on the logic input A, and the additional component diode is open circuited as its cathode is at logic HIGH. When ENABLE input is LOW, regardless of the state of logic input A, the base-emitter junction of Q₁ is forward biased and as a result it turns ON. This shunts the current through R₁ away from Q₂ making it OFF. As Q₂ is OFF, there is no sufficient drive for Q₄ to conduct and hence Q₄ turns off. The LOW at ENABLE input also forward-biases diode D₂, which shunt the current away from the base of Q₃, making it OFF. In this way, when ENABLE input is LOW, both transistors are OFF and output is at high impedance state. Fig. 7.25 shows the logic symbols for tristate inverter. In above case circuit operation is enabled when ENABLE input is HIGH. Therefore, ENABLE input is active high. The logic symbol for active high enable input is shown in Fig. 7.25 (a). In some circuits ENABLE input can be active low, i.e. circuit operates when ENABLE input is LOW. The logic symbol for active low ENABLE input is shown in the Fig. 7.25 (b).



(a) Logic symbol for active enable input (b) Logic symbol for active low enable input
Fig. 7.25

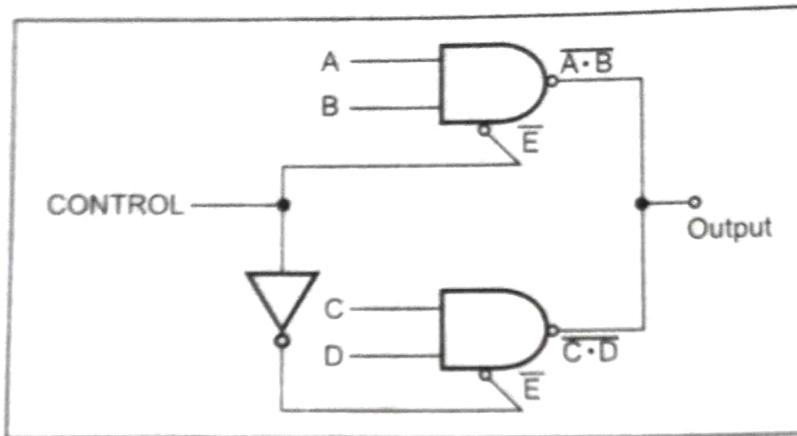


Fig. 7.26 Tristate outputs connected together

same concept is used when two or more device shares a common bus (A bus is a set of conducting paths). This is illustrated in Fig. 7.26.

As shown in the Fig. 7.27 there are two output devices which can give data to the one input device. These three devices are connected together with a common data bus. The common data bus is shared by the two output devices. When CONTROL signal is LOW

As mentioned earlier, tristate outputs can be connected together. This is illustrated in Fig. 7.26. When CONTROL input is LOW, upper NAND gate is enabled and its output ($A \cdot B$) is available on the output terminal. The output of lower NAND gate is in the tristate. When CONTROL input is high, the output of upper gate is in the tristate while output of lower NAND gate ($C \cdot D$) is available on the output terminal. The

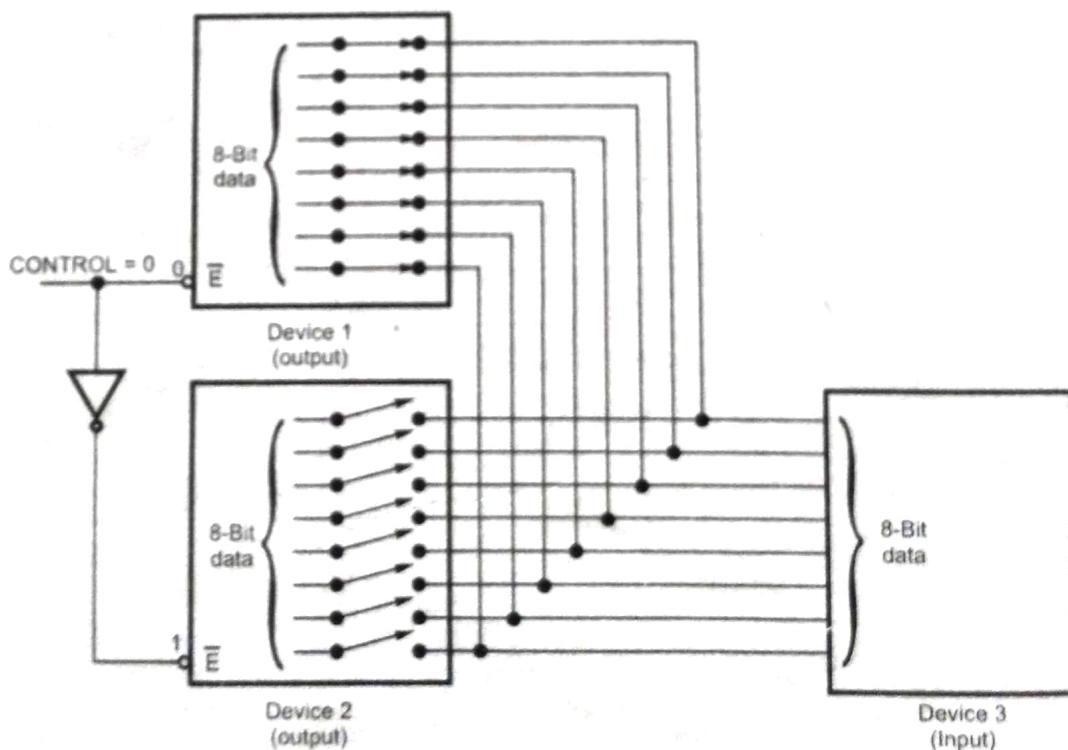


Fig. 7.27 (a)

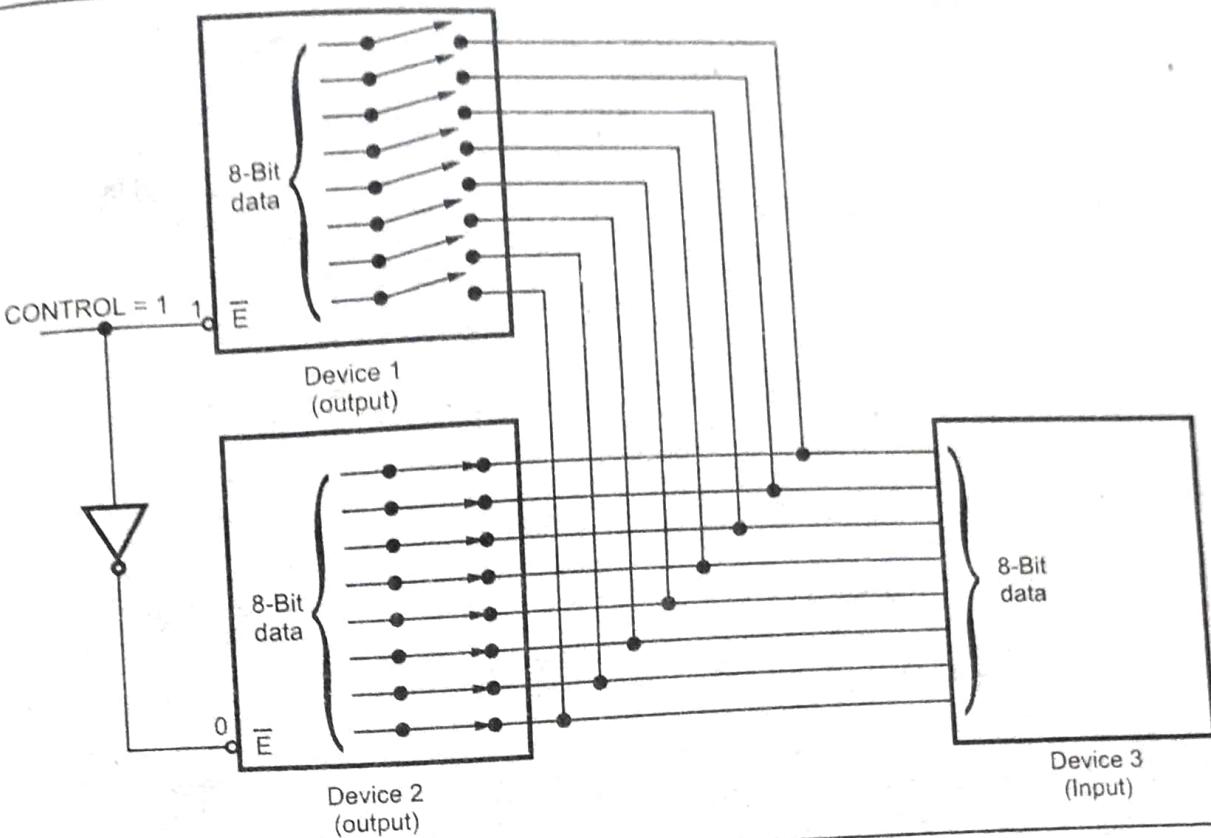


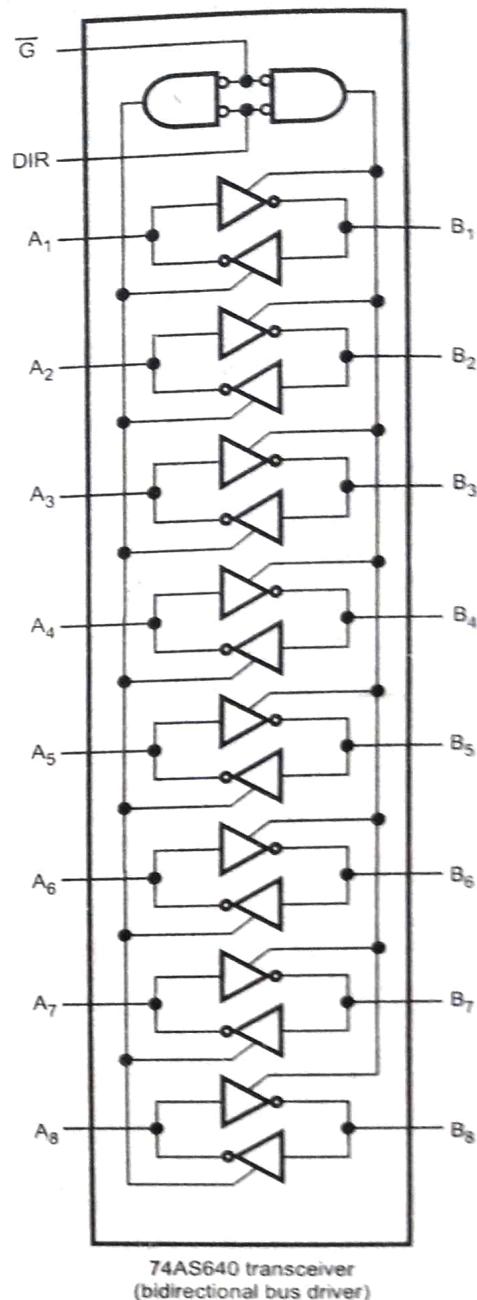
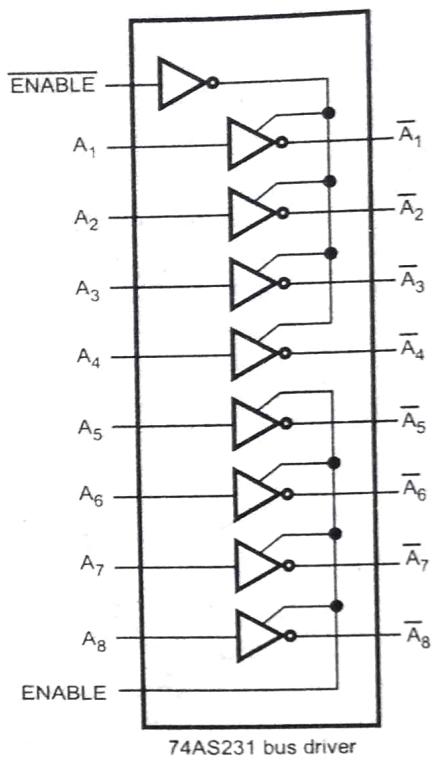
Fig. 7.27 (b)

device 1 is enabled and device 2 is disabled. As a result the data (8-bit) from device 1 is available on the data bus, as shown in the Fig. 7.27 (a). When CONTROL signal is HIGH device 1 is disabled and device 2 is enabled. In this case the data from the device 2 is available on the data bus as shown in the Fig. 7.27 (b).

As said earlier bus is a common connection between number of devices. When devices are more, required current sourcing and sinking capabilities may exceed than those provided by standard TTL. For such requirements buffer ICs are used. They can source and sink more current than a standard TTL. The buffer ICs used for increasing sinking and sourcing capabilities of bus are called bus drivers.)

Any logic circuit that is called a buffer, or a driver is designed to have a greater output current and /or voltage capability than an ordinary logic circuit. Buffer/driver ICs are available with totem-pole outputs and with open-collector outputs.

A typical TTL bus driver contains eight inverters, or eight noninverting drivers, all with tristate outputs and enable signal. Many have more than one enable input and/or built-in gates that can be used to perform logic operations on the enable inputs (s). Many versions have separate enable inputs that can be of four drivers each, as shown in the Fig. 7.28 (a). Bus transceivers are two-directional bus drivers : They can be used to pass data in one direction while the other direction is in high impedance state and vice-versa. They are also known as bidirectional bus drivers. Fig. 7.28 (b) shows the logic diagram for bidirectional bus driver.



(a) (b)
Fig. 7.28 A typical tristate bus driver and transceiver

7.7 MOSFET Logic

Digital circuits with MOSFETs can be grouped into three categories :

- PMOS - uses only P-channel enhancement MOSFETs,
- NMOS - uses only N-channel enhancement MOSFETs, and
- CMOS (complementary MOS) - uses both P- and N-channel devices.

PMOS and NMOS digital ICs are economical than CMOS ICs because they have greater packing density than CMOS. NMOS has twice the packaging density than PMOS. Further more, NMOS can operate at about three times faster than their PMOS

counterparts. This is because NMOS has faster moving current carriers (electrons) whereas PMOS has slower moving current carriers (holes). CMOS has the greatest complexity and lowest packaging density; however, it has important advantages of high speed and much lower power dissipation. NMOS and CMOS are widely used in the digital ICs, but PMOS ICs are no longer part of new designs. Hence, in the following section we will see some digital logic circuits using NMOS and CMOS families and their characteristics.

7.8 NMOS

In this section we will see some basic NMOS logic circuits

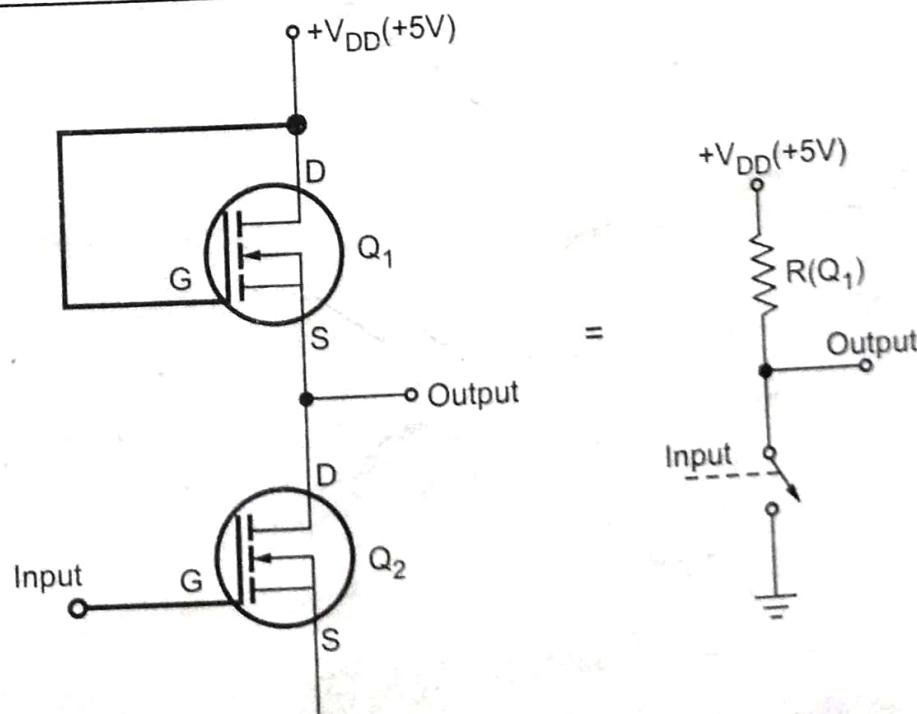
7.8.1 NMOS Inverter

Fig. 7.29 shows the basic NMOS inverter circuit. It contains two N-channel MOSFETs. Q_2 is a switching MOSFET and Q_1 is a load MOSFET. Q_1 acts as load resistance (R_d) for Q_2 . As gate of Q_1 is permanently connected to the V_{DD} , it is always ON, and hence the load resistance is equal to the R_{ON} of the MOSFET. Particularly, Q_1 is designed to have greater R_{ON} than the R_{ON} of Q_2 . To achieve this channel of Q_1 is made much narrower than channel of Q_2 . Typically R_{ON} of Q_1 is $100\text{ k}\Omega$ whereas R_{ON} of Q_2 is $1\text{ k}\Omega$. We know that MOS devices are voltage controlled devices. When positive voltage (HIGH input) is applied between gate and source, Q_2 is switched ON and it makes the output low. On the other hand, when input is LOW Q_2 is switched OFF and therefore, output is high.

Table 6.9 summarizes the operation of NMOS inverter

V_{IN} (VGS)	Q_2	$V_0 = \overline{V_{IN}}$
0 V (logic 0)	OFF	+ 5 V (logic 1)
5 V (logic 1)	ON	0 V (logic 0)

Table 7.10



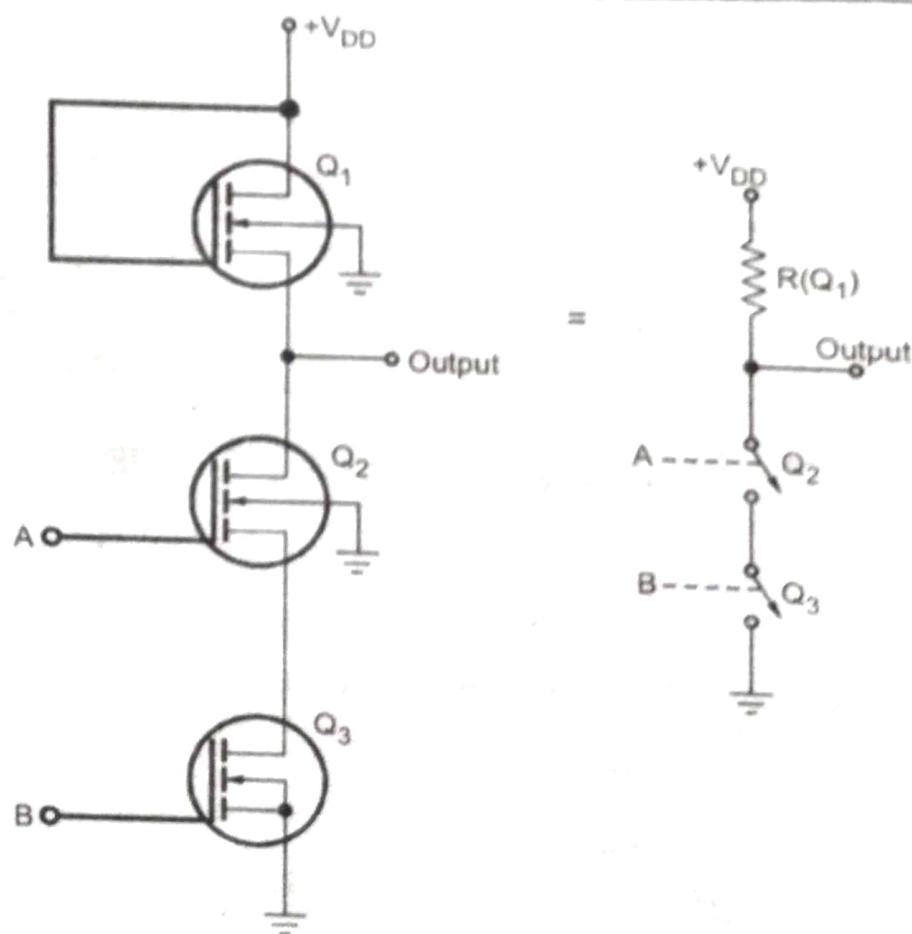
7.8.2 NMOS NAND Gate

Fig. 7.30 shows 2-input NMOS NAND gate. Q_1 acts as a load resistor and Q_2 and Q_3 are the switching MOSFETs controlled by the inputs A and B. Fig. 7.30(b) shows the equivalent switching circuit, consisting of a resistor and two switches in series. If either A or B or both inputs are low, the corresponding MOSFETs are OFF i.e., the corresponding switches are open and the output is high. If A and B both inputs are high, the corresponding MOSFETs are ON i.e., the corresponding switches are closed and the output is low.

Table 7.11 summarizes the operation of NMOS NAND gate

A	B	Q_2	Q_3	$V_o = \overline{AB}$
0	0	OFF	OFF	1
0	1	OFF	ON	1
1	0	ON	OFF	1
1	1	ON	ON	0

Table 7.11



(a) Schematic diagram

(b) Equivalent switching circuit

Fig. 7.30 2-input NMOS NAND gate

7.8.3 NMOS NOR Gate

Fig. 7.31(a) shows 2-input NMOS NOR gate. Q_1 acts as a load resistor and Q_2 and Q_3 are the switching MOSFETs controlled by the inputs A and B. Fig. 7.31 (b) shows the equivalent switching circuit, consisting of a resistor and two switches connected in parallel. When either or both input are high, the corresponding MOSFETs are ON i.e., corresponding switches are closed making the output low. If both inputs are low, both MOSFETs are OFF i.e., both switches are open and the output is high.

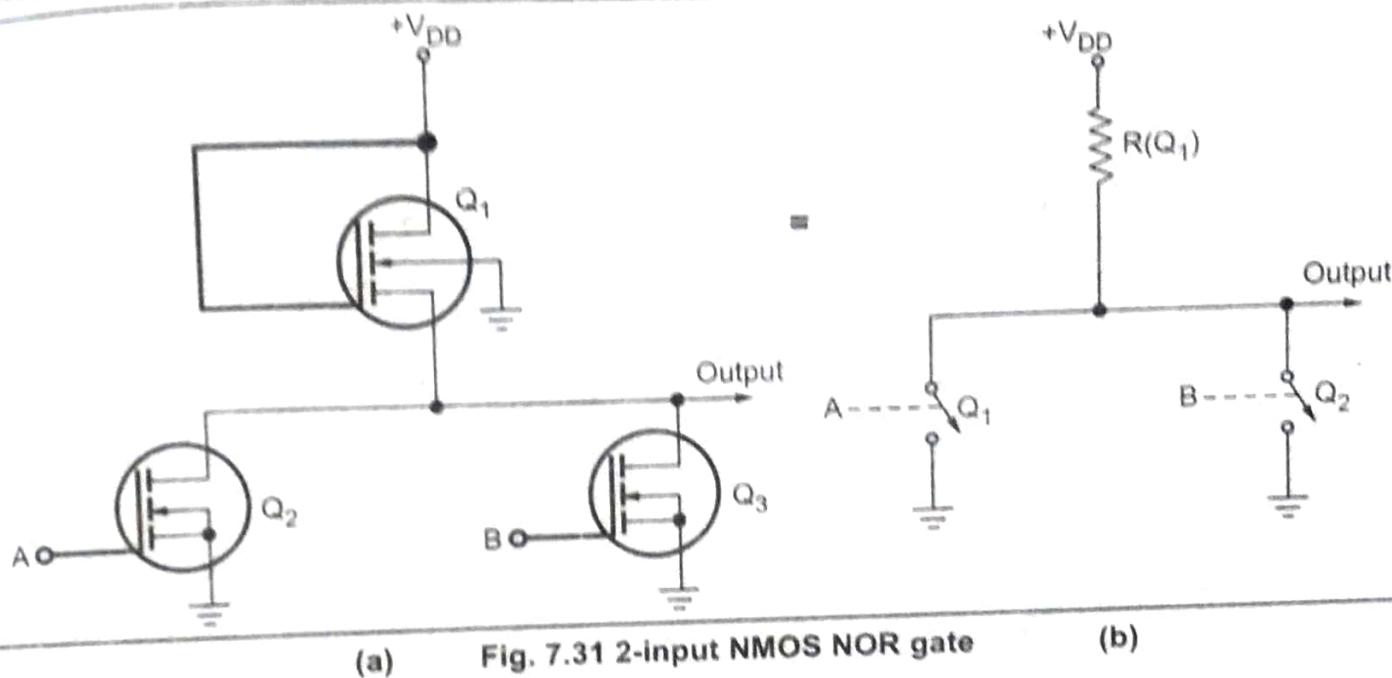


Table 7.12 summarizes the operation of NMOS NOR gate.

A	B	Q_2	Q_3	$V_o = \overline{A + B}$
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	0

Table 7.12

Characteristics of NMOS

Operating speed : Low operating speed with propagation delay time around 50ns. This is because it has high output resistance, very high input resistance and reasonably high input capacitance.

Noise Margin : Typically 1.5 V

Fan out : Typically 30

Power drain : Less, around 0.1 mW per gate.

7.9 CMOS

CMOS circuits contain both NMOS and PMOS devices to speed the switching of capacitive loads. It consumes low power and can be operated at high voltages, resulting in improved noise immunity.

7.9.1 CMOS Inverter

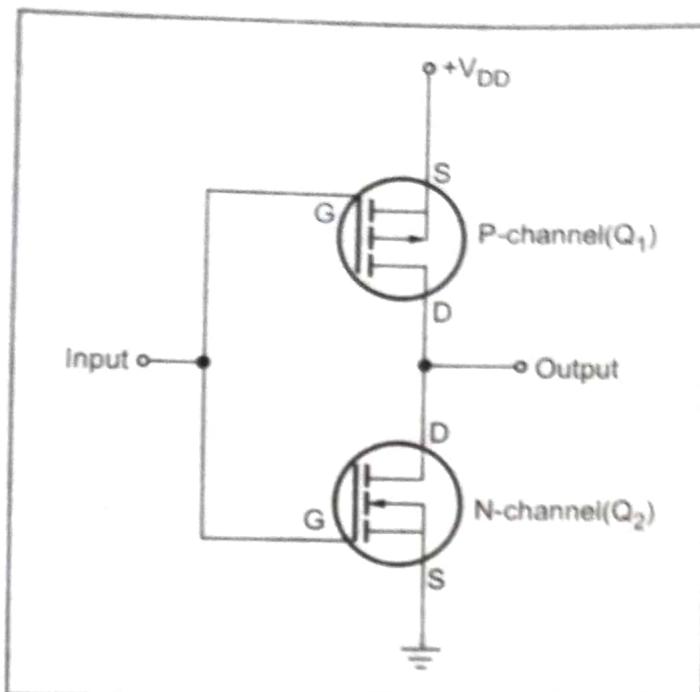
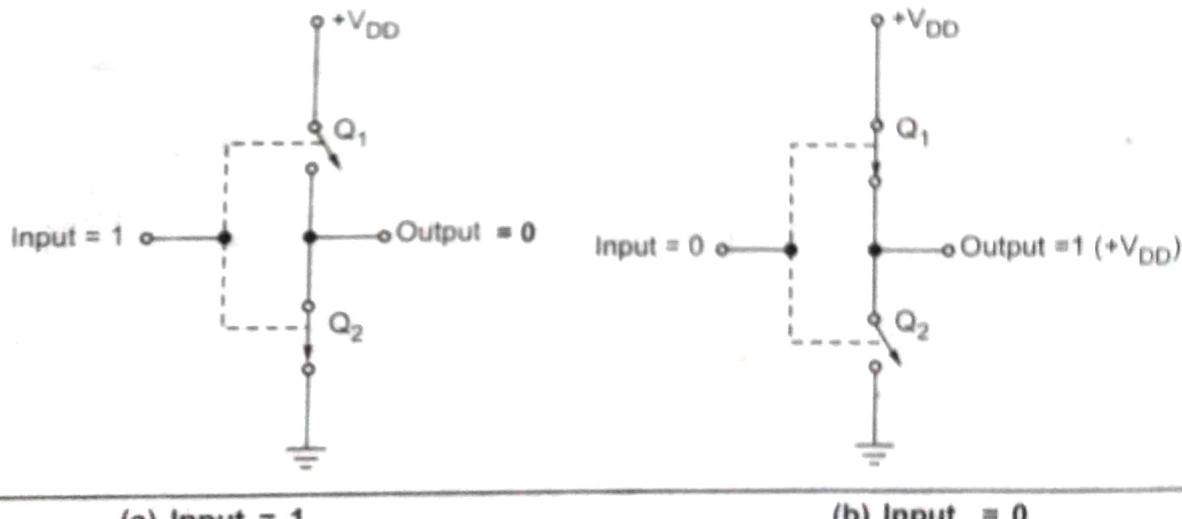


Fig. 7.32 CMOS inverter circuit

LOW, the gate of Q_1 (P-channel) is at a negative potential relative to its source while Q_2 has $V_{GS} = 0$ V. Thus, Q_1 is ON and Q_2 is OFF. This produces output voltage approximately $+V_{DD}$, as shown in the Fig. 7.33 (b).

Fig. 7.32 shows the basic CMOS inverter circuit. It consists of two MOSFETs in series in such a way that the P-channel device has its source connected to $+V_{DD}$ (a positive voltage) and the N-channel device has its source connected to ground. The gates of the two devices are connected together as the common input and the drains are connected together as the common output.

When input is HIGH, the gate of Q_1 (P-channel) is at 0V relative to the source of Q_1 i.e. $V_{GS1} = 0$ V. Thus, Q_1 is OFF. On the other hand, the gate of Q_2 (N-channel) is at $+V_{DD}$ relative to its source i.e. $V_{GS2} = +V_{DD}$. Thus, Q_2 is ON. This will produce $V_{OUT} \approx 0$ V, as shown in the Fig. 7.33 (a). When input is



(a) Input = 1

(b) Input = 0

Fig. 7.33 Operation of CMOS inverter for both input conditions

Table 7.13 summarizes the operation of CMOS inverter circuit

A	Q_1	Q_2	Output
0	ON	OFF	1
1	OFF	ON	0

Table 7.13 Truth table of inverter

7.9.2 CMOS NAND Gate

Fig. 7.34 shows CMOS 2-input NAND gate. It consists of two P-channel MOSFETs, Q_1 and Q_2 , connected in parallel and two N-channel MOSFETs, Q_3 and Q_4 connected in series.

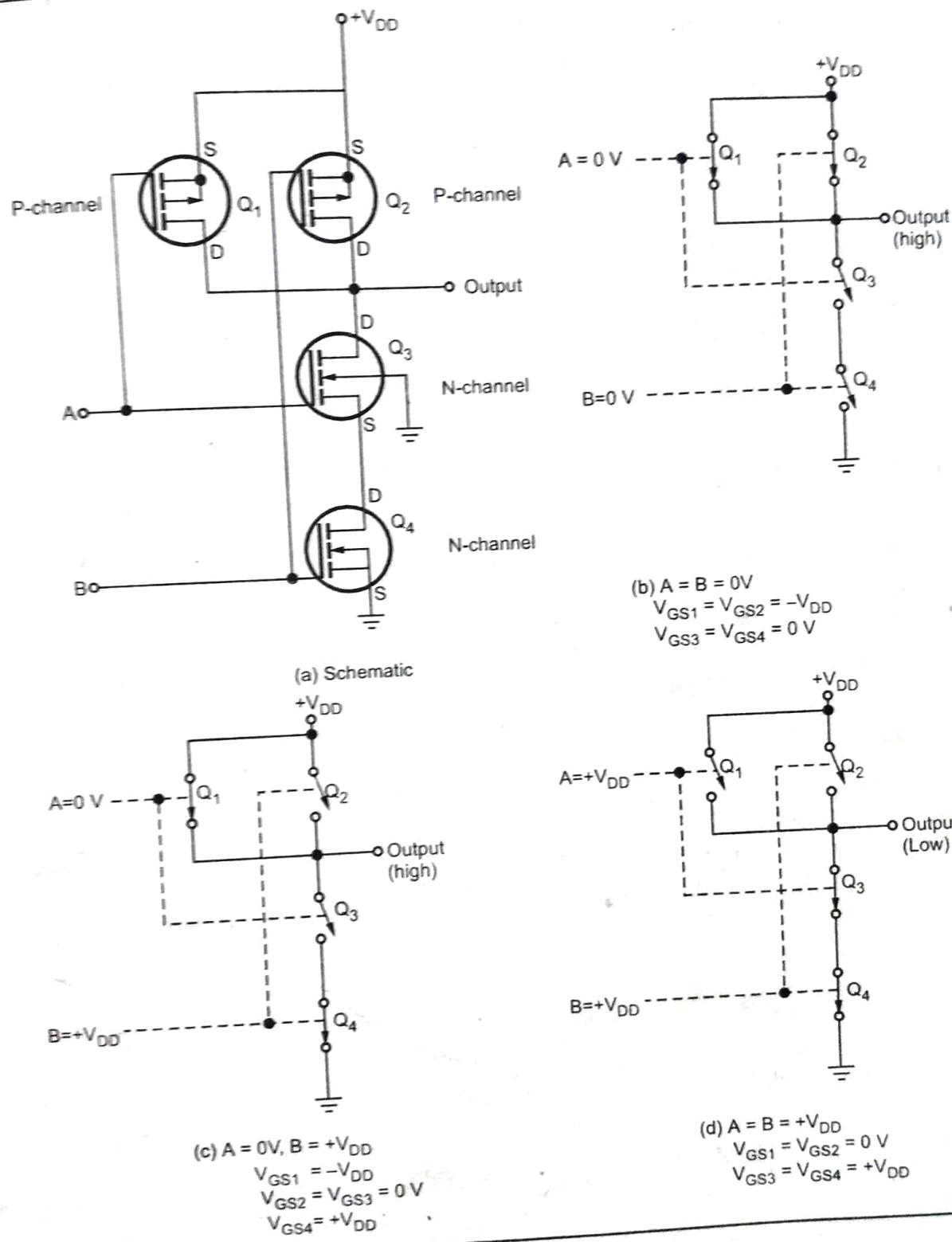


Fig. 7.34 CMOS NAND gate

* P-channel MOSFET is ON when its gate voltage is negative with respect to its source whereas N-channel MOSFET is ON when its gate voltage is positive with respect to its source

Fig. 7.34 (a) shows the equivalent switching circuit when both inputs are low. Here, the gates of both P-channel MOSFETs are negative with respect to their sources, since the sources are connected to $+V_{DD}$. Thus, Q_1 and Q_2 are both ON. Since the gate - to - source voltages of Q_3 and Q_4 (N-channel MOSFETs) are both 0V, those MOSFETs are OFF. The output is therefore connected to $+V_{DD}$ (HIGH) through Q_1 and Q_2 and is disconnected from ground, as shown in the Fig. 7.34 (b). Fig. 7.34 (c) shows the equivalent switching circuit when $A = 0$ and $B = +V_{DD}$. In this case, Q_1 is on because $V_{GS_1} = -V_{DD}$ and Q_4 is ON because $V_{GS_4} = +V_{DD}$. MOSFETs Q_2 and Q_3 are off because their gate-to-source voltages are 0 V. Since Q_1 is ON and Q_3 is OFF, the output is connected to $+V_{DD}$ and it is disconnected from ground. When $A = +V_{DD}$ and $B = 0V$, the situation is similar (not shown); the output is connected to $+V_{DD}$ through Q_2 and it is disconnected from ground because Q_4 is OFF. Finally, when both inputs are high ($A = B = +V_{DD}$), MOSFETs Q_1 and Q_2 are both OFF and Q_3 and Q_4 are both ON. Thus, the output is connected to the ground through Q_3 and Q_4 and it is disconnected from $+V_{DD}$. The Table 7.14 summarizes the operation of 2-input CMOS NAND gate.

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

Table 7.14 Truth table of NAND gate

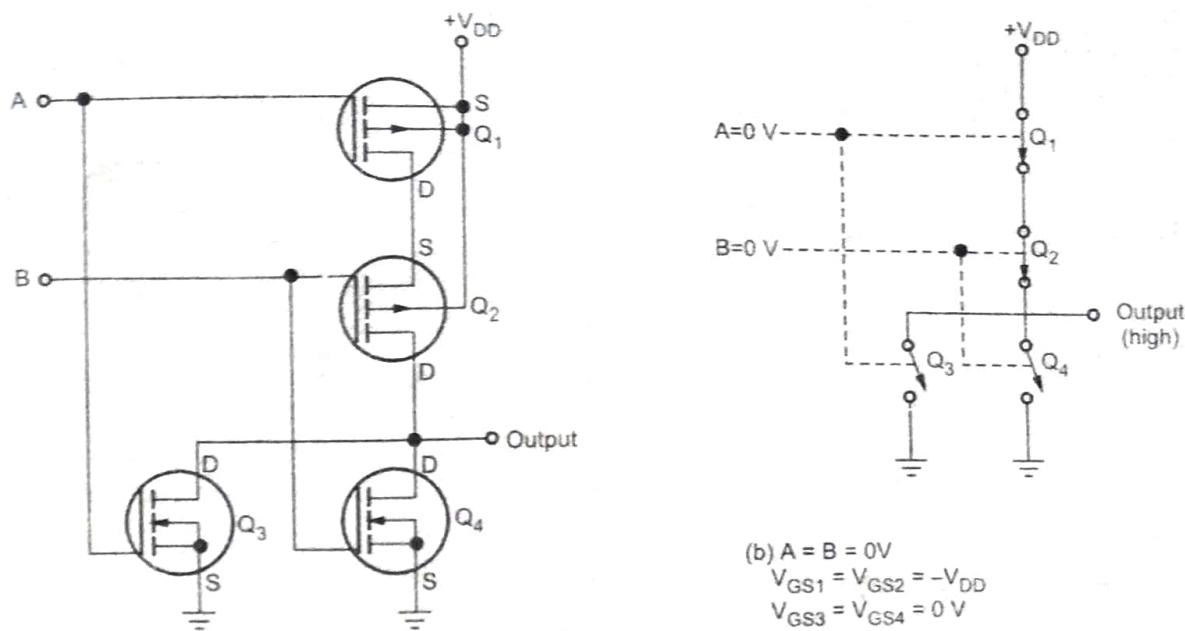
7.9.3 CMOS NOR Gate

Fig. 7.35 shows 2-input CMOS NOR gate. Here, P-channel MOSFETs Q_1 and Q_2 are connected in series and N-channel MOSFETs Q_3 and Q_4 are connected in parallel.

Like NAND circuit, this circuit can be analyzed by realizing that a LOW at any input turns ON its corresponding P-channel MOSFET and turns OFF its corresponding N-channel MOSFET, and vice versa for a HIGH input. This is illustrated in Fig. 7.35. The Table 7.15 summarizes the operation of 2-input NOR gate.

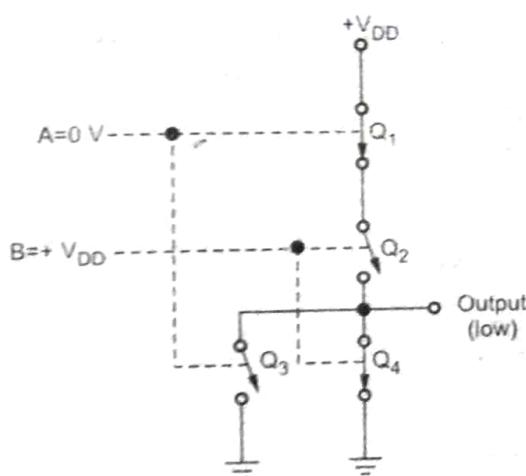
A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

Table 7.15 Truth table for NOR gate

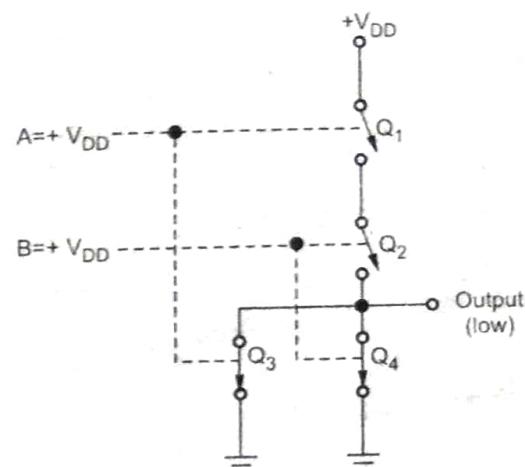


(a) Schematic

$$\begin{aligned} (b) \quad & A = B = 0V \\ & V_{GS1} = V_{GS2} = -V_{DD} \\ & V_{GS3} = V_{GS4} = 0V \end{aligned}$$



$$\begin{aligned} (c) \quad & A = 0V, B = +V_{DD} \\ & V_{GS1} = -V_{DD} \\ & V_{GS2} = V_{GS3} = 0V \\ & V_{GS4} = +V_{DD} \end{aligned}$$



$$\begin{aligned} (d) \quad & A = B = +V_{DD} \\ & V_{GS1} = V_{GS2} = 0V \\ & V_{GS3} = V_{GS4} = +V_{DD} \end{aligned}$$

Fig. 7.35 CMOS NOR gate

7.9.4 Characteristics of CMOS

Operating Speed : Slower than TTL series. Approximately 25 to 100 ns depending on the subfamily of CMOS. It also depends on the power supply voltage.

Voltage levels and Noise Margins : The voltage levels for CMOS varies according to their subfamilies. These are listed in Table 7.16. Noise margins in table are calculated as follows.

$$\begin{aligned} V_{NH} &= V_{OH(\min)} - V_{IH(\min)} \\ V_{NL} &= V_{IL(\max)} - V_{OL(\max)} \end{aligned}$$

Parameter	CMOS series				
	4000-B	74 HC	74 HCT	74 AC	74 ACT
$V_{IL(\text{min})}$	3.8	3.8	2.0	3.8	2.0
$V_{IL(\text{max})}$	1.5	1.0	0.8	1.5	0.8
$V_{OL(\text{min})}$	4.95	4.9	4.9	4.9	4.9
$V_{OL(\text{max})}$	0.05	0.1	0.1	0.1	0.1
V_{NH}	1.45	1.4	2.9	1.4	2.9
V_{NI}	1.45	0.9	0.7	1.4	0.7

Table 7.16

Fanout : The CMOS inputs have an extremely large resistance ($10^{12}\Omega$) that draws essentially no current from the signal source. Each CMOS input, however, typically presents a 5 pF load to ground as shown in the Fig. 7.36. This input capacitance limits the number of CMOS inputs that one CMOS output can drive.

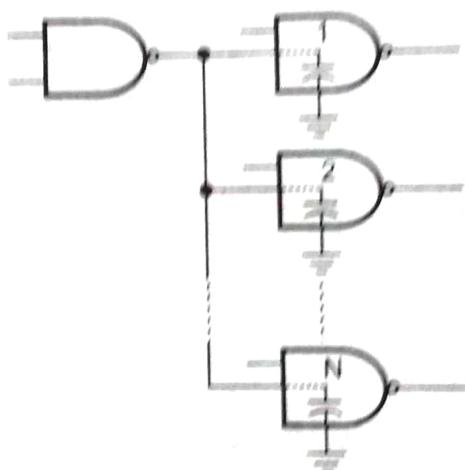


Fig. 7.36 One CMOS output driving several CMOS inputs

The CMOS output has to charge and discharge the parallel combination of all the input capacitances. This charging and discharging time increases as we increase number of loads. Typically, each CMOS load increases the driving circuit's propagation delay by 3 ns. Thus, fan-out for CMOS depends on the permissible maximum propagation delay. Typically, CMOS outputs are limited to a fan-out of 50 for low-frequency operation ($\leq 1\text{ MHz}$). Of course, for high-frequency operation the fan-out would have to be less.

Power Dissipation (P_D) : The power dissipation of a CMOS IC is very low as long as it is in a dc condition. Unfortunately, power dissipation of CMOS IC increases in proportion to the frequency at which the circuits are switching states. For example, a CMOS NAND gate that has $P_D = 10\text{ nW}$ under DC conditions will have $P_D = 0.1\text{ mW}$ at a frequency of 100 kHz , and 1 mW at 1 MHz .

When CMOS output switches from LOW to HIGH, a transient charging current has to be supplied to the load capacitance. Therefore, as the switching frequency increases, the average current drawn from V_{DD} also increases, resulting increase in power dissipation.

Propagation Delay : The propagation delay in CMOS is the sum of delay due to internal capacitance and due to load capacitance. The delay due to internal capacitance is called the intrinsic propagation delay. The delay due to load capacitance can be approximated as follows :

$$t_p(C_L) \approx 0.5 R_o C_L \text{ seconds}$$

where $t_p(C_L)$ is either t_{PLH} or t_{PHL} .

R_o is the output resistance of the gate, and C_L is the total load capacitance.

The R_o depends on the supply voltage and it can be approximated as

$$R_o \approx \frac{V_{CC}}{I_{os}}$$

where I_{os} is the short circuit output current.

Unused Inputs : CMOS inputs should never be left disconnected. All CMOS inputs have to be tied either to a fixed voltage level (0V or V_{DD}) or to another input. This rule applies even to the inputs of extra unused logic gates on a chip. An unused CMOS input is susceptible to noise and static charges that could easily bias both the P-and N-channel MOSFETs in the conductive state, resulting in increased power dissipation and possible overheating.

Static-charge susceptibility (CMOS Hazards) : Every CMOS device is vulnerable to the building up of electrical charge on its insulated gate. Recall that the relationship between charge Q and voltage V on a capacitor having capacitance C is

$$V = \frac{Q}{C}$$

Since the input capacitance at the gate is usually quite small (a few picofarads), a relatively small amount of charge can create a large voltage which may be greater than the breakdown voltage of a MOS gate (typically 100 V).

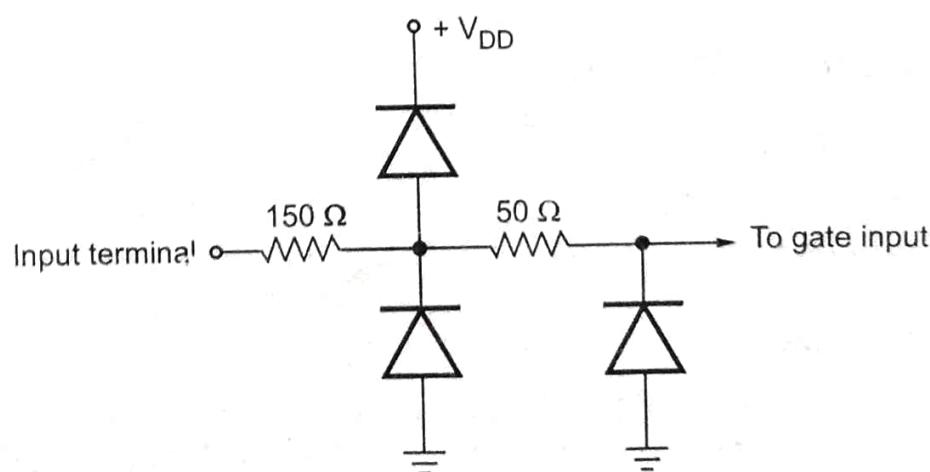


Fig. 7.37 Typical network used to protect CMOS from static charges

The primary source of charge is "static" electricity, usually produced by handling and the motion of various kinds of plastics and textiles. The CMOS devices are protected against this static charge by on-chip diode-resistor network, as shown in the Fig. 7.37. These diodes are designed to turn ON and limit the size of the input voltage to well below any damaging value.

Latch-up : CMOS integrated circuits contain parasitic PNP and NPN transistors : transistors that exist because of the proximity of P and N materials embedded in the substrate. Their existence is not intentional but is unavoidable. Because of conducting paths between a pair of such transistors, a device can be triggered into a heavy conduction mode, known as **latch-up**. This heavy conduction mode, results large current flow which can destroy IC. Most CMOS circuits contain protective measures to prevent latch-up, but it can still occur if the manufacturers specified maximum ratings are exceeded.

7.10 Interfacing CMOS and TTL Devices

Interfacing means connecting the output(s) of one circuit or system to the input(s) of another circuit or system that may have different electrical characteristics. When two circuits have different electrical characteristics direct connection cannot be made. In such cases driver and load circuits are connected through interface circuit. Its function is to take the driver output signal and condition it so that it is compatible with requirements of the load.

One must consider following important points while interfacing two circuits or systems.

- The driver output must satisfy the voltage and current requirements of the load circuit.
- The driver and load circuit may require different power supplies. In such cases the output of both circuit must swing between its specified voltage ranges.

7.10.1 TTL Driving CMOS

Here, TTL is a driver circuit and CMOS is a load circuit. The two circuits are from different families with different electrical characteristics. Therefore, we must check that the driving device can meet the current and voltage requirements of the load device.

Parameter	CMOS		TTL		
	4000B	74HC/HCT	74	74LS	74AS
I _{IH} (max)	1 μA	1 μA	40 μA	20 μA	200 μA
I _{IL} (max)	1 μA	1 μA	1.6 mA	0.4 mA	2 mA
I _{OH} (max)	0.4 mA	4 mA	0.4 mA	0.4 mA	2 mA
I _{OL} (max)	0.4 mA	4 mA	16 mA	8 mA	20 mA

Table 7.17 Input/output currents for standard devices with supply voltage of 5 V

Table 7.17 indicates that the input current values for CMOS are extremely low compared with the output current capabilities of any TTL series. Thus, TTL has no problem meeting the CMOS input current requirements.

But when we compare the TTL output voltages with the CMOS input voltage requirements we find that :

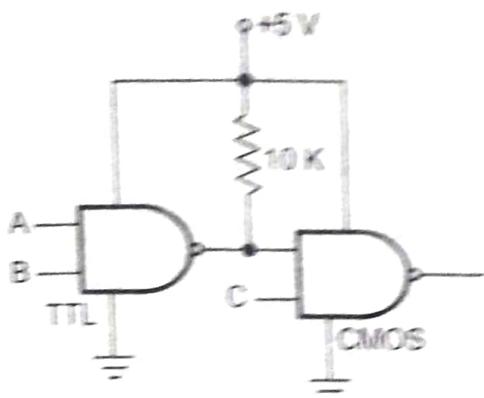


Fig. 7.38 TTL driving CMOS using external pull-up resistor

input voltage level.

TTL Driving HIGH Voltage CMOS : When output CMOS circuit is operating with V_{DD} greater than 5V, the situation becomes more difficult. The outputs of many TTL devices cannot be operated at more than 5V. In such cases some alternative arrangement are made. Two of them are discussed below :

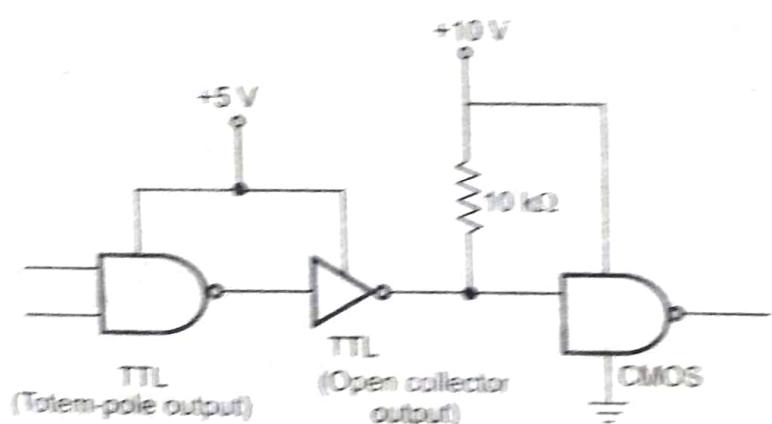


Fig. 7.39 Open collector buffer used as interface circuit

$V_{OH\ min}$ for TTL $\ll V_{IH\ min}$ for CMOS for these situations TTL output must be raised to an acceptable level for CMOS. This can be done by connecting pull-up resistor at the output of TTL, as shown in the Fig. 7.38. The pull-up resistor causes the TTL output to rise to approximately 5 V in the HIGH state, thereby providing an adequate CMOS

1. When the TTL output cannot be pulled up to V_{DD} , one can use open collector buffer as an interface between totem-pole TTL output and CMOS operating at $V_{DD} > 5V$, as shown in the Fig. 7.39.

2. The second alternative is to use level translator circuit, such as the 40104. This is a CMOS chip that is designed to take a low-voltage input (e.g., from TTL) and translate it to high voltage output for CMOS. Fig. 7.40 shows the circuit arrangement.

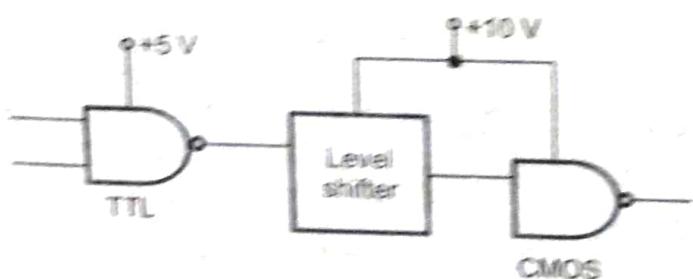


Fig. 7.40 Level shifter used as interface circuit

7.10.2 CMOS Driving TTL

Before we consider the problem of interfacing CMOS outputs to TTL inputs, it will be helpful to review the CMOS output and TTL input characteristics for the two logic states.

For CMOS (4000B)	For TTL
$V_{OH(\min)} : 4.95 \text{ V}$	$V_{IH(\min)} : 2.0 \text{ V}$
$V_{OL(\max)} : 0.05 \text{ V}$	$V_{IL(\max)} : 0.8 \text{ V}$
$I_{OH(\max)} : 0.4 \text{ mA}$	$I_{IH(\max)} : 40 \mu\text{A}$
$I_{OL(\max)} : 0.4 \text{ mA}$	$I_{IL(\max)} : 1.6 \text{ mA}$

Table 7.18

CMOS Driving TTL in the HIGH state : Above voltage parameters show that CMOS outputs can easily supply enough voltage (V_{OH}) to satisfy the TTL input requirement in the HIGH state (V_{IH}). The parameters also show that CMOS outputs can supply more than enough current (I_{OH}) to meet the TTL input current requirements (I_{IH}). Thus no special consideration is required for CMOS driving TTL in the HIGH state.

CMOS Driving TTL in LOW state : The parameters in the Table 7.18 show that CMOS output voltage (V_{OL}) satisfies TTL input requirement in the LOW state (V_{IL}).

However, the current requirements in the LOW state are not satisfied. The TTL input has a relatively high input current in the LOW state (1.6 mA) and CMOS output current at LOW state (I_{OL}) is not sufficient to drive even one input of the TTL. In such situations some type of interface circuit is needed between the CMOS and TTL devices. Fig. 7.41 shows the possible interface circuit.

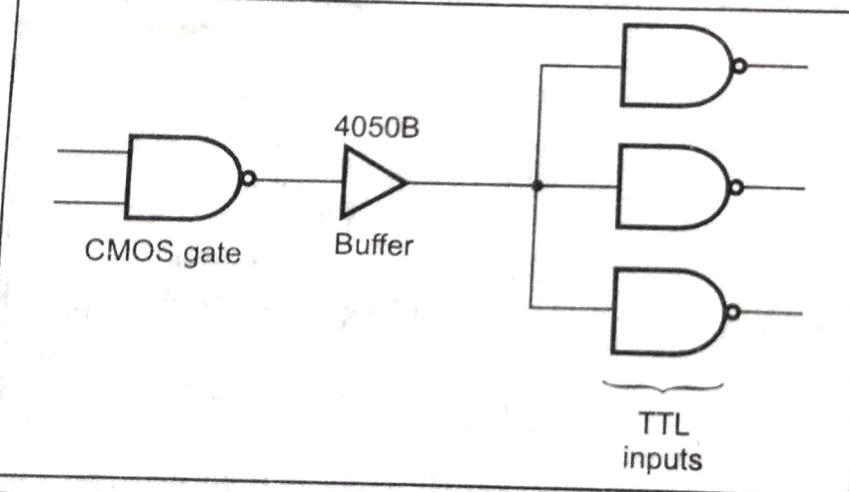


Fig. 7.41 CMOS driving TTL in LOW state using buffer

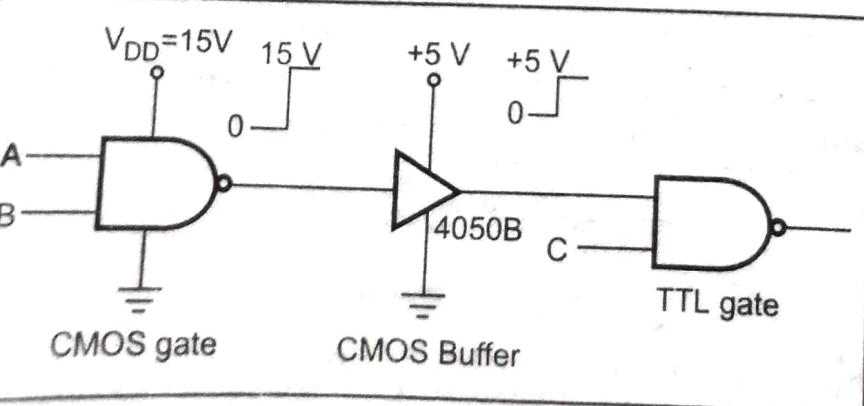


Fig. 7.42 Level translation using CMOS buffer

In Fig. 7.41 the CMOS 4050B, noninverting buffer is used as an interfacing circuit. It has an output current rating of $I_{OL(\max)} = 3 \text{ mA}$ which satisfies the TTL input current requirement.

HIGH Voltage CMOS Driving • TTL : Some IC manufacturers have provided several 74LS TTL devices that can

withstand input voltages as high as 15V. These devices can be driven directly from CMOS outputs operating at $V_{DD} = 15$ V. However, most TTL inputs cannot handle more than 7 V, and so interface is necessary if they are to be driven from high-voltage CMOS. In such situations **voltage level translators** are used. They convert the high voltage input to a 5V output that can be connected to TTL. Fig. 7.42 shows how the 4050B can be used to perform this level translation between 15 V and 5 V.

7.11 Comparison of CMOS and TTL Families

Parameter	CMOS		TTL			
	Silicon gate CMOS	Metal gate CMOS	74	74LS	74AS	74ALS
V_{IH} (min)	3.5	3.5	2.0	2.0	2.0	2.0
V_{IL} (max)	1.0	1.5	0.8	0.8	0.8	0.8
V_{OH} (min)	4.9	4.95	2.4	2.7	2.7	2.7
V_{OL} (max)	0.1	0.05	0.4	0.5	0.5	0.4
V_{NH}	1.4	1.45	0.4	0.7	0.7	0.7
V_{NL}	0.9	1.45	0.4	0.3	0.3	0.4
Propagation Delay (ns)	8	105	10	10	1.5	4
Power per gate (mW)	0.17	0.1	10	2	8.5	1
Speed power product or figure of merit	1.4 pJ	10.5 pJ	100 pJ	20 pJ	12.8 pJ	4 pJ
Input connection	Input cannot be left open. It has to be connected to 0, or to V_{DD} or to the another input.		Input can be left open. It is treated as logic high input.			
Power dissipation	Very less, but increases with increase in switching speed		More than CMOS. It is constant, does not depend on switching speed.			
Fan out	Fan-out is more than TTL typically 50		Fan-out for TTL is 10.			
Noise	More susceptible to noise		Less susceptible to noise			

Table 7.19

7.12 Introduction to Emitter Coupled Logic

The TTL family uses transistors operating in the saturation mode. As a result, their switching speed is limited by the storage delay time associated with a transistor that is driven into saturation. Another logic family has been developed that prevents transistor saturation, thereby increasing overall switching speed by using a radically different circuits structure, called **current mode logic** (CML). This logic family is also called **emitter-coupled logic** (ECL). This family belongs to non saturated logic systems.

Unlike TTL and CMOS families, ECL does not produce a large voltage swing between the LOW and HIGH levels. It has a small voltage swing, less than a volt, and it internally switches current between two possible paths, depending on the output state.

7.12.1 ECL Characteristics

1. It is the fastest of logic families. The popular 10K and 100K ECL families offer propagation delays as short as 1ns. The latest ECL family, ECL in PS (ECL in picoseconds), offers maximum delays under 0.5 ns (500 ps).
2. Transistors are not allowed to go into complete saturation and thus eliminating storage delays.
3. To prevent transistors from going into complete saturation, logic levels are kept close to each other. Due to this transistor is not driven into saturation when its input switches from low to high.
4. As logic levels are kept close to each other, noise margin is reduced and it is difficult to achieve good noise immunity.
5. Another disadvantage of this approach is that power consumption is more because transistors are not completely saturated.
6. Switching transients are less because power supply current is more stable than in TTL and CMOS circuits.

7.12.2 Basic ECL Circuit

The Fig. 7.43 shows the basic inverter/buffer circuit in ECL family. It consists of two transistors connected in differential single ended input mode with a common emitter resistance. The circuit has two outputs : inverting output (OUT1) and noninverting output (OUT2). For this circuit, the input LOW and HIGH voltage levels are defined as 3.6V and 4.4V, and it produces output LOW and HIGH levels as 4.2 V and 5.0V.

When V_{IN} is HIGH (4.4V), (see bold figures) transistor Q_1 is ON, but not saturated and transistor Q_2 is OFF. Thus, V_{OUT2} is pulled to 5.0V (HIGH) through R_2 and drop across R_1 is 0.8V so that V_{OUT1} is 4.2V (LOW).

When V_{IN} is LOW (3.6V) (see normal figures), transistor Q_2 is ON, but not saturated and transistor Q_1 is OFF. Thus, V_{OUT1} is pulled to 5.0V (HIGH) through R_1 and drop across R_2 is 0.8V so that V_{OUT2} is 4.2V (LOW).

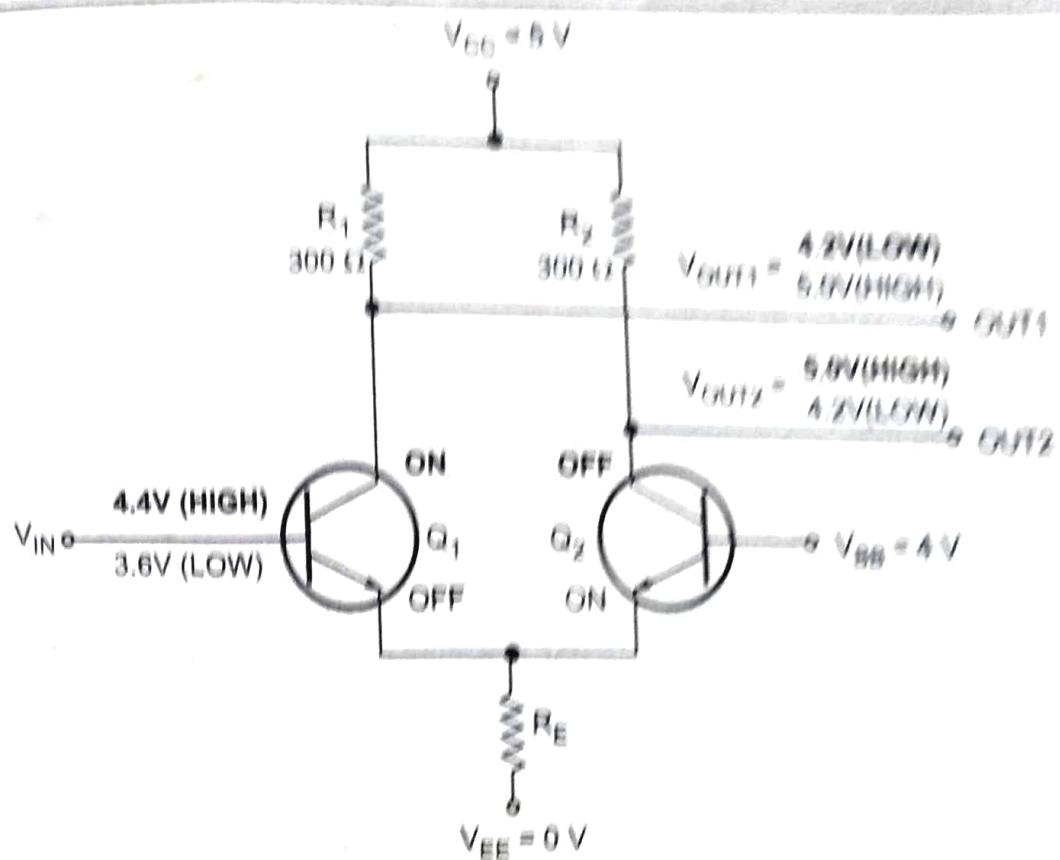


Fig. 7.43 Basic ECL inverter/buffer circuit

7.12.3 ECL OR/NOR Gate

Fig. 7.44 shows, 2-input ECL OR/NOR gate and its logic symbol. It has an additional transistor in parallel with Q_1 as compared to ECL inverter. If any input is HIGH corresponding transistor is active, and V_{OUT1} is LOW (NOR output). At the same time Q_2 is OFF producing V_{OUT2} HIGH (OR output).

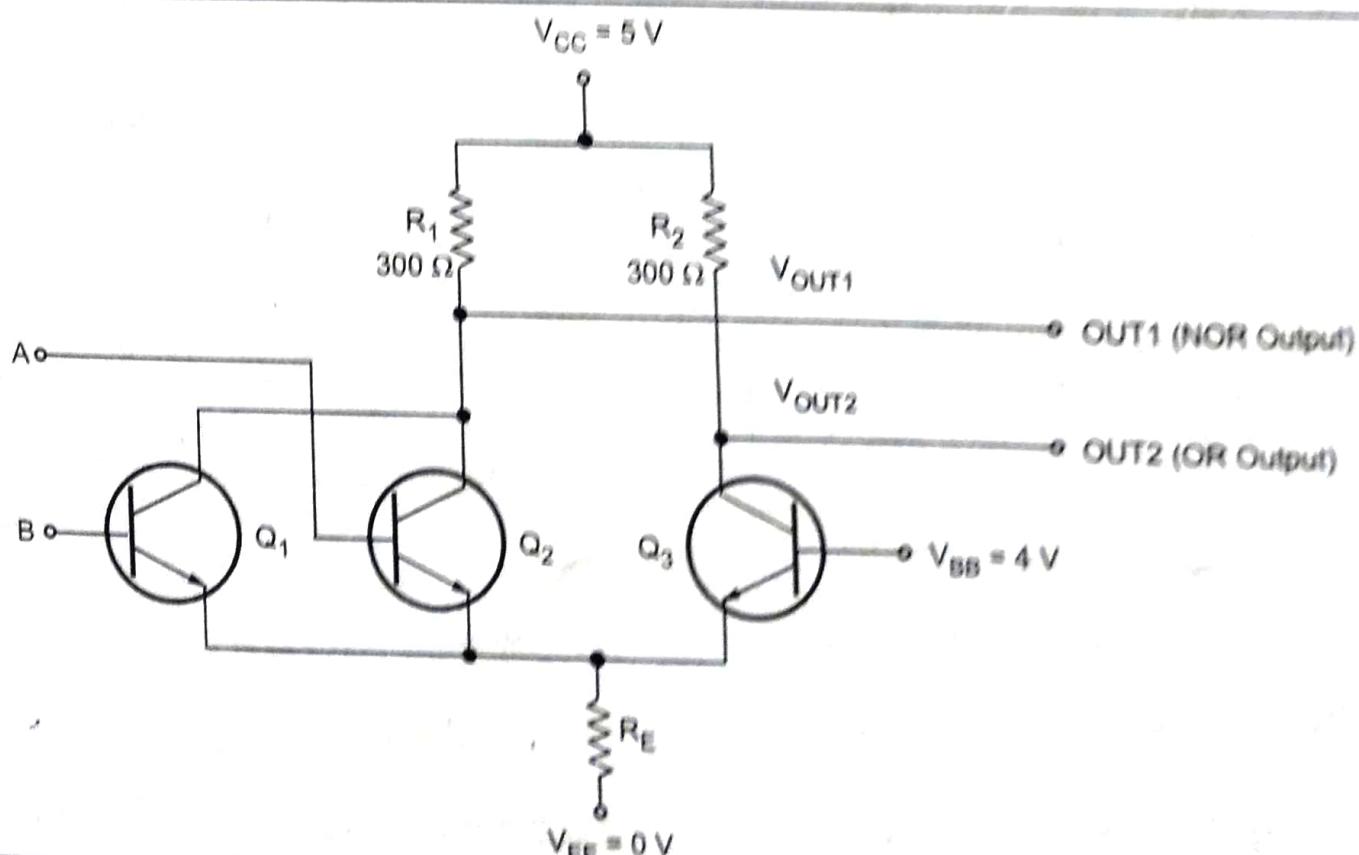


Fig. 7.44 (a) 2-Input ECL OR/NOR gate

We can observe that the input and output LOW and HIGH voltage levels for basic ECL family are not same, it has 0.6V difference. This is a problem. This problem can not be solved by connecting diode in series with output to lower its voltage by 0.6 volt because if we does this, it results poor fanout. Another problem occurs when output is HIGH and it drives an another ECL input. This HIGH output has to drive base current of another ECL input, resulting drop across R_1 or R_2 , reducing the output voltage. These problem of basic ECL are solved by 10K ECL family.



Fig. 7.44 (b) Logic symbol

7.12.4 ECL 10K Family

Improvement Over Basic ECL Family

- An emitter follower output stage is added to shift the output and input levels and to provide very high current-driving capacity, up to 50mA per output.
- An internal bias network is added to provide V_{BB} without the need for a separate, external power supply.
- It is designed to operate with $V_{CC} = 0$ and $V_{EE} = -5.2V$, to improve noise immunity.

Voltage Levels and Noise Margin

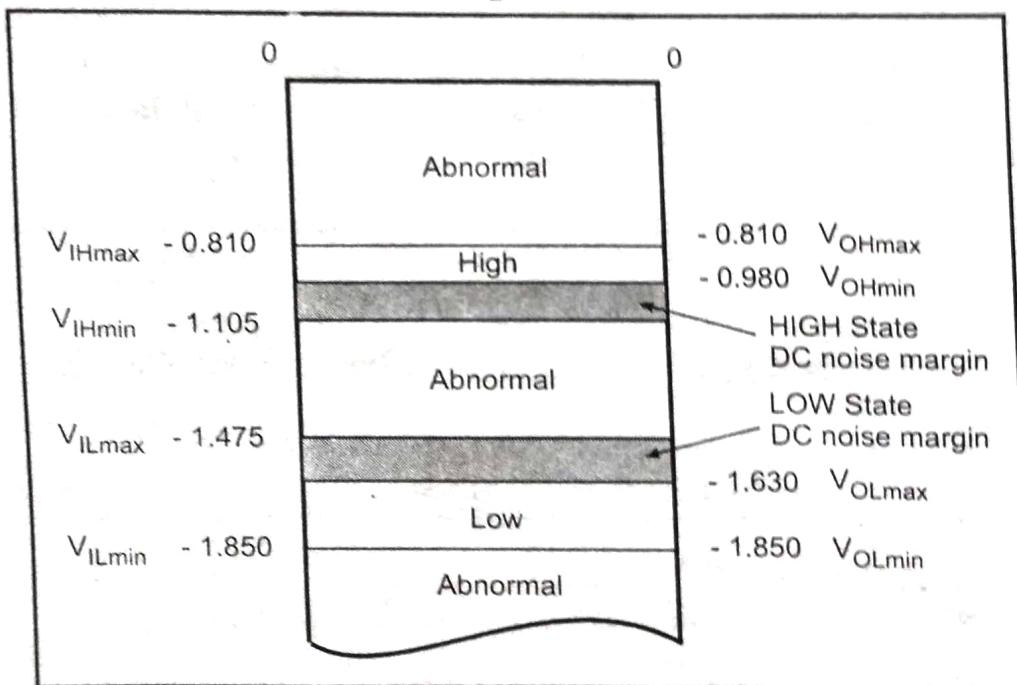


Fig. 7.45

than TTL and CMOS noise margins.

ECL 10K 2-input OR/NOR Gate

The Fig. 7.46 shows the 10K ECL 2-input OR/NOR Gate. As mentioned earlier it has two additional components : bias network and complementary emitter-follower pair. The

The Fig. 7.45 shows the voltage levels and noise margin provided by 10K ECL family. As shown in the Fig. 7.45, even though power supply is ECL negative assigns the names LOW and HIGH to the algebraically lower and higher voltages, respectively.

The DC noise margins for ECL are 0.155 V in the low state and 0.125 V in the high state. These noise margins are much less

Pull-down resistors are provided at the two inputs of OR/NOR gate. They ensure that if the input is left unconnected, it is treated as LOW. The bias network component values are selected to provide $V_{BB} = -1.29$ V. The complementary emitter-follower outputs shift the output voltage levels down by 0.6 volts matching input and output voltage levels and increase the current sourcing capacity. As shown in the Fig. 7.46, the emitter follower outputs used in ECL 10K requires external pull-down resistors.

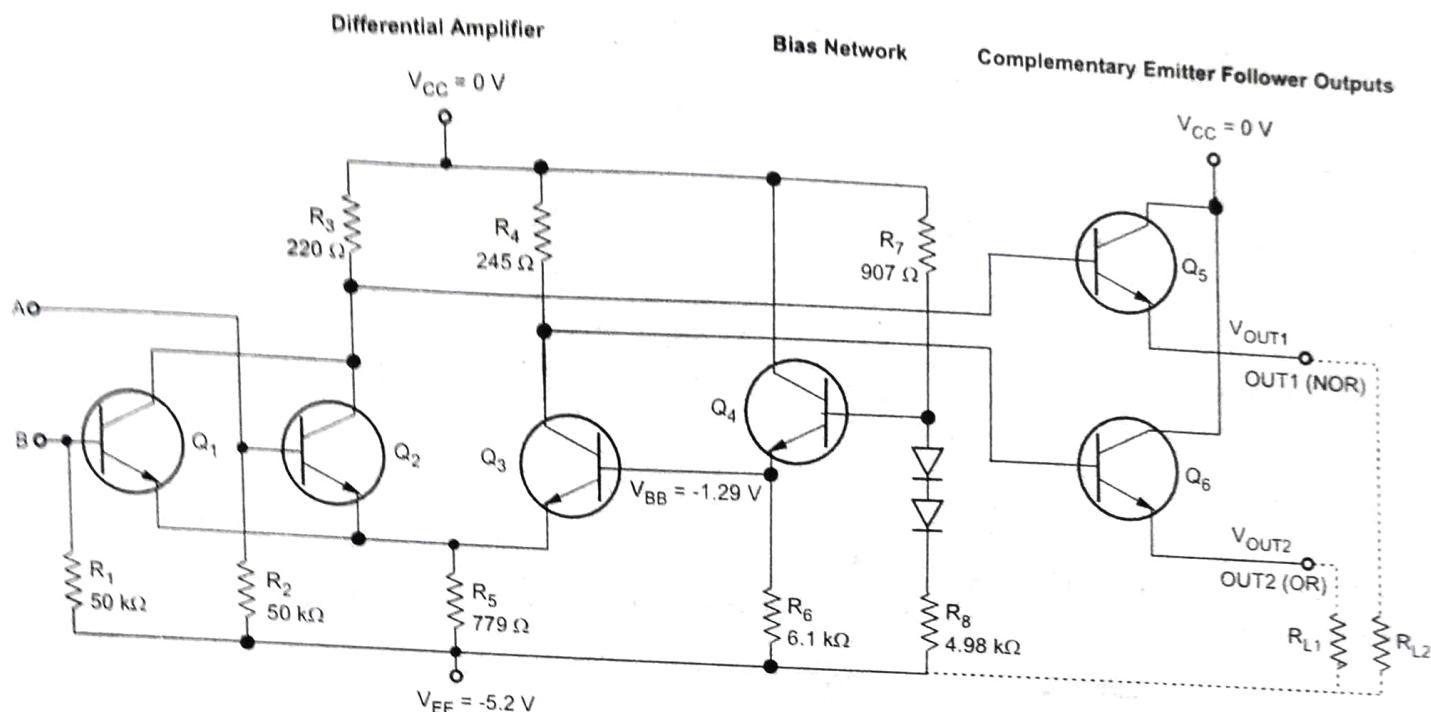


Fig. 7.46 Two input 10K ECL OR/NOR gate

7.12.5 ECL 100K Family

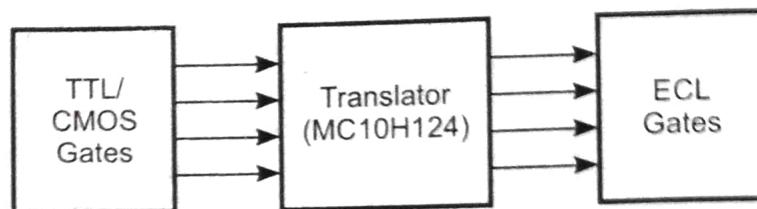
This family has 100xxx (100101, 100107, 100170) part numbers. The differences in 10K and 100K ECL family are as follows :

Parameters	ECL 10 K	ECL 100 K
Power supply voltage	- 5.2 volts	- 4.5 volts
Propagation delay	2 ns	0.75 ns
Transitions times	1.75 ns	0.75 ns
Power conjunction	20 mW	14 mW

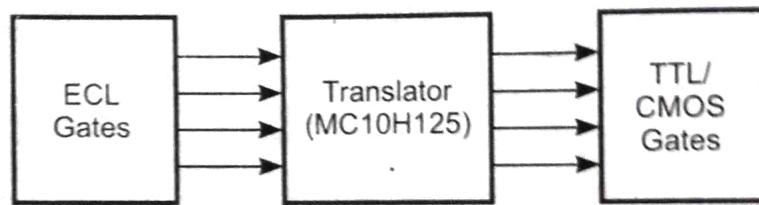
Table 7.20 Comparison between ECL 10 K and ECL 100 K families

7.12.6 Interfacing CMOS and TTL with ECL Gates

We have seen that logic levels for ECL gates are very different from those of TTL and CMOS gates. Therefore, for interfacing ECL gates with TTL and CMOS gates requires more than just a pull-up resistor. Special level-shifting circuits called **translators** are available in the ECL family to allow interfacing ECL with other families Fig. 7.47 shows the required interfacing circuits.



(a) TTL/CMOS to ECL interfacing



(b) ECL to TTL/CMOS interfacing

Fig. 7.47 Interfacing TTL/CMOS and ECL

7.13 Integrated Injection Logic (I^2L)

The integrated injection logic uses only bipolar transistors for the construction of gates. They don't use resistors. Because of absence of space consuming resistors it makes it possible to integrate a large number of gates in a single package. Therefore, compared to other families, circuits in I^2L family are easy to fabricate and they are economical. The speed-power product of I^2L circuits is quite small, on the order of 4 pJ, so it is comparable to advanced low-power schottky TTL.

7.13.1 I^2L Inverter

Before going to study the I^2L inverter we will see the simple circuit with same operating principle. Fig. 7.48 shows the simple inverter circuit. Here, Q_1 transistor serves as a constant current source that supplies current to node X. The direction that the current flows after entering node X depends on the input voltage level. When input is low, it sinks the current and current is diverted from the base of Q_2 , making Q_2 off. As Q_2 is off, output is high. When input is high, the constant current flows into the base of Q_2 , making Q_2 ON. As Q_2 is ON, output is low.

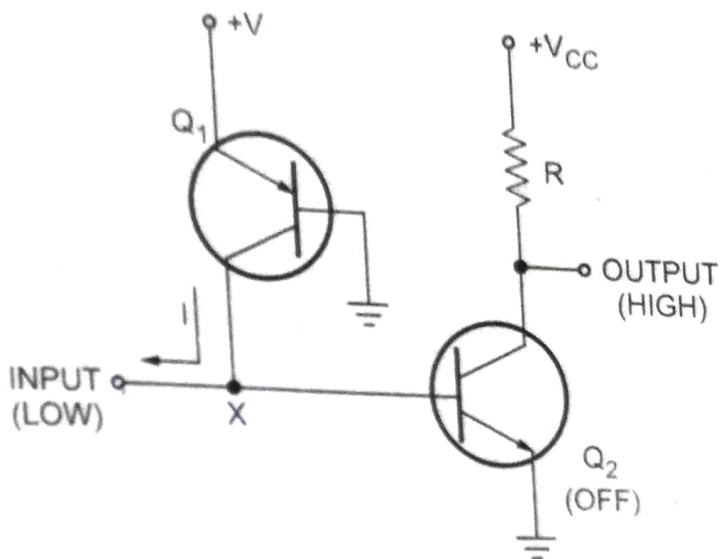


Fig. 7.48 (a) A low input sinks the injected current, thus holding Q_2 off and making the output high

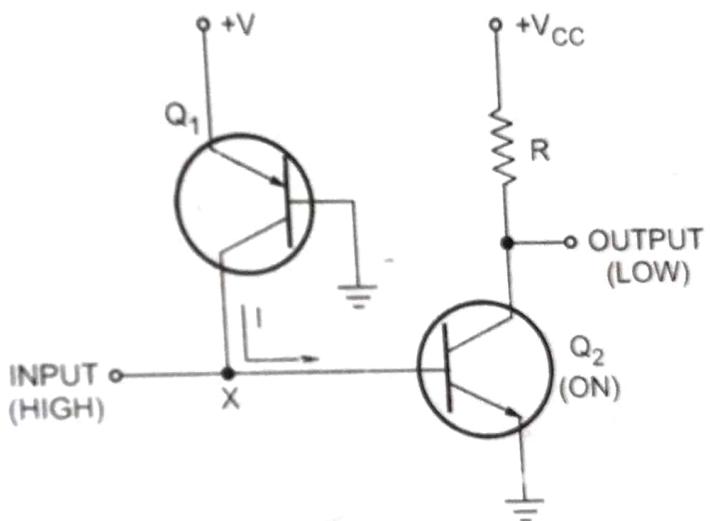


Fig. 7.48 (b) A high input causes the injected current to flow into Q_2 , turning it on and making the output low

Let us study the I^2L inverter circuit. Fig. 7.48 (c) and (d) shows the I^2L inverter circuit. Here output transistor has two collectors, producing two equal outputs and instead of collector resistor, the outputs are connected directly to the inputs of other I^2L gates. Fig. 7.48 (e) and (f) shows I^2L inverter driving other two inverters. When the input of Q_1 is high, Q_2 is ON and its output therefore serves as a current sink to draw current from Q_3 and Q_4 . Q_5 and Q_6 are therefore both off. (Refer Fig. 7.48 (e)). When the input to Q_1 is low, Q_2 is off and on current is drawn from Q_3 and Q_5 . Q_4 and Q_6 are both on and can sink current from other gates. (Refer Fig. 7.48 (f)).

The supply voltage used in I²L family is very small on the order of 0.8 V to keep current flowing through transistors low. The speed and power dissipation of an I²L gate depends heavily on the value of voltage source V. Increase in V increases power dissipation but reduces propagation delay, increasing speed.

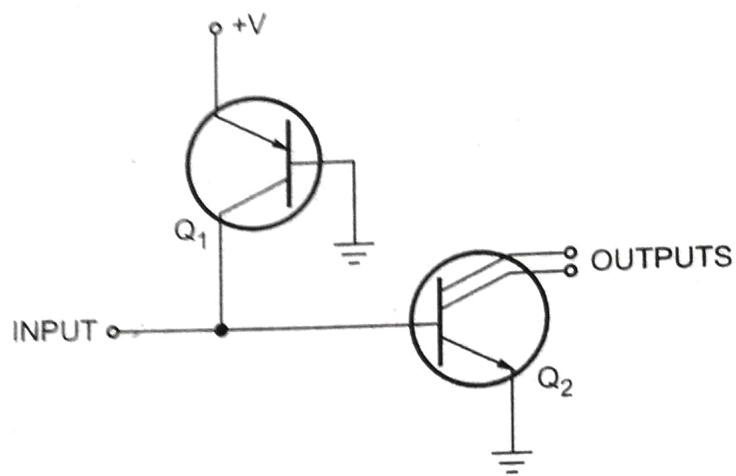


Fig. 7.48 (c) An actual I²L inverter having two output collectors and collector resistor

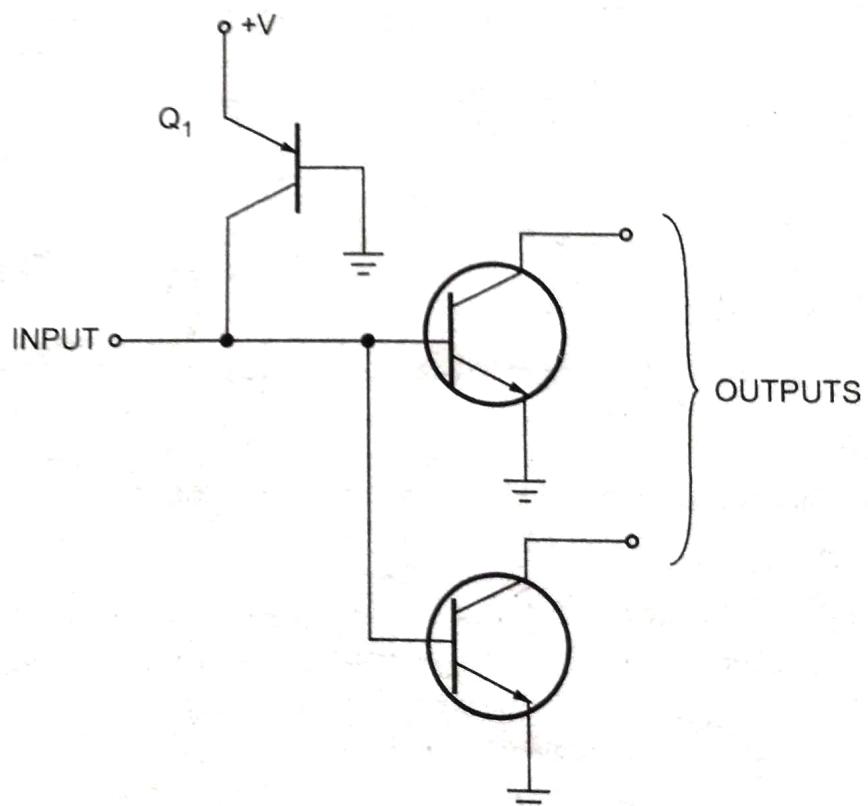


Fig. 7.48 (d) Two-transistor equivalent of the output transistor

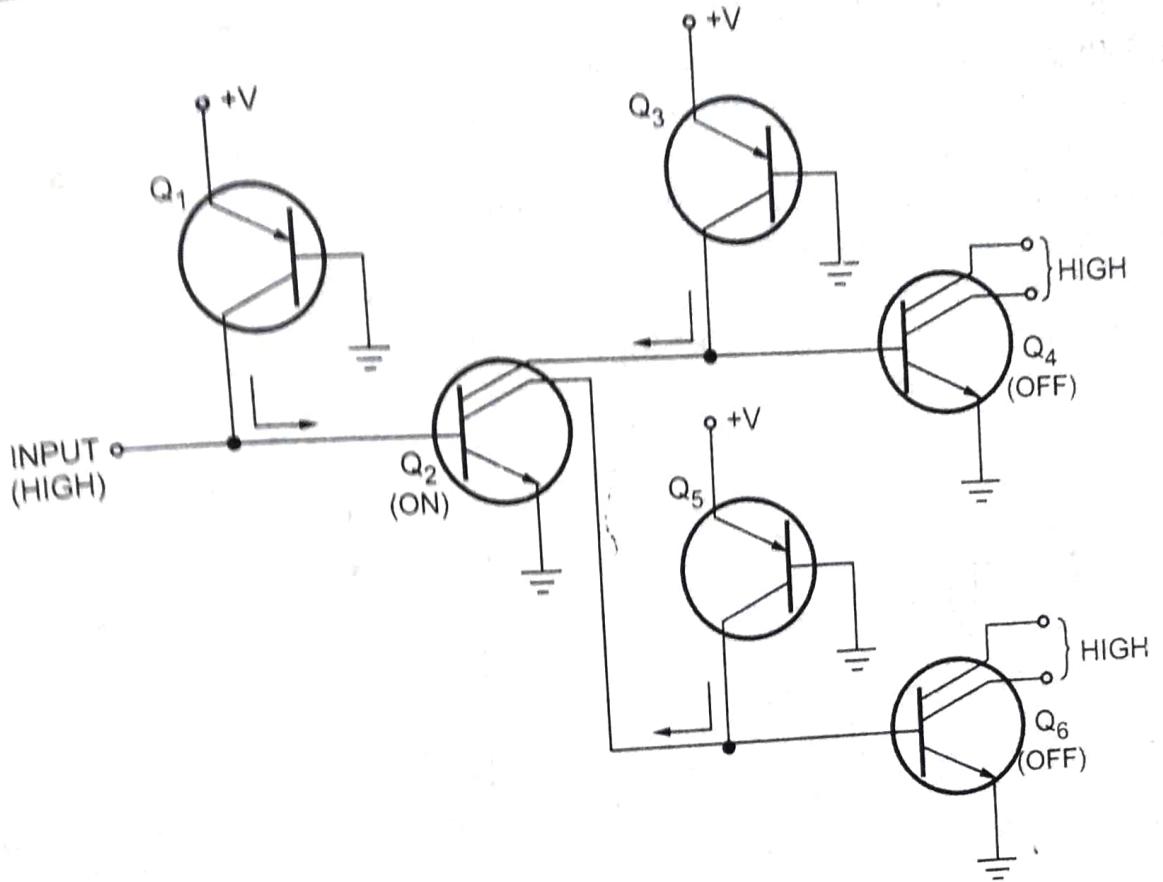


Fig. 7.48 (e)

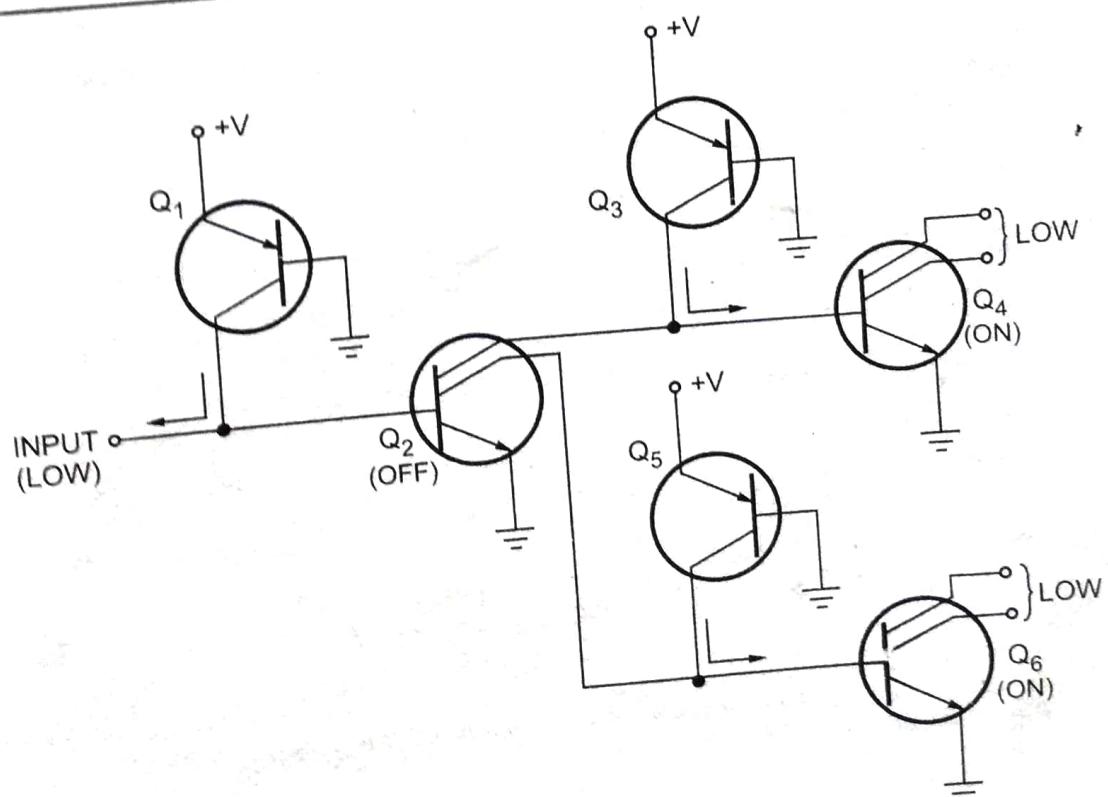
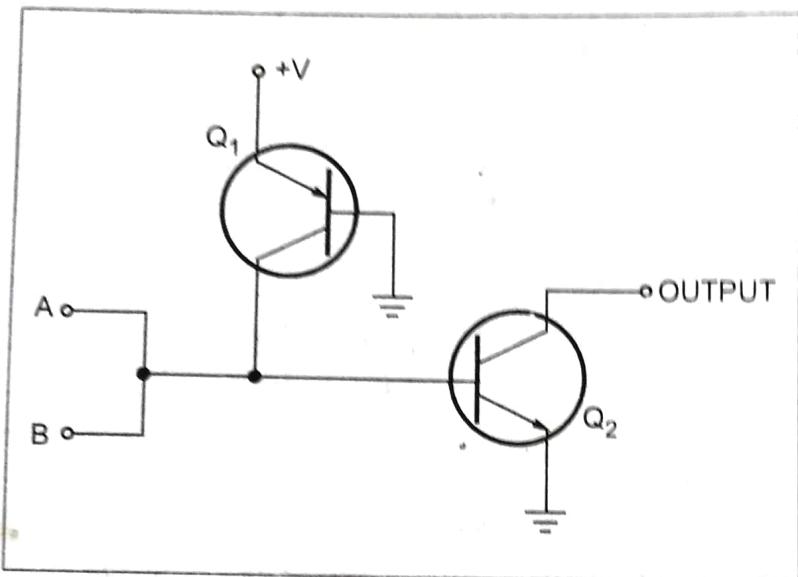


Fig. 7.48 (f) One I^2L inverter driving two others

7.13.2 I²L NAND and NOR Gates

Fig. 7.49 (a) and b) shows I²L NAND and NOR gates, respectively. The NAND gate is simply an inverter with inputs connected directly together at the inverter input. When either or both inputs are low, input(s) sink current and Q₂ is OFF. When both inputs are high, Q₂ is turned ON, making the output low. The NOR gate is simply two inverters with their outputs connected together. When either or both inputs are high, the corresponding output transistor is on (low), and the output is a current sink. When both inputs are low, both output transistors are off, so the output is high.



(a) I²L NAND gate

A	B	Q ₂	Output = AB
0	0	OFF	1
0	1	OFF	1
1	0	OFF	1
1	1	ON	0

0 = current sink (ON transistor)

I = OFF transistor

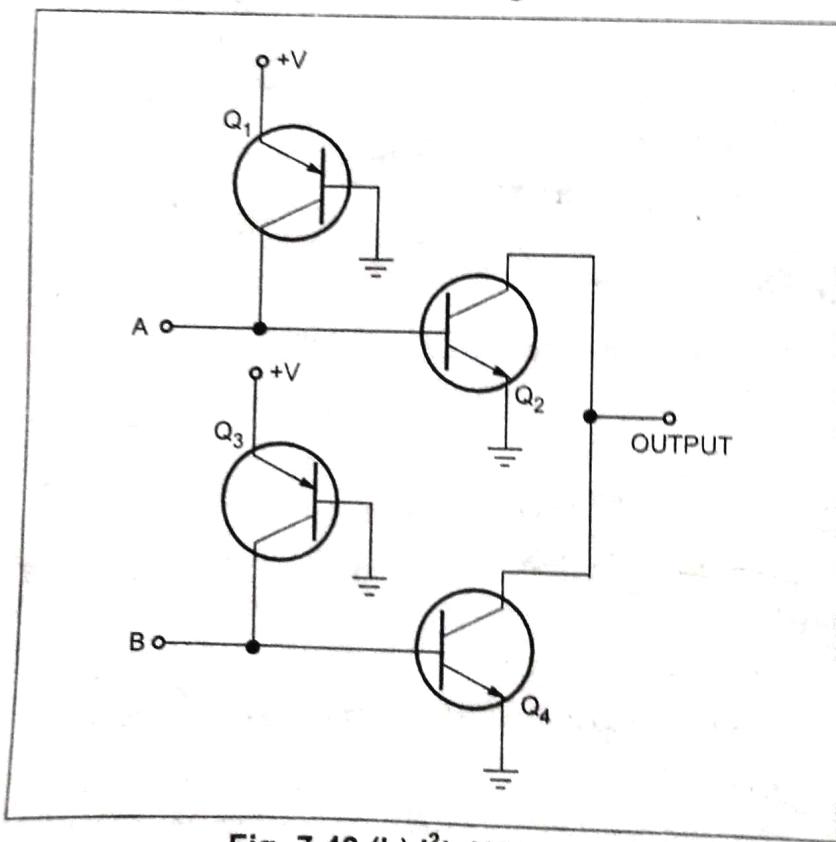


Fig. 7.49 (b) I²L NOR gate

A	B	Q ₂	Q ₄	Output = A + B
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	0

0 = current sink (ON transistor)

I = OFF transistor