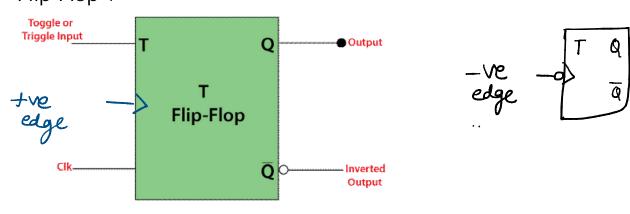
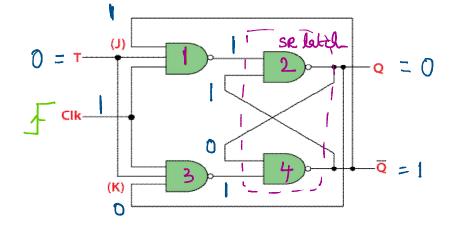
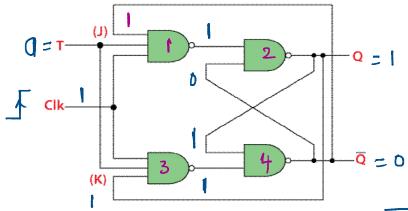
In T flip flop, "T" defines the term "Toggle". In SR Flip Flop, we provide only a single input called "Toggle" or "Trigger" input to avoid an intermediate state occurrence. Now, this flip-flop work as a Toggle switch. The next output state is changed with the complement of the present state output. This process is known as "Toggling". We can construct the "T Flip Flop" by making changes in the "JK Flip Flop". The "T Flip Flop" has only one input, which is constructed by connecting the input of JK flip flop. This single input is called T. In simple words, we can construct the "T Flip Flop" by converting a "JK Flip Flop". Sometimes the "T Flip Flop" is referred to as single input "JK Flip Flop".



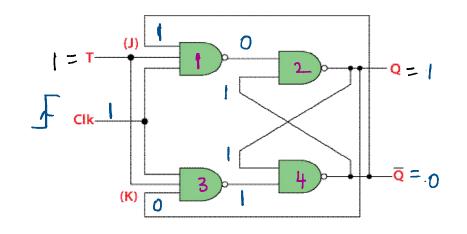


clock	T	Q	a(+1)
子	0	0	0

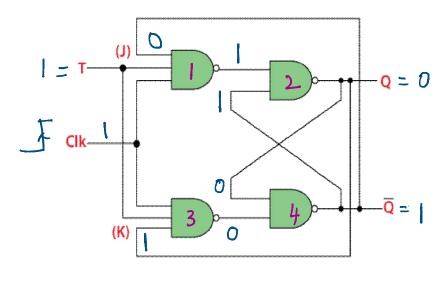


clock	Т	a	QUH)
子	0	0	l

doch	T	Q	alt+1)	8telte	
	0	0	0 %	Noche	1000
王	0	1	17	NOCK	rye

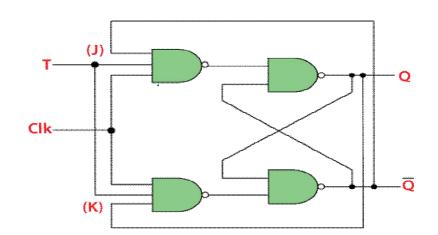


clock	T	Q	alty)
子	1	0	!



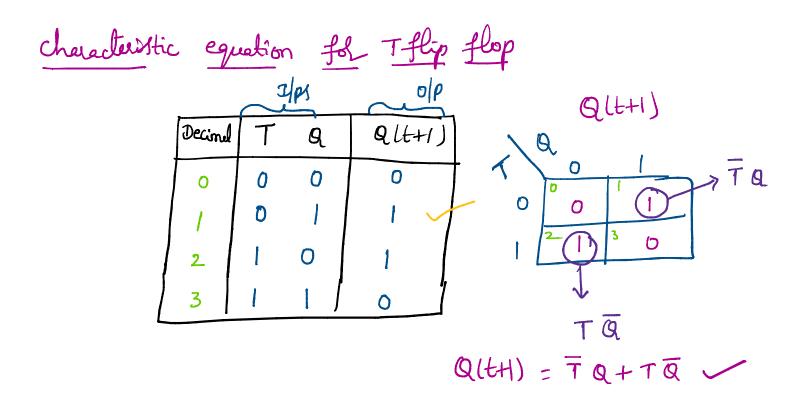
clock	Т	Q	QUH)
于	1	1	٥

clou	T	Q	QLLH)	8lete
F	I	0	ا کہ	Toggle
<u> </u>	1	1	ال	. The

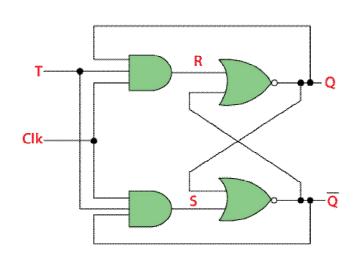


Clock	T	O.	Q(H)
丕	0	0	O ? No 1 J change
不	0	l	1 Jange
土	1	٥	1 /
廴	1	1	o J Tigg

T	alt+1)
O	Q
1	ā

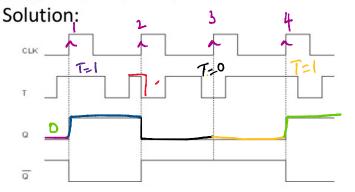


Let
$$W$$
: take $T=0$, $Q=1$, determine nent stelle $Q(t+1)$
 $Q(t+1) = \overline{T}Q + \overline{T}Q$
 $Q(t+1) = 1$
 $Q(t+1) = 1$



FUNCTION OF SEQUENTIAL LOGIC

Toggle flip-flop: output waveforms



1st clock $T=1, Q=0 \Rightarrow Q(t+1)=1$ 2nd clock $T=1, Q=1 \Rightarrow Q(t+1)=0$ 3rd clock $T=0, Q=0 \Rightarrow Q(t+1)=0$ 4th clock T=1, Q=0, Q(t+1)=0