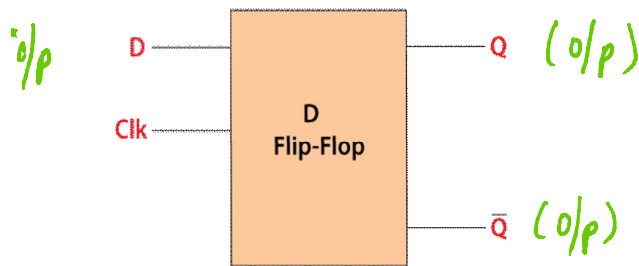


D flipflop

Block Diagram

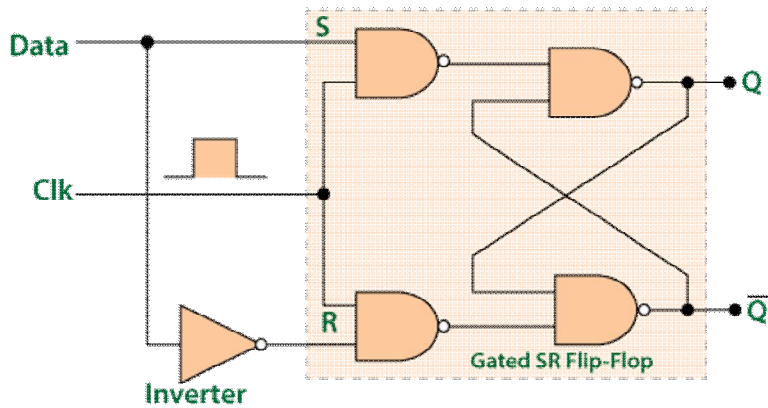


In D flip flop, the single input "D" is referred to as the "**Data**" **input**. When the data input is set to 1, the flip flop would be set, and when it is set to 0, the flip flop would change and become reset. However, this would be pointless since the output of the flip flop would always change on every pulse applied to this data input.

The "**CLOCK**" input is used to avoid this for isolating the data input from the flip flop's latching circuitry. When the clock input is set to true, the D input condition is only copied to the output Q. This forms the basis of another sequential device referred to as **D Flip Flop**.

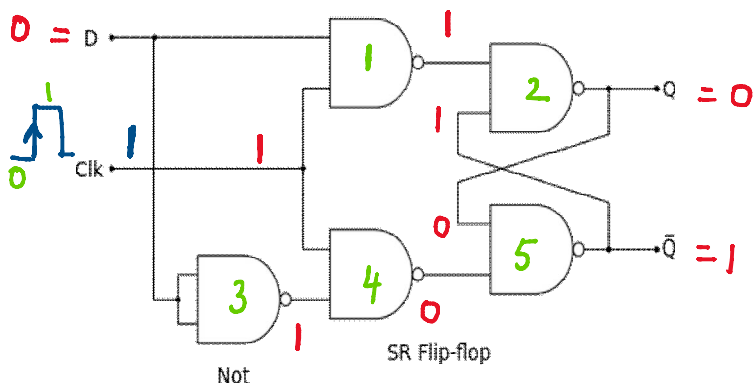
When the clock input is set to 1, the "set" and "reset" inputs of the flip-flop are both set to 1. So it will not change the state and store the data present on its output before the clock transition occurred. In simple words, the output is "latched" at either 0 or 1.

Circuit Diagram

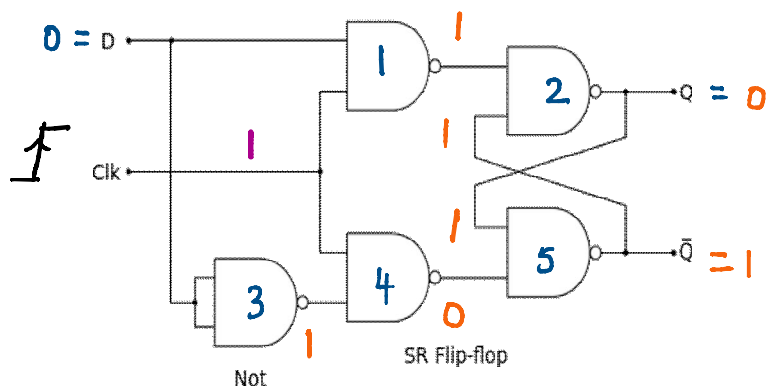


D flip flop (+ve edge triggering)

$A \rightarrow \text{D} \rightarrow \bar{A} \approx \text{D} \rightarrow \bar{A}$



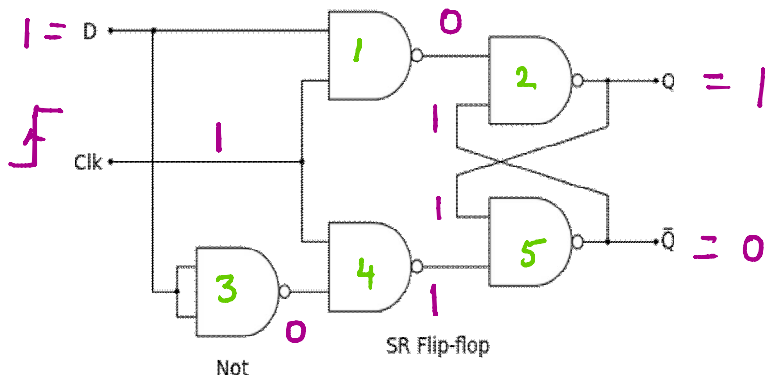
clock	D	Q	Q(t+1)
\uparrow	0	0	0



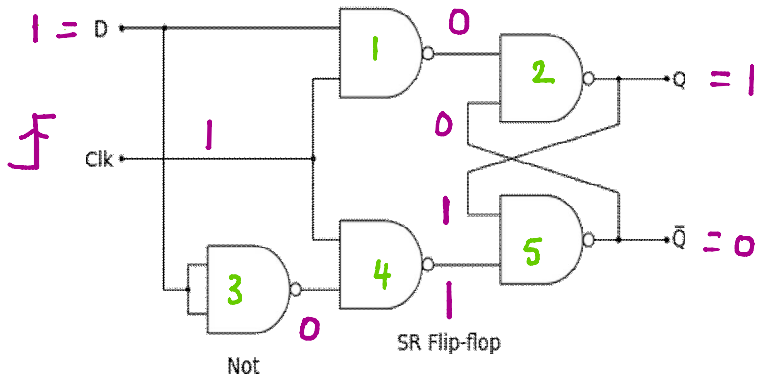
clock	D	Q	Q(t+1)
\uparrow	0	1	0

clock	D	Q	Q(t+1)
\uparrow	0	0	0
\uparrow	0	1	0

$\left. \begin{matrix} 0 \\ 0 \end{matrix} \right\} D=0$



clock	D	Q	Q(t+1)
\uparrow	1	0	1

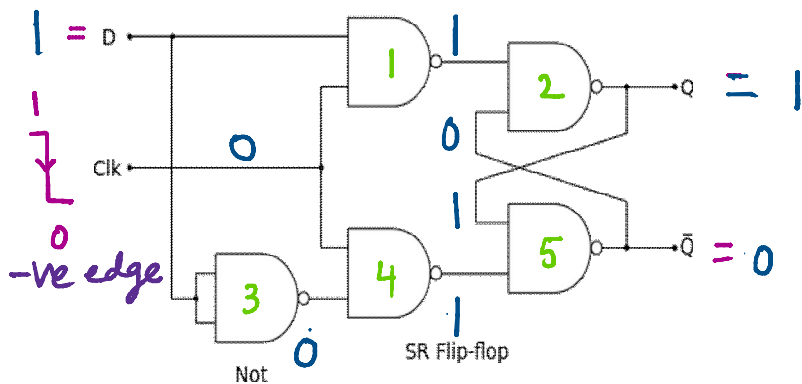


clock	D	Q	Q(t+1)
\uparrow	1	1	1

clock	D	Q	Q(t+1)
\uparrow	1	0	1
\uparrow	1	1	1

$\rightarrow D=1$

+ve edge triggered D flip flop

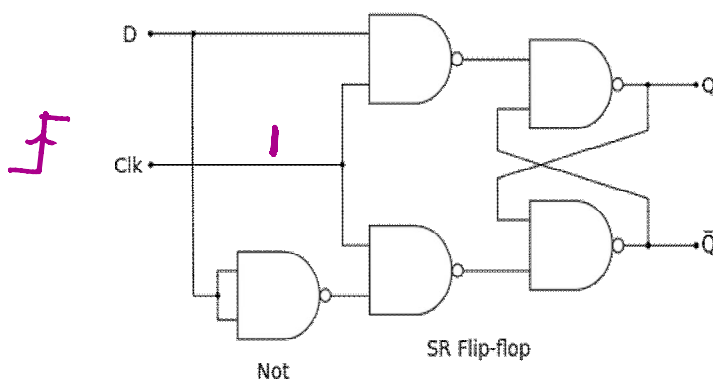


Clock	D	Q	Q(t+1)	State
\downarrow 0	0	0	0	No change
\downarrow 0	0	1	1	
0	1	0	0	No change
0	1	1	1	

for +ve edge triggered flip flop. If you apply -ve edge triggering then flip flop will always get no change state



+ve edge triggered D flip flop



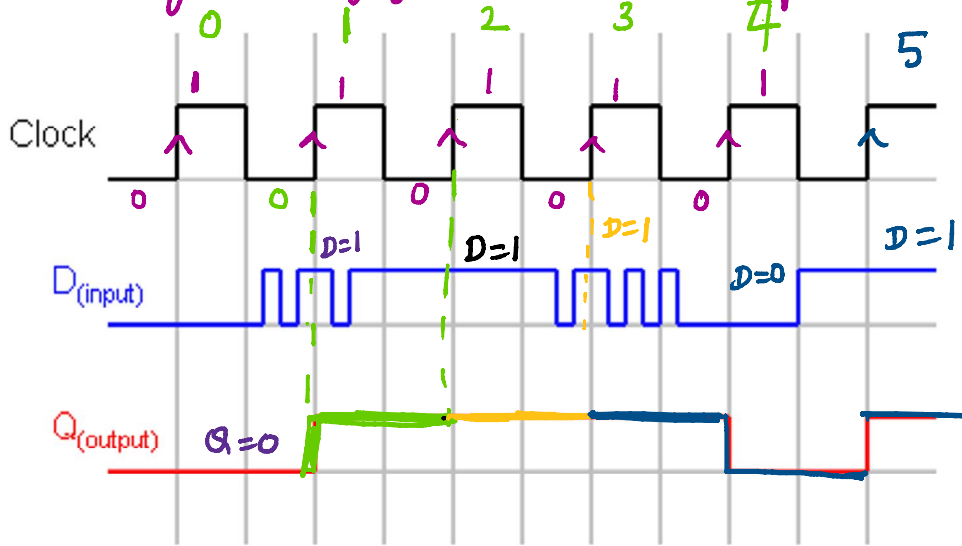
-ve

Clock	D	Q	Q(t+1)	State
0	x	x	No change state	
1	0	0	0	D=0
1	0	1	0	
1	1	0	1	D=1
1	1	1	1	

D	Q(t+1)
0	0
1	1

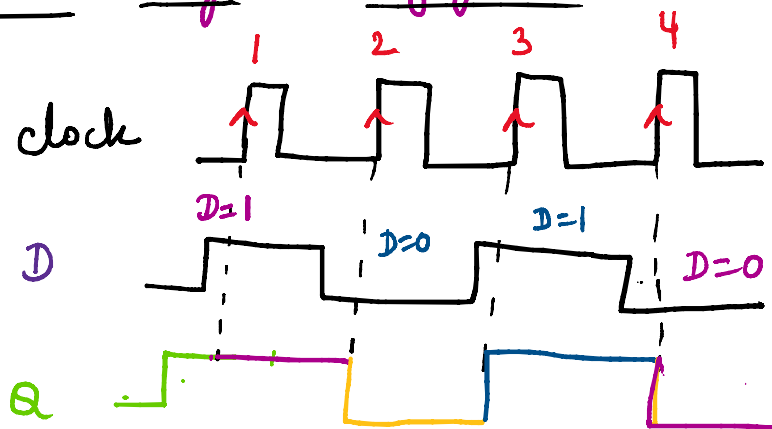
$$Q(t+1) = D$$

+ve edge triggered D flip flop



$$D=1 \Rightarrow Q(t+1)=1$$

+ve edge triggered D flip flop



$$D=1, Q=1$$

$$\text{Then } Q(t+1)=1$$

2nd clock

$$D=0, Q=1$$

$$Q(t+1)=0$$

3rd clock

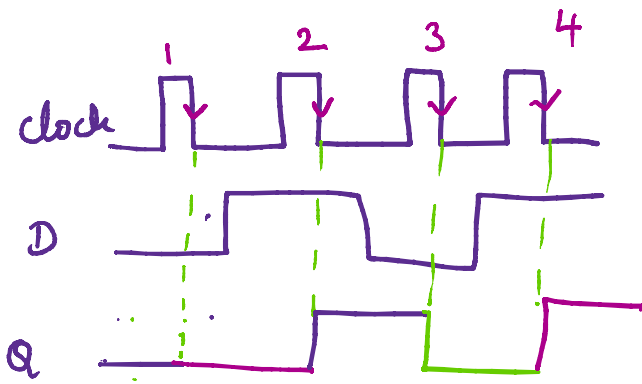
$$D=1, Q=0, Q(t+1)=1$$

4th clock

$$D=0, Q=1, Q(t+1)=0$$

$$D=0 \quad Q=1 \quad Q(t+1)=0$$

-ve edge triggered . D flip flop



$$1^{st} \text{ clock} \rightarrow D=0, Q=0, Q(t+1)=0$$

$$2^{nd} \text{ clock} \rightarrow D=1, Q=0, Q(t+1)=1$$

$$3^{rd} \text{ clock} \rightarrow D=0, Q=1, Q(t+1)=0$$

$$4^{th} \text{ clock} \rightarrow D=1, Q=0, Q(t+1)=1$$