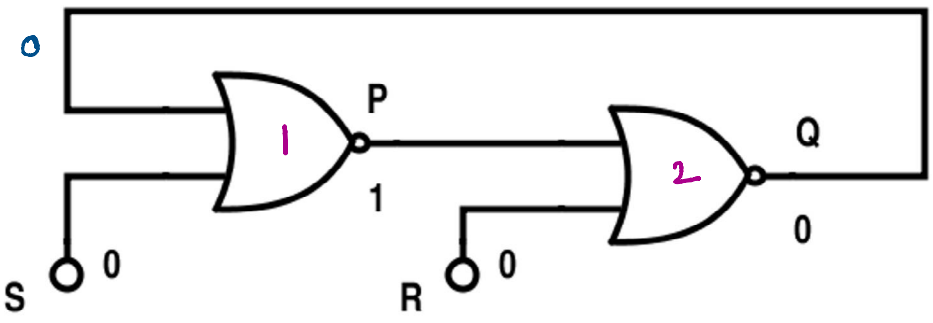
Introduction to Latches

- Latch is an electronic logic circuit with two stable states i.e. it is a bistable multivibrator.
- Latch has a feedback path to retain the information. Hence a latch can be a memory device.
- Latch can store one bit of information as long as the device is powered on.
- When enable is asserted, latch immediately changes the stored information when the input is changed i.e. they are level triggered devices. It continuously samples the inputs when the enable signal is on

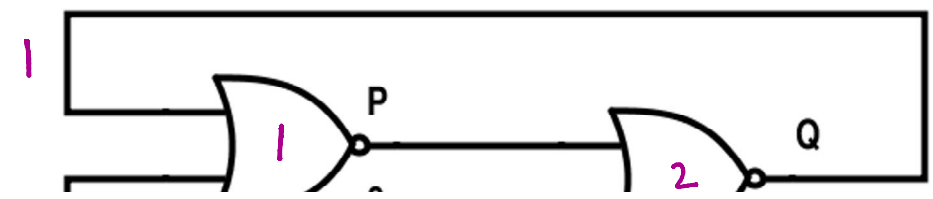
SR LATCH

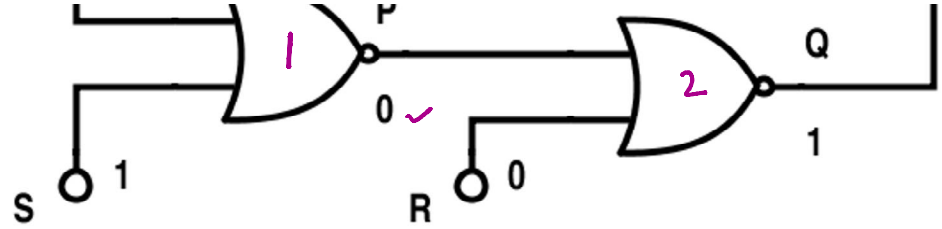
We can use static gates as basic building blocks in order to construct a simple latch and it can be constructed with two NOR gates by introducing feedback to a NOR gate circuit.

A simple NOR gate logic with feedback is shown below.



Here, both the inputs S and R are 0 (S = R = 0). The output of first NOR gate is P = 1. This is fed to the second NOR gate along with R = 0. Hence the output of the second gate is Q = 0. The circuit is said to be in stable state with P = 1 and Q = 0. If we make S = 1, then P = 0. This will make Q =1 as shown below.

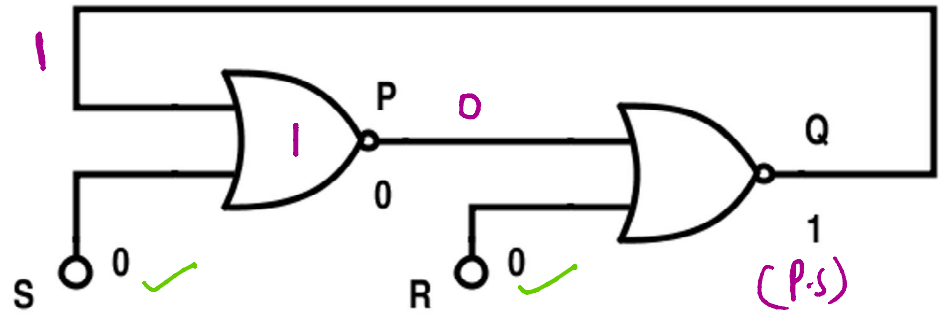




This is also a stable state. If S is made 0, there is no change as Q = 1 is fed back to first NOR and P still remains 0. It is shown in the below figure.

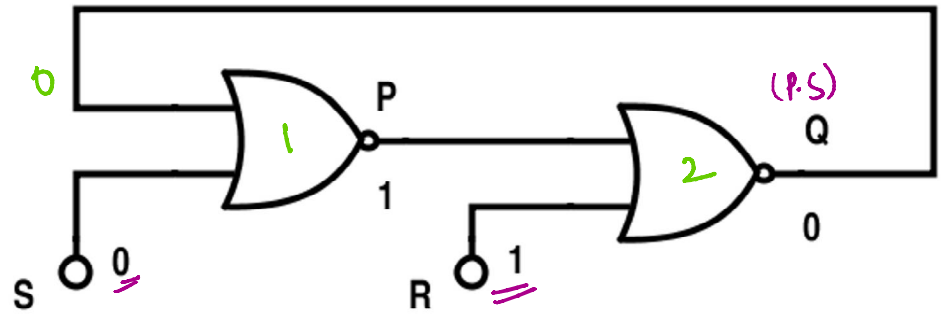
S	R	P.S Q_t	N.S Q_{t+1}
0	0	1	1

Q_{t+1} (N.S) = 1

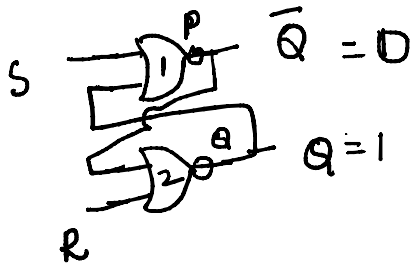


If R is made 1, then Q becomes 0 which will change P back to 1.

S	R	P.S Q_t	N.S Q_{t+1}
0	1	0	0

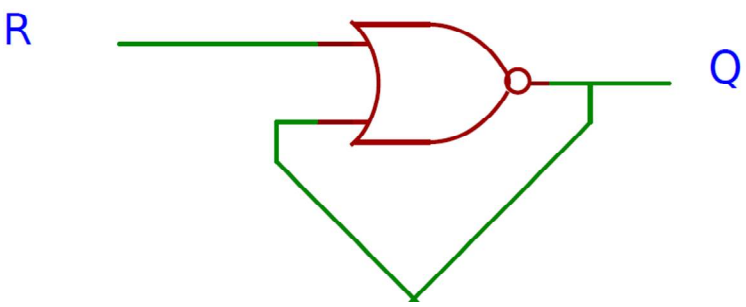


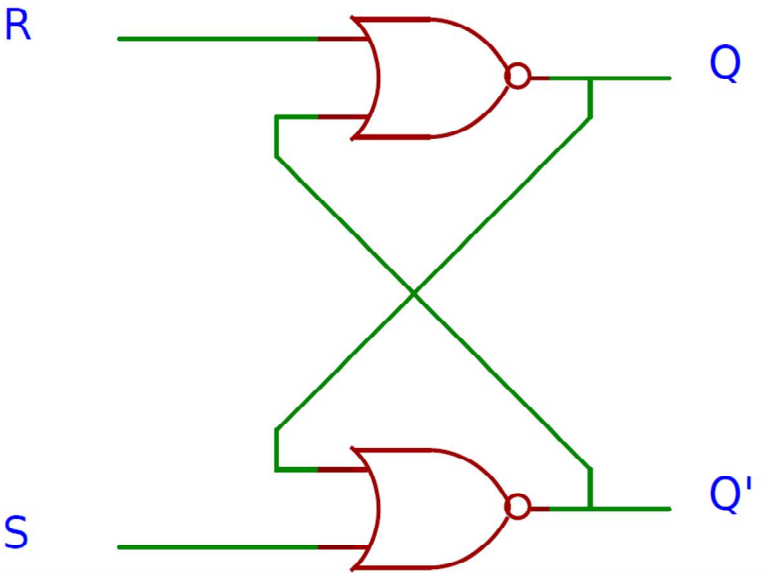
If R is made 0, then there is no change and we arrive at where we started.



As the output depends not only on present inputs but also on past sequence of inputs, the circuit is said to have memory. If the input condition S = R = 1 is not allowed, the stable state outputs are always complementary. When both S and R are equal to 1, P = 0 and Q = 0 which contradicts the complementary condition. Hence the input condition S = R = 1 is said to be not allowed. The latch circuit is always drawn as a cross coupled form to emphasize the symmetry between the gates.

R = Reset
S = set
Q = present state
$Q_{(t+1)}$ = Next state





Q = present state
$Q_{(t+1)}$ = Next state

In this circuit, when S = 1, it 'sets' the output Q to 1 and when the input R = 1, it 'resets' the output Q to 0. With the restriction of S = R = 1, this circuit is called a Set – Reset Latch (SR Latch).