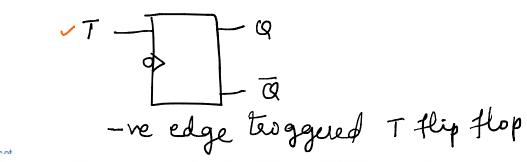
synchronous inputs & Asynchronous inputs

T

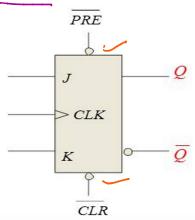
The normal data **inputs** to a **flip flop** (D, S and R, or J and K) are referred to as **synchronous inputs** because they have an effect on the outputs (Q and not-Q) only in step, or in sync, with the clock signal transitions.

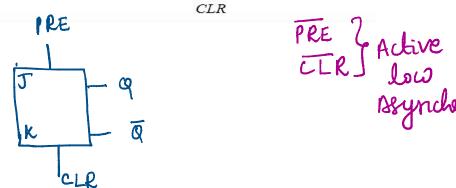


Synchronous inputs (for example the D or J-K inputs) affect the output on the triggering edge of the clock. Most flip-flops also have other inputs that are asynchronous, meaning they affect the output independent of the clock.

Two such inputs are normally labeled *PRE* (preset) and *CLR* (clear). These inputs are usually active LOW, as shown here.

Other common names for these pins are *SET* and *RESET*.





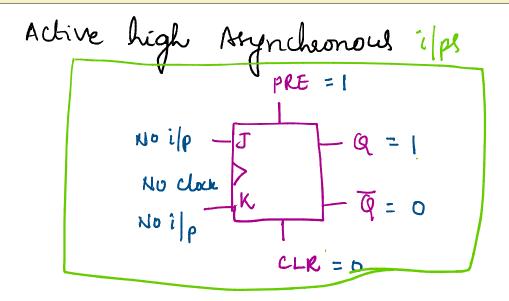
PRE, CLR -> Active high Asynchemous ilp

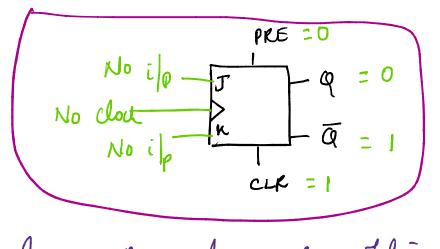
active high means, we need to give logic 11 at alyncheonous to

active low means, we need to give logic 'o' at alyncheonous Up.

Flip-flops with Asynchronous Preset and Clear

- It is often necessary to initialize a flip-flop to a known state before the circuit operation starts.
 - Preset (sets Q = 1) and Clear (sets Q = 0).
 - These are asynchronous operations, and can be easily implemented by using additional inputs on the cross-coupled gates.
 - The term "asynchronous" means that it does not depend on the clock.





Active low seynchronous flip flop

PRE = 0

C perset is activated)

No i/p J Q = 1

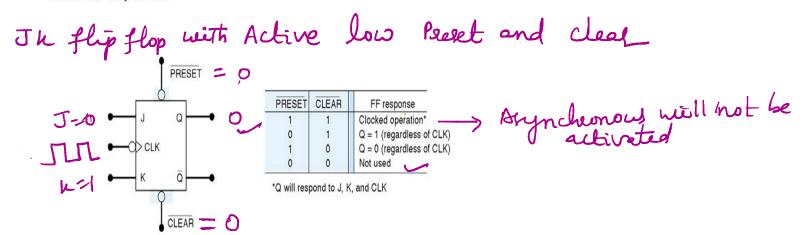
No clock

No i/p

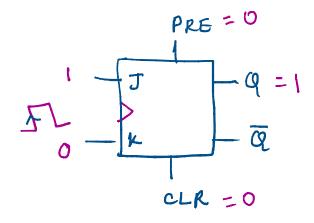
Cio = 1

Peut means set le Q=1

Asynchronous inputs (override inputs) operate independently of the synchronous inputs and clock and can be used to set the FF to 1/0 states at any time.



logic diagram of baric Jk flip flop with Active high Peelet and clear



PRE	CLR	FF segme
0	0	clocked operation
O	1	Q = 0
1	0	Q = 1
l	1	Not used