

UNIT

I Diode and Applications

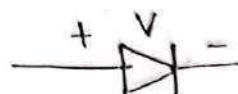
⇒ Static and Dynamic Resistance.

→ A diode has two types of resistors.

(i) Static or DC resistance (ii) Dynamic or AC resistance.

(i) Static resistance:- It is defined as the ratio of the voltage across the diode to the current passing through the diode.

Mathematically, $R = \frac{V}{I}$



where V is the voltage across the diode, I is current passing through the diode.

(ii) Dynamic resistance:- It is defined as reciprocal of the slope of V-I characteristics of diode.

Mathematically, Slope = $\frac{\partial I}{\partial V}$ $r = \frac{1}{\text{slope}} = \frac{\partial V}{\partial I}$.

The current passing through diode,

$$I = I_0 (e^{\frac{V}{nV_T}} - 1).$$

$$I = I_0 e^{\frac{V}{nV_T}} - I_0 \quad \text{--- (1)}$$

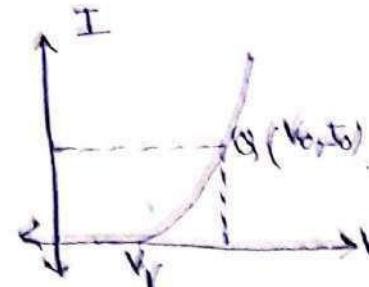
$$\frac{\partial I}{\partial V} = I_0 \cdot e^{\frac{V}{nV_T}} \cdot \frac{1}{nV_T}.$$

$$\frac{\partial I}{\partial V} = \frac{I + I_0}{nV_T}.$$

In forward bias $I \gg I_0$, $\frac{\partial I}{\partial V} = \frac{I}{nV_T}$.

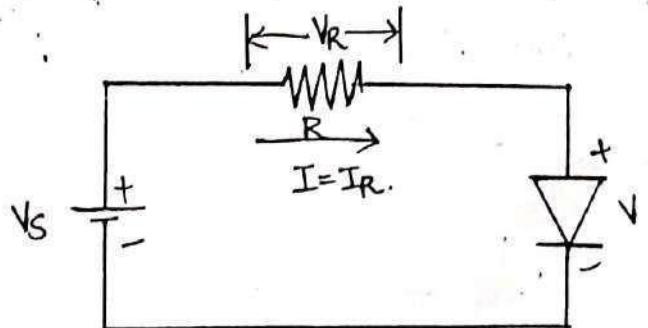
$$r = \frac{\partial V}{\partial I}$$

$$r \approx \frac{nV_T}{I}$$



- ② → If voltage across diode is V_D and current passing through diode is I_D , then (V_D, I_D) is the operating point of diode on VI characteristics.
- If diode is a non-linear element because the current varies non-linearly with respect to voltage.
- If diode voltage is varied by a small amount i.e., a few milli volts then diode current varies almost linearly with voltage. This is called a small signal operation of diode.
- In small signal operation diode behaves as linear resistor.
- The resistor offered by the diode in small signal operation is known as dynamic resistance or AC resistance or small signal resistance.

⇒ Diode equivalent circuit.



Simple diode circuit.

- The PN junction diode is considered as a circuit element. The basic diode circuit shown above consists of a dc voltage V_s which is supplied across a resistor and a diode. In order to find the instantaneous

⑤ - diode voltage V and current I , the circuit can be analysed when the instantaneous source voltage is V_s . From KVL, the instantaneous diode voltage is

$$V_s = IR + V \quad \text{--- (1)}$$

which can be expressed as $I = \frac{V_s}{R} - \frac{V}{R}$.

The ideal diode current equation relating the diode voltage V_D and current I_D is

$$I = I_0 [e^{(V_D/V_T)} - 1]. \quad \text{--- (2)}$$

where I_0 diode sat. current at room temp. η is a constant (1 for Ge and 2 for Si) and V_T is thermal voltage i.e., $V_T = \frac{T}{11,600}$ in which T is the temperature of the diode junction (300K) or $V_T = 26 \text{ mV}$ at room temp.

Sub (2) in (1)

$$V_s = I_0 R [e^{(V_D/V_T)} - 1] + V.$$

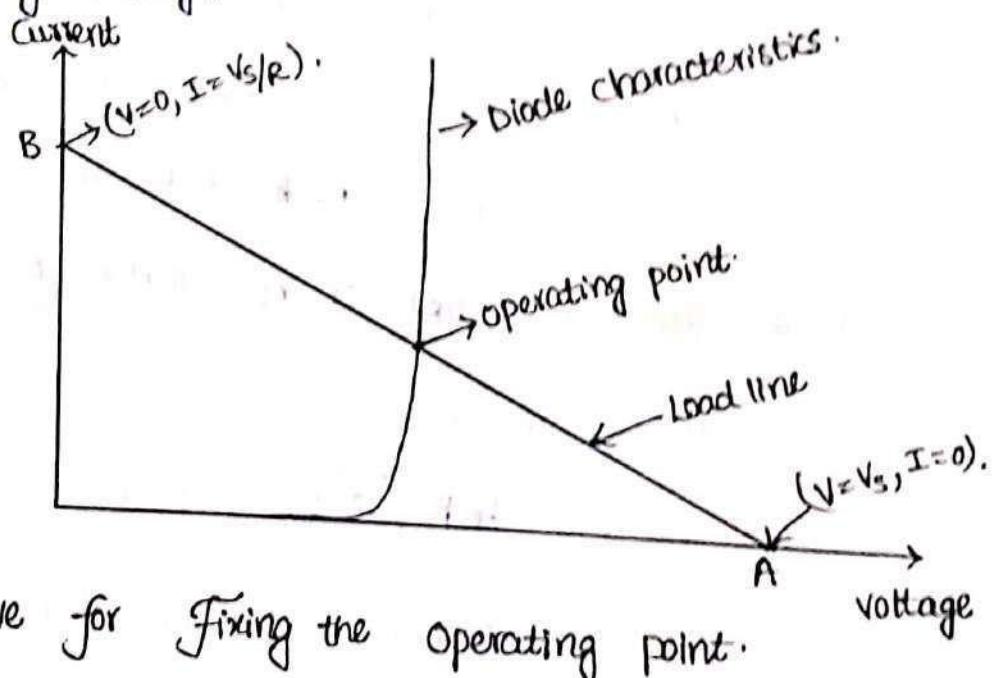
As these equations contains both linear and exponential terms, it is difficult to solve by hand.

Load Line Analysis:

In the second method to draw the load line, I is determined when the device is short-circuited and V is determined when the device is open-circuited. So that the point B ($V=0, I=V_s/R$)

\therefore on y-axis x coordinate is zero.
 $V_s = IR + 0$.

④ and A ($V=V_S, I=0$) lies somewhere on the y-axis and x-axis respectively of the diode characteristic curve as shown in figure. Thus a straight line drawn connecting the points A and B is called load line. This load line intersects the diode characteristics at some point which is chosen as operating point for the device. The operating point provides the diode voltage V , appearing across the diode and the current I , flowing through the diode.



Loadline Curve for Fixing the Operating point.

* Diode Capacitances *

→ Diode has two types of capacitances.

- 1) → Transition/Junction/Depletion/Space charge capacitance.
- 2) → Diffusion Capacitance.

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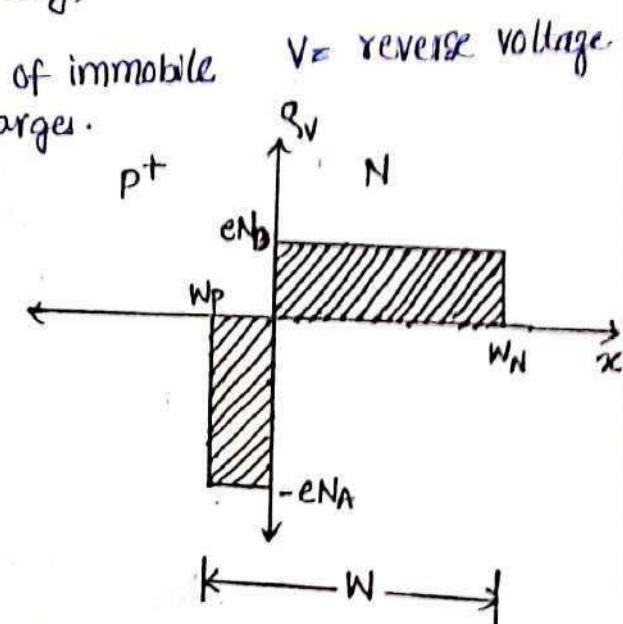
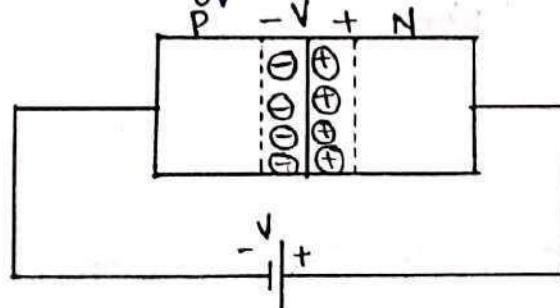
1) Transition Capacitance

It appears when diode is in reverse bias.

When the reverse voltage is increased depletion width increases and thereby the amount of immobile charges present in depletion region also increases i.e., diode behaves as capacitor.

- The rate of change of immobile charge in the depletion region wrt the reverse voltage is known as transition capacitance. Mathematically,

$$C_T = \frac{\partial Q}{\partial V} \quad \text{where } Q = \text{Amount of immobile charges.}$$



P⁺N junction:-

$$N_A \gg N_D, \quad W_p \ll W_N$$

$$W = W_N + W_p$$

$$W \approx W_N$$

$$C_T = \frac{\partial Q}{\partial V} = \frac{\partial Q}{\partial W} \times \frac{\partial W}{\partial V} \quad \text{--- (1)}$$

$$Q = eN_D \times A \times W_N$$

$$Q \approx A e N_D W$$

$$\begin{aligned} \therefore Q_V &= \frac{Q}{V} \\ Q &= Q_V \times V \\ Q &= eN_D \times V. \end{aligned}$$

$$\boxed{\frac{\partial Q}{\partial W} = A e N_D}$$

⑥ From poisson's Equation

$$\frac{\partial^2 V}{\partial x^2} = -\frac{P_V}{\epsilon} \Rightarrow \int \frac{\partial^2 V}{\partial x^2} = \int -\frac{eN_D}{\epsilon}$$

$$\frac{\partial V}{\partial x} = -\frac{eN_D x}{\epsilon} + C_1, \text{ At } x=W_N, \frac{\partial V}{\partial x} = E=0.$$

$$0 = -\frac{eN_D x}{\epsilon} + C_1 \Rightarrow C_1 = \frac{eN_D W_N}{\epsilon}$$

$$\int \frac{\partial V}{\partial x} = \int -\frac{eN_D x}{\epsilon} + \int \frac{eN_D W_N}{\epsilon}$$

$$V = -\frac{eN_D x^2}{2\epsilon} + \frac{eN_D W_N x}{\epsilon} + C_2$$

$C_2=0$, At $x=0, V=0$

$$\text{Now, } V = -\frac{eN_D x^2}{2\epsilon} + \frac{eN_D W_N x}{\epsilon}.$$

At N , $V=V_N$, $x=W_N$.

$$V_N = -\frac{eN_D W_N^2}{2\epsilon} + \frac{eN_D W_N^2}{\epsilon} = \frac{eN_D W_N^2}{2\epsilon}$$

$$V_N = \frac{eN_D W_N^2}{2\epsilon}$$

$$\text{I.Iy } V_P = \frac{-eN_A W_P^2}{2\epsilon}$$

$$V_B = V_N - V_P = \frac{eN_D W_N^2}{2\epsilon} + \frac{eN_A W_P^2}{2\epsilon}$$

Where,

E = permittivity of
S.C

$$V_B = \frac{e}{2\epsilon} [N_D \cdot W_N \cdot W_N + N_A \cdot W_P \cdot W_P] \quad A = \text{area of cross section}$$

W = width of dept reg.

$$V = \frac{e}{2\epsilon} N_D W_N [W_N + W_P]$$

$$V = \frac{e}{2\epsilon} N_D W^2 \quad | \because W_N \approx W$$

$$\frac{\partial V}{\partial W} = \frac{e}{\epsilon} N_D \cdot W, \quad \frac{\partial W}{\partial V} = \frac{\epsilon}{e N_D \cdot W}$$

$$C_T = A e N_D \times \frac{\epsilon}{e N_D \cdot W}$$

$$C_T = \frac{e A}{W}$$

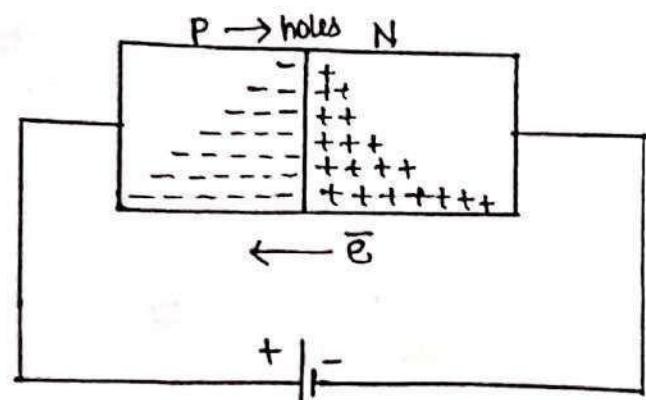
- * Transition capacitance decreases with increases in the applied reverse voltage. Hence the diode in reverse bias can be used as voltage dependent capacitor.
- * If a diode is used as a voltage dependent Capacitor then it is called as varactor diode (or) variable Capacitor^{diode}.

2) Diffusion Capacitance.

→ It occurs when the diode is operated in forward bias. When forward bias is occurred the +ve charge i.e., holes injected into N-side and -ve charge i.e., free electrons inject into P-side. This injected carriers maximum near the junction and gradually decreases due to the recombination.

→ When forward voltage is increased the flow of holes from P to N and flow of es from N to P increases. Hence the injected charge carrier also increases.

→ The rate of change of injected charge wrt forward voltage is called diffusion capacitance.



$$C_D = \frac{\partial Q}{\partial V}, \text{ where } Q = \text{injected charge}$$

V = forward voltage.

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Consider a p^+N junction in F.B. in which current is dominantly due to holes.

The differential amount of injected charge on N-side is

$$\partial Q = \text{Injected hole density} \times e \times A \times dx \quad \text{differential volume.}$$

$$\partial Q = eA \times \Delta P \cdot e^{-x/L_p} \times dx$$

Total charge is integration of above equation over length of n region

$$Q = eA \times \int_{x=0}^{x=x_N} \Delta P \cdot e^{-x/L_p} dx \Rightarrow eA \times \Delta P \left[e^{-x/L_p} \right]_{x=0}^{x=x_N} \times \frac{1}{(1/L_p)}.$$

$$Q = -eA \Delta P \cdot \left[e^{-x_N/L_p} - e^0 \right] \times L_p$$

$$\text{But } x_N \ggg L_p \Rightarrow e^{-x_N/L_p} \approx 0.$$

$$Q = -AeL_p \cdot \Delta P [0-1] = AeL_p \Delta P.$$

$$\text{Differentiate wrt } V = \frac{\partial Q}{\partial V} = AeL_p \frac{\partial}{\partial V}(\Delta P). \quad \text{--- (1)}$$

$$\text{WFT, } I \cong I_{pn}(0) = Ae \frac{D_p}{L_p} \times \Delta P.$$

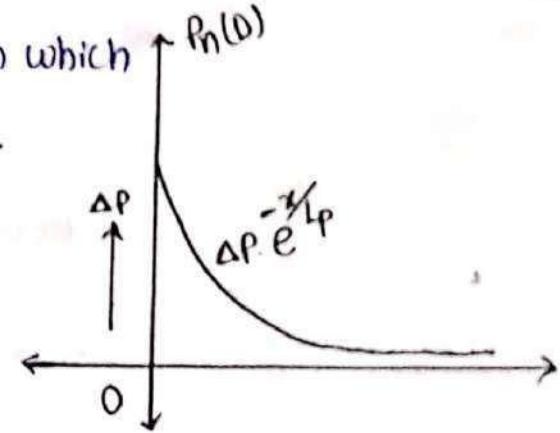
Diff wrt V.

$$\frac{\partial I}{\partial V} = \frac{AeD_p}{L_p} \frac{\partial}{\partial V}(\Delta P).$$

$$\Rightarrow \frac{\partial}{\partial V}(\Delta P) = \frac{L_p}{AeD_p} \cdot \frac{\partial I}{\partial V} \quad \text{--- (2)}$$

Sub (2) in (1)

$$\frac{\partial Q}{\partial V} = C_D = \frac{AeL_p}{AeD_p} \times \frac{L_p}{AeD_p} \cdot \frac{\partial I}{\partial V}$$



$$C_D = \frac{I_p^2}{D_p} \times \frac{\partial I}{\partial V}$$

$$C_D = T_p \times \frac{1}{V}$$

$$\therefore I_p = \sqrt{D_p \cdot T_p}$$

$$V = \frac{\partial V}{\partial I}$$

$T_p = \frac{I_p^2}{D_p}$ = Life time of holes. V = dynamic resistance.

$$C_D = \frac{T_p}{V I} = \frac{T_p \cdot I}{V \cdot I} = C_D$$

$\therefore C_D \propto$ forward current (I_f)

$$C_D \propto e^{V/I_f}$$

i.e., C_D increases exponentially

for PN Junction : $C_D = \frac{T_p}{V}$ with voltage (forward voltage).

NOTE:- For ordinary PN junction,

$$C_D = \frac{T_p}{V} + \frac{T_n}{V}$$

Diode switching times:

→ Diode in forward bias ≡ ON switch

→ Diode in reverse bias ≡ OFF switch

Switching speed of a diode depends upon forward and reverse recovery times

Forward recovery time: It is the time taken by a diode to change from OFF state to ON state

Reverse recovery time: It is the time taken by a diode to change from ON to OFF state

For a diode $t_{RRI} \gg t_{FRI}$.

t_{RRI} = Reverse recovery time

t_{FRI} = Forward recovery time

⑩ → Reverse recovery time is the sum of storage time and transition time.

Storage time (t_s): When diode is in ON condition, large amount of +ve charge is injected into N side in the form of holes and large amount of negative charge is injected into P side in the form of electrons.

- When applied voltage changes to reverse bias, injected holes move back to P-side and injected electrons move back to n-side. During this reverse movement of carriers, recombinations occur and injected charge gradually reduces to zero.
- The time taken by injected charge to become 0, is storage time.

Transition time (t_t): When injected charge becomes zero, the transition capacitance of diode will start charging upto applied reverse voltage (capacitance voltage cannot change abruptly, it takes time to charge.)

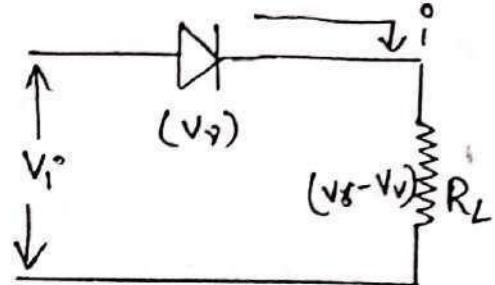
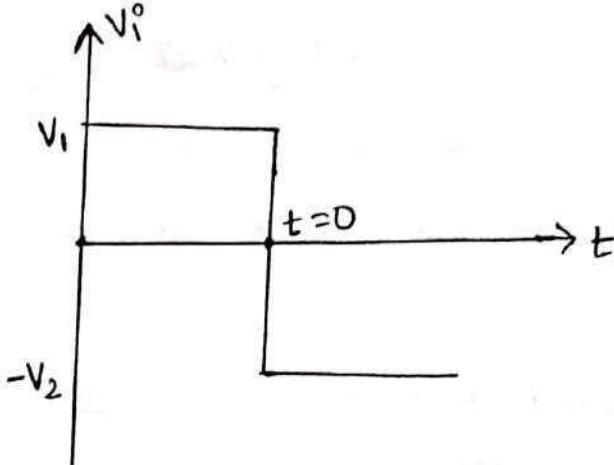
- The time taken by transition capacitance to charge upto applied reverse voltage is known as transition time.

$$t_{\text{RR}} = t_s + t_t$$

i.e., Reverse recovery time is large due to two events taking place

i.e., injected charge should be 0 &

C_T should charge upto the R.B volt

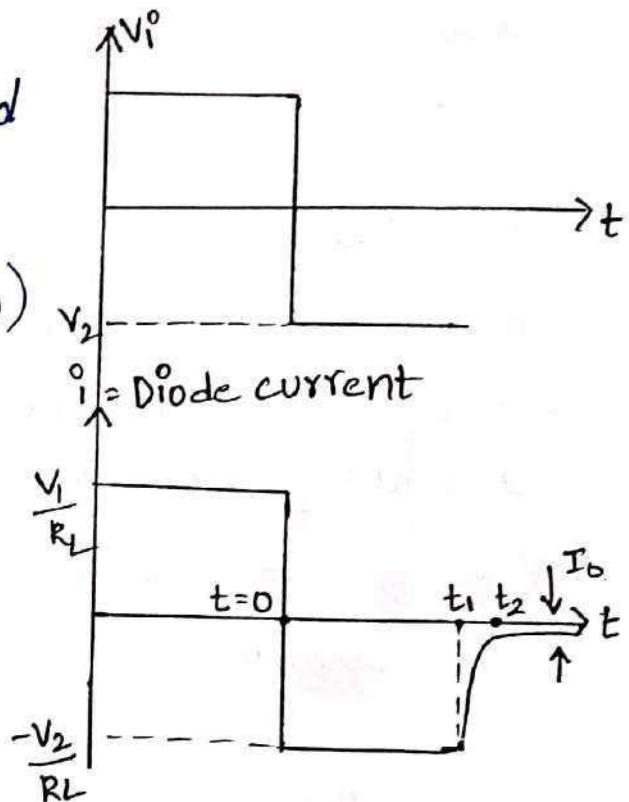


For $t < 0$: Diode is in forward bias (ON)

$$i = \frac{V_i - V_d}{R_L} \approx \frac{V_i}{R_L} \quad (\text{if } V_i \gg V_d)$$

At $t = 0$: V_o changes from $+V_1 + 0 - V_2$ i.e from F.B to R.B

At $t = 0$, current through the diode does not become 0, but current reverses its direction and a current equal to $\frac{V_2}{R_L}$ will flow



through the diode from N side to P-side due to reversal of movement of injected carriers.

At $t = 0$, when voltage changes abruptly (act as a s.c., and entire V_2 appears across R (diode acts as c))

This current flow continues till injected charge becomes 0 at $t = t_1$.

For $t > t_1$: The transition capacitance of diode starts charging & hence voltage across diode keeps increasing and current through diode keeps decreasing (capacitive action)

(12) Transition capacitance gets fully charged at $t=t_2$ and diode current is I_0 (reverse current that flows when diode is OFF) Diode is fully recovered when current becomes I_0 .

- To improve switching speed of a diode, reverse recovery time should be reduced by decreasing storage time.

Rectifiers

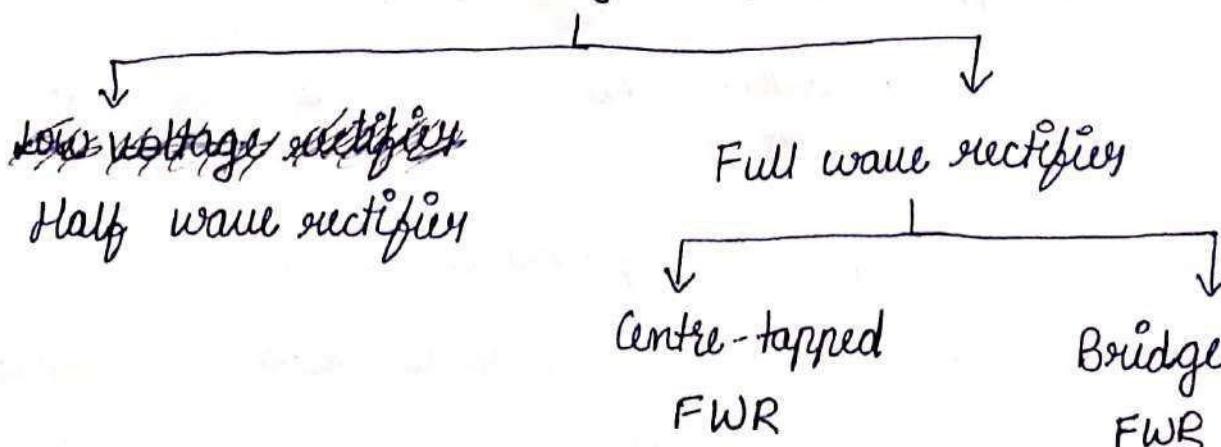
An electronic circuit which converts pure AC into pulsating DC (or) a circuit which converts bidirectional signal to unidirectional signal

It is of two types

- Low voltage rectifier (produces low DC output voltage of few V to few 10's of volt)
- High voltage rectifier (produces DC output voltage of 100's of volt)

- Low voltage rectifier consists of normal diodes whereas high voltage rectifier consists of power diodes & SCR

Low voltage rectifiers



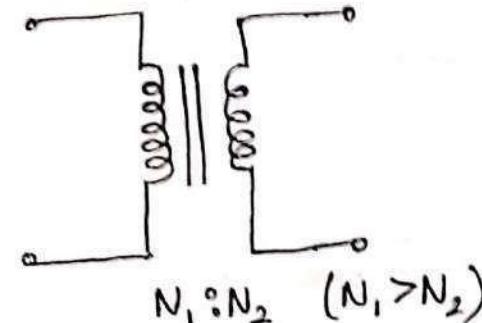
(13) Step down transformer \Rightarrow to convert 220V AC to smaller AC or downsize AC voltages according to requirement before rectifying

- In low voltage rectifiers stepdown transformer is used to reduce the strength of AC voltage. (less no. of winding in secondary than primary)

$$\frac{V_1}{V_2} = \frac{N_1}{N_2}$$

Turns ratio

Ex: 220V $\xrightarrow{10:1} \frac{220}{10} = 22V$



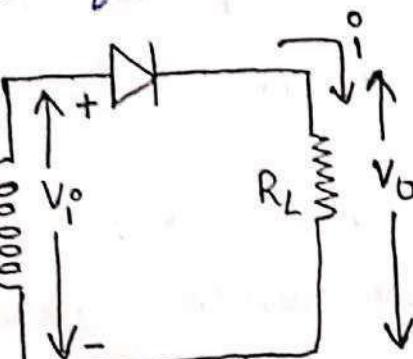
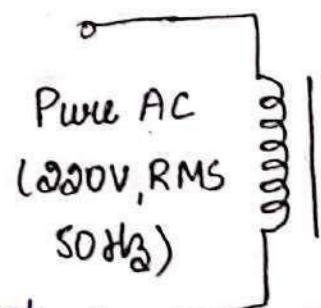
- Step down transformer is necessary to obtain low DC output voltage from rectifier

Half wave rectifier

220V : Line voltage

50Hz : Line frequency

or frequency of AC supply



V_1 : Pure AC voltage having smaller RMS value

$$V_1 = V_m \sin \omega_0 t \text{ or } V_m \sin \alpha \rightarrow \text{Mathematical representation of pure AC}$$

V_m = peak value, $\frac{V_m}{\sqrt{2}}$ = RMS value, $2V_m$ = peak to peak value
 $\omega_0 = 2\pi f_0$ = line frequency

$$f_0 = 50 \text{ Hz}, \quad \omega_0 = 2\pi \times 50 = 314 \text{ rad/sec}$$

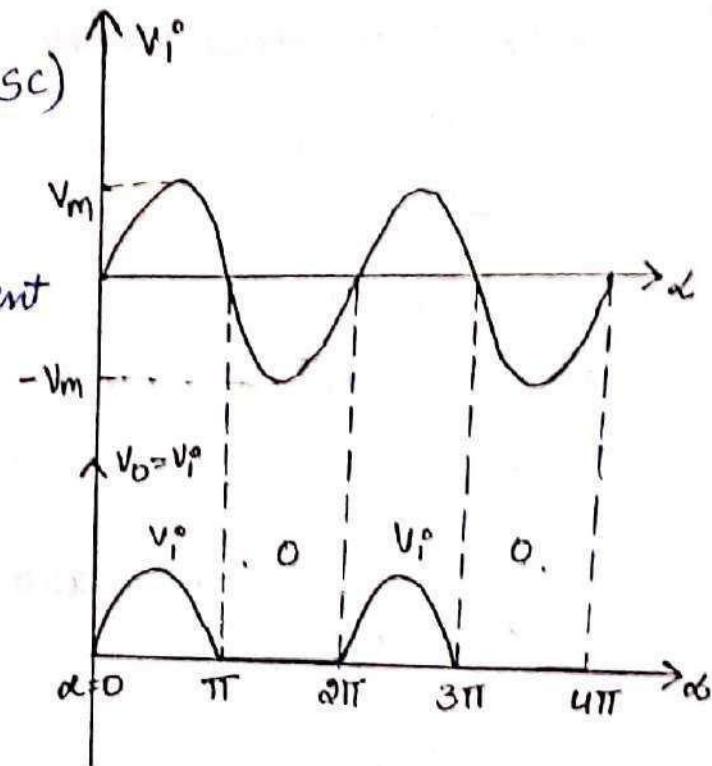
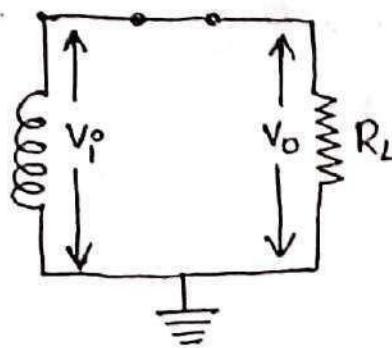
(14)

For $0 < \alpha < \pi$: (Diode in F.B \rightarrow SC)

V_i° = positive

\therefore Diode operates in F.B equivalent to a short circuit

$$V_o \approx V_i^\circ$$

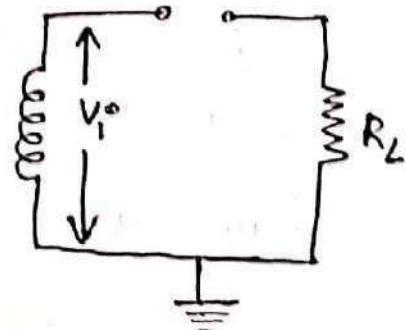


For $\pi < \alpha < 2\pi$:

V_i° = Negative or input has negative cycle

\therefore Diode operates in R.B equivalent to O.C.

V_i° appears fully across diode $V_o = 0$



- Output is a pulsating DC waveform. It varies with time which indicates the presence of AC components. Hence, a pulsating DC signal has AC and DC components.

Analysis of half-wave rectifier:

i) Instantaneous output current:

for $0 < \alpha < \pi$, $R_F =$ Diode is F.B

Apply KVL in secondary loop

$$-V_i^\circ + iR_F + iR_L = 0$$

$$i = \frac{V_i^\circ}{R_F + R_L} = \frac{V_m \sin \alpha}{R_F + R_L} = I_m \sin \alpha$$

R_F = Bulk resistance or internal resistance

where $I_m = \frac{V_m}{R_F + R_L}$
 I_m = peak O/P current

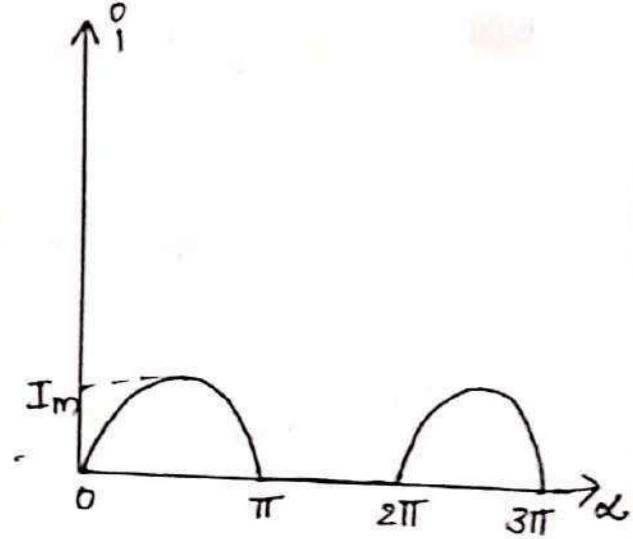
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$$\pi < \alpha < 2\pi :$$

diode is in R.B

diode passes negligible current in reverse bias condition $\therefore i \approx 0$

$$\therefore i = I_m \sin \alpha, 0 < \alpha < \pi \\ 0, \pi < \alpha < 2\pi$$



2) DC output current (I_{DC}):

I_{DC} = Average value of the instantaneous current = $\frac{\text{Area}}{\text{Time Period}}$

$$I_{DC} = \frac{1}{2\pi} \int_0^{2\pi} i \cdot d\alpha = \frac{1}{2\pi} \times \int_0^{2\pi} I_m \sin \alpha \cdot d\alpha = -\frac{I_m}{2\pi} [\cos \alpha]_0^{2\pi} = -\frac{I_m}{2\pi} [0 - 1] = \frac{I_m}{2\pi}$$

$$I_{DC} = \frac{-I_m}{2\pi} - (1-1) = \frac{I_m}{\pi}, \quad \boxed{I_{DC} = \frac{I_m}{\pi}}$$

3) RMS output current (I_{RMS}):

$$I_{RMS} = \sqrt{\frac{1}{2\pi} \int_0^{\pi} i^2 d\alpha} = \sqrt{\frac{1}{2\pi} \int_0^{\pi} (I_m \sin \alpha)^2 \cdot d\alpha}$$

$$= \sqrt{\frac{I_m^2}{2\pi} \int_0^{\pi} \sin^2 \alpha \cdot d\alpha} = \sqrt{\frac{I_m^2}{2\pi} \int_0^{\pi} \left(1 - \frac{\cos 2\alpha}{2}\right) d\alpha}$$

$$= \sqrt{\frac{I_m^2}{4\pi} \left[\alpha - \frac{\sin 2\alpha}{2}\right]_0^{\pi}} = \sqrt{\frac{I_m^2}{4\pi} [\pi - 0]}$$

$$= \sqrt{\frac{I_m^2}{4 \cdot 1}} = \frac{I_m}{2}$$

$$\boxed{I_{RMS} = \frac{I_m}{2}}$$

(16) RMS value of the AC component (I_{RMS}^1):

$$i = AC + DC$$

$$i = I_{DC} + i^1 \Rightarrow i^1 = i - I_{DC}$$

$$I_{RMS}^1 = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} i^1^2 d\alpha}$$

$$I_{RMS}^1 = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} (i - I_{DC})^2 d\alpha}$$

$$I_{RMS}^1 = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} (i^2 + I_{DC}^2 - 2 \cdot i \cdot I_{DC}) d\alpha}$$

$$I_{RMS}^1 = \frac{1}{2\pi} \int_0^{2\pi} i^2 \cdot d\alpha + \frac{I_{DC}}{2\pi} \int_0^{2\pi} d\alpha - \frac{2I_{DC}}{2\pi} \int_0^{2\pi} i d\alpha$$

$$I_{RMS}^1 = I_{RMS} + I_{DC}^2 - 2I_{DC}^2$$

$$I_{RMS}^1 = I_{RMS} - I_{DC}^2$$

$$I_{RMS}^1 = \sqrt{I_{RMS}^2 - I_{DC}^2}$$

5) Ripple factor:

It is defined as the amount of AC component present at the output of the rectifier.

Mathematically, it is given as, $\text{RI} = \frac{\text{RMS value of AC component}}{\text{DC component}}$

$$\boxed{\text{RI} = \frac{I_{RMS}^1}{I_{DC}}}$$

$$\text{RI} = \frac{\sqrt{I_{RMS}^2 - I_{DC}^2}}{I_{DC}}$$

$$= \sqrt{\frac{I_{RMS}^2 - I_{DC}^2}{I_{DC}^2}}$$

$$\boxed{\text{RI} = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1}}$$

$$= \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{4} - 1} \Rightarrow \boxed{\text{RI} = 1.11}$$

⑦ c) Input power (P_i):

It is average value of the product of instantaneous voltage across the secondary winding and instantaneous current through the secondary winding

Mathematically $P_i = \text{Avg value } (v_i \times i)$

$$P_i = \frac{1}{2\pi} \int_0^{2\pi} (v_i \times i) d\alpha$$

$$P_i = \frac{1}{2\pi} \int_0^{2\pi} i^2 (R_F + R_L) d\alpha$$

$$P_i = (R_F + R_L) \cdot \frac{1}{2\pi} \int_0^{2\pi} i^2 \cdot d\alpha$$

$$\boxed{P_i = I_{\text{RMS}}^2 (R_F + R_L)}$$

7) efficiency (η):

$$\eta = \frac{P_{DC}}{P_i} = \frac{I_{DC}^2 R_L}{I_{\text{RMS}}^2 (R_F + R_L)}$$
$$= \frac{\left(\frac{Im}{\pi}\right)^2 \cdot R_L}{\left(\frac{Im^2}{2}\right) (R_F + R_L)} = \frac{4}{\pi^2} \cdot \frac{R_L}{R_F + R_L} \times 100$$

$$\boxed{\% \eta = 40.5 \cdot \frac{R_L}{R_F + R_L} \%}$$

$$R_F \approx 0$$

$$\boxed{\eta = 40.5 \%}$$

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8) Average diode voltage (V_D , avg)

Let V_{diode} is the instantaneous diode voltage

$0 < \alpha < \pi$: diode is in F.B $V_{\text{diode}} = i \cdot R_F \approx 0$

$\pi < \alpha < 2\pi$: diode is in R.B $V_{\text{diode}} = V_f = V_m \sin \alpha$

$$\boxed{V_{\text{diode}} = 0 \quad 0 < \alpha < \pi \\ = V_m \sin \alpha \quad \pi < \alpha < 2\pi} \rightarrow \text{instantaneous diode voltage}$$

$$V_{D, \text{avg}} = \frac{1}{2\pi} \int_0^{2\pi} V_{\text{diode}} \cdot d\alpha$$

$$= \frac{1}{2\pi} \int_0^{\pi} 0 \cdot d\alpha + \int_0^{2\pi} 1 \cdot \sin \alpha \cdot d\alpha$$

$$= \frac{1}{2\pi} \int_0^{2\pi} V_m \sin \alpha \cdot d\alpha = \frac{V_m}{2\pi} \cdot [\cos \alpha]_0^{2\pi}$$

$$= -\frac{V_m}{2\pi} [1+1] = -\frac{V_m}{\pi}$$

$$\boxed{V_{D, \text{avg}} = -\frac{V_m}{\pi}}$$

q) Ripple factor:

q) Peak inverse voltage (PIV):

It is defined as the maximum voltage which appears across the diode in non-conducting state of a rectifier.

$$PIV = |V_{\text{diode}}|_{\text{max}}$$

$$= |V_m \sin \alpha|_{\text{max}}$$

$$\boxed{PIV = V_m}$$

(19)

10) Transformer utilisation factor (TUF)

$$TUF = \frac{\text{DC power delivered to load}}{\text{AC rating of transformer secondary}}$$

$$TUF = \frac{P_{dc}}{P_{ac, \text{rated}}}$$

$$P_{ac, \text{rated}} = V \times I$$

$$= \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}$$

$$= \frac{\frac{I_{dc}^2 R_L}{V_m I_m}}{\frac{2\sqrt{2}}{2\sqrt{2}}} = \frac{\frac{I_m^2}{\pi^2} \cdot R_L}{\frac{V_m \cdot I_m}{2\sqrt{2}}}$$

$$= \frac{\frac{V_m^2}{\pi^2} \cdot \frac{1}{R_L}}{\frac{V_m}{\sqrt{2}} \times \frac{V_m}{\sqrt{2} R_L}} = \frac{2\sqrt{2}}{\pi^2} \Rightarrow 0.287 = TUF$$

11) Form factor (F)

It is the measure of smoothness in wave form.

Smaller 'f' indicates greater smoothness (or) less variation in output wave form

$$F = \frac{I_{rms}}{I_{dc}} = \frac{I_m / 2}{I_m / \pi} = \frac{\pi}{2} = 1.57$$

$$F = 1.57$$

relation between ripple factor and form factor

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} \Rightarrow \boxed{\gamma = \sqrt{F^2 - 1}}$$

(20) 12) Regulation factor

It is a measure of the change in the DC output voltage due to change in the load current.

$$\text{Mathematically, } R = \frac{V_{DCNL} - V_{DCFL}}{V_{DCFL}} \times 100$$

V_{DCNL} = No load DC output voltage

$$V_{DCNL} = V_{DC} \mid \begin{array}{l} C=0 \\ R_L = \infty \end{array}, \boxed{V_{DCNL} = \frac{V_m}{\pi}}$$

V_{DCFL} = full load DC output voltage

$$V_{DCFL} = V_{DC} \mid i \neq 0$$

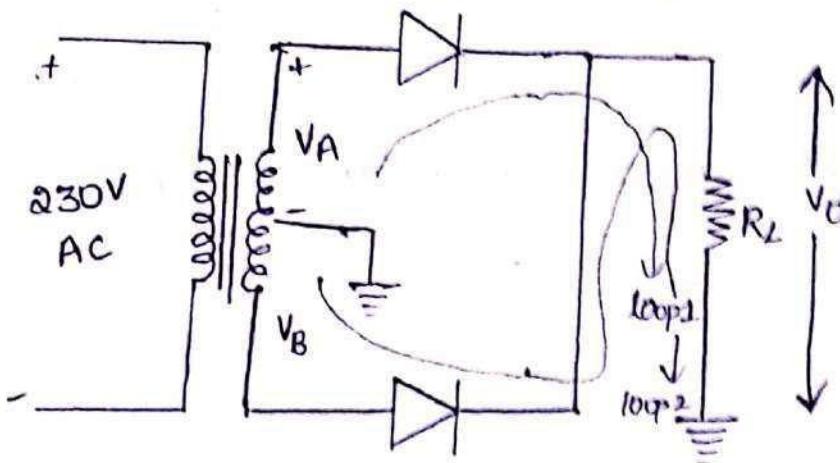
$$\boxed{V_{DCFL} = I_{DC} \times R_L}$$

$$\boxed{V_{DCFL} = \frac{V_m}{\pi} - I_{DC} \cdot R} \quad R = R_F + R_S$$

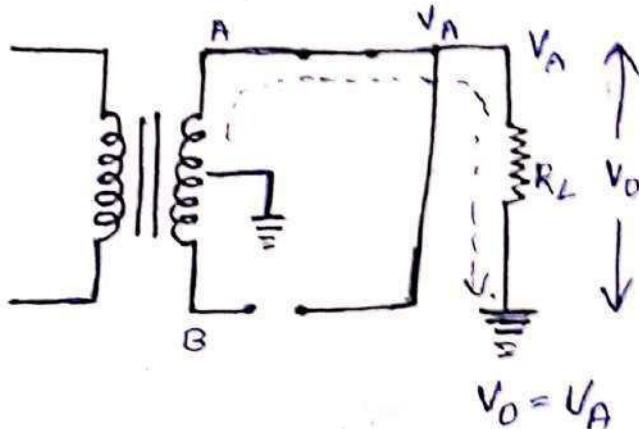
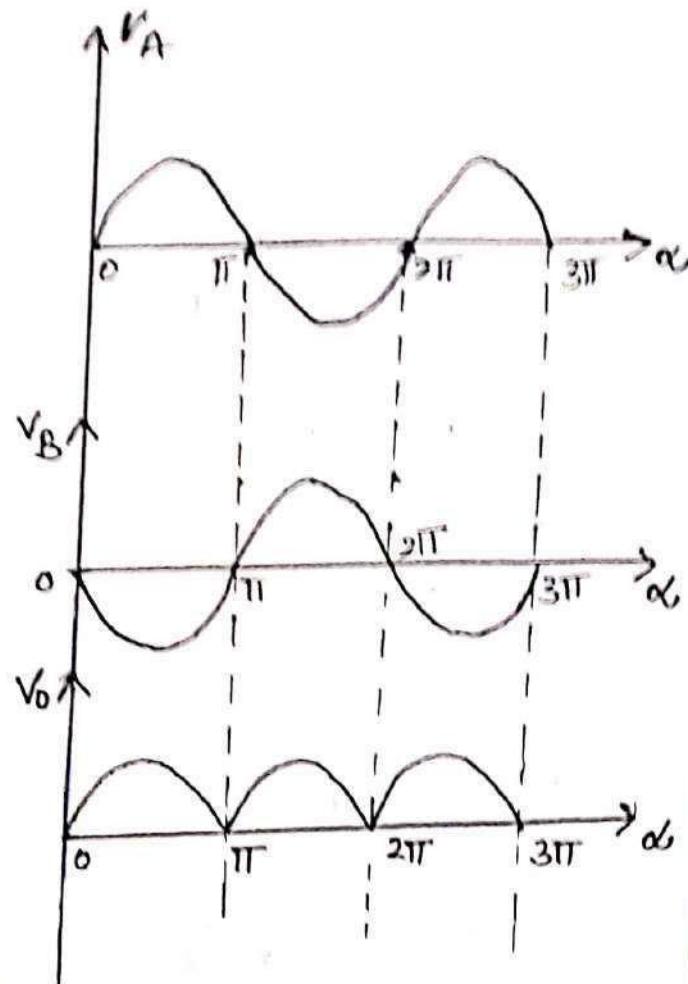
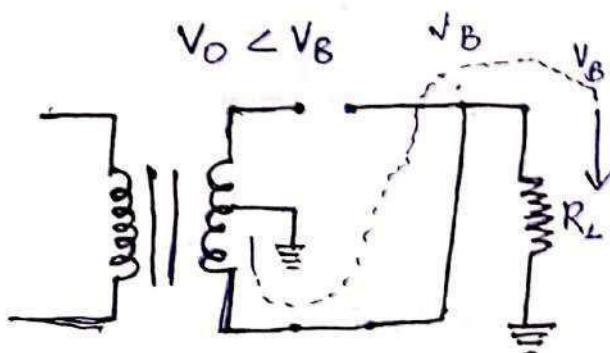
$$\boxed{R_{eq} = \frac{R}{R_L} \times 100 \%}$$

Full wave Rectifier

In this method we use 2 diodes i.e., full wave rectifier is the combination of two half wave rectifiers



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case - 1°: $0 < \alpha < \pi$ D_1 - ON D_2 - OFFcase - 2°: $\pi < \alpha < 2\pi$ Analysis1) Instantaneous output current (θ) load current (i)

$$i = i_m \sin \alpha, \quad 0 < \alpha < \pi$$

$$= -i_m \sin \alpha, \quad \pi < \alpha < 2\pi$$

$$\text{for } 0 < \alpha < \pi, \quad -V_A + i R_F + i R_L = 0$$

$$i = \frac{V_A}{R_F + R_L} = \frac{V_m \sin \alpha}{R_F + R_L} \Rightarrow i = I_m \sin \alpha$$

$$\text{for } \pi < \alpha < 2\pi, \quad -V_B + i R_F + i R_L = 0$$

$$i = \frac{V_B}{R_F + R_L} = \frac{-V_m \sin \alpha}{R_F + R_L} \Rightarrow i = -I_m \sin \alpha$$

2) DC output current (I_{DC})

I_{DC} = average value of instantaneous current (i)

$$\begin{aligned}
 I_{DC} &= \frac{1}{2\pi} \int_0^{2\pi} i \cdot d\alpha = \frac{1}{2\pi} \left[\int_0^{\pi} i_m \sin \alpha \, d\alpha - \int_{\pi}^{2\pi} i_m \sin \alpha \, d\alpha \right] \\
 &= \frac{i_m}{2\pi} \left[(-\cos \alpha)_0^{\pi} + (\cos \alpha)_{\pi}^{2\pi} \right] = \frac{i_m}{2\pi} [(1+1) + (1+1)] \\
 &= \frac{4i_m}{2\pi} = \frac{2i_m}{\pi} \quad \boxed{I_{DC} = \frac{2i_m}{\pi}}
 \end{aligned}$$

3) RMS output current (I_{RMS})

$$I_{RMS} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} i^2 \cdot d\alpha} \Rightarrow \boxed{I_{RMS} = \frac{i_m}{\sqrt{2}}}$$

4) RMS value of AC component (I'_{RMS})

$$\boxed{I'_{RMS} = \sqrt{I_{RMS}^2 - I_{DC}^2}}$$

5) Ripple factor (γ)

$$\begin{aligned}
 \gamma &= \frac{I'_{RMS}}{I_{DC}} = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1} = \sqrt{\frac{(i_m/\sqrt{2})^2}{(2i_m/\pi)^2} - 1} \\
 &= \sqrt{\frac{\frac{i_m^2}{2}}{\frac{4i_m^2}{\pi^2}}} - 1 = \sqrt{\frac{\pi^2}{8}} - 1 = 0.483
 \end{aligned}$$

$$\boxed{\gamma = 0.483}$$

(23)

6) Input power (P_i)

$$P_i = I_{\text{rms}}^2 (R_F + R_L)$$

7) Efficiency (η)

$$\eta = \frac{P_{DC}}{P_i} \times 100 = \frac{I_{DC}^2 \cdot R_L}{I_{\text{rms}}^2 (R_F + R_L)}$$

$$\eta = \frac{\frac{4I_m^2}{\pi^2} \cdot R_L}{\frac{I_m^2}{2} (R_F + R_L)} \times 100 = \frac{8}{\pi^2} \times 100 \cdot \frac{R_L}{R_F + R_L}$$

$$\eta = 81 \cdot \frac{R_L}{R_F + R_L}$$

 $R_F \approx 0$

$$\eta = 81\%$$

8) Average diode voltage (V_d, avg)For $0 < \alpha < \pi$

$$V_{\text{diode}} = 0$$

$$\text{for } \pi < \alpha < 2\pi \quad V_A - V_B$$

$$= V_m \sin \alpha - (-V_m \sin \alpha)$$

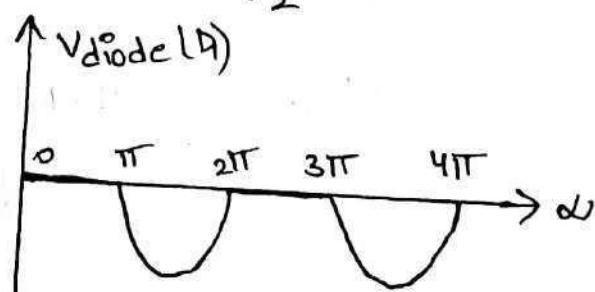
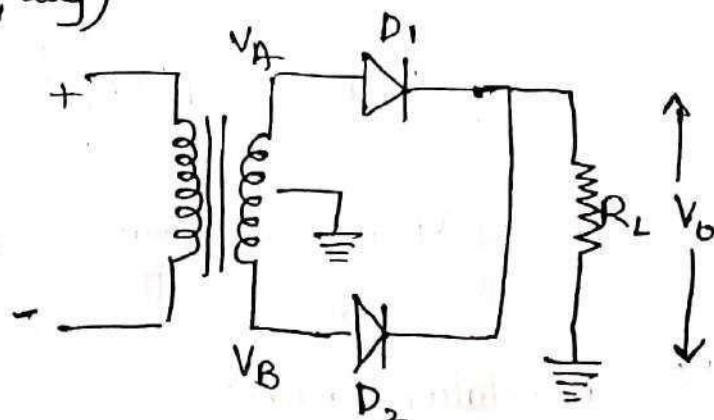
$$= 2V_m \sin \alpha$$

$$D_1 \rightarrow V_{\text{diode}} = 0 \Rightarrow 0 < \alpha < \pi$$

$$2V_m \sin \alpha, \Rightarrow \pi < \alpha < 2\pi$$

$$D_2 \rightarrow V_{\text{diode}} = -2V_m \sin \alpha \quad 0 < \alpha < \pi$$

$$= 0 \quad \pi < \alpha < 2\pi$$



$$V_d, \text{avg} = \frac{1}{2\pi} \int_0^{2\pi} V_{\text{diode}} \cdot d\alpha$$

$$V_d, \text{avg} = -\frac{2V_m}{\pi}$$

(24)

9) Peak Inverse voltage (PIV)

$$\text{PIV} = |V_{\text{diode}}| = |\omega V_m \sin \omega t_{\max}| = \omega V_m$$

$$\boxed{\text{PIV} = \omega V_m}$$

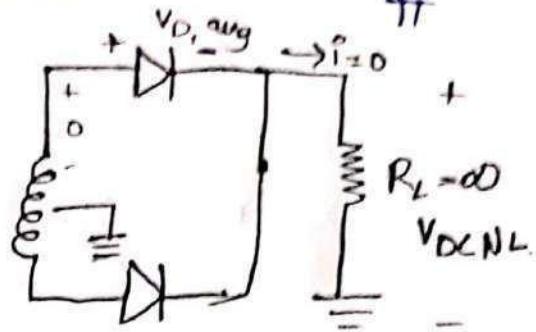
10) No load DC O/P voltage (V_{DCNL}):

$$V_{DCNL} = V_{DC} \mid i=0 \text{ or } R_L = \infty$$

$$0 + V_{D,\text{avg}} + V_{DCNL} = 0.$$

$$\boxed{V_{DCNL} = \frac{\omega V_m}{\pi}}$$

$$V_{DCNL} = -V_{D,\text{avg}} = \frac{\omega V_m}{\pi}$$

11) Full load DC O/P voltage (V_{DCF})

$$V_{DCF} = V_{DC} \mid i \neq 0.$$

$$\boxed{V_{DCF} = I_{DC} \cdot R_L}$$

$$\boxed{V_{DCF} = \frac{\omega V_m}{\pi} - I_{DC} \cdot R}$$

$$R = R_F + \frac{R_S}{2}$$

12) Regulation factor:

$$\% \text{ reg.} = \frac{V_{DCNL} - V_{DCF}}{V_{DCF}} \times 100$$

$$\boxed{\% \text{ regulation} = \frac{R}{R_L} \times 100 \%}$$

$$R = R_F + \frac{P_{SW}}{Q}$$

25) 13) Form factors (F).

$$F = \frac{I_{RMS}}{I_{DC}} = \frac{I_m / \sqrt{2}}{\omega I_m / \pi} = \frac{\pi}{2\sqrt{2}} = 1.11$$

$$F = 1.11$$

Bridge Rectifier

$$V_i^\circ = V_m \sin \alpha$$

for $0 < \alpha < \pi$

$$V_i^\circ \text{ is } +V_L, D_1, D_3 - F.B, D_2, D_4 = O.N.$$

$$D_2, D_4 = R.B.$$

$$V_o = V_i^\circ$$

for $\pi < \alpha < 2\pi$

$$V_i^\circ \text{ is } -V_L, D_2, D_4 = F.B, D_1, D_3 = O.N.$$

$$V_o = V_i^\circ$$

Analysis

1) Instantaneous output current (i)

$$\begin{aligned} i^\circ &= I_m \sin \alpha, \quad 0 < \alpha < \pi \\ &= -I_m \sin \alpha, \quad \pi < \alpha < 2\pi \end{aligned}$$

$$\text{where } I_m = \frac{V_m}{\omega R_F + R_L}$$

2) I_{DC}

$$I_{DC} = \frac{\omega I_m}{\pi}$$

3) I_{RMS}

$$I_{RMS} = \frac{I_m}{\sqrt{2}}$$

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4) I_{RMS}^1

$$I_{RMS}^1 = \sqrt{I_{RMS}^2 - I_{DC}^2}$$

5) supply factor

$$\eta = 0.483$$

6) Input power

$$P_i = I_{RMS}^2 (\delta R_F + R_L)$$

7) Efficiency

$$\% \eta = 81 \times \frac{R_L}{\delta R_F + R_L} \%$$

8) Average diode voltage

consider D_1 , $V_{diode} = 0$, $0 < \alpha < \pi$

$$= V_m \sin \alpha, \pi < \alpha < 2\pi$$

$$V_{D, avg} = - \frac{V_m}{\pi}$$

9) PIV

 $|V_{diode}|_{max}$ in R.B, $PIV = |V_m \sin \alpha|_{max}$

$$PIV = V_m$$

10) V_{DCNL}

$$V_{DCNL} = \frac{\alpha V_m}{\pi}$$

11) V_{DCF}

$$V_{DCF} = I_{DC} \cdot R_L$$

$$V_{DCF} = \frac{\alpha V_m}{\pi} - I_{DC} \cdot R$$

12) Regulation factors

$$\% \text{ reg} = \frac{R}{R_L} \times 100 \%$$

13) Form factors

$$F = 1.11$$

(27) Clipper circuits

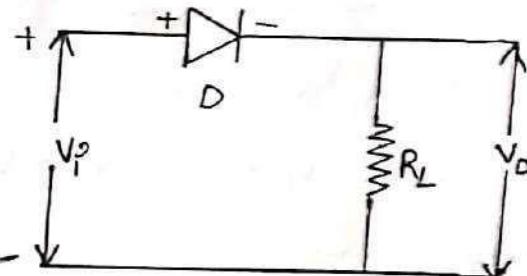
The circuits which are used to clip off unwanted portion of the waveform, without distorting the remaining part of the waveform, are called clipper circuits or clippers. When the diode is connected in series with the load, such circuit is called series clipper. When the diode is connected in a branch which is parallel to the load, it is called Parallel clipper.

Series clippers

It is of two types

i) Series Negative clipper circuit

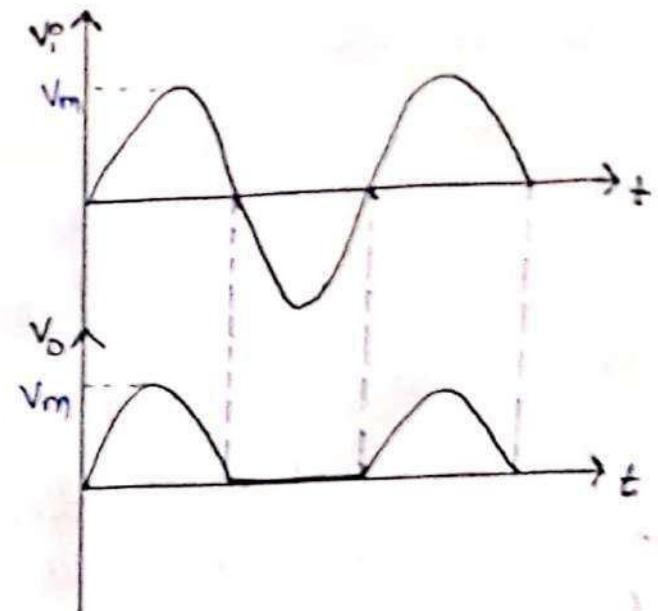
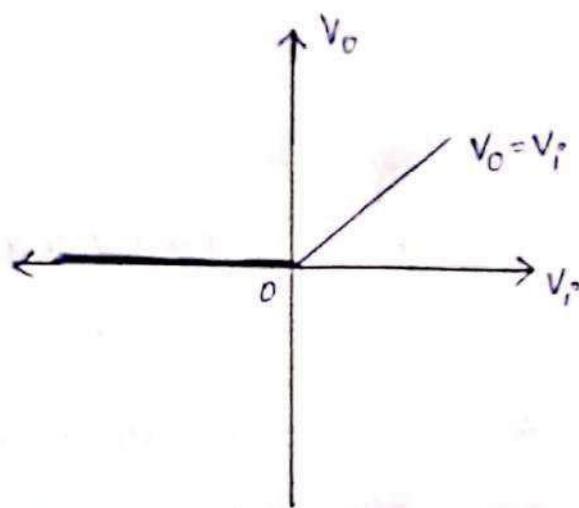
For a positive half cycle, the diode D is forward biased, hence the voltage waveform across R_L looks like a +ve half cycle input voltage. While for negative half cycle, diode D is reverse biased and hence will not conduct at all. Hence there will not be any voltage available across resistance R_L . Hence the -ve half cycle of input voltage gets clipped off. As it clips off negative half cycle of the input is called series negative clipper.



Case-1 : when the diode is ideal

$$V_P = V_i, V_N = 0$$

$$\text{i)} V_P > V_N, V_i > 0, V_o = V_i \quad \text{ii)} V_P < V_N, V_i < 0, V_o = 0.$$



Transfer characteristics with ideal diode

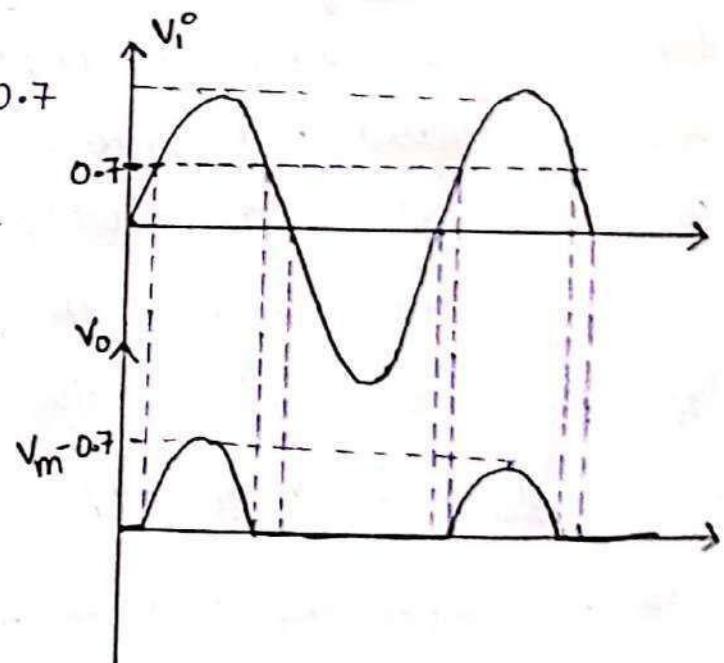
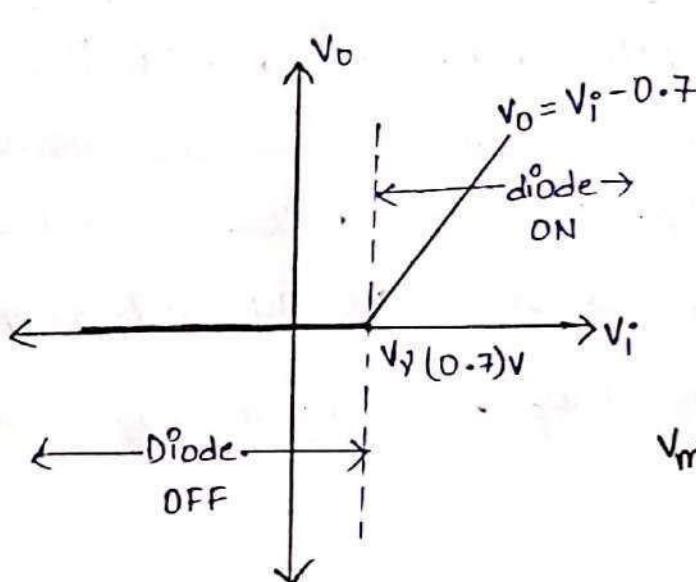
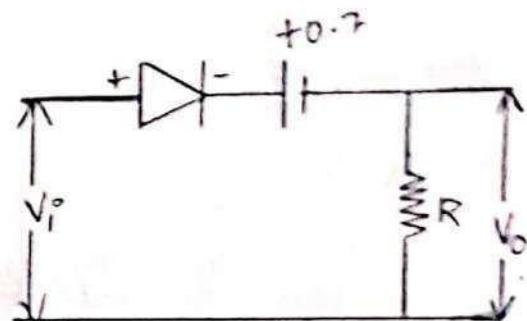
Case-II: considering V_r

Effect of cut-in voltage of diode

$$V_p = V_i^+ , V_N = 0.7$$

i) $V_p > V_N , V_i^+ > 0.7 , V_o = V_i^+ - 0.7V$
Diode is ON

ii) $V_p < V_N , V_i^+ < 0.7 , V_o = 0$ - Diode is OFF



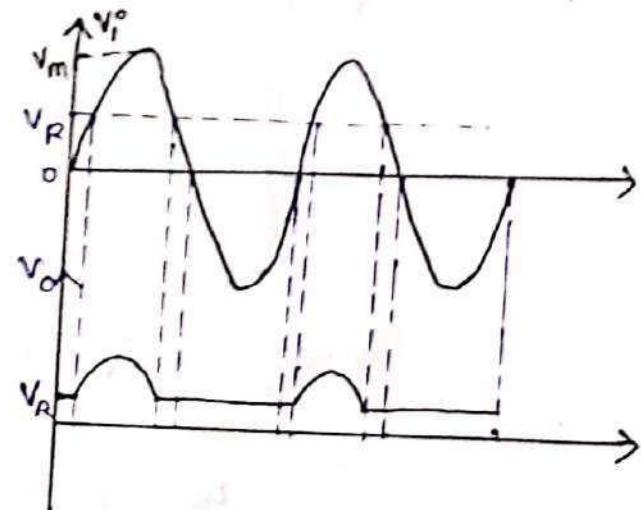
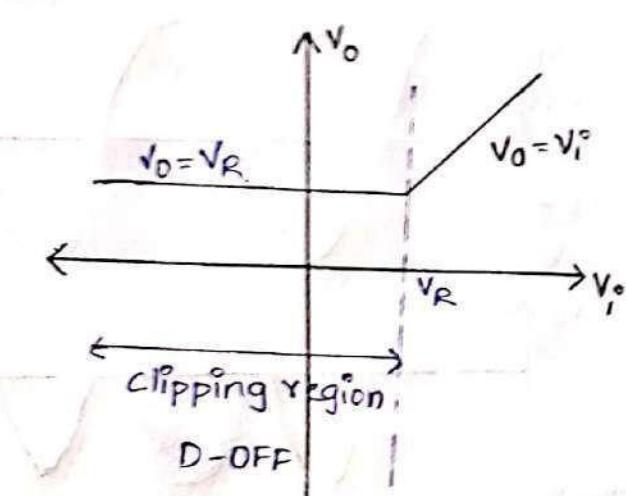
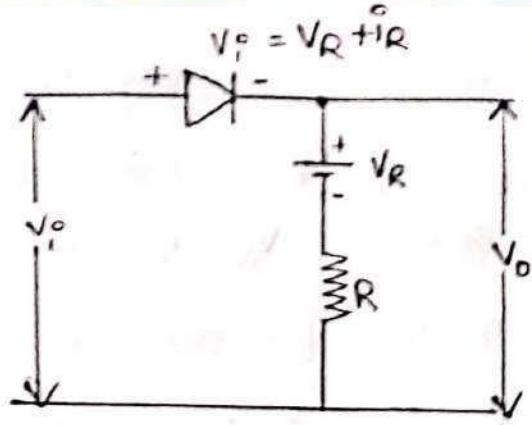
Case - III: Considering V_R

clipping above V_R below V_R

$$V_P = V_i^o, V_N = V_R$$

i) $V_P > V_N, V_i^o > V_R, V_o = V_i^o \rightarrow \text{Diode ON}$

ii) $V_P < V_N, V_i^o < V_R, V_o = V_R \rightarrow \text{Diode OFF}$



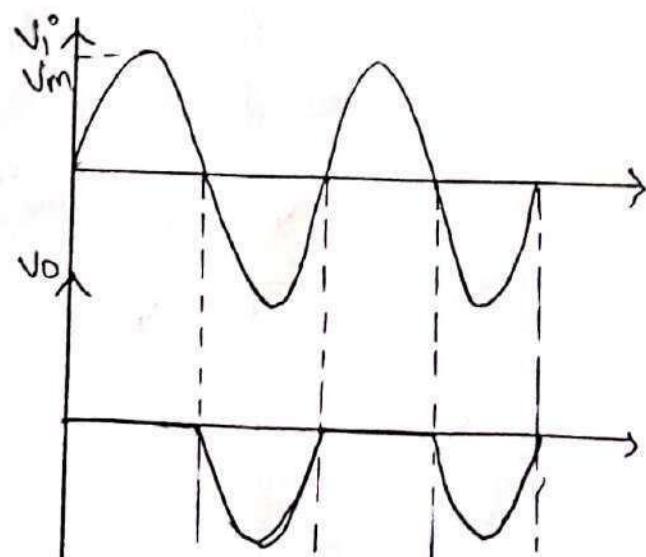
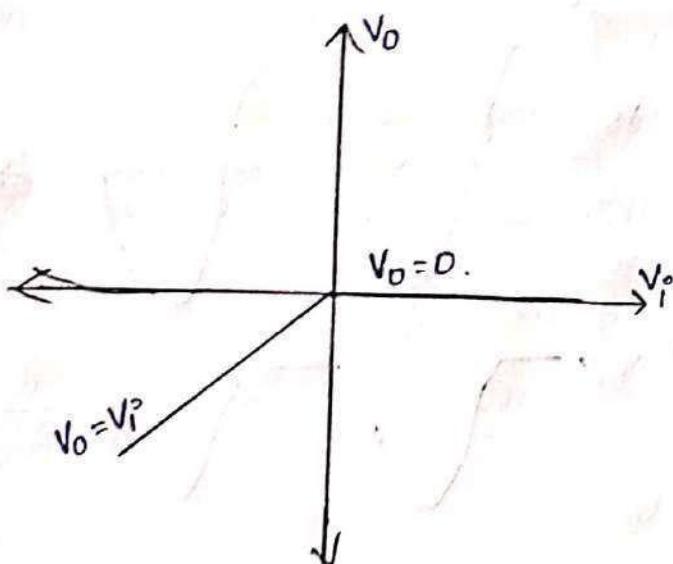
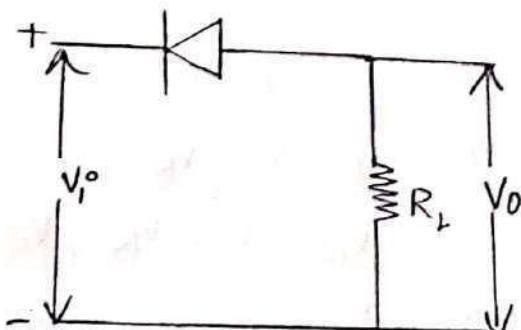
iii) Series Positive clipper circuit

Case - I: Considering the diode is ideal

$$V_N = V_i^o, V_P = 0$$

i) $V_P > V_N, V_i^o < 0, V_o = V_i^o \rightarrow \text{Diode - ON}$

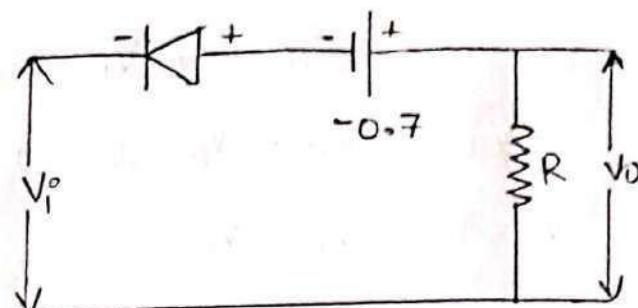
ii) $V_P < V_N, V_i^o > 0, V_o = 0 \rightarrow \text{Diode - OFF}$



③ Case-II: Considering V_D

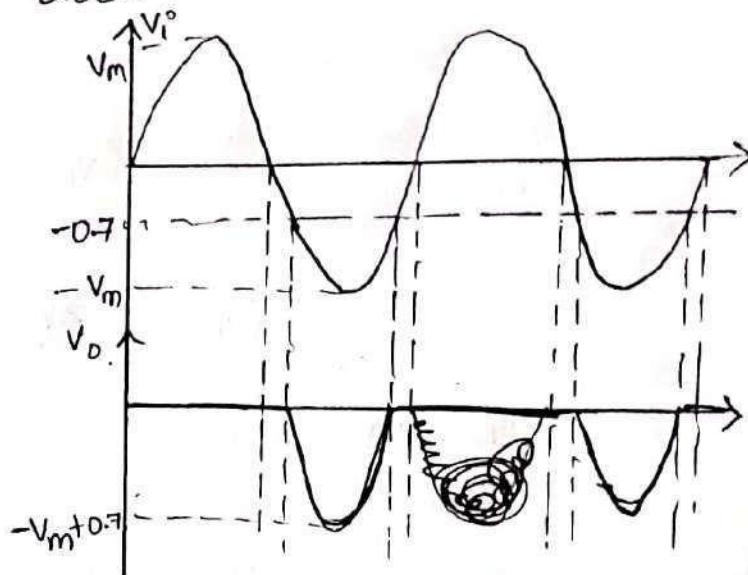
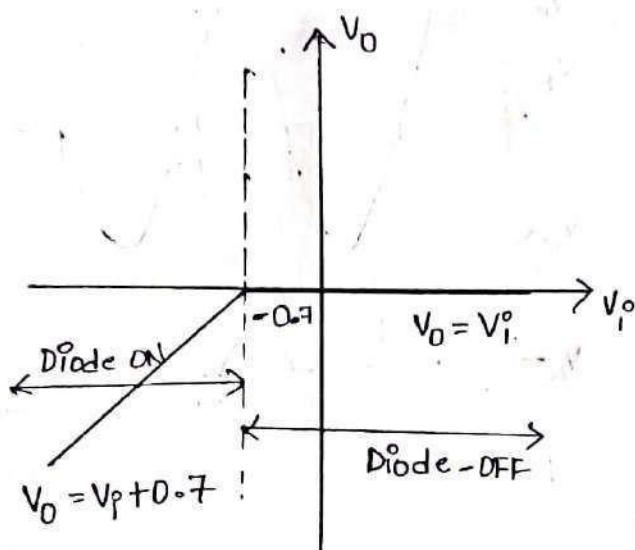
Effect of V_D on positive clipper circuit

$$V_N = V_P, V_P = -0.7$$



i) $V_P > V_N, V_i^o < -0.7, V_O = V_i^o + 0.7 - \text{Diode ON}$

ii) $V_P < V_N, V_i^o > -0.7, V_O = 0 - \text{Diode OFF}$

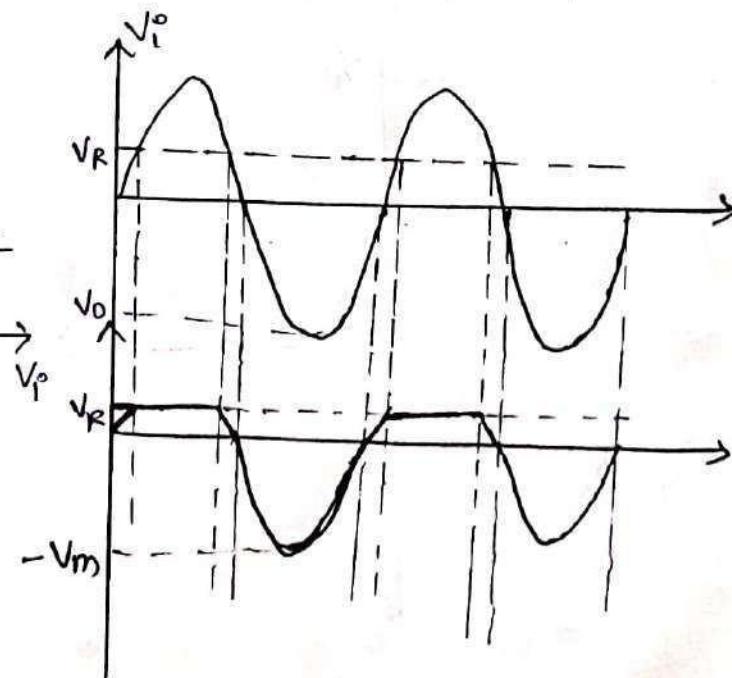
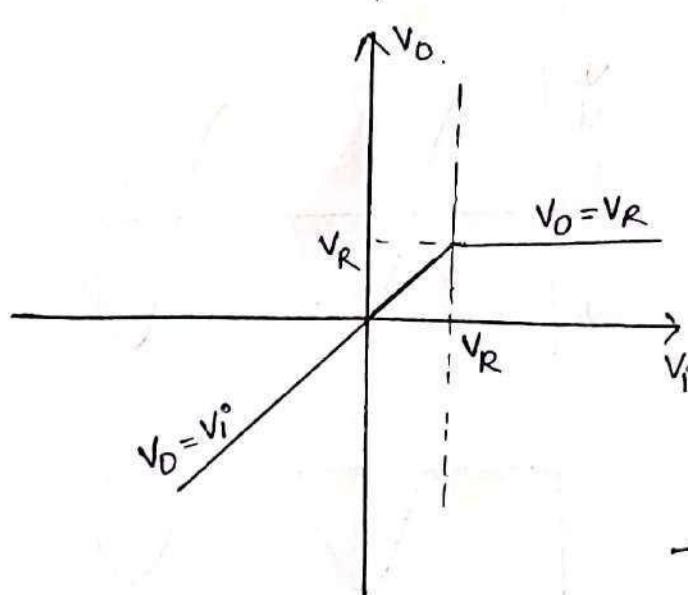
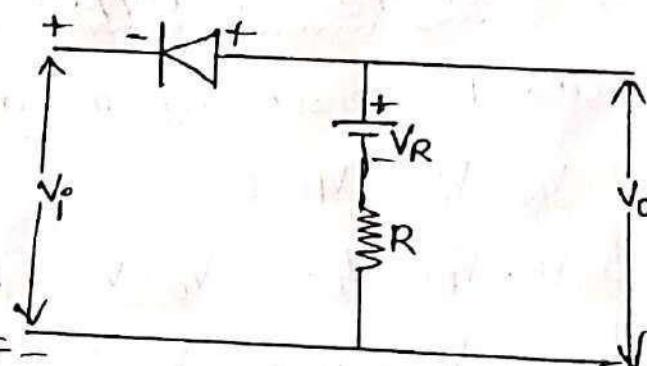


Case-III: Clipping above V_R

$$V_N = V_P, V_P = V_R$$

i) $V_P > V_N, V_i^o < V_R, V_O = V_i^o - \text{Diode ON}$

ii) $V_P < V_N, V_i^o > V_R, V_O = V_R - \text{Diode OFF}$



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Parallel Clippers

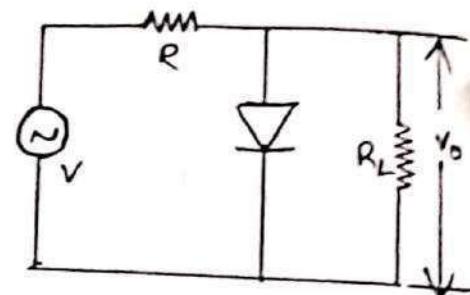
In a parallel clipper circuit, the diode is connected across the load terminals. It can be used to clip the positive or negative part of the input signal, as per the requirement.

1) Basic parallel clipper with positive clipping

Assume the diode is ideal

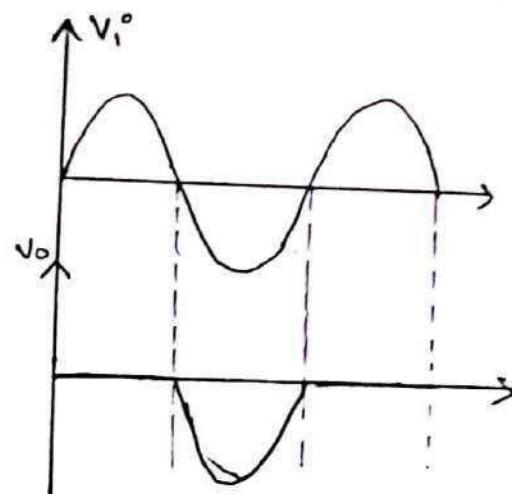
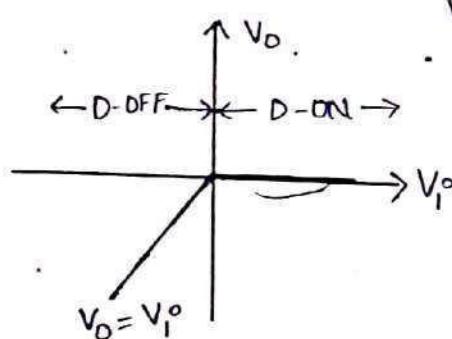
acts as S.C when forward biased

case-I : $V_P > V_N, V_i > 0$ Diode-ON
 $V_O = 0$.



case-II : $V_P < V_N, V_i < 0$ Diode-off
 $V_O = V_i$

$$V_O = \frac{V_i \times R_L}{R} \text{ if } R \ll R_L$$



2) Effect of cut-in voltage with positive clipping

$$V_P = V_i, V_N = 0.7$$

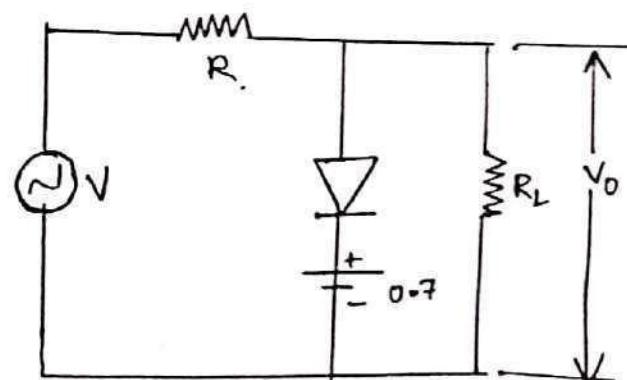
case-I : $V_P > V_N, V_i > 0.7$

$$\text{D-ON}, V_O = 0.7$$

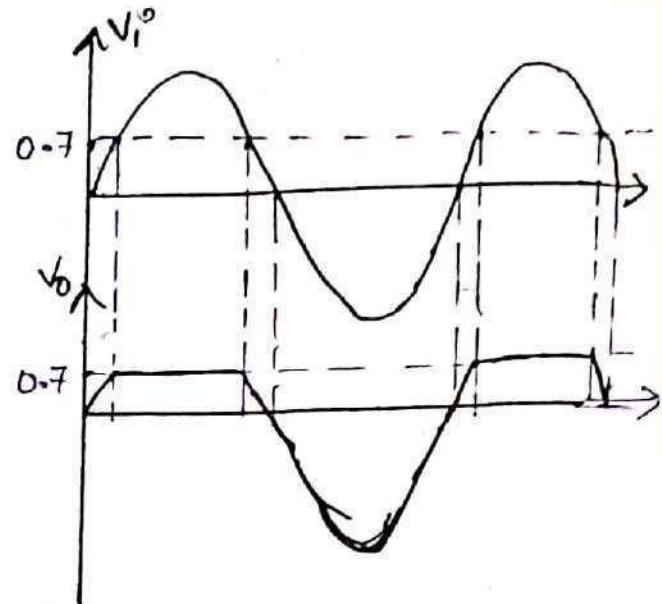
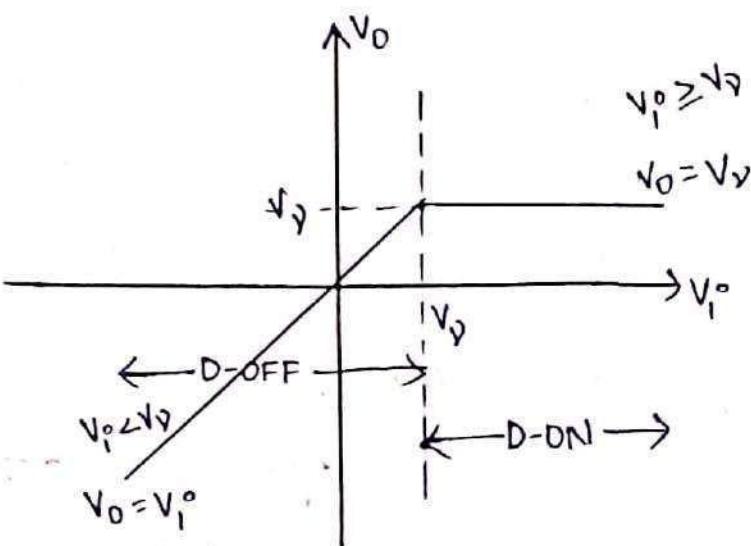
case-II : $V_P < V_N, V_i < 0.7$

$$\text{D-OFF}, V_O = V_i \times \frac{R_L}{R}$$

$$R \ll R_L, V_O = V_i$$



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3) Positive parallel clipper with reference voltage V_R

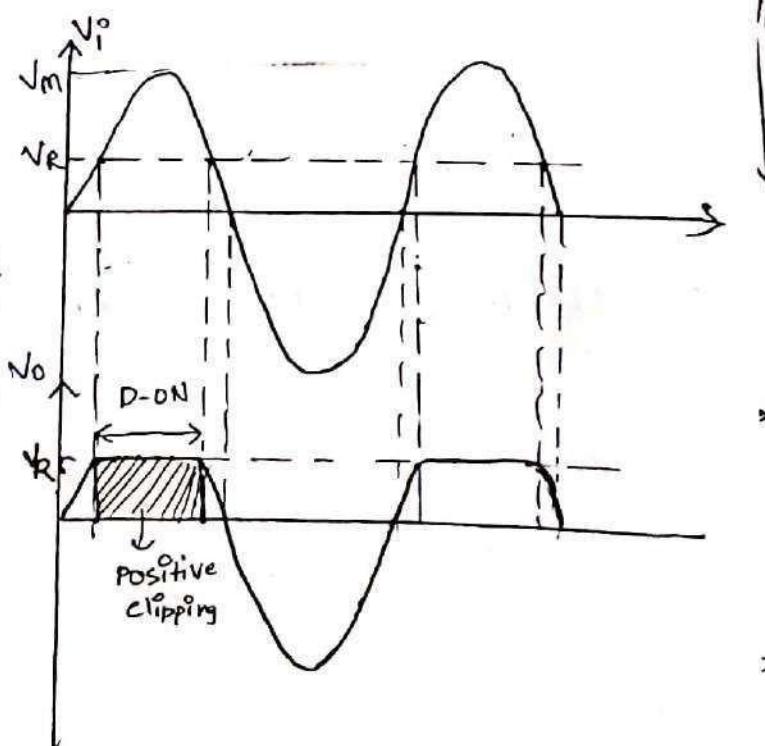
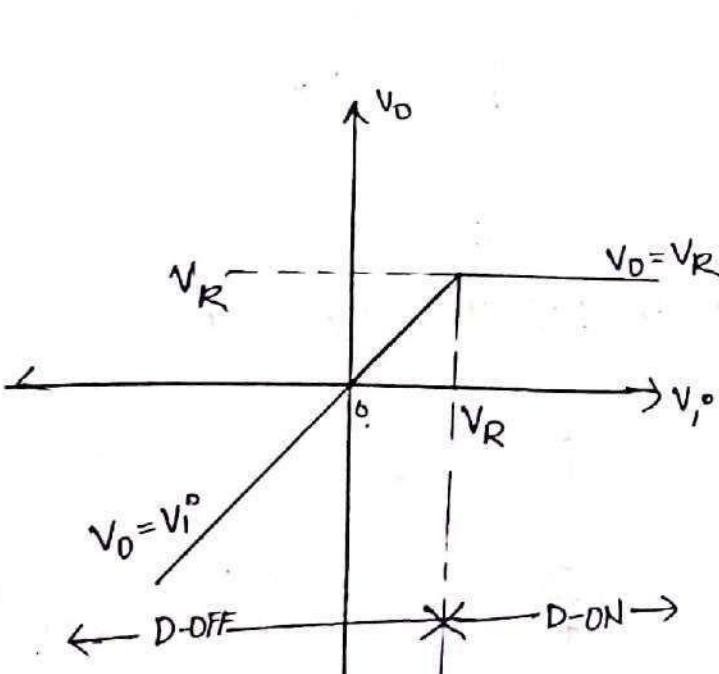
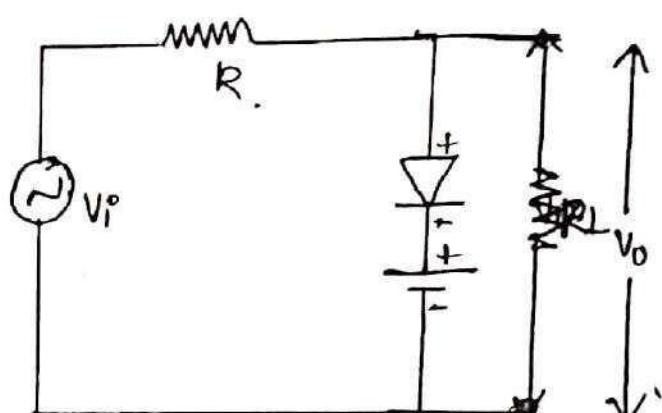
$$V_P = V_i^o, \quad V_N = V_R$$

Case - I : $V_P > V_N$, diode-ON

$$V_i^o > V_R, \quad V_o = V_R$$

Case - II : $V_P < V_N$, $V_i^o < V_R$

$$V_o = V_i^o - \text{diode-OFF}$$



(33)

u) Basic Parallel Clipper with negative clipping

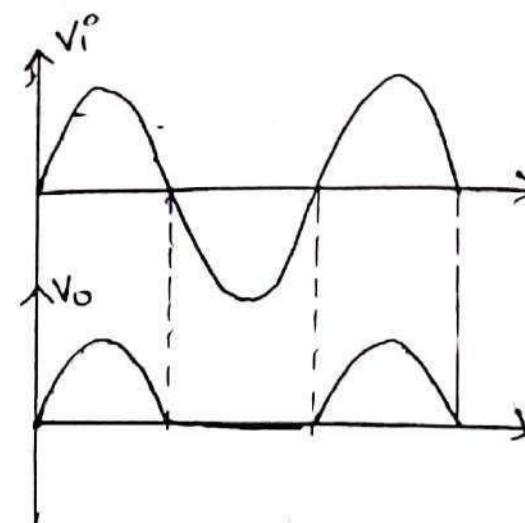
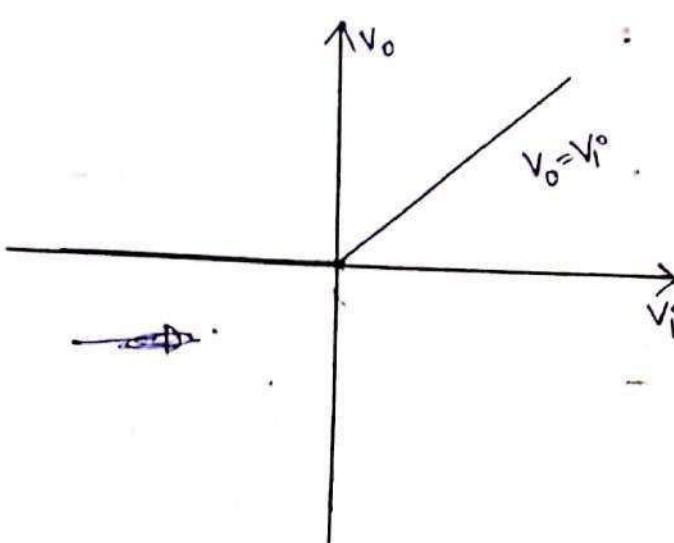
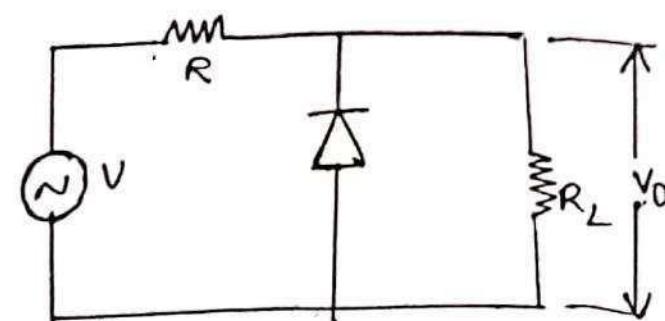
$$V_p = 0, V_N = V_i^o$$

Case-1 : $V_p > V_N, V_i < 0$ - D-ON

$$V_D = 0$$

Case-II : $V_p < V_N, V_i > 0$ - D-OFF

$$V_o = V_i \times \frac{R_L}{R} \quad R \ll R_L \quad V_o = V_i^o$$



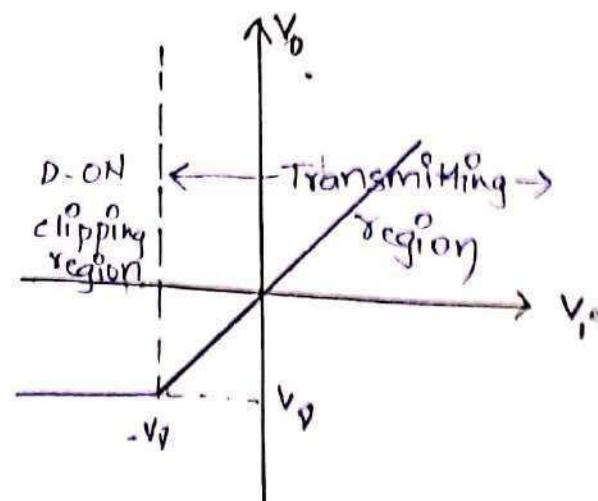
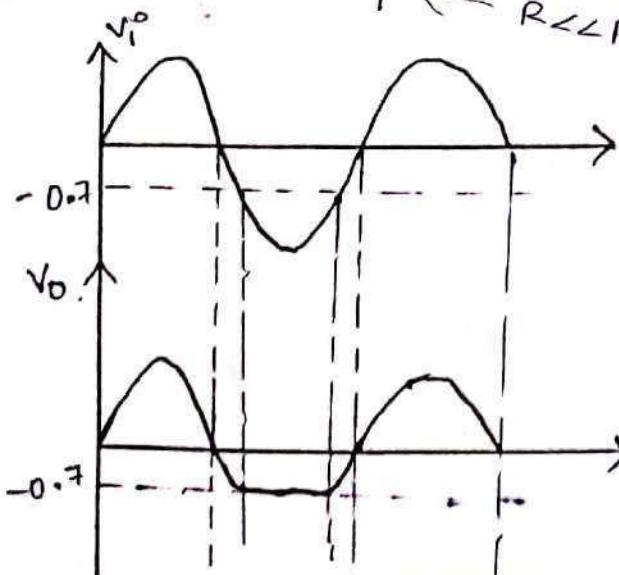
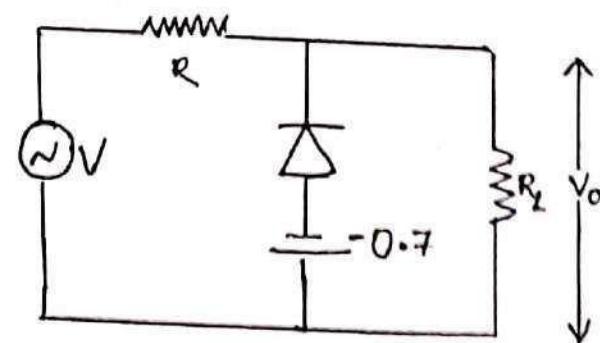
5) Effect of cutin voltage with negative clipping

$$V_p = -0.7, V_N = V_i^o$$

Case-1 : $V_p > V_N, V_i < -0.7, V_o = -0.7$

case-II : $V_p < V_N, V_i > -0.7$ D-ON

$$\text{D-OFF} \quad V_o = V_i^o \quad R \ll R_L \quad V_D = V_i^o \times \frac{R_L}{R}$$



6) Negative parallel clipper with reference voltage V_R

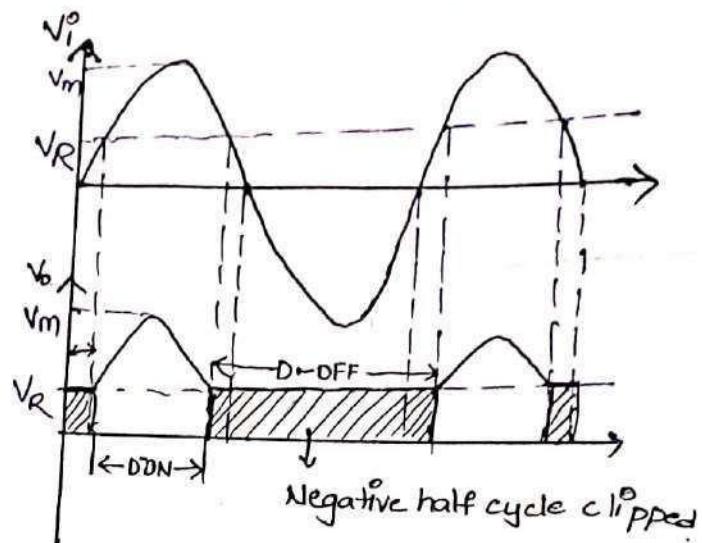
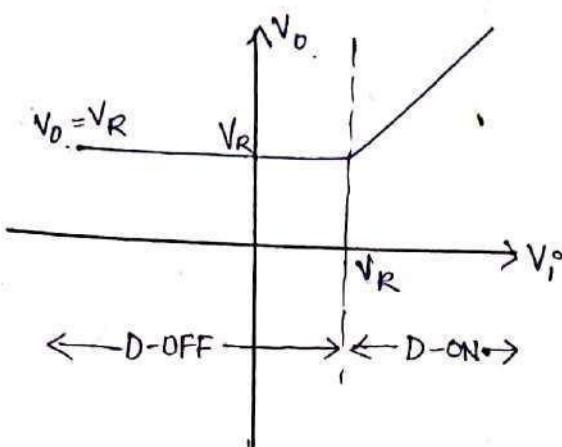
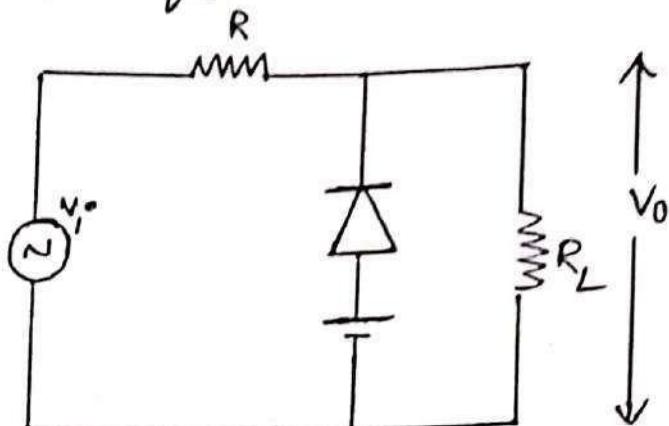
$$V_P = V_R ; V_N = V_i^o$$

Case-1 : $V_P > V_N \rightarrow D\text{-ON}$

$$V_i^o < V_R , V_0 = V_R$$

Case-2 : $V_P < V_N \rightarrow D\text{-OFF}$

$$V_i^o > V_R , V_0 = V_i^o$$



Two way Parallel clipper circuit.

Combining positive and negative clipper circuits with V_R , a two way parallel clipper can be obtained.

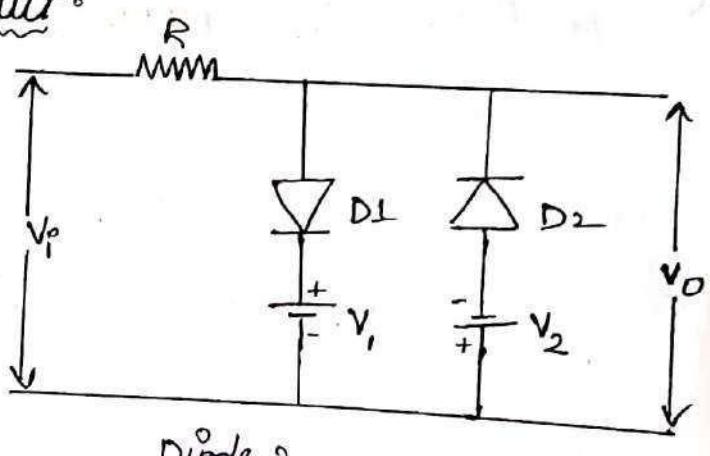
Diode 1

Assume $D_1\text{-OFF}$

$$V_P = V_i^o , V_N = V_R$$

i) $V_P > V_N , V_i^o > V_1 , V_0 = V_R$
 $D_1\text{-ON}$

ii) $V_P < V_N , V_i^o < V_1 , V_0 = V_i^o$
 $D_1\text{-OFF}$



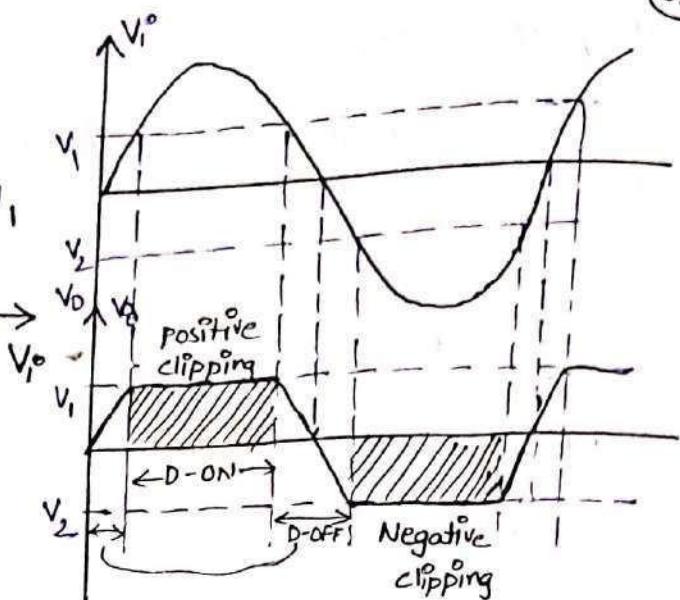
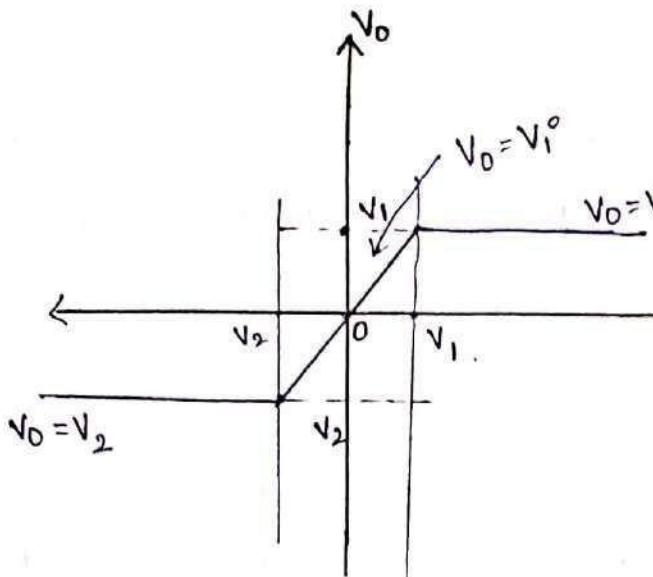
Diode 2

Assume $D_2\text{-OFF}$

$$V_N = V_i^o , V_P = -V_2$$

i) $V_P > V_N , V_i^o < -V_2 , V_0 = -V_2$
 $D_2\text{-OFF}$

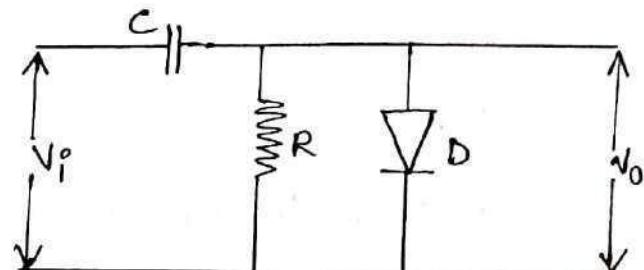
ii) $V_P < V_N , V_i^o > -V_2 , V_0 = V_i^o$
 $D_2\text{-ON}$



Clamping - Circuit Theorem

Statement: Under steady state conditions, for any input waveform, the ratio of the area under the output curve in forward direction (when the diode conducts) to the area under the output curve in reverse direction [when diode does not conduct] is given by,

$$\frac{A_F}{A_R} = \frac{R_f}{R}$$



where

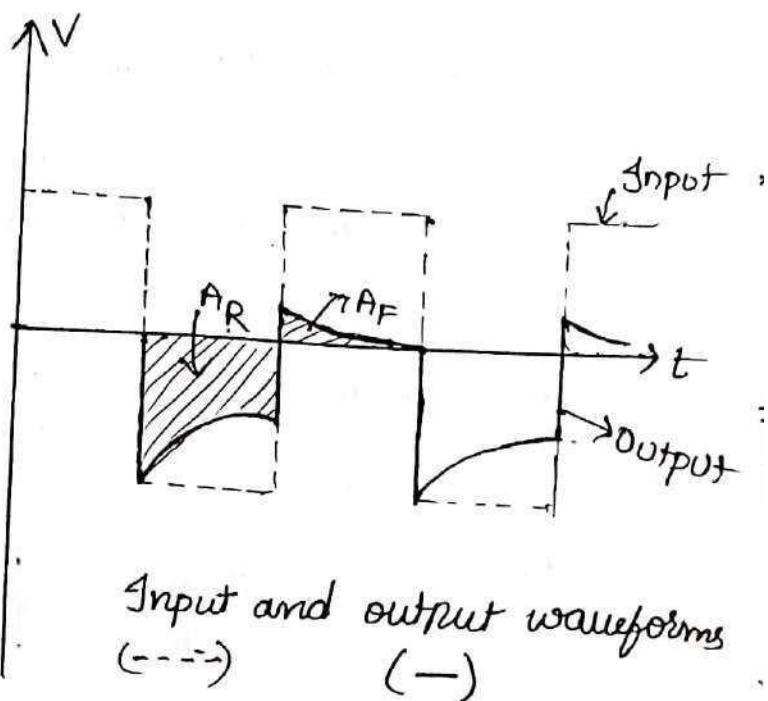
A_F = Area under output curve
in forward direction

A_R = Area under output curve
in reverse direction

R_f = Forward resistance of
the diode

R = shunt resistance.

Input applied is square wave



Clamper Circuits

The circuits which are used to add a D.C level as per the requirements to the A.C output signal are called clamper circuits.

Types of clamps

i) Negative clamp

The following assumptions are made while analysing the clamps circuit

1. The diode is ideal in behaviour
2. The time constant $\tau = RC$ is designed to be very large by selecting large values of R and C

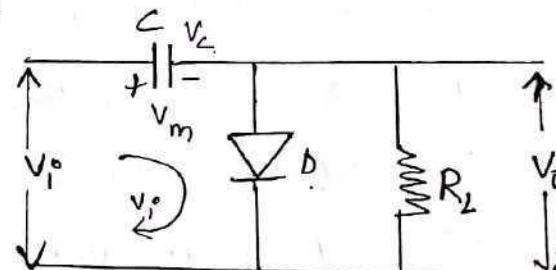
$$V_i^o - V_c - V_o = 0$$

$$V_c = V_m$$

Due to large RC time const the capacitor holds its

$$V_o = V_i^o - V_c$$

entire charge & capacitor V remains as $V_c = V_m$



$$V_i^o = V_m ;$$

$$V_o = V_m - V_m = 0 \Rightarrow V_o = 0$$

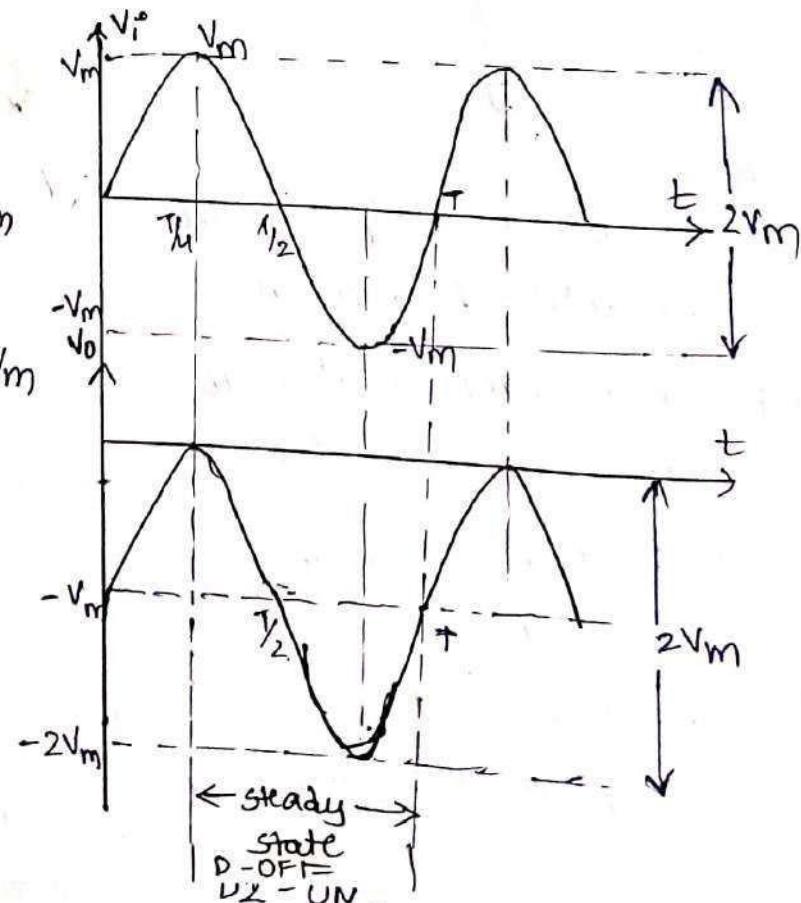
$$V_i^o = 0 ;$$

$$V_o = 0 - V_m = -V_m \Rightarrow V_o = -V_m$$

$$V_i^o = -V_m ;$$

$$V_o = -V_m - V_m = -2V_m \Rightarrow V_o = -2V_m$$

$V_o = -V_m$	for $V_i^o = 0$
$V_o = 0$	for $V_i^o = V_m$
$V_o = -2V_m$	for $V_i^o = -V_m$



i) Positive clamping

It adds $+V_C$ DC level to AC output signal

$$V_C = -V_m$$

$$-V_i + V_C - V_o = 0$$

$$V_o = V_i - V_c$$

when $V_i = V_m$

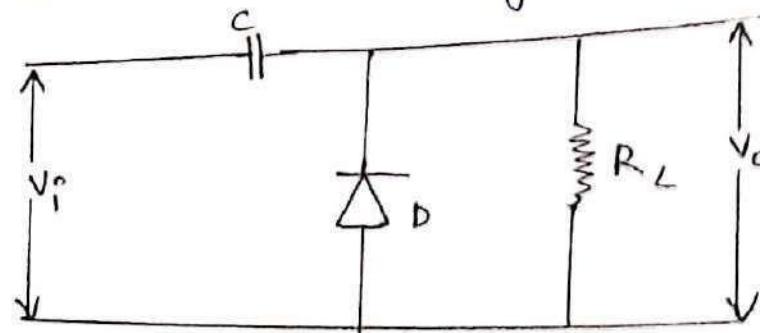
$$V_o = V_m + V_m = 2V_m$$

$$\Rightarrow V_i = 0$$

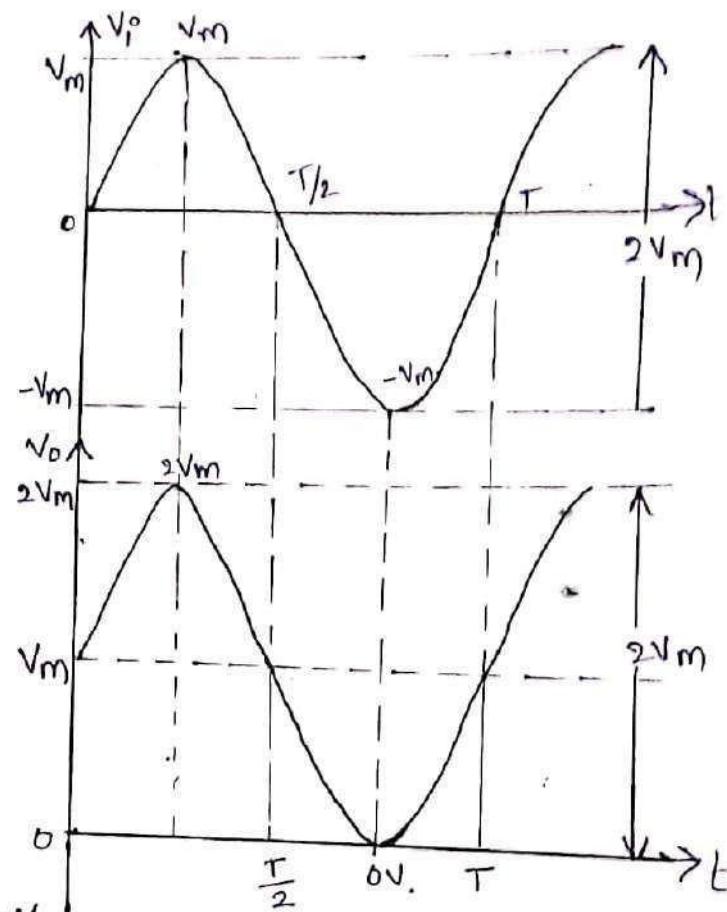
$$V_o = 0 + V_m = V_m$$

$$\Rightarrow V_i = -V_m$$

$$V_o = -V_m + V_m = 0$$



$V_o = V_m$	for $V_i = 0$
$V_o = 2V_m$	for $V_i = V_m$
$V_o = 0$	for $V_i = -V_m$

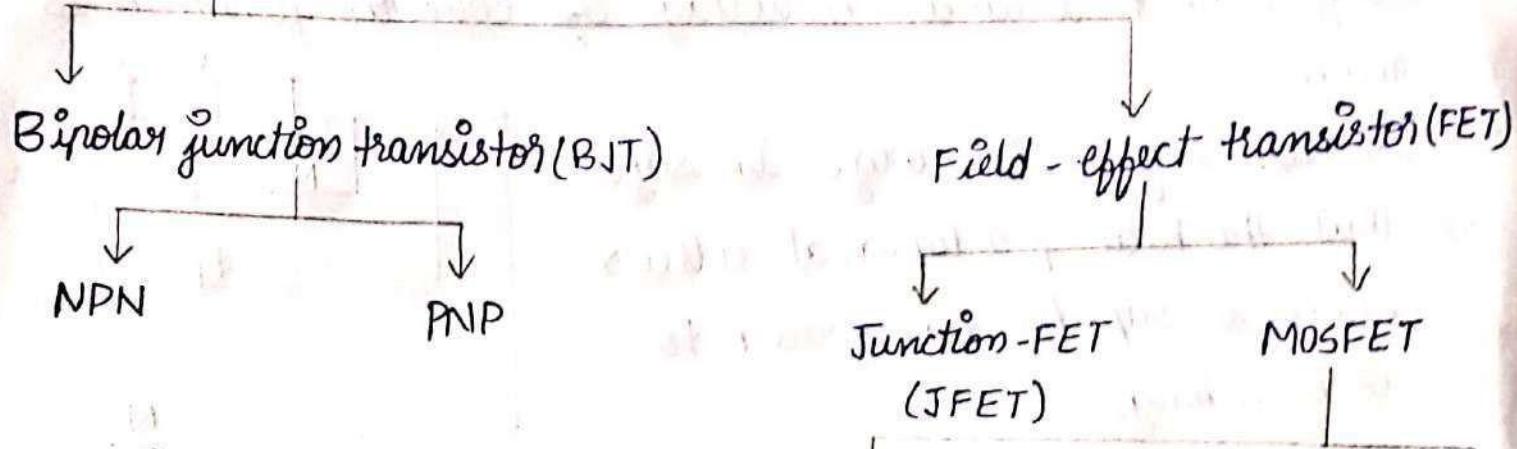


Steps to Analyze clamping Network

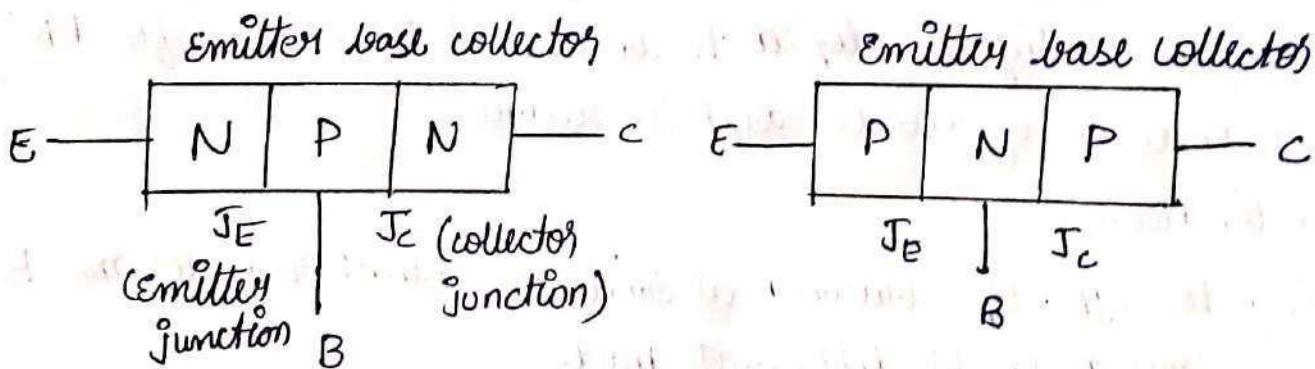
- 1) start the analysis of the clamping network by considering that part of the input which will forward bias the diode
- 2) when the diode is conducting, assume the capacitor charges instantly to the peak value of the input
- 3) assume that the diode is not conducting, the capacitor remains charged at the peak value as there is no discharging path
- 4) Analyze the output and sketch the wave form

UNIT-II. BIPOLAR JUNCTION TRANSISTOR

Transistor (classification)



- BJT is called a bipolar device because both majority and minority carriers participate in flow of current.
- BJT is a current controlled device because base current controls the carriers flow from emitter to collector.



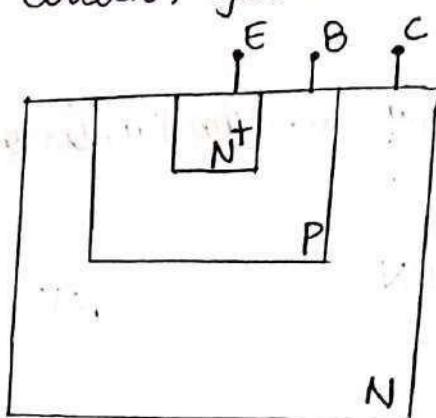
Emitter : A region which emits or supplies majority carriers

NPN → Emitter emits or injects e^- from emitter to base,

PNP → Emits holes

→ Emitter region is heavily doped so that it supplies large no. of carriers.

- Collector - A region which collects or receives carriers supplied by emitter. collector region is moderately doped.
- If collector is lightly doped, its conductivity becomes low.
- If collector is heavily doped then "Early effect" becomes stronger and breakdown voltage of collector junction is smaller
- collector region is large in size so that the heat produced at collector junction is rapidly transferred to surroundings



Base - A region through which carriers are transported from emitter to collector.

- To minimize recombinations inside base region, base width should be much smaller than the diffusion length of carriers injected by the emitter. or $W_B \ll L_N$ for NPN
 $W_B \ll L_P$ for PNP
- Base region is lightly doped to increase emitter injection efficiency and to reduce recombinations

According to type of biasing at emitter & collector junctions BJT can be operated in 4 different modes

Mode	J_E	J_C	Property	Application
1) cutoff	R.B	R.B	Very high internal resistance (Negligible current flow)	OFF switch
2) saturation	F.B	F.B	Very low internal resistance	ON switch
3) Active or forward active	F.B	R.B	Excellent transistor action (efficient transport of carriers from emitter to base)	Amplifier
4) Reverse active	R.B	F.B	Poor transistor action	Attenuator

Transistor action: It refers to efficient transportation of carriers from emitter to collector (3)

NOTE: In Analog circuits BJT is not operated in reverse active mode

Flow of current in Active Mode:

Consider a PNP-transistor operated in active mode

V_{EB} : Forward voltage across Emitter junction (J_E)

V_{CB} : Reverse voltage across (J_C)

A PNP transistor operates in active mode if $V_E > V_B > V_C$

(NPN transistor operates in active mode if $V_E < V_B < V_C$)

→ Due to forward biasing of emitter junction:

i) Holes are injected from emitter to base which results in current I_{PE}

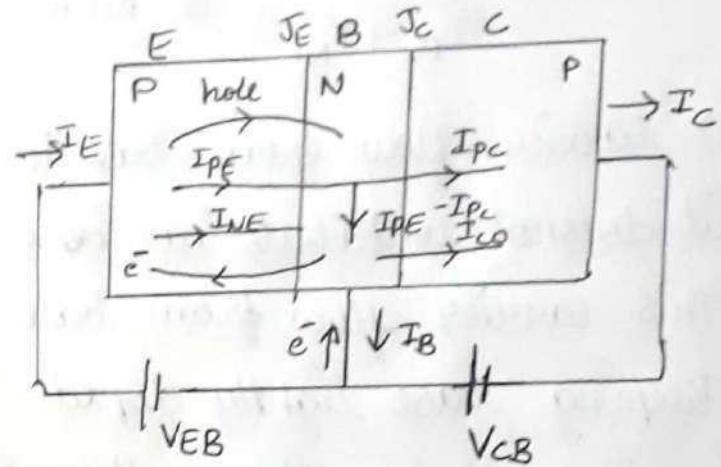
ii) Free e^- are injected from base to emitter which results in current I_{NE}

Total current through emitter junction $I_E = I_{PE} + I_{NE}$

∴ Emitter is heavily doped, hole flow will be much greater than e^- flow i.e. $I_{PE} \gg I_{NE}$

$$I_E \approx I_{PE}$$

Current through emitter junction is mainly due to the carriers of emitter



Emitter Injection Efficiency: It is the ratio of current through emitter junction due to carriers injected by Emitter and total current through emitter junction.

$$\gamma = \frac{I_{PE}}{I_E} = \frac{I_{PE}}{I_{PE} + I_{NE}} \quad (\text{for PNP}) \quad I_{DE} \ggg I_{NE}$$

$$\gamma = \frac{I_{NE}}{I_{PE} + I_{NE}} \quad (\text{for NPN}) \quad \gamma = \frac{I_{PE}}{I_{PE}} = 1$$

$$\boxed{\gamma = 1}$$

- carrier flow from base to emitter is undesired because it does not contribute carriers which can reach collector. This carrier flow from base to emitter is minimised by keeping base lightly doped.
- Injected holes diffuse through base region and a few of them recombine with electrons of base. Remaining holes cross collector junction in the form of current I_{PC} .
- Reverse voltage V_{CB} does not oppose hole flow from base to collector because holes are minority carriers with respect to base.

Base Transport Factor (β^*): It is measure of how efficiently injected carriers are transported through base to the collector.

$$\boxed{\beta^* = \frac{I_{PC}}{I_{PE}}}$$

$$I_{PC} \approx I_{PE}$$

$$\boxed{\beta^* = 1}$$

- when recombinations occur base region loses, its e^- , and thereby it may get positively charged and it can oppose hole flow from emitter to collector.

→ Hence base region must be kept electrically neutral by providing compensating e^- to base from external supply. These compensating e^- result in a current ($I_{PE} - I_{PC}$) It is called recombination current $I_B \cong I_{PE} - I_{PC}$

- If electron supply to base is increased, base becomes negatively charged due to excess e^- and thereby it attracts greater no. of holes from emitter. Thus hole flow from emitter to collector increases
- If electron supply to base is reduced then base becomes positively charged due to electron deficiency, and thereby it attracts less no. of holes from the emitter. Thus hole flow from emitter to collector decreases
- Thus base current or electron supply to base will control carrier flow from emitter to collector
- Due to reverse biased V_{CB} , reverse saturation current I_{CO} also flows through collector junction.

Total current through collector junction (I_c) is

$$I_c = I_{PC} + I_{CO} \quad I_{PC} : \text{due to majority carriers at emitter}$$

I_{CO} : due to minority carriers of collector and base

signal current gain (α): It is the ratio of change in collector current to change in emitter current when BJT operation changes from cut-off to active mode

i.e.
$$\alpha = \frac{\Delta I_c}{\Delta I_E}$$

→ In cut-off mode : $I_E = 0$, $I_C = I_{CO}$ $\Delta I_C = I_{PC} + I_{CO} - I_{CO} \quad (6)$
 active mode : $I_E \neq 0$, $I_C = I_{PC} + I_{CO}$ $= I_{PC}$
 $\Delta I_E = I_E - 0 = I_E$

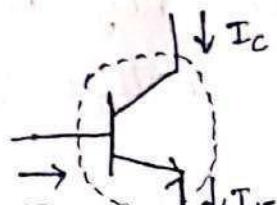
$$\alpha = \frac{I_{PC}}{I_E} \quad \alpha = \frac{I_{PC}}{I_{PE}} \times \frac{I_{PE}}{I_E} = B^* \times r \quad i.e. \alpha = B^* \cdot r$$

$$\because \beta^* = 1 \text{ & } r \approx 1 \Rightarrow \alpha \approx 1$$

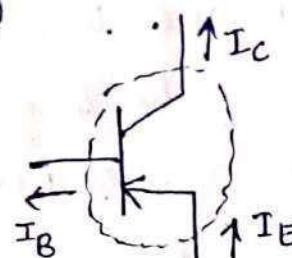
In active mode : $I_C = I_{PC} + I_{CO}$ ($\because I_{PC} = \alpha I_E$)

$$I_C = \alpha I_E + I_{CO} \quad (I_C \text{ in terms of } I_E) \quad (1)$$

symbol :



(NPN)



(PNP)

$$I_E = I_B + I_C \quad (2)$$

Combining ① & ② we get, $I_C = \alpha(I_B + I_C) + I_D$

$$I_C(1-\alpha) = \alpha I_B + I_{CO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CO} \quad (3)$$

$$\text{let } \frac{\alpha}{1-\alpha} = \beta, \text{ then } 1+\beta = 1 + \frac{\alpha}{1-\alpha} = \frac{1}{1-\alpha}$$

$$\text{Eq ③ becomes } I_C = \beta I_B + (1+\beta) I_{CO} \quad (4)$$

→ α and β are large signal current gains for common base and common emitter configurations

$$\beta = \frac{\alpha}{1-\alpha} \quad \text{and} \quad \alpha = \frac{\beta}{1+\beta}$$

→ B is a measure of amplification ability of BJT

→ A higher B indicates better amplification

If $\alpha \rightarrow 1$, $B \rightarrow \infty$

→ $\alpha \rightarrow 1$ when:

1) If emitter doping much greater than base doping

i.e. ($N_E \gg N_B$), then $\beta \rightarrow 1$

2) If $w_B \ll L_B$ then B^* approaches 1

NOTE: B value depends upon emitter doping (N_E), base do-

-g (N_B) and base width (w_B) If $N_E \uparrow \Rightarrow B \uparrow$ & $N_B \uparrow = B \downarrow$

I_{CBO} : It is the collector current when emitter doping (N_E) is open circuited

If $w_B \uparrow \Rightarrow B \downarrow$

$$I_{CBO} = I_c / I_{E=0}$$

$$* I_{CBO} = I_{CO}$$

I_{CEO} : It is the collector current when base is open circuited.

$$I_{CEO} = I_c / I_{B=0} \Rightarrow I_{CEO} = (1+B)I_{CO} = \frac{I_{CO}}{1-\alpha}$$

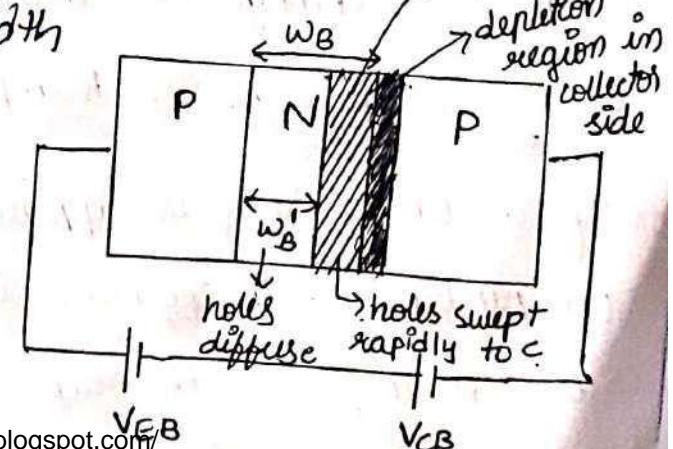
Early Effect or Base Width Modulation:

→ It refers to decrease in effective base width due to increase in reverse voltage of collector junction

w_B : physical or geometrical base width

w'_B : effective base width

→ If reverse voltage V_{CB} is ↑ then depletion width of collector junction increases



(8)

→ Since base is lightly doped, depletion region penetrates more into base and hence effective base width becomes smaller

Consequences of early effect:

Early effect has three consequences

1) α increases: If $V_{CB} (\uparrow) \rightarrow$ effective base width $(\downarrow) \rightarrow$ No of recombination inside base

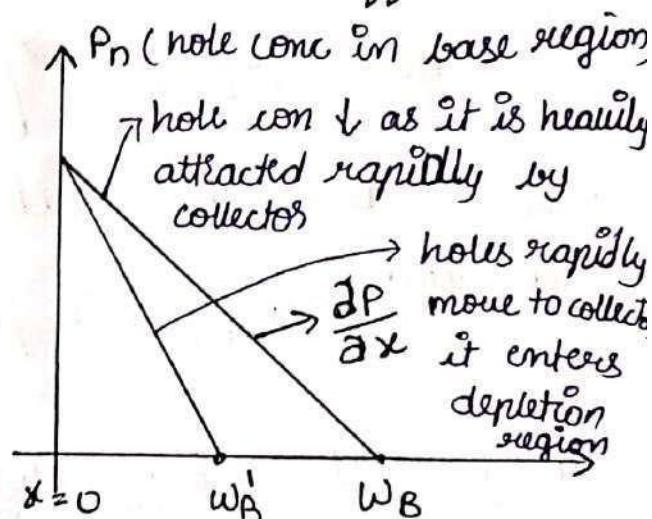
$$\alpha \uparrow \leftarrow \beta^* \uparrow \leftarrow (\downarrow)$$

→ increases by small amount but β increases by large amount

2) I_E increases: $I_E \approx I_{PE}$ which is a hole diffusion current $I_{PE} \propto \frac{\partial P}{\partial x}$ or $\frac{\Delta P}{\Delta x}$

→ If $V_{CB} (\uparrow) \rightarrow$ effective base width (\downarrow)

$$I_E (\uparrow) \leftarrow I_{PE} (\uparrow) \leftarrow \frac{\partial P}{\partial x} (\uparrow) \leftarrow$$



→ J_E and J_c are called interacting junctions because a change in voltage across one junction causes a change in the current through other junction

3) Punch through (or) Reach through can occur

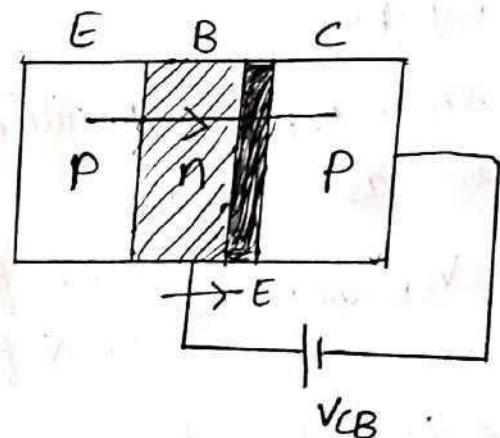
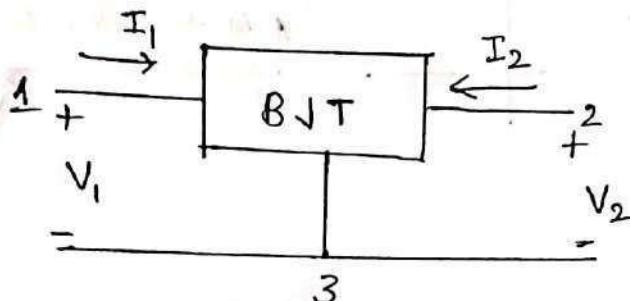
→ If a large V_{CB} is applied then depletion region will fully occupy base and effective base width becomes zero. This is called punch through and corresponding V_{CB} is called

(4)

~~punch~~ punch through voltage.

→ When punch through occurs, collector and emitter get electrically shorted. As collector is at negative potential, it attracts large no. of holes from emitter. Hence a heavy current flows and damage can occur to BJT

BJT Characteristics:



→ I_1 = Input current, I_2 = Output current

V_1 = Input voltage, V_2 = output voltage

→ I_1 , I_2 , V_1 and V_2 are inter-dependent they vary with respect to each other. Their inter-dependence is represented through V-I plots which are called as BJT characteristics

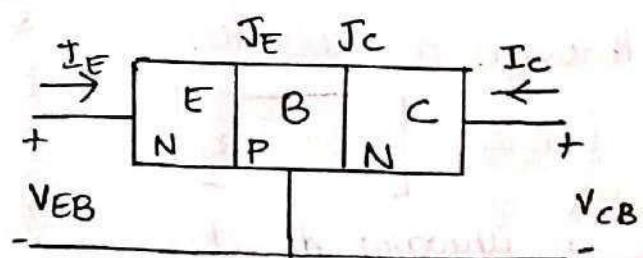
Input characteristics: It is a plot of input current vs input voltage when output voltage is kept constant

Output characteristics: It is a plot of output current vs output voltage when input current is kept constant.

Common Base Configuration

• Input characteristics

I_E vs V_{EB} when V_{CB} is kept constant.



I_E = current through emitter junction

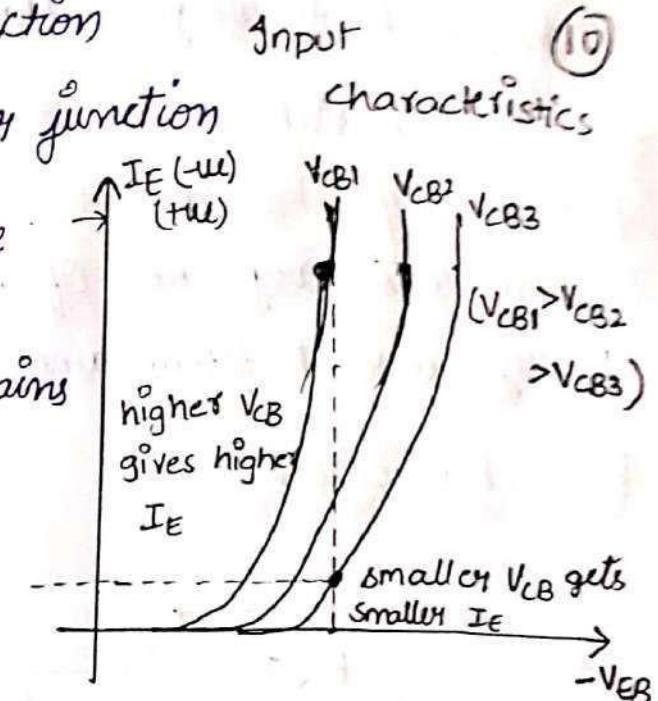
V_{EB} = Forward voltage across emitter junction

I_E Vs V_{EB} plot is identical to diode characteristics

→ For small values of V_{EB} , I_E remains negligible

→ When V_{EB} exceeds cutting voltage I_E increases rapidly

$$V_{EB(\text{cutin})} \begin{cases} -0.6V & \text{for Si} \\ -0.1V & \text{for Ge} \end{cases}$$



→ I_E depends upon V_{CB} also due to early effect. Greater V_{CB} results in greater I_E

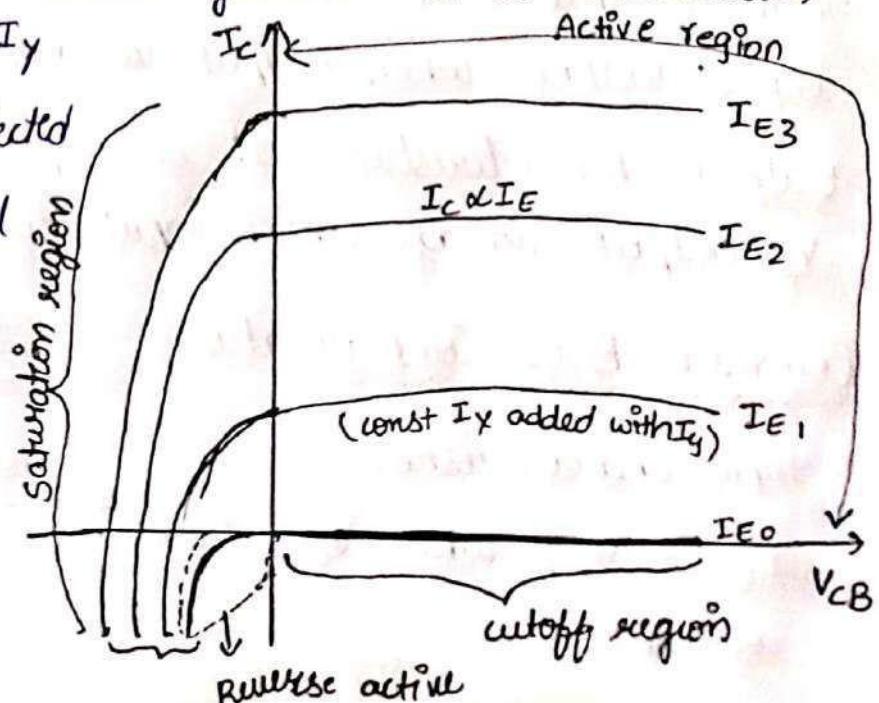
→ Output characteristics is a plot of I_C vs V_{CB} when I_E is kept constant

→ $V_{CB} = \text{Voltage across } I_C \quad V_{CB} = +V_E \quad (V_{CB} > 0) \Rightarrow J_C \text{ is in R.B.}$

$V_{CB} = -V_E \quad (V_{CB} < 0) \Rightarrow J_C \text{ is in F.B.}$

→ I_C is current through collector junction. It is combination of 2 currents i.e., I_x and I_y

→ I_x = It flows when injected carriers of emitter travel through the collector junction $I_x \propto I_E$ in upward direction



Cut-off region: A region where I_C is negligible. It lies on $I_E = 0$ curve and to the right of the $V_{CB} = 0$

$$I_E = 0 \Rightarrow J_E \text{ is in R.B}$$

$$V_{CB} = 0 \Rightarrow J_C \text{ is in R.B}$$

} cut off mode

In cut-off mode, $I_E = 0$, $I_C = I_{CO}$, $I_B = -I_{CO}$

Saturation region: A region where I_C varies with V_{CB} . It lies above $I_E = 0$ curve and to the left of $V_{CB} = 0$.

$$I_E > 0 \Rightarrow J_E \text{ is in F.B}$$

$$V_{CB} < 0 \Rightarrow J_C \text{ is in F.B}$$

} saturation mode.

Active region: A region where I_C remains constant with respect to V_{CB} .

It lies above $I_E = 0$ curve and to right of $V_{CB} = 0$

$$I_E > 0 \Rightarrow J_E \text{ is in F.B}$$

$$V_{CB} > 0 \Rightarrow J_C \text{ is in R.B}$$

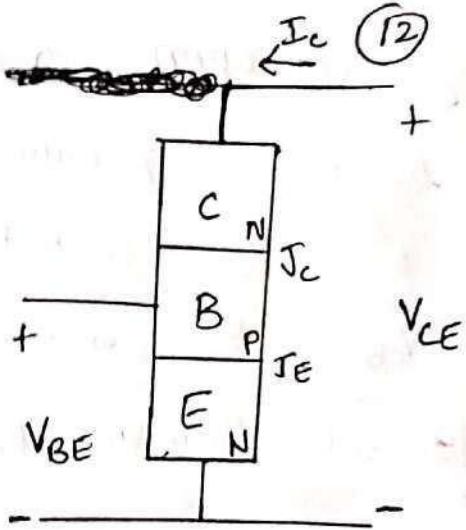
} active mode

In active region $I_C = \alpha I_E + I_{CO} \approx \alpha \cdot I_E$ (As I_E is kept const, I_C is also const)

→ When BJT is in active region,

output current I_C changes only with input current I_E . This property is necessary when BJT is used as amplifier

Common Emitter Configuration:



It is a plot of I_B Vs V_{BE} when

~~Because~~ V_{CE} is ~~const~~ const

$V_{BE} = \text{forward voltage of } J_E = +V_E = \text{NPN}$
 $\Rightarrow -V_E = \text{PNP}$

$$V_{BE} = -V_{EB}$$

I_B = recombination current

→ If V_{BE} is less than cutting voltage then emitter cannot inject carriers into base therefore no recombination occurs, hence I_B remains 0 or negligible

→ If V_{BE} exceeds cutting voltage then emitter injects carriers into base, a few recombinations occur and then I_B starts flowing.

→ Therefore I_B vs V_{BE} plot is similar to diode characteristic

$V_{BE}(\text{cutin})$:- It is V_{BE} value above which I_B starts flowing

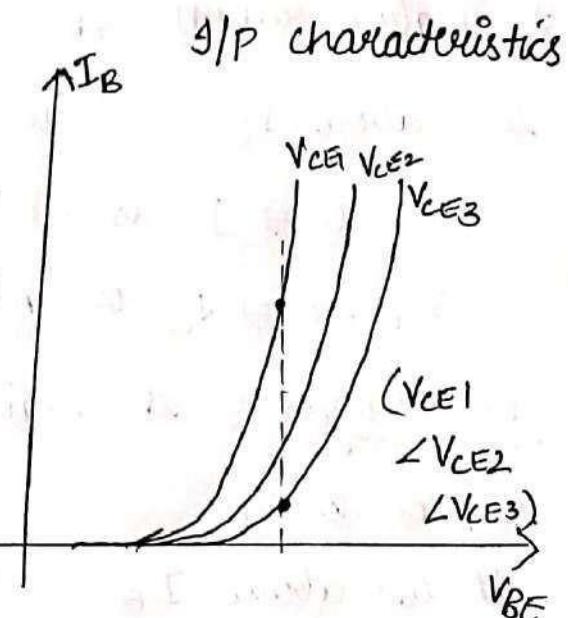
$$V_{BE}(\text{cutin}) \left. \begin{array}{l} \xrightarrow{\text{0.6V for Si}} \\ \xrightarrow{\text{0.1V for Ge}} \end{array} \right\} \text{NPN}$$

→ I_B depends upon V_{CE} also due to early effect.

→ Greater V_{CE} results in smaller I_B ; smaller V_{CE} produces higher I_B at constant V_{BE}

If $V_{CE} \uparrow = V_{CB} (\uparrow) \rightarrow \text{effective bandwidth} (\downarrow)$

$$\therefore V_{CB} = V_{CE} - V_{BE} \quad I_B (\downarrow) \leftarrow \text{Recombination} (\downarrow)$$



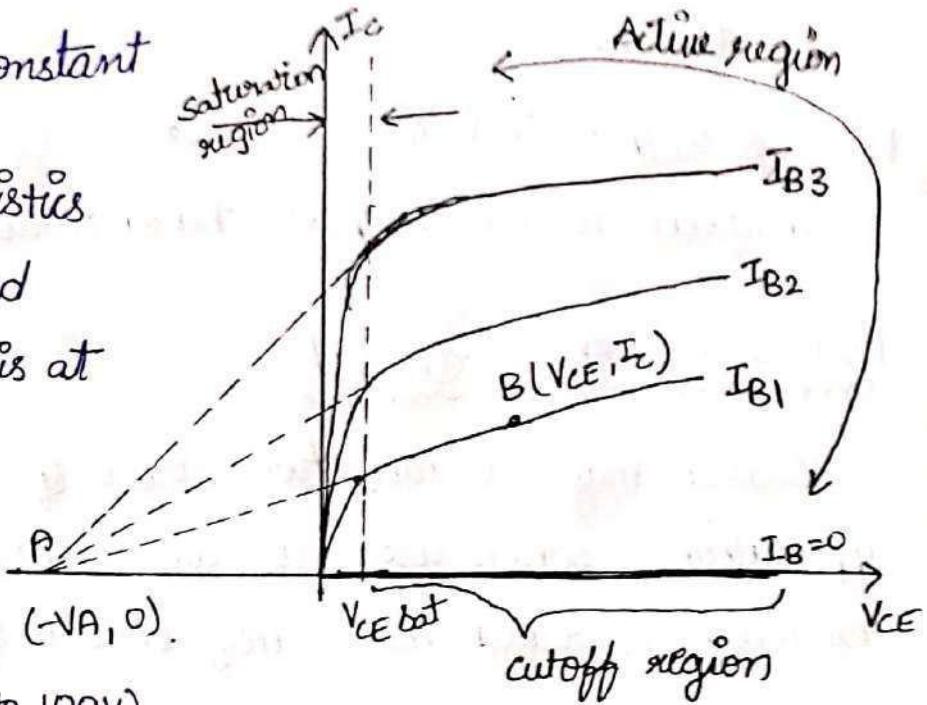
Output characteristics: It is a plot of I_C Vs (13)

V_{CE} when I_B is kept constant

→ If CE output characteristics are projected in backward direction, they cut V_{CE} axis at a common point $(-V_A, 0)$

where

V_A = early voltage. It lies in the range (50 to 100V)



Common Collector Configuration:

Input characteristics

It is a plot of I_B Vs. V_{BC} when V_{EC} is kept constant - Input characteristics

V_{BC} = Reverse Voltage of J_C

$V_{BC} = -V_E$ for NPN

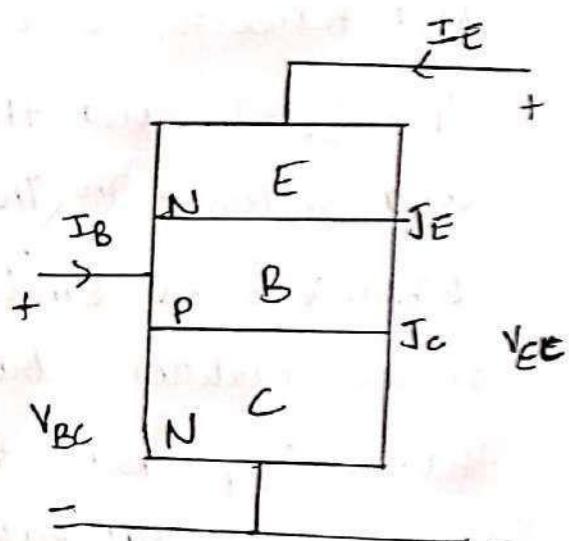
= $+V_E$ for PNP.

V_{EC} is negative for NPN

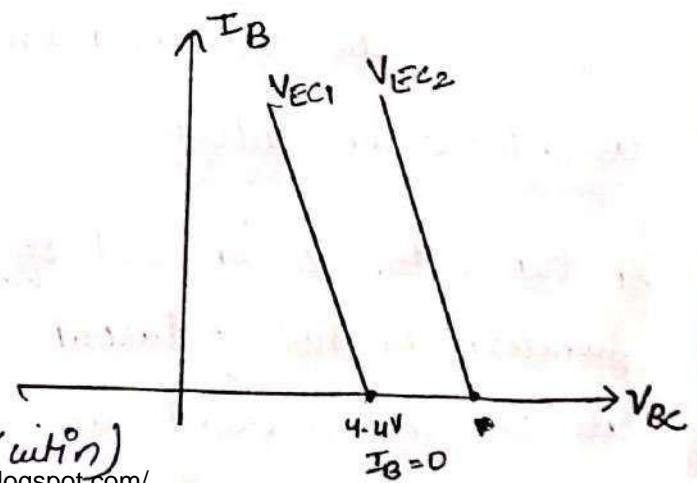
Let $V_{EC} = \text{const at } = -5V$,

$$V_{BE} = V_{BC} - V_{EC}$$

V_{BC}	V_{BE}
-4.3	+0.7
-4.35	0.65
-4.4	0.6 → V_{BE} (cut-off)
-4.45	0.55 → $I_B = 0, V_{BE} < V_{BE}$ (cut-off)



Input characteristics



→ when V_{BC} is increased, V_{BE} reduces and hence I_B decreases.

NOTE : output characteristics is I_E vs V_{EC} Net is identical to CE output characteristics (I_C vs V_{CE} Net)

Transistor As a Switch

→ Second major amplification area of BJT is switching applications. When used as an electronic switch, a BJT is normally operated alternately in cut-off and saturation.

→ When $V_i = 0$, emitter-base junction is reverse biased and transistor is in cut-off region. In this condition

$I_B = I_C = 0$ and there is open circuit between collector and emitter. This is illustrated in figure (a)

→ When $V_i = +V$, emitter-base junction is forward biased. In this condition, base current flows and it is greater than I_c^*/β , hence transistor is operated in saturation region. In saturation condition, voltage between collector and emitter, $V_{CE(sat)}$ is typically 0.2V. This voltage is too small and can be neglected to treat a short-circuit between collector and emitter. This is illustrated in fig(b)

Conditions in Cutoff:

A transistor is in cut-off region when the base-emitter junction is not forward-biased. Neglecting leakage current, all of the currents are zero, and V_{CE} is equal to V_{CC} .

$$V_{CE} (\text{cut off}) = V_{CC}$$

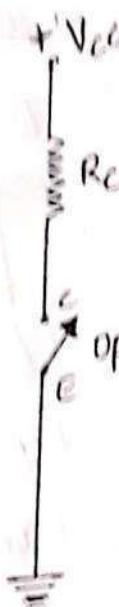
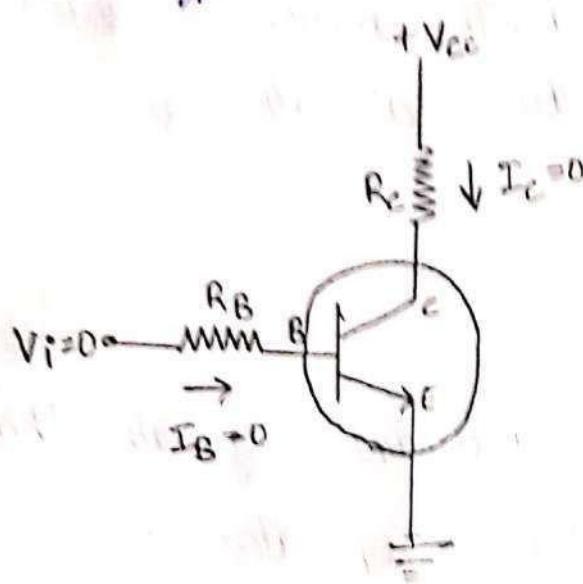


fig. a

a) operated in
cut-off (open
switch)

Conditions in Saturation

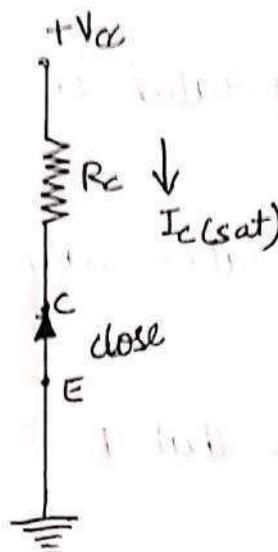
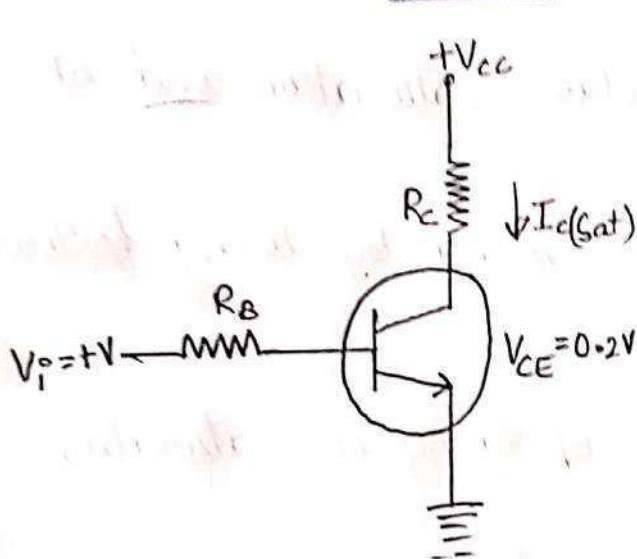


figure b

operated in
saturation
(closed switch)

→ when the base-emitter junction is forward-biased and there is enough base current to produce a maximum collector current, the transistor is saturated

The formula for collector saturation current is,

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

→ Since V_{CE} is very small compared to V_{CC} , it can usually be neglected. The minimum value of base current needed to produce saturation is

$$I_{B(\min)} = \frac{I_{C(sat)}}{\beta_{dc}}$$

Normally, I_B should be significantly greater than $I_{B(\min)}$ to ensure the transistor is operated in saturation region.

Region of operation

BJT can be operated in active, saturation and cut-off regions.

→ Region of operation can be found by using following method:

Step-1: Assume that BJT is operating in saturation region

Here $V_{CE} = V_{CE, \text{sat}}$

0.2V for Si^o

0.3V

0.1V for Ge

} for NPN

transistors

} for PNP

$V_{BE} = V_{BE, \text{sat}}$

0.8V for Si^o

0.3V for Ge

Step-2: Calculate I_B and I_C independently

all values are -ve

Step-3: calculate minimum base current needed to operate BJT in saturation

$$I_{B,\min} = \frac{I_{C,i\text{ sat}}}{\beta}$$

calculate from step-2

Step-4: Compare I_B and $I_{B,\min}$. If $I_B \geq I_{B,\min} = \text{BJT}$, in saturation region.

If $I_B < I_{B,\min} = \text{BJT}$ in active region

DC load line and operating point

→ DC load line is a straight line

plotted on I_C vs V_{CE} graph.

It is useful in graphical calculation

of V_{CE} and I_C in a given circuit

→ equation of DC load line is obtained

by applying KVL in collector loop

Applying KVL in collector loop.

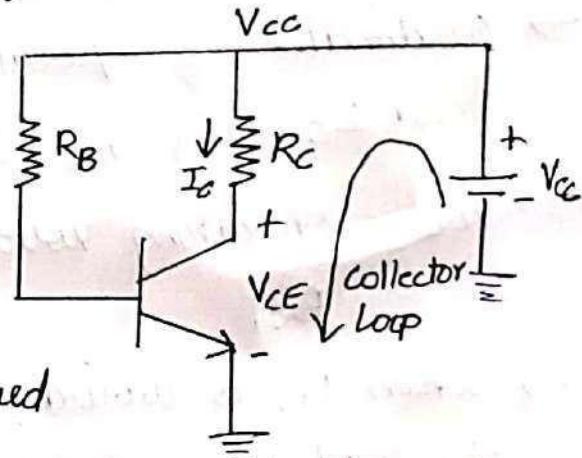
$$-V_{CC} + I_C R_C + V_{CE} = 0$$

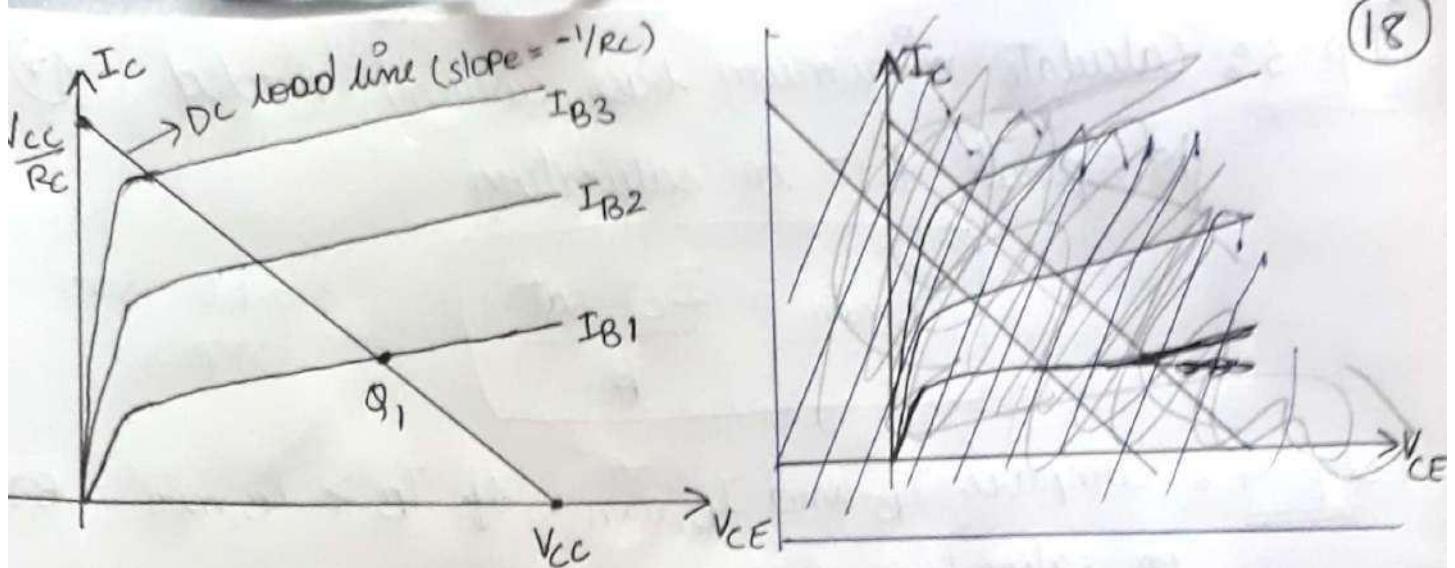
$$I_C R_C = -V_{CE} + V_{CC} \Rightarrow I_C = \frac{-1}{R_C} V_{CE} + \frac{V_{CC}}{R_C} \quad \text{---(1)}$$

$y = mx + c$ (eq ① is of this form)

Above eq ① represents straight line having slope $-\frac{1}{R_C}$ and y intercept $\frac{V_{CC}}{R_C}$. It is called DC load line

x intercept = V_{CC} [putting $I_C = 0$ in ①]





- For a given value of I_B , the point of intersection of characteristics curve and DC load line is known as operating point or quiescent point or Q point or bias point
- Coordinates of operating point are the DC values of V_{CE} and I_C i.e. $Q(V_{CE}, I_C)$
- $V_{CE} = \text{operating voltage}$ (and) $I_C = \text{operating current}$ of BJT
- When I_B is varied, operating point will keep moving on the load line. Hence load line is the locus of Q point
- If distortionless output is desired from a BJT amplifier, then Q point should be kept at the centre of the load line

Instability of ~~in~~ collector current:

$$\text{If we know } I_C = B I_B + (1+B) I_{C0}$$

I_C of BJT is unstable due to

3 reasons:

1) Variation in I_{C0} : Reverse saturation current of collector junction I_{C0} is temp dependent.

If $T \uparrow$ by 1°C then $I_{CO} \uparrow$ by 7°

$$\frac{\partial I_{CO}}{\partial T} = 7\% \text{ of } I_{CO} = 0.07 I_{CO}/^\circ\text{C}$$

Main factor of instability in I_c is variation in I_{CO}
This change in I_{CO} with respect to temp causes a change
in I_c .

2) Variation in V_{BE} : Forward voltage of emitter junction V_{BE} is also temp dependent. If $T \uparrow$ by 1°C then $V_{BE} \downarrow$ by 2.5 mV . This dependence of V_{BE} on temp causes a change in I_B

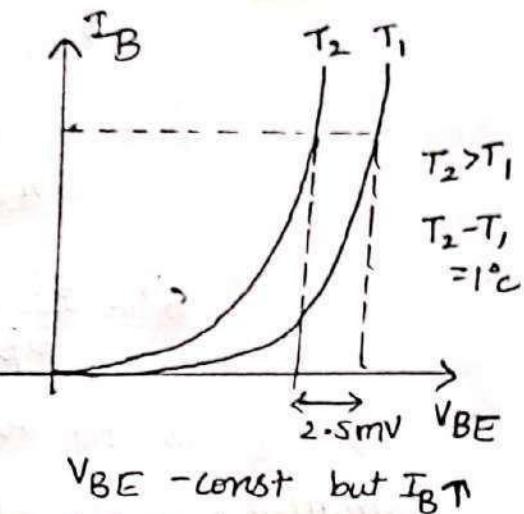
and hence I_c also changes $\frac{\partial V_{BE}}{\partial T} = -2.5\text{ mV}/^\circ\text{C}$

3) Variation in β : Common emitter current gain β , can vary due to transistor replacement and also due to change in temp If $T \uparrow \rightarrow \beta \uparrow$

Instability in I_c has 2 undesired effects:

- i) operating point or Q point becomes unstable i.e Q point may not remain at center of load line which causes distortion in the output signal of amplifier
 - ii) thermal runaway can occur which damages BJT
- hence I_c should be kept stable by using stabilization method and compensation method

$$I_c = f(I_{CO}, V_{BE}, \beta)$$



$$\Delta I_C \cong \frac{\partial I_C}{\partial I_{CO}} \cdot \Delta I_{CO} + \frac{\partial I_C}{\partial V_{BE}} \cdot \Delta V_{BE} + \frac{\partial I_C}{\partial B} \cdot \Delta B \quad (20)$$

$$\boxed{\Delta I_C \cong S \cdot \Delta I_{CO} + S' \Delta V_{BE} + S'' \Delta B}$$

where $S = \frac{\partial I_C}{\partial I_{CO}} = s_I$ = current stability factor

$S' = \frac{\partial I_C}{\partial V_{BE}} = s_V$ = voltage stability factor

$S'' = \frac{\partial I_C}{\partial B} = s_B$ = β stability factor

→ If I_C is to remain stable then ΔI_C should be smaller. Hence stability factors should be smaller.

Calculation of stability factor : (s)

It is the rate of change of I_C with respect to I_{CO}

$$S = \frac{\partial I_C}{\partial I_{CO}}$$

$$I_C = \beta I_B + (1+\beta) I_{CO} \cdot \text{differentiate w.r.t } I_C$$

$$1 = \beta \times \frac{\partial I_B}{\partial I_C} + (1+\beta) \cdot \frac{\partial I_{CO}}{\partial I_C}$$

$$1 - \beta \times \frac{\partial I_B}{\partial I_C} = (1+\beta) \frac{\partial I_{CO}}{\partial I_C}$$

$$\boxed{\frac{\partial I_C}{\partial I_{CO}} = S = \frac{1+\beta}{1-\beta} \frac{\partial I_B}{\partial I_C}}$$

For any BJT circuit, $\frac{\partial I_B}{\partial I_C}$ lies between 0 and -1.

Hence stability factor, $s = \frac{\partial I_C}{\partial I_B}$ lies between 1 and $1+\beta$.

∴ smaller s is desired, ideally $\boxed{s=1}$ *

Procedure to calculate 's':

Step-1: Apply KVL in a proper loop and obtain expression for I_B

Step-2: Differentiate above expression with respect to I_C and get $\frac{\partial I_B}{\partial I_C}$

Step-3: substitute $\frac{\partial I_B}{\partial I_C}$ in $s = \frac{1+\beta}{1-\beta \cdot \frac{\partial I_B}{\partial I_C}}$

BJT biasing:

Biasing refers to providing DC current and voltage to an electronic device to obtain desired functionality from the device

→ BJT is biased i) To operate BJT in active region so that it can be used as an amplifier.

ii) To keep collector current stable so that Q-point remains stable and thermal runaway does not occur.

BJT biasing methods:

i) Fixed bias circuit or base bias circuit

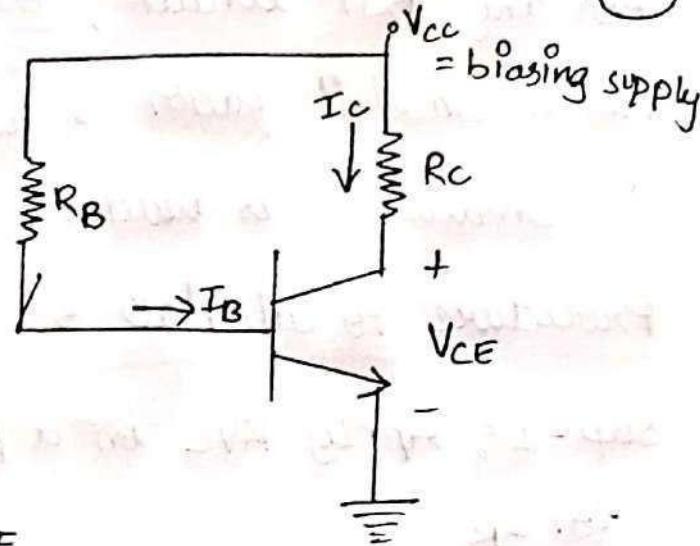
- V_{CC} : collector supply if $V_{CC} = 0$, BJT = off

- V_{CC} provides the necessary biasing currents and voltages to BJT. $V_{CC} = +ve$ for NPN, $V_{CC} = -ve$ for PNP

→ R_B is connected to provide base voltage and base current
 R_B also limits base current

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

I_B remains const
or fixed



$$V_{CE} = V_{CC} - I_C R_C$$

R_C controls V_{CE}

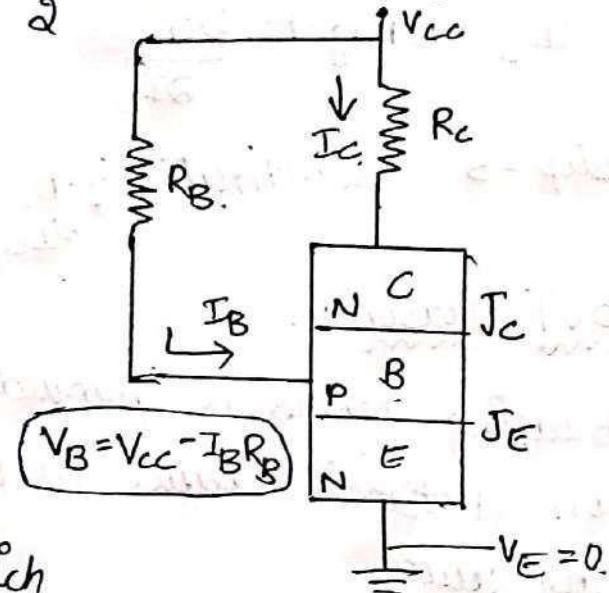
→ R_C is selected such that $V_{CE} = \frac{V_{CC}}{2}$ and thereby Q-point will be at the center of load line.

→ $V_B > V_E \Rightarrow J_E$ is in F.B

→ R_C is selected such that $V_C > V_B$

→ J_E is in R.B

→ Hence BJT is operated in Active region



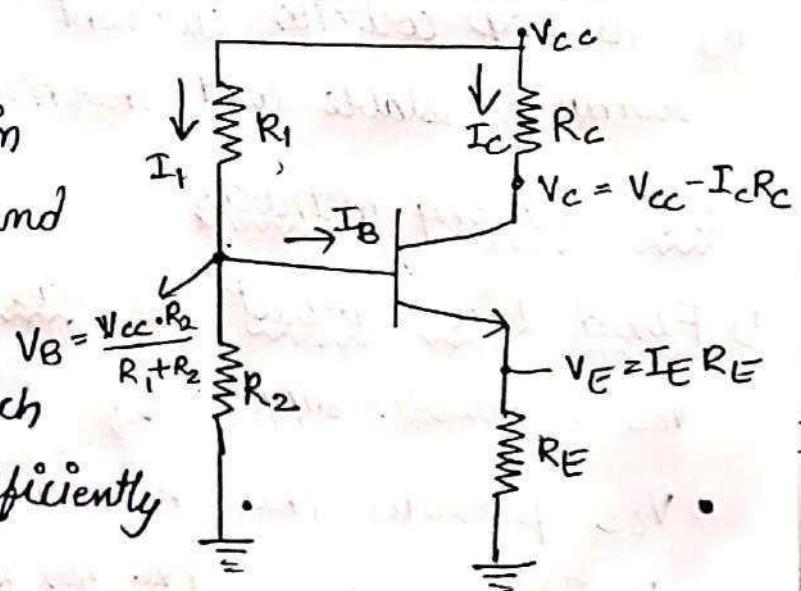
$$V_B = V_{CC} - I_B R_B$$

→ For fixed bias circuit $S = 1 + B$ which is the highest value. Hence I_C remains unstable

2) Self bias circuit or voltage divider bias circuit or Emitter bias circuit

→ R_1 and R_2 are effectively in series ($I_1 \gg I_B$). Hence R_1 and R_2 form voltage divider

→ R_1 and R_2 are selected such that V_B (Base voltage) is sufficiently greater than V_E .



$$V_B - V_E = 0.7 \text{ V for Si}$$

$$V_B - V_E = 0.2 \text{ V for Ge}$$

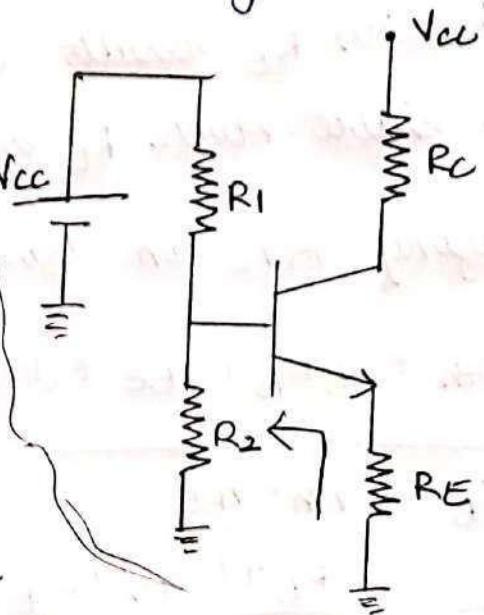
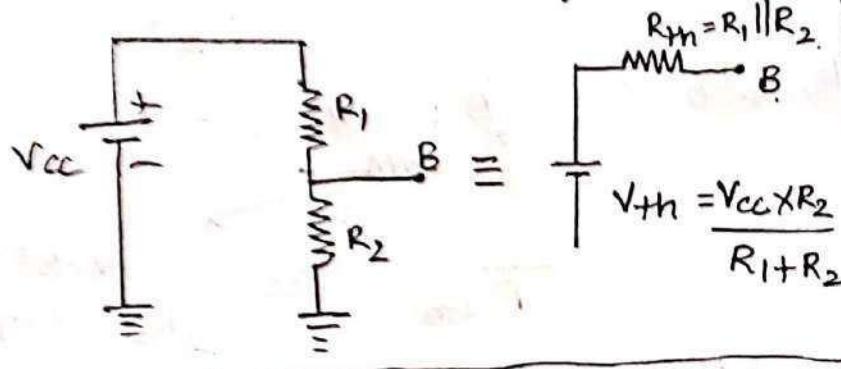
→ Hence emitter junction operates in F.B

→ R_C is selected such that $V_C > V_B$. Hence J_C operates in R_E , thereby BJT will operate in Active region

→ Self bias circuits can be

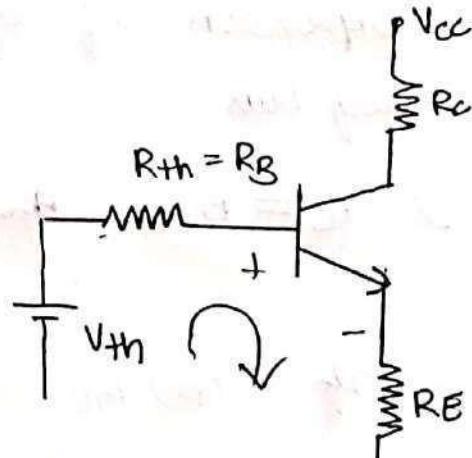
simplified by replacing R_1, R_2

Network with Thevenin equivalent



$$V_{th} = \frac{V_{cc} \times R_2}{R_1 + R_2} ; R_{th} = R_1 || R_2$$

$$S = \frac{1+B}{1+B R_E} \quad R_B = R_{th}$$



→ If R_E (\uparrow) or R_B (\downarrow) then $S \downarrow$ and hence I_C becomes more stable

(Simplified self bias circuit)

$$I_B = \frac{V_{th} - V_{BE}}{R_B + R_E} - \frac{I_C R_E}{R_B + R_E}$$

If $T \uparrow \rightarrow I_{CO} \uparrow \rightarrow I_C \uparrow \rightarrow \frac{I_C R_E}{R_B + R_E} \uparrow \rightarrow I_B \downarrow \rightarrow I_C \downarrow$
= stabilization method

NOTE :

- Increase and decrease in I_C will cancel each other. Hence I_C remains stable.
- Self bias circuit is also an example for stabilisation method. It is also called as negative feedback.
- Resistor R_E results in -ve feedback action which keeps I_C stable. Hence R_E is responsible for stability in I_C .

Applying KVL in base loop

$$-V_{th} + I_B R_B + V_{BE} + (1+B) I_B R_E = 0$$

$$1) I_B = \frac{V_{th} - V_{BE}}{R_B + (1+B) \cdot R_E}$$

Expression of base current in self bias

$$2) I_C \approx B I_B, \text{ then } = \frac{B(V_{th} - V_{BE})}{R_B + (1+B)R_E}$$

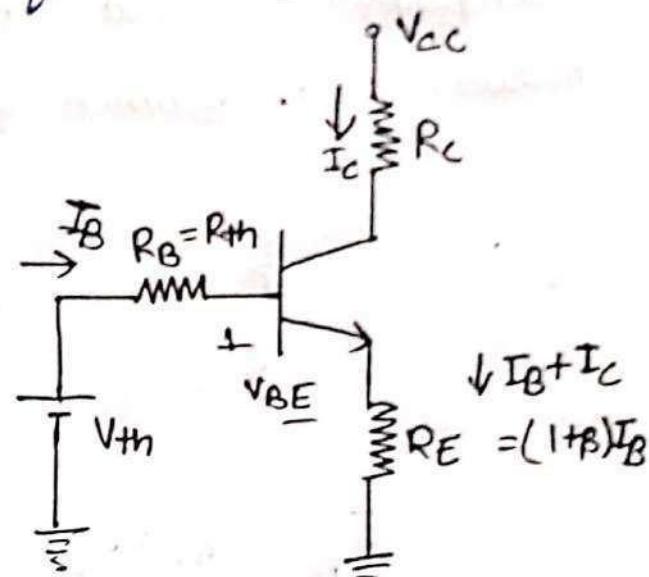
If $(1+B) R_E \gg R_B$, then

$$I_C = \frac{V_{th} - V_{BE}}{R_E}$$

→ Expression of I_C can be used if B is not provided or if B is large

→ I_C is independent of B , so B variation doesn't affect I_C

* Self bias circuits provides stable collector current irrespective of variations in temperature and B



$$3) V_{CE} = V_{CC} - I_C R_C - (I_B + I_C) R_E$$

$$V_{CE} \approx V_{CC} - I_C (R_C + R_E)$$

→ Expression for collector to emitter voltage.

$$4) S = \frac{1+B}{1+\frac{B R_E}{R_B + R_E}}$$

$$\text{where } R_B = R_{Th} = R_1 || R_2$$

$$= \frac{1+B(R_B + R_E)}{R_B + (1+B)R_E}$$

$$\text{If } (1+B) R_E \gg R_B$$

→ condition for stable I_C

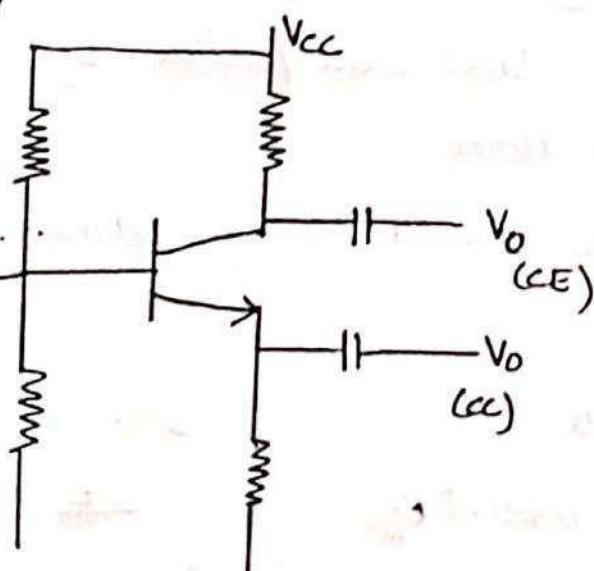
$$S \approx \frac{R_B + R_E}{R_E}$$

$$OR S \approx 1 + \frac{R_B}{R_E}$$

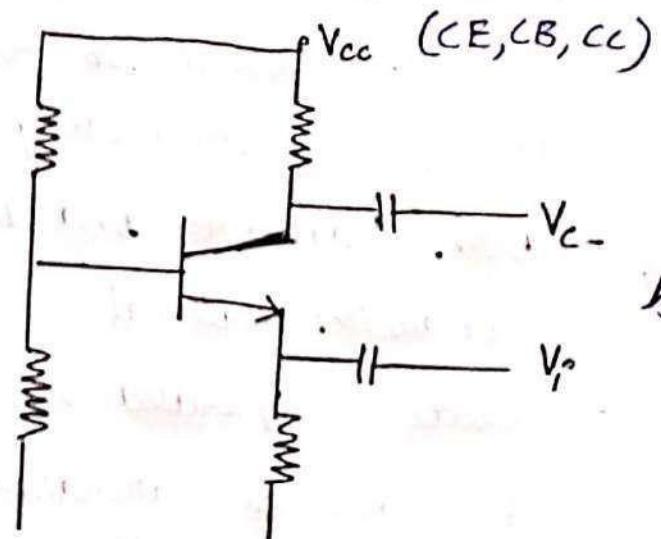
→ Expression for stability of B is unknown

Advantages of Self bias circuit

- 1) Smaller stability factor or excellent stability in I_C among all biasing circuits
- 2) Self bias circuit can be used for all BJT configurations.



(CE & CC)



(C.B)

(fixed bias and collector to base bias circuits can be used only for CE configuration)

Disadvantage of Self bias:

(26)

Resistor R_E causes negative feedback which reduces voltage gain.

Compensation Method:

It is a method of keeping I_C stable by connecting a temp dependent device such as diode, thermistor, and a varistor (temp coeff +ve) (temp coeff -ve)

- Thermistor and varistor are temperature dependent resistors
- Thermistor has -ve temp coefficient. i.e if $T \uparrow \rightarrow R \downarrow$
- Temperature coefficient $\frac{\Delta R}{\Delta T} = -\text{ve}$
- Varistor has +ve temp coefficient i.e if $T \uparrow \rightarrow R \uparrow$
temperature coefficient $\frac{\Delta R}{\Delta T} = +\text{ve}$

Diode Compensation for I_{CO} :

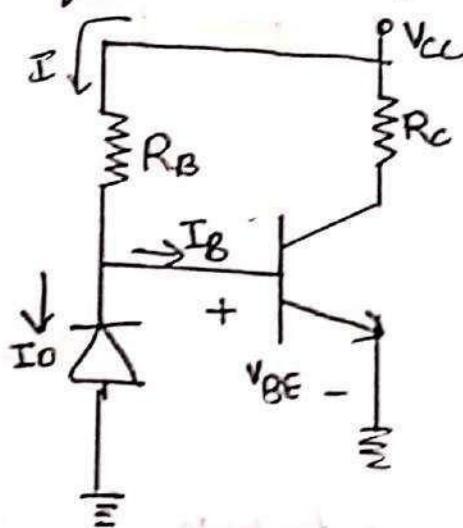
Collector current is kept stable irrespective of variations in I_{CO} by connecting a diode.

- Both transistor and diode should be of same semiconductor material

- Diode is operated in R.B

I_0 = Reverse saturation current of diode

$$I = \frac{V_{CC} - V_{BE}}{R_B} = \text{constant} \quad (I \text{ remains const})$$



Using KCL; $I = I_B + I_0$ or $I_B = I - I_0$ - (1)

$$I_C = \beta I_B + (1+\beta) I_{CO} \text{ or } I_C = \beta(I_B + I_{CO})$$

$$I_C = \beta(I - I_0 + I_{CO})$$

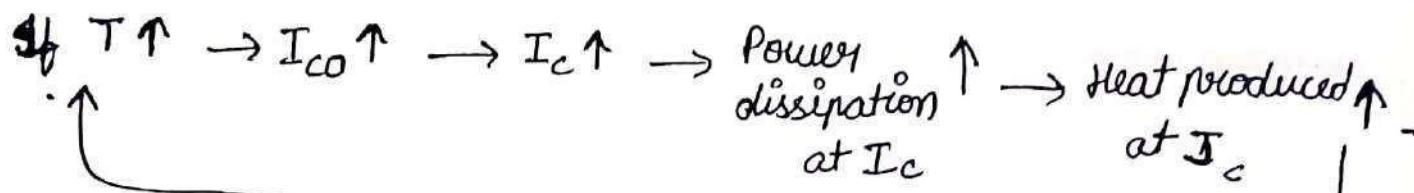
↓
reverse saturation current of diode

→ Reverse saturation current of I_C

- When temperature increases both I_0 and I_{CO} will increase. Increase in I_{CO} is approximately cancelled in I_0 . Hence I_C remains stable even if I_{CO} changes.

Thermal Runaway:

It is a process of self damage of BJT because of over heating at collector junction due to increase in I_c with I_{CO} .



- If above cycle repeats large no. of times then collector junction gets overheated, then damage occurs to BJT
- Thermal runaway occurs mostly in power transistors which operate at greater I_c and V_{CE} . (I_c will be few A;
 V_{CE} = tens of volt)
- It is also called secondary breakdown of BJT

Condition to prevent Thermal runaway:

Thermal runaway can be prevented if the rate at which heat is produced at T_c is less than the rate at which

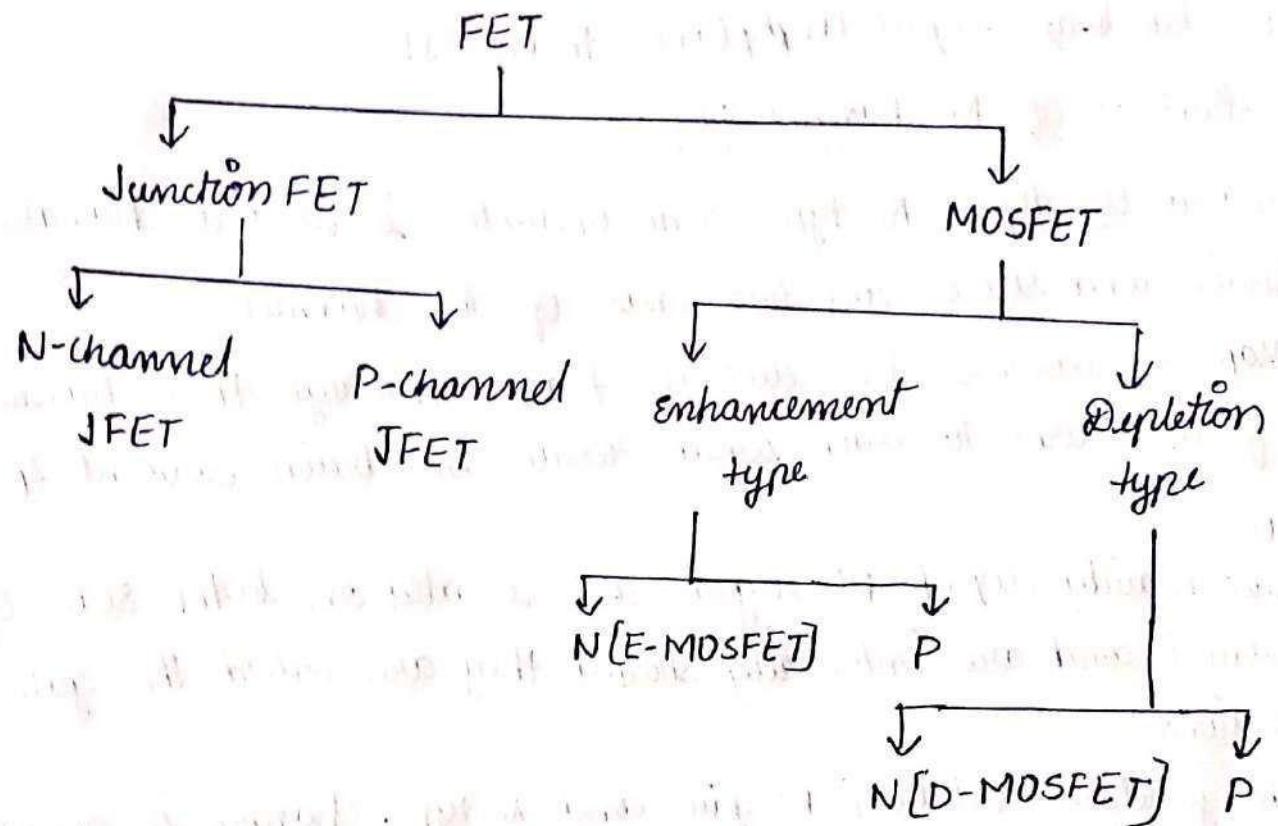
heat is dissipated or transferred to surrounding

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<https://intuhbtechadda.blogspot.com/>

UNIT-III. JUNCTION FIELD EFFECT TRANSISTOR (JFET)

- OR

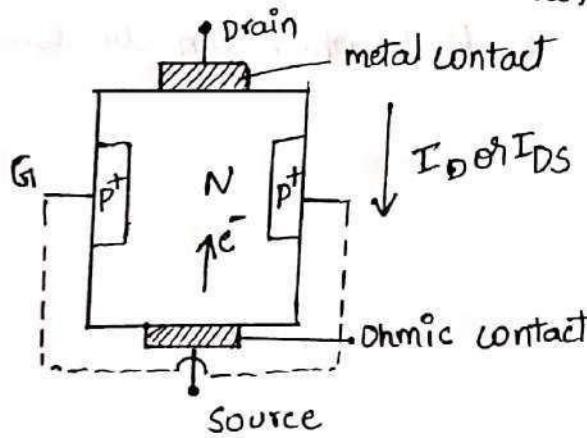


- FET is a semiconductor device as BJT which can be used as amplifier and switch
- 3-terminals of FET
 - (D) Drain - C
 - (S) Source - E
 - (G) Gate - B
- FET is a unipolar device because current flows due to only majority carriers
- FET is a voltage controlled device because the gate voltage controls the carrier flow from source to drain

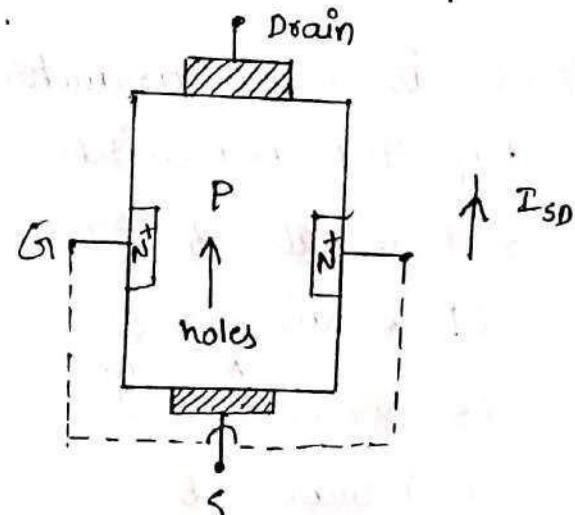
- The majority carriers drift through the channel due to electric field hence it is called Field Effect transistors
- Thermal Runaway cannot occur in FET because it is more temperature stable (independent of temp) than BJT
- FET has high input impedance than BJT

Construction of N-channel JFET:

- Moderately doped N-type semiconductor is used as channel
- Drain and source are two ends of the channel
- Majority carriers i.e., electrons travel through the channel from source to drain which results in drain current I_D or I_{DS}
- Two heavily doped p+ regions are created on both sides of channel and are internally shorted they are called the gate regions.
- The junction between p+ gate and n-type channel is operated in R.B to control the carrier flow.



N-channel JFET



- The proper operation of JFET requires the application of two voltages V_{DS} and V_{GS}
- V_{DS} is applied between drain and source so that majority carriers drift through the channel source to drain

thereby drain current flows through the channel

(3)

	N-channel	P-channel
V_{DS}	+ve	-ve
$(V_D - V_S)$

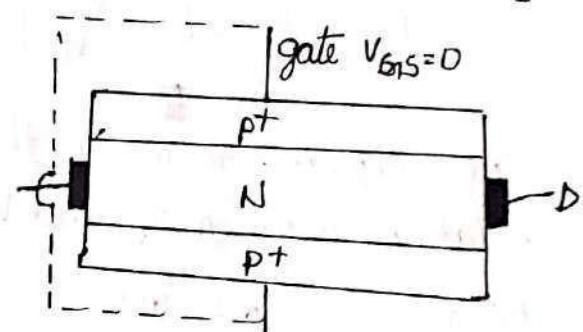
V_{GS}	-ve	+ve
----------	-----	-----

→ V_{GS} is applied between gate and source to operate the gate channel junction in R.B in order to control the carrier flow

Operation of N-Channel JFET

Case-1: Let V_{DS} is constant and V_{GS} is -ve from 0 to -ve

i) $V_{GS} = 0$ then full channel is available for conduction, hence maximum carrier flow occurs from source to drain. Hence, drain current is maximum.



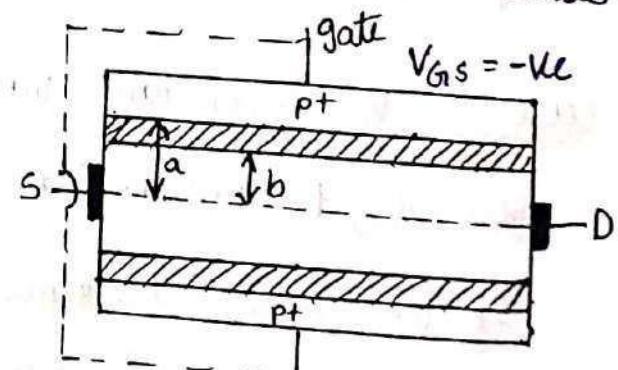
ii) When $V_{GS} = -ve$ gate-channel junction becomes reverse bias and depletion region is formed on the channel due to which effective channel width decreases and carrier flow from source to drain decreases thereby drain current decreases

a = half channel width

b = effective channel width

, $V_{GS} = -ve$, $V_{DS} = \text{constant}$

w = width of depletion



iii) when $V_{GS} = \text{strongly negative}$ then the depletion region completely occupies the channel and channel gets pinched off i.e. width of the depletion region is becoming

equal to channel width.

The voltage at which channel pinch off occurs and drain current becomes zero is called Pinch off voltage (or) (V_p) $V_{GDS}(\text{OFF})$

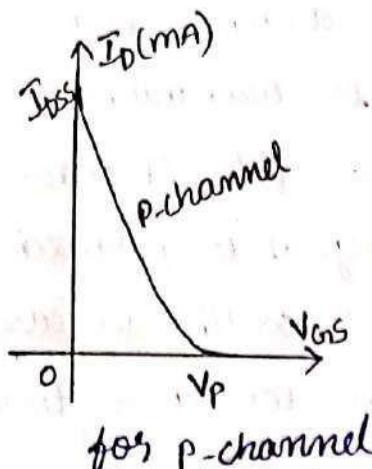
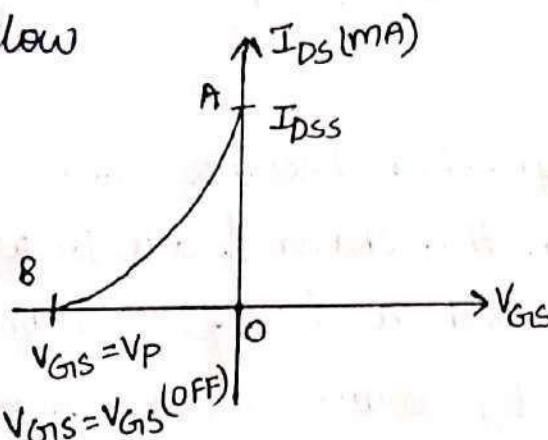
Transfer characteristics of N-channel JFET:

- 1) The relationship between drain current I_D and gate to source voltage V_{DS} is non-linear as shown in diagram
- 2) This relationship is defined by Shockley equation

$$I_{DS} = I_{DSS} \left[1 - \frac{V_{GDS}}{V_p} \right]^2$$

max I_D

- 3) The square term in the above equation results in non linear relation between I_D and V_{DS} producing a curve as shown below



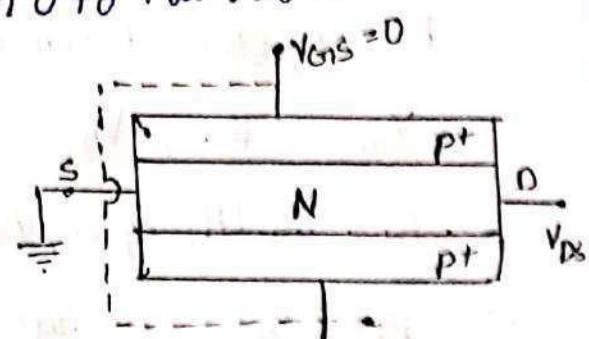
At A, $V_{GDS} = 0, I_D = I_{DSS}$
= max. drain current

At B, $V_{GDS} = V_p$
 $I_D = 0$, drain current = 0

Case-2: V_{GDS} = constant, vary V_{DS} from 0 to +ve values

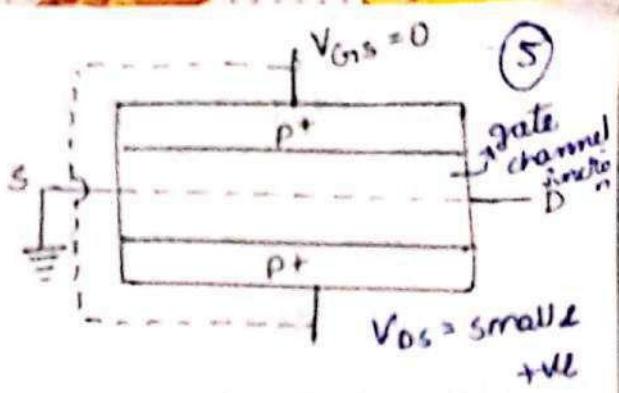
Let V_{GDS} be constant at 0V

- i) If $V_{DS} = 0$, I_D becomes zero due to there is no potential difference



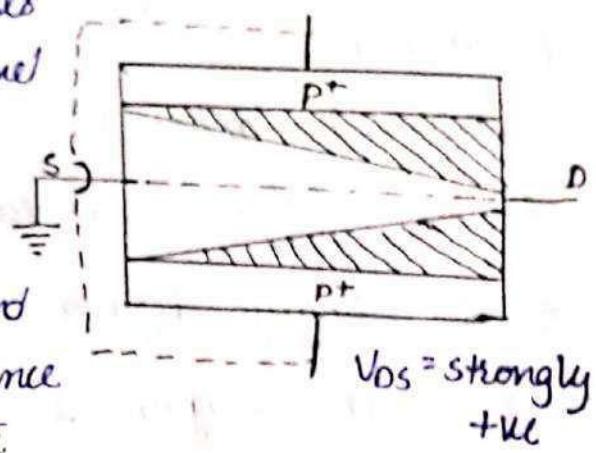
iii) If V_{DS} = small and constant

then I_D increases linearly with V_{DS} and channel resistance remains constant.



iv) If V_{DS} = strongly positive

then the the voltage of channel causes reverse biasing. ($V_N > V_D$) of gate-channel junction and depletion region has non uniform width and it is max at drain end and minimum at source end. Resistance of channel increases and hence drain current increases at slow rate.

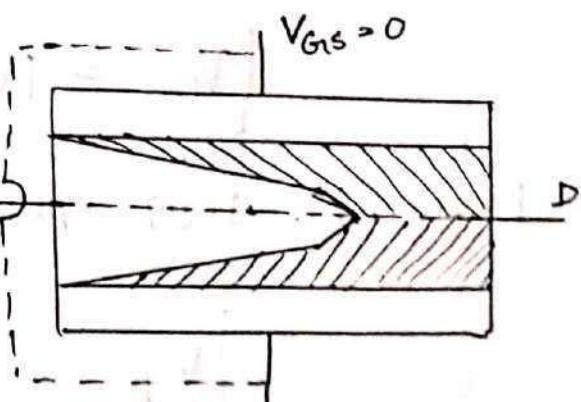


v) if $V_{DS} \geq |V_p| - |V_{GS}|$

channel pinch off occurs at drain end but channel is fully opened at source end therefore electrons keep flowing from source to drain and +ve voltage of drain will attract the electrons, therefore I_D does not become zero.

v) if $V_{DS} \geq |V_p| - |V_{GS}|$

channel pinch off occurs at small distance ΔL away from the drain. A very strong electric field will develop in ΔL distance. when e⁻ move through this ΔL distance s due to very high electric field.



[$> 10^4 \text{ MV/cm}$] the velocity of electrons becomes constant velocity saturation takes places. Hence drain current I_D becomes constant

$$E = \frac{V}{\Delta L}$$

Drain characteristics:

- FET acts as a constant current source
- Locus of pinch off point is parabola
- Drain characteristics is divided in two regions i) Linear ii) Saturation

Linear / Ohmic Region:

- It is the region in drain characteristics where drain current increases linearly with V_{DS}
- In this region FET acts as resistor and it follows ohm's law ($V = IR$)

Saturation / Pinch off Region:

- It is the region in drain characteristics curve where the drain current remains constant with respect to V_{DS}
- N-channel JFET operates in saturation when

$$V_{DS} \geq |V_p| - |V_{GS}|$$

P-channel JFET operates in saturation

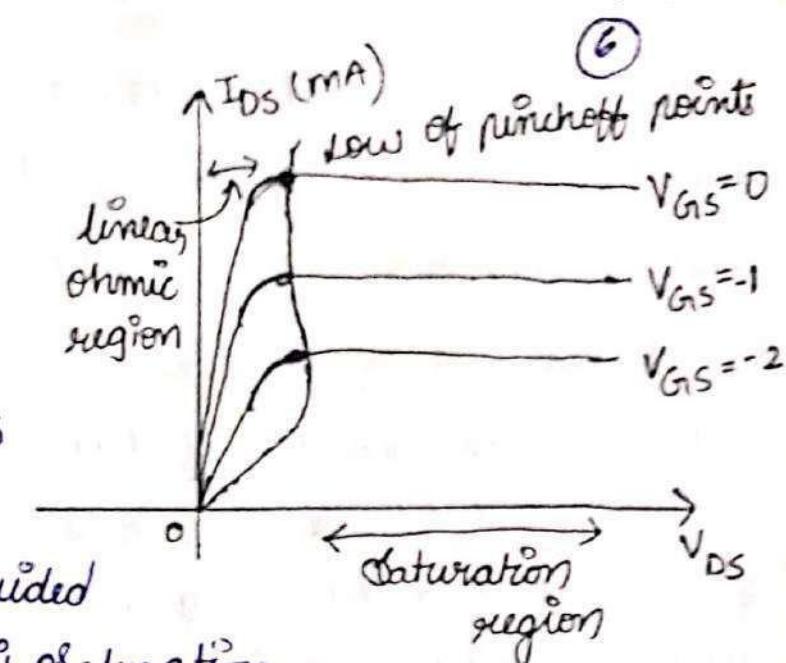
$$V_{SD} \geq V_p - V_{GS}$$

$$V_{DS} = -ve$$

$$V_{DS} - V_S = -ve$$

$$V_{SD} = +ve$$

$$V_D < V_S$$



7

→ In saturation region FET acts as constant current source with respect of V_{DS}

→ In saturation region FET acts as a voltage dependent current source with respect V_{GS}

$$I_{DS} = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

→ FET is used as an amplifier in saturation region because a small change in V_{GS} creates a large changes in I_D (P drain) (O/P) current.

→ FET acts as switch

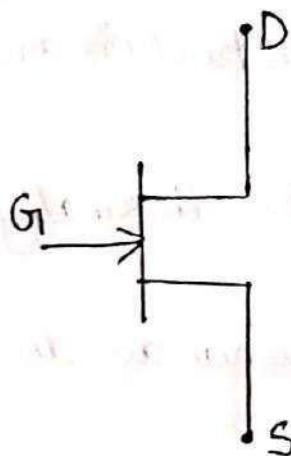
when $V_{GS} = 0$, $I_{DS} = I_{DSS}$, = ON

$V_{GS} = V_P$, $I_{DS} = 0$ = OFF

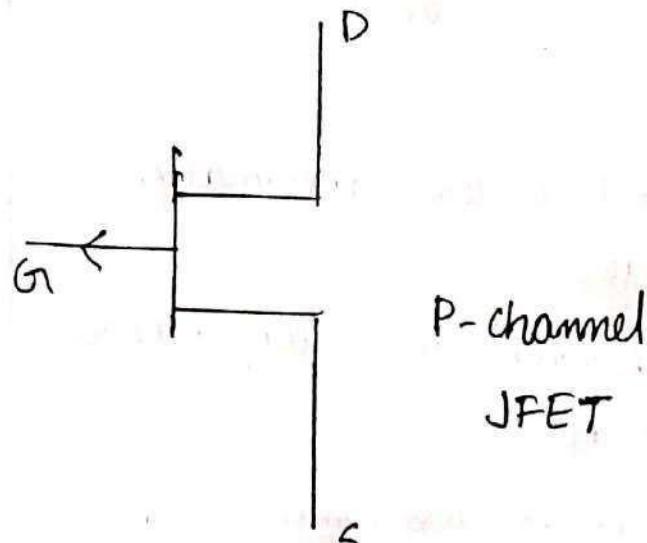
Application of JFET

- 1) FET is used as voltage dependent resistor in linear region
- 2) It is used as amplifier in saturation region.
- 3) It can be used as switch

Symbol:



N-channel JFET

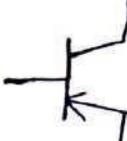
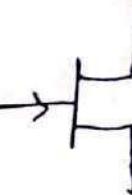


P-channel

JFET

Comparision between BJT and FET

(8)

BJT	FET
1) Current controlled device	1) Voltage controlled device
2) Bipolar	2) Unipolar
3) BJT is bipolar because current flows due to both majority and minority	3) FET is unipolar because current flows due to only majority
4) BJT is of 2 types i) NPN ii) PNP	4) FET is of 2 types i) N-channel ii) P-type
5)  	5)  
6) BJT has 3 configurations i) CB ii) CC iii) CE	6) FET has 3 configuration i) CS ii) CD iii) CG
7) Less S/I/P impedance compare to FET	7) FET has high impedance
8) BJT is bigger in size than FET	8) FET is smaller in size, small in construction and used in IC's
9) BJT is less thermally stable	9) FET is more thermally stable
10) Thermal runaway occurs in BJT	10) Thermal runaway does not exist
11) BJT is less expensive	

1) BJT is less immune to noise i.e. it is highly effected by noise

$$12) I_C = \beta I_B, \text{ linear}$$

1) FET is more immune to noise i.e. it is less effected to noise

$$12) I_{DS} = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

nonlinear

Biasing of FET:

- 1) Gate bias
- 2) Source self bias
- 3) Voltage divider bias

Biasing is used in order to keep the drain current (I_{DS}) stable and to operate FET or FET in saturation region so that we can use as amplifier

BJT - to keep I_C constant and keep in active region (amplifier)

1) Gate Bias

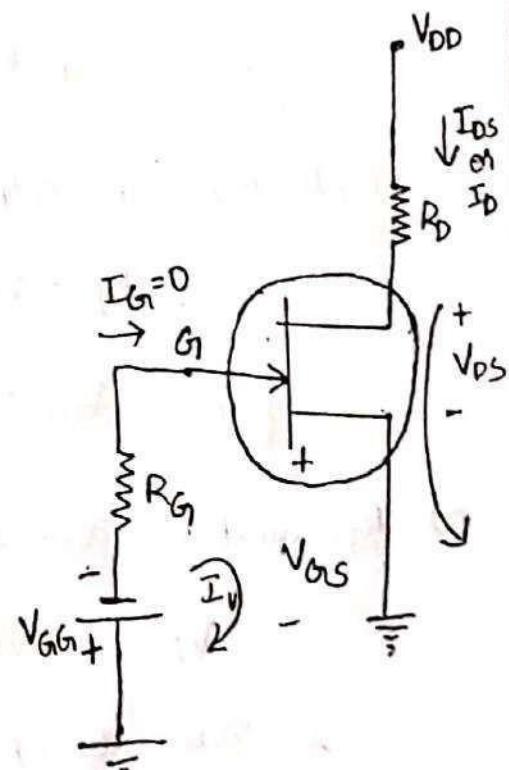
→ Here V_{DD} is biasing supply and V_{GGS} is another biasing supply

used to R.B the gate channel junction hence $I_{G1} = 0$ [only majority carriers so no reverse saturation current]

* Apply KVL in Loop 1 [Input loop]

$$-V_{GGS} - I_{G1}R_{G1} - V_{GS} = 0$$

$$V_{GS} = -V_{GGS} \quad \text{--- (1)}$$



→ Apply KVL in output loop

$$V_{DD} - I_{DS} R_D - V_{DS} = 0$$

$$V_{DS} = V_{DD} - I_D R_D \quad \rightarrow ②$$

$$V_{DS} \geq |V_P| - |V_{G_S}|$$

R_D is selected in such a way that hence JFET will be operated in saturation region and used as Amplifier.

Because of we are using two biasing supply it is so expensive so we go for source self

2) Source self bias :

→ In source self bias the voltage drop across ' R_s ' is used to R.B. the gate channel junction

→ Apply KVL in input loop

$$-V_{G_S} - I_{DS} R_S = 0$$

$$V_{G_S} = -I_{DS} R_S \quad \rightarrow ①$$

→ Apply KVL in output loop

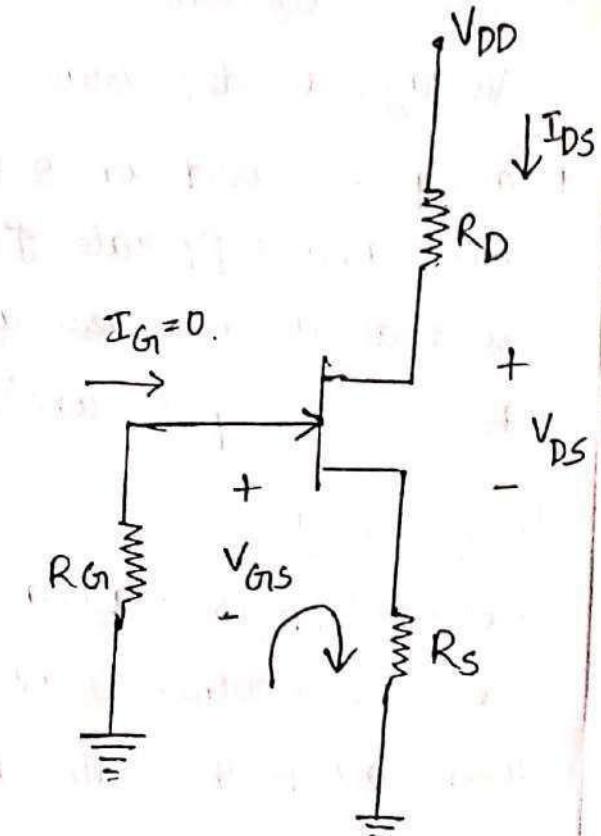
$$V_{DD} - I_{DS} R_D - V_{DS} - I_{DS} R_S = 0$$

$$V_{DS} = V_{DD} - I_{DS} (R_D + R_S)$$

→ R_D and R_S are selected in such a way that

$$V_{DS} > |V_P| - |V_{G_S}|$$

in order to operate in saturation



→ And R_s is used as Negative feedback [self correction] increase in one quantity decrease in other quantity so that it will be constant

Advantages:

- 1) No separate biasing is required to R.B the gate-channel
- 2) R_s helps to keep I_{DS} stable through the process of Negative feedback

i.e., $I_{DS} \uparrow$

$$V_{GS} = -I_{DS} \cdot R_s$$

The voltage drop across R_s increases hence $V_{GS} \uparrow$ and becomes more negative. When R.B increases [$V_{GS} \uparrow$] the depletion region increases and width of the channel decreases. Hence the flow of current decreases.

→ Increase in I_{DS} gets cancelled by decrease in I_{DS} this is called as Negative feedback.

Zener diode

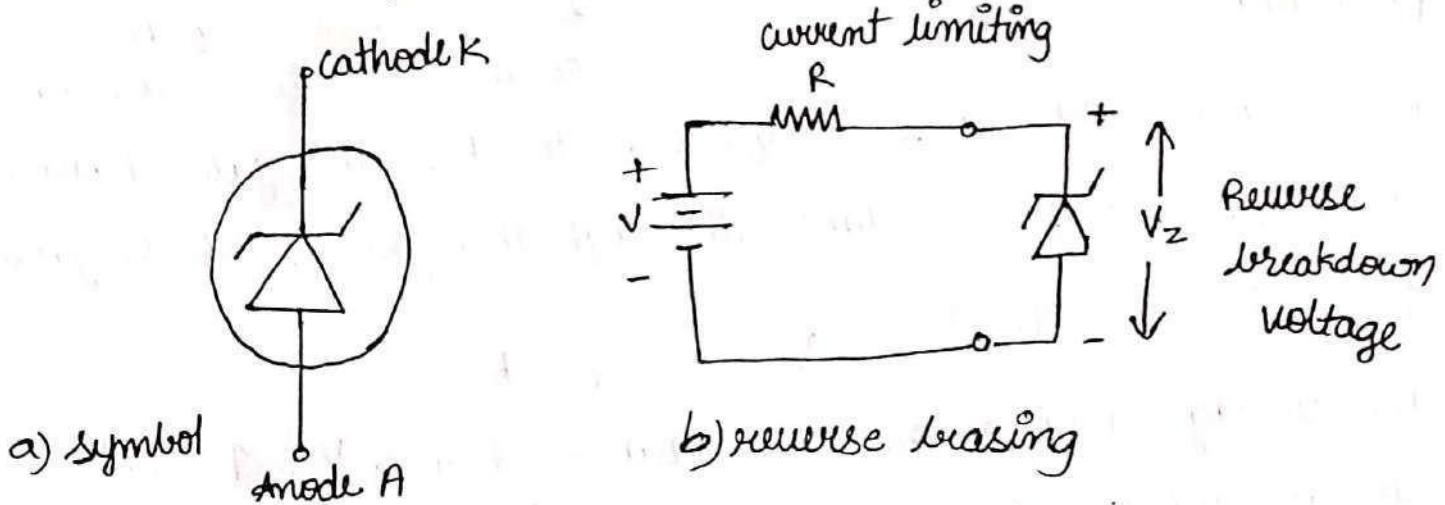
A zener diode is a silicon $p-n$ junction semiconductor device which is operated in its reverse breakdown region.

→ The zener diodes are fabricated with precise breakdown voltages by controlling the doping level during manufacturing.

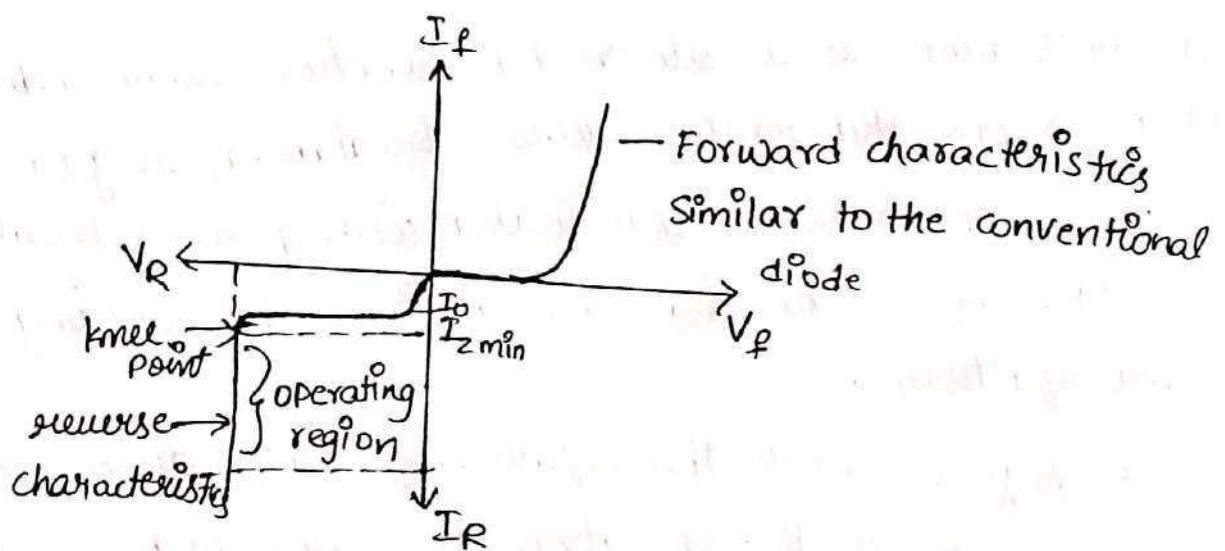
→ The figure shows the symbol of zener diode while the figure shows the operation of zener diode in reverse breakdown region

→ When the reverse voltage is applied to zener diode, at a certain ~~at~~ reverse voltage, the reverse breakdown occurs and current in the zener diode increases rapidly.

The sharp change in zener current is called knee. (12)
Or zener knee of the reverse characteristics



- The reverse bias voltage at which the breakdown occurs is called zener breakdown voltage, denoted as V_z . This value is carefully designed by controlling the doping level during manufacturing.
- The V-I characteristics of zener diode is shown in figure



- For zener diodes, practically two currents are specified. The $I_{z\min}$ is minimum current through the zener diode to maintain its reverse breakdown operation.
- The $I_{z\max}$ is the max current which zener diode can take safely maintaining its reverse breakdown operation.
i.e. constant V_z across it

Zener Diode as a Voltage Regulator

(13)

→ As long as current through the zener diode is between

$I_{Z, \min}$ & $I_{Z, \max}$ the voltage across it is constant and equal to zener voltage

→ Zener diode is connected in shunt with load. Hence output voltage $V_o = V_z$

→ from the above figure KCL total current $I = I_L + I_Z$

Case - I: Regulation with varying input voltage (V_{in})

$$\text{load current } (I_L) = \frac{V_o}{R_L} = \frac{V_z}{R_L} \quad I_L = \text{constant}$$

If $V_{in} \uparrow$ total current $I \uparrow$ but I_L is constant.
Hence the I_Z increases to keep I_L constant

$$\uparrow I = (I_L) + I_Z \uparrow$$

when $V_{in} \uparrow \quad I \downarrow$

$$\downarrow I = (I_L) + I_Z \downarrow$$

but to keep I_L constant $I_Z \downarrow$. Thus the change in I/P voltage is compensated and O/P is maintained constant.

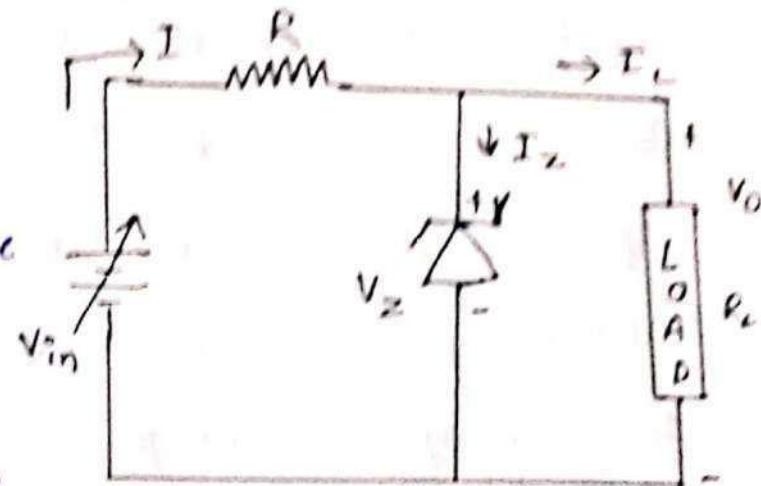
ii) Regulation with varying load.

$V_{in} = \text{constant}$ [I/P voltage]

$R_L = \text{variable}$ [load resistance]

$$I = I_L + I_Z$$

$$I = \frac{V_{in} - V_z}{R} = \text{constant}$$



and V_{in} = constant, V_Z = constant

(14)

→ If $R_L \uparrow$ then I_L decreases and to keep I constant $I_Z \uparrow$ accordingly $\textcircled{I} = \downarrow I_L + I_Z \uparrow$

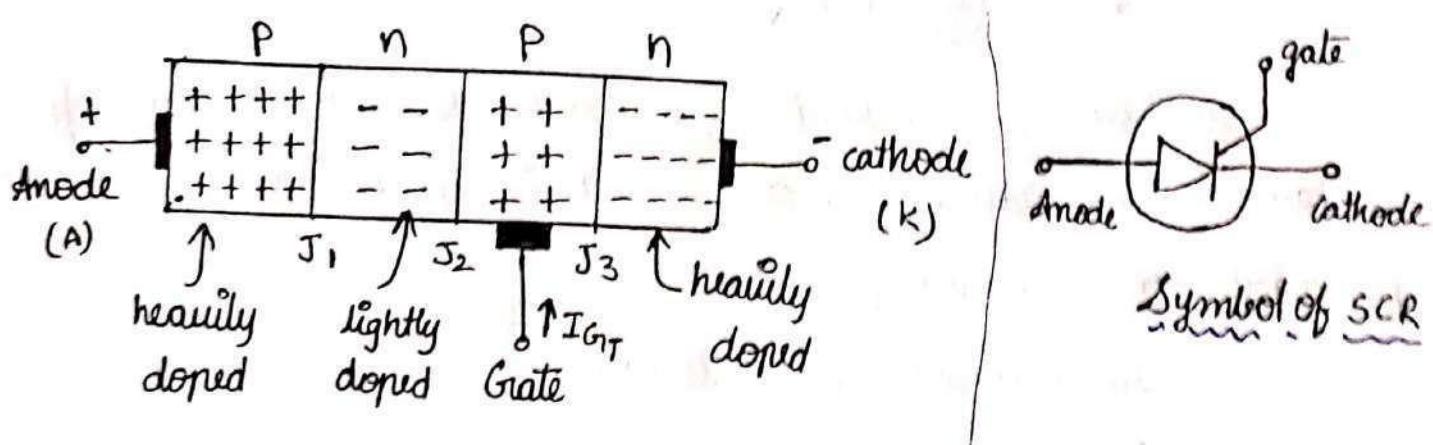
→ If $R_L \downarrow$ then I_L increases and to keep I constant $I_Z \downarrow$ accordingly $\textcircled{I} = \uparrow I_L + I_Z \downarrow$

thus change in load gets compensated and constant o/p is maintained

Silicon Controlled Rectifier (SCR)

Construction:

- The SCR is a four layer p-n-p-n device where p and n layers are alternately arranged. The outer layers are heavily doped while inner layers are lightly doped.
- There are three p-n junctions called J_1 , J_2 and J_3
- The outer p layer is called anode while outer n layer is called cathode. Middle p layer is called gate
- The three terminals are taken out respectively from these three layers, as shown in figure



construction of SCR

- Anode must be positive with respect to cathode of forward bias the SCR
- But this is not sufficient criterion to turn SCR ON. To make it ON, a current is to be passed through the gate terminal denoted as I_{GT} . Thus it is a current operated device
- The I_{GT} is gate trigger current required to make the SCR ON
- The basic material used for the SCR fabrication is silicon

Working principle of SCR

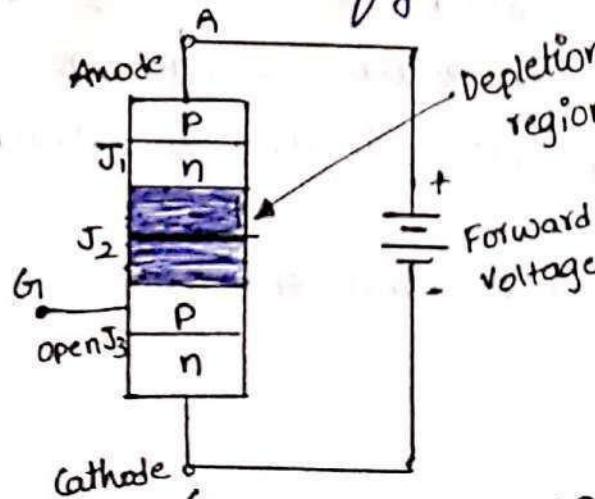
The operation of SCR is divided into two categories,

i) when gate is open and ii) when gate is closed

i) when gate is open:

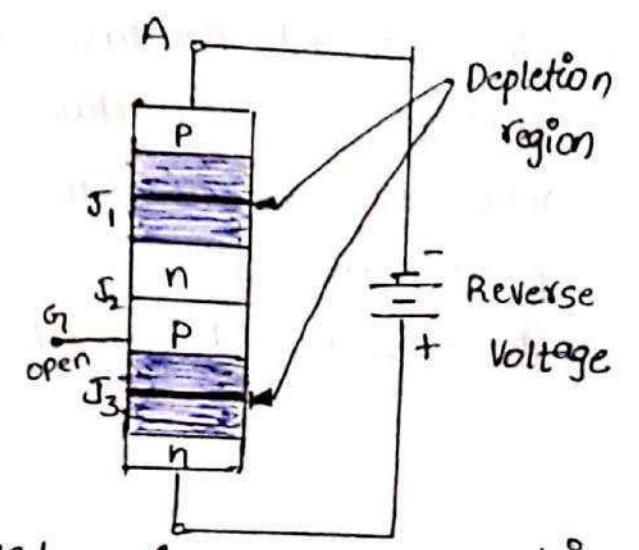
- Consider that the anode is +ve with respect to cathode and gate is open
- The junctions J_1 and J_3 are forward biased and junction J_2 is reverse biased. There is depletion region around J_2 and only leakage current flows which is negligibly small
- Practically the SCR is said to be OFF. This is called forward blocking state of SCR and voltage applied to anode and cathode with anode +ve is called forward voltage.

This is shown in figure



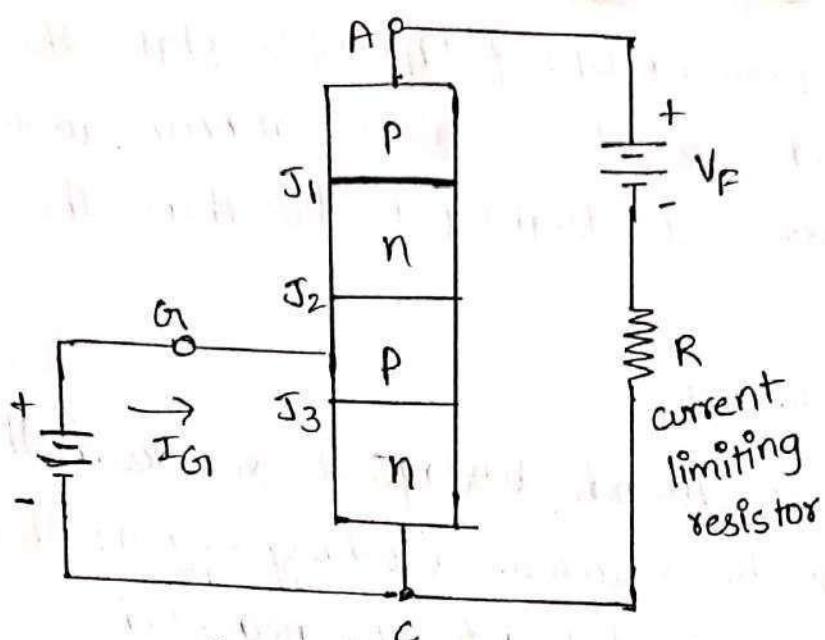
$J_1, J_3 \rightarrow$ Forward biased

J_2 - reverse biased



J_1, J_3 reverse biased
 J_2 Forward biased

- with gate open if cathode is made +ve with (16) to anode, the junctions J_1 , J_3 become reverse biased and J_2 forward biased. still the current flowing is leakage current, which can be neglected as it is very small
- The voltage applied to make cathode +ve is called reverse voltage and SCR is said to be in reverse blocking state. This is shown in the figure
- In forward blocking state, if the forward voltage is increased and made sufficiently large, the reverse biased junction J_2 breaks down and SCR conducts heavily
- 2) When gate is closed:
- consider that the voltage is applied between gate and cathode when the SCR is in forward blocking state
- The gate is made positive with respect to the cathode.
- The electrons from n-type cathode which are majority in number, cross the junction J_3 to reach to positive of battery
- While holes from P types move towards the negative of battery, this constitutes the gate current
- This current increases the anode current as some of electrons cross junction J_2 . As anode current increases, more electrons cross the junction J_2 and the anode current further increases
- The resistance R is required to limit the current.



operation of SCR when gate is closed

→ Once the SCR conducts, the gate loses its control

Characteristics of SCR:

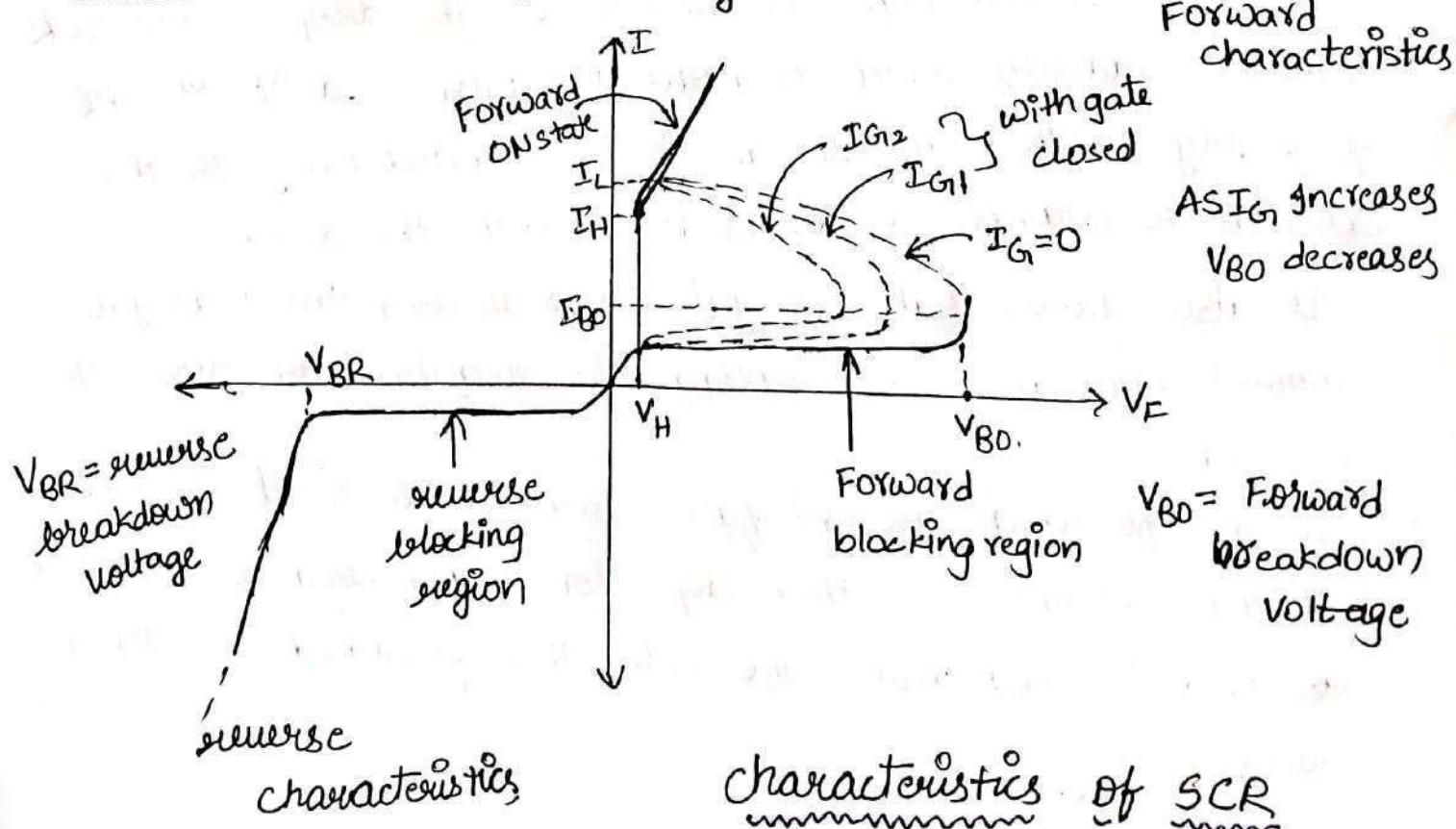
i) Forward characteristics:

- It shows a forward blocking region, when $I_G = 0$, it also shows that when forward voltage increases upto V_{BO} , the SCR turns ON and high current results. The drop across SCR reduces suddenly which is now the ohmic drop in the four layers. The current must be limited only by the external resistance in series with the device.
- It also shows that, if gate bias is used then as gate current increases, less voltage is required to turn ON the SCR.
- If the forward current falls below the level of the holding current I_H , then depletion region begins to develop around J_2 and device goes into the forward blocking region.

→ When SCR is turned ON from OFF state, the resulting forward current is called latching current I_L . The latching current is slightly higher than the holding current.

Reverse Characteristics:

- If the anode to cathode voltage is reversed, then the device enters into the reverse blocking region. The current is negligibly small and practically neglected.
- If the reverse voltage is increased, similar to the diode, at a particular value avalanche breakdown occurs and a large current flows through the device. This is called reverse breakdown and the voltage at which this happens is called reverse breakdown voltage V_{BR} .
- The forward breakdown voltage is greater than reverse breakdown voltage.



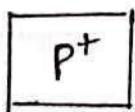
TUNNEL Diode :

- It refers to a special diode which works on the principle of quantum mechanical tunneling. It is a P-N junction in which both the sides are heavily doped [P^+ and N^+]
- Both P & N region are degenerated type. That is fermilimits should lie inside the valence band in P-region and inside the conduction band in N-region
- Heavily doped diodes has very narrow depletion region, Hence tunneling occurs
Electron tunneling occurs if two conditions are satisfied
 - i) energy barrier should be smaller width
 - ii) An empty energy level should be present of the other side of energy level.

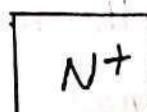
Energy band diagram:

i) zero bias

P & N are separate



E_C



E_{FN}

E_F^a

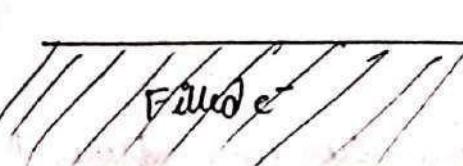
Intrinsic
energy fermi
level

E_F^b

E_V

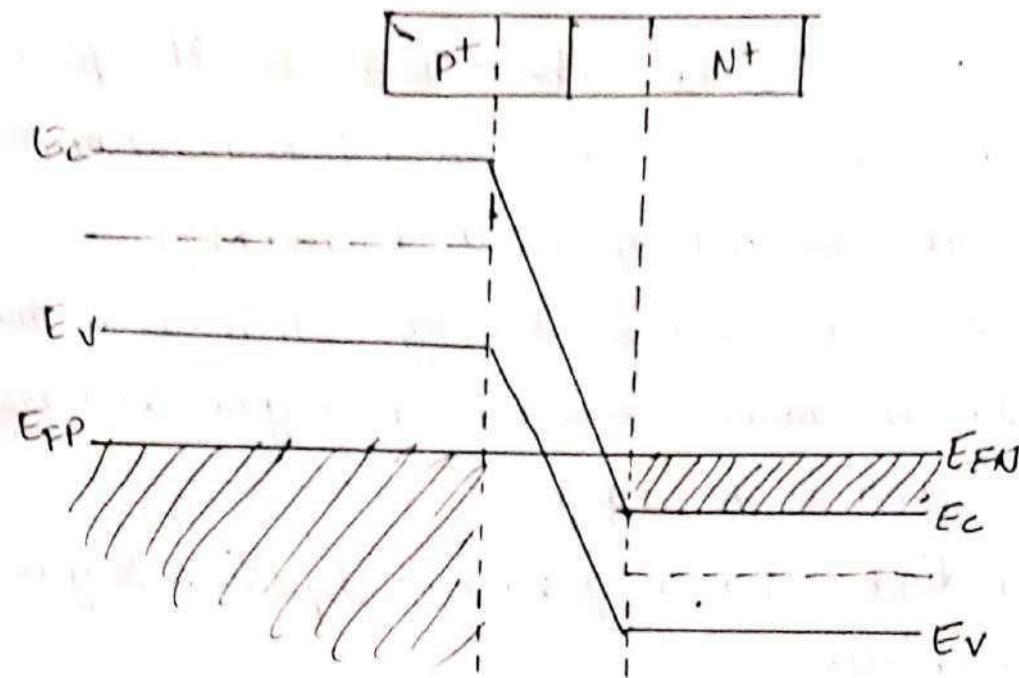
E_{FP}

Max Energy Level



E_V

2) P & N are together,



- Energy levels above E_{FN} and E_{FP} are assumed to be empty
- Electron tunneling does not occur in zero biased because no vacant energy is present.

Reverse bias

→ When positive voltage is applied

to N side Energy levels

will move down by an

amount $-ev$, And the net

energy barrier becomes

$$e(V_0 + V)$$

→ The filled levels in the valence

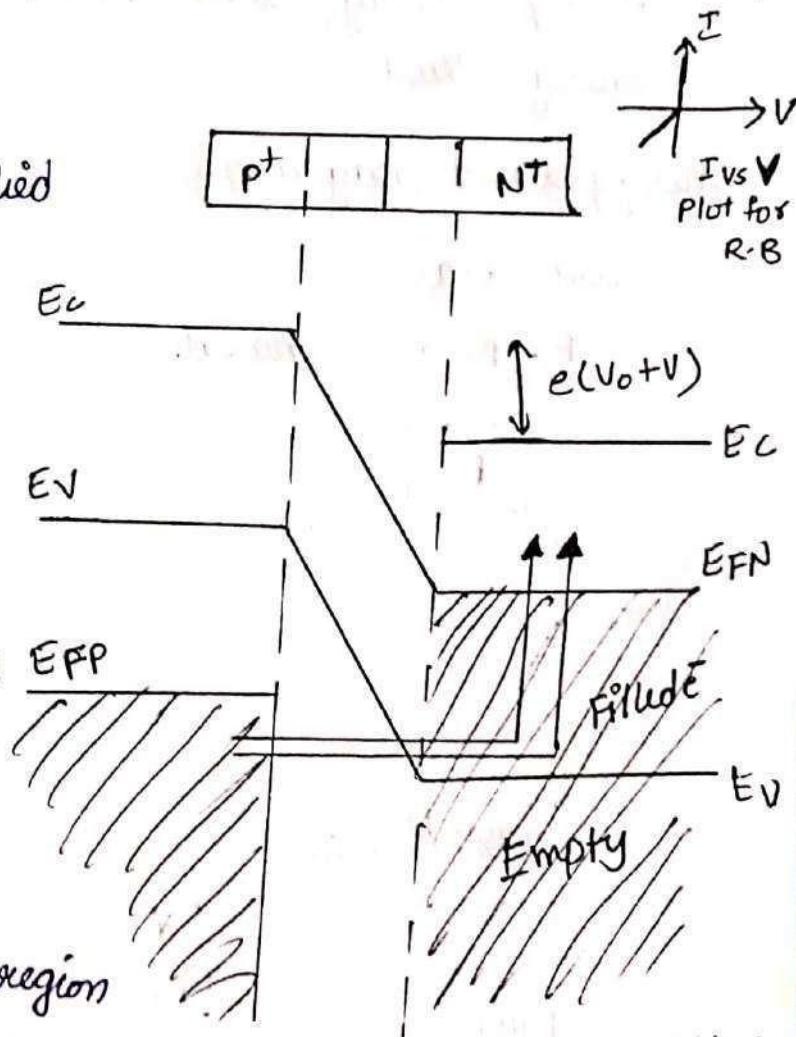
band of P-region are in

line with empty levels in the

CB of N-region. Hence electron

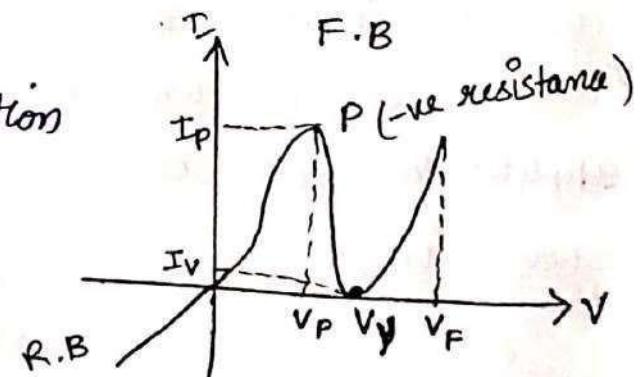
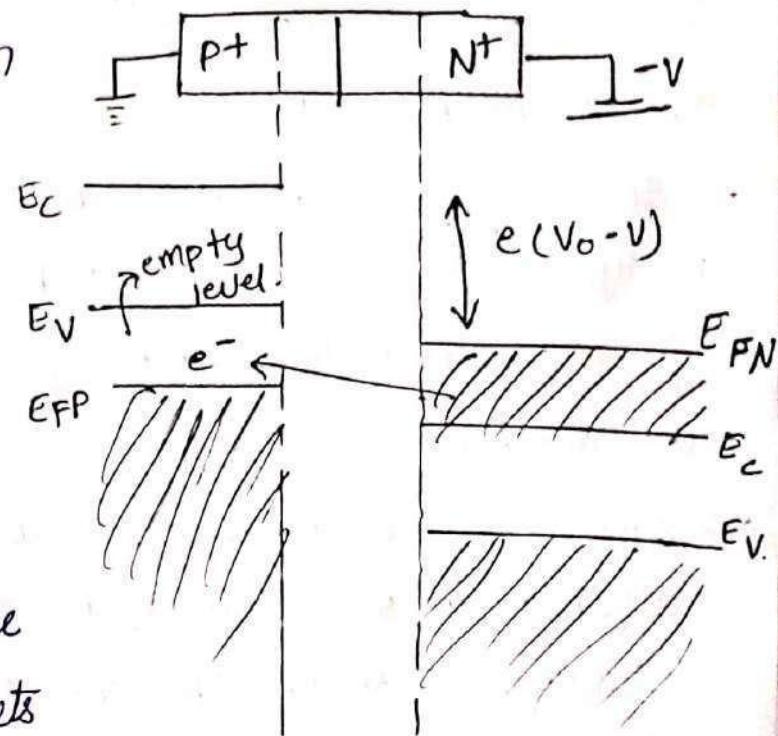
tunneling occurs from VB of P-region

to conduction band of N-region. Tunneling current flows N to P



Forward bias

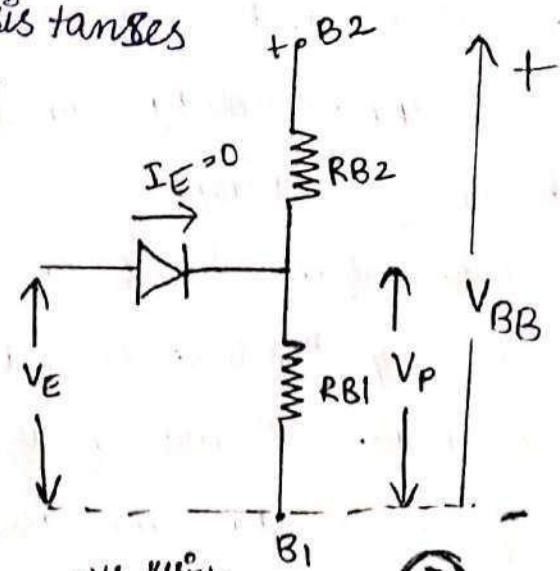
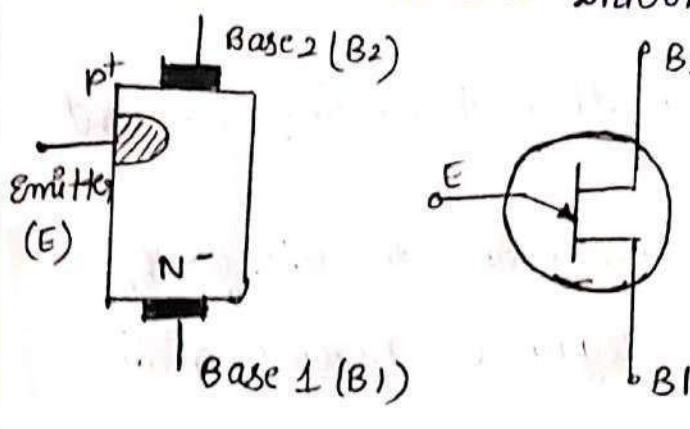
- If 've voltage is applied on N-side the energy levels will move up by amount $+ev$ on N-side. And net energy barrier becomes $e(V_0 - V)$
- (If '+ve' voltage is applied on)
- A few filled levels in the conduction band of N-side gets aligned with the empty levels in the V.B of P-side. Hence e^- tunneling occurs from N to P and tunneling current flows from P to N
- If applied voltage is increased then tunneling current keeps increasing.
- When filled levels in C.B of N-region is in line with the empty level in V.B of P-region e^- tunneling will be max and max flows
- If the voltage increases further the eliminating e^- tunneling decreases and gradually becomes zero.
- The net current through the tunnel diode is the superposition of tunneling current and diffusion current



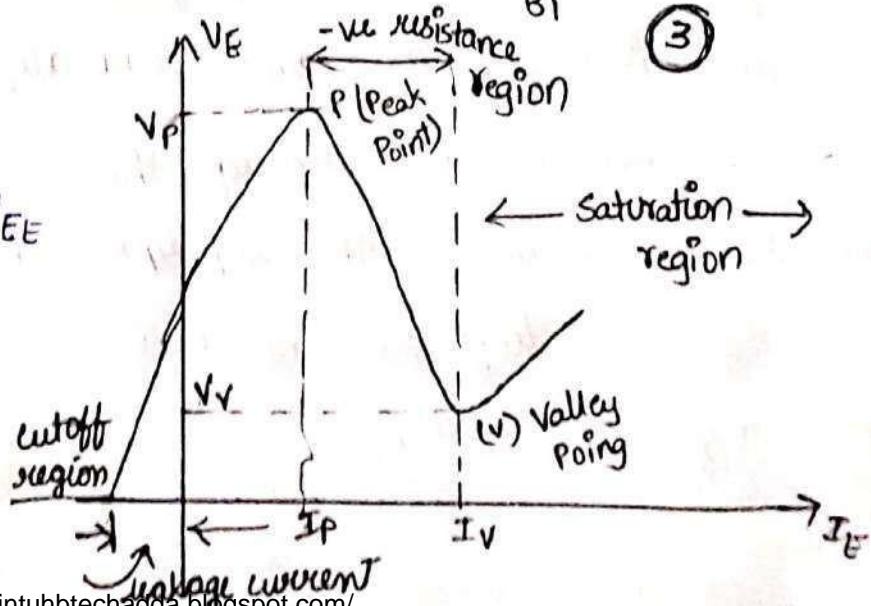
UJT : Uni Junction Transistor

Special purpose devices

- It is a 3 terminal device consisting of lightly doped n-type silicon slab and a p-type material forming a P-N junction and two ends of the slab, two bases B_1 and B_2 are attached
- Emitter 'E' is taken from aluminium rod which is obtained attached at one end of p-type material
- Figure ① shows the construction of UJT
- Figure ② shows the symbol of UJT
- Figure ③ shows the equivalent circuit of UJT where R_{B1} and R_{B2} are internal resistances



- The supply V_{BB} is connected between the bases B_1 and B_2 while V_{EE} applied to emitter as shown in ③



→ The potential across R_{B1} is given by V_p

(23)

$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

η - Intrinsic stand off ratio

case-1: $V_E < V_p$

PN junction is reverse bias and I_E does not flow. UJT is said to be off. But there will a small leakage current from B_2 to emitter due to minority carriers

case-2: $V_E \geq V_p$

PN junction is forward bias with

$$V_p = \eta V_{BB} + V_D \text{ (diode drop or cutin voltage)}$$

Under this condition holes are injected into N-type base. These holes are repelled by B_2 terminal and attracted to B_1 terminal.

Accumulation of holes across R_{B1} reduces resistance in this region and emitter current (I_E) increases. But voltage (V_p) decreases. UJT is said to be ON.

$$R \downarrow I_E \uparrow V_p \downarrow$$

Figure ④ shows input characteristics of UJT

→ Upto peak point P, diode is R.B and the region to the left of P point is cutoff region

→ When V_E becomes $V_E \geq V_p$ the diode starts conducting. Hence holes are injected into the N-layer. Hence $R \downarrow$, $I_E \uparrow$, $V \downarrow$. So there is negative resistance region from peak point (P) to valley point V. After valley point the device driven

into saturation and behaves like normal P-N junction diode.

V_F → Firing voltage of UJT [on]

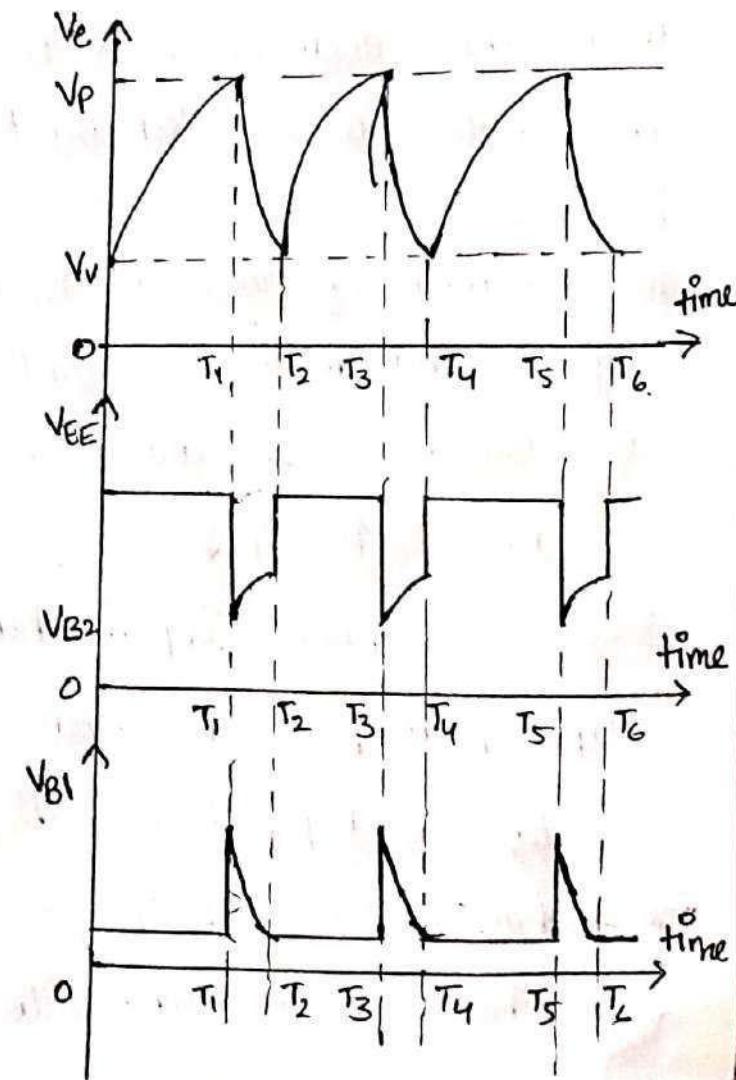
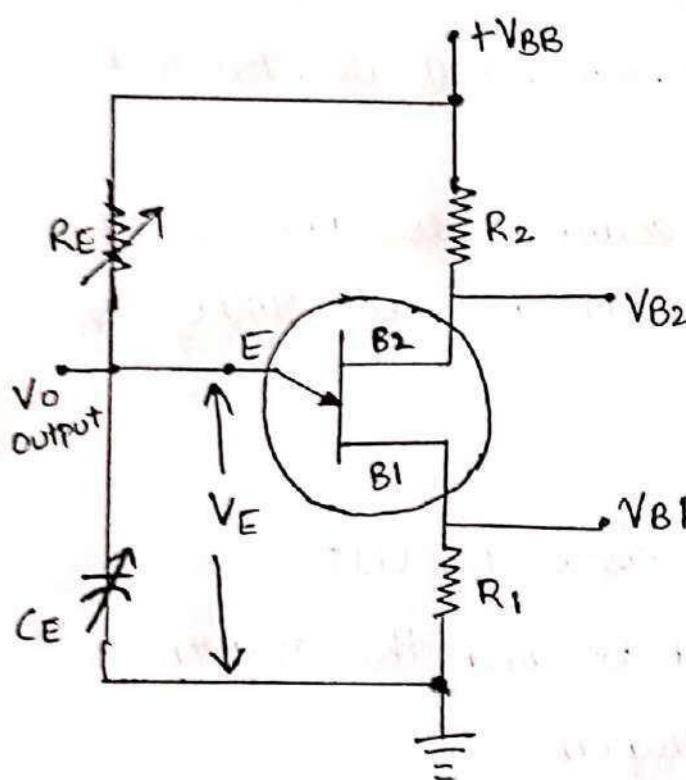
P^+ → heavily doped [Alloying] Aluminium

N^- → Negatively doped

Application of UJT

- 1) Sawtooth wave generators
- 2) Pulse generators
- 3) Relaxation oscillators

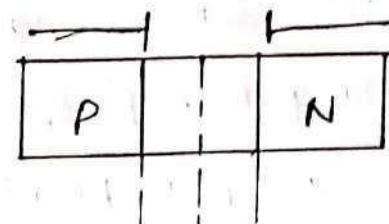
UJT Relaxation oscillator



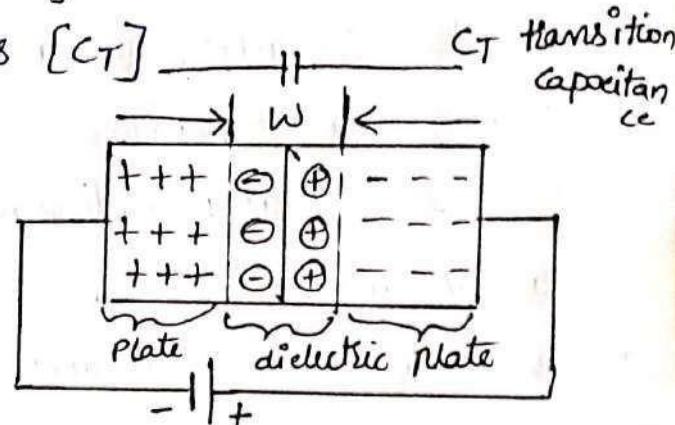
- The relaxation oscillator using UJT which is meant for generating sawtooth waveform as shown in figure. It consists of a UJT and a capacitor C_E which is charged through R_E as the supply voltage V_{BB} is switched ON.
- The voltage across the capacitor increases exponentially and when the capacitor voltage reaches the peak point voltage V_p , the UJT starts conducting and the capacitor voltage is discharged rapidly through B_1 and R_1 . ~~After the peak~~
- After the peak point voltage of UJT is reached, it provides negative resistance to the discharge path which is useful in the working of the relaxation oscillator.
- As the capacitor voltage reaches zero, the device then cuts off and capacitor C_E starts to charge again. This cycle is repeated continuously generating a sawtooth wave from across C_E .
- The inclusion of external resistors R_2 & R_1 in series with B_2 and B_1 provides spike waveforms. When UJT fires, the sudden surge of current through B_1 causes drop across R_1 , which provides +ve going spikes. Also, at the time of firing, fall of V_{EB1} causes I_2 to increase rapidly which generates -ve going spikes across R_2 .
- By changing the values of C_E or R_E , frequency of the output waveform can be changed as desired, since these values control the time constant $R_E C_E$ of the capacitor charging circuit.

Varactor Diode:

- Varactor diode are special types of diode in which transition capacitance property is predominant
- It is also called as voltage variables capacitor (VVC) or varicap or tuning diodes.
- In R.B the depletion region exists between P & N as shown in diagram
- In the P & N region acts like the plates of the capacitor while the depletion region acts as dielectric.



- There exists a capacitance at PN junction called the transition capacitance denoted as C_T
- Mathematically $C_T = \frac{\epsilon A}{w}$
- ϵ = permittivity of semiconductor
 A = Area of cross section
 w = width of depletion region



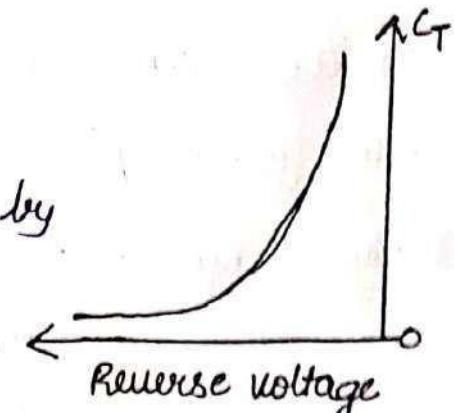
- As the R.B voltage increases the width of depletion region increases thus transition capacitance C_T decreases

→ Similarly

R.B voltage \downarrow $w \downarrow C_T \uparrow$

- In short capacitance can be controlled by applied voltage

- The variation of C_T with respect to R.B voltage is seen.



UNIT-4. ANALYSIS AND DESIGN OF

SMALL SIGNAL LOW FREQUENCY BJT

AMPLIFIERS

Transistor Hybrid Model

$$V_1 = h_i I_1 + h_{\gamma} V_2 \quad \text{--- (1)}$$

$$I_2 = h_f I_1 + h_o V_2 \quad \text{--- (2)}$$

The hybrid parameters in the above equations defines as follows

h_i = input resistance with output short circuited

$$h_{11} = h_i = \left. \frac{V_1}{I_1} \right|_{V_2=0} \text{ in } \Omega$$

h_{γ} = reverse voltage gain, input is open circuit

$$h_{12} = h_{\gamma} = \left. \frac{V_1}{V_2} \right|_{I_1=0}$$

h_f = forward current gain, output is short circuit

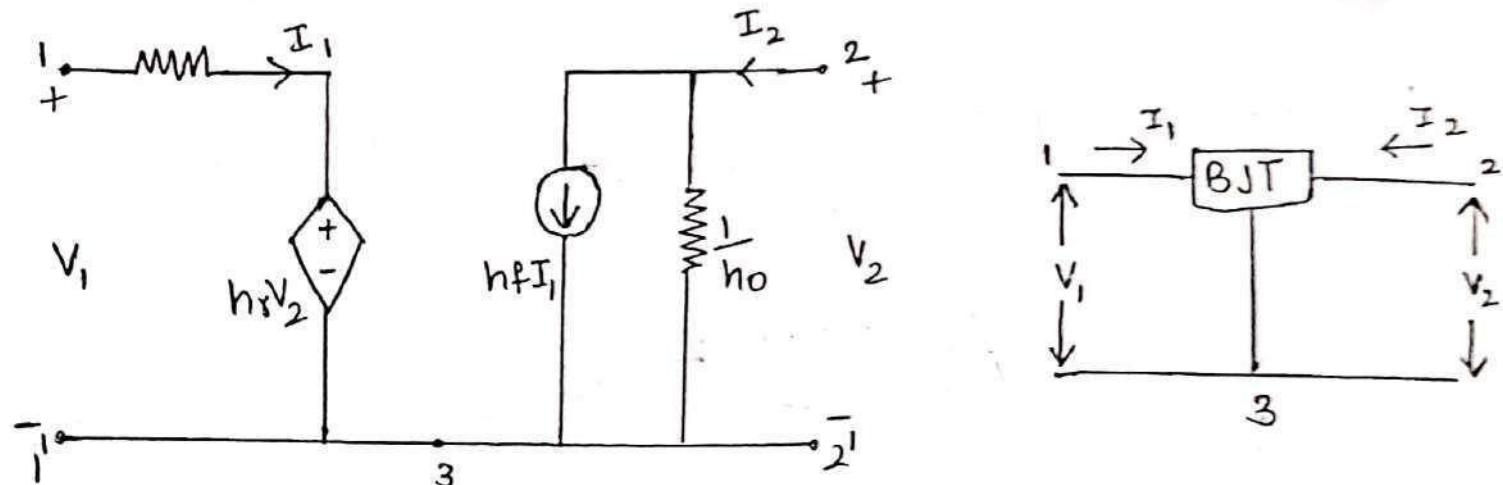
$$h_{21} = h_f = \left. \frac{I_2}{I_1} \right|_{V_2=0}$$

h_o = output admittance when input is open circuit

$$h_{22} = h_o = \left. \frac{I_2}{V_2} \right|_{I_1=0} \text{ or}$$

$\frac{1}{h_o}$ = resistance

H - parameter of transistor equivalent circuit



★

Parameters	CE	CB	CC
h_i	h_{ie}	h_{ib}	h_{ic}
h_o	h_{re}	h_{rb}	h_{rc}
h_f	h_{fe}	h_{fb}	h_{fc}
h_{o2}	h_{oe}	h_{ob}	h_{oc}

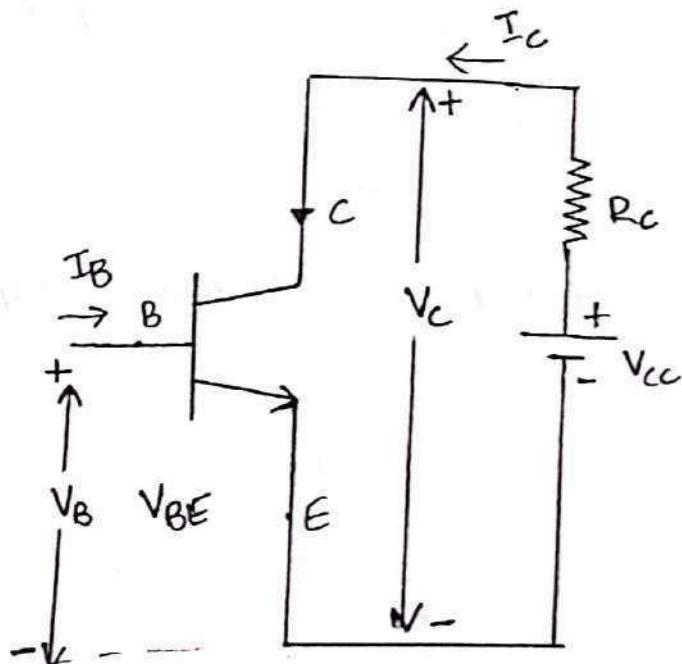
1) The hybrid model for CE transistor

$$h_{ie} = \frac{V_{BE}}{I_b} \Big|_{V_{CE}=0}$$

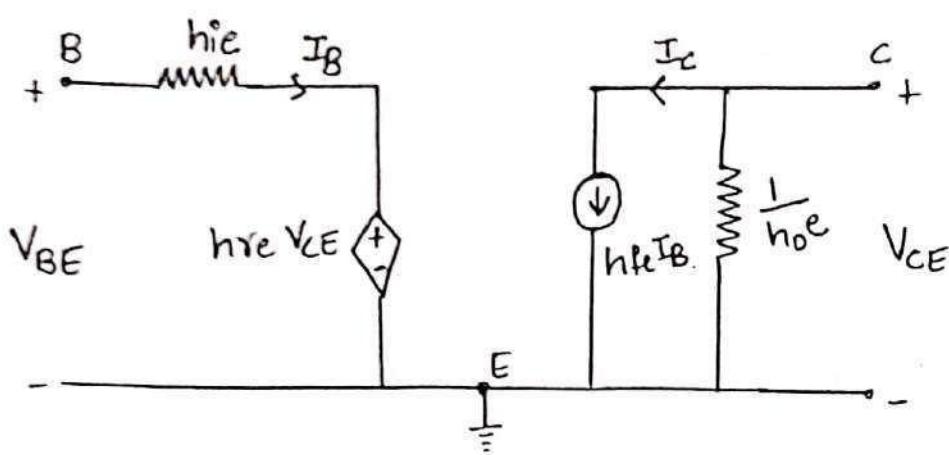
$$h_{re} = \frac{V_{BE}}{V_{CE}} \Big|_{I_A=0}$$

$$h_{fe} = \frac{I_c}{I_b} \Big|_{V_{CE}=0}$$

$$h_{oe} = \frac{I_c}{V_{CE}} \Big|_{I_B=0}$$



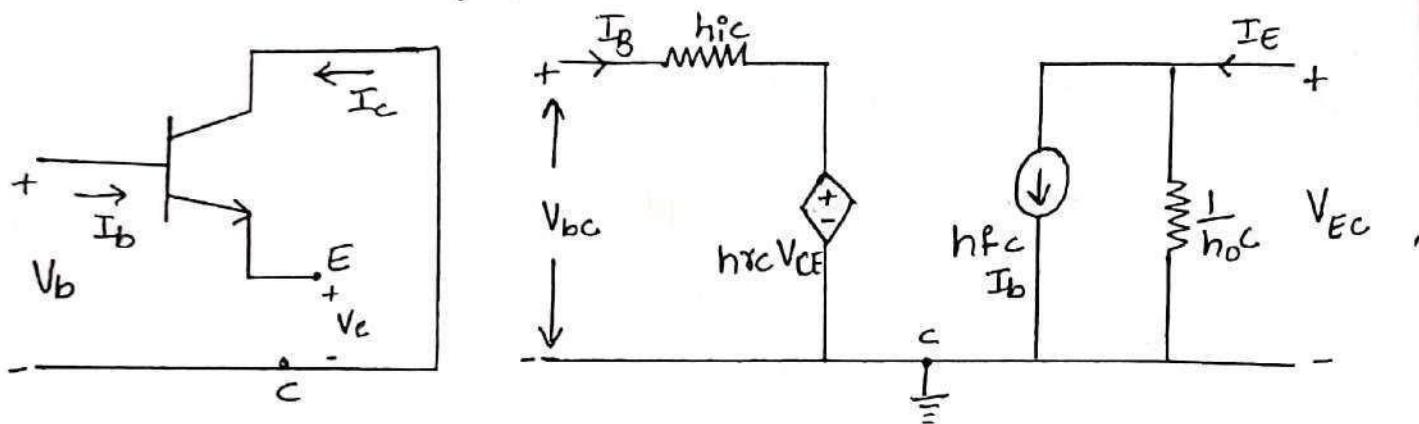
③



$$V_{BE} = hie I_B + hre V_{CE} \quad \text{---(1)}$$

$$I_C = hfe I_B + hoe V_{CE} \quad \text{---(2)}$$

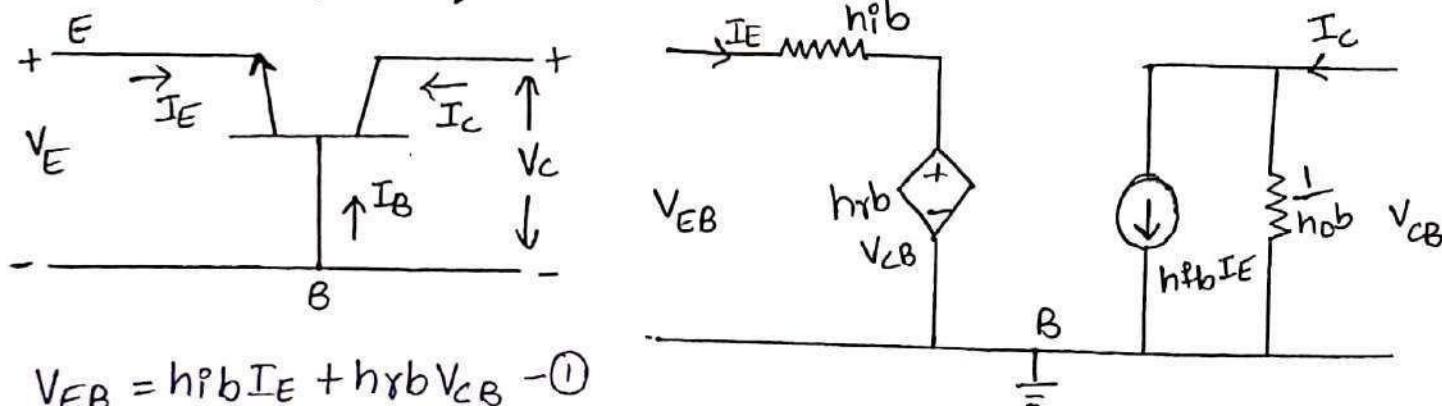
2) The hybrid model for CC transistors



$$V_{BC} = hic I_B + hrc V_{EC} \quad \text{---(1)}$$

$$I_E = hf c I_B + hoc V_{EC} \quad \text{---(2)}$$

3) The hybrid model for CB transistors



$$V_{EB} = hib I_E + hrb V_{CB} \quad \text{---(1)}$$

$$I_C = hfb I_E + hob V_{CB} \quad \text{---(2)}$$

$$hib = \frac{V_{EB}}{I_E} \Big|_{V_{CB}=0}$$

$$hrb = \frac{V_{EB}}{V_{CB}} \Big|_{I_E=0}$$

$$hfb = \frac{I_C}{I_E} \Big|_{V_{CB}=0}$$

$$hob = \frac{I_C}{V_{CB}} \Big|_{I_E=0}$$

	CC	CE	CB
Input node :	Base	Base	emitter
Input current	I_b	I_b	I_E
Output node	emitter	collector	collector
Output current	I_e	I_c	I_c
Input voltage	V_{bc}	V_{BE}	V_{EB}
Output voltage	V_{EC}	V_{CE}	V_{CB}

Typical Value of H-parameters for

CE configuration

$$h_{ie} = 1.1 \text{ k}\Omega$$

$$h_{re} = 2.5 \times 10^{-4}$$

$$h_{fe} = 50$$

$$h_{oe} = 25 \times 10^6 \text{ V}$$

CB configuration

$$h_{ib} = 21.6 \Omega$$

$$h_{rb} = 2.9 \times 10^{-4}$$

$$h_{fb} = -0.98$$

$$h_{ob} = 0.49 \mu\text{A/V}$$

CC configuration

$$h_{ic} = 1,100 \Omega$$

$$h_{rc} = 1$$

$$h_{fe} = -51$$

$$h_{oc} = 25 \mu\text{A/V}$$

Conversion formula from

CE to CC

$$h_{fc} = -(1+h_{fe})$$

$$h_{ic} = h_{ie}$$

$$h_{oc} = h_{oe}$$

$$h_{re} = 1-h_{rc}$$

Conversion formula from CE to

CB

$$h_{fb} = \frac{-h_{fe}}{1+h_{fe}}$$

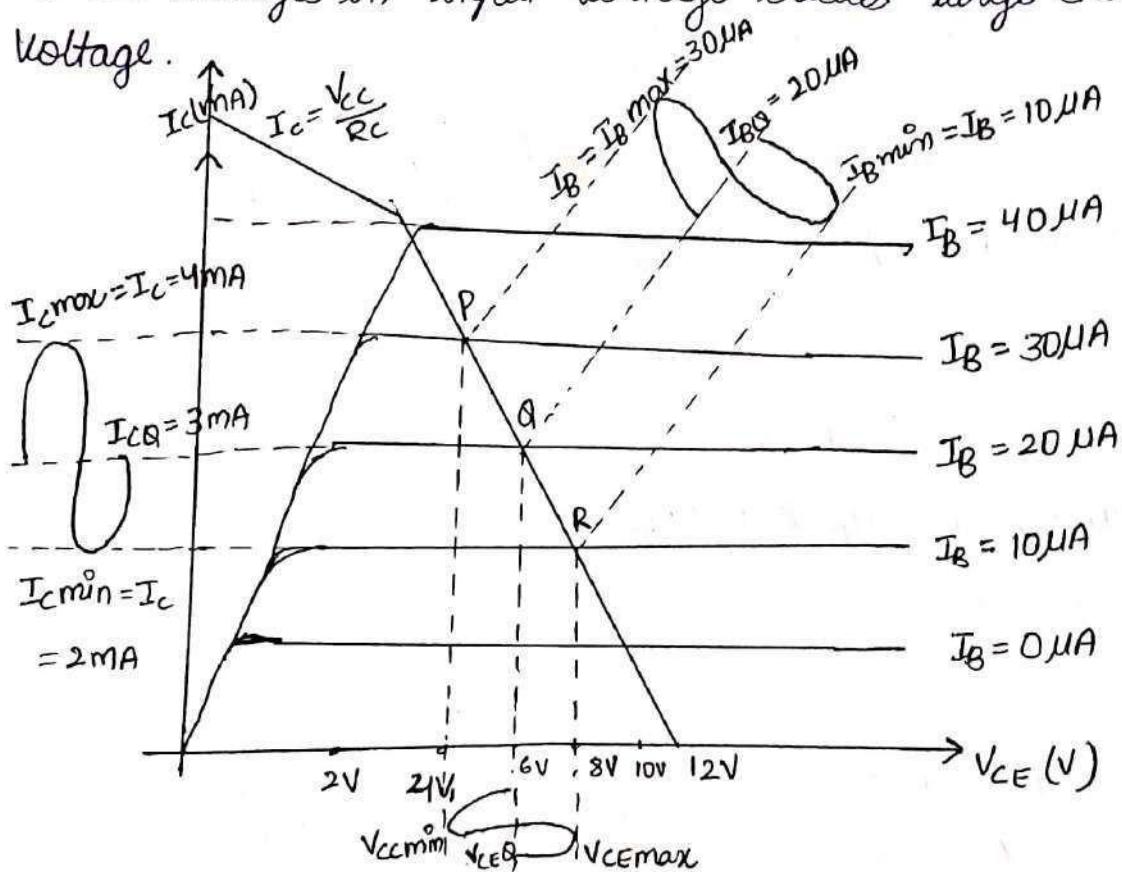
$$h_{ib} = \frac{h_{ie}}{1+h_{fe}}$$

$$h_{ob} = \frac{h_{oe}}{1+h_{fe}}$$

$$h_{rb} = \frac{h_{ie} \cdot h_{oe}}{1+h_{fe}} - h_{re}$$

Transistor Amplifying Action :

- Amplifier is a device which increases the power level of the signal without changing frequency and shape of signal.
- Transistor is used as amplifier in active region.
- Small changes in input voltage creates large change in output voltage.



- The above figure shows the CE output characteristics and DC load line
- When input signal is applied the base current I_B varies sinusoidally

$$I_{B,\max} = 30 \mu A$$

$$I_{B,\min} = 10 \mu A$$

$$\boxed{\Delta I_B = 20 \mu A}$$

Due to change in I_B the I_c also changes

$$\boxed{\Delta I_c = 4 \text{ mA} - 2 \text{ mA} = 2 \text{ mA}}$$

$$\boxed{B = \frac{\Delta I_C}{\Delta I_B} = \frac{2mA}{20\mu A} = 100}$$

→ The current amplification is given by $\frac{\Delta I_C}{\Delta I_B} = 100$

→ Due to change in I_C the collector to emitter voltage V_{CE} varies

$$\Delta V_{CE} = 8 - 4 \quad \boxed{\Delta V_{CE} = 4V}$$

→ The output voltage of CE amplifier

$$\boxed{V_o = V_{CE}}$$

→ Small change in input voltage

$$\Delta V_{in} = \Delta I_B \cdot R_B$$

$$V_{in} = V_{cc} - I_B R_B$$

→ Small change in output voltage

$$V_o = V_{cc} \cdot I_C R_C$$

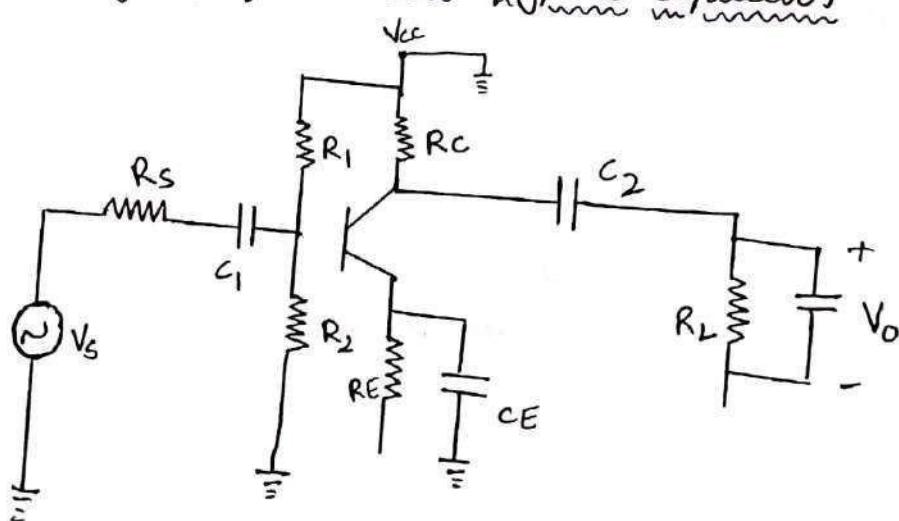
$$\Delta V_o = \Delta I_C \cdot R_L$$

$$\frac{\Delta V_o}{\Delta V_{in}} = \frac{B \cdot \Delta I_B \cdot R_C}{\Delta I_B \cdot R_B}$$

$$\boxed{\Delta V_o = \frac{B \cdot R_L}{R_B} \cdot \Delta V_{in}}$$

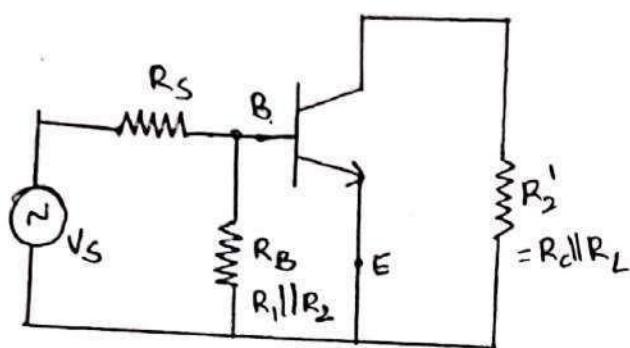
Thus for a small change in V_{in} we get larger output V_o

AC Analysis of CE with Bypass Capacitor

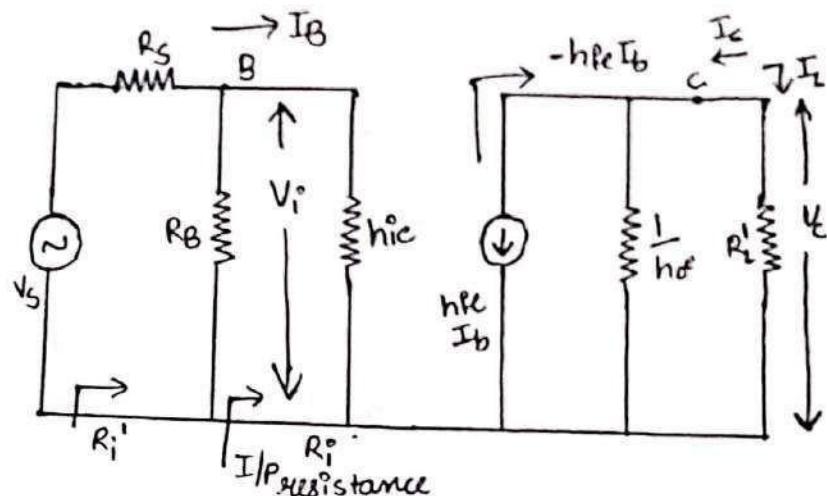


In order to draw AC equivalent circuit of RC coupled CE amplifier we follow some steps:

- 1) Identify BJT configuration in the circuit
- 2) Draw the AC equivalent circuit by replacing the large capacitors with s.c and small capacitors with open circuit and $V_{CC} = \text{ground}$.
- 3) Replace the BJT with approximate hybrid model as shown in figure



AC equivalent circuit



Approximate CE model hybrid

1) Current gain: $A_i^o = \frac{I_L}{I_B}$ By current division rule

$$I_L = \frac{-h_{FE} I_B \times \frac{1}{h_{OE}}}{\frac{1}{h_{OE}} + R_L'} = \frac{-h_{FE} I_B}{h_{OE}} \quad / \quad \frac{1 + h_{OE} \cdot R_L'}{h_{OE}}$$

$$A_i^o = \frac{I_L}{I_B} = \frac{-h_{FE}}{1 + h_{OE} R_L'}$$

where $R_L' = R_c || R_L$

$$A_i^o = \frac{I_L}{I_B} = -h_{FE} \quad / \quad \text{if } h_{OE} \neq 0$$

current gain is -ve means

I_L, I_C are in different directions

2) Input resistance:

$$R_i = \frac{V_i}{I_B}$$

$$V_i = h_{ie} \times I_B \Rightarrow$$

$$\frac{V_i}{I_B} = h_{ie}$$

$$R_i' = R_B \parallel R_i$$

3) Voltage gain:

$$AV_i = \frac{V_o}{V_i}$$

$$R_i' = R_B \parallel h_{ie}$$

$$V_o = -h_{fe} \cdot I_B \cdot R_L''$$

$$AV_m = \frac{V_o}{V_i} \quad \text{where } AV_m \rightarrow \text{medium frequency}$$

$$\text{where } R_L'' = \frac{1}{h_{oe}} \parallel R_L'$$

$$R_L' = R_c \parallel R_L$$

$$V_i = I_B \times h_{ie}$$

$$\frac{V_o}{V_i} = -\frac{h_{fe} I_B \cdot R_L''}{I_B \times h_{ie}}$$

$$AV_i = \frac{-h_{fe} R_L''}{h_{ie}}$$

→ Here -ve indicates 180° phase shift between output and input

$$AV_s = \frac{V_o}{V_s}$$

$$AV_s = \frac{V_o}{V_i} \times \frac{V_i}{V_s} = AV_i \times \frac{V_i}{V_s}$$

$$V_i = V_s \times \frac{R_i'}{R_s + R_i'}$$

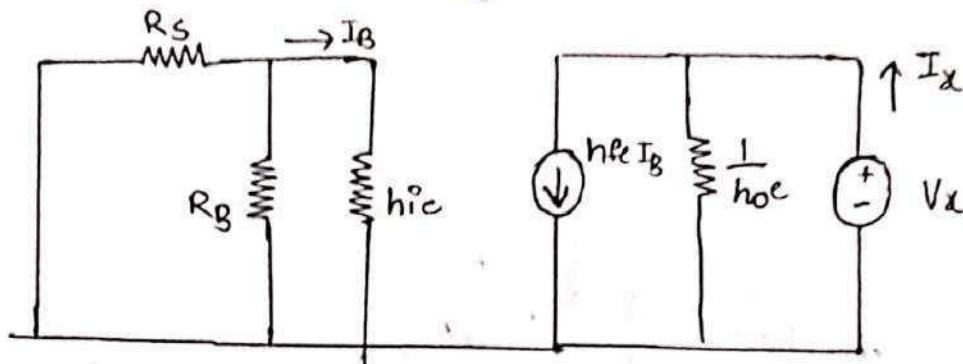
$$AV_s = AV_i \times \frac{R_i'}{R_s + R_i'}$$

$$\frac{AV_s}{AV_p} = 1$$

if $R_s = 0$

(9)

4) Output resistance: $R_o = \frac{V_x}{I_x}$



$$R_s' = R_s \parallel R_B$$

$$I_B R_s' + I_B h_{ie} = 0$$

$$I_B = 0$$

(KVL)
in I/P loop

Apply KCL at O/P
[$I_x = h_{fe} I_B + h_{oe} \cdot V_x$]

$$I_x = h_{oe} \cdot V_x \Rightarrow \frac{I_x}{V_x} = h_{oe}$$

$$R_o = \frac{V_x}{I_x} = \frac{1}{h_{oe}}$$

In order to calculate R_o we must follow some steps.

- 1) Disable V_s (s.c.)
 - 2) Remove R_L' from O/P (Load)
 - 3) Apply voltage source V_x across the output terminal
- We can also R_o when we O.C

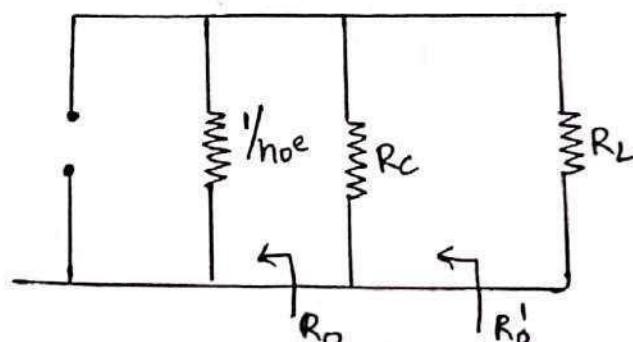
$h_{fe} I_B$

$$R_o = \frac{1}{h_{oe}}$$

$$R_o' = R_o \parallel R_C$$

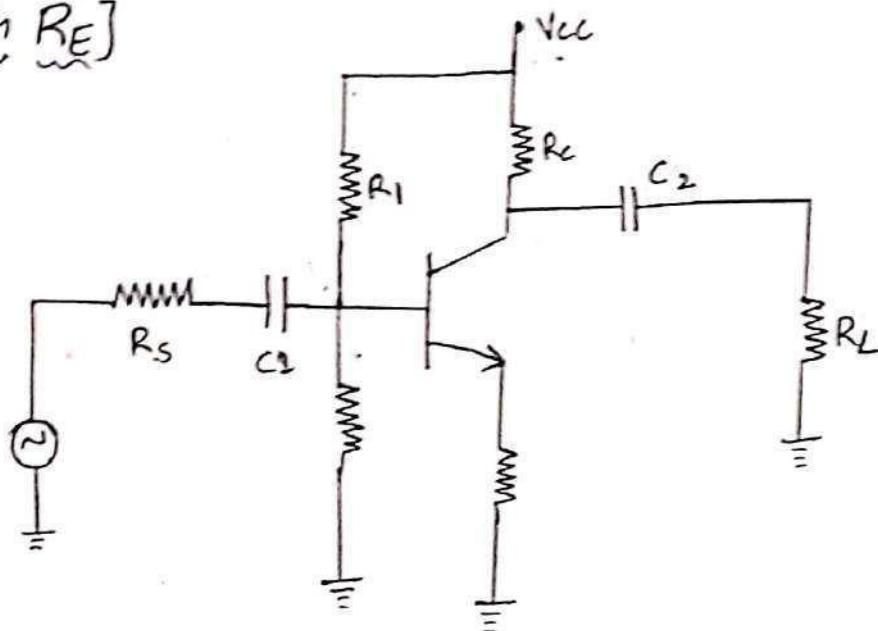
$$R_o' = \frac{1}{h_{oe}} \parallel R_C$$

if $h_{oe} = 0$, $[R_o' = R_C]$

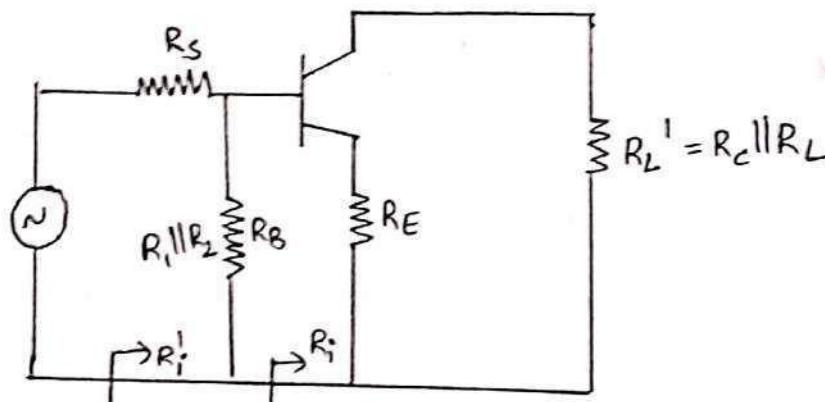


AC Analysis of CE without Bypass Capacitor

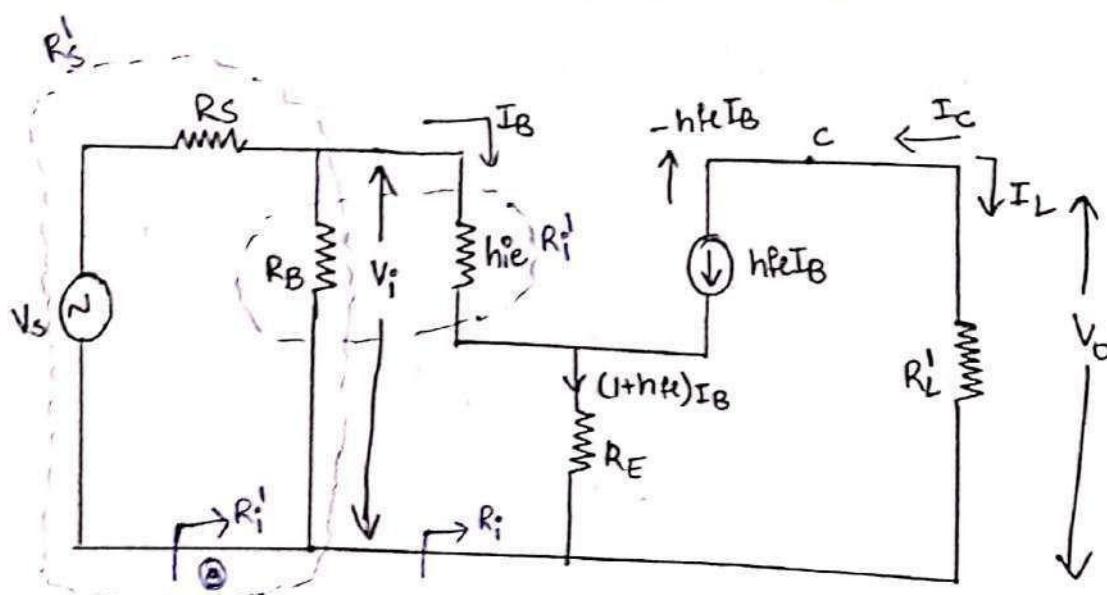
CE [with R_E]



RC Coupled CE Amplifier



AC Equivalent Circuit



Approximate CE Hybrid Model

neglect h_{oe}

$$h_{oe} = 0$$

1) Current gain: $A_i^o = \frac{I_L}{I_B}$ (11)

 $I_L = -h_{FE} \cdot I_B$

$\frac{I_L}{I_B} = A_i^o = -h_{FE}$

[with and without bypass capacitor current gain is same]

2) Input resistance: (R_i) $R_i^o = \frac{V_i^o}{I_B}$

$V_i^o - I_B h_{IE} - (1+h_{FE}) I_B \cdot R_E = 0$

$V_i^o = I_B h_{IE} + (1+h_{FE}) I_B \cdot R_E$

$V_i^o = I_B [h_{IE} + (1+h_{FE}) R_E]$

$R_i^o = \frac{V_i^o}{I_B} = h_{IE} + (1+h_{FE}) R_E$

In CE amplifier without bypass IP resistor increases

3) Voltage gain: $A V_i^o = \frac{V_o}{V_i^o}$

$V_o = -h_{FE} I_B \cdot R_L' ; V_i^o = I_B [h_{IE} + (1+h_{FE}) R_E]$

$\frac{V_o}{V_i^o} = \frac{-h_{FE} \cdot R_L'}{h_{IE} + (1+h_{FE}) R_E}$

-ve indicates V_o, V_i 180° phase shift

→ Voltage gain decreases when compared to CE Amplifier without RE [with bypass]

$A V_S = \frac{V_o}{V_i^o} \times \frac{V_i^o}{V_S} = A V_i^o \times \frac{V_i^o}{V_S}$

$A V_S = A V_i^o \times \frac{R_i^o}{R_S + R_i^o}$

where $R_i^o = R_i || R_B$

4) Output Resistance: $R_o^1 = R_S \parallel R_B$

(12)

$$I_B R_S^1 + I_B h_{ie} + (1+h_{fe}) I_B R_E = 0$$

$$\boxed{I_B = 0}$$

$$I_X = -h_{fe} I_B \quad I_X = 0$$

$$R_o = \frac{V_X}{I_X} = \frac{V_X}{0} = \infty$$

$$R_o^1 = R_o \parallel R_C \quad \boxed{R_o^1 = R_C}$$

In CE Amplifier without bypass

- i) I/P resistance increases
- ii) Current gain remains the same
- iii) Voltage gain decreases
- iv) O/P resistance increases

AC Analysis of Common Collector:

CC Amplifier circuit

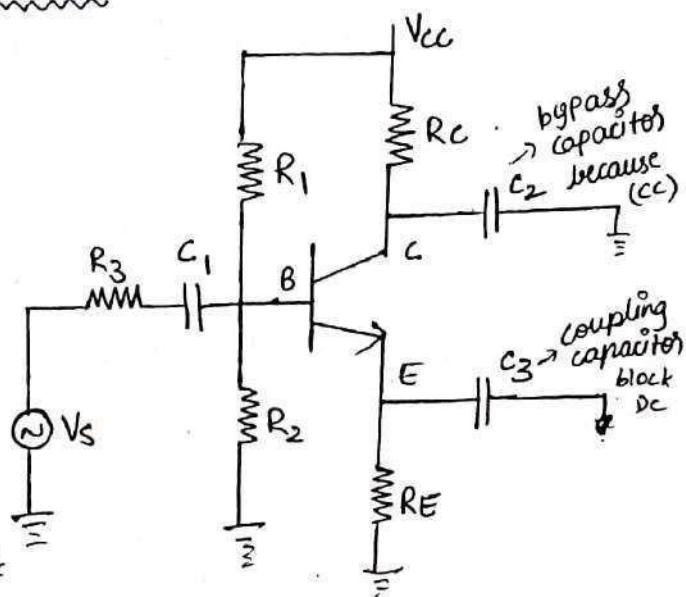
→ Here the I/P Node - Base
O/P Node - emitter

→ C_1 & C_3 are the input and output coupling capacitors

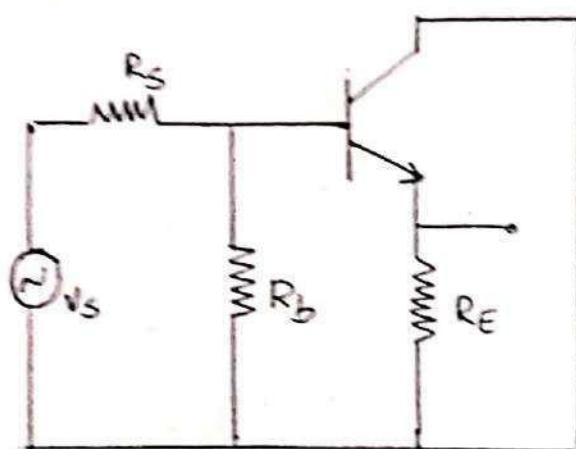
→ C_2 is a bypass capacitor [$C_C \rightarrow R_C$]

In [CE] C_3 was bypass $\rightarrow R_E$

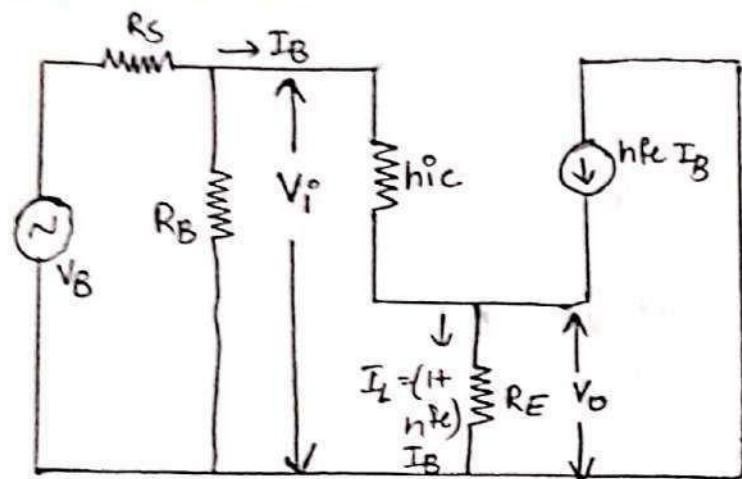
→ In order to AC equation ckt, V_{cc} node is grounded and large capacitors are s.c



→ In figure R_C is bypassed with the help of a bypass capacitor C_2 . Hence R_C becomes dead



AC Equivalent circuit



Approximate H-parameters model

1) Current gain: $A_i = \frac{I_L}{I_B}$

$$I_L = (1 + h_{fe}) I_B \Rightarrow \frac{I_L}{I_B} = 1 + h_{fe} = A_i$$

Current gain in
cc is high

2) Input resistance: $R_i = \frac{V_i}{I_B}$

Apply KVL in I/P Loop

$$V_i = I_B \cdot h_{ie} - (1 + h_{fe}) I_B \cdot R_E = 0$$

$$V_i = I_B [h_{ie} + ((1 + h_{fe}) R_E)]$$

$$\boxed{\frac{V_i}{I_B} = h_{ie} + (1 + h_{fe}) R_E}$$

3) Voltage gain: $A_{Vi} = \frac{V_o}{V_i}$

$$\frac{V_o}{V_i} = \frac{(1 + h_{fe}) I_B \cdot R_E}{I_B [h_{ie} + ((1 + h_{fe}) R_E)]}$$

$$A_{Vi} = \frac{(1 + h_{fe}) R_E}{h_{ie} + ((1 + h_{fe}) R_E)}$$

Assuming $h_{ie} \ll (1 + h_{fe}) R_E$

$$A_{Vi} = \frac{(1 + h_{fe}) R_E}{(1 + h_{fe}) R_E} \approx 1$$

→ CC amplifier has unity voltage i.e. output voltage (V_o) follows the input voltage. Hence it is called "Emitter Follower Circuit"

$$A_{VS} = A_{Vi} \times \frac{V_i}{V_s} = A_{Vi} \times \frac{R'_i}{R_s + R'_i} \quad R'_i = R_i \parallel R_B \quad (14)$$

4) Output resistance

Apply KVL.

$$I_B R'_S + I_B h_{ie} + V_x = 0$$

$$V_x = -I_B R'_S - I_B h_{ie}$$

$$V_x = -I_B (R'_S + h_{ie})$$

Apply KCL at E

$$I_B + h_{fe} I_B + I_x = 0$$

$$I_x = -I_B - h_{fe} I_B = -I_B (1+h_{fe})$$

$$R_o = \frac{V_x}{I_x} = \frac{-I_B (R'_S + h_{ie})}{-I_B (1+h_{fe})} = \frac{R'_S + h_{ie}}{1+h_{fe}} \quad \because R'_S = R_B \parallel R_S$$

1) CC Amplifier → Voltage gain is unity

2) Current gain is high

3) I/P impedance is high

4) O/P resistance is low

AC Analysis of Common base:

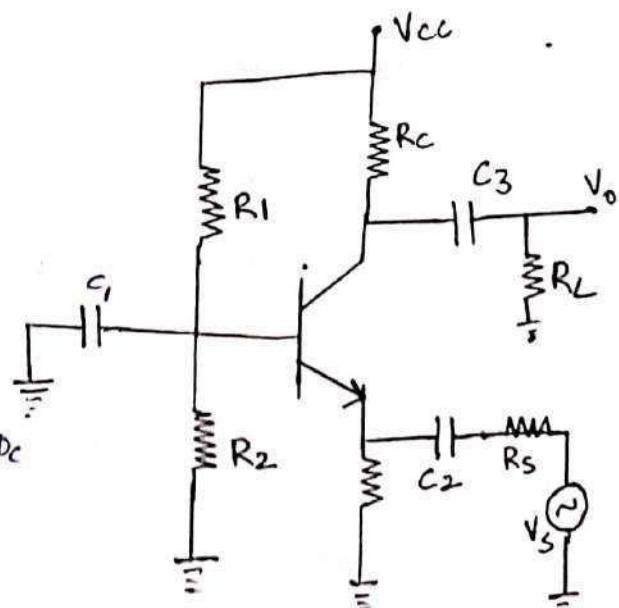
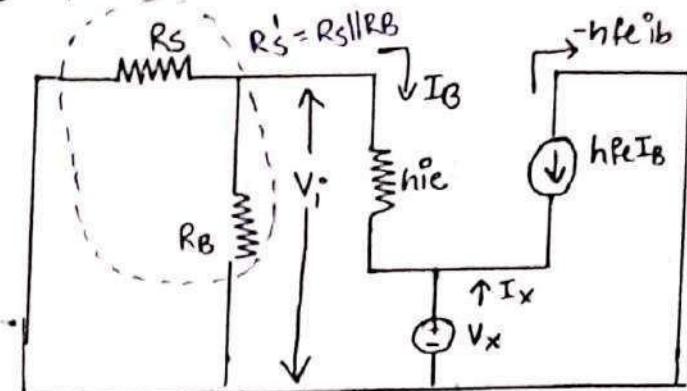
1) In order to draw AC equivalent ckt

C_1, C_2, C_3 are s.c

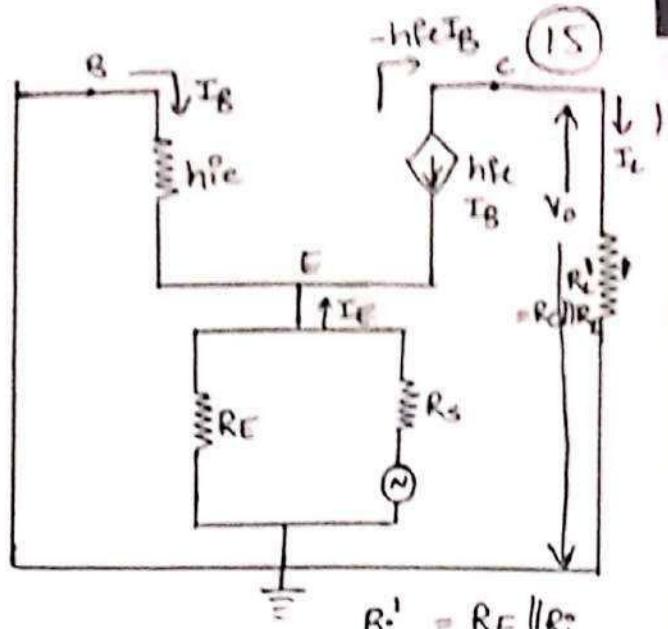
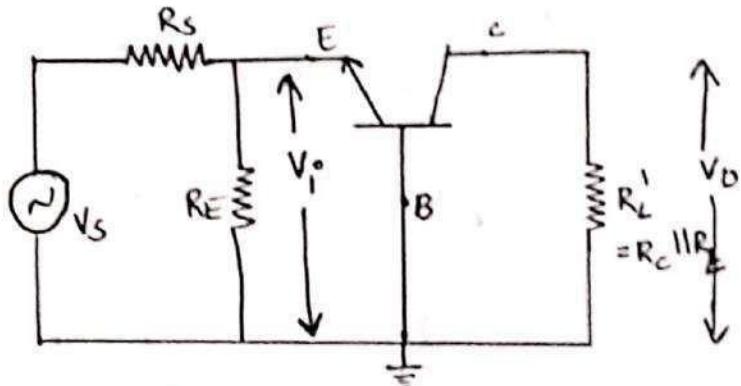
2) C_2, C_3 acts as coupling capacitors / blocks DC

3) C_1 bypasses resistors R_1 & R_2 .

Hence R_1, R_2 acts as de-dc because



bypass capacitors isn't parallel
 → The AC Eq circuit is shown below.



i) Current gain: $A_i = \frac{I_L}{I_E}$

$$I_L = -h_{fe} \cdot I_B \quad \text{---(1)}$$

Apply KCL at E

$$I_B + I_E + h_{fe} I_B = 0 \Rightarrow I_E = -I_B - h_{fe} I_B$$

$$I_E = -I_B (1 + h_{fe}) \quad \text{---(2)}$$

$$A_i = \frac{\text{---(1)}}{\text{---(2)}} = A_i = \frac{h_{fe} \cdot I_B}{I_B (1 + h_{fe})} \Rightarrow A_i = \frac{h_{fe}}{1 + h_{fe}} = \frac{h_{fe}}{h_{fe}} = 1$$

Common base has unity current gain

ii) Input Resistance: $R_i = \frac{V_i}{I_E}$

$$\text{Apply KVL, } -I_B h_{ie} - V_i = 0 \Rightarrow V_i = -I_B h_{ie} \quad \text{---(3)}$$

$$\frac{\text{---(3)}}{\text{---(2)}} R_i = \frac{-I_B h_{ie}}{I_B (1 + h_{fe})} \quad R_i = \frac{h_{ie}}{1 + h_{fe}}$$

iii) Voltage gain: $A_{Vi} = \frac{V_o}{V_i} \quad V_o = -h_{fe} I_B \cdot R'_L \quad \text{---(4)}$

$$A_V = \frac{\text{---(4)}}{\text{---(3)}} = \frac{h_{fe} I_B R'_L}{I_B h_{ie}}$$

$$A_{Vi} = \frac{h_{fe} R'_L}{h_{ie}}$$

In CB Amplifier Voltage gain is positive i.e., there is zero phase shift between I/P V and O/P V

Input resistance:

$$R_i = \frac{V_x}{I_x}$$

I/P loop KVL

$$I_B h_{ie} + (1+h_{fe}) I_B R_S' = 0$$

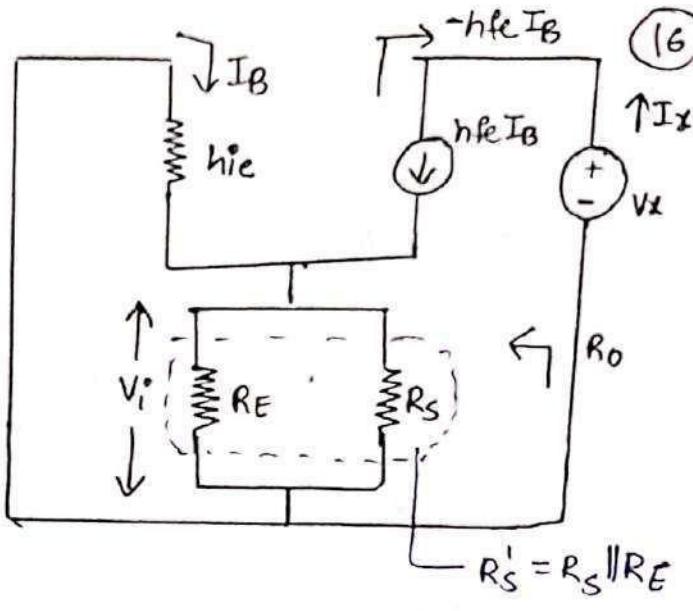
$$I_B = 0$$

$$I_x = -h_{fe} I_B = 0$$

$$R_i = \frac{V_x}{I_x} = \infty$$

$$R_o' = R_o \parallel R_c$$

$$R_o' = R_c$$



$$R_o' = R_o \parallel R_c$$

- * Common emitter configuration is superior because it provides both voltage and current amplification. In CE both voltage gain and current gain is high.
- * In CE Amplifier it has highest power gain
- * Miller effect - At high frequency it has defect

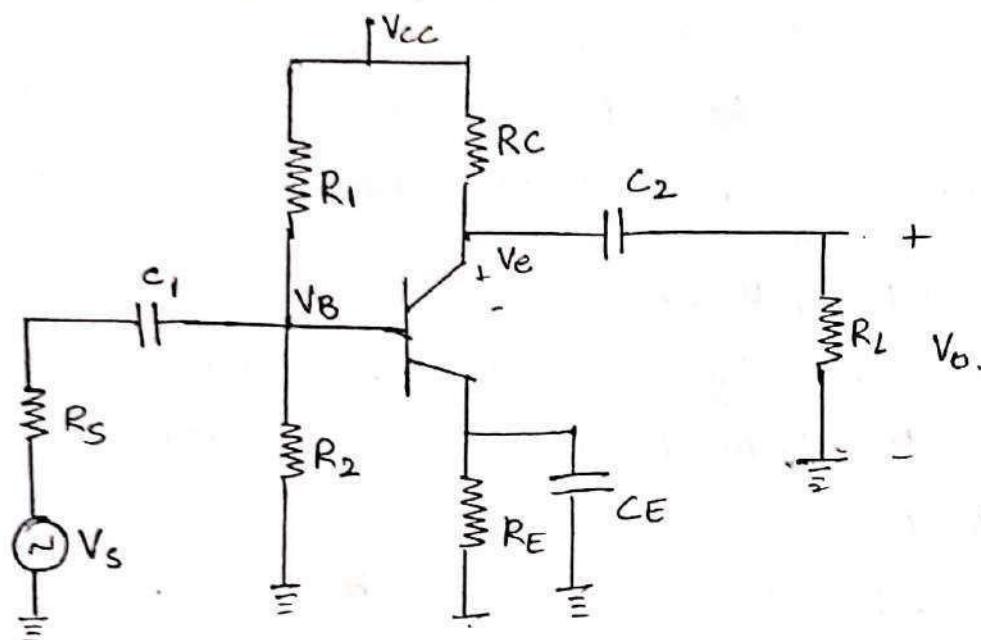
$$A_p = A_v \times A_i$$

	CE	CB	CC
A _v	large	large	1
A _i	large	1	large
R _i	Moderate	Small	large
R _o	Moderate	Large	Small
Application	Amplifiers	Current buffer	Voltage buffer

Low Frequency Analysis of CE Amplifier

- At low frequency large capacitors offer considerable reactance.
- Hence the effect of large capacitors is considered in low frequency analysis of RC coupled CE amplifier

RC Coupled CE Amplifier :



In above figure shows the practical circuit of common emitter transistor amplifier. It consists of different circuit components as follows

i) Biasing Circuit

→ The resistances R_1, R_2, R_E form the voltage divider biasing circuit

→ The function of biasing circuit is to set proper operating point for CE amplifier so that we get distortion less output

ii) Input Capacitor C_1 :

→ The input capacitor C_1 it couples the signal to base of transistor

- It blocks any DC component present in the input signal and passes only AC signal for amplification
- It also prevents the operating point being disturbed (V_B, I_B)
- iii) Emitter Bypass Capacitor C_E :
- It is connected in parallel to emitter resistance R_E and it provides a low reactance path to the amplified AC signal
- If it is not present the amplified signal will pass through R_E which result in voltage drop across it. Hence the O/P voltage reduces. $\downarrow A_V = \frac{V_{O\downarrow}}{V_i}$ and voltage gain also reduces

- iv) Output coupling capacitor C_2 :

If couples the output of amplifier to the load (or) to the next stage of amplifier. It blocks the DC component and passes only the AC

Q (V_{CE}, I_C)

All are DC components which keep Q point stable. If one disturbs everything disturbs and Q points will not be in stable

$\left. \begin{array}{l} V_{CC} \\ I_C \\ V_{BE} \\ I_B \\ V_{CE} \end{array} \right\}$

If $V_{in} =$ DC component

$$X_C = \frac{1}{2\pi f_C} \quad f = 0 \text{ in DC}$$

$X_C = \infty$ Hence C becomes DC and OC

→ AC - SC (capacitor)

→ DC-OC (capacitor)

→ It is known as RC coupled CE amplifier because the amplifier and load is connected by capacitors

→ C_1 blocks input DC and prevents in disturbance

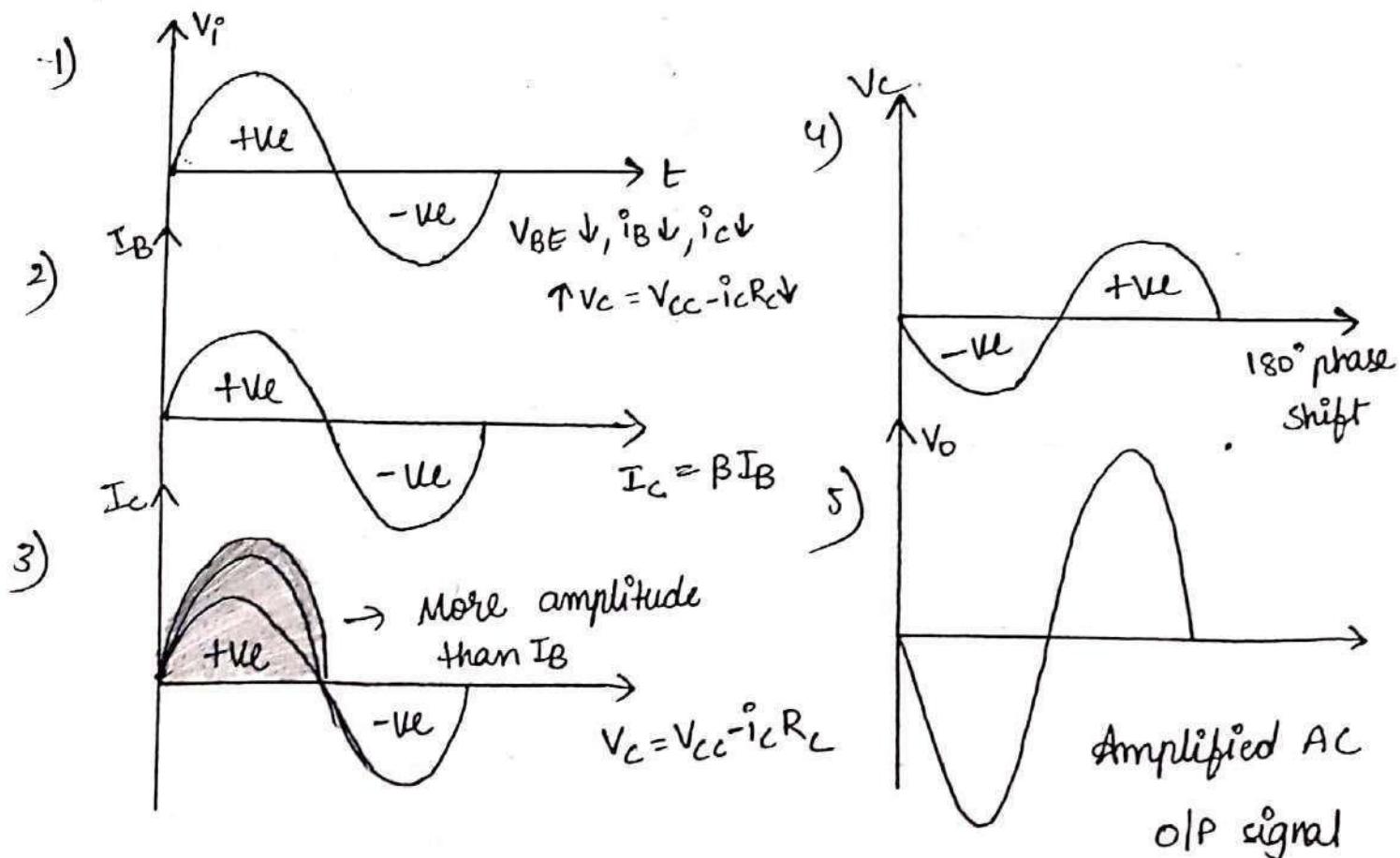
If $V_B \downarrow i_B \downarrow$ then Q point also disturbs. It couples input to base.

Working of CE Amplifier:

→ Here the I/p V_i is applied to the base via C_1 . When V_i increases in positive direction the input junction becomes F.B and increases V_{BE}

→ With increase in V_{BE} , i_B increases. Hence i_c increases ($i_c = \beta i_B$) thereby the voltage drop across R_C increases and V_C decreases i.e. ($V_C = V_{CC} - i_c R_C$)

→ When V_i increases in positive direction in negative direction thus we can say that there is 180° phase shift (OPP) between input & output

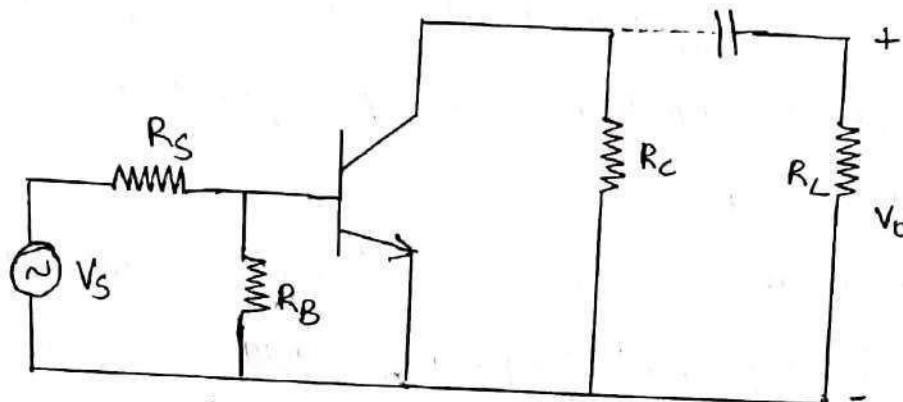


An RC coupled CE Amplifier has 3 large capacitors

(20)

- i) Input coupling (or) Blocking capacitor (C_B)
- ii) Output coupling capacitor (or) coupling capacitor (C_C)
- iii) Emitter - Bypass capacitor (C_E)

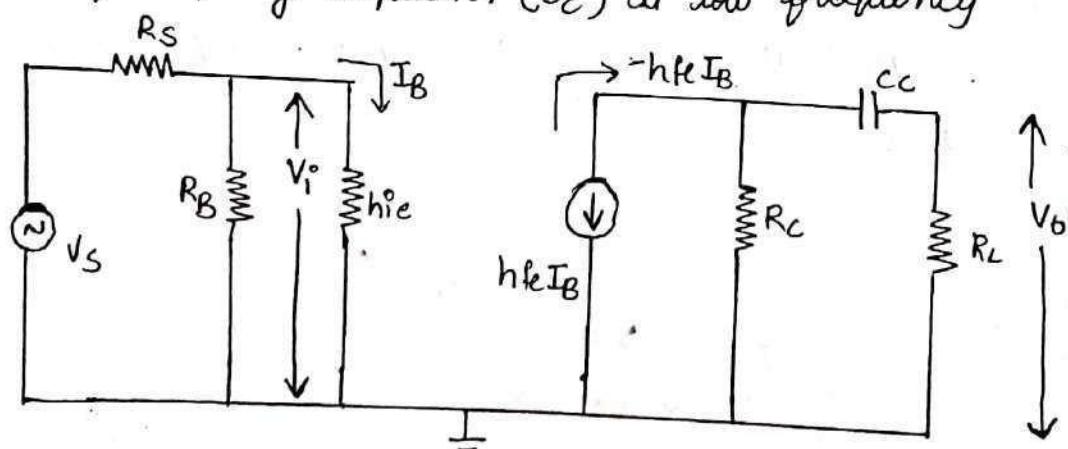
1)



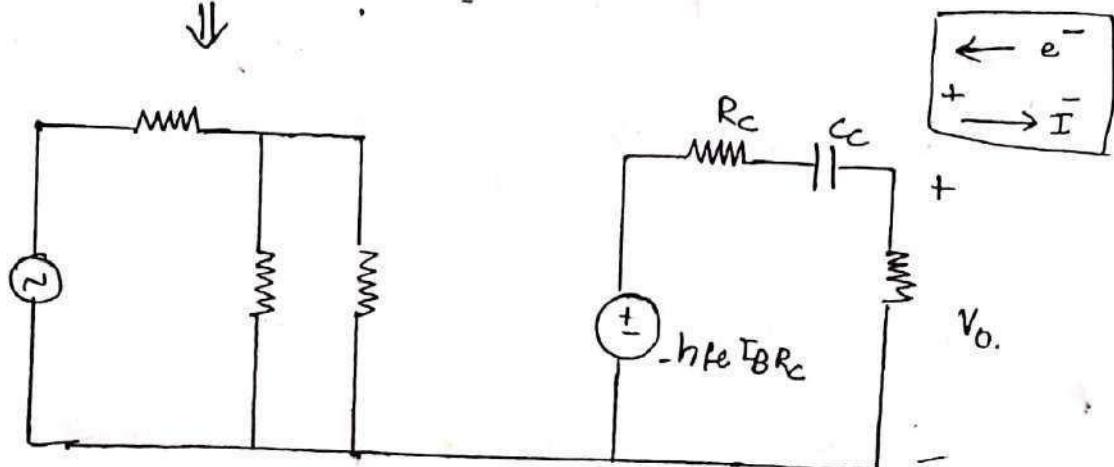
Low frequency AC equivalent circuit

Effect of coupling capacitor (C_C) at low frequency

2)



3)



Current source $-h_{FE} I_B$ can be replaced with voltage source

→ Coupling capacitor (C_C) & R_C forms a high pass RC network at low frequency

→ If frequency is low then reactance of (C_C) increases, hence voltage drop across (C_C) increases and in order to satisfy KVL the voltage drop across (R_C) decreases i.e. V_o decreases
 $f \downarrow, X_C \uparrow, \text{ voltage drop across } C_C \uparrow$

$$V_o \downarrow, A V_i \downarrow = \frac{V_o \downarrow}{V_i}$$

Hence voltage gain of RC coupled amplifier decreases at low frequency due to large capacitors such as coupling capacitors.

$$V_o = \frac{-h_{FE} I_B \cdot R_C \cdot R_L}{R_C + R_L - jX_C}$$

$$V_o = \frac{-h_{FE} I_B \cdot R_C R_L}{R_C + R_L - jX_C \times \frac{j}{j}} = \frac{-h_{FE} I_B R_C R_L}{R_C + R_L + \frac{X_C}{j}}$$

$$V_o = \frac{-h_{FE} I_B R_C R_L}{R_C + R_L + \frac{1}{j\omega C_C}} = \frac{-h_{FE} I_B \cdot (R_C \cdot R_L)}{(R_C + R_L) \left[1 + \frac{1}{j\omega C_C (R_C + R_L)} \right]}$$

$$R'_L = R_C // R_L$$

$$= \frac{-h_{FE} I_B R'_L}{1 + \frac{1}{j\omega C_C (R_C + R_L)} \times \frac{j}{j}}$$

Multiply & divide j

$$V_o = \frac{-h_{FE} \cdot I_B R'_L}{1 - \frac{j}{\omega C_C (R_C + R_L)}} \quad -①$$

$$V_i = I_B \times h_{ie} \quad -②$$

$$A_{VL} = \frac{-h_{FE} \frac{R_L'}{I_B \cdot h_{ie}}}{1 - j \frac{1}{\omega_{CC}(R_C + R_L)}} = \frac{-h_{FE} R_L'}{h_{ie}} \cdot \frac{1}{1 - j \frac{1}{\omega_{CC}(R_C + R_L)}}$$

↓
low frequency

$$\omega_L = \frac{1}{C_C (R_C + R_L)}$$

$$A_{Vm} = \frac{-h_{FE} R_L'}{h_{ie}}$$

$$A_{VL} = A_{Vm} \cdot \frac{1}{1 - j \frac{\omega_L}{\omega}}$$

$$A_{VL} = A_{Vm} \cdot \frac{1}{1 - j \frac{f_L}{f}}$$

$$|A_{VL}| = \frac{|A_{Vm}|}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}}$$

→ voltage gain at low frequency

$$\angle A_{VL} = 180^\circ + \tan^{-1} \left(\frac{f_L}{f} \right)$$

→ phase shift at low frequency

If $f_L = f$

$$|A_{VL}| = \frac{|A_{Vm}|}{\sqrt{2}}$$

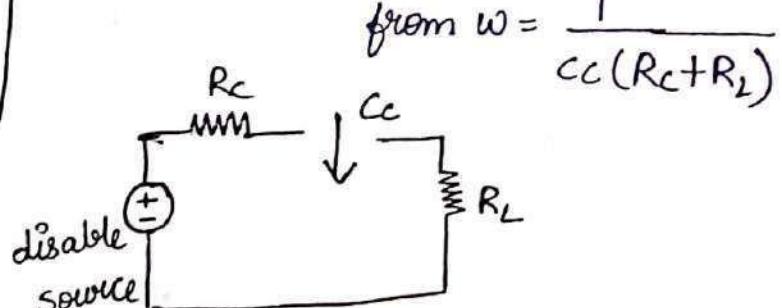
The frequency at which the voltage gain becomes $\frac{|A_{Vm}|}{\sqrt{2}}$ is known as cutoff frequency (or) 3dB frequency

f_L = lower cutoff frequency or

lower 3dB frequency of RC coupled CE amplifier

$$f_L = \frac{1}{2\pi C_C (R_C + R_L)}$$

$$f = \frac{1}{2\pi R C_C}$$



Effect of I/P coupling capacitor or (C_B)

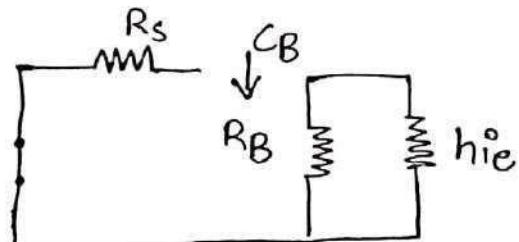
(23)

$$f_{L_2} = \frac{1}{2\pi R \cdot C_B}$$

R is the resistance seen by the blocking capacitor

$$R = R_s + (R_B \parallel h_{ie})$$

Effect of Emitter - Bypass capacitor (C_E):



If the effect of C_E is considered then

$$f_{L_3} = \frac{1}{2\pi R C_E}$$

$$R = \frac{R_s^1 + h_{ie}}{1+h_{fe}} \parallel R_E \quad [\text{common collector } R_o]$$

$$\boxed{\text{NET } f_L = 1.1 \times \sqrt{f_{L_1}^2 + f_{L_2}^2 + f_{L_3}^2}}$$

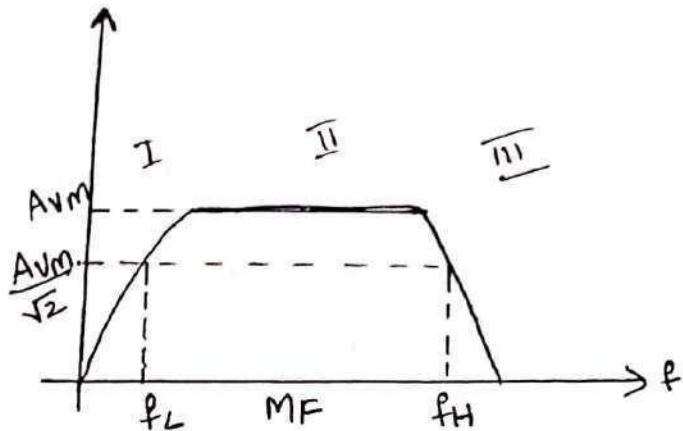
Frequency Response of RC coupled Amplifier :

It is a plot of voltage gain magnitude (V_s) frequency
It consists of 3 regions

- i) Low frequency Region where voltage gain decreases due to large capacitors such as coupling capacitors.
- ii) Medium frequency region where voltage gain is maximum and constant, i.e., A_v is independent of frequencies because capacitors have negligible effect.

iii) High frequency Region where voltage gain decreases due to small capacitors.

(24)



RC coupled amplifier has two cutoff frequency f_L & f_H

→ Difference between f_L & f_H is called as 3dB Band width

$$B.W = f_H - f_L$$

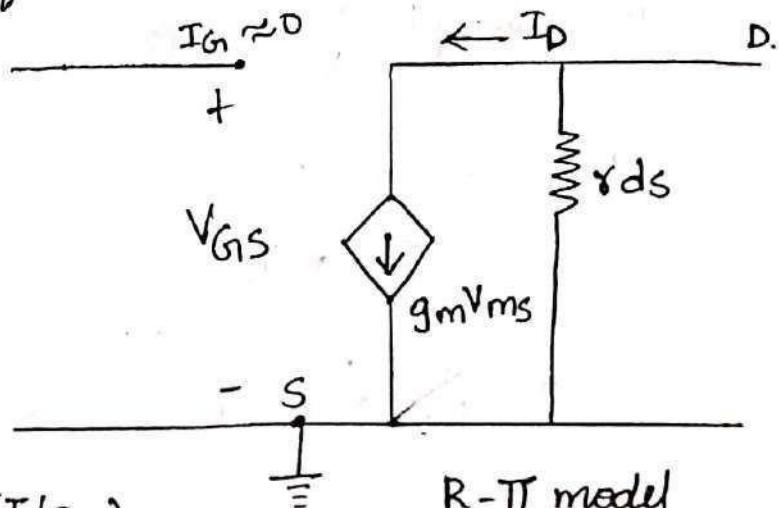
A_{Vm} = Mid band voltage gain

UNIT-5. FET AMPLIFIERS

Small Signal Model of JFET:

Small signal model is the equivalent circuit of FET which is used for analysis purpose.

The small signal model of FET is shown below



Here g_m , r_{ds} are the small signal FET parameters

1) Transconductance of FET (g_m): R- π model

→ It is defined as the change in drain current for a given change in gate to source voltage keeping ~~down~~ drain to source voltage constant.

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \quad | \quad V_{DS} = \text{constant}$$

→ g_m is also known as slope of the transfer characteristics of FET.

→ The drain current for FET is given by

$$I_{DS} = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2 \quad \text{--- (1)}$$

diff eq ① w.r.t to V_{GS}

②

$$\frac{\partial I_{DS}}{\partial V_{GS}} = \frac{\partial I_{DSS}}{|V_P|} \left[1 - \frac{V_{GS}}{V_P} \right]$$

$$g_m = \frac{\partial I_{DS}}{V_P}$$

$$g_m = m \frac{A}{V}$$

$$g_m = \text{milli siemens}$$

$$g_m = g_m \left[1 - \frac{V_{GS}}{V_P} \right] - ②$$

$$g_m = \frac{\partial I_{DSS}}{|V_P|} \sqrt{\frac{I_{DS}}{I_{DSS}}}$$

$$g_m = \frac{2}{|V_P|} \sqrt{I_{DS} \cdot I_{DSS}} - ③$$

2) Dynamic drain resistance (r_{DS}) :

It is defined as the reciprocal of the slope of drain characteristics of FET

$$r_{DS} = \frac{1}{\text{slope of drain characteristics}}$$

$$= \frac{1}{\frac{\partial I_{DS}}{\partial V_{DS}}} \Big|_{V_{GS} = \text{constant}}$$

$$r_{DS} = \frac{\partial V_{DS}}{\partial I_{DS}}$$

(3)

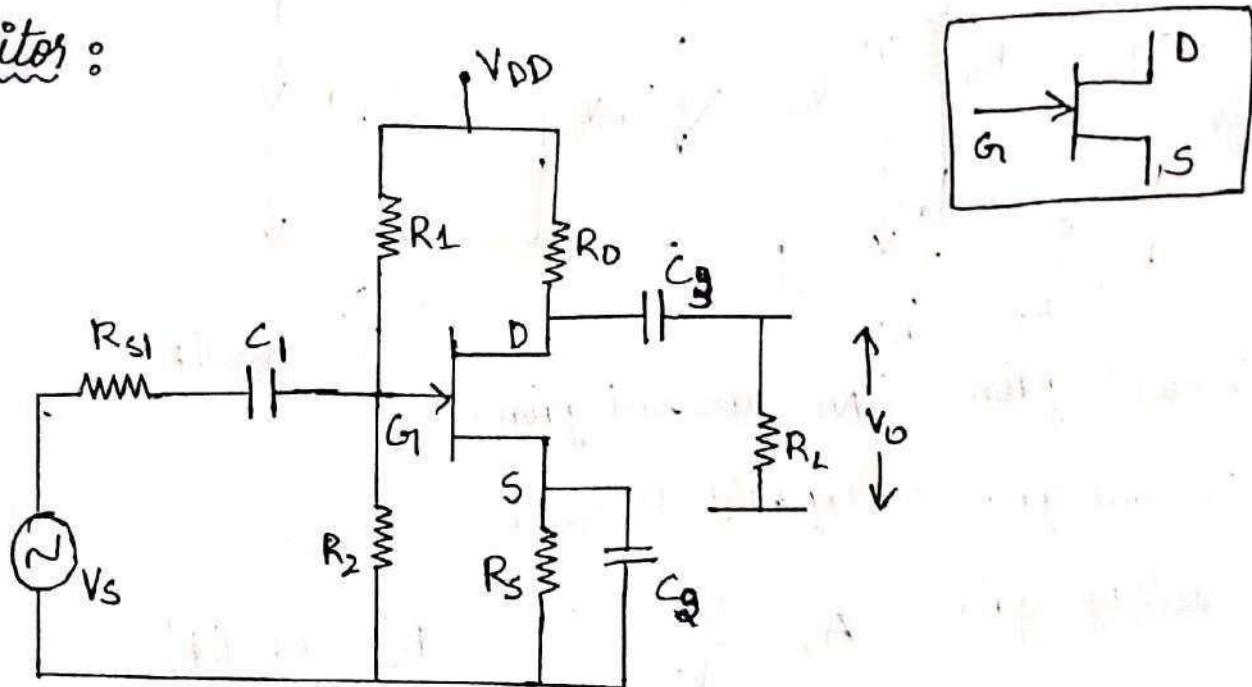
3) Amplification factor (μ):

It is defined as the product of transconductance of FET(g_m) and dynamic drain resistance (r_{ds})

$$\mu = g_m \times r_{ds}$$

$$\mu = \frac{\partial I_{DS}}{\partial V_{GS}} \times \frac{\partial V_{DS}}{\partial I_{DS}} \Rightarrow \mu = \frac{\partial V_{DS}}{\partial V_{GS}}$$

Analysis of Common Source Amplifier with bypass capacitors:

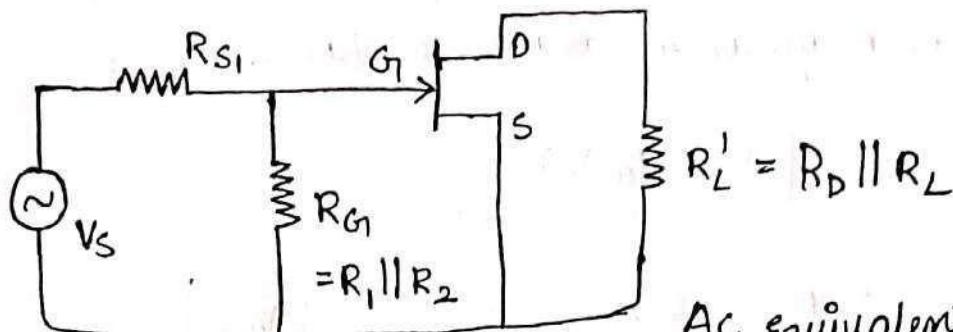


Here the Input Node - Gate ; output drain ->
output Node - drain

- C_1, C_2, C_3 are the large capacitors connected
- Here C_2 is called "bypass capacitor"
- C_1, C_3 are called as I/P, O/P [coupling] capacitors

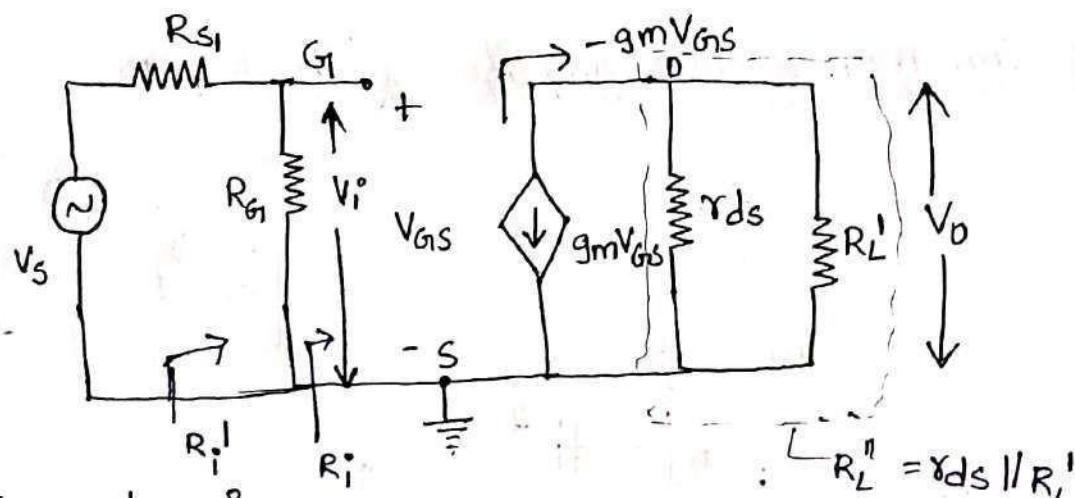
→ In order to draw AC equivalent circuit replace all the large capacitors with S.C and V_{DD} to ground

(4)



AC equivalent Circuit

→ Replace FET with small signal model



i) Current gain: (No current gain)

Current gain is infinity as $I_{G1} = 0$

ii) Voltage gain: $A_V = \frac{V_o}{V_i}$ $R_L'' = r_{ds} || R_L'$

$$V_o = -g_m V_{GS} R_L''$$

$$R_L'' = r_{ds} || R_L'$$

$$R_L' = R_D || R_L$$

$$V_i = V_{GS}$$

$$A_V = \frac{-g_m V_{GS} R_L''}{V_{GS}}$$

$$A_V = -g_m R_L''$$

"-ve" sign indicates there is a phase shift of input and output voltage

if $R_L = 0$

$$A_V = -g_m R_L'$$

$$\begin{aligned} \therefore R_L'' &= r_{ds} \parallel R_L' \\ &= 0 \parallel R_L' \end{aligned}$$

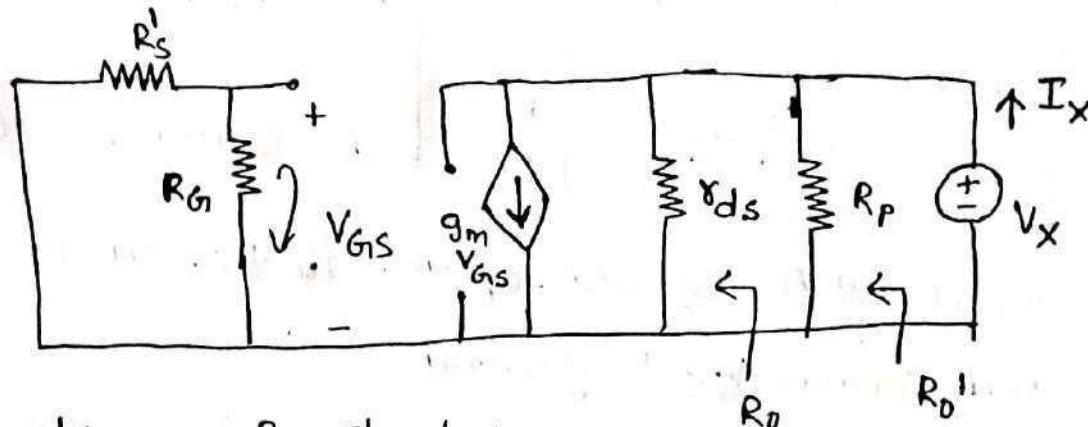
III) Input resistance:

$$R_i = \infty \text{ because } \frac{V_{GS}}{I_G} = \frac{V_{GS}}{0}$$

$$R_i' = R_G$$

IV) Output Resistance:

- 1) disable V_S
- 2) disconnect only load " R_L ".
- 3) Apply a voltage source V_x across the load and redraw the circuit



Apply KVL in I/P loop ($I_G \times R_G = 0$)

$$V_{GS} = 0$$

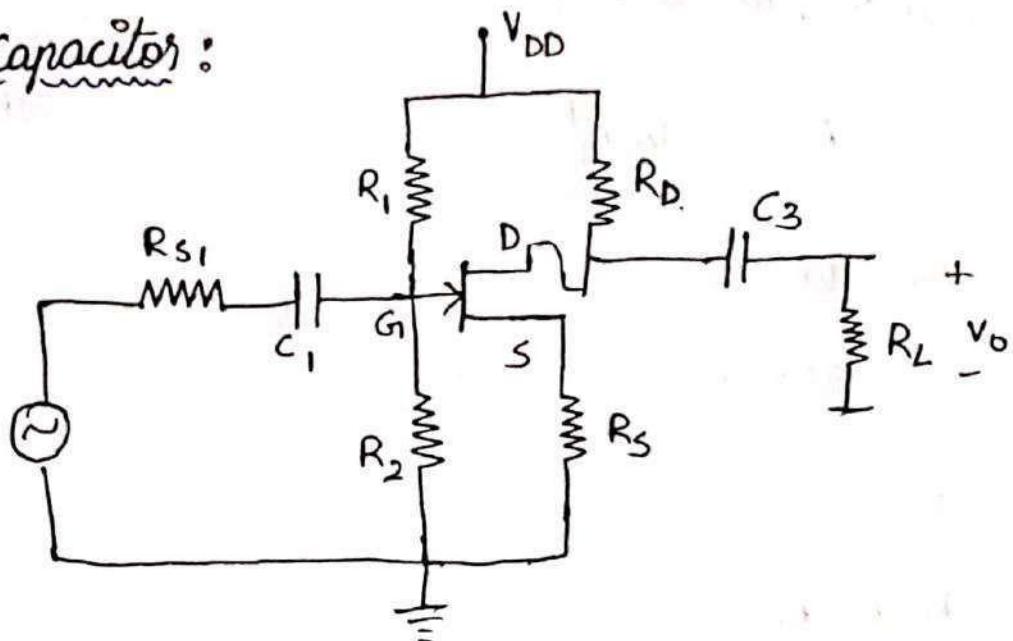
Hence the dependent current source with o.c (since $V_{GS} = 0$)

$$R_0 = r_{ds}$$

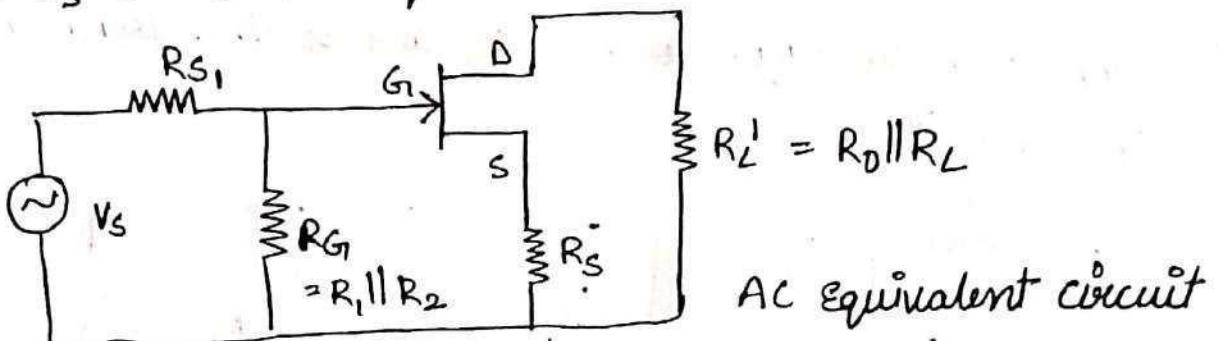
$$R_0' = r_{ds} \parallel R_0$$

$$V_{GS} = 0$$

Analysis of Common Source Amplifiers without bypass capacitor:

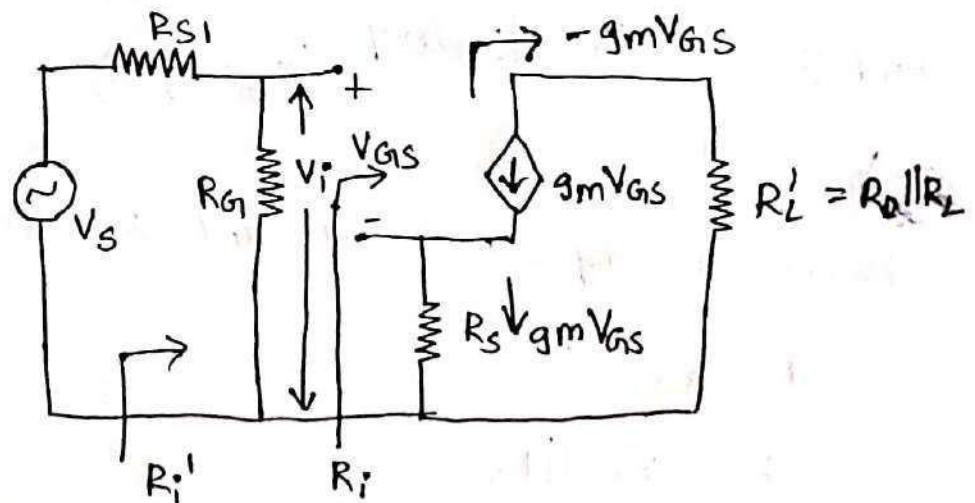


→ In this case the bypass capacitor C_2 is removed. Hence effect of R_s comes into picture.



→ In order to draw AC eq. ckt replace all the large capacitors with s.c and connect V_{DD} to ground

→ In order to draw small signal model replace FET with its equivalent small signal model



I) Voltage gain : $A_V = \frac{V_O}{V_i}$

$$R_L' = R_D \parallel R_L$$

$$V_O = -g_m V_{GS} \cdot R_L' \quad \text{--- (1)}$$

$$V_i = V_{GS} + g_m V_{GS} \cdot R_S$$

$$V_i = V_{GS} (1 + g_m R_S) \quad \text{--- (2)}$$

$$A_V = \frac{(1)}{(2)} = \frac{-g_m V_{GS} R_L'}{V_{GS} (1 + g_m R_S)} \Rightarrow$$

$$A_V = \frac{-g_m R_L'}{1 + g_m R_S}$$

when bypass capacitor is not present

R_S decreases the voltage drain

II) Input resistance :

As the I/P current $I_{G1} = 0$, input resistance $R_i^o = \infty$

$$\text{and } R_i^o = R_G$$

III) Output resistance :

In order to calculate O/P resistance

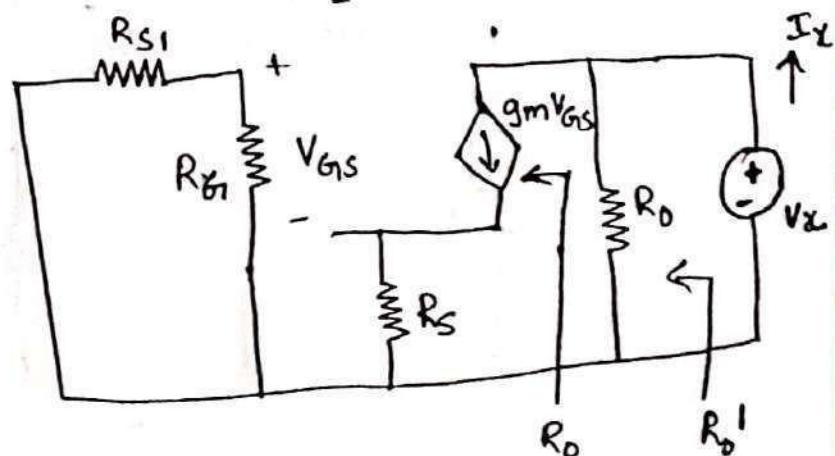
i) disable voltage source

ii) disconnect R_L and connect V_x across R_L

$$R_o = \infty$$

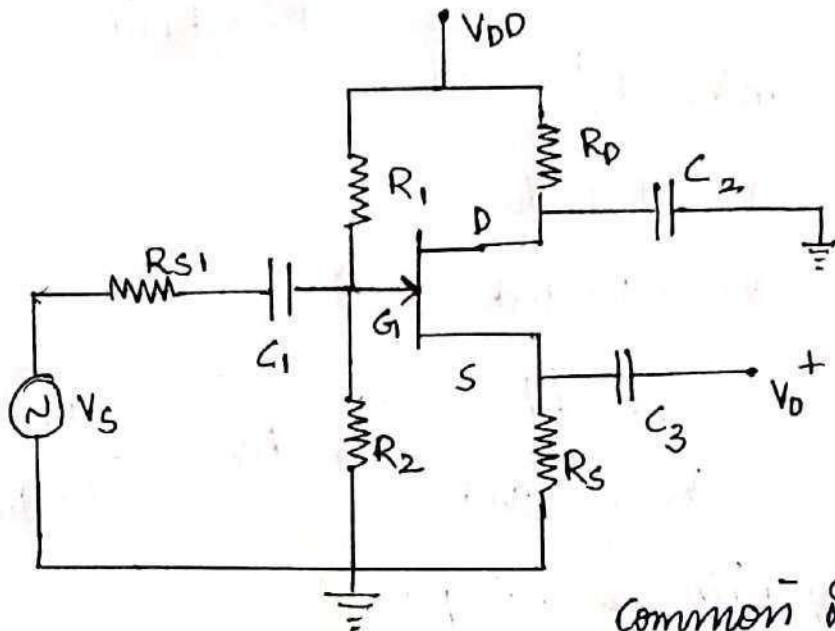
$$R_o' = R_D \parallel R_L$$

$$R_o' = R_D$$



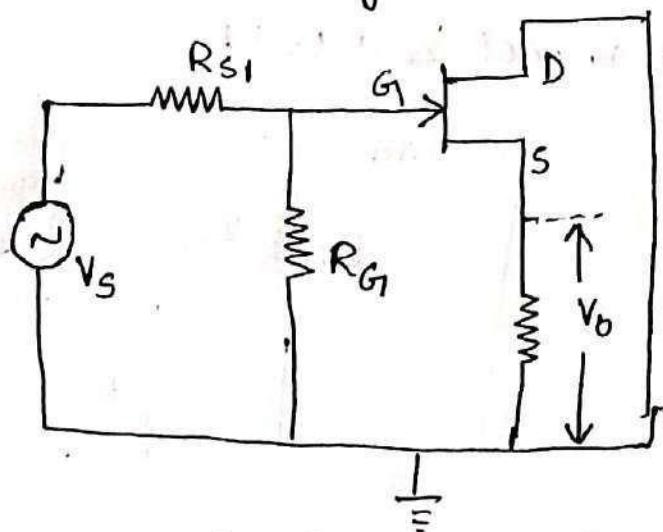
Analysis of Common Drain Amplifiers

(8)



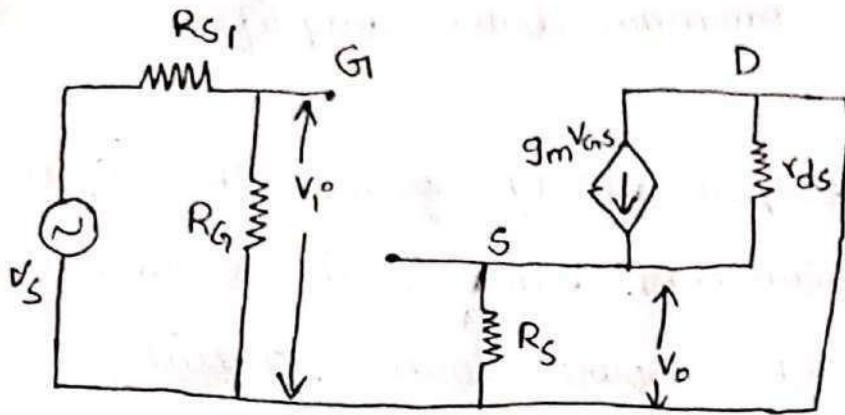
Common Drain

- Here the input node is GATE and the output node is source
- C_1 and C_3 are the input and output coupling capacitors
- C_2 is the bypass capacitor
- In order to draw the AC equivalent circuit, connect all the large capacitors as short circuit
- Connect V_{DD} node to ground

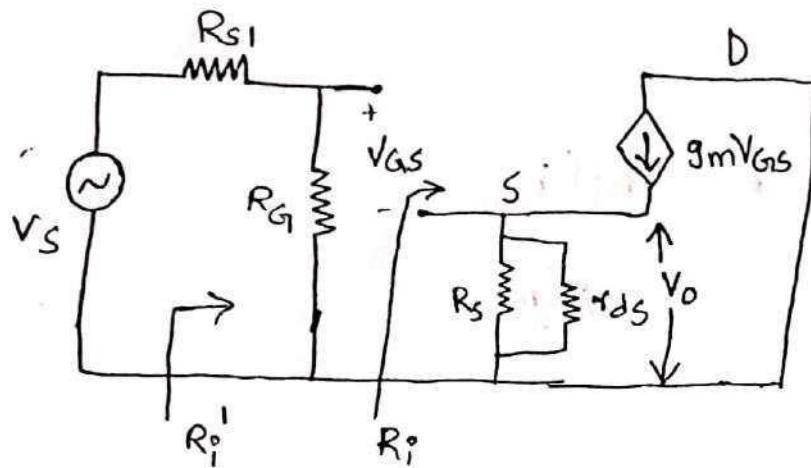


- Replace FET with its small signal model.

9



↓

 R_S & r_{ds}

are parallel

i) Current gain: No current gain

ii) Voltage gain: $A_V = \frac{V_o}{V_i}$

$$V_o = g_m V_{GS} (R_S \parallel r_{ds}) \quad \text{--- (1)}$$

$$V_i = V_{GS} + g_m V_{GS} (R_S \parallel r_{ds})$$

$$V_i = V_{GS} (1 + g_m (R_S \parallel r_{ds})) \quad \text{--- (2)}$$

$$A_V = \frac{g_m (R_S \parallel r_{ds})}{1 + g_m (R_S \parallel r_{ds})} \approx 0.99 = 1$$

If r_{ds} is not present,

$$A_V = \frac{g_m R_S}{1 + g_m R_S}$$

$$\boxed{A_V = 1}$$

$$\boxed{V_o = V_i}$$

The voltage gain of common drain amplifier is slightly less than.

$A_v \approx 1$ i.e. the output voltage follows the input voltage. Hence the common drain circuit is known as "SOURCE FOLLOWER" (source follower circuit)

iii) Input resistance: (R_i)

$$R_i = \frac{V_i}{I_{G_1}} \quad I_{G_1} \approx 0$$

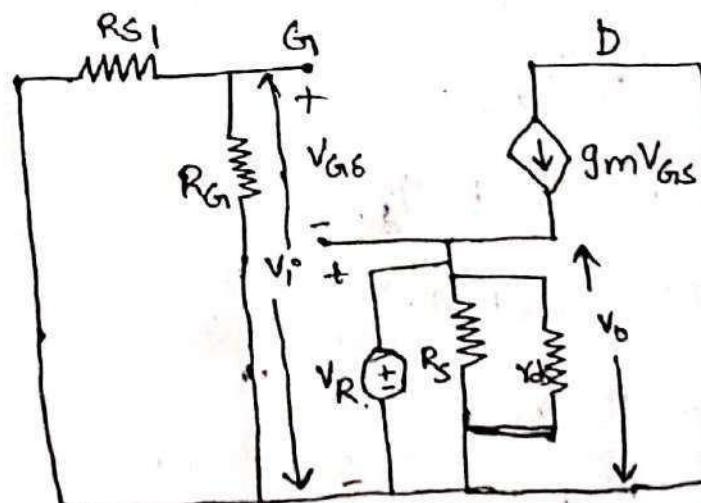
$$R_i = \frac{V_i}{0} = \infty \quad R'_i = R_i \| R_{G_1}$$

$R'_i = R_{G_1}$

High

iv) Output resistance:

In order to calculate the output resistance disable the voltage source V_s . Disconnect the load. Apply a voltage source V_x



KVL to V_i loop

$$-V_{Gis} - V_x = 0$$

$$V_{Gis} = -V_x$$

Apply KCL

$$I_X = \frac{V_S}{R_S} + \frac{V_S}{R_{DS}} - g_m V_{GS}$$

$$I_X = \frac{V_X}{R_S} + \frac{V_X}{r_{DS}} + g_m V_{SC}$$

$$I_X = V_X \left[\frac{1}{R_S} + \frac{1}{r_{DS}} + \frac{1}{1/g_m} \right]$$

$$\frac{I_X}{V_X} = \frac{1}{R_S} + \frac{1}{r_{DS}} + \frac{1}{1/g_m}$$

$$R_0 = \frac{V_X}{I_X} \left[R_S \parallel r_{DS} \parallel \frac{1}{g_m} \right]$$

without R_S , $R_0 = r_{DS} \parallel \frac{1}{g_m}$

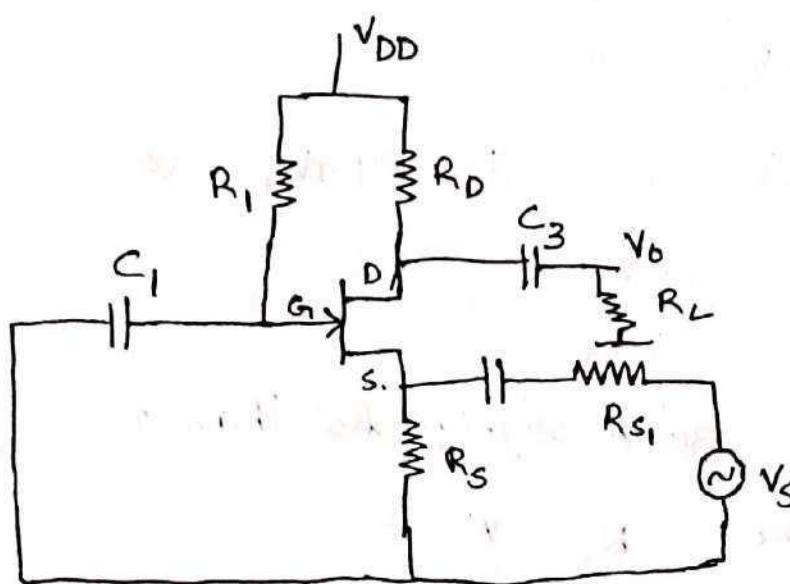
Analysis of Common Gate Amplifier

I/P - source

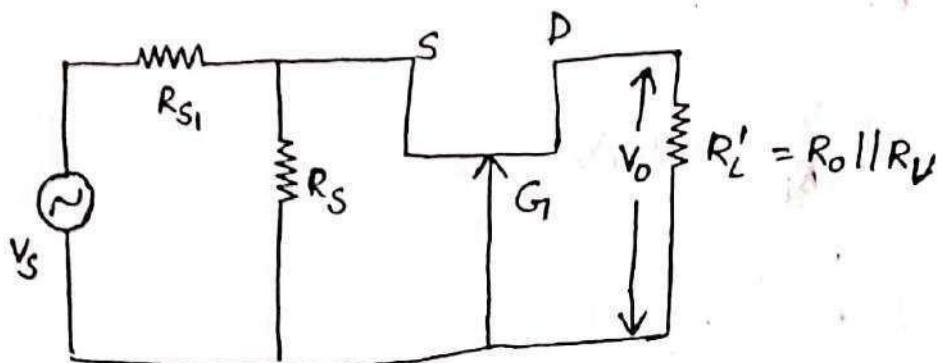
O/P - drain

C_1 - Bypass capacitor

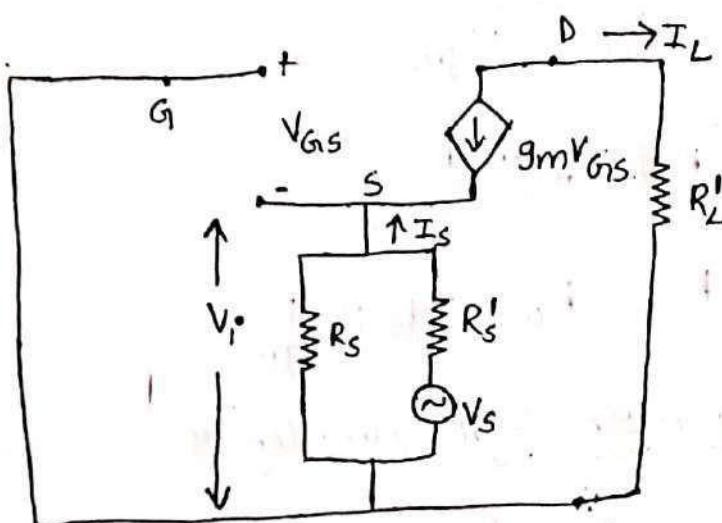
so V_P is source to ground



In order to redraw AC equivalent circuit replace all capacitors with s.c and connect V_{DD} node to ground



Replace FET transistor with small signal equivalent model



i) Current gain: $A_i = \frac{I_L}{I_S}$

$$I_L = -g_m V_{GS} \quad \textcircled{1}$$

$$I_S + g_m V_{GS} = 0 \Rightarrow I_S = -g_m V_{GS} \quad \textcircled{2}$$

$$A_i = \frac{\textcircled{1}}{\textcircled{2}} = \frac{-g_m V_{GS}}{-g_m V_{GS}} = 1$$

current gain is unity slightly less than 1

ii) Input resistance: $R_i = \frac{V_i}{I_S}$

$$-V_{GS} - V_i = 0 \Rightarrow V_i = -V_{GS} \quad \textcircled{3}$$

$$R_i = \frac{③}{②} \Rightarrow R_i = \frac{1}{g_m}$$

$$R_i' = R_i \parallel R_s, R_i' = \frac{1}{g_m} \parallel R_s$$

iii) Voltage gain: $A_V = \frac{V_o}{V_i}$

$$V_o = -g_m V_{GS} \cdot R_L' \quad \text{---(4)}$$

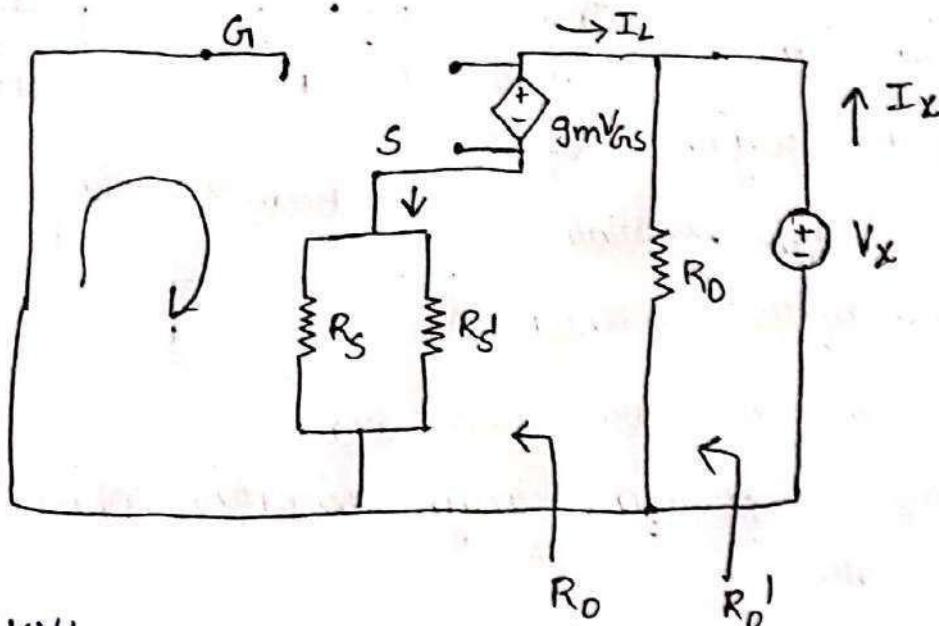
$$A_V = \frac{④}{③} = \frac{-g_m V_{GS} R_L'}{-V_{GS}}$$

$$\boxed{A_V = g_m R_L'}$$

In common gate Amplifier voltage gain is positive i.e no phase shift between V_o & V_i .

iv) Output Resistance:

In order to calculate ' R_o ' disable V_s , disconnect only R_L and connect a voltage source V_x as shown in figure below.



Apply KVL

$$V_{GS} + g_m V_{GS} \cdot R_s' = 0$$

$$V_{GS} = 0$$

when $V_{GS} = 0$, the dependent current source at op

becomes open circuit. Hence $R_o = \infty$

and $R_o' = R_o || R_D$.

$$R_o' = R_D$$

MOSFET [Metal oxide semiconductor Field Effect transistor]

Mosfet

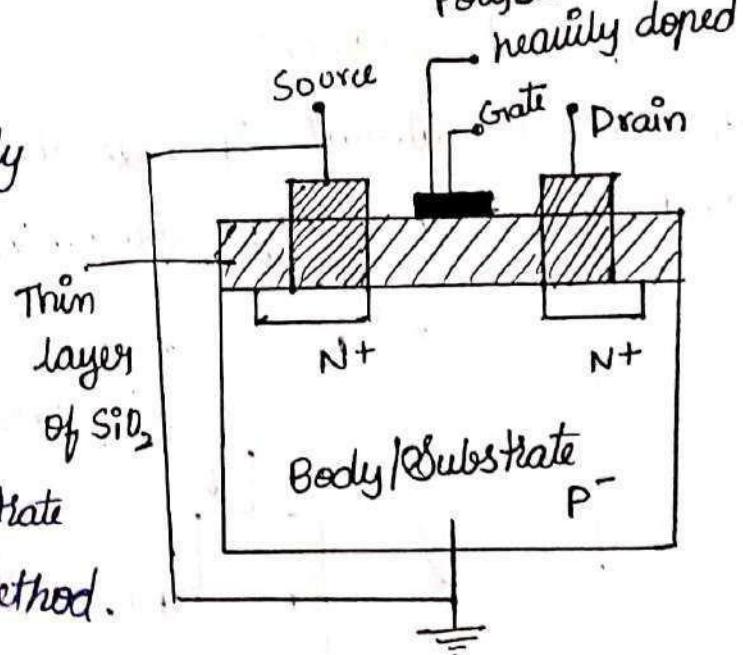
↓
Enhancement type depletion type

- N-channel E-MOSFET
- P-channel E-MOSFET

- N-channel D-MOSFET
- P-channel D-MOSFET

N-channel E-MOSFET:

It is fabricated on a lightly doped P-type semi-conductor called as body / substrate.



Two heavily doped N⁺ regions of SiO₂ are created in a P-type substrate through impurity diffusion method.

These N⁺ regions acts as source and drain.

A thin SiO₂ layer is formed through oxidation which acts as dielectric or insulator.

A part of SiO₂ is removed to create contact cuts.

A metal is disposed in these cuts to make e- contact with source drain.

Another layer of heavily doped polysilicon above SiO_2 is formed. This acts as gate. Source and body are shorted.

Enhancement MOSFET does not have physically fabricated channel but a N-channel can be created electrically by applying gate voltage.

Operation:

Two voltages V_{GS} , V_{DS} are required

→ V_{GS} is applied to create, control channel conductivity

$V_{GS} \rightarrow$ +ve N-channel
-ve P-channel

→ V_{DS} is applied to make majority carriers drift and to form I_{DS}

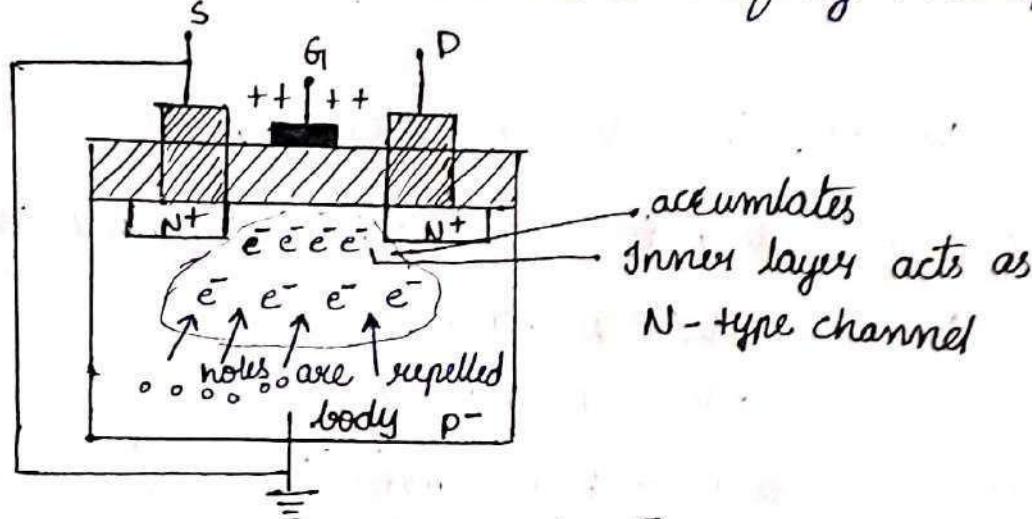
$V_{DS} \rightarrow$ +ve N-channel
-ve P-channel

Case - i: $V_{DS} = \text{const}$, V_{GS} vary

- 1) $V_{GS} = 0$ channel can't be formed $I_{DS} = 0$
- 2) V_{GS} = small +ve, +ve charge of SiO_2 will repel the holes of P-type body and the depletion region is formed between source, drain
- 3) V_{GS} = strong +ve, +ve charge of SiO_2 becomes stronger and attraction is seen in majority e^- of N^+ source, drain minority e^- of P-type substrate.

These e^- accumulate below SiO_2 and a inversion layer is formed which acts as a N-type channel

- 4) When $V_{GS} = V_T$ (threshold voltage) e^- density in the channel equals to the e^- density in the substrate. Then e^- drift from source to drain opposite direction I_{DS} flows.
- 5) As $V_{GS} \uparrow$ e^- density \uparrow in the channel e^- drifting \uparrow so $I_{DS} \uparrow$

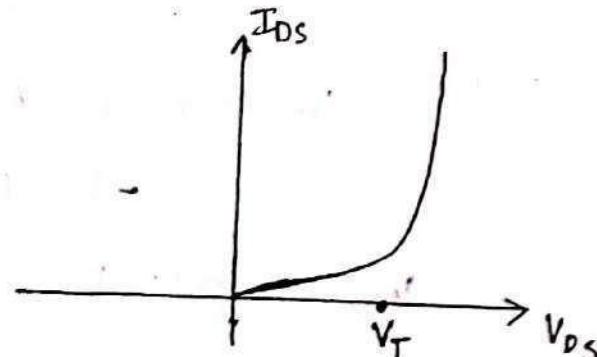


Transfer characteristics:

plot between I_{DS} , V_{GS} , V_{DS} as constant

case (ii):

$V_{GS} = \text{const}$, $V_{DS} = \text{varies}$



But, $V_{GS} > V_T$ as only then channel is created

$V_{GS} - V_T$ is the net gate voltage

Let R_{DS} be the channel resistance

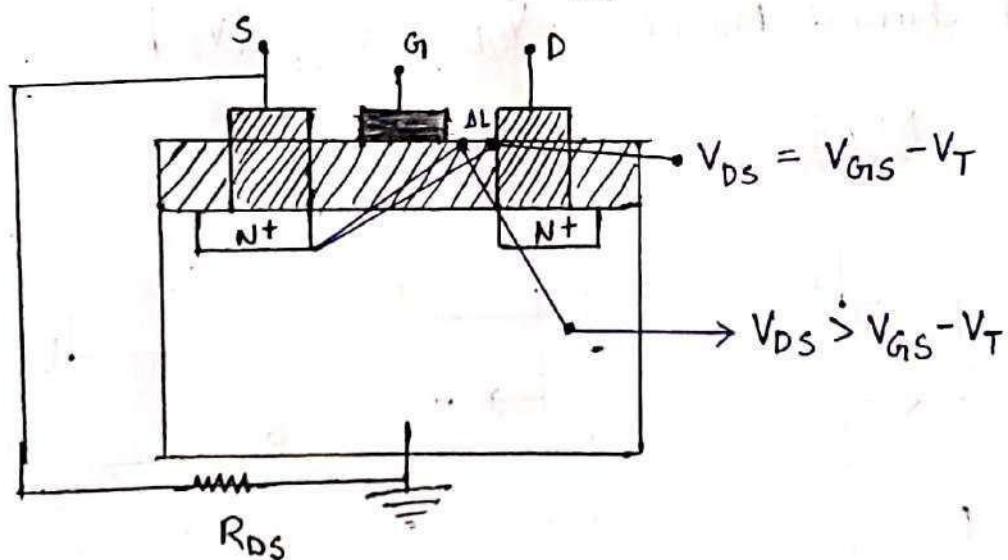
- 1) $V_{DS} = 0$, no electron drift no current
- 2) $V_{DS} = \text{small +ve}$, resistance becomes const
 I_{DS} increases linearly with V_{DS}

(17)

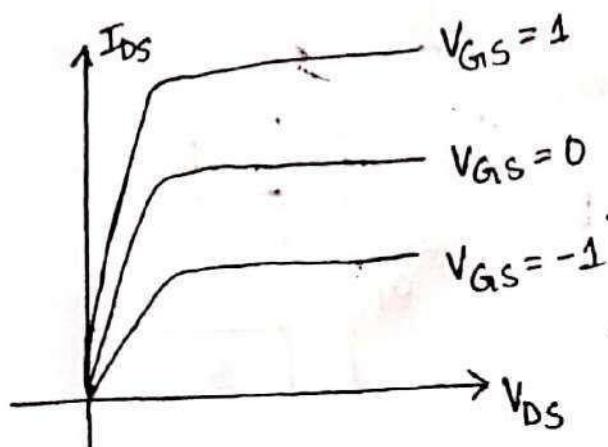
3) V_{DS} = large +ve, the gate to channel voltage becomes smaller at the drain end. Hence the channel starts to operate at the drain end. Hence the less no. of electrons are attracted to the channel. So, channel resistance increases, I_{DS} increases at slow rate.

4) $V_{DS} = V_{GS} - V_T$. channel becomes pinched off at the drain end.

5) If $V_{DS} > V_{GS} - V_T$ channel pinch off occurs at ΔL dist away from drain end. strong electron field is created at ΔL so velocity saturation occurs. So, $I_{DS} \rightarrow \text{const}$



Drain characteristics:



→ Plot b/w V_{DS} , I_{DS}

→ $V_{GS} = V_T$ (const)

→ Divided into 2 regions

Triode / linear region : Current increases linearly with V_{DS} .

MOSFET acts as a resistor.

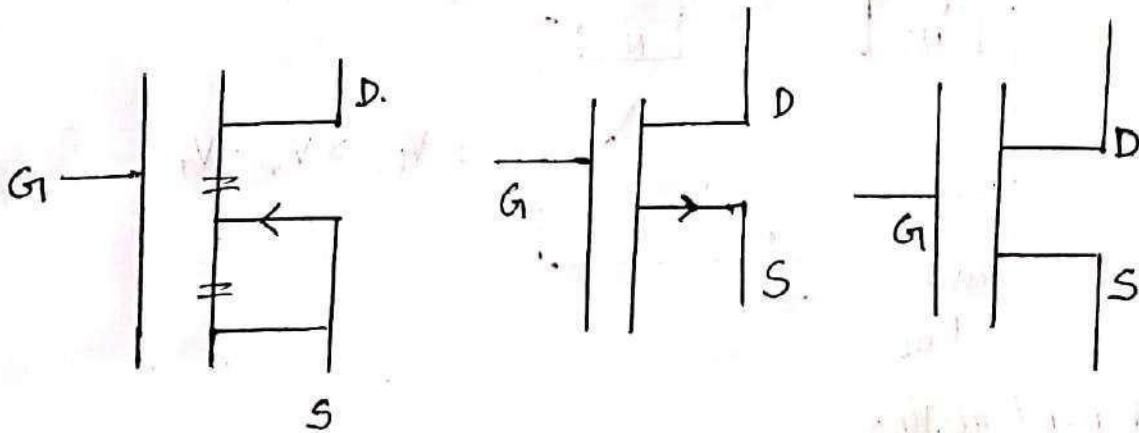
Saturation / Pinch off region : Current is const. MOSFET acts as amplifier.

for N-channel MOSFET to be in saturation

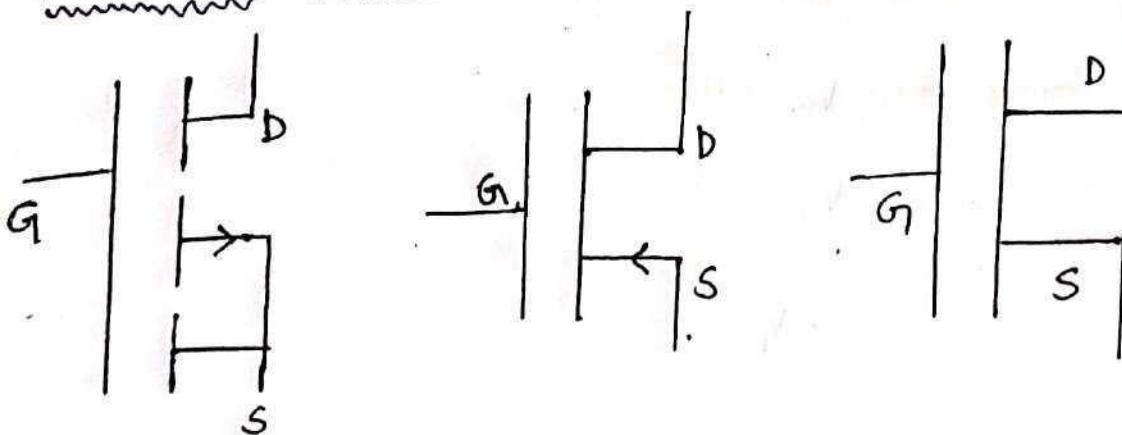
$$V_{DS} \geq V_{GS} - V_T$$

$$\text{for P-channel MOSFET } V_{SD} \geq V_{SG} - |V_T|$$

N-channel MOSFET:



P-channel MOSFET:



N-Channel depletion MOSFET

Construction:

The structure of D-MOSFET is similar to E-MOSFET but depletion MOSFET has a physically fabricated channel.

N-channel is created by using impurity implantation method.

Depletion MOSFET can conduct for all values of V_{GS}

i) If $V_{GS} = 0$

single channel is physically present a non-zero drain current flows

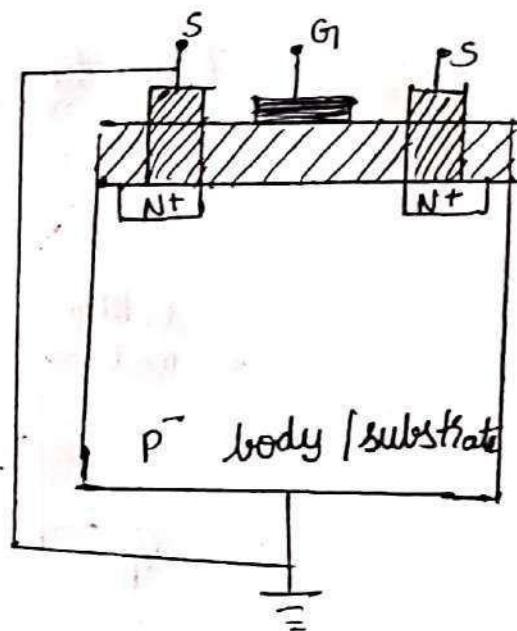
If $V_{GS} = -V_L$, gate layer becomes -ve by charge and polarisation of SiO_2 occurs

→ -ve charge of SiO_2 will repel the electron from the channel.

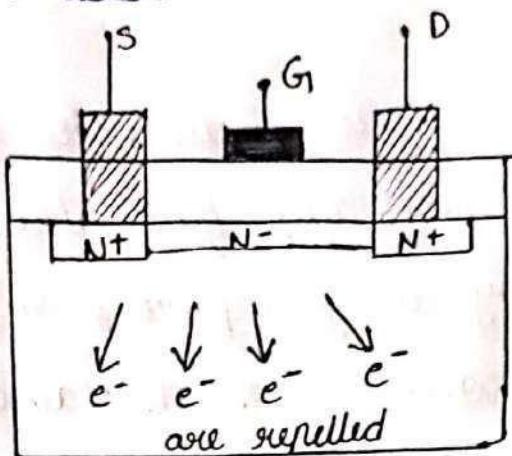
Hence channel conductivity decreases channel depletion occurs due to drain current decreases.

→ V_{GS} is sufficiently negative channel depletion occurs completely. Hence drain current becomes i.e. the channel gets pinched off. This voltage of V_{GS} is "pinched off voltage".

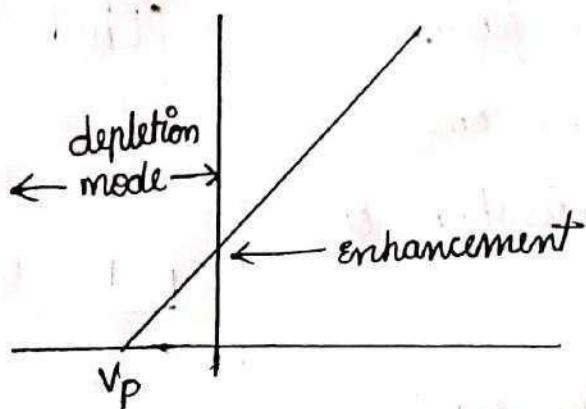
→ If V_{GS} is +ve the +ve charge of SiO_2 will attract the minority electron of P-type substrate and majority electron from source and drain. Hence the electron density in the



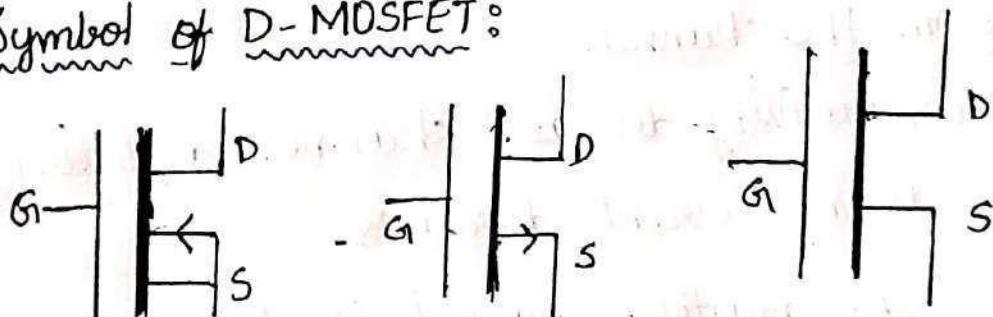
channel increases. channel conductive increases, and drain current increases.



Transfer characteristics:



Symbol of D-MOSFET:



Drain characteristics:

The depletion MOSFET drain characteristics is similar to that of enhancement MOSFET