Parity bit generator

odd parity bit generator

a	b	c	Parity bit (odd)
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

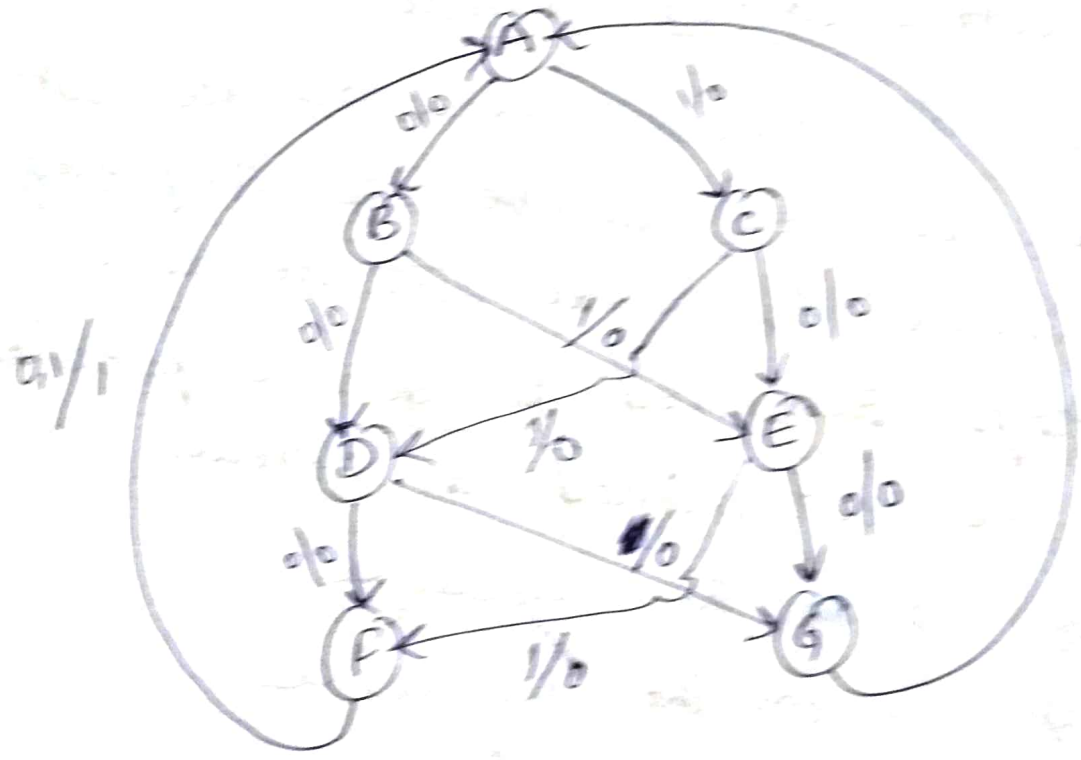
Serial parity bit generator is a two terminal circuit which receives coded messages and adds a parity bit to every m bits of the message, so the resulting outcome is an error detecting coded message

The inputs are assumed to arrive in groups of three symbols ($m = 3$) and strings are separated by a single time unit (fourth place is blank). The parity bits are inserted in appropriate spaces so that the resulting outcome is a (extended) string of symbols with out spaces. For even parity, a parity bit 1 is inserted, if and only if the number of 1s in the preceding string of three symbols is odd.

For odd parity, a parity bit 1 is inserted, if and only if no of 1s in the preceding string of three symbols is even.

State assignment

A = 000
B = 001
C = 010
D = 011
E = 100
F = 101
G = 110



States B, D, F correspond to even no of 1's out of (three) incoming inputs respectively. Similarly states E, F, G correspond to odd no of 1's out of 1, 2, 3 incoming inputs respectively.

From states either F (or) G, machine goes to state A regardless of the input.

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	x = 0	x = 1
A	B, 0	C, 0
B	D, 0	E, 0
C	E, 0	D, 0
D	F, 0	G, 0
E	G, 0	F, 0
F	A, 1	A, 1
G	A, 0	A, 0