Unit-2: 8051 Microcontrollers

Introduction to Microcontrollers	Overview, Architecture, I/O Ports, Memory Organization, Addressing Modes and Instruction set.
8051 Real-time control	Programming Timer Interrupts, external hardware interrupts, serial communication interrupts, and timers and counters.

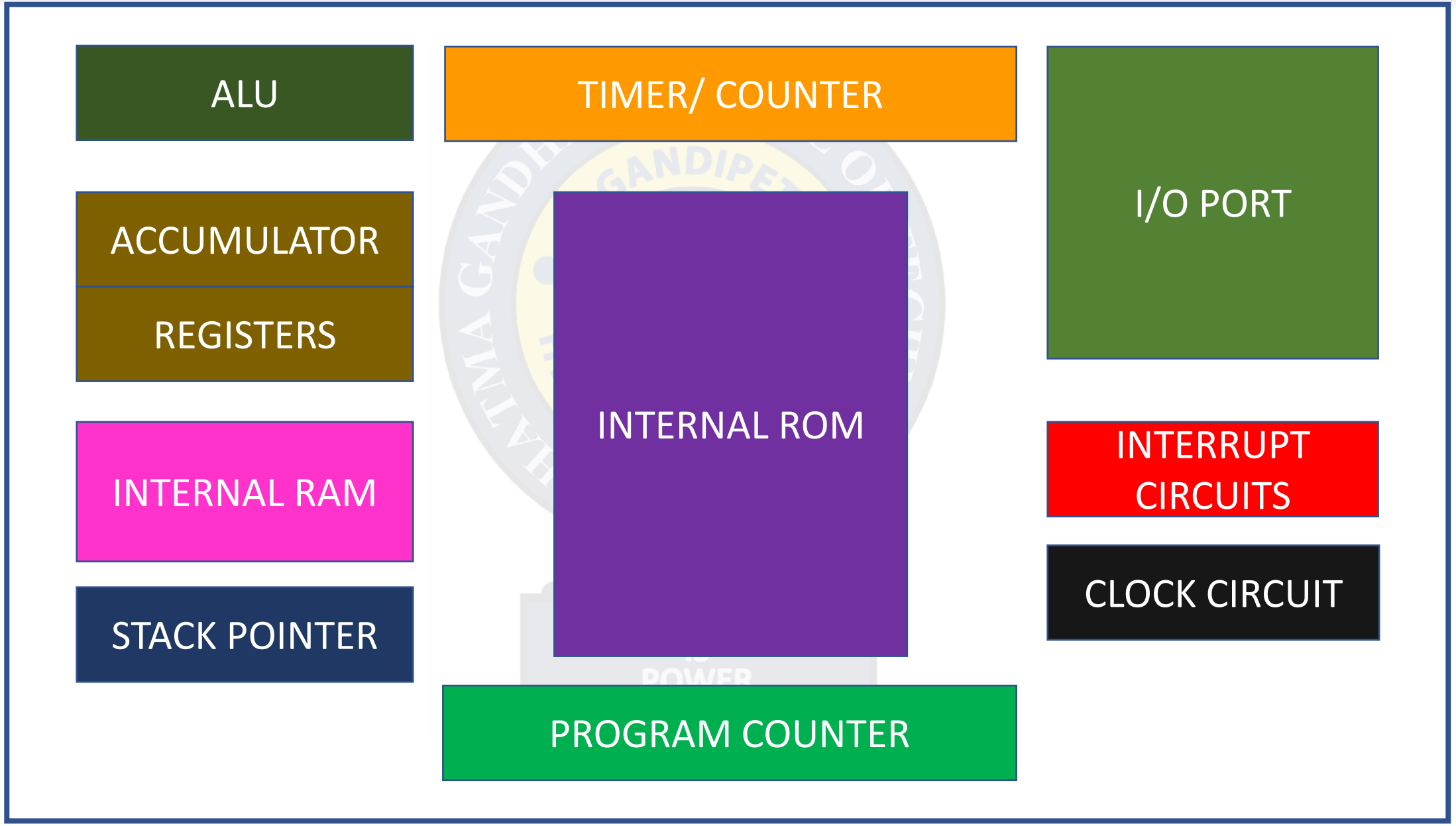
Introduction

- A register-based programmable electronic device that performs various operations on data.
- True system-on-chip unlike microprocessor.
- Consisting of on-chip ROM, RAM, I/O Ports, and Timer & Counters.
- Primarily used to control the operation of a machine using a fixed program stored in ROM and that does not usually changed/ upgraded.
- Most of the instructions are coupled with pins on IC package also, the pins are programmable.
- Instructions can also handle data bit-by-bit.
- 8051 is an Intel's 8-bit microcontroller.
- Highly successful in industry and academia.

Introduction

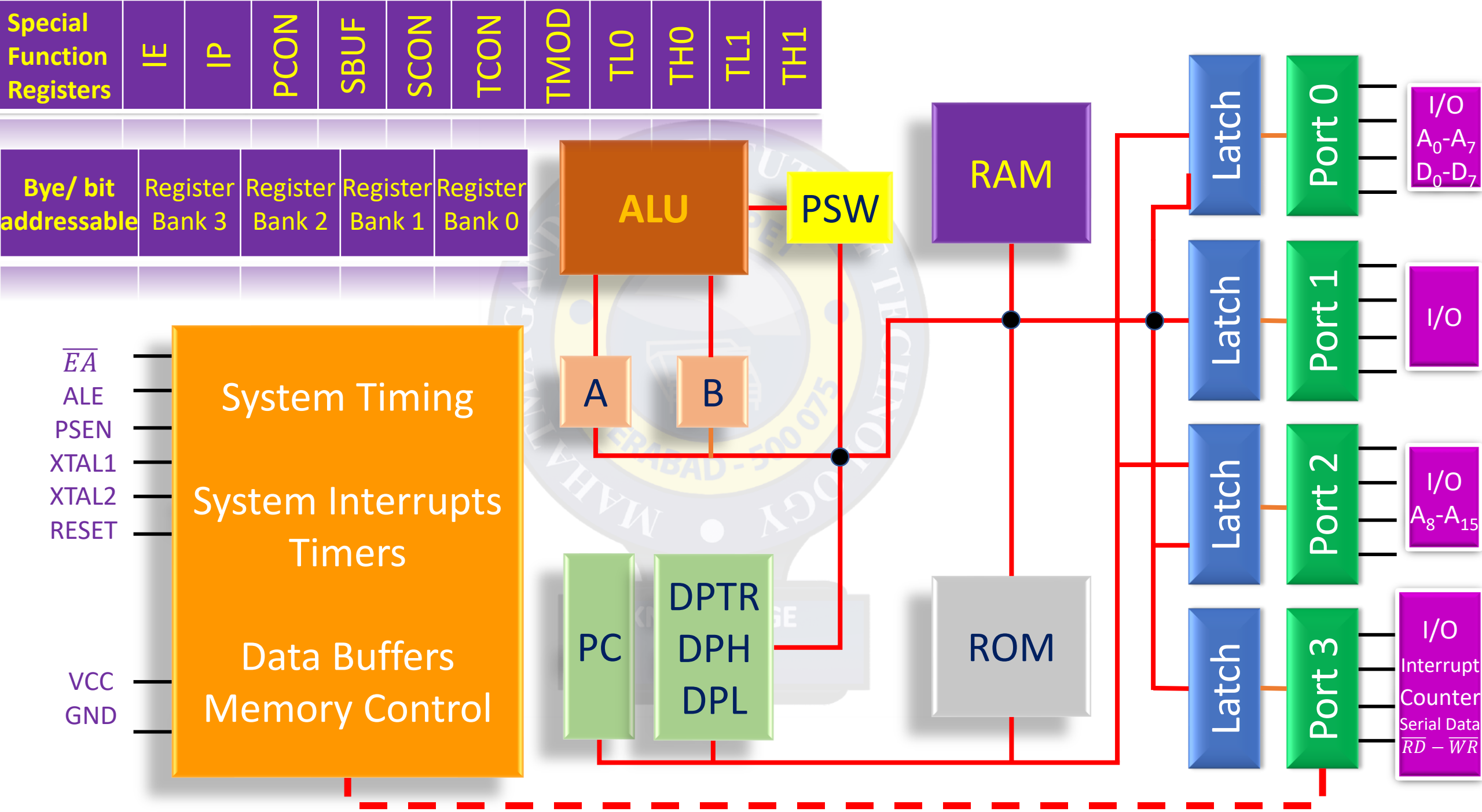
- 4-bit Microcontrollers: 4004 was the beginner.
- Hitachi, Toshiba, National and Texas instruments were the first manufacturers of 4-bit controllers.
- 8-bit Microcontrollers: Intel 8048 was first of Intel series.
- 8048 has 64 Bytes of RAM 1K Bytes of ROM with an external memory support up to 8 KB.
- 8051 Microcontroller: 8-bit microcontroller.
- Most popular with 128 Bytes of RAM and 2 KB of ROM (flash).
- External memory support up to 128 KB.
- CISC architecture.
- 8096 was a 16-bit microcontroller from Intel.

Introduction



Introduction

Device	Flash Memory	Data Memory
AT89C1051	1 KB	64 Bytes
AT89C2051	2 KB	128 Bytes
AT89C4051	4 KB	128 Bytes
AT89C51/S51	4 KB	128 Bytes
AT89C52/S52	8 KB	256 Bytes
AT89C55	20 KB	256 Bytes
AT89S8252	8 KB	256 Bytes
AT89S53	12 KB	256 Bytes


Special Function Registers
IE
IP
PCON
SBUF
SCON
TCON
TMOD
TL0
TH0
TL1
TH1
Bye/ bit addressable
Register Bank 3
Register Bank 2
Register Bank 1
Register Bank 0
ALU
PSW
RAM
A
B
PC
DPTR
DPH
DPL
ROM
System Timing
System Interrupts
Timers
Data Buffers
Memory Control
EA
ALE
PSEN
XTAL1
XTAL2
RESET
VCC
GND
Latch
Port 0
I/O
A0-A7
D0-D7
Latch
Port 1
I/O
Latch
Port 2
I/O
A8-A15
Latch
Port 3
I/O
Interrupt
Counter
Serial Data
RD – WR

Register Organization

Program Counter (PC) & Data Pointer (DPTR)

- Two 16-bit registers used to hold the address.
- Program instructions are fetched by the PC from the memory.
- PC incremented by 1 after the execution of each instruction.
- PC is the only register without internal address.
- DPTR: has two 8-bit registers DPH & DPL.
- Used to store memory addresses related to data.
- DPH & DPL have internal addresses individually but DPTR has no address.

Register Organization

A and B CPU Registers

- A & B two of 34 general purpose registers of 8051.
- A is an accumulator and used widely in arithmetic/logical operations.
- A is used in data transfer between 8051 and external memory.
- B is used in multiplication and division operations.
- B also stores the result and has other applications.

Program Status Word (PSW)

- An 8-bit register (can be accesses bit-by-bit) used to store the status of operations of 8051.
- Each flag has individual addresses.

Register Organization

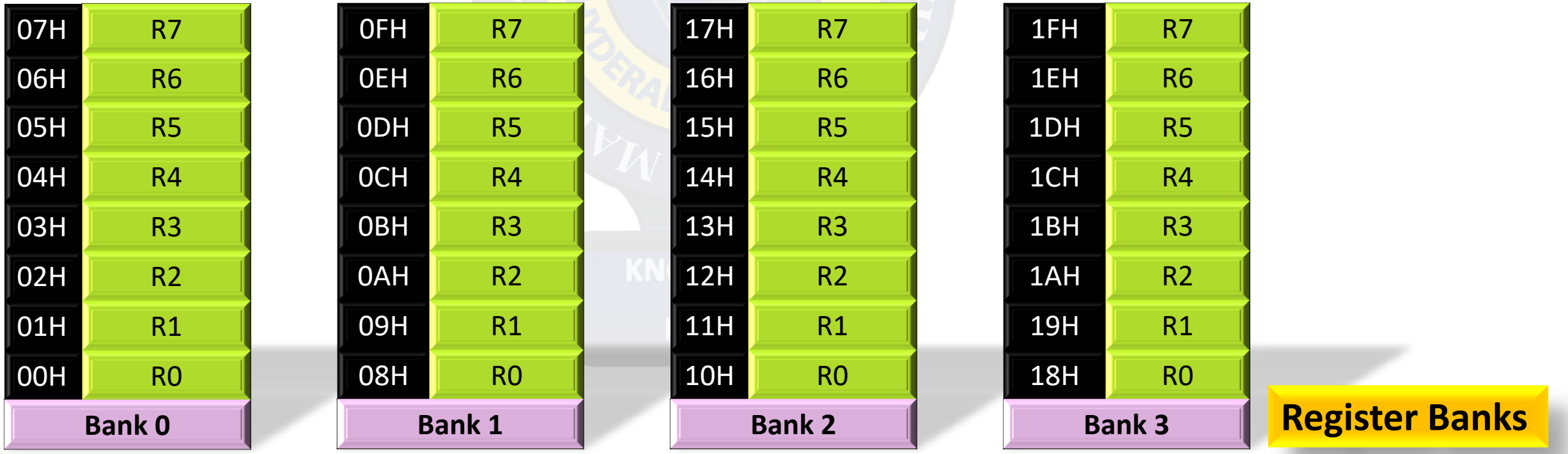
- CY: Carry flag.
- AC: Auxiliary Carry flag.
- User flag 0.
- RS1: Register bank select bit 1.
- RS0: Register bank select bit 0.
- OV: Overflow flag.
- P: Parity flag.
- Bit addressable as PSW.0 to PSW.7.

Internal Memory

- 8051 uses Harvard architecture which uses same memory for code and data.
- Internal RAM: 128 bytes
  - **32 bytes of registers** from 00H – 1FH. (organized as 4 register banks)
  - **Bit-addressable area** of 16 bytes from 20H – 2FH
  - **A general purpose RAM** (30H – 7FH) addressable as bytes
- Register banks are numbered from 0 – 3 each consists of 8 registers R0 – R7.
- Each register can be addressed by name or by its RAM address.
- R3 of register bank 3 is R3 when the register bank is selected otherwise, it addressed by 1BH.
- Unused register banks can be used as general purpose RAM.
- When RESET, the register bank 0 is selected.

Internal Memory

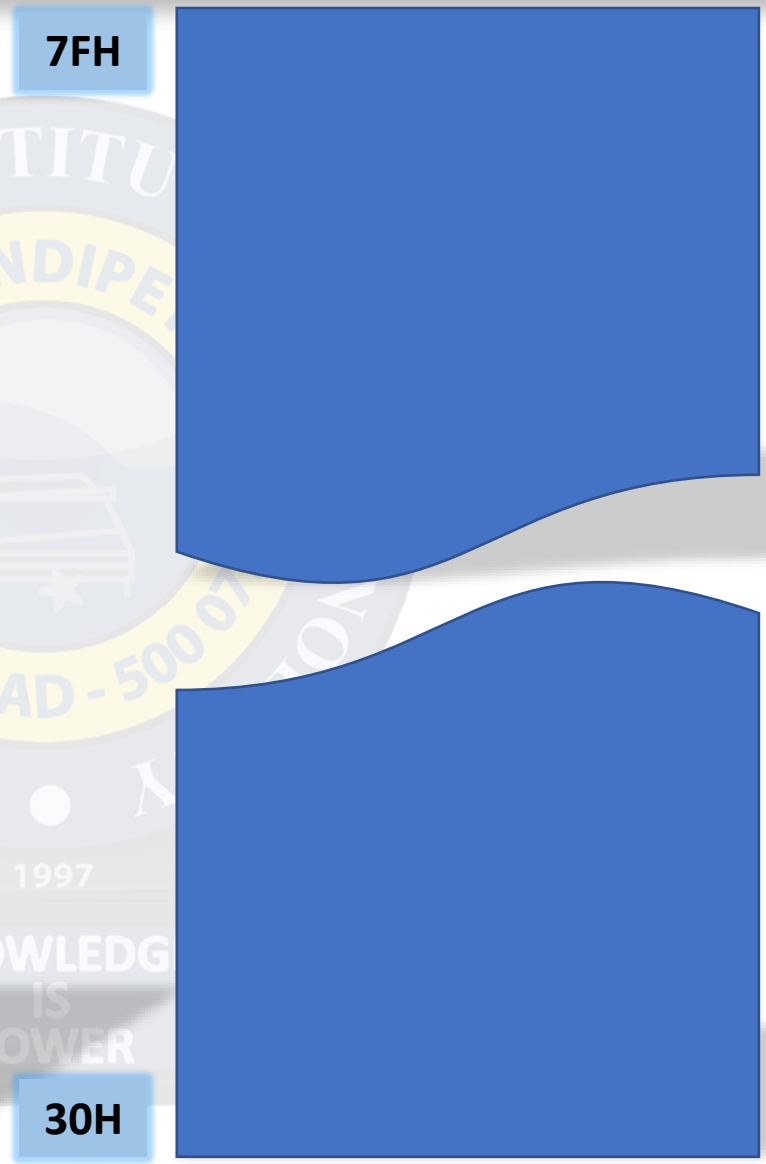
- 20H – 2FH are bit-addressable. Hence, 128 addressable bits in total.
- Each bit may be specified by its bit address 00H – 7FH.
- Entire 8-bits form any byte address from 20H – 2FH.
- Addressable bits are used when program needs to remember binary events.



8051 Architecture

2FH	7F	78
2EH	77	70
2DH	6F	68
2CH	67	60
2BH	5F	58
2AH	57	50
29H	4F	48
28H	47	40
27H	3F	38
26H	37	30
25H	2F	28
24H	27	20
23H	1F	18
22H	17	10
21H	0F	08
20H	07	00

Bit addressable



Internal RAM

Stack and SP

- Stack is a part of internal RAM.
- An 8-bit stack pointer (SP) register holds the top of the stack address.
- SP incremented by 1 before every PUSH operation and decremented by 1 after every POP operation.
- SP is set to 07H when 8051 is RESET.
- Can be changed to any internal RAM address.
- Care is needed to avoid any accidental data loss due to PUSH and POP operations.

Special Function Registers (SFRs)

- All are 8-bit registers (except PC & DPTR) with internal addresses.
- Addressed from 80H to FFH. This addressing is dynamic in nature.
- IP, IE, TCON, A, B, SCON, and PSW are bit addressable.
- All the latches (0-3) are bit addressable.

8051 Architecture

NAME	FUNCTION	RAM ADDRESS
A	Accumulator	E0H
B	Arithmetic	F0H
DPH	Addressing External Memory	83H
DPL	Addressing External Memory	82H
IE	Interrupt Enable	A8H
IP	Interrupt Priority	B8H
P0	I/O Port latch	80H
P1	I/O Port latch	90H
P2	I/O Port latch	A0H
P3	I/O Port latch	B0H
PCON	Power Control	87H
PSW	Program Status Word	D0H
SCON	Serial Port Control	98H
SBUF	Serial Port Data Buffer	99H
SP	Stack Pointer	81H

NAME	FUNCTION	RAM ADDRESS
TMOD	Timer/Counter Mode Control	89H
TCON	Timer/Counter Control	88H
TL0	Timer 0 Low Byte	8AH
TH0	Timer 0 High Byte	8CH
TL1	Timer 1 Low Byte	8BH
TH1	Timer 1 High Byte	8DH

Special Function Registers

Internal ROM

- Memory for data and code has different physical entities.
- Each has the same address ranges from 0000H – 0FFFH.
- PC is used to address the program code.
- Program addresses higher than 0FFFH will e automatically fetched from the external memory.
- $\overline{EA}$ is used to fetch the code bytes from an external memory.
- Program can be stored either completely in internal ROM, completely in external ROM, or combination of internal and external ROM.

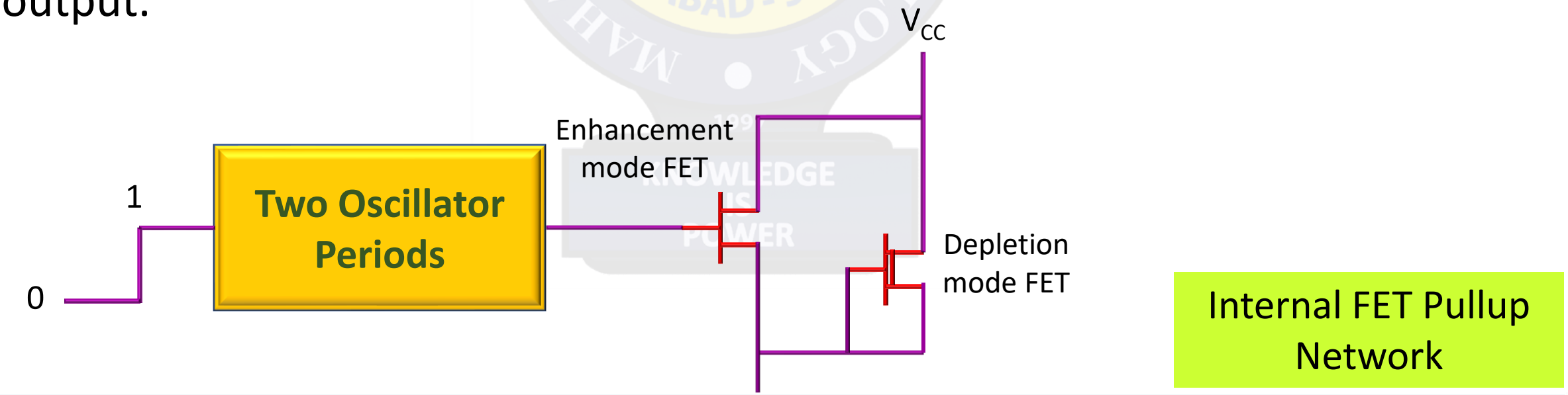
I/O Ports

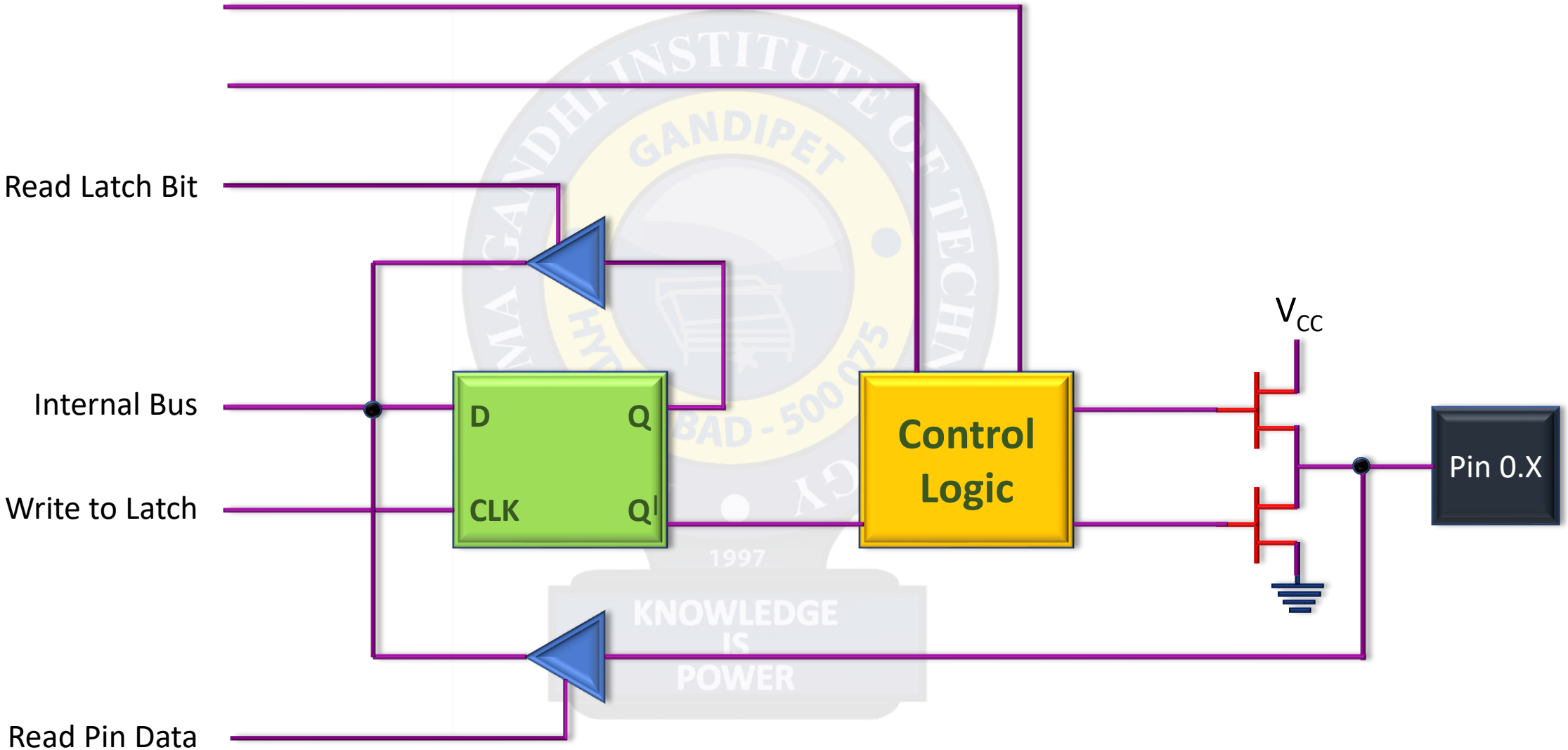
- 8051 has 4 ports P0 – P3.
- Each has the same address ranges from 0000H – 0FFFH.
- **Port-0** pins (P0.0 – P0.7) are from 39 – 32. These are multiplexed with $AD_0 – AD_7$.
- **Port-1** pins (P1.0 – P1.7) are from 1 – 8.
- **Port-2** pins (P2.0 – P2.7) are from 21 – 28. Multiplexed with $A_8 – A_{15}$.
- **Port-3** pins (P3.0 – P3.7) are from 10 – 17. Multiplexed with other various functions of 8051.

Pin diagram of 8051 Microcontroller

I/O Ports

- **Port-0** pins used as input/output and bi-directional lower order address and data bus for external memory.
- A '1' must be written to the Port0 latch by the program for using the pin as input.
- A '0' must be written to the Port0 latch by the program for using the pin as output.

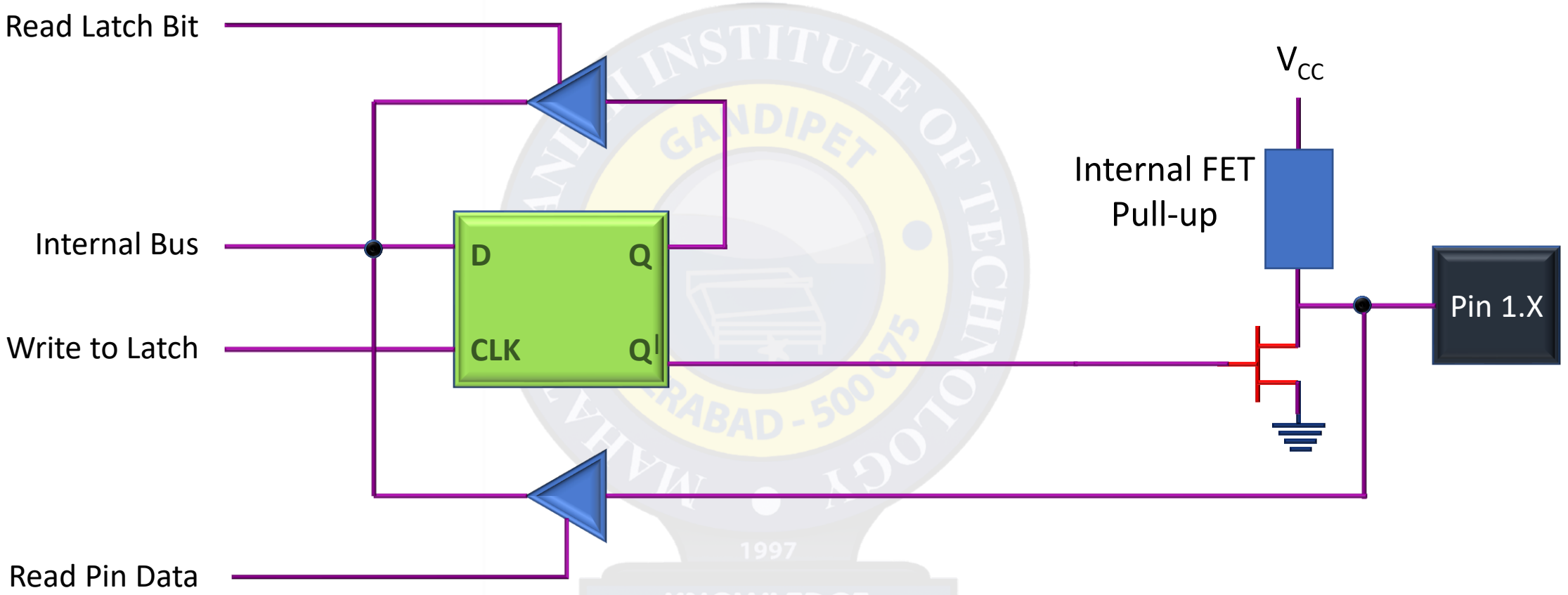




Port 0 Pin Configuration

I/O Ports (Port-0)

- When Port-0 used as an address bus to external memory, internal control signals switch the address lines to the gates of the FETs.
- A logic ‘1’ on an address bit turn the upper FET ON and lower FET OFF.
- A logic ‘0’ on an address bit turn the upper FET OFF and lower FET ON.
- ALE pin controls this address bus.
- **Port-1** pins have no dual functions..
- A ‘1’ must be written to the Port-1 latch for using the pin as input.
- If used as an output, the latches containing a 1 can drive the input of an external circuit high through the pullup.
- If a ‘0’ is written to the latch, the lower FET is ON, pullup is OFF.



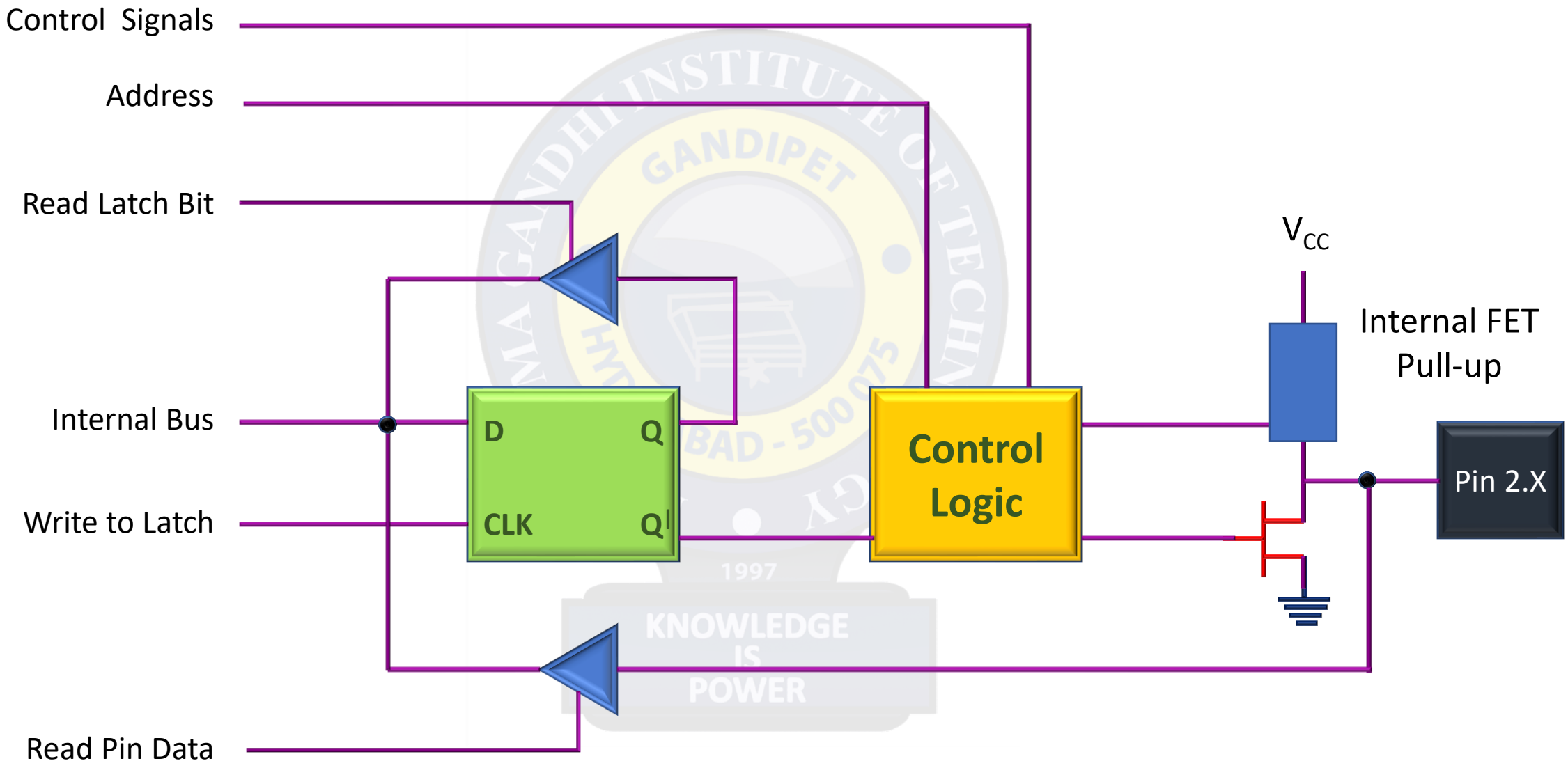
Port 1 Pin Configuration

I/O Ports (Port-1)

- Another FET in parallel to the pullup speedup the switching times.
- Provides a low impedance path to the positive voltage supply that helps in reducing rise times.

Port-2 can be used as I/O port similar to Port-1.

- Alternative function is to supply higher order address byte in conjunction with the Port-0 lower byte.
- Can be momentarily changed by the address control signals when supplying the higher byte of a 16-bit address.
- When external memory is addressed, the latches remain same.
- It does not carry any data as in the case of Port-0.

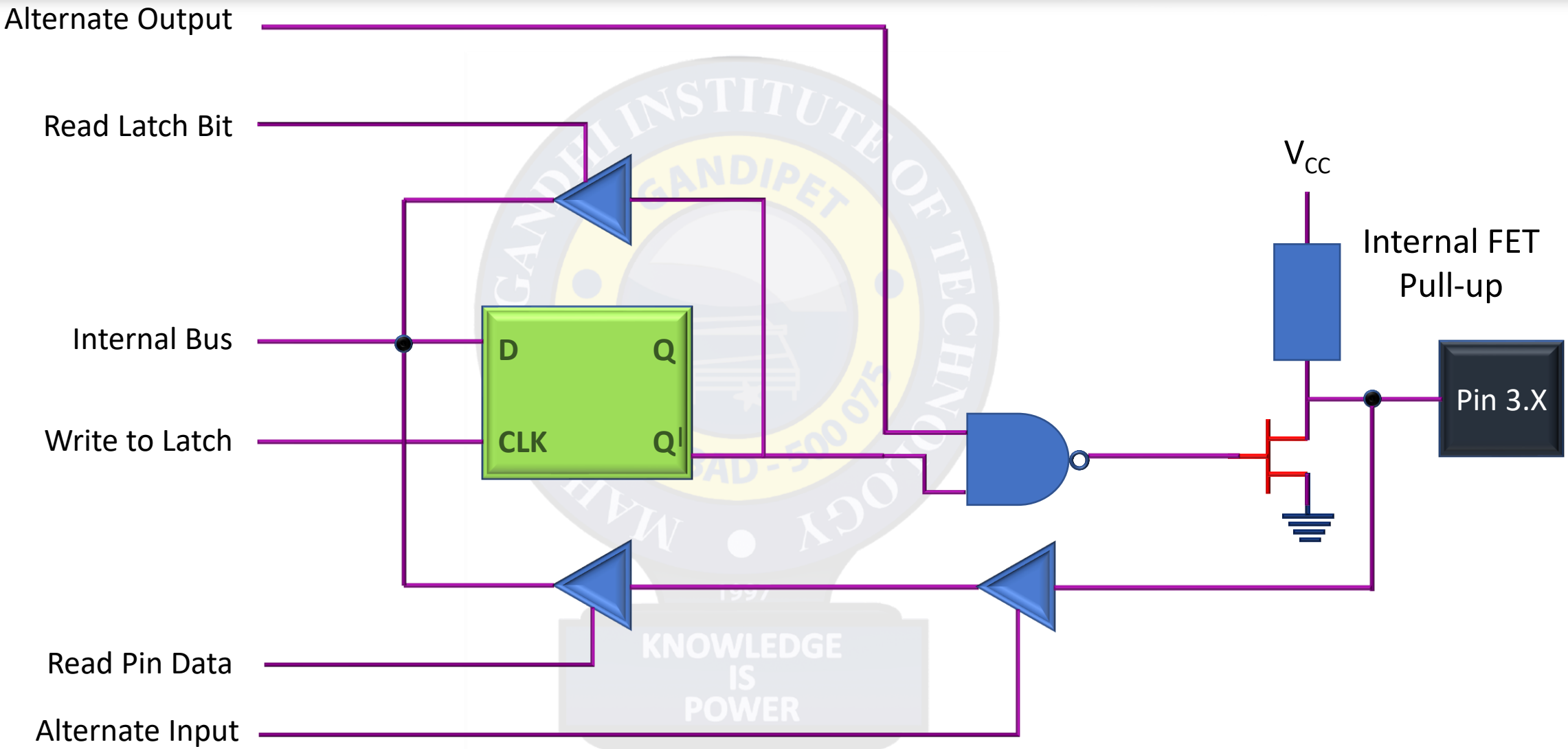


Port 2 Pin Configuration

I/O Ports (Port-3)

- Port-3 has an I/O port similar to Port-1.
- The I/O functions can be programmed under the control of P3 latches and the SFRs.

PIN	ALTERNATE USE	SFR
P3.0 – RXD	Serial Data Input	SBUF
P3.1 – TXD	Serial Data Output	SBUF
P3.2 – $\overline{INT0}$	External Interrupt 0	TCON.1
P3.3 - $\overline{INT1}$	External Interrupt 1	TCON.3
P3.4 – T_0	External Timer 0 Input	TMOD
P3.5 – T_1	External Timer 1 Input	TMOD
P3.6 – $\overline{WR}$	External Memory Write Pulse	---
P3.7 – $\overline{RD}$	External Memory Read Pulse	---



Port 3 Pin Configuration

Oscillator and Clock

- Pins XTAL1 and XTAL2 are used for connecting a resonant circuit.
- Usually quartz crystal is used to generate oscillations.
- Crystal frequency is the basic internal clock frequency.
- The frequency vary between 1 – 16 MHz depending on the version of 8051.
- Minimum frequency is required to maintain dynamic memories internally to avoid data loss.
- Clock frequency is divided to establish standard communication data rates (bit rates).
- The smallest interval of time within the microcontroller is called a pulse.

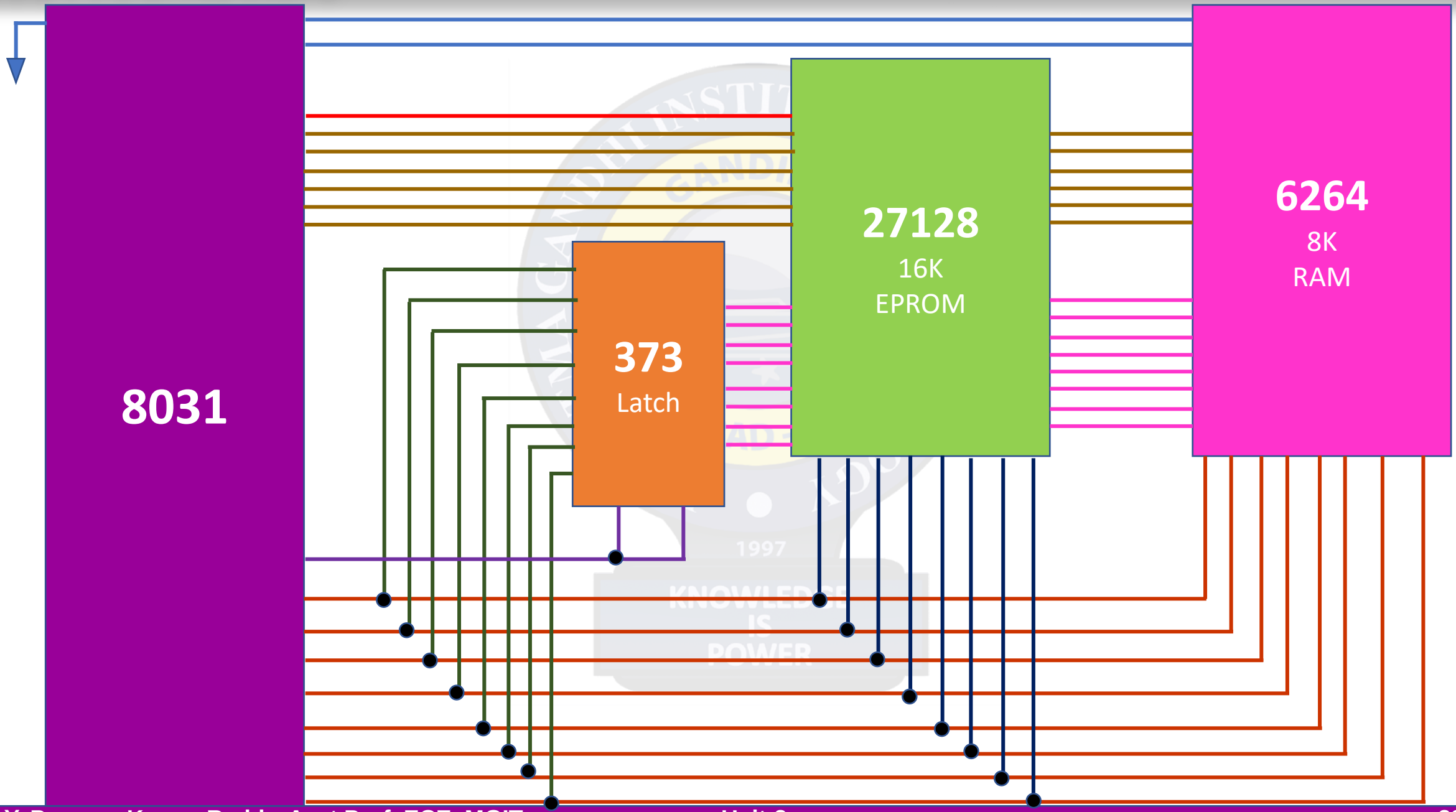
- The smallest interval of time to accomplish any simple instruction or part of a complex instruction is called the machine cycle.
- 8051 machine cycle is made up of six states.
- A state is discrete time interval for discrete operations of microcontroller such as fetching an opcode byte, decoding an opcode, executing an opcode, or writing a data byte.
- Two oscillator pulses define each state.
- Program instructions may require one, two, or four machine cycles to be executed.

$$T_{inst} = \frac{C \times 12d}{f_{crystal}}$$

External Memory:

- External memory can be program memory or data memory pointed by using PC or DPTR, respectively.
- Most of the times the internal ROM may not be sufficient to store the code when it is written in HLL.
- $\overline{EA}$ pin is to be grounded.
- External RAM of 64K bytes can also be added in addition to the internal RAM of 128 bytes.
- DPTR register is used to access the external RAM.

8051 Architecture



TCON:

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Bit	Symbol	Function
7	TF1	**Timer 1 Overflow flag:** Sets when timer rolls from all ones to all zeros. Cleared when processor vectors to execute ISR located at program address 001BH.
6	TR1	**Timer 1 Run Control:** Set 1 by program to enable timer to count; cleared to 0 by program to halt timer. It doesn't reset timer.
5	TF0	**Timer 0 Overflow flag:** Sets when timer rolls from all ones to all zeros. Cleared when processor vectors to execute ISR located at program address 000BH.
4	TR0	**Timer 0 Run Control:** Set 1 by program to enable timer to count; cleared to 0 by program to halt timer. It doesn't reset timer.
3	IE1	**External Interrupt 1 Edge Flag:** Set to 1 when a high to low edge signal is received on port 3 pin 3.3. cleared when processor vectors to ISR located at program address 0013H. Not related to timer operations.
2	IT1	**External Interrupt 1 Signal Type Control:** Set to 1 by program to enable external interrupt 1 to be triggered by a falling edge signal. Set to 0 by program to enable a low level signal on external interrupt 1.
1	IE0	**External Interrupt 0 Edge Flag:** Set to 1 when a high to low edge signal is received on port 3 pin 3.2. cleared when processor vectors to ISR located at program address 0003H. Not related to timer operations.
0	IT0	**External Interrupt 0 Signal Type Control:** Set to 1 by program to enable external interrupt 1 to be triggered by a falling edge signal. Set to 0 by program to enable a low level signal on external interrupt 0.

TMOD:

7	6	5	4	3	2	1	0
Gate	C/T’	M1	M0	Gate	C/T’	M1	M0

Bit	Symbol	Function
7/3	Gate	**OR gate enabled bit:** Controls RUN/STOP of timer 1/0. Set by program to enable timer to run if bit TR1/0 in TCON is set and signal on external interrupt INT’ 1/0 pin is high. Cleared to enable timer to run if bit TR1/0 in TCON is set.
6/2	C/T’	Set 1 by program to make Timer 1/0 act as a counter by counting pulses from external input pins 3.5 (T1) or 3.4 (T0). Cleared to make timer act as a timer by counting internal frequency.
5/1	M1	**Timer/ Counter operating mode select bit 1:** Set/cleared by program to select mode.
4/0	M0	**Timer/ Counter operating mode select bit 0:** Set/cleared by program to select mode.

M1	M0	MODE
0	0	0
0	1	1
1	0	2
1	1	3

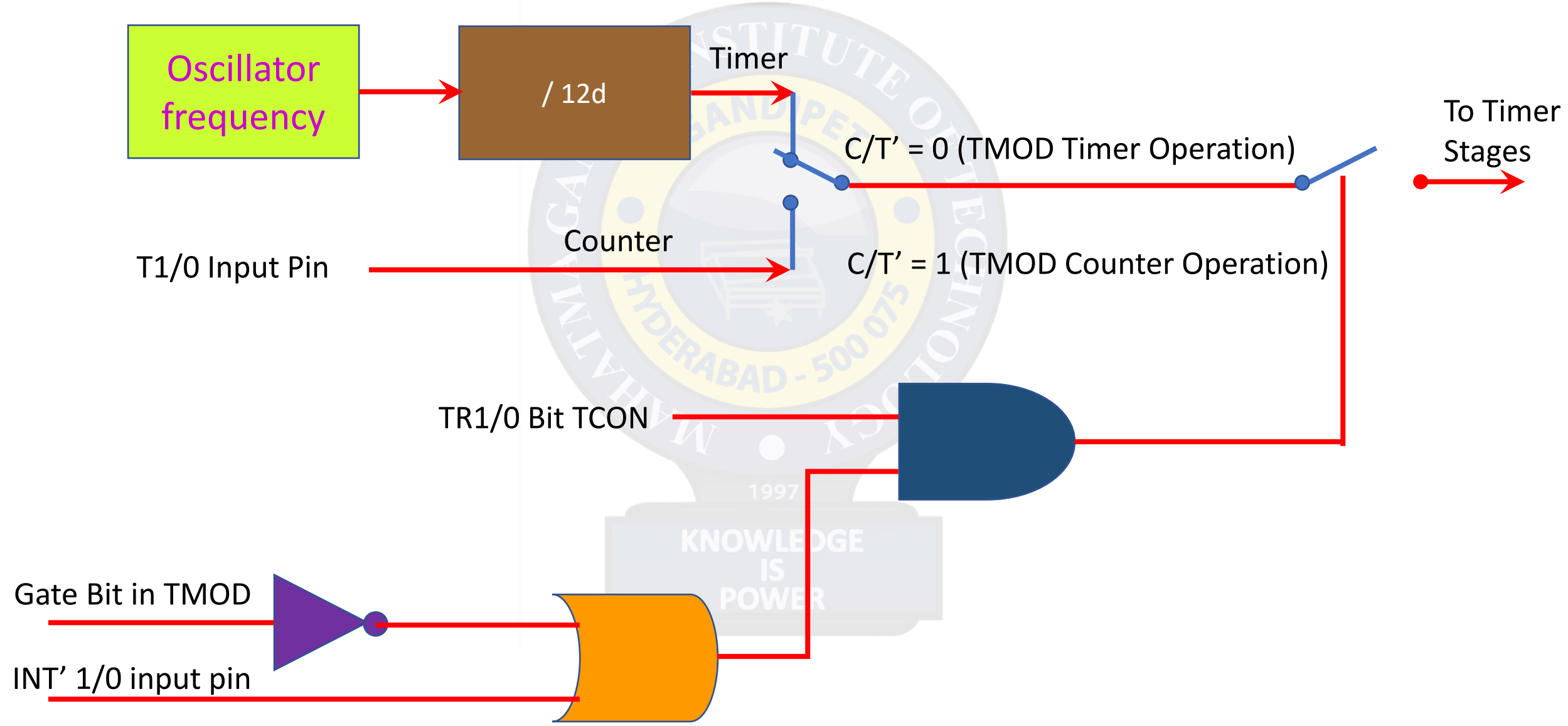
Counters and Timers:

- Used to count the external events such as frequency of pulse train, generation of delay, and precise internal time.
- Two 16-bit up counters T0 (TH0 & TL0) and T1 (TH1 & TL1) are provided in 8051.
- Counter action is controlled by bit states in the TMOD, TCON registers, and certain program instructions.
- TMOD is dedicated to two timers. Each timer controlled by 4-bits of TMOD.
- TCON has control bits and flags for the timers in the upper nibble and control bits and flags for the external interrupts in the lower nibble.

Timer Counter Interrupts:

- A number (max count or delay) is placed in one of the counters. Counter increments from initial value to the specified max value then goes back to zero. And sets the timer flag.
- Flag condition can be tested through program or can be used to interrupt the program.
- If a counter is programmed to be a timer, it will count the internal clock frequency of the 8051 oscillator divided by 12d. controlled by bit states in the TMOD, TCON registers, and certain program instructions.

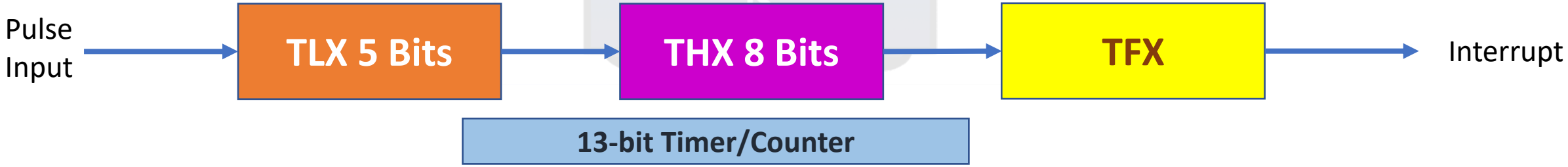
8051 Architecture



Timer Modes

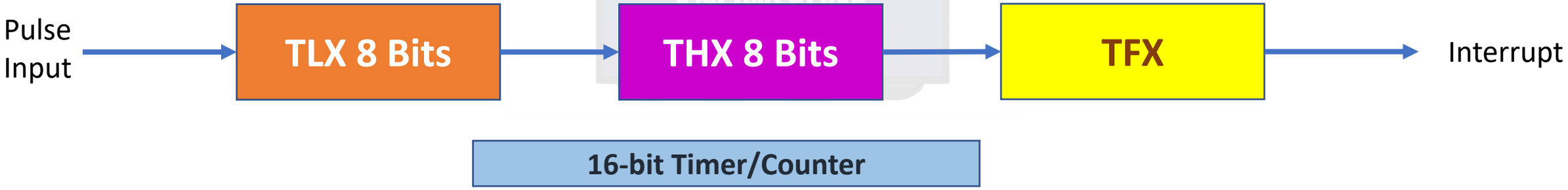
Mode 0:

- Selected by setting mode bits in TMOD to 00b.
- THX register can be used as 8-bit counter and TLX as a 5-bit counter.
- The pulse input is divided by 32d in TL so that TH counts the original oscillator frequency reduced by a total 384d.
- Ex: f = 6MHz would result in a final frequency to TH of 15265Hz.
- The timer flag sets whenever THX goes from FFh to 00h. Or it takes 0.0164 seconds for a 6MHz crystal if THX starts at 00h.



Mode 1:

- Selected by setting mode bits in TMOD to 01b.
- Similar to Mode 0 except for TLX is set to full 8-bit counter.
- The pulse input is divided by 128d in TL so that TH counts the original oscillator frequency reduced by a total 1,536d.
- Ex: f = 6MHz would result in a final frequency to TH of 3906Hz.
- The timer flag sets whenever THX goes from FFh to 00h. Or it takes 0.1311 seconds for a 6MHz crystal if THX starts at 00h.

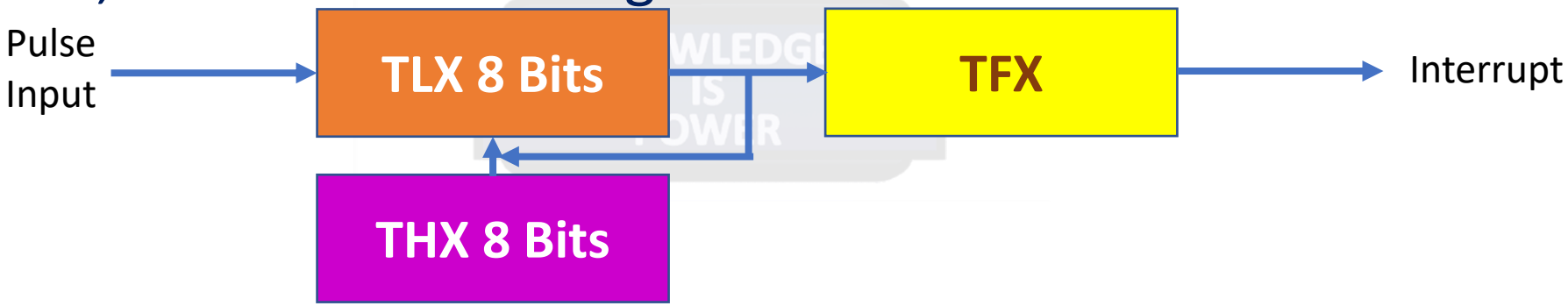


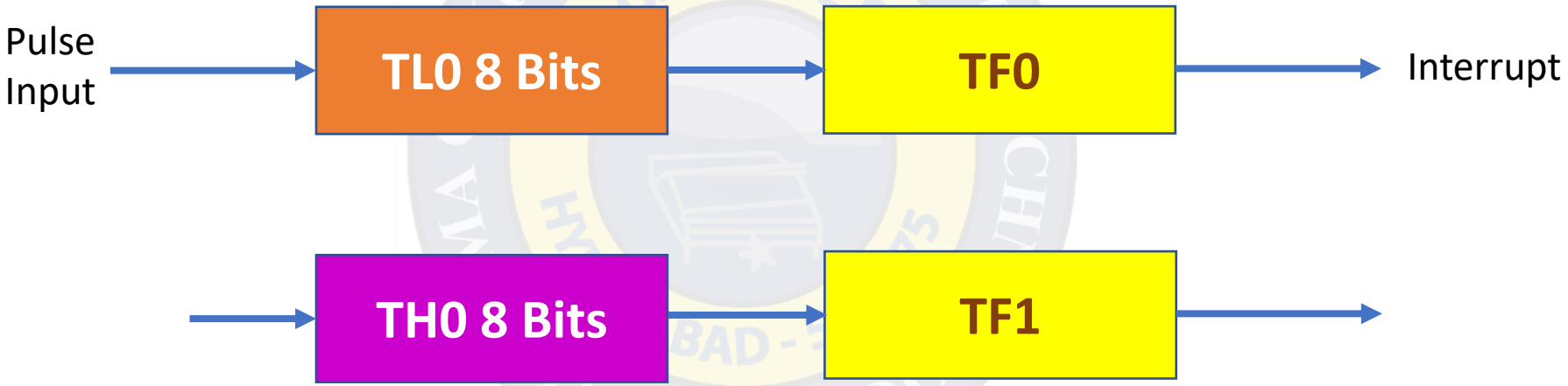
Mode 2:

- Selected by setting mode bits in TMOD to 10b.
- Uses only TLX as 8-bit counter.
- THX is used to hold a value that is loaded into TLX every time TLX overflows from FFH to 00H.
- Timer flag sets when TLX overflows.
- This exhibits an auto reload feature: TLX will count up from the number in THX, overflow, and be initialized again with the contents of THX.

Mode 3:

- Selected by setting mode bits in TMOD to 11b.
- Timers do not operate independently.
- Placing Timer 1 in Mode 3 makes to stop counting.
- The control bit TR1 and the Timer 1 flag TF1 are then used by Timer 0.
- Timer 0 will become two separate 8-bit counters.
- This exhibits an auto reload feature: TLX will count up from the number in THX, overflow, and be initialized again with the contents of THX.




Pulse
Input
TL0 8 Bits
TF0
Interrupt
TH0 8 Bits
TF1

Serial Data Input/Output

- 8051 has SBUF to hold data for serial communication.
- SCON register controls the data transmission. Bit addressable from SCON.0 to SCON.7.
- PCON controls the data rates.
- RXD (P3.0) and TXD (P3.1) controls the direction of data flow and connect to the serial data network.
- SBUF has the address 99H used hold data during READ/WRITE operations of 8051.
- Four programmable modes are available by setting SMX bits in SCON.
- These modes are differentiated by their baud rates.

SCON

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Bit	Symbol	Function
7	SM0	0 0 **Mode 0:** Shift register; baud = f/12 0 1 **Mode 1:** 8-bit UART; baud = variable 1 0 **Mode 2:** 9-bit UART; baud = f/32 or f/64 1 1 **Mode 3:** 9-bit UART; baud = variable
6	SM1	
5	SM2	**Multiprocessor Communication:** controlled by program to enable multiprocessor communication in Modes 2 & 3. When set to 1: an interrupt is generated if bit 9 of the received data is a 1; no interrupt is generated if bit 9 is a zero. If set to 1 for Mode 1, no interrupt will be generated unless a valid stop bit is received. Clear to 0 if Mode bit is in use.
4	REN	**Receive Enable Bit:** Set 1 to enable reception; cleared to disable data reception.
3	TB8	**Transmitted bit 8:** Set/cleared by program in Modes 2 & 3.
2	RB8	**Received bit 8:** Bit 8 of received data in Modes 2 & 3. Stop bit in Mode 1, not used in Mode 0.
1	TI	**Transmit Interrupt Flag:** Set to 1 at the end of bit 7 time in Mode 0, and at the beginning of the stop bit for other Modes. Must be cleared by the program.
0	RI	**Receive Interrupt Flag:** Set to 1 at the end of bit 7 time in Mode 0, and halfway through the stop bit for other Modes. Must be cleared by the program.

PCON (Not a bit addressable)

7	6	5	4	3	2	1	0
SMOD	-	-	-	GF1	GF0	PD	IDL

Bit	Symbol	Function
7	SMOD	**Serial Baud rate Modify:** Set to 1 by program to double baud rate using timer 1 for modes 1, 2, and 3. Cleared to 0 by program to use timer 1 baud rate.
6-4	---	Not Defined
3	GF1	**General Purpose User Flag bit 1:** Set/cleared by program.
2	GF0	**General Purpose User Flag bit 0:** Set/cleared by program.
1	PD	**Power down bit:** Set to 1 by program to enter power down configuration for CHMOS processors.
0	IDL	**Idle Mode bit:** Set to 1 by program to enter idle mode configuration for CHMOS processors.

Serial Data Interrupts:

- Used for effective serial data communication.
- Control bits are included in SCON register.
- TXD: has complete control through program. But RXD is unpredictable and at random times that are beyond the control of the program.
- TI and RI in SCON are Set whenever the data byte transmitted or received.
- TI & RI are ORed together to produce an interrupt.
- These flags are not cleared automatically but only through program.
- Programmer has the complete control over the serial data communication by setting and clearing the corresponding flags.

Data Transmission:

- Data stored in SBUF will be transmitted when TXD is activated and TI is set 1 at the end of the transmission of each byte to notify that the SBUF is empty.
- If the program fails to wait on TI flag, the SBUF is overwritten with the new byte and the result will be unpredictable.

Data Reception:

- Data reception begins if REN bit in SCON is set to 1 for all Modes.
- RI must be cleared for Mode 0.
- RI is set after data has been received in all modes.
- Before the last bit is received, the RI must be Set to avoid incoming data lost.
- Incoming data not transferred to SBUF until the last data bit has been received.

Serial Data Transmission Modes

- 8051 has four modes of data transmission.
- Modes are selected by SM1 and SM0 bits of SCON.
- Baud rates are fixed for Mode 0.
- Baud rates are variable, using timer 1 and serial baud rate modify bit (SMOD) in PCON registers for Modes 1, 2 , and 3.

Serial Data Mode 0 – Shift Register Mode:

- Setting bits SM0 and SM1 in SCON to 00b configures SBUF to receive or transmits 8 data bits using RXD for both functions.
- TXD is connected to the internal shift frequency pulse source to spply shift pulses to external circuits.
- The shift frequency or baud rate is fixed at f/12.

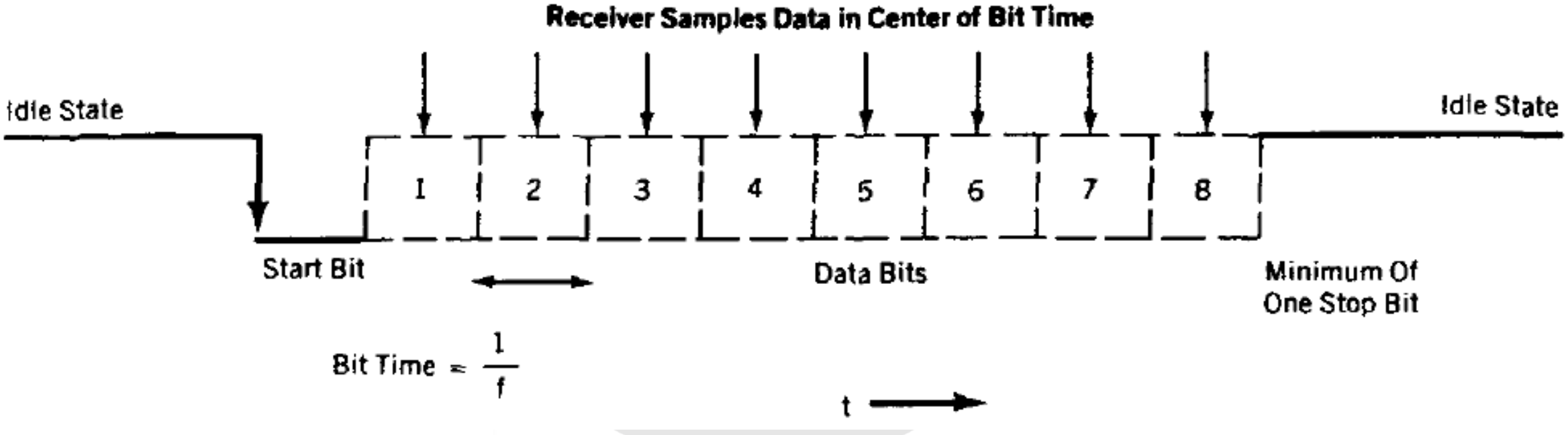
- The TXD shift clock is a square wave that is low for machine cycle states S3-S4-S5 and high for S6-S1-S2.
- When transmitting, the data is shifted out of RXD.
- Baud rates are fixed for Mode 0.
- Baud rates are variable, using timer 1 and serial baud rate modify bit (SMOD) in PCON registers for Modes 1, 2 , and 3.

Serial Data Mode 1 – Standard UART:

- Setting bits SM0 and SM1 in SCON to 01b configures SBUF 10-bit full-duplex receiver or transmitter.
- TXD transmits all data.
- Pin RXD receives all data.

- START BIT, 8-DATABITS, STOP BIT.
- Interrupt flag TI bit is set once all 10 bits have been sent.
- Each bit interval is the inverse of the baud rate frequency.
- Received data obtained in the same order.
- Reception triggered by the falling edge of the start bit and continues if the stop bit is true (0 level) halfway through the start bit interval.
- This is to avoid the errors due to noise.
- Data word will be loaded to SBUF only when
  - RI must be 0 AND mode bit SM2 is 0 OR the stop bit is 1.
- RI = 0 indicates successful reception of the previous byte.
- SM2= 1 forces the reception of only GOOD stop bits.
- SM2 = 0 enables the reception of a byte with any stop bit state.

- Of the received 10 bits, the start bit is discorded, 8 data bits go to SBUF, and stop bit is saved in RB8 of SCON.
- RI is set to 1 indicating new data byte has received.



Mode 1 baud rates:

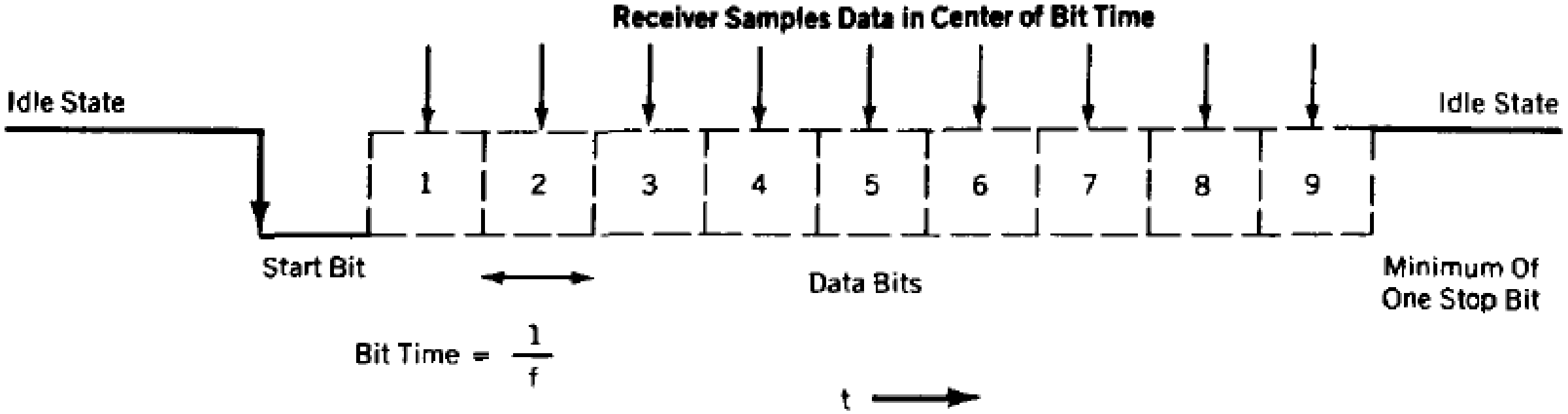
$$f_{baud} = \frac{2^{SMOD}}{32d} \times \frac{f_{osc}}{12d \times [256d - (TH1)]}$$

- SMOD is the control bit in PCON and can be 0 or 1.
- If the timer is not run in mode 2, the baud rate is

$$f_{baud} = \frac{2^{SMOD}}{32d} \times (timer1\ overflow\ frequency)$$

Serial Data Mode 2 – Multiprocessor Mode:

- Similar to Mode 1 except 1 bits are transmitted.
- START BIT, 9-DATA BITS, STOP BIT.
- The 9th bit is taken from TB8 in SCON during transmission and stored to RB8 in SCON during the reception.



Serial Data Mode 2 – Multiprocessor Mode:

- Baud rate is high which is the necessity in multiprocessor applications.
- RI must be 0 before the last bit is reeived, AND SM2 bit must be 0 or the 9th data bit must be a 1.
- Only those 8051's that have SM2 set to 0 will be interrupted by received data which has 9th data bit set to 0 and the rest will not be interrupted.
- All receivers will be interrupted by data words that have the 9th data bit set to 1; the state of SM2 will not block reception of such messages.

$$f_{baud} = \frac{2^{SMOD}}{64d} \times (oscillator\ frequency)$$

Serial Data Mode 2 – Multiprocessor Mode:

- This mode used to communicate 8051 with other selected 8051's without interrupting the rest.

Serial Data Mode 3 – Multiprocessor Mode:

- This mode is similar to Mode 2 except for the baud rate.
- Baud rate is determined exactly as in Mode 1 using Timer 1 to generate communication frequencies.

$$f_{baud} = \frac{2^{SMOD}}{64d} \times (oscillator\ frequency)$$

Interrupts:

- Interrupts used to call a sub-routine on a priority base.
- Can be generated using program (software) or by the hardware.
- Response to interrupts is faster in microcontrollers.
- This allows the controllers in real-time programming.
- Interrupts can be generated either by internal circuits or by external hardware.
- Five interrupts provided in 8051.
- Three are: timer flag 0, timer flag 1, and the serial port interrupt (RI/TI).
- Two interrupts are triggered by the external hardware through $\overline{\text{INTO0}}$ and $\overline{\text{INTO1}}$

Interrupts:

- Interrupts are controlled by the programmer through IE, IP, and TCON registers.

IE (Interrupt Enable)

7	6	5	4	3	2	1	0
EA	-	ET2	ES	ET1	EX1	ET0	EX0

Bit	Symbol	Function
7	EA	**Enable Interrupts:** cleared to 0 by program to disable all interrupts.
6	---	Not Defined
5	ET2	Reserved
4	ES	**Enable serial port interrupt:** Set/cleared by program.
3	ET1	**Enable Timer 1 Overflow Interrupt**
2	EX1	**Enable External Interrupt 1**
1	ET0	**Enable Timer 0 Overflow Interrupt**
0	EX0	**Enable External Interrupt 0**

IP (Interrupt Priority)

7	6	5	4	3	2	1	0
-	-	PT2	PS	PT1	PX1	PT0	PX0

Bit	Symbol	Function
7	-	**Not implemented**
6	-	Not Implemented
5	PT2	Reserved
4	PS	**Priority of Serial Port Interrupt**
3	PT1	**Priority of Timer 1**
2	PX1	**Priority of External Interrupt 1**
1	PT0	**Priority of Timer 0**
0	PX0	**Priority of External Interrupt 0**

8051 Instruction Set
&
Addressing Modes

Addressing Modes

Immediate

- Data is part of the instruction itself.
- When an immediate data move is executed, the PC is automatically incremented to point to the byte(s) following the opcode byte in the program memory.
- Data found at that location is copied into destination address.
- # is the mnemonic for immediate data.

Ex: **MOV A**, #DATA

MOV Reg, #DATA

Register

- Registers are part of the opcode.
- Registers A, DPTR, R0 – R7 may be part of the opcode mnemonic.
- Other registers may be addresses using direct addressing mode.

Ex: **MOV A, R0**

MOV R5, DPH

Direct

- All 128 bytes of internal RAM can be addresses directly.
- Internal RAM uses address from 00H-7FH.
- The SFRs are existing from 80H to FFH.

Ex: **MOV A**, Addr

MOV Addr, **DPH**

Indirect

- Uses a register to hold the actual address that will finally be used in the data move.
- The register itself is not the address, but the register content.
- Indirect addressing for **MOV** opcodes uses R0 or R1, often called data pointers to hold the address of one of the data locations.

Ex: **MOV @Rp**, #DATA

MOV @Rp, A

Data Transfer

- Transfer data between registers, registers and memory.
- Memory is divided into four distinct physical parts
  - Internal RAM
  - Internal Special function registers (SFRs)
  - External RAM
  - Internal and External ROM

MOV Move

Syntax: MOV destination operand, source operand

➢ Both the operands must be of same size.

References

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2. Microprocessors and Interfacing – D. V. Hall, TMH, 2nd Edition 2006.
3. The Intel Microprocessors: Architecture, Programming, and Interfacing – Barry B. Brey, Pearson, 8th Edition 2009.

Thank You