

## Timers and phase Locked Loops

IC 555 Timer:-

\* This 555 timer IC is a very popular IC and very useful in the timing related applications.

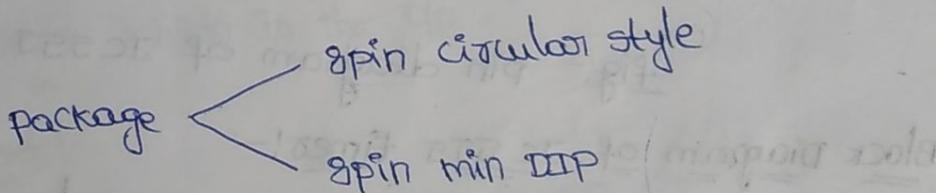
\* For example whenever it is used as a relaxation oscillator, then it can be used as a tone and Alarm Generator.

\* And it can be used for the frequency division or for generating the timing delays.

\* This is available in so many packages.

\* The 555 timer is a highly stable device for generating accurate time delays or oscillations.

\* It is available in two package styles.



\* A single 555 timer can provide time delay ranging from micro seconds to hours, where as counter timer

can have

\* The 555 timer can be used with supply voltage in the range of +5V to +18V can drive load upto 200 mA.

\* Because of this wide range of supply voltage, the

555 timer is easy to used in various applications.

\* The various applications like oscillator, pulse generator, Ramp and square wave generator, traffic light control

and voltage monitor etc.

### \* The 8 pin IC Timer:-

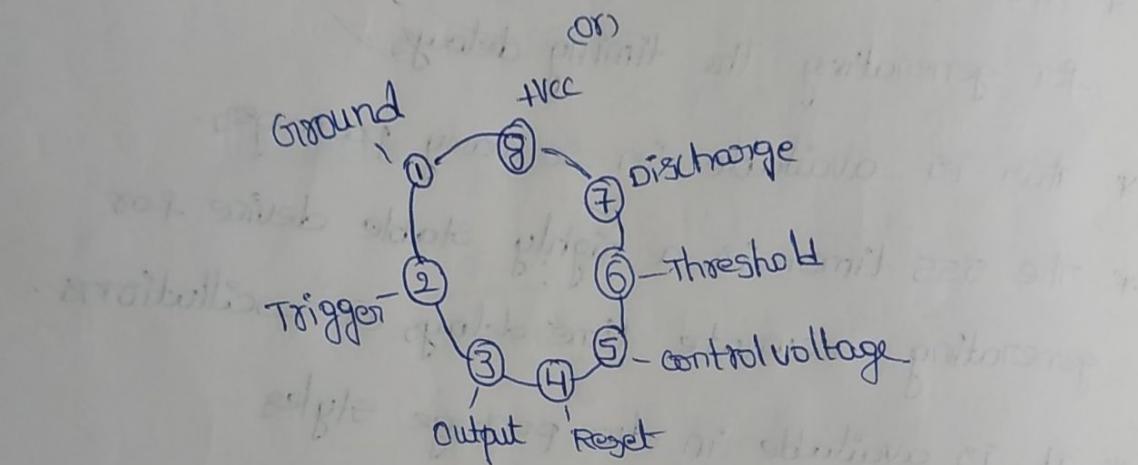
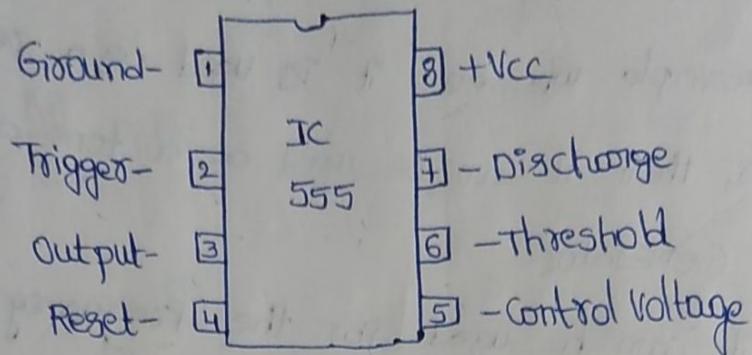
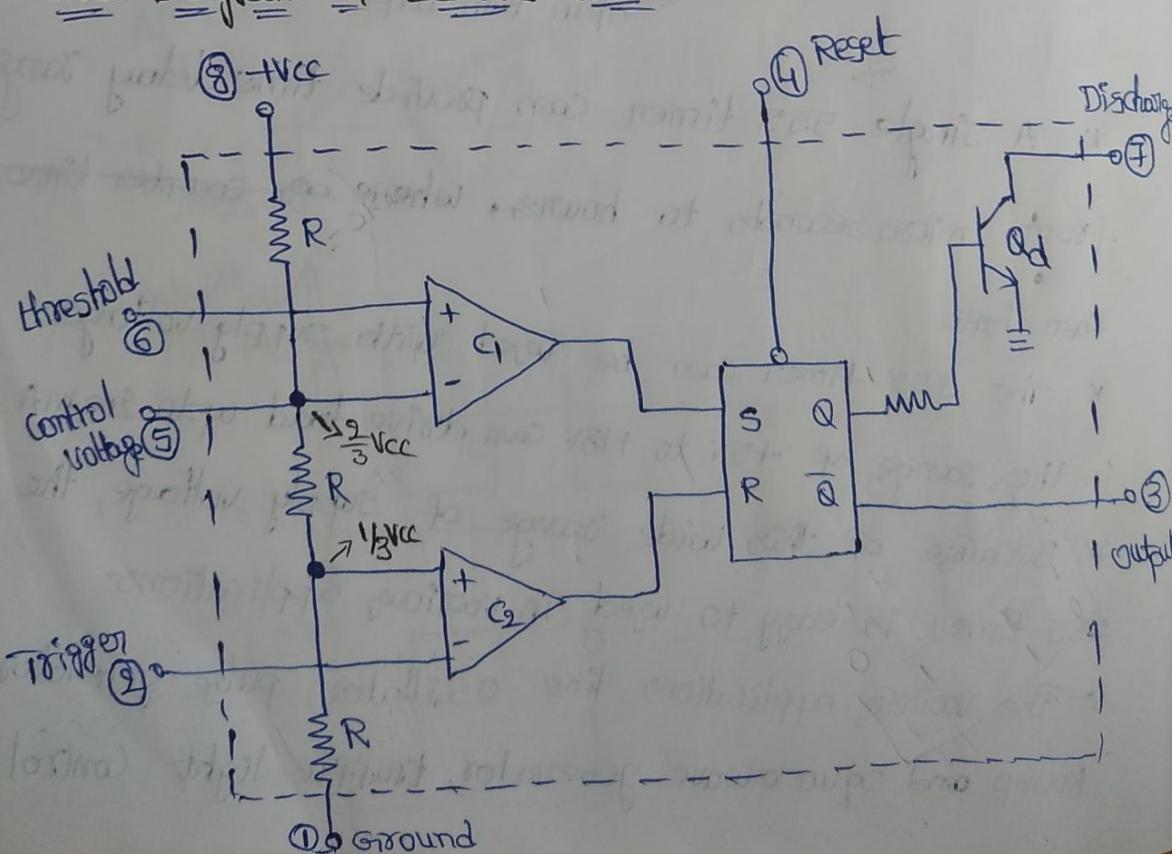


fig:- pin diagram of IC 555

### Block Diagram of IC 555 timer:-



### Pin 1 :- Ground :-

- \* All the voltages are measured with respect to this terminal.

### Pin 2 :- Trigger :-

- \* The IC 555 timer uses two comparators  $C_1$  &  $C_2$ .
- \* The voltage divider consists of three equal resistors. Due to the voltage divider, the voltage at the terminal of  $C_2$  is fixed at  $\frac{V_{CC}}{3}$ .
- \* The -ve terminal of  $C_2$ , which is compared with  $\frac{V_{CC}}{3}$ .
- \* When the trigger input  $< \frac{V_{CC}}{3}$  then  $C_2$  output goes high.
- \* This op-amp given to Reset pin of SR flip-flop.  
If trigger input  $> \frac{V_{CC}}{3}$  then  $C_2$  output goes low.

### Pin 3 :- Output :-

- \* The complementary signal output ( $\bar{Q}$ ) of the flip-flop goes to pin 3, which is the QP.

### Pin 4 :- Reset :-

- \* This is an interrupt to the timing device.
- \* Pin 4 provides ON/OFF feature to the IC 555.
- \* This pin 4 also overrides all other functions within the timer when it is momentarily grounded.

### Pin 5 :- Control Voltage

- \* In most of the applications, external control voltage input is not used.
- \* This pin connected to -ve terminal of  $C_1$ . Due to the voltage divider circuit, the -ve terminal of  $C_1$  holds the voltage of  $\frac{2}{3}V_{CC}$ .

- \* This  $\frac{2}{3}V_{CC}$  can compare with threshold applied at the terminal of  $C_1$ . In some cases, if we require more than the  $\frac{2}{3}V_{CC}$  as control signal, at that time we can externally apply this control voltage input.
- \* If external sig applied to pin 5 is alternating then the reference level for  $C_1$  keeps on increasing.
- \* Due to this, the variable pulse width o/p is possible. This is called pulse width modulation, which is possible due to pin 5.

#### Pin 6:- Threshold:-

\* This is non-inverting o/p terminal of  $C_1$ . The external

~~control~~ voltage is applied to this pin 6.

\* When this threshold voltage is more than  $\frac{2}{3}V_{CC}$ ,  $C_1$  output goes high. So, this is given to o/p of SR flipflop to set pin.

\* This high o/p of  $C_1$  sets the flipflop. Then o/p of flipflop  $Q$  is high &  $\bar{Q}$  is low. Then the o/p of IC 555 at pin 3 goes low.

\* If threshold  $> \frac{2}{3}V_{CC}$ ,  $C_1$  o/p high, flp set &  $Q \rightarrow$  high.  
pin 3  $\bar{Q} \rightarrow$  low

\* If threshold  $< \frac{1}{3}V_{CC}$   $C_1$  o/p is low, flp reset &  $Q \rightarrow$  low  
trigger pin 3  $\bar{Q} \rightarrow$  high.

### Pin 7:- Discharge:-

- \* This pin is connected at collector of the discharge transistor Qd.
- \* When output pin is high, Q is low, due to this Qd is off. Now, it act as an open circuit to the external capacitor C to be connected across it.
- \* When the OLP pin is low, Q is high, due to this Qd is ON and it act as short circuit, shorting the external capacitor C to be connected across it.

### Pin 8:- Supply +Vcc:-

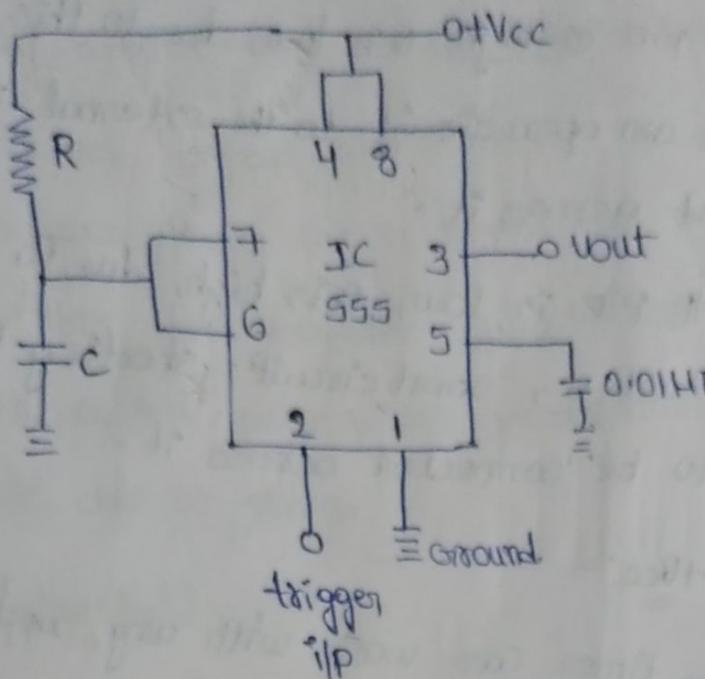
→ The IC 555 timer can work with any supply voltage between 4.5V to 16V.

### Features of IC 555 timer:-

- \* The 555 is a monolithic timer device which can be used to produce accurate and highly stable time delays or oscillations. It can be produce time delays ranging from few micro seconds to several hours.
- \* It has two basic operating modes :-
  1. Monostable
  2. Astable.
- \* It is available in 2 packages.
- \* The NE 555 can operate with a supply voltage in the range of 4.5V to 18V and is capable of sourcing and sinking OLP currents of 200mA.
- \* It has very high temperature stability range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .
- \* Its output is compatible with TTL, CMOS and op-amp circuits.

## Mono stable Multivibrator using IC 555:-

Schematic Diagram of Mono stable Multivibrator using IC 555.



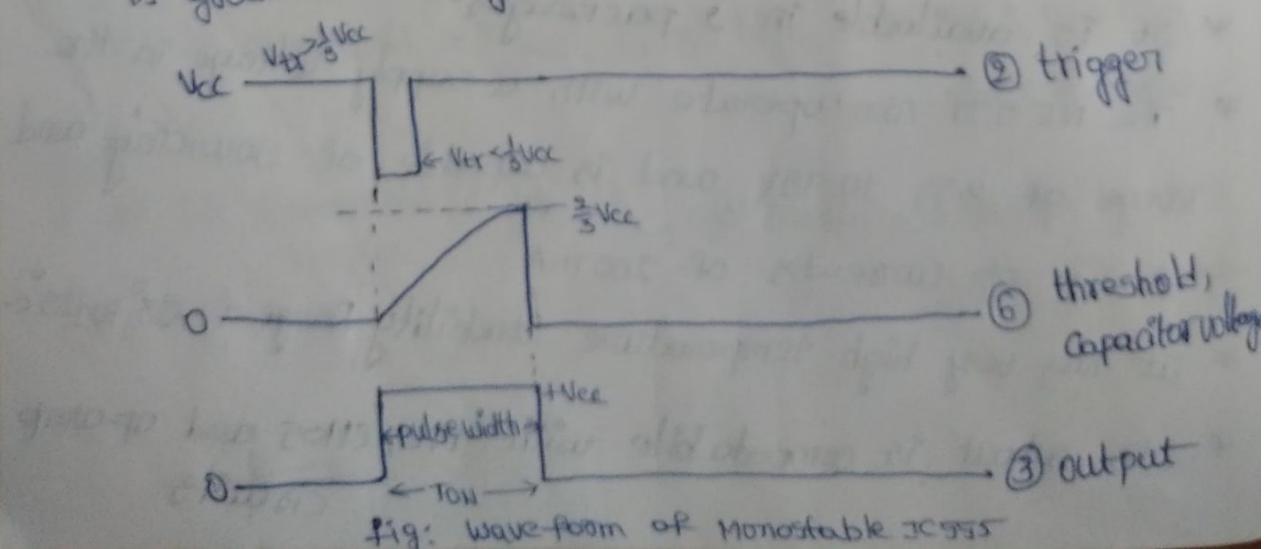
- \* The schematic diagram of IC 555, in which does not include comparators, flipflops etc.

- \* It only shows the external components to be connected to this 8 pin of IC 555.

- \* Here, the external components are R & C

- \* To avoid accidental reset, pin 4 is connected to pin 8, which is connected to +Vcc.

- \* To achieve the noise filtering of control voltage, the pin 5 is grounded through a small capacitor of 0.01μF.



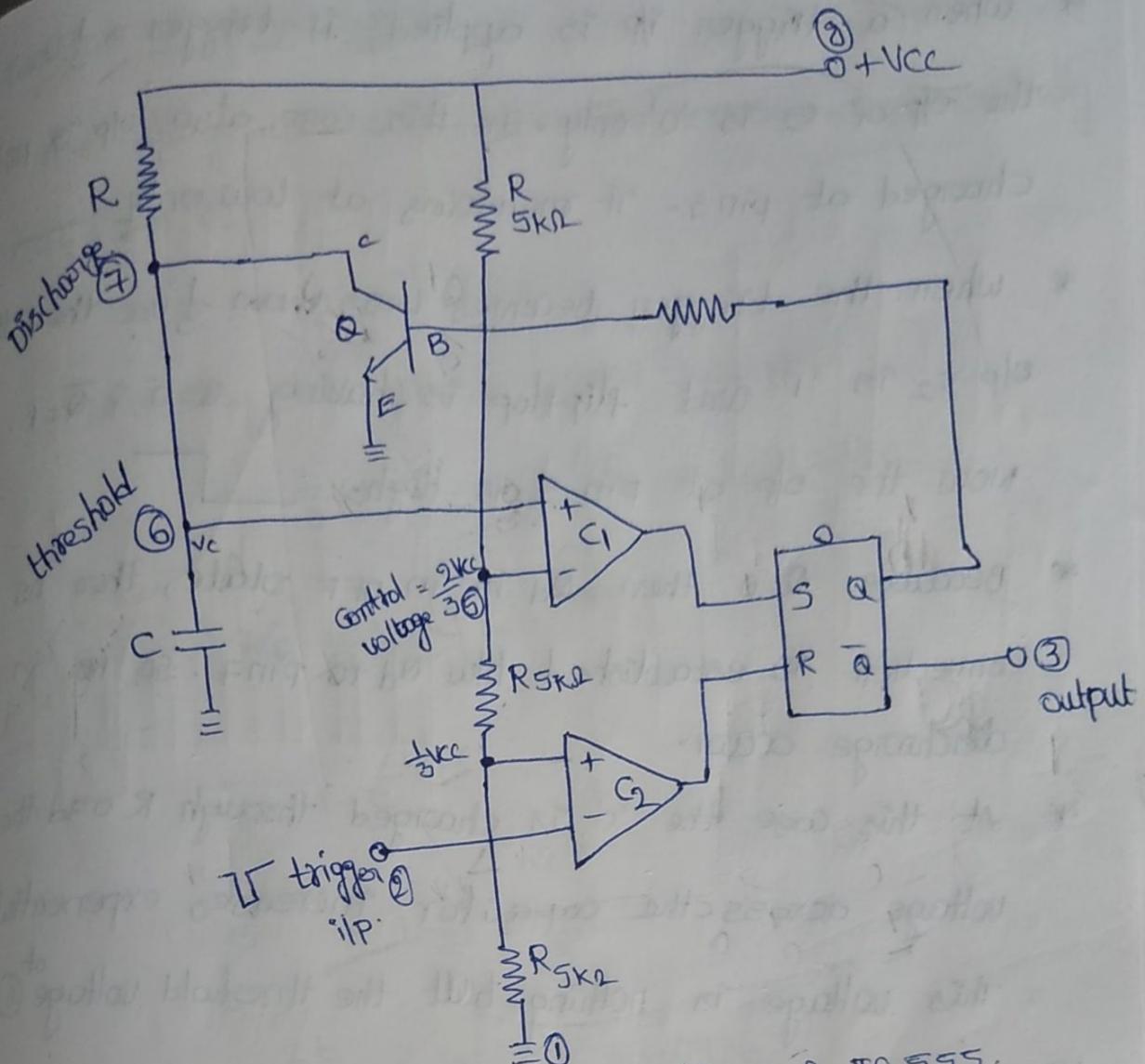


Fig:- Monostable operation of IC 555.

\* The IC 555 timer can be operated as a monostable multivibrator by connecting a external  $R \& C$ .

\* This circuit has only one stable state.

\* When trigger is applied, it produces a pulse at the output & return back to its stable state.

### operation:-

\* The SR flip-flop is initially set, i.e.,  $Q=1$  then OLP is  $\bar{Q}$ . So, the  $\bar{Q}=0$ , i.e. OLP is Low —

\* due to  $Q=1$ , the  $Q_d$  is ON and the external capacitor 'C' discharges to the ground.

\* When a trigger voltage is applied, if trigger >  $\frac{1}{3} V_{CC}$  the o/p of  $C_2$  is '0' only. In this case also o/p is not charged at pin 3. It maintains at low only.

\* When the trigger becomes less than  $\frac{1}{3} V_{CC}$  then the o/p  $C_2$  is '1' and flip-flop is having  $Q=0 \& \bar{Q}=1$ . Now the o/p at pin 3 is high.

\* Because,  $Q=0$  then  $Q_d$  is in OFF state, then no connection is established b/w  $Q_d$  to pin 7. So, no discharge occurs.

\* At this stage the 'C' is charged through R and the voltage across the capacitor increases exponentially. This voltage is nothing but the threshold voltage  $V_T$ .

\* If this threshold voltage increases  $V_T > \frac{2}{3} V_{CC}$ , then  $C_1$  o/p goes high. So,  $Q=1, \bar{Q}=0$ , here again o/p goes to low at pin 3.

\* This high Q drives the  $Q_d$  in saturation, then 'C' quickly discharges through  $Q_d$ .

\* The pulse width of this rectangular pulse is controlled by the charging time of capacitor, this depends on the time constant  $RC$ . This  $RC$  controls the pulse width of o/p signal.

Derivation of pulse width:-

The voltage across the capacitor increases exponentially and given by,

$$V_C = V_C(1 - e^{-t/RC}) \quad \text{--- (1)}$$

According to virtual ground concept,

$$V_C = \frac{2}{3} V_{CC} \quad \text{and from eqn, } V = V_{CC}$$

$$\therefore \frac{2}{3} V_{CC} = V_C [1 - e^{-t/RC}]$$

$$\frac{2}{3} = 1 - e^{-t/RC}$$

$$e^{-t/RC} = 1 - \frac{2}{3} = \frac{1}{3}$$

$$\frac{t}{RC} = \ln\left(\frac{1}{3}\right) = -1.0986$$

$$t = 1.0986 RC$$

$$\therefore t \approx 1.1 RC$$

\* So, we can say that the voltage across capacitor will reach  $\frac{2}{3} V_{CC}$  in approximately 1.1 times time constant.

Applications of monostable multivibrator using IC 555:-

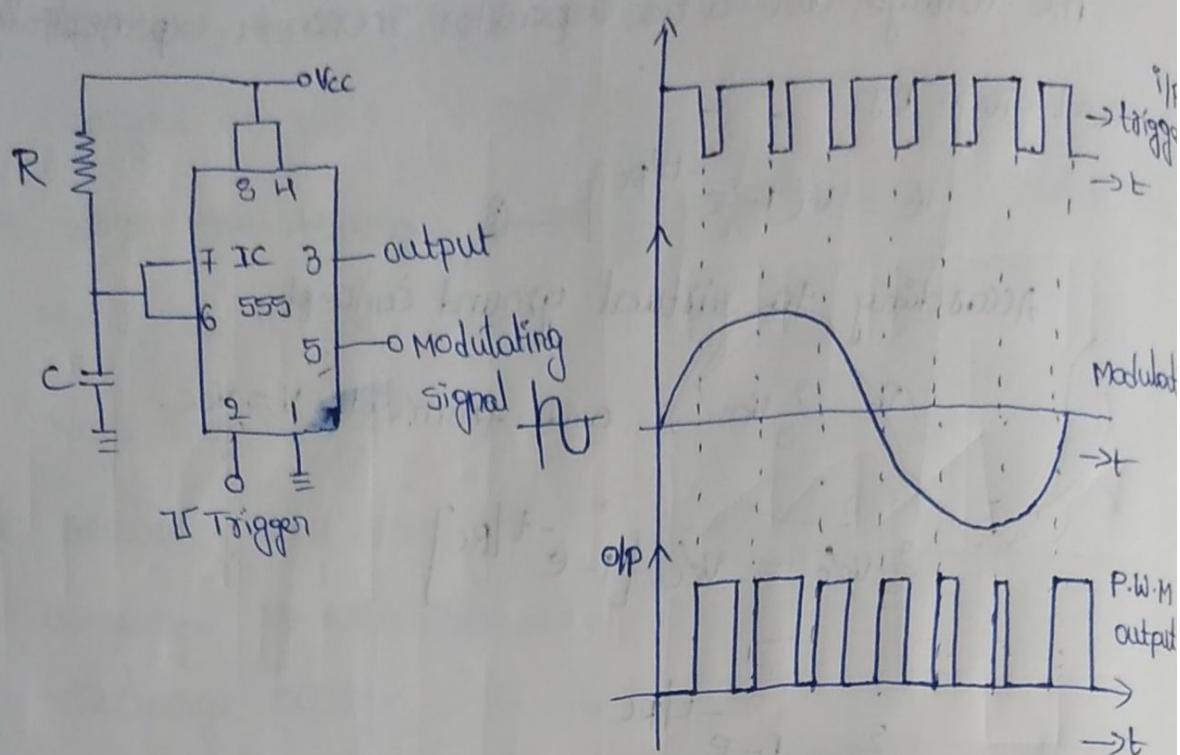
1. pulse width modulation

2. Frequency divider

3. Linear ramp generator

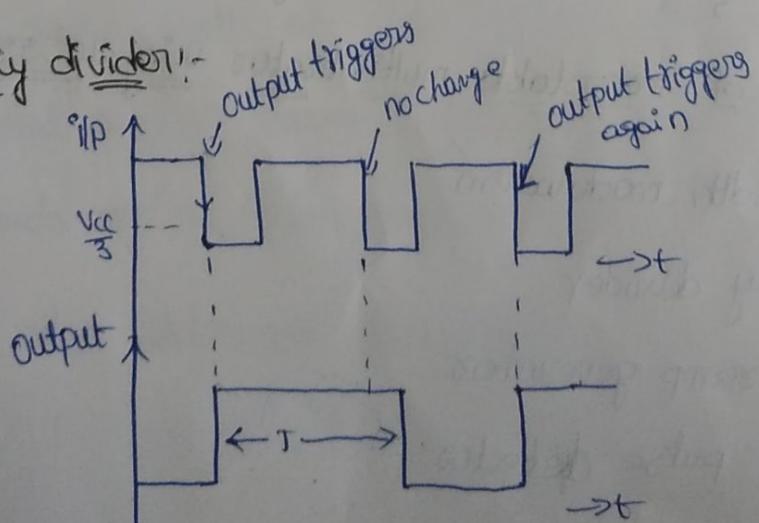
4. Missing pulse detector.

## 1) pulse width modulation :-



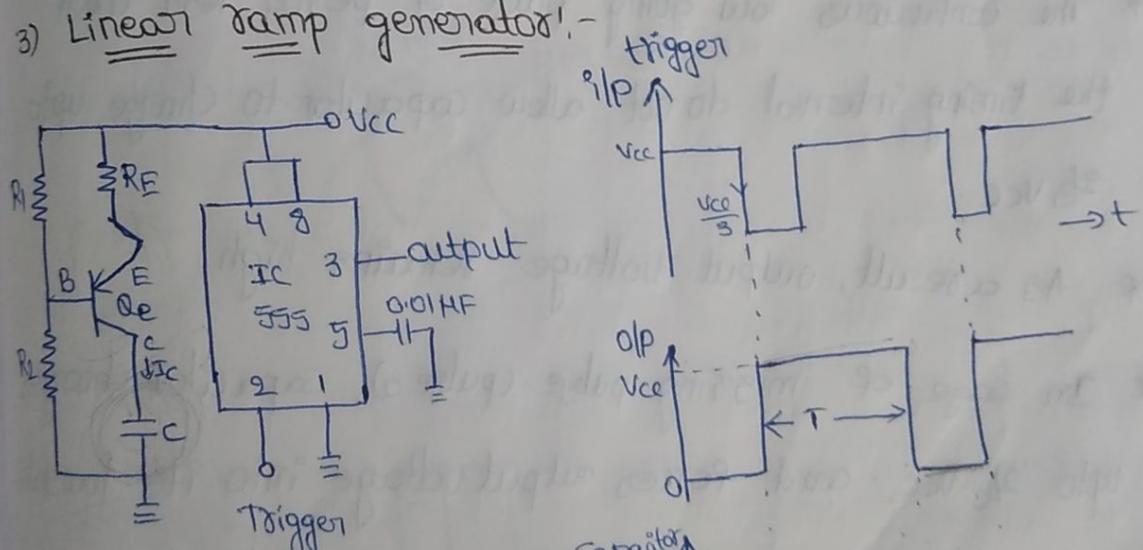
- \* It is basically a monostable multivibrator with a modulating input signal applied at the control voltage input pins.
- \* Internally, the control voltage is adjusted to the  $\frac{2}{3} V_{CC}$ .
- \* Externally, applied modulating signal changes the control voltage and hence the threshold voltage level of the comparator (A) also effected.
- \* As a result, time period required to charge the capacitor upto threshold voltage level changes, so, the output of pulse width is modulated.

## 2) Frequency divider :-



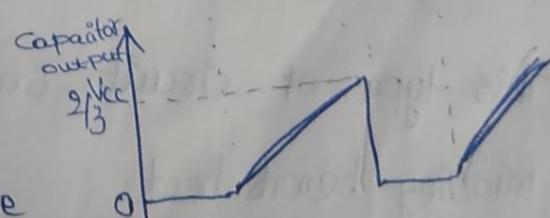
- \* A continuously triggered monostable circuit when triggered by a square wave generator can be used as frequency divider.
- \* If the timing interval is adjusted to be longer than the period of triggering square wave input signal.
- \* The monostable multivibrator will be triggered by the first negative going edge of  $i_{lp}$  but  $o_{lp}$  will remain HIGH for next negative going edge of  $i_{lp}$ . [because of greater timing interval]
- \* The  $o_{lp}$  will trigger on the third negative going  $i_{lp}$ , depending on the choice of the time delay.
- \* In this way, the output can be made integral fractions of the frequency of the input triggering pulse.

### 3) Linear ramp generator:-



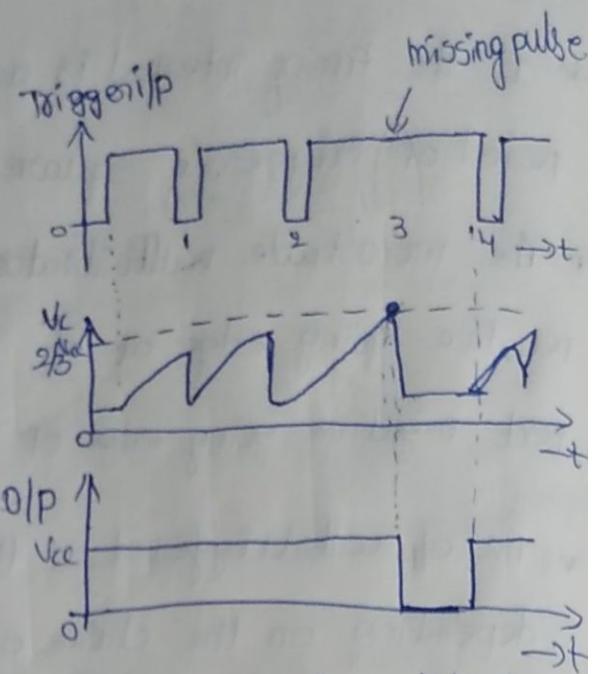
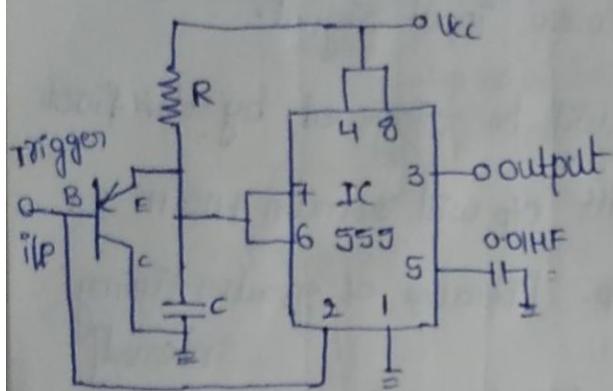
- \* The current  $I_c$  charges capacitor C at a constant rate towards  $+V_{CC}$ .

- \* When capacitor voltage  $V_c$  becomes  $\frac{2}{3}V_{CC}$ , the comparator makes internal transistor ON. Then capacitor discharges.



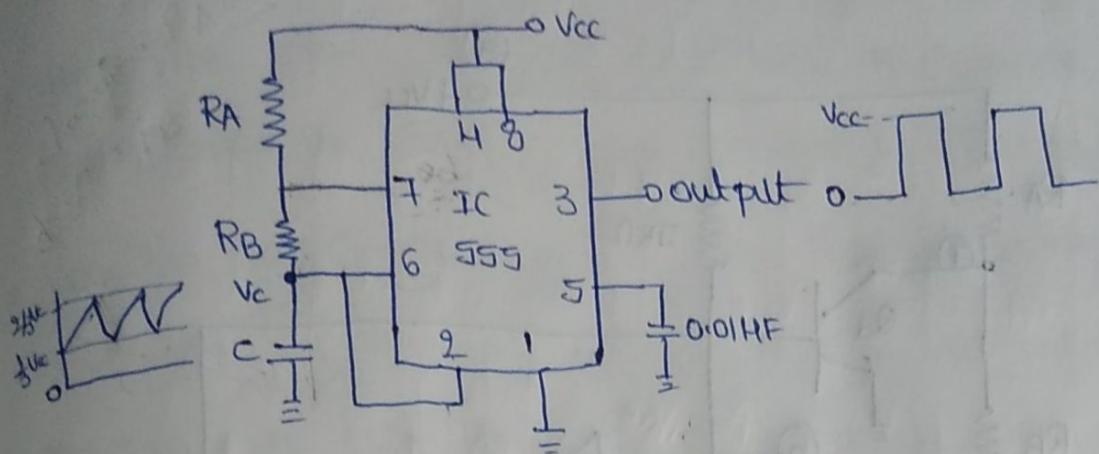
- \* The capacitor is charged linearly by the constant current source formed by the transistor Qe.

#### 4) Missing pulse detector:-



- \* In this circuit timing interval is adjusted such that it is slightly longer than the period of input signal.
- \* The continuous low going pulse of period less than the timing interval do not allow capacitor to charge upto  $\frac{2}{3}V_{CC}$ .
- \* As a result, output voltage remains high.
- \* In case of missing pulse (pulse 3), capacitor charges upto  $\frac{2}{3}V_{CC}$  and forces output voltage into its low state.
- \* This type of circuit can be used to detect a missing heart beat.

# Astable multivibrator using IC 555:-



- \* It shows only the external components RA, RB & C.
- \* The pin 4 is tied to pin 8. and pin 5 is grounded through a small capacitor.
- \* The important application of Astable multivibrator is voltage controlled oscillator (vco).
- \* Here, the pin 2 & pin 6 also tied.

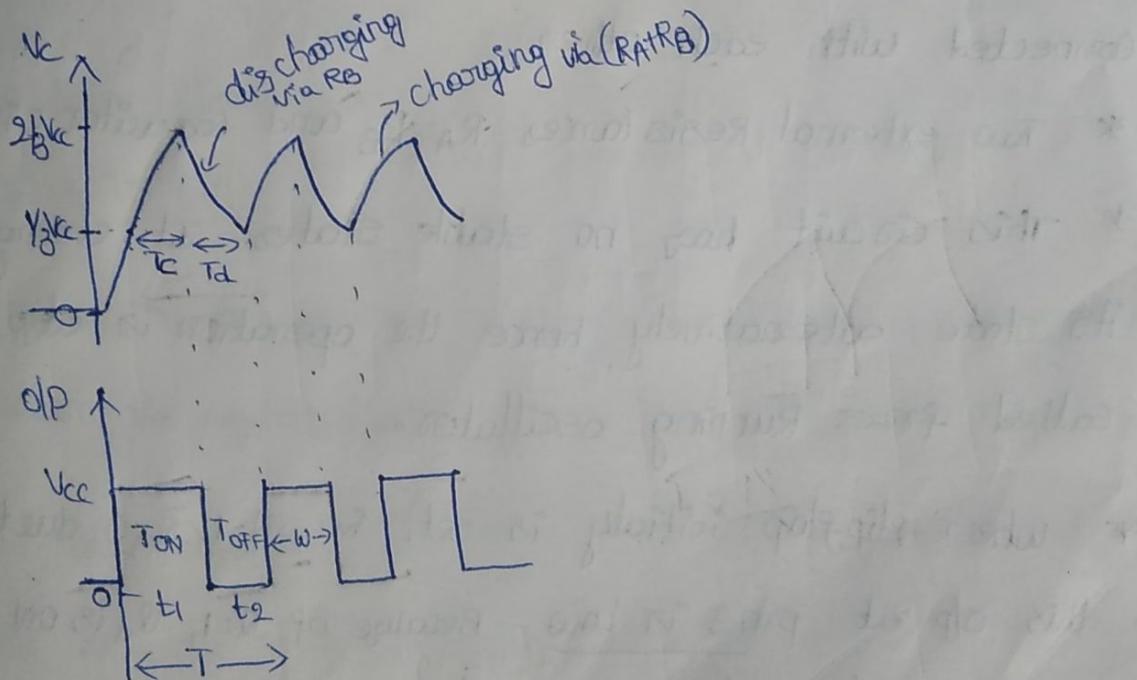
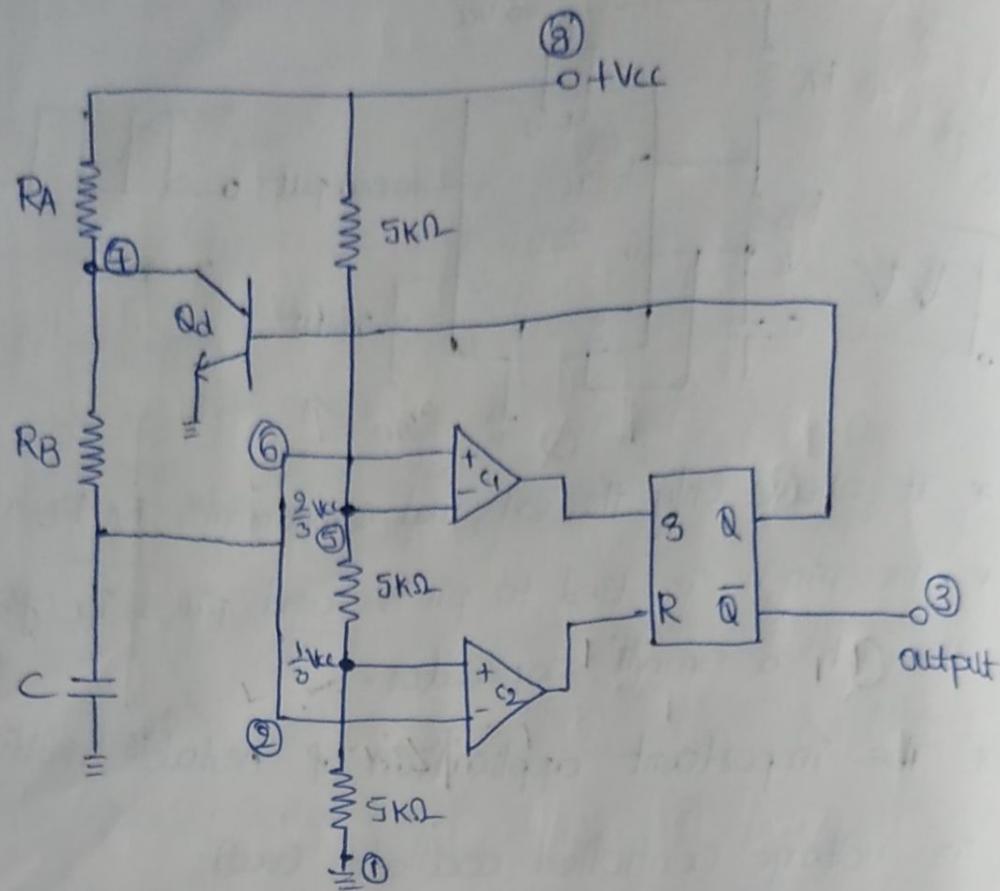


fig:- Wave forms of astable operation.

## Operation:-



- \* In this circuit the threshold o/p & trigger o/p are connected with each other.
- \* Two external resistances  $R_A$ ,  $R_B$  and capacitor  $C$  is used.
- \* This circuit has no stable states. It changes its state alternatively, hence the operation is also called free running oscillator.
- \* When flip flop initially is set, i.e.,  $Q=1$ ,  $\bar{Q}=0$  due to this o/p at pin 3 is low. Because of  $Q=1$ ,  $Q_d$  is ON &  $C$  gets discharged.
- \* Now, the capacitor voltage is nothing but the trigger voltage, so, while discharging, it becomes less than the  $\frac{1}{3}V_{cc}$  then o/p of  $c_2$  is high.  $Q$  is low.
- \* Then flip flop output  $Q=0$ ,  $\bar{Q}=1$ , now o/p at pin 3 is high.

\* Because of  $Q=0$ , the Qd is OFF and the capacitor charges through the resistors  $R_A, R_B \& V_{CC}$ .

\* Here, the total charging path total resistance is  $(R_A+R_B)$  and the charging time constant is  $(R_A+R_B)C$ .

\* Now, the capacitor voltage is also threshold voltage. If C is charged, the threshold voltage is also increased than the  $\frac{2}{3}V_{CC}$ . At this time the o/p of  $C_1$  is high,  $Q_1$  is low.

then o/p of flipflop is  $Q=1 \& \bar{Q}=0$ . i.e the o/p at pin 3 is Low.

\* This  $Q=1$  drives the Qd and capacitor starts discharging. The discharging constant is  $R_B \cdot C$ .

\* When voltage across C is discharged, then trigger o/p is also decreased & o/p of  $Q_2$  is high,  $Q_2$  is low. Due to this flipflop o/p  $Q=0 \& \bar{Q}=1$ . i.e, the o/p at pin 3 is high.

\* Thus, when the o/p is high, Capacitor is charged and when the o/p at pin 3 is low, Capacitor is discharged.

\* The capacitor charges exponentially and output of Astable multivibrator is a rectangular wave.

\* The voltage across the capacitor increases exponentially and given by,

$$V_C = V_{CC} (1 - e^{-t/R_C}) \quad \text{--- ①}$$

\* if capacitor charges from 0 to  $\frac{2}{3}V_{CC}$  then

$$\frac{2}{3}V_{CC} = V_{CC}(1 - e^{-t_1/RC})$$

$$\therefore t_1 = 1.09 RC$$

\* if capacitor charges from 0 to  $\frac{1}{3}V_{CC}$  then

$$\frac{1}{3}V_{CC} = V_{CC}(1 - e^{-t_2/RC})$$

$$t_2 = 0.405 RC$$

In Astable multivibrator capacitor charges from  $\frac{1}{3}V_{CC}$  to  $\frac{2}{3}V_{CC}$  and discharges from  $\frac{2}{3}V_{CC}$  to  $\frac{1}{3}V_{CC}$ .

∴ time to charge from  $\frac{1}{3}V_{CC}$  to  $\frac{2}{3}V_{CC}$

$$t_{High} = t_1 - t_2 = 1.09 RC - 0.405 RC$$

$$\therefore T = t_{High} = 0.69 RC \Rightarrow T = 0.69(R_A + R_B)C$$

time to discharge from  $\frac{2}{3}V_{CC}$  to  $\frac{1}{3}V_{CC}$

$$T_d = 0.69 R_B C$$

one cycle period = Total time =  $T_c + T_d$

$$= 0.69(R_A + R_B)C + 0.69 R_B C$$

$$T = 0.69(R_A + 2R_B)C$$

$$\therefore \text{frequency} = f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

## Duty cycle:-

- \* Generally the charging time constant is greater than the discharging time constant. Hence, the o/p waveform is not symmetric.
- \* The high o/p remains for longer period than low o/p. The Ratio of high o/p period ( $T_{ON}$ ) and low o/p period is given by a mathematical parameter called duty cycle.
- \* It is defined as the ratio of ON time, i.e., high o/p to the total time of one cycle.

$$\therefore \text{Duty cycle (D)} = \frac{W}{T} = \frac{T_{ON}}{T_{total}}$$

$$\% D = \frac{W}{T} \times 100 = \frac{T_{ON}}{T_{total}} \times 100$$

$$\therefore \% D = \frac{0.693(R_A + R_B)C}{0.693(R_A + 2R_B)C} \times 100$$

$$\% D = \frac{(R_A + R_B)}{(R_A + 2R_B)} \times 100$$

- \* If  $R_A$  is much smaller than  $R_B$ , then duty cycle approaches to 50% and o/p waveform approaches to square wave.

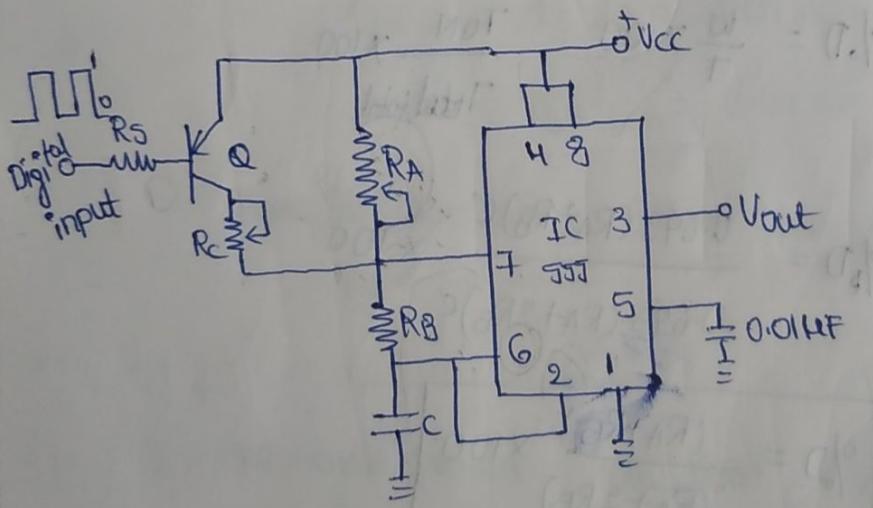
square wave

## Applications of Astable multivibrator using IC 555:-

1. square wave generator
2. FSK generator
3. voltage controlled oscillator (VCO)

FSK generator: - [Frequency shift keying generator]

- Binary code consists of 1's and 0's. It can be transmitted by shifting a carrier frequency. One fix frequency represents one and other represents zero. This type of transmission is called frequency shift keying technique. Astable multivibrator using 555 can be used to generate FSK signal.



- when digital input is high (1), transistor Q is OFF and 555 timer works as normal astable mode. The frequency of the op waveform is

$$f_o = \frac{1.45}{(RA + 2RB)C}$$

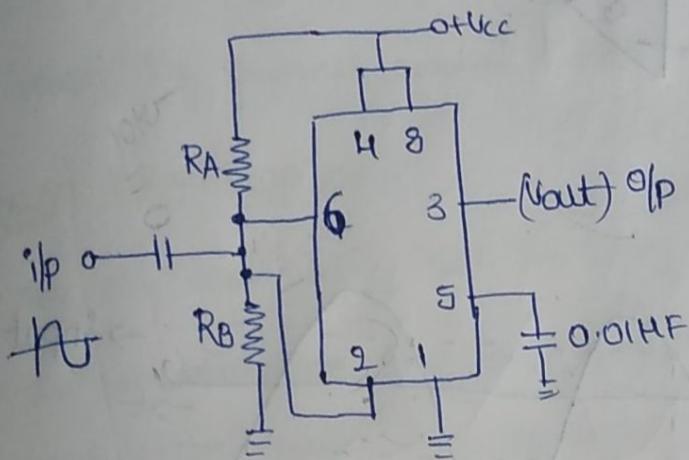
- when input is Low (0), transistor Q is ON and connects the resistor RC in parallel with RA.

The frequency of the o/p waveform is

$$f_o = \frac{1.45}{[(R_{A||R_C}) + 2R_B]C}$$

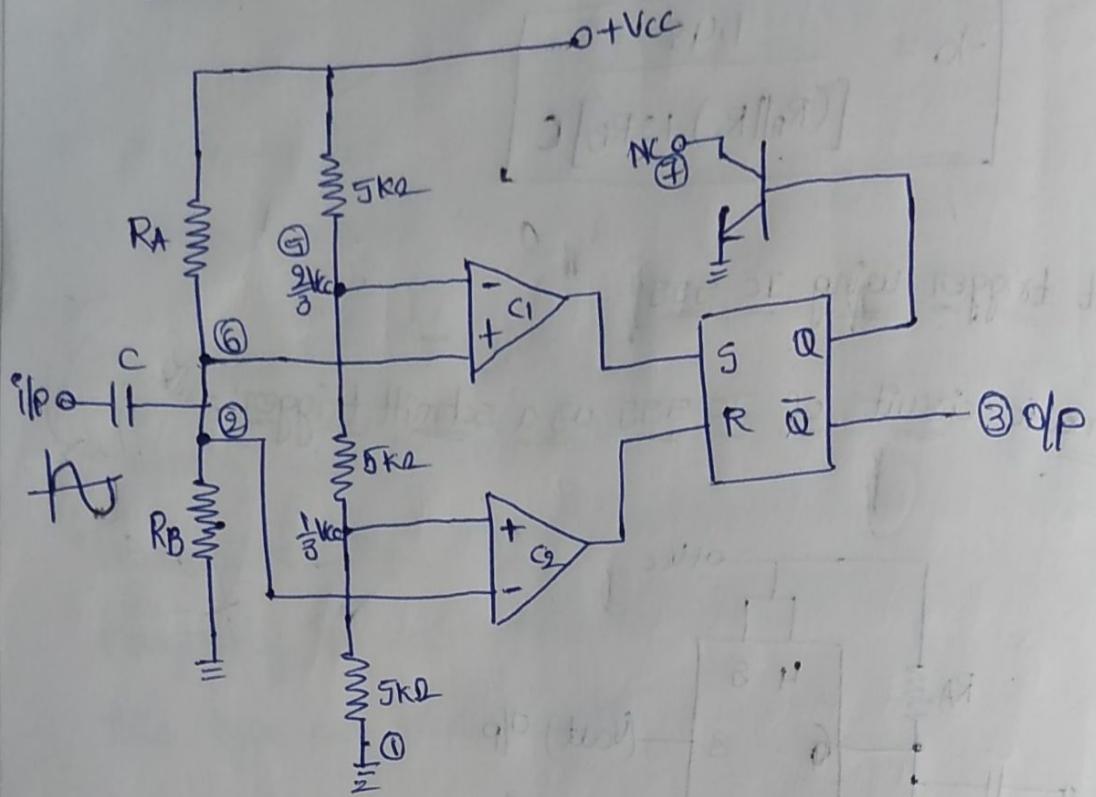
Schmitt trigger using IC 555:

Schematic circuit of IC 555 as a Schmitt trigger:

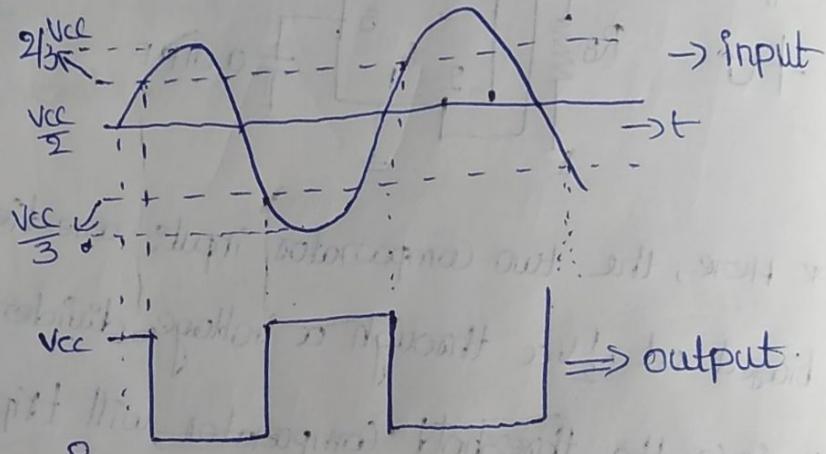


- \* Here, the two comparator inputs are tied together and biased at  $\frac{1}{2}V_{CC}$  through a voltage divider  $R_A \approx R_B$ .
- \* Since, the threshold comparator will trip at  $\frac{2}{3}V_{CC}$  and the trigger comparator will trip at  $\frac{1}{3}V_{CC}$ , this bias is provided by the  $R_A \approx R_B$  is centered within comparators trip limits.
- \* A sine wave i/p of sufficient amplitude to exceed the reference levels causes the internal flip flop to be set and Reset.
- \* In this way, it creates a square wave at the o/p.
- \* If  $R_A = R_B$ , then bias voltage is  $V_{CC}/2$ .
- \* The o/p waveform is  $180^\circ$  out of phase with the applied sine wave.

## Operation:-



\* Initially



\* Initially set the flip-flop op at 0'. i.e  $Q=0$  and  $\bar{Q}=1$ . Now the o/p pin ③ is high.

\* Now, we know that i/p for a schmitt trigger is a sine wave. if i/p signal is high then capacitor is charged

\* if the voltage at 'd' increased then the terminal of  $i_1$  is increased due to this  $+ve\ i/p > \frac{2}{3}V_{CC}$  then o/p of  $C_1$  is increased

\* similarly, the voltage at -ve terminal of  $C_2$  is also increased. due to this  $-ve\ i/p > \frac{1}{3}V_{CC}$  then o/p of  $C_2$  is 0.

\* Now the op's given to the flip-flop as  $S=1$  &  $R=0$  due to this  $Q=1$ ,  $\bar{Q}=0$  then op at pin 3 is Low.

- \* the output is high when 'ilp' signal is low (decreasing) the capacitor voltage is decreased. when it decreased less than  $\frac{1}{2}V_{cc}$  then  $C_1$  output is 0,  $C_2$  output is 1. then the op's given to the flip-flop as  $S=0$ ,  $R=1$  then  $Q=0$ ,  $\bar{Q}=1$  then op at pin 3 is high. \* then the output wave form is square wave.

### phase Lock loop:-

\* The PLL are widely used in many applications in electronics.

\* In communication, they are used in the synchronization and Demodulation circuit. For example, in the FM demodulation and in the FSK, they are commonly used.

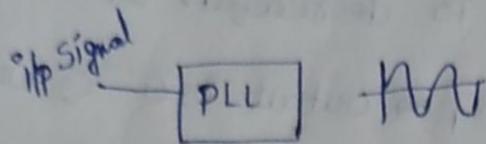
\* Apart from that, when one wants to recover the clock from incoming bit stream, then using the PLL, it quite possible.

\* In communication system, for the noise reduction, the PLL commonly used.

\* Now, one of the most common application of the PLL is the frequency synthesizer.

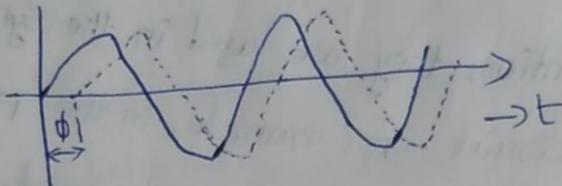
\* So, using this PLL, it is possible to generate the op frequency which is multiple of the 'ilp' frequency.

PLL: - PLL is basically a closed loop system, designed to lock output frequency and phase to frequency and phase of an input signal.



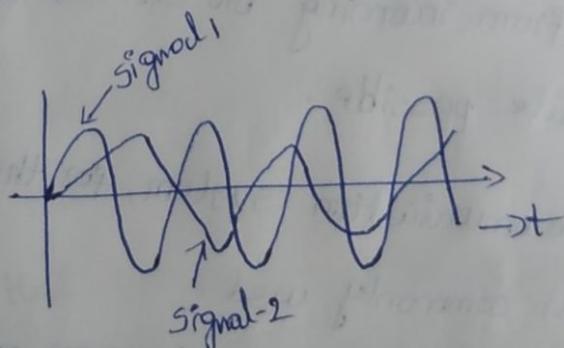
- \* As per name, it is control system as, the control loop which maintains the same phase b/w the o/p and i/p signal.
- \* In some systems, we get some phase difference b/w the two signals. At this time the phase difference can be corrected by these type of systems.

For ex:-



- \* In the above fig, the two signals are at the same frequency but there is a constant phase difference b/w the two signals.

\* Another example:-

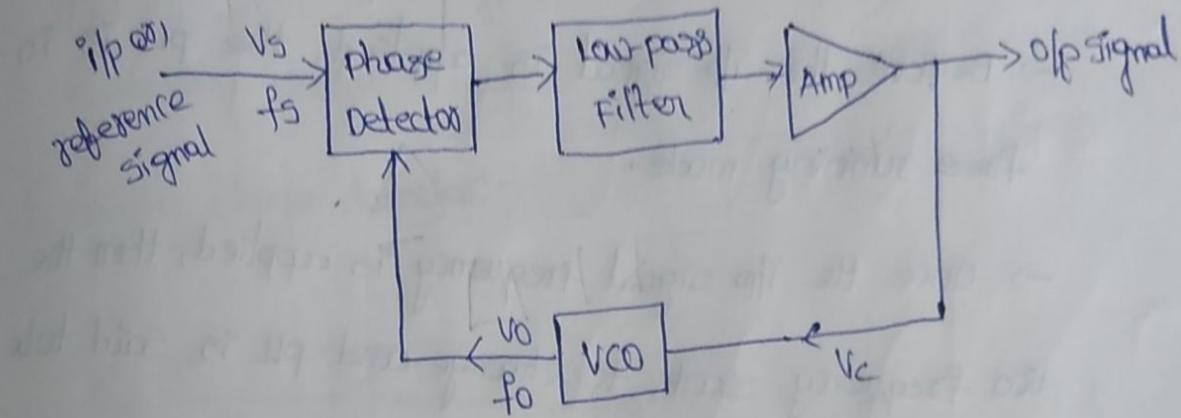


- \* In the above figure, the two waveforms started at the same time, but there is a different frequency of the signal and the phase b/w the two signals continuously changing with time.

→ The phase Lock loop system, synchronize the output signal with the input signal in the page as well as in frequency.

so, when the o/p frequency is equal to the i/p frequency and there is no phase difference or, the constant phase difference b/w the two signals, then we can say that the loop is in the lock condition.

### Block diagram of PLL :-



\* The PLL consists of ~~three~~ <sup>four</sup> basic building blocks.

- They are
  1. phase detector
  2. Low-pass filter
  3. Amplifier
  4. VCO

\* The VCO, as the control voltage changes, then the frequency of the oscillation also changes.

\* The phase detector is fundamentally a multiplier, and produces the sum ( $f_s + f_o$ ) and the difference ( $f_s - f_o$ ) components at its o/p.

\* The high frequency component ( $f_s + f_o$ ) is removed by the low pass filter and the difference frequency component through amplifier.

is amplified and then applied as a control voltage  $V_C$  to the VCO.

\* The signal  $V_c$  shifts the VCO frequency in a direction to reduce the frequency difference b/w  $f_s$  and  $f_o$ .

\* The PLL operates 3 modes:

1. Free running mode
2. Capture mode
3. Lock mode.

→ Before the  $i_{pp}$  signal is applied, the PLL is in free running mode.

→ Once the  $i_{pp}$  signal frequency is applied, then the VCO frequency starts to change and PLL is said to be in capture mode.

→ The VCO frequency continuously changes until it equals the input frequency and PLL is in phase lock mode.

### Definitions:

1. Lock-in-Range: - The range of frequencies over which the PLL can maintain the lock with the incoming signals is called the Lock-in-range or tracking range.

2. Capture Range: - The range of frequencies over which the PLL can acquire the lock with an input signal is called Capture Range.

3. Pull-in-time: - The total time taken by the PLL

to establish the lock is called pull-in-time. This depends on the initial phase or, frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

### Phase Detector / Phase Comparator:-

\* There are two types of phase detectors.

1. Analog phase detector
2. Digital phase detector.

### Analog phase detector:-

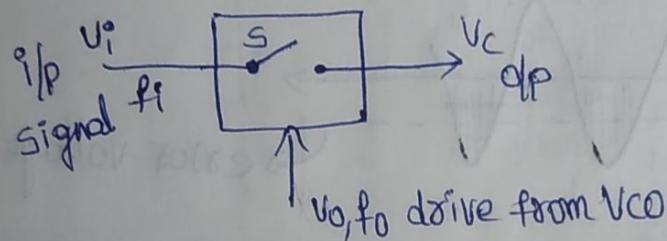


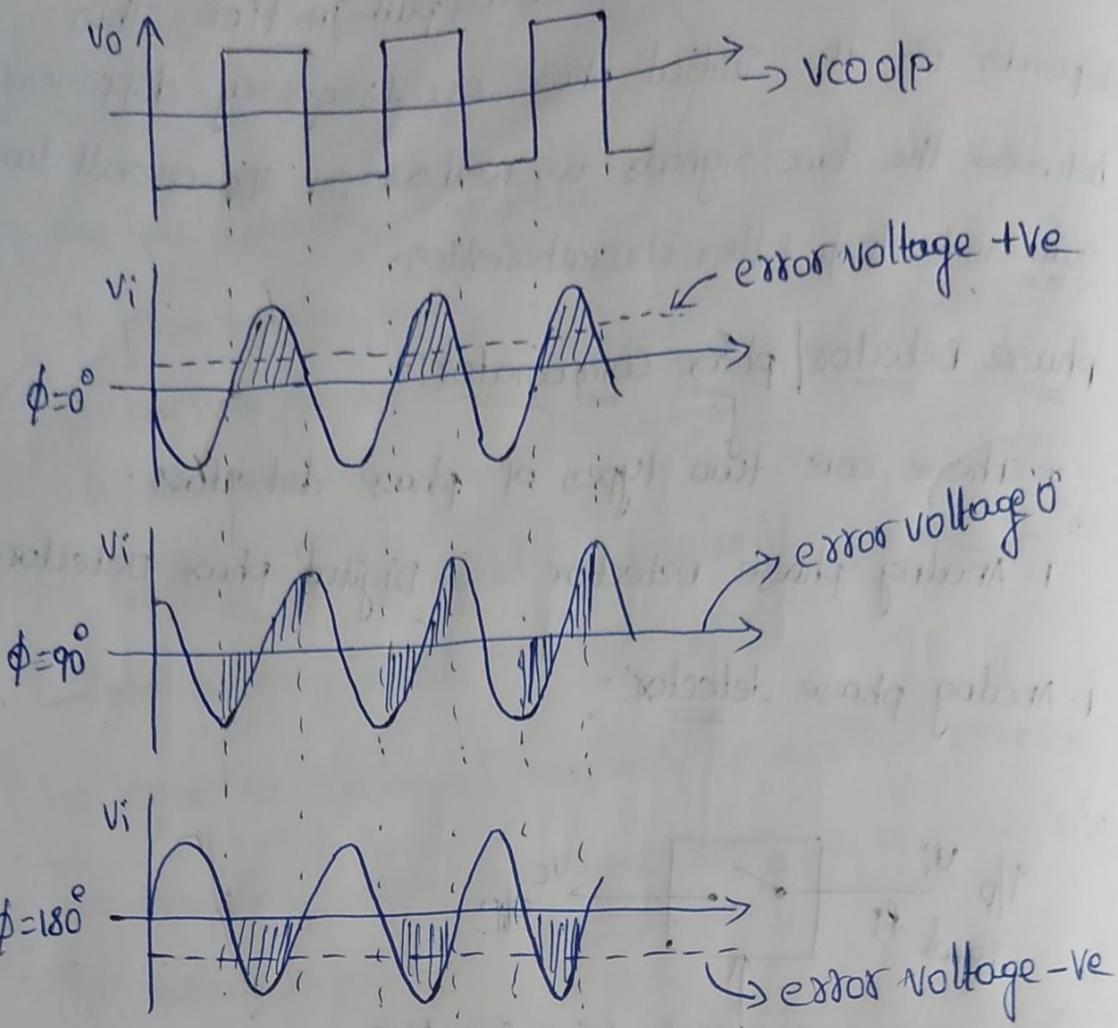
fig:- electronic switch.

\* The Analog phase detector realized by using an electronic switch.

\* Assuming that, the signal from VCO operates the electronic switch, the i/p signal  $v_i$  is chopped by the VCO frequency.

\* The  $v_i \& v_{co}$  o/p square wave produces different values of filtered error voltages w.r.t. various values of phase error  $v_c$ . is shown in waveforms.

\* The o/p of the phase detector when passed through the filter gives out an average error signal shown by dotted lines in the below waveforms.



when  $\phi = 90^\circ$ , error voltage  $V_c = 0$ , perfect lock is achieved.

Digital phase Detector:-

\* The digital type XOR act as phase detector.

\* The op of the XOR gate is high when only one of the ifp signals fo or fi is high.

\* This type of detector is used where both the ifp signals are square waves.

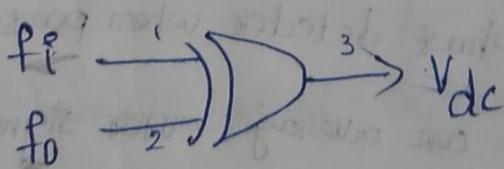
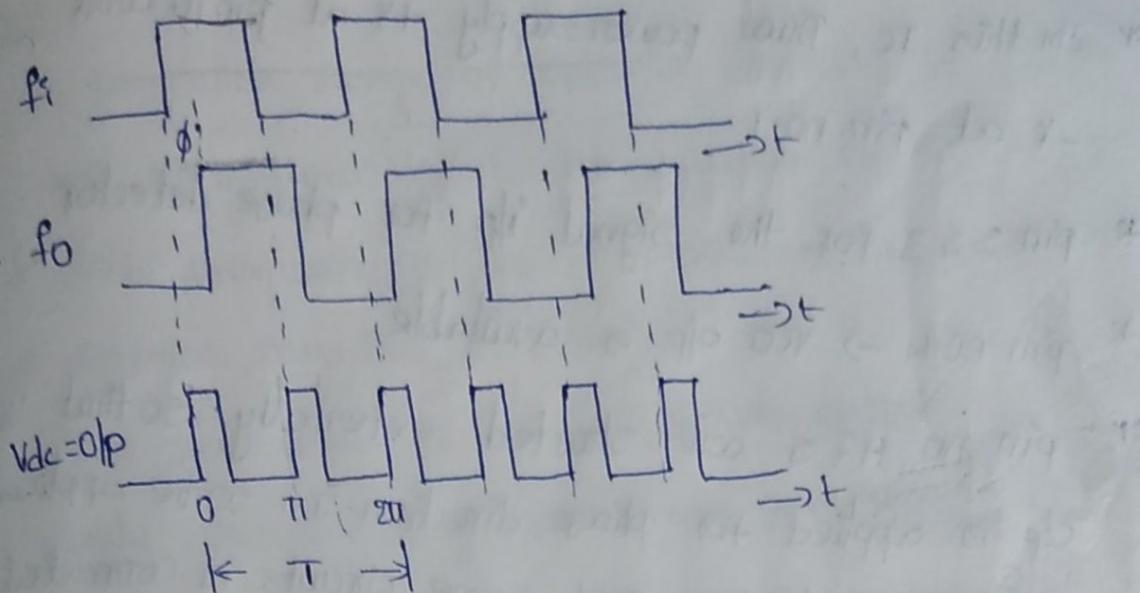


fig: EX-OR phase detector



PLL IC - 565:-

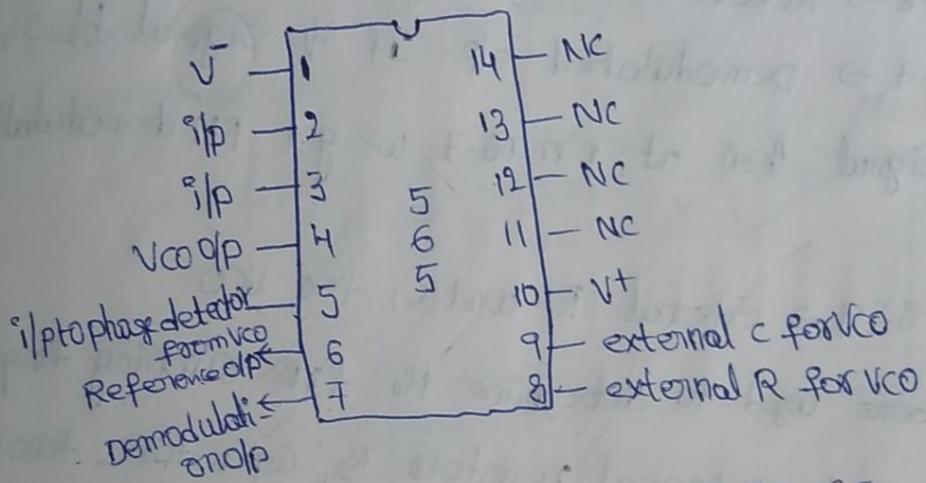
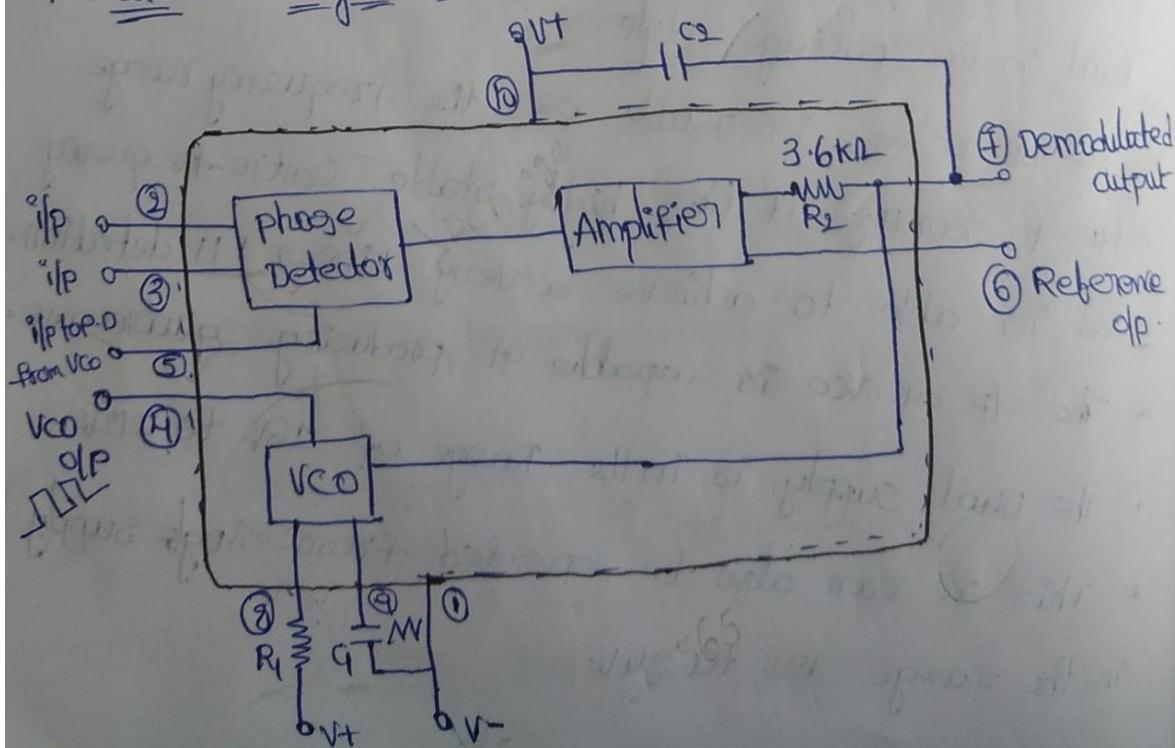


Fig. Pin diagram of IC 565.

- \* The IC 565 acts as a PLL, and it is a 14 pin IC, in dual in line package style.
- \* The PLL IC 565 is usable over the frequency range 0.1 Hz to 500 kHz. It has highly stable centre frequency and is able to achieve a very linear FM detection.
- \* The o/p of VCO is capable of producing squarewave.
- \* The dual supply is in the range of  $\pm 6V$  to  $\pm 12V$ .
- \* This IC can also be operated from single supply in the range 12V to 24V.

- \* In this IC, Dual power supply +V at pin 10 and -V at pin no. 1.
- \* pin 2 & 3 for the signal ifp for phase detector.
- \* pin no. 4 → VCO o/p is available
- \* pin no 4 & 5 are shorted externally, so that VCO o/p is applied for phase direction. In some application PLL loop is broken and some circuits is connected b/w pin no: 4 & 5.
- \* pin no-6 → Reference dc Voltage is available.
- \* pin no-7 → Demodulated o/p. If ifp signal b/w 2 & 3 is FM signal then at pin no. 7, we get FM demodulation output.
- \* pin no. 8 & 9 → external  $R_1$  and  $C_1$  for VCO.
- \*  $R_1, C_1$  are used to determine the free running frequency of VCO. and Internal resistor  $R_2$ , capacitor  $C_2$  form LPF of VCO. The value of internal resistor  $R_2$  is 3.6 k $\Omega$ .

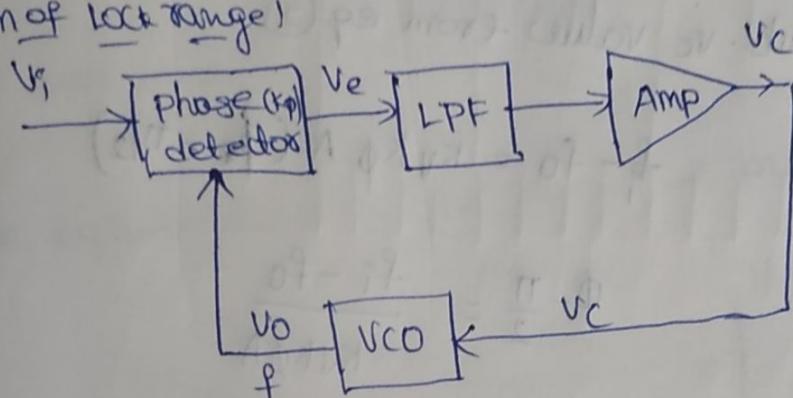
Functional Diagram of IC 565:-



## features:

1. it has wide range of operating voltage  $\pm 16V$  to  $\pm 12V$
2. very high linearity of demodulated o/p typically  $0.2\%$
3. centre frequency of  $V_O$  is programmable by means of resistors, capacitors or voltage
4. VCO generates the square wave output.
5. highly linear triangular wave o/p available at pin no: 9.
6. Loop can broken b/w pin no. 4 & 5 and external circuit can be added.
7. conversion ratio of phase detector  $K_\phi = 1.4/\pi$

## Derivation of lock range



\* output of voltage of phase detector is

$$V_e = K_\phi (\phi - \frac{\pi}{2}) \quad \text{--- ①}$$

where  $\phi$  is phase error.

$K_\phi$  is phase coefficient.

\* The output voltage of a phase detector is filtered by the low pass filter to remove the high frequency component.

\* The output of the filter is amplified by a gain A and then applied as the control voltage  $V_C$  to the VCO as given by.

$$V_C = A V_{BE}$$

$$V_C = A K_\phi (\phi - \frac{\pi}{2}) - ②$$

- this control voltage  $V_C$  will result in a shift in the VCO frequency from its center frequency  $f_0$  to a frequency  $f_i$ .

- When PLL is locked, if frequency is

$$f = f_i = f_0 + K_V V_C$$

sub:  $V_C$  value from eq ②

$$f_i - f_0 = K_V K_\phi A (\phi - \frac{\pi}{2})$$

$$\phi - \frac{\pi}{2} = \frac{f_i - f_0}{K_V K_\phi A}$$

$$\phi = \frac{\pi}{2} + \frac{f_i - f_0}{K_V K_\phi A}$$

- The  $V_C(\max)$  available from the phase detector occurs for  $\phi = \pi$  and  $0$ .

$$V_C(\max) = \pm K_\phi (\frac{\pi}{2})$$

$$V_C(\max) = \pm K_\phi (\frac{\pi}{2}) \cdot A$$

where  $\Delta f_L$  will be then,

$$f = f_i = f_0 \pm K_V K_\phi (\frac{\pi}{2}) \cdot A$$

$$= f_0 \pm \Delta L$$

where  $\pm \Delta f_L$  will be lock-in frequency range given by,

$$\text{lock range} = \pm \Delta f_L = K_V K_d \cdot A \cdot \frac{\pi}{2} \quad \therefore \Delta f_L = K_V K_d A \cdot \frac{\pi}{2}$$

$$\text{From VCO, } K_V = \frac{8f_0}{V}$$

$$\text{where } V = +V_{cc} - (V_{cc}) \quad \therefore f_0 = \frac{0.95}{R_1 C_1} \text{ from VCO}$$

$$\text{FOR PLL 565, } K_d = \frac{1.4}{\pi} \text{ and } A = 1.4. \text{ then}$$

Substitute the values we get,

$$\Delta f_L = \pm \frac{8f_0}{V} \times \frac{1.4}{\pi} \times 1.4 \times \frac{\pi}{2}$$

$$\text{Lock range: } \boxed{\Delta f_L = \pm \frac{7.84f_0}{V}}$$

\* The equation for capture range of PLL is given by,

$$\Delta f_{cap} = \pm \left[ \frac{\Delta f_L}{2\pi \times 3.6 \times 10^3 \times Q} \right]^{1/2}$$

Applications:-

1. Frequency multiplication/Division:-

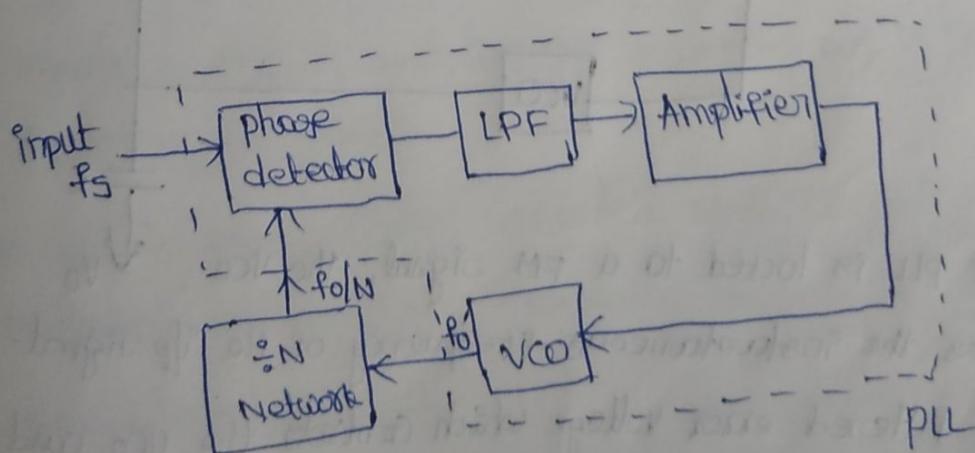
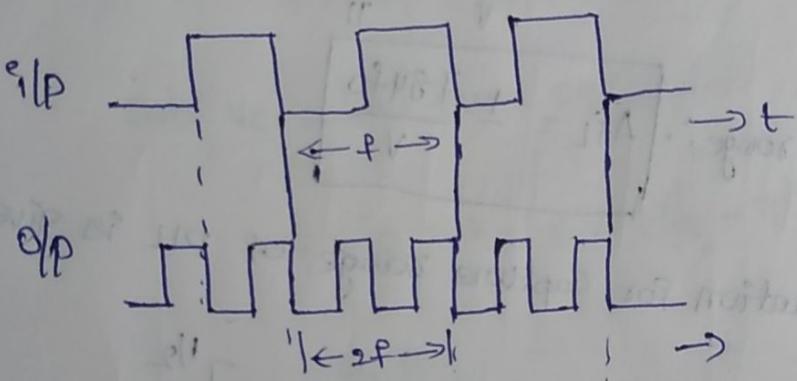


Fig.: Frequency multiplier using IC PLL.

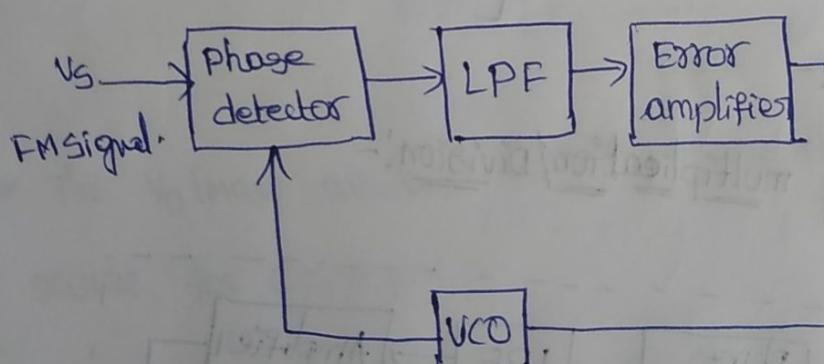
- \* Here, A divide by N network is inserted between the VCO output (pin 4) & phase comparator input (pin 5).
- \* The o/p of the divider will lock the i/p frequency, so, the VCO is actually running at a multiple of the input frequency.
- \* Therefore, in the locked state, the VCO output frequency

$$f_o = N f_i$$

if  $N=2$ , then



### FM demodulator:-



- \* If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the i/p signal.
- \* The filtered error voltage which controls the VCO and maintains lock with the i/p signal is the demodulated FM output.

- \* The VCO transfer characteristics determine the linearity of the demodulated output.
- \* Since VCO used in PLL is highly linear, it is possible to realize highly linear FM demodulators.

### AM Detection:-

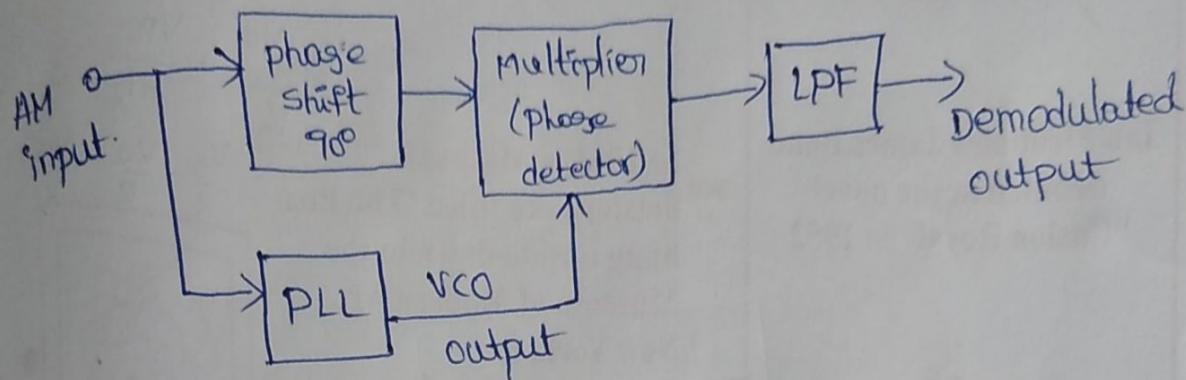


Fig:- PLL used as AM demodulator.

- \* A PLL may be used to demodulate AM signals.
- \* The PLL is locked to the carrier frequency of the I/p AM signal. The o/p of VCO, has the same frequency as the carrier, but unmodulated is fed to the multiplier.
- \* Since VCO output is always  $90^\circ$  out of phase with incoming AM signal under the lock condition, both the signals applied to multiplier then multiplier out is sum and difference of signals.
- \* The lowpass filter connected at the output of the multiplier rejects high frequency components, gives demodulated output.