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## Voltage controlled oscillator (VCO)

A common type of VCO is available in IC form i.e. Signetics NE/SE 566. The pin configuration and basic block diagram of 566 VCO are shown in Fig. A tuning capacitor  $C_T$  is linearly charged or discharged by constant current source or current can be controlled. The amount of current applied at the chip.

The voltage at pin 6 is held at the same voltage as pins. Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across  $R_T$  and thereby decreasing the charging current.

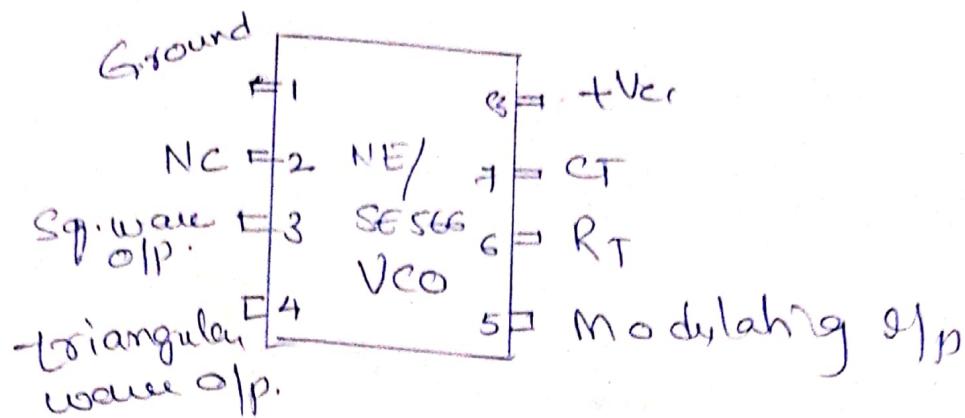


Fig (a)

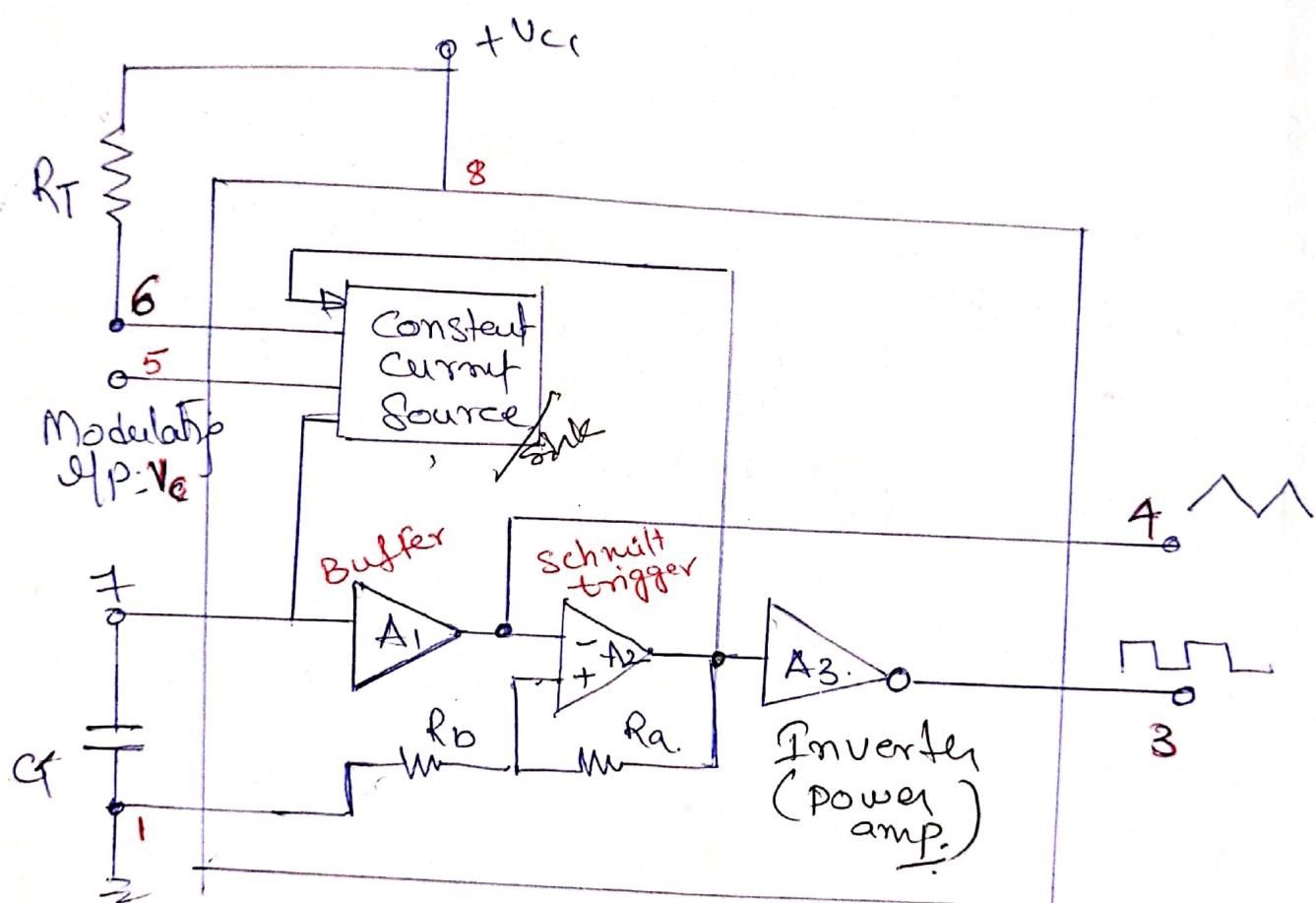


Fig (b)

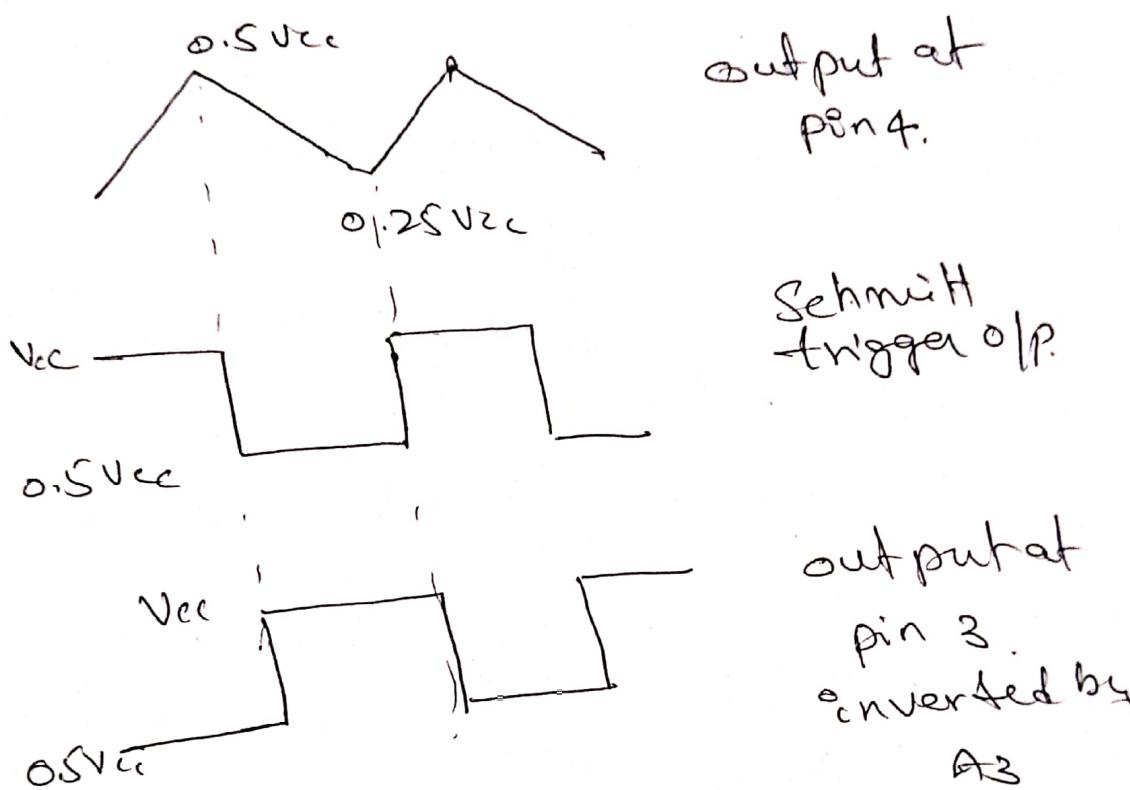
Voltage controlled oscillator (a) Pin configuration

(b) Block diagram.

- \* The voltage across the capacitor  $C_T$  in ③ applied to the inverting input terminal of Schmitt trigger  $A_2$  via buffer amplifier  $A_1$ ,
- \* The output voltage swing of the Schmitt trigger is designed to  $V_{cc}$  and  $0.5V_{cc}$ .
- \* If  $R_a = R_b$  in the positive feedback loop, the voltage at the non inverting input terminal of  $A_2$  swings from  $0.5V_{cc}$  to  $0.25V_{cc}$ .
- \* When the voltage on the capacitor  $C_T$  exceeds  $0.5V_{cc}$  during charging, the output of the Schmitt trigger goes low ( $0.5V_{cc}$ ).
- \* The capacitor now discharges and when it is at  $0.25V_{cc}$ , the output of Schmitt trigger goes HIGH ( $V_{cc}$ ).
- \* Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time.
- \* This gives a triangular voltage wave form across  $C_T$  which is also available at pin 4.

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The square wave output of the Schmitt trigger is inverted by inverter A<sub>3</sub> and is available at pin 3. The output waveforms are shown in Fig.



The output frequency of the VCO can be calculated as follows.

The total voltage on the capacitor changes from 0.25 V<sub>cc</sub> to 0.5 V<sub>cc</sub>.

Thus  $\Delta V = 0.25 V_{cc}$ .

The capacitor charges with a constant current source.

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$$\text{So } \frac{\Delta V}{\Delta t} = \frac{i}{C_T}$$

$$\frac{0.25 V_{cc}}{\Delta t} = \frac{i}{C_T}$$

$$\Delta t = \frac{0.25 V_{cc} \cdot C_T}{i} \quad \rightarrow (1)$$

The time period 'T' of the triangular waveform =  $2 \Delta t$ . The freq. of oscillation  $f_0$  is

$$f_0 = \frac{1}{T} = \frac{1}{2 \Delta t}$$

~~$$f_0 = \frac{0.25 V_{cc} \cdot C_T}{2 \times 0.25 V_{cc} \cdot C_T}$$~~

$$f_0 = \frac{i}{2 \times 0.25 V_{cc} \cdot C_T} \quad \rightarrow (2)$$

$$f_0 = \frac{i}{0.5 V_{cc} C_T}$$

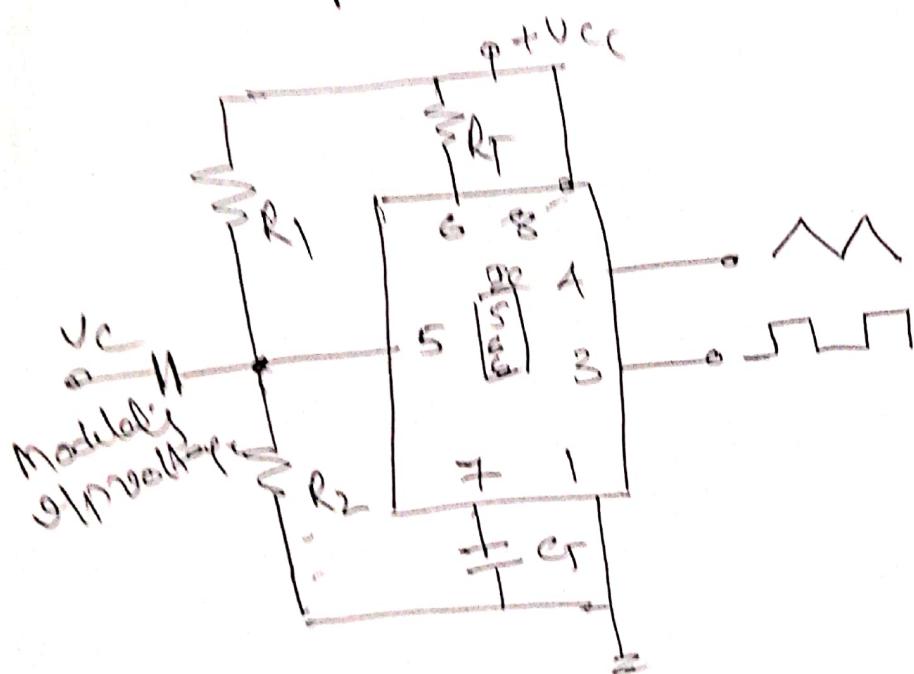
$$\text{But } i = \frac{V_{cc} - V_c}{R_T}$$

where  $V_o$  is the Voltage at pin 5. ⑥

$$\therefore f_o = \frac{2(V_{ee} - V_e)}{C_F R_F V_o} \quad (3)$$

The output frequency of the VCO can be change by (i)  $R_f$  (ii)  $C_F$  or (iii) the Voltage  $V_e$  at the modulating I/P terminal Pin 5.

The Voltage  $V_e$  can be varied by connecting a  $R_1 R_2$  circuit as shown in Fig.



Typical connection diagram.

The components  $T_F$  and  $C_F$  are first selected so that VCO output frequency lies in the center of the operating frequency band.

Now the modulating S/p voltage is usually varied from  $0.75 V_{cc}$  to  $V_{cc}$  which can produce a freq variation of about 10 to 1.

With no modulating S/p signal, if the voltage at pin 5 is biased at  $(7/8) V_{cc}$

So from eq ③

$$f_0 = \frac{2 \left[ V_{cc} - (7/8) V_{cc} \right]}{C_T R_T V_{cc}}$$

$$f_0 = \frac{1}{4 R_T C_T} = \frac{0.25}{R_T C_T} \quad \rightarrow ④$$

Voltage to Frequency Conversion Factor

A parameter of importance for VCO is voltage to frequency conversion factor  $k_V$  and is defined as

$$k_V = \frac{\Delta f_0}{\Delta V_c}$$

Here  $\Delta V_c$  is the modulation voltage required to produce the freq shift  $\Delta f_0$ , for a VCO. If we assume that the original freq is  $f_0$  and the new

in  $f_1$  then.

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$$\Delta f_0 = f_1 - f_0$$

$$= \frac{2(V_{ce} - V_c + \Delta V_c)}{C_T R_T V_{ce}} - \frac{2(V_{ce} - V_c)}{C_T R_T V_{ce}}$$

$$= \frac{2 \Delta V_c}{C_T R_T V_{ce}}$$

$$\Delta V_c = \frac{\Delta f_0 \cdot C_T R_T V_{ce}}{2}$$

putting the value of  $C_T R_T$  from eq(4)

$$f_0 = \frac{1}{4 C_T R_T}$$

$$\Delta V_c = \frac{\Delta f_0 \cdot V_{ce}}{8 f_0}$$

$$K_V = \frac{\Delta f_0}{\Delta V_c} = \frac{8 f_0}{V_{ce}}$$

$$K_V = \frac{8 f_0}{V_{ce}}$$

# Phase - locked Loops.

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## Introduction :-

The phase-locked loop (PLL) is an important building block of linear systems. Electronic phase-locked (PLL) came into vogue in the 1930s when it was used for radar synchronisation and communication applications. The high cost of realizing PLL in discrete form due to its use earlier. Now with the advances in IC technology, PLLs are available as inexpensive monolithic ICs.

This technique for electronic frequency control is used in satellite communication systems, air borne navigational systems, FM communication systems, computers etc.

## Basic principle :-

- ① Phase detector / comparator.
- ② A LPF.
- ③ An error amplifier.
- ④ A Voltage Controlled Oscillator (VCO).

- \* The VCO is a free running multivibrator and operates at a free frequency  $f_0$  called free running frequency.
- \* This freq<sub>y</sub> is determined by an external tuning capacitor and an external resistor.
- \* It can also be shifted to either side by applying a dc control voltage  $V_c$  to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a 'Voltage Controlled Oscillator' or VCO.
- \* If an input signal  $V_s$  of freq<sub>s</sub> is applied to the PLL, the phase detector compares the phase and freq<sub>y</sub> of the incoming signal to that of the output  $V_o$  of the VCO.
- \* If the two signals differ in freq<sub>y</sub> and/or phase, an error voltage  $V_e$  is generated. The phase detector is basically a multiplier and produces

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the sum ( $f_s + f_o$ ) and difference ( $f_s - f_o$ ) components at its outputs. The high freq component ( $f_s + f_o$ ) is removed by the LPF and the difference frequency component is amplified and then applied as control voltage  $V_c$  to VCO.

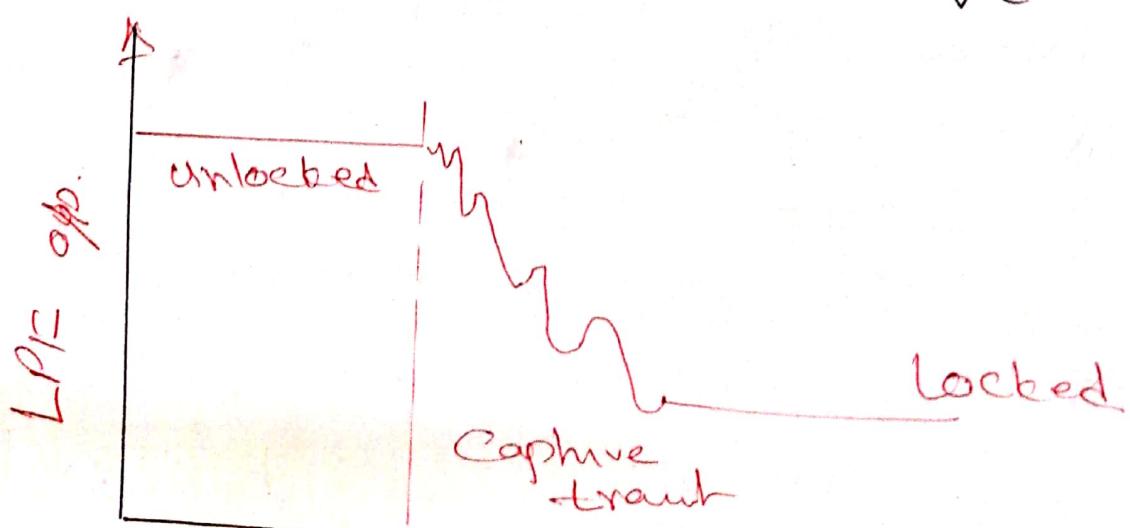
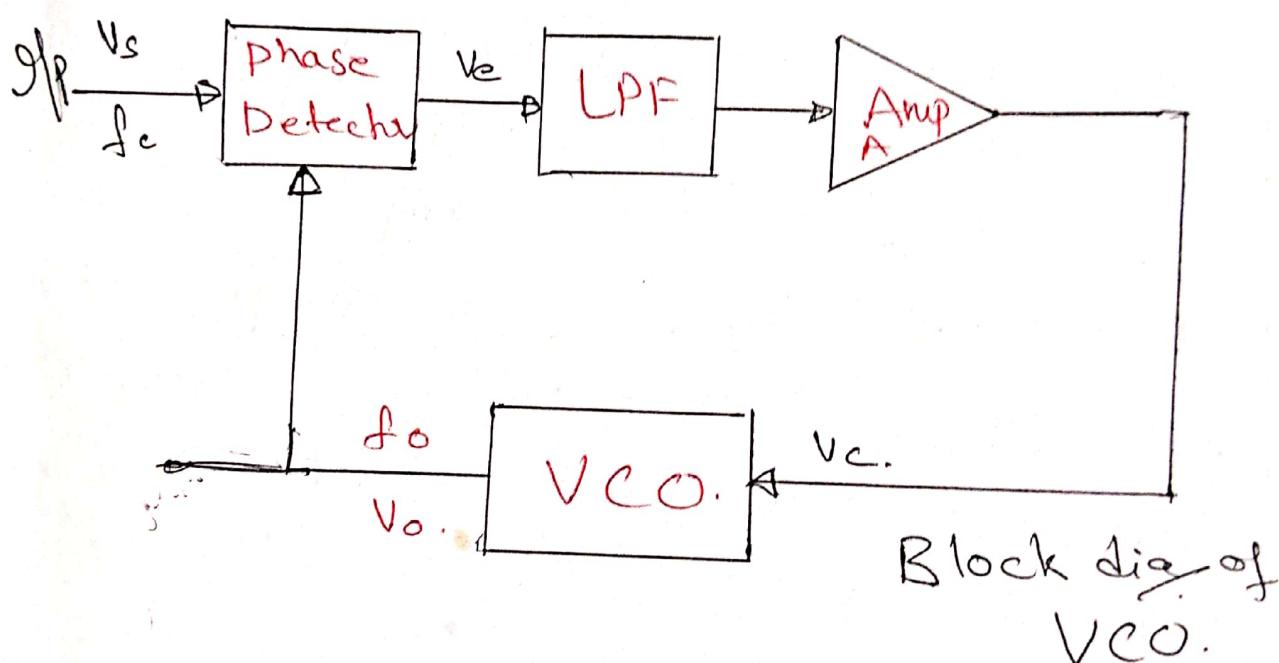
The signal  $V_c$  shifts the VCO freq. in a direction to reduce the freq. difference between  $f_s$  and  $f_o$ . Once this action starts, the signal is in the capture range.

The VCO continues to change freq. till its output freq. is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency  $f_o$  of VCO is identical to  $f_s$  except for a finite phase difference  $\phi$ . This phase difference generates a corrective control voltage  $V_c$  to shift the VCO frequency from  $f_o$  to

fs. and thereby maintain the lock.  
once locked, PLL tracks the freq  
changes of the input signal.

Thus PLL goes through three stages.

- (i) Free running
- (ii) Capture
- (iii) Locked or tracking.



Rq: The capture transient. Start f in  $\omega_0$

Fig shows the capture transient.

- \* As capture starts, a small sine wave appears. This is due to the difference frequency between the VCO and the input signal. The dc component of the beat drives the VCO towards lock.
- \* Each successive cycle causes the VCO frequency to move closer to the input signal frequency.
- \* The difference in frequency becomes smaller and a larger dc component is passed by the filter, shifting the VCO frequency further.
- \* The process continues until the VCO locks on to the signal and the difference freq is dc.
- \* The LPF controls the capture range. If VCO freq is far away the beat freq will be too high to pass through the filter and the PLL will not respond. We say the the signal is out of the capture band. However once locked, the filter no longer

restricts the PLL. The VCO can track the signal well beyond the capture band.

Thus tracking range is always larger than the capture range.

### Lock-in Range

Once the PLL is locked, it can track freq changes in the incoming signals. The range of freq over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range.

The lock range is usually expressed as a percentage of  $f_0$ , the VCO freq.

The lock range  $f_L$  is given by

$$f_L = \pm \frac{8f_0}{V} \text{ Hz}$$

Capture Range - The range of freqs over which the PLL can acquire lock with an s/p signal is called the capture range. This parameter is also expressed as

$$f_c = \pm \left[ \frac{f_L}{(k_1)(3.6)(10^3)(C_2)} \right]^{1/2} \quad (15)$$

pull-in time

The total time taken by the PLL to establish lock is called pull in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

### Phase detector / Comparator

The phase detector is the most important part of the PLL system. There are two types of phase detectors used. Analog and digital.

The phase detector compares the input frequency and the VCO frequency and generates a dc voltage that is proportional to the phase diff between the two frequencies. Depending on whether the analog or digital phase detector is used the PLL is called

either an analog or digital type 14

A double-balanced mixer is an example of an analog phase detector.

The examples of digital phase detector are

1. Exclusive-OR phase detector
  2. Edge-triggered phase detector.
  3. Monolithic phase detector (4049)
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Exclusive-OR phase detector uses an

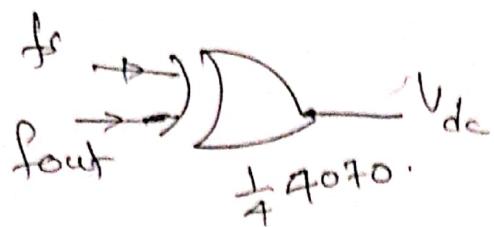
ex-OR gate such as CMOS type 4070.

The output of X-OR gate is high only when  $f_s$  or  $f_o$  is high.

In this fig.,  $f_s$  is leading  $f_o$  by  $\phi'$  degree. i.e. the phase difference between  $f_s$  and  $f_o$  is  $\phi$  degrees.

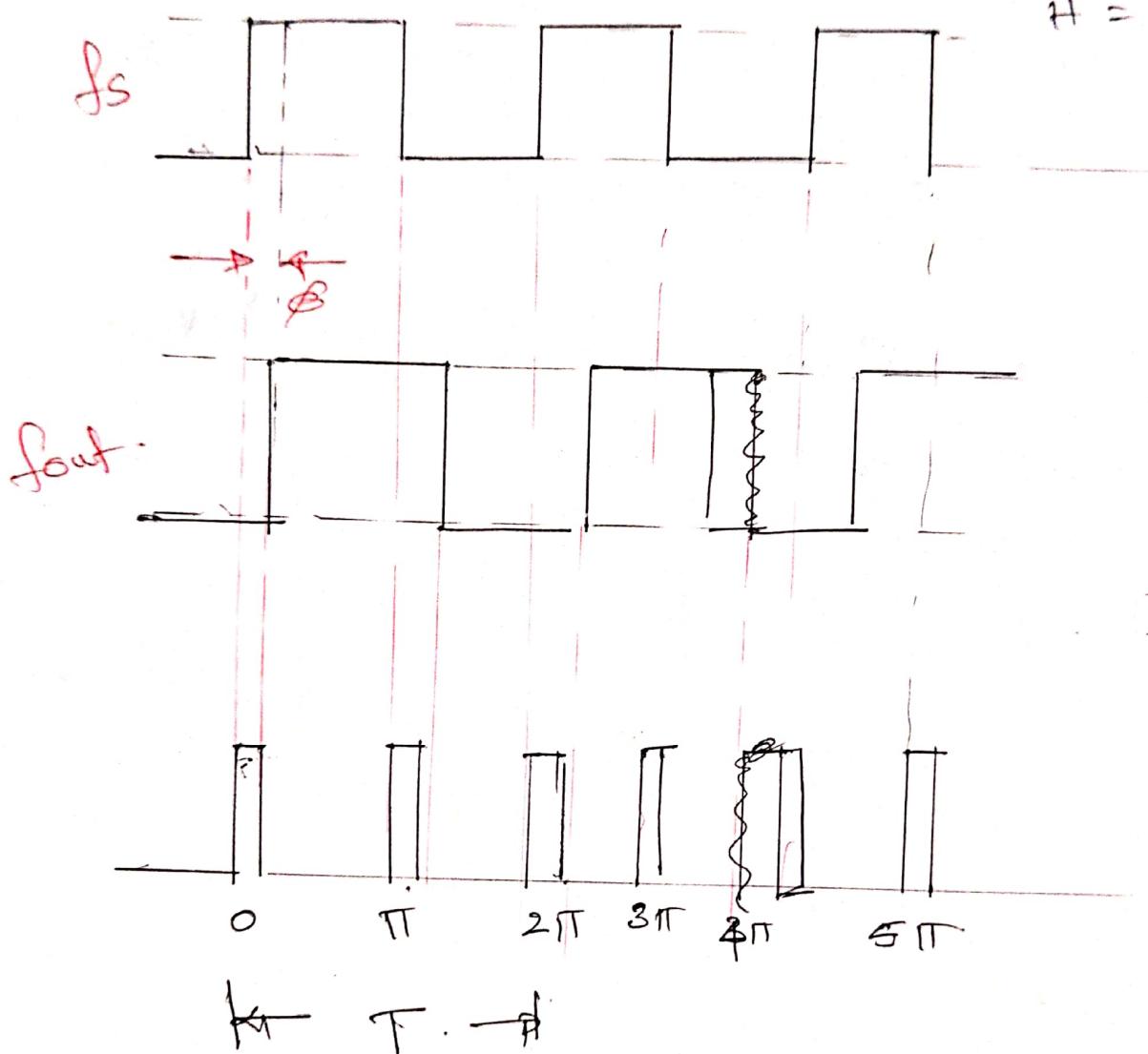
The dc o/p voltage of the ex-OR phase detector is a function of the phase difference between its two inputs.

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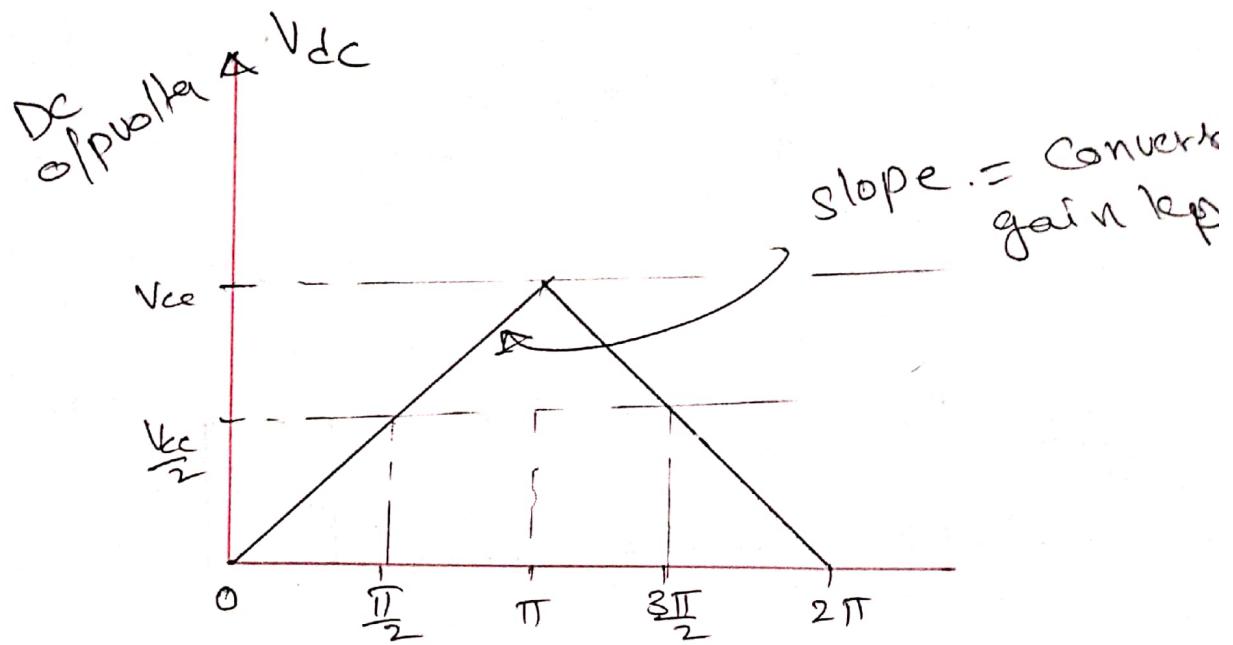


Inputs		o/p
A	B.	Y
L	L	L
L	H	H
H	L	H
H	H	L

L = Low  
H = High.



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phase difference ( $\phi$ ) between  
 $f_H$  and  $f_{out}$