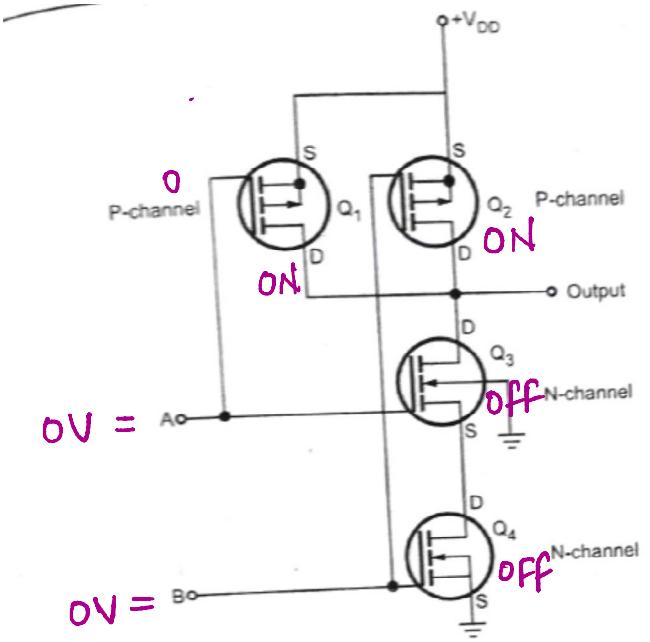
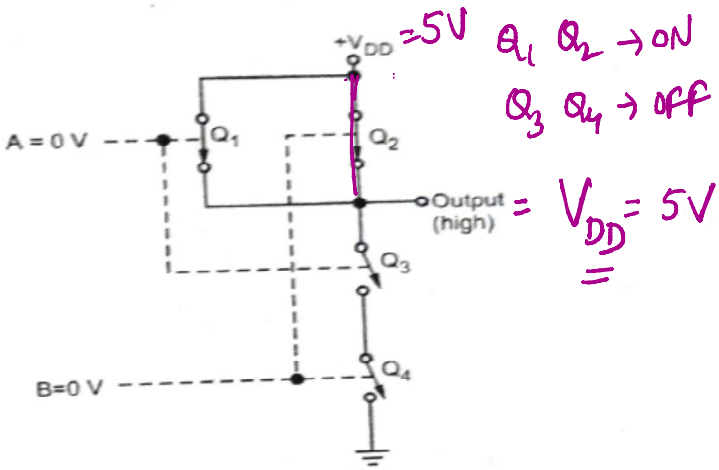
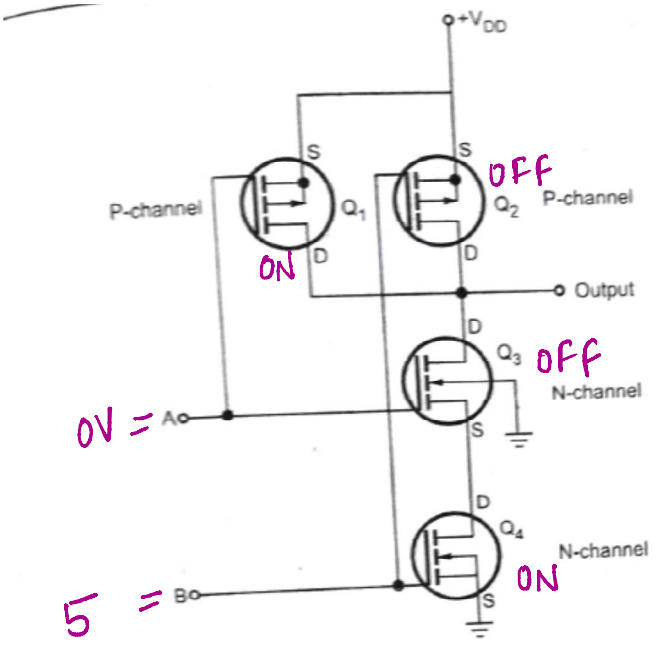
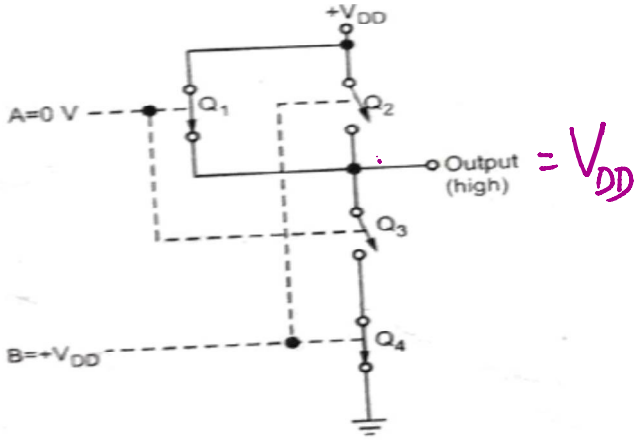
CMOS NAND GATE



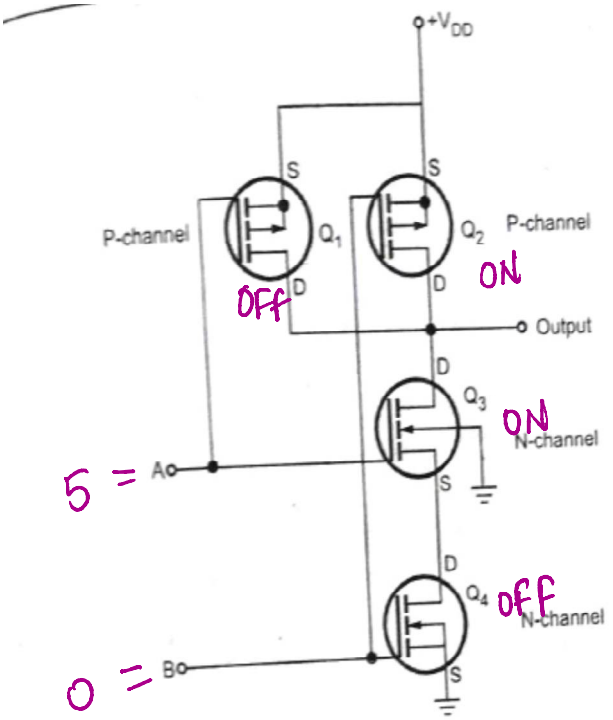


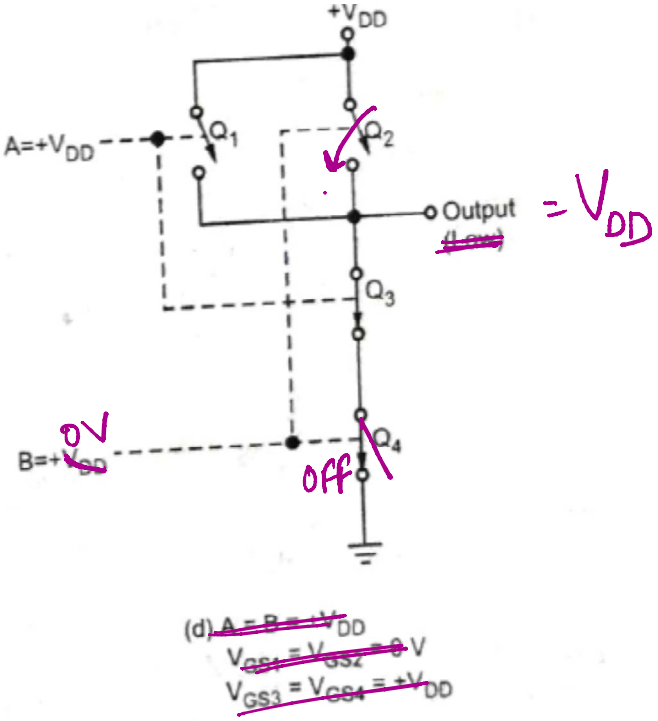
(b) A = B = 0V
$V_{GS1} = V_{GS2} = -V_{DD}$
$V_{GS3} = V_{GS4} = 0\ V$



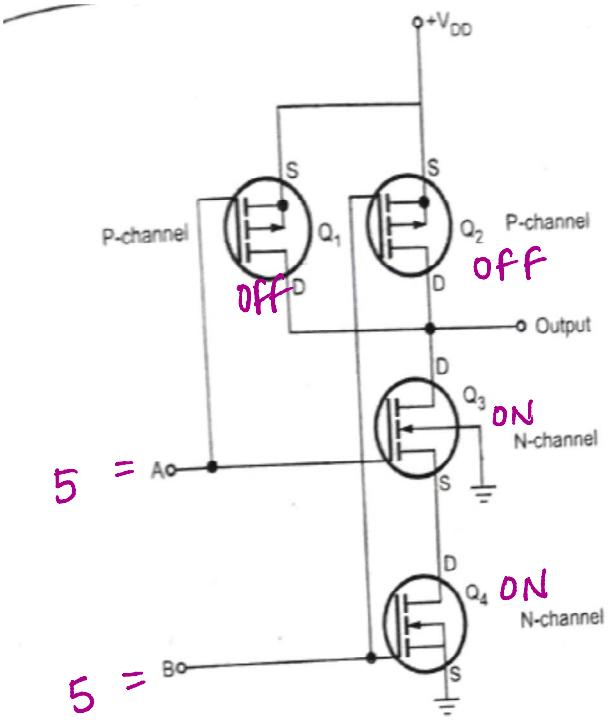


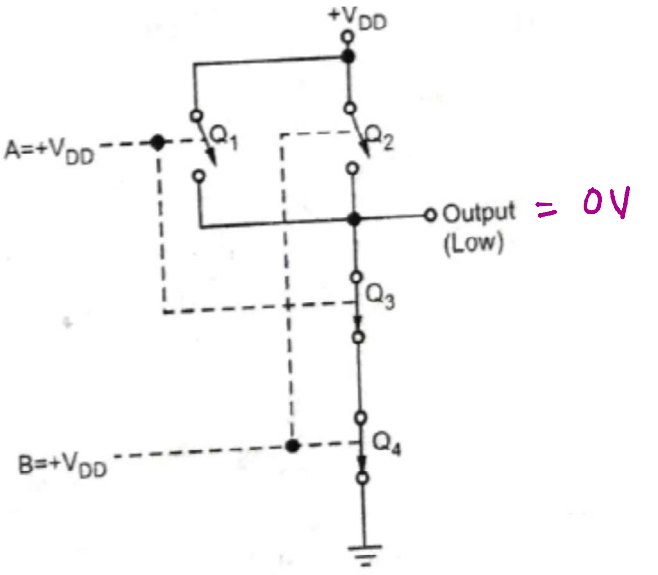
(c) A = 0V, B = $+V_{DD}$
$V_{GS1} = -V_{DD}$
$V_{GS2} = V_{GS3} = 0\ V$
$V_{GS4} = +V_{DD}$





(d) ~~A = B = +V_DD~~
~~V_GS1 = V_GS2 = 0 V~~
~~V_GS3 = V_GS4 = +V_DD~~





(d) A = B = $+V_{DD}$
$V_{GS1} = V_{GS2} = 0$ V
$V_{GS3} = V_{GS4} = +V_{DD}$

A	B	output
0	0	$V_{DD} = 5V$
0	5	V_{DD}
5	0	V_{DD}
5	5	0

$\cong$ NAND

CMOS NAND $\longrightarrow$ PMOS $\rightarrow$ parallel

NMOS $\rightarrow$ series

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

Table 7.14 Truth table of NAND gate