Timing Considerations

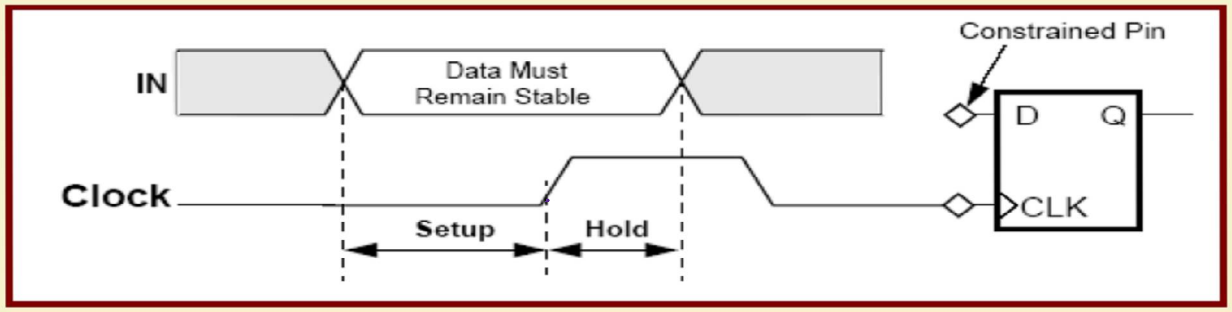
Timing Issues

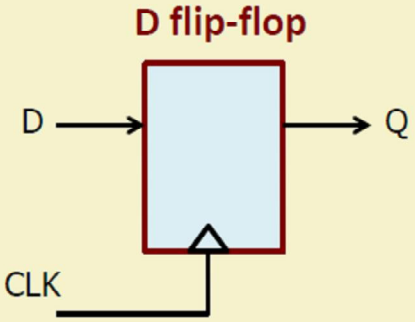
- For correct operation of a synchronous sequential circuit, several timing issues need to be considered.
  - Some of these issues relate to the properties of flip-flops.
  - Some of these issues relate to circuits external to the flip-flops.
- All these taken together determines the maximum speed with which the circuit can operate.
  - Typically specified in terms of the clock frequency.

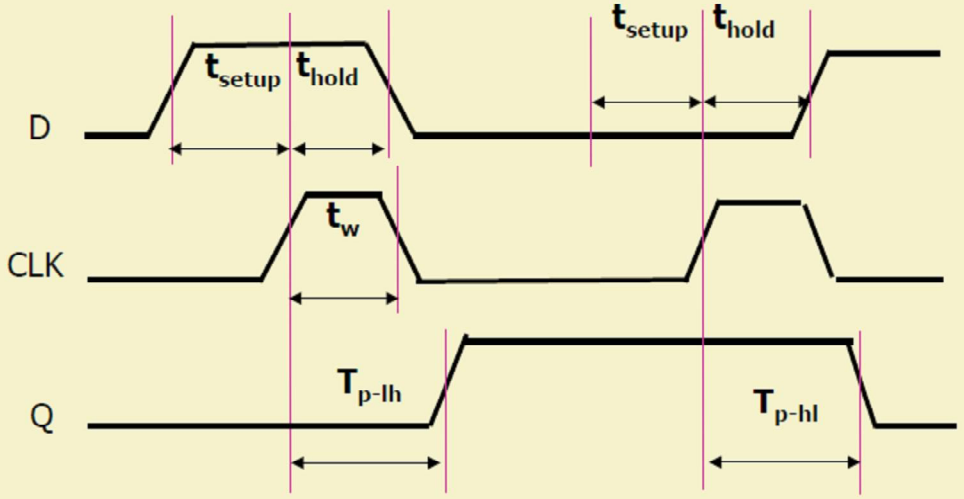
Some Definitions

- *Clock width (t_w)*: Minimum time duration for which the clock signal needs to be high in order that the flip-flops it feeds work properly.
- *Setup time (t_{setup})*: Amount of time the input to a flip-flop must be stable *before* the clock transitions high (for positive-edge triggered), or transitions low (for negative-edge triggered).
- *Hold time (t_{hold})*: Amount of time the input to a flip-flop must be stable *after* the clock transitions high (for positive-edge triggered), or transitions low (for negative-edge triggered).

- *Propagation delays ($t_{p\text{-}lh}$ and $t_{p\text{-}hl}$)*: Delay between clocking event (low-to-high or high-to-low transition) and change in the output.

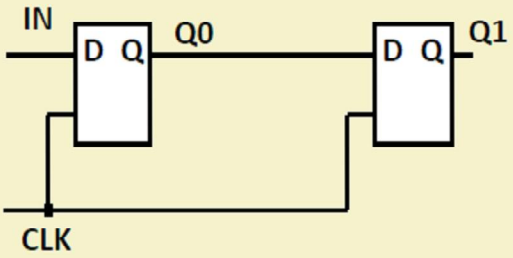


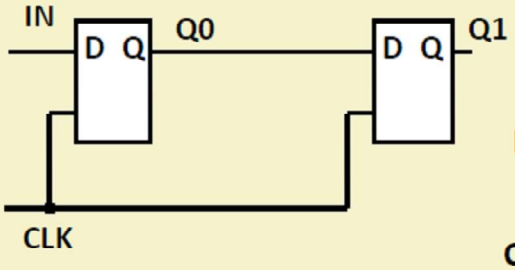




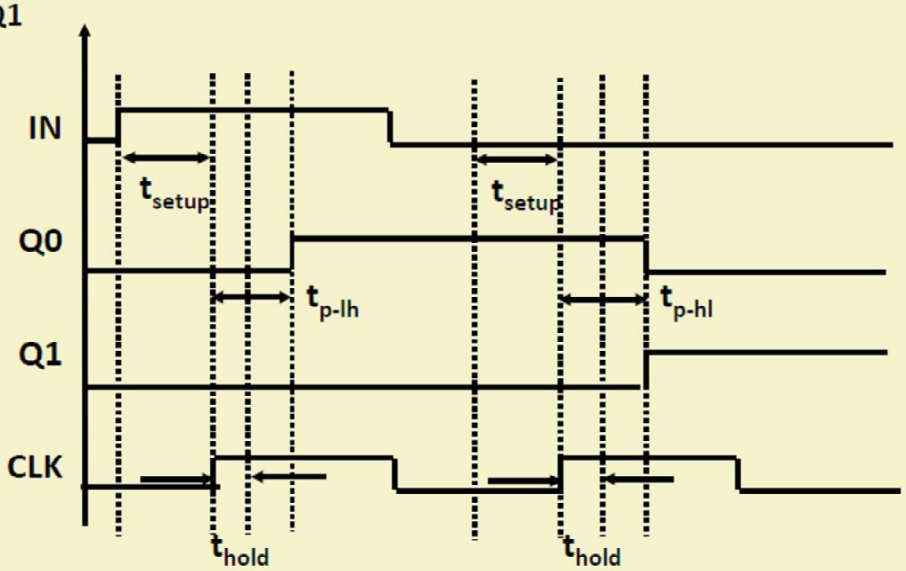
Cascading Flip-flops

- Suppose that the flip-flop propagation delay exceeds the hold time.
- Second stage can commit its input before Q0 changes.





The correct scenario



Edge-triggered Clocking

- Edge-triggered operation (either positive or negative edge triggered)
  - Data leaving at time *t* must arrive at the next flip-flop *one setup time before t+T*, where *T* is the clock period.
- Clocking relationships are relatively simple:
  - Delay from each input flip-flop to each output flip-flop of a combinational block should be less that ($T - t_{setup}$).
- Ideally, the clock signal should arrive *all* flip-flops at *exactly* the same time.
  - In practice, clock skew exists.

Example 1

- Given a clock signal of frequency *f Hz*, how to generate another clock of frequency *f/2 Hz*.
  - Frequency division.

Example 2

- Given a clock signal of frequency *f Hz*, how to generate another clock of frequency $f/2^k$ *Hz*, for some integer *k*.
  - Frequency division by some power of 2.