Normally $L > x_{ds} + x_{dD}$ to avoid Edge Effect in mos ϵ^{γ}

MGIT

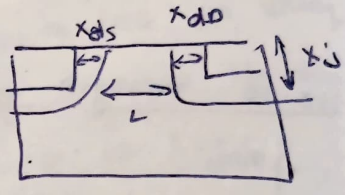
Short Channel transistor :- MOSFET is Considered to be Short, when the Channel length L is in the same order of mag of the depletion layer width of Source & drain

$L = x_{ds}$ & x_{dD}

↓ Channel length — depletion layer width of S & D.

$L_{eff} = L - \Delta L = x_j$ (↓ jus depth)

⇒ When the Channel length is $<< 1\mu m$, SCE becomes dominant leading to undesirable Effect in MOSFET.



⇒ With Short Channel, faster CKT, drive ↑, High ~~gate~~ I

Cap reduced, ↑ Operating Speed possible

Short Channel Effect

1. Velocity Saturation
2. Mobility degradation
3. Channel length modulation
4. punch through Effect
5. DIBL Effect
6. Hot Electron Effect.

due to Short channel Effect a lots of operating charg ϵ^{s} varies

→ 2 E.f in mosfet

$E_{lat} = V_{ds}/L$; ϵ_{γ}

$E_{vert} = V_{gs}/t_{ox}$; ϵ_y

(1) **Velocity Saturation Effect :-** As device dimensions L_G, gate oxide thickness, Entire physical dimensions of device are Scaled down. So supply V is also Scale.

In Long channel, gate V produced vertical Ef (E_y)

Lateral E.f " due to V_{ds} (E_x) ✓ plays a Crucial role

MGIT

$V_{DS}\uparrow\uparrow$, $E_x\uparrow\uparrow$ V_d ⇒ drift velocity of Carrier

Linear region $V_{DS} > 0$

$V_{DS} < (V_{GS} - V_t)$

↳ Drain Saturation voltage

⇒ $V_{DS}\uparrow$, $E_x\uparrow$, V_d across the Channel $\uparrow$, $\downarrow$ Current density $\uparrow$, $I_D\uparrow$

(μ Const) $V_d = \mu \cdot E$ [Drift velocity] V_d of Carrier $\uparrow$

$J = n q \mu_n E$

$I = J \cdot A$ ↳ (Cross Sectional Area of mos ϵ^r]

I_D & V_{DS}

⇒ E.f is produced. when we apply small amount of drain to Source voltage [$V_{DS} < (V_{GS} - V_t)$]

⇒ mobility is Const for Smaller value of E.f ($v_d \propto E$)

⇒ Large V_{DS}, Large E.f (Lateral E.f Stronger) at drain, μ is not Const

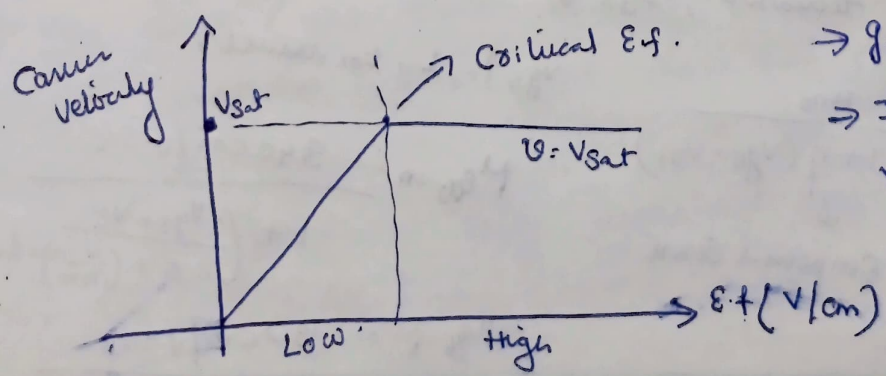
μ is decreases $\mu \propto \frac{1}{E}$ (mobility of e^- decreases), v_d Const

$v_d = \mu E$ ↳ large, so drift velocity Const. No Linear relationship

Small (v_D Const)

Imp ⇒ Above Critical E.f, Carriers tends to loose drift velocity. Stabilise E.f, so ultimately they can't move faster Imp towards Speed

⇒ V_{GS} is main Controlling Element for the movement of Charge Carrier, but $\downarrow$ V_d, μ are Controlled by Large applied V_{DS} in above case



⇒ g_m of device reduces

⇒ I_D is limited by velocity Sat. instead of pinch off.

⇒ I_D is limited by velocity Sat. instead of pinch-off. This occurs

MGIT This occurs in short channel devices when the dimensions are scaled c/o lowering the bias voltage

→ Carriers travelling along the channel in the existence of high lateral E.f.

→ Above a critical E.f, the carriers tend to lose its drift velocity & stabilise their speed & ultimately can't move faster

→ The value of critical E.f is set by the choice of materials used in the channel.

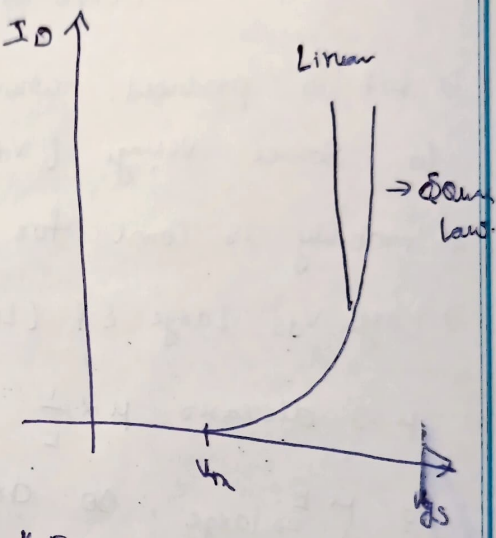
$$v_d = \frac{\mu \cdot E_{lat}}{1 + \frac{E_{lat}}{L \cdot E_C}}$$

$$I_{D_{sat}} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) \frac{(V_{gs} - V_{tn})^2}{1 + \left(\frac{V_{gs} - V_{tn}}{L \cdot E_C}\right)}$$

If $L \uparrow$, $\frac{V_{gs} - V_{tn}}{L \cdot E_C}$ term neglected

If $L \downarrow$, $I_{D_{sat}} = \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{gs} - V_{tn}) E_C$

$$I_{D_{sat}} = \mu_n C_{ox} (W) (E_C) (V_{gs} - V_{tn})$$



(8) Mobility degradation :- $E_{ver} \uparrow = \frac{V_{gs} \uparrow}{t_{ox}}$; $V_{gs} \uparrow$, more e^- are move towards channel, so collision occur among the channel & all e^- move towards surface of sub. So mobility decreases, $I_{ds} \downarrow$

$$\mu_n = \frac{\mu_{no}}{1 + \eta (V_{gs} - V_{tn})}$$

↓ Empirical Const

$V_{gs} \uparrow$, L, t_{ox} reduces

$$\mu_{eff-n} = \frac{540\ cm^2/V\text{-}sec}{1 + \left(\frac{V_{gs} + V_t}{0.54 \left(\frac{V}{nm}\right) \cdot t_{ox}}\right)}$$

$$\mu_{eff-p} = \frac{180\ cm^2/V\text{-}sec}{1 + \left(\frac{V_{gs} + 1.5 V_t}{0.338 / \cdot t_{ox}}\right)}$$

(5)

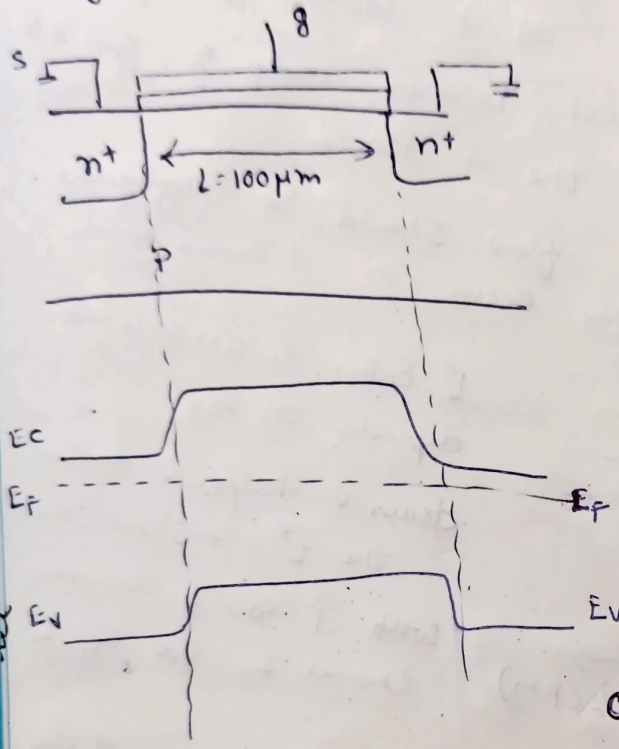
DIBL Effect

In Long Channel The current is Controlled by V_{GS}

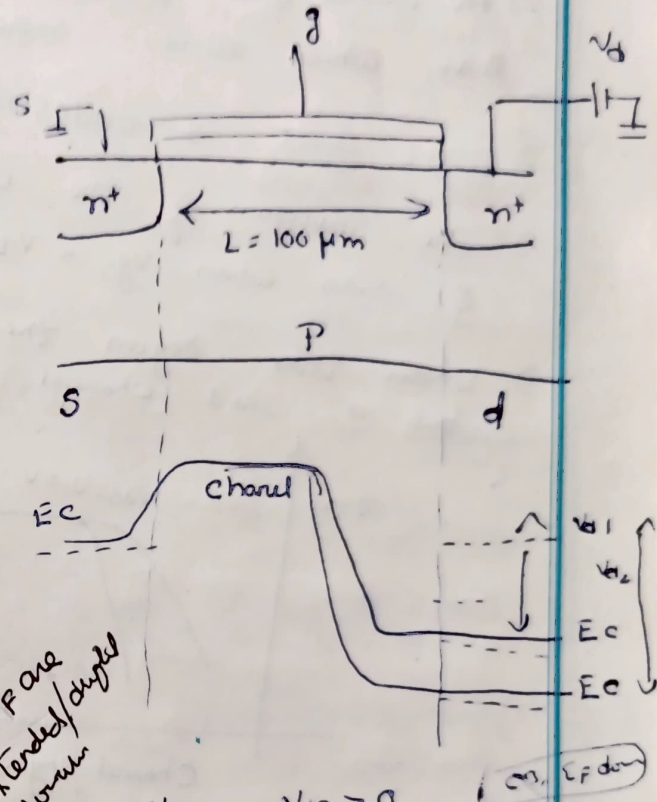
In Short " " " by V_{GS} & V_{DS} &

e^- are Easily penetrate into the Channel

Long Channel b^y



$V_S = 0, \; V_d = 0$



$V_S = 0, \; V_{DS} > 0$

Drain does not influence Source of Barrier

⇒ When V_{DS} is applied at drain side, $V_{GS} > V_{Th}$, Conduction Band at drain side is starts to decrease ↑ of C.B, D.R Extends downwards, C.B at drain side, Extended downwards, E_F are also drifting down (more Band Bending), Barrier at Source no change ~~irrespective~~, Barrier at drain side ↑ bcoz S & D are largely separated

⇒ Barrier at Source is only modulated/Controlled/Effected at gate side. In long Channel

V_{th} is indep of V_{ds} ⇒ In long channel

Short Channel :- As Channel is Short, Bain & Source Side is also Effected by drain. So drain influence Source of Barrier

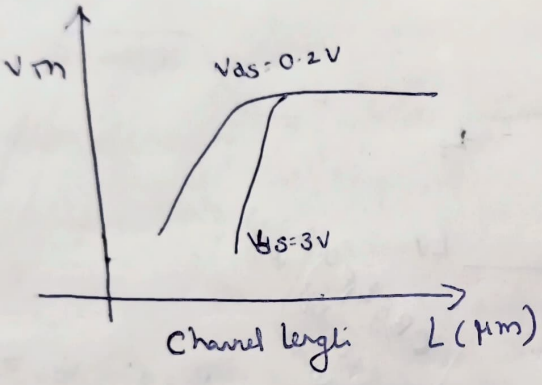
⇒ Barrier at Source is modulated / Controlled by drain Bias

⇒ At Source Side potential Barrier is reduced due to Drain Bias, which allows more e^- to flow from S to Drain

⇒ DIBL Effect is undesirable, as it lowers V_{th} of device

⇒ The inversion of the Channel becomes indep of gate voltage even when $V_{gs} < V_{th}$, the I flows.

⇒ Under this region the I flow should be negligible but in Short Channel, this occur in a Reverse manner



t^r Enters in ON State w/o depends on V_{ds}.

drain V helps to Conduct the t^r. ⇒ Short Channel with ↑ V_{ds} & decreasing Channel L, we try to ~~ON~~ Operate the t^r.

ΔV_{ds}, with immediate ΔV_{th} to so t^r ON State

$$DIBL = \frac{V_{th}}{V_{ds}}$$

Short channel

- ① It leads mosfet has good processing speed
- ② Require low operating potential
- ③ ↑ t^r density on a chip

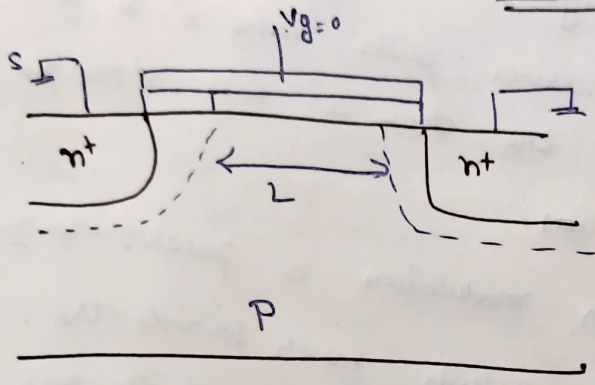
- DIBL
- Surface Scattering
- Velocity Saturation
- Impact ionization
- HEE

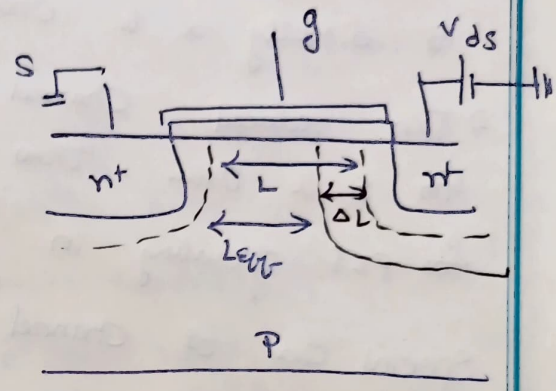
The potential Barrier at Source is now reduced due to drain Bias, which allows more e^- to flow from S to Drain

⇒ Through at Shorter gate length, the inversion of channel starts Earlier.

(3)

Channel Length Modulation (CLM)





When $V_{ds} \uparrow$, $\Delta L \uparrow$

$\Delta L \propto V_{ds} \Rightarrow \Delta L = \lambda' V_{ds}$

$L_{eff} = L - \Delta L$

$\Rightarrow \frac{\Delta L}{L} = \frac{\lambda'}{L} \cdot V_{ds} \Rightarrow \lambda \cdot V_{ds}$

Drain Resistance $\downarrow R = \frac{\rho L}{A} \downarrow$

$I_{ds,n} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{gs} - V_{tn})^2 \left(1 + \frac{\Delta L}{L}\right)$

$$I'_{ds} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{gs} - V_{tn})^2 [1 + \lambda V_{ds}]$$

$$I'_{ds} = I_{ds} (1 + \lambda V_{ds})$$

I'_{ds} ↓ With CLM

I_{ds} ↓ w/o CLM

$$r_d = \frac{\partial V_{ds}}{\partial I'_{ds}} \Rightarrow \frac{1}{r_d} = \frac{\partial I'_{ds}}{\partial V_{ds}}$$

$$\frac{1}{r_d} \Rightarrow \lambda \cdot I_{ds} \Rightarrow r_d = \frac{1}{\lambda \cdot I_{ds}} = \frac{1}{\lambda \left[\frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) (V_{gs} - V_{tn})^2\right]}$$

CLM & punch through Effect

illustrate Similar issue of DIBL related to Shortening of length of Channel region with an increase in drain Bias is known as CLM.

The Inversion region Expands towards Source. with ↑ in drain bias.

⇒ Shortening the channel Length ↓ the channel Resistance is directly ∝ to Channel Length.

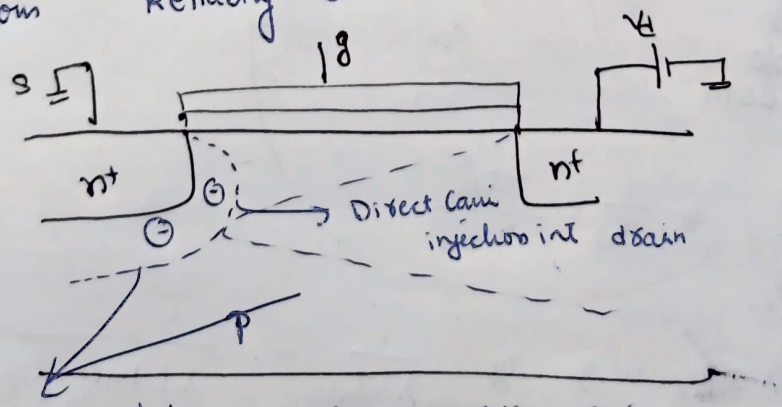
⇒ This reduced Channel Resistance pulls more e^- to flow from S to Drain. thus ↑ing the drain I with drain bias for FET operating in Saturation.

Special Case of Channel length modulation is punch through Effect

⇒ When V_{DS} is High, Drain D.R Extends much towards the Source side Causing a greater number of e^- to directly reach drain Effortlessly.

⇒ The I_D is ↑sed irrespective of V_{GS}. This Effect is undesirable as gate has no Control over the channel & e^- Starts to move Even at the Sub Vth. region.

& this Current would be a sub Th. leakage I Causing Serious Reliability issue.



6

Impact Ionization :- As gate length is reduced, E.f at drain in saturation ↑s.o. keeping fixed drain voltage

$$E_{lat} = \frac{V_{ds}}{L}, \quad E_{ver} = \frac{V_{gs}}{t_{ox}}$$

$$E_{lat} = \frac{V_{ds}}{L'} = \frac{V_{ds}}{\frac{L}{S}} = \frac{S V_{ds}}{L}$$

⇒ As L is scaled down, V_{ds} ↑, E_{lat} ↑, v_d ↑, e^- move with high velocity, so kinetic energy of this e or carriers ↑ drastically, so e^- become hot.

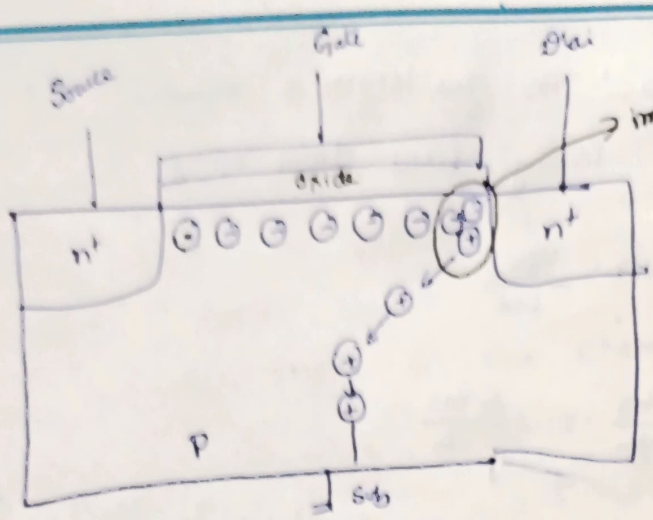
⇒ When V_{ds} ↑, E_{lat} ↑, so E.f ~~move towards the~~ at drain ↑ v_d ↑, kinetic energy ↑, As hot e are moving towards drain with very high energy, as E.f towards drain High, so we observe impact ionization.

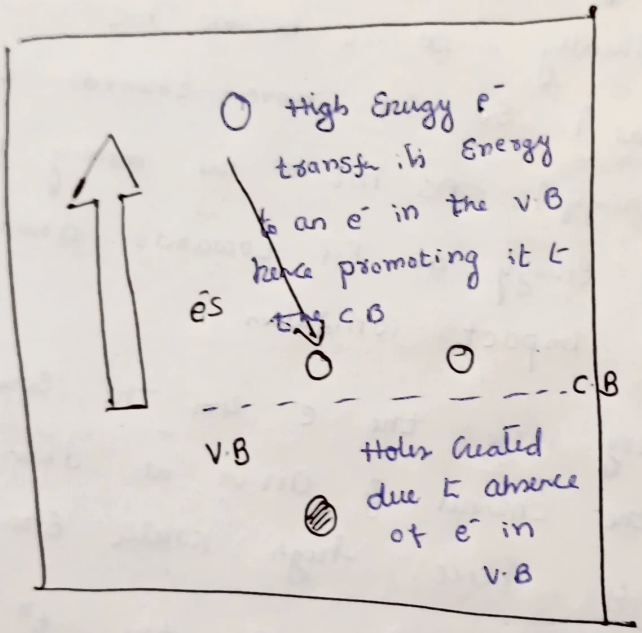
[When V_{ds} is very large, the e^- frm the source are accelerated in the channel & arrive at drain with high velocities & hence high kinetic energy]

⇒ These can cause "degradation of the t^x or instability

This phenomenon is called Hot Carrier Effect

⇒ [At Drain side, E.f is high, e^- are imparted Enough energy to become hot. These hot e^-'s impact the drain, dislodging holes that are there is swept toward the -vely charged substrate. Due to this there is a substrate I. [This Effect is known as impact ionization]





It is the process in a material by which one Energetic Charge Carrier can lose Energy by the creation of other.

⇒ In S.C, an e⁻ (hole) with Enough K.E can knock a bound e⁻ out of its Bound State (in V.B) & promote it to a State in C.B, creating an e⁻-hole pair