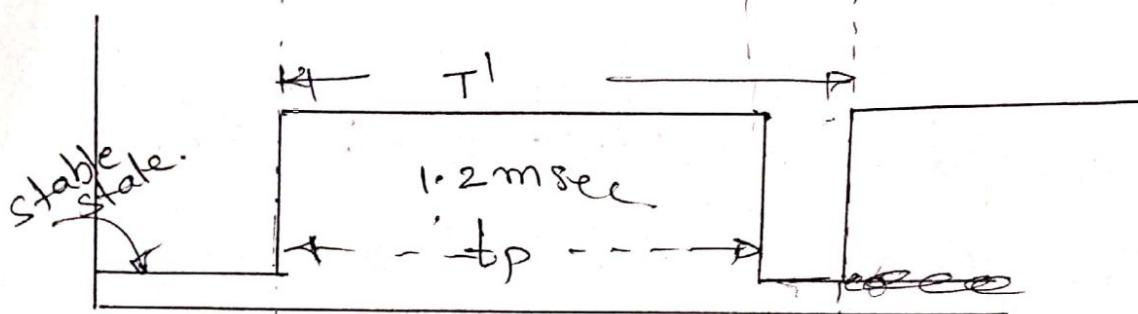
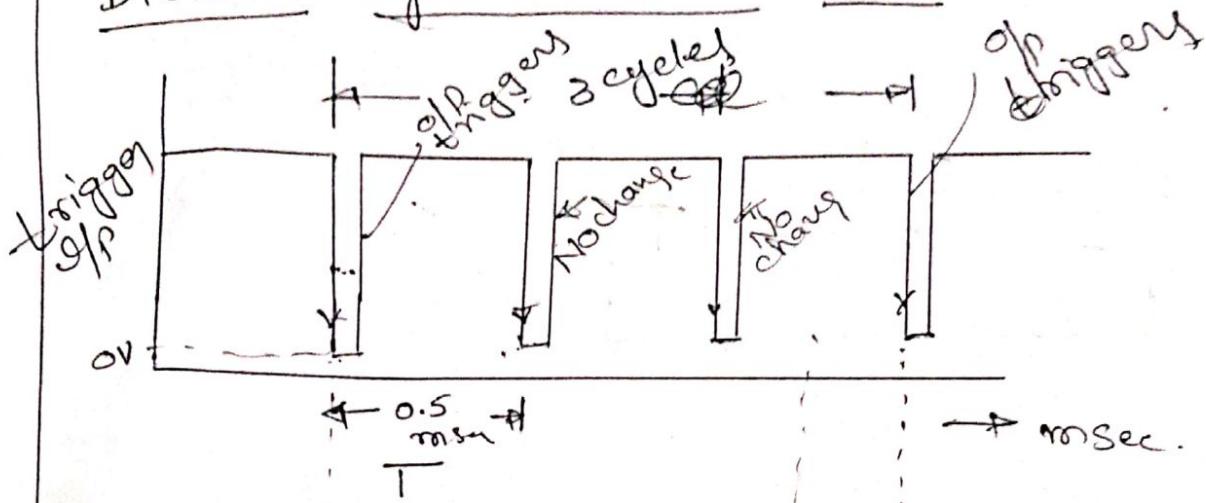


①

Divide - By - three circuit



$$\boxed{t_p > 2T}$$

Op Frequency is  
 ~~$f = 1.2 \text{ KHz} \cdot 2 \text{ KHz}$~~   
 $T = \cancel{0.5 \text{ msec}} (0.5 \text{ msec})$

choose  $t_p = (1.2)(2T)$ .  $= 0.967 \text{ msec}$   
 $\approx (1.2)(2)(\cancel{0.5})(10^{-3})$

$t_p = 1.2 \text{ msec}$

$T_1$  is the op wave form time period.

To design Now take  $t_p = 1.2 \text{ msec}$

choose  $C = 0.01 \mu F$

$$\boxed{t_p = 1.1RC}$$

cd R  $\therefore R = \frac{t_p}{1.1 \times C} = \frac{1.2 \times 10^{-3}}{1.1 \times 0.01 \times 10^{-6}}$   
 $\boxed{T_f = 109 \cancel{10^3} \text{ k}\Omega}$

(2)

So to design Divide by 'n'

circuit we have to choose, gear  
stable state time period

$$t_p > (n-1)T$$

(2)

The monostable multivibrator is used as a divide-by-3 network.

The frequency of the Ip trigger is 15 kHz. If the value of  $C = 0.01 \mu F$ . cal the value of resistance  $R$ .

$$t_p > 2T$$

$$f = 15 \text{ kHz}$$

$$T = \frac{66}{66} \text{ msec}$$

$$t_p = (1.2)(2)(66) \times 10^{-3}$$

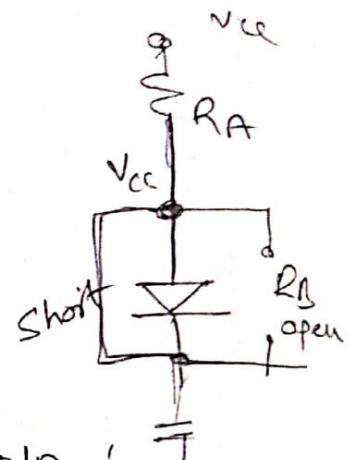
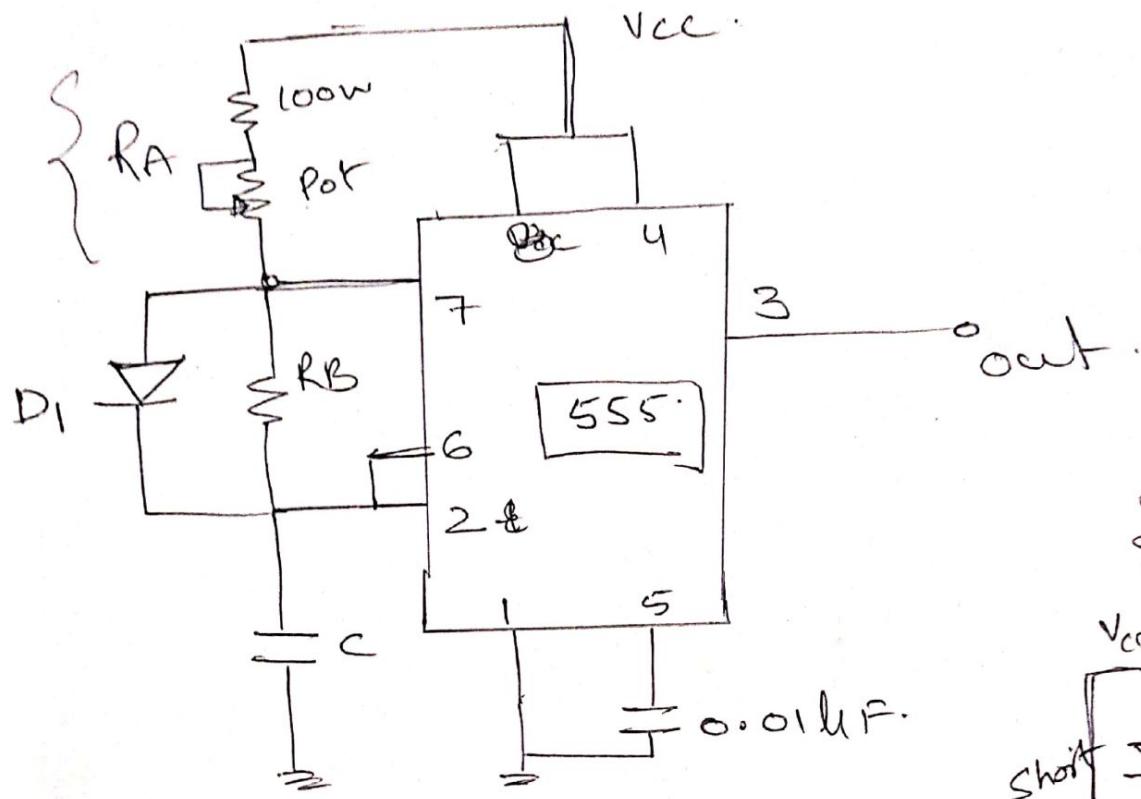
$$t_p = \underline{\hspace{2cm}}$$

$$t_p = 1.1 \times R \times C$$

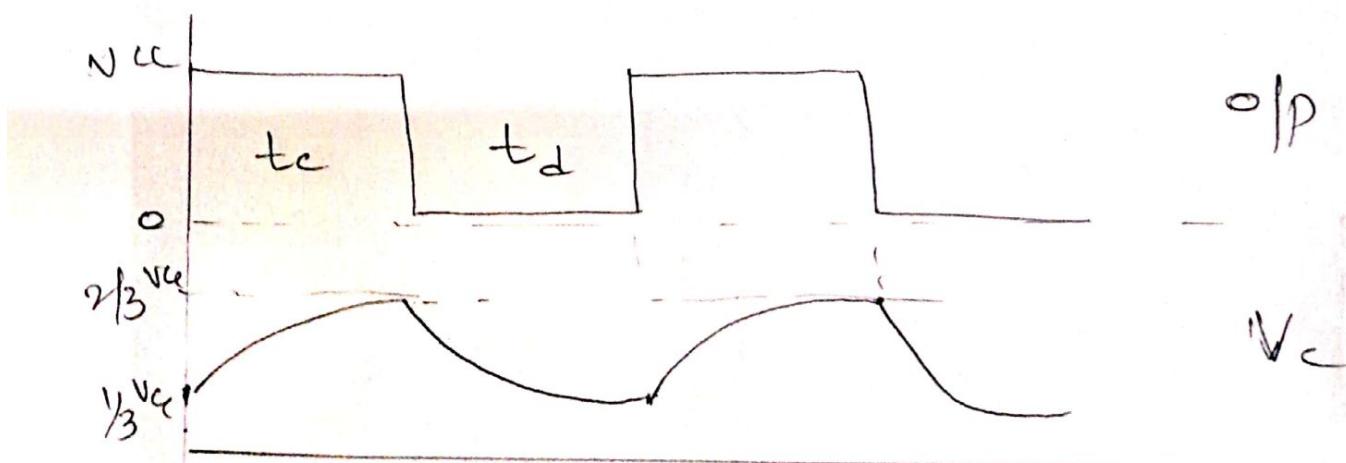
$$R = \frac{t_p}{1.1 \times 0.01 \mu F} = \underline{\hspace{2cm}}$$

(3)

## Square wave generator.



D	7 pin.	Q <sub>1</sub>	O/P
(short) ON.	$\approx V_{cc}$	OFF	1
(open) OFF	$\approx 0$	ON	0



$$t_c = 0.69 R_A C \quad (4)$$

$$t_d = 0.69 R_B C$$

$$T = t_c + t_d = 0.69 (R_A + R_B) C$$

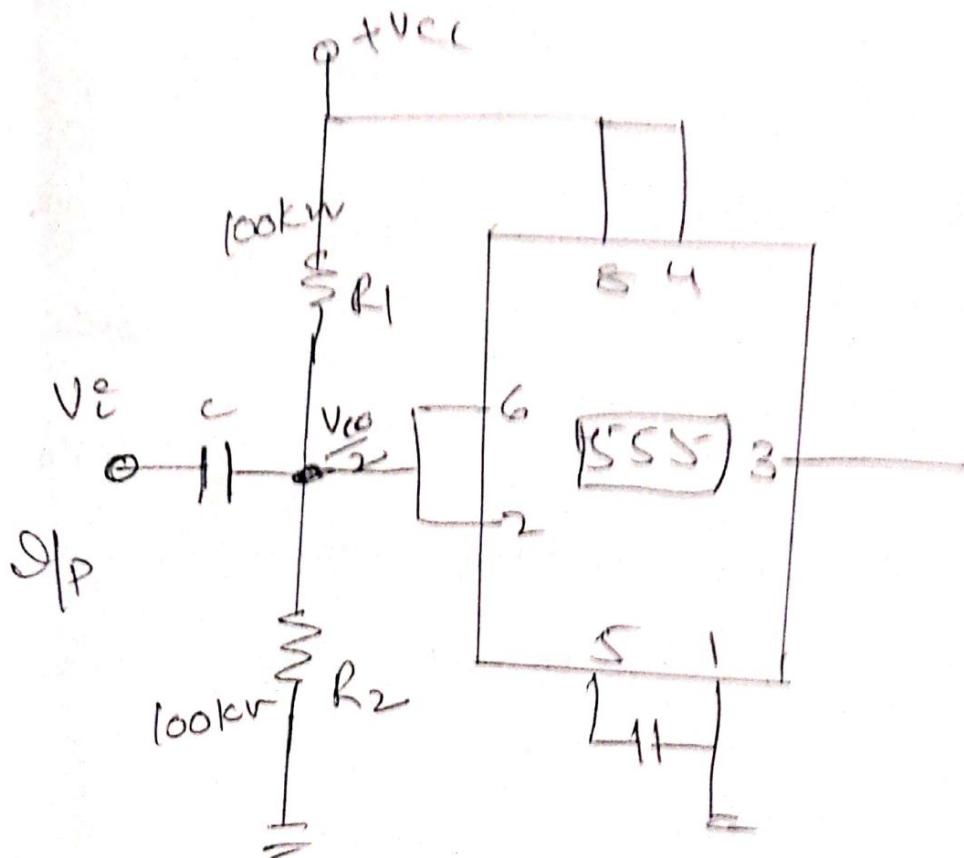
$$f = \frac{1.45}{(R_A + R_B) C}$$

$$\text{and duty cycle} = \frac{R_B}{R_A + R_B}$$

if  $R_A$  is made equal to  $R_B$

then 50% duty cycle is  
achieved.

## Schmitt trigger.



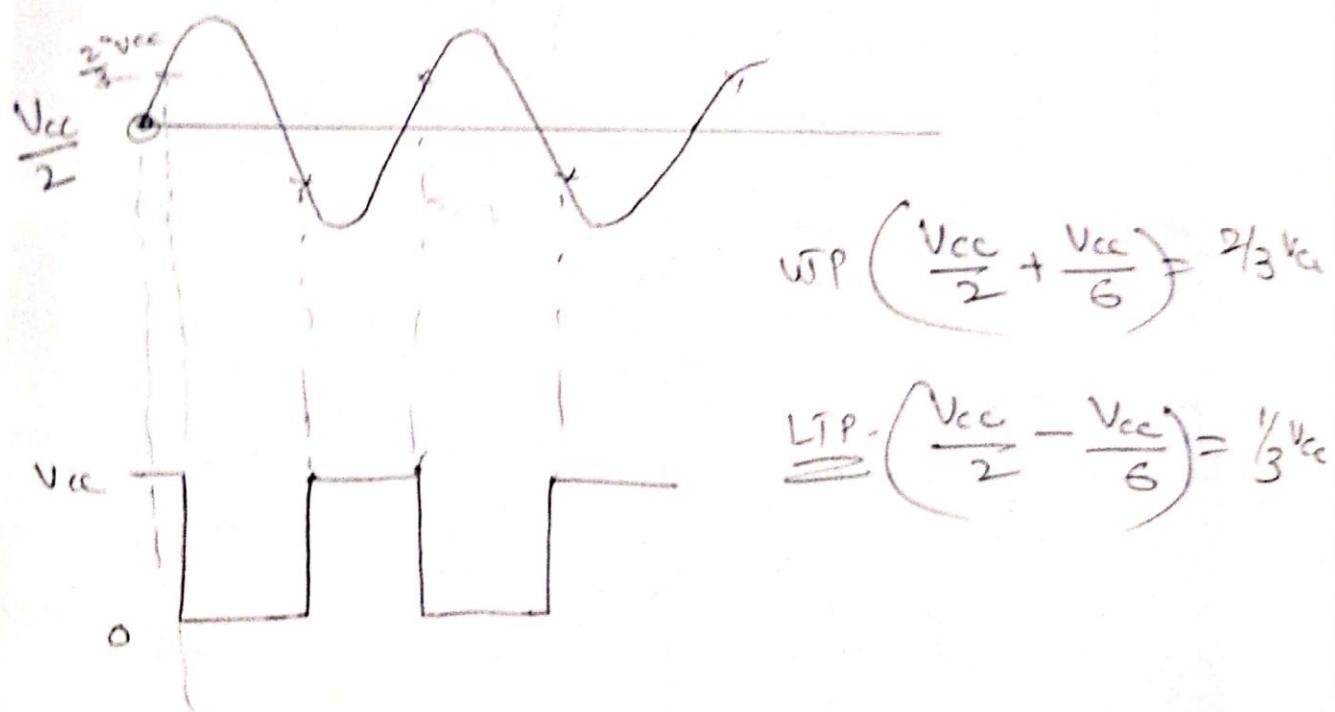
The two internal comparators are tied together and externally biased at  $\frac{V_{cc}}{2}$  through  $R_1$  and  $R_2$ .

Since the upper comparator will trip at  $(\frac{2}{3}) V_{cc}$  and lower comparator at  $(\frac{1}{3}) V_{cc}$  the bias provided by  $R_1$  and  $R_2$  is centered with in these two thresholds.

Thus a fine value of feedback voltage  
amplitude ( $> \frac{V_{cc}}{6} = \frac{2}{3}V_{cc} - \frac{V_{cc}}{2}$ )

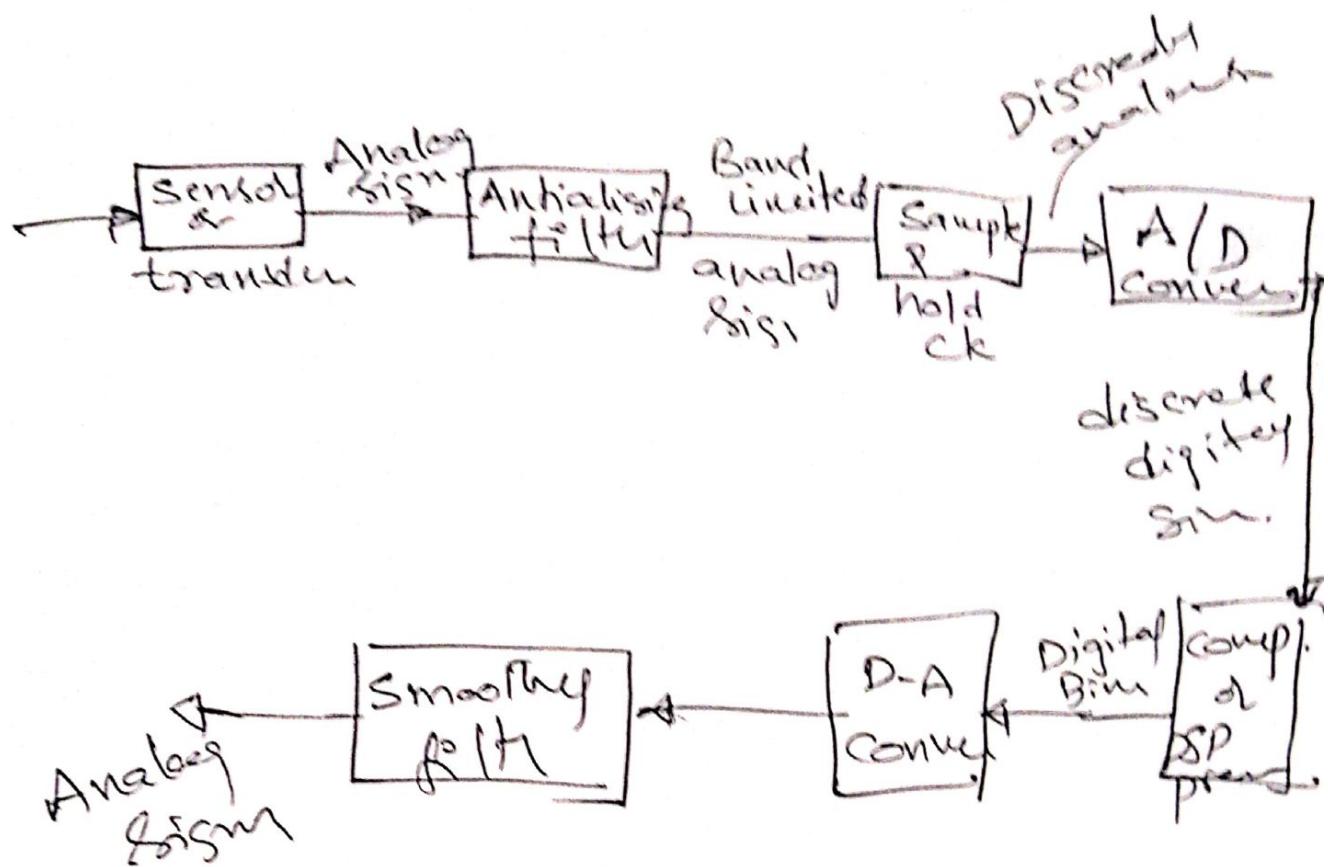
to exceed the ref level causes  
the internal op to alternately  
set and reset, providing a square  
wave o/p.

No freq division is taking place  
and freq of square wave remain  
the same as that of Ipp signal.



Ipp and o/p waveform of Schmitt trigger.

# D-A AND A-D converters.



Applications of A/D and D/A

Convert.

①

## Basic DAC Technique.

The schematic of DAC is shown in Fig. The input is an  $n$ -bit binary word  $D$  and is combined with a ref. voltage  $V_R$  to give an analog o/p signal. The o/p of a DAC can be either a voltage or current. For a voltage output DAC, the D/A converter is mathematically described as

$$V_o = K V_{FS} \left( d_1 \bar{2}^1 + d_2 \bar{2}^2 + \dots + d_n \bar{2}^n \right)$$

$V_o$  = output Voltage.

$V_{FS}$  = full scale output voltage

$K$  = scaling factor usually adjusted to 1.

$d_1, d_2, \dots, d_n$  =  $n$  bit binary word with

$d_1$  = Most Significant (MSB) with a

$$\frac{V_{FS}}{2}$$

$d_n$  = Least Significant bit (LSB)

with a weight of  $\frac{V_{FS}}{2^n}$

(2)

There are various ways to implement.

1. weighted resistor DAC.
2. R-2R Ladder.
3. Inverted R-2R ladder.

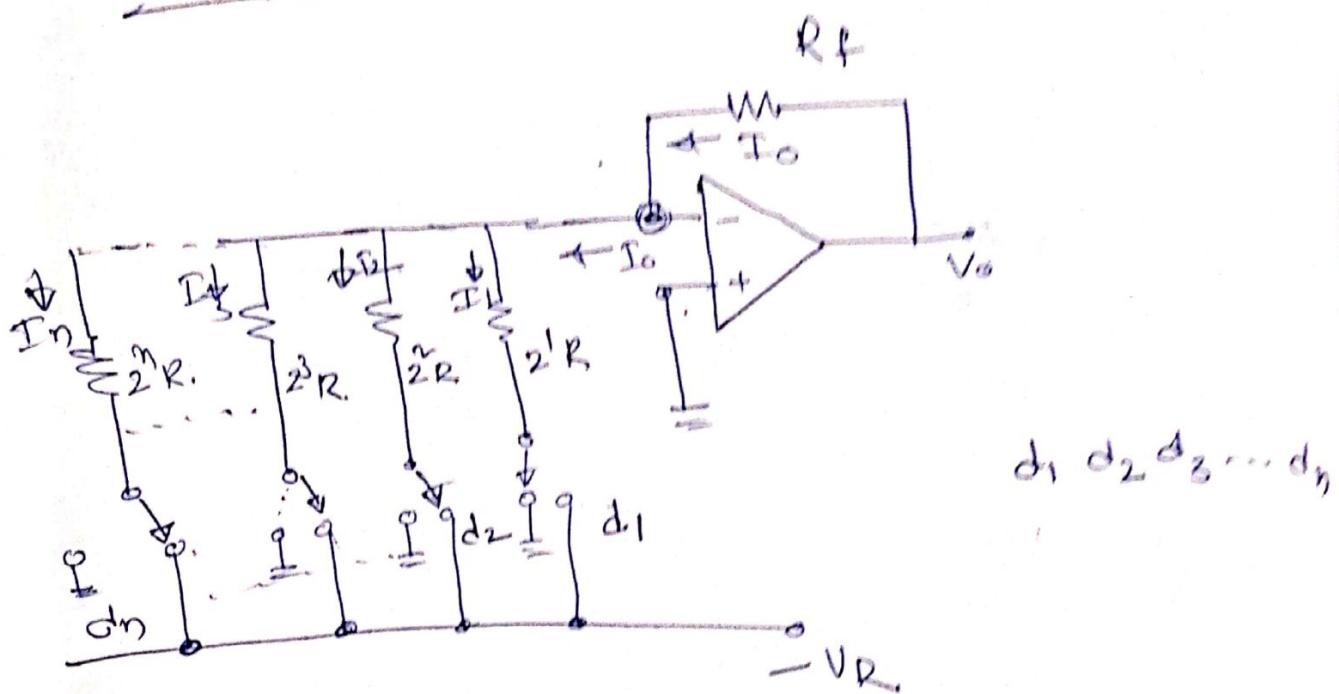
### Weighted Resistor DAC.

- \* It uses a summing amplifier with a binary weighted resistor network.
- \* It has  $n$ -electronic switches  $d_1, d_2, \dots, d_n$  controlled by binary  $I/p$  w.d.
- \* These switches are single pole double throw (SPDT) type
- \* If the binary  $I/p$  to a particular switch is 1, it connects the resistance to the reference voltage ( $-V_R$ ).
- \* If the  $I/p$  bit is '0', the switch connects the resistor to the ground.
- From the fig the output current  $I_o$  for an ideal op-amp can be written as

$I_o$  for an ideal op-amp can be written as

(2)

## weighted resistor DAC



$$I_o = I_1 + I_2 + I_3 + \dots + I_n,$$

$$I_o = \frac{V_R}{2^1 R} d_1 + \frac{V_R}{2^2 R} d_2 + \dots + \frac{V_R}{2^n R} d_n,$$

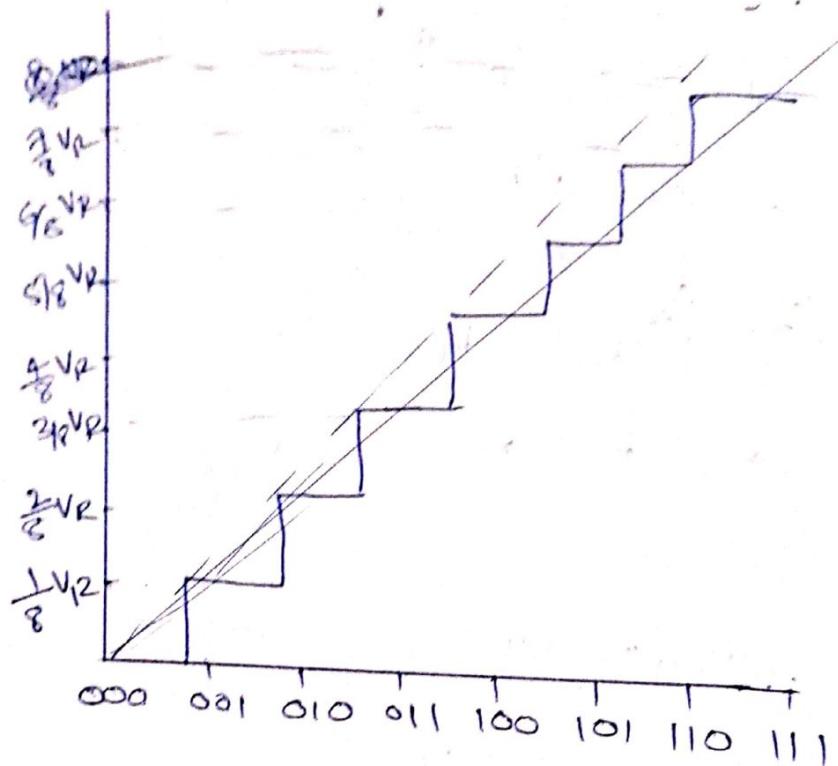
$$= \frac{V_R}{R} \left[ d_1 \bar{2}^1 + d_2 \bar{2}^2 + \dots + d_n \bar{2}^n \right]$$

The output voltage

$$V_o = I_o R_f = V_R \cdot \frac{R_f}{R} \left( d_1 \bar{2}^1 + d_2 \bar{2}^2 + \dots + d_n \bar{2}^n \right)$$

If  $\frac{R_f}{R} = R_1$ , ;  $k=1$  and  $V_{FS} = V_R$ .

(4)



(b) Transfer characteristics of a  
3-bit DAC.

The ckt shown in fig. uses a 5-bit reference. The analog op-p voltage is therefore the state code as shown in fig. It is a 5-bit weighted resistor DAC.

It may be noted that

(i) Fig (a) is connected in inverting mode, it can also be connected in non-inverting mode.

(ii) The op amp is simply working as a current to voltage converter.

(iii) The polarity of the reference voltage is chosen in accordance with the type of the switch used. For ex. if TTL compatible switches, the ref voltage should be +5V and the op voltage will be -5V.

\* The accuracy and stability of a DAC depends upon the accuracy of the resistive track.

(6)

## Limitations (d) Disadvantages of weighted resistor DAC are

In this resistor divider (d) Binary

weighted resistor DAC

is required in the network

1. Each resistor in

has a different value.

2. The resistor used for the MSB

is required to handle a much greater current than that used for the LSB resistor.

For better resolution, the word length has to be increased. Thus as the number of bits increases, the range of resistor values increase.

For 8-bit DAC, the resistor

required are  $2^0 R, 2^1 R, \dots, 2^7 R$

The largest resistor is 128 times the smallest one. for 8-bit DAC

for a 12-bit DAC, the largest resistor required is 5.12 mA if smallest is 2.5 kΩ.

(5)

The fabrication of such a large resistor value has  $I_C$  is not practical. Also the voltage drop across such a large resistor due to the bias current would also effect the accuracy.

The choice of smallest resistor value as  $2.5\text{ k}\Omega$  is reasonable, otherwise loading effect will be there.

### R-2R Ladder DAC

\* wide range of resistors are required in binary weighted resistor type DAC.

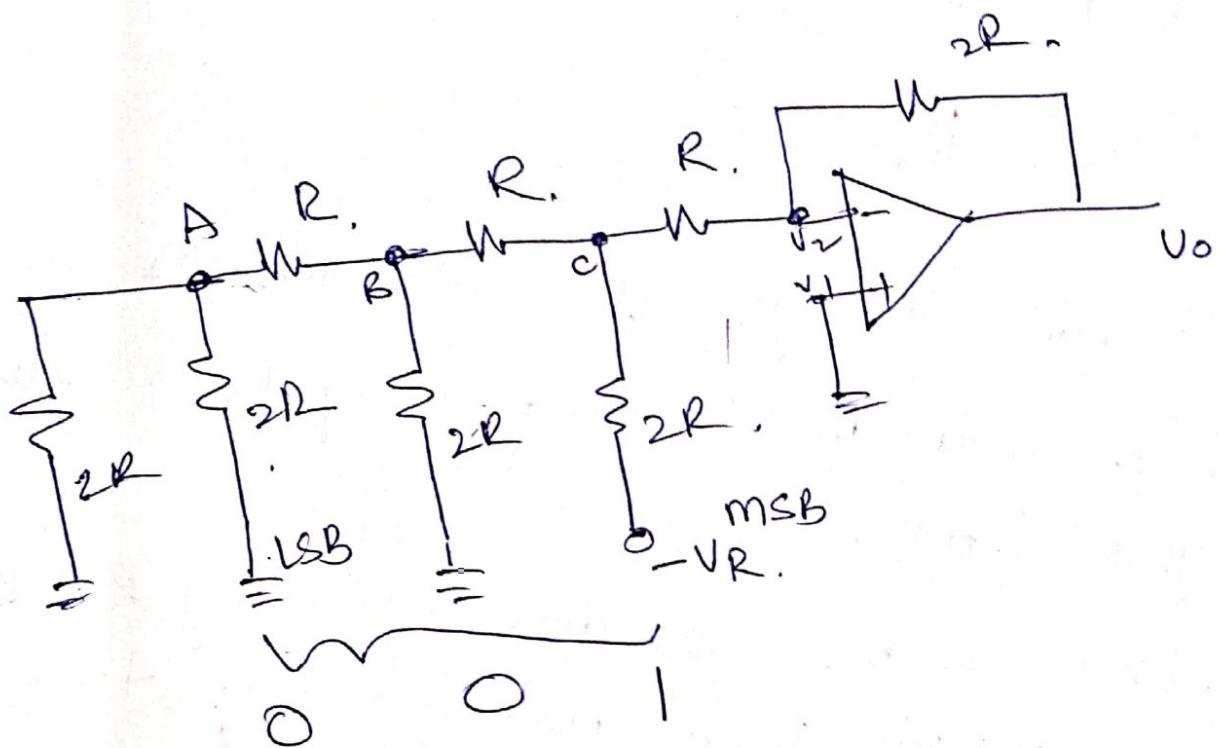
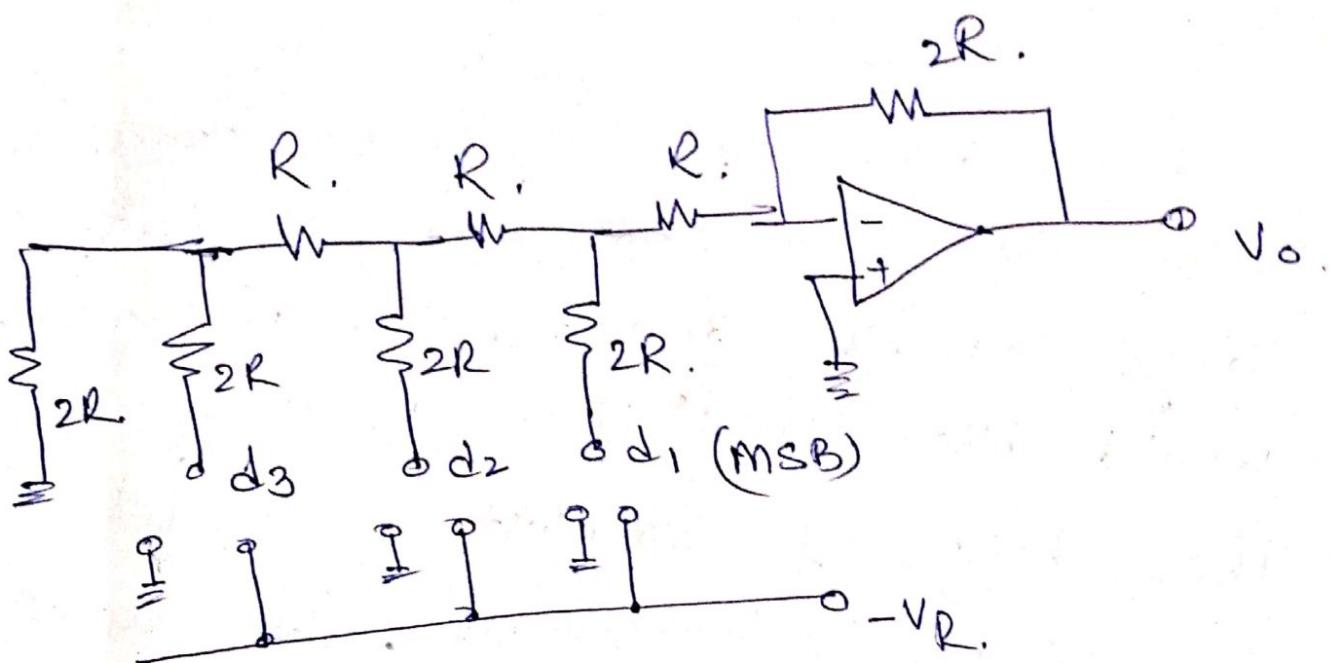
This can be avoided by using R-2R ladder type DAC where only two

values of resistors are required.

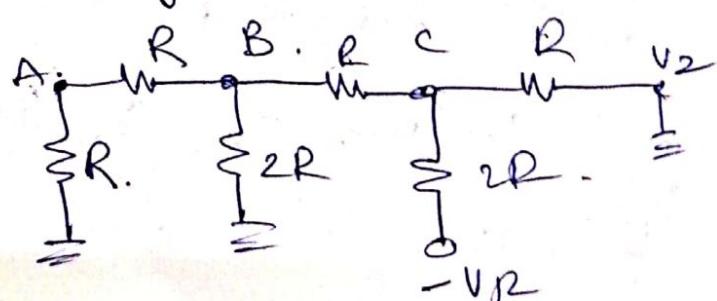
It is well suited for IC realization.

The typical values of R ranges from  $2.5\text{ k}\Omega$  to  $10\text{ k}\Omega$ .

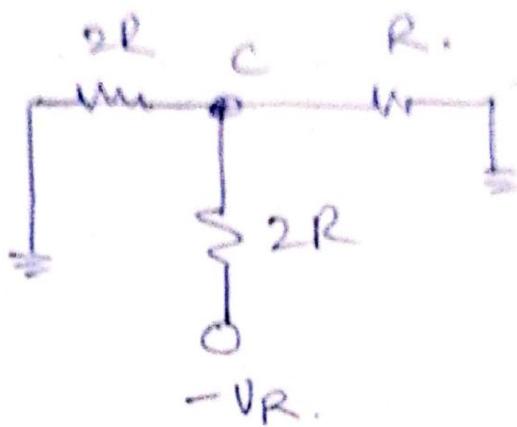
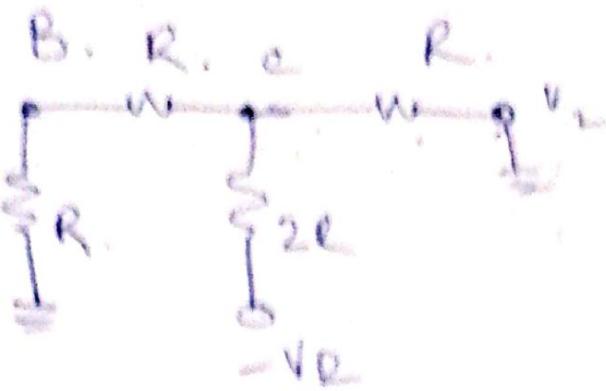
6



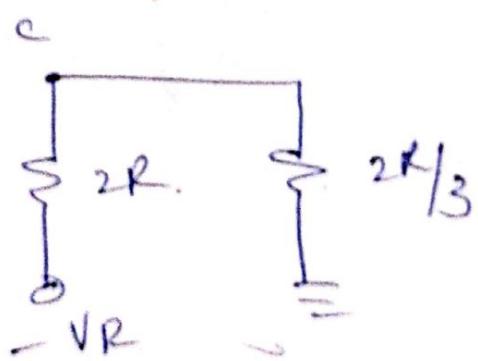
The Voltage at mode C



(7)



$$\frac{(2R)(CR)}{2R+R} = \frac{2R}{3R} = \frac{2R}{3}$$



$$\frac{2R}{2R+6R} = \frac{2R}{8R} = \frac{1}{4}$$

Voltage at node 'c' is

$$= -V_R \times \frac{\frac{2R}{3}}{\frac{2R}{3} + 2R} = -\frac{V_R}{4}$$

(8)

The output Voltage

$$V_o = \left( \frac{-2R}{R} \right) \left( -\frac{V_R}{4} \right) = \frac{V_R}{2} = \frac{V_{PS}}{2}$$

In a similar fashion we can  
cal the voltages for

$$010 \rightarrow \frac{V_{PS}}{4} \rightarrow \frac{V_{PS}}{2^2}$$

$$001 \rightarrow \frac{V_{PS}}{8} \rightarrow \frac{V_{PS}}{2^3}$$

$$\begin{aligned} 111 &\rightarrow \frac{V_{PS}}{2} + \frac{V_{PS}}{4} + \frac{V_{PS}}{8} \\ &= \frac{4+2+1}{8} = \frac{7}{8} V_{PS} \approx V_{PS} \end{aligned}$$

## Mono lithic DAC

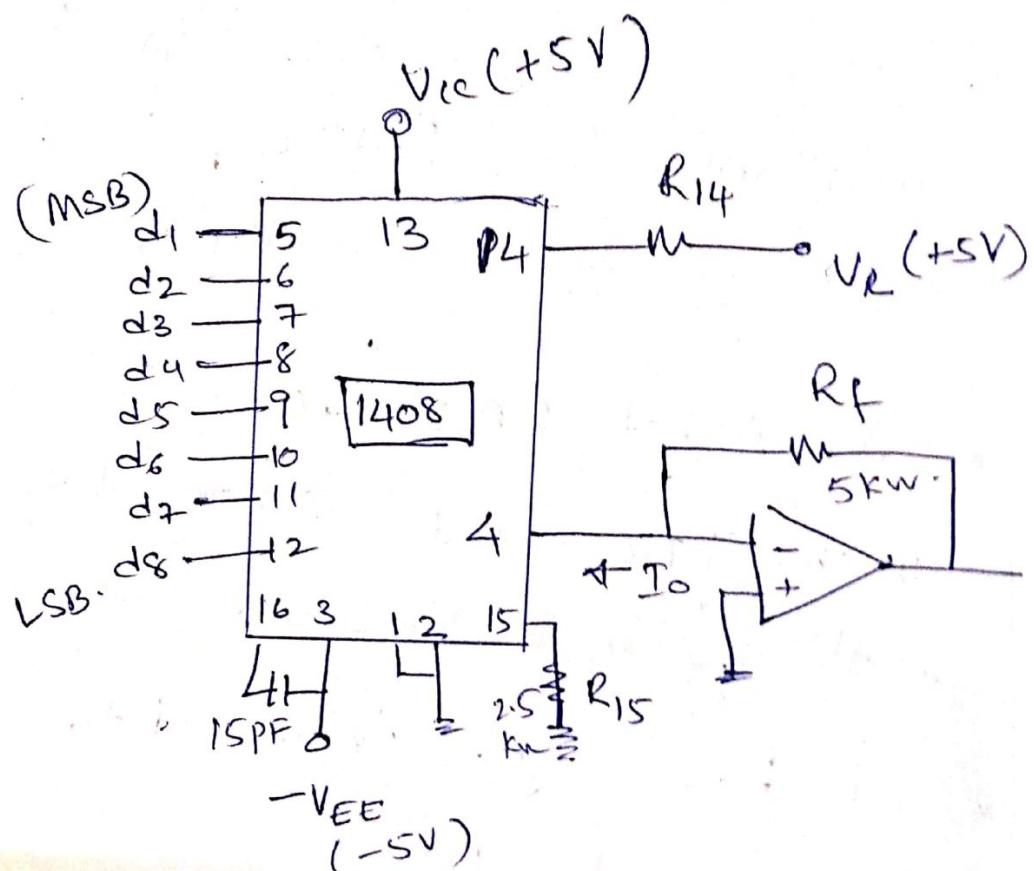
(9)

- \* Mono lithic DAC's consists of R-2R ladder, switches and the R<sub>R</sub> resistor are available for 8, 10, 12, 14 and 16 bit resolution from various manufacturers.
- \* The MC 1408 L is a 8-bit DAC with current output.
- \* There are hybrid D/A converters available in DATEL DAC-H-2 series for current as well as voltage output.
- \* A 8-bit DAC 1408 is compatible with TTL and CMOS logic with settling time around 300 nsec.
- \* It has eight input data lines d<sub>7</sub>(MSB) through d<sub>0</sub>(LSB).
- \* It requires 2mA reference current for full scale I<sub>f</sub> and two power supplies V<sub>cc</sub> = +5V and V<sub>EE</sub> = -5V

The total reference current source is determined by resistor  $R_{14}$  and voltage reference  $V_R$  and equal to

$$\frac{V_R}{R_{14}} = \frac{5V}{2.5k\Omega} = 2mA.$$

- \* The resistor  $R_{15} = R_{14}$  match the input impedance of the reference source.



The output current  $I_o$  is cal. of

$$I_o = \frac{V_R}{R_{14}} \left( \sum_{i=1}^8 d_i 2^i \right) \quad d_1 = 0 \text{ or } 1$$

For full scale I/P (i.e. ds through  
 $d_1 = 1$ )

$$I_O = \frac{5V}{2.5k\Omega} \left[ \sum_{i=1}^8 1 \times \bar{z}_i \right]$$

$$= 2mA \left( \frac{255}{256} \right) = \underline{\underline{1.992 \text{ mA}}}$$

MSB                    LSB                     $\rightarrow$  Full Scale.

1 1 1 1 1 1 1

$$\left( \frac{1}{2} + \frac{1}{2^2} + \frac{1}{2^3} + \frac{1}{2^4} + \frac{1}{2^5} + \frac{1}{2^6} + \frac{1}{2^7} + \frac{1}{2^8} \right)$$

$$\frac{2^7 + 2^6 + 2^5 + 2^4 + 2^3 + 2^2 + 2^1 + 1}{2^8} = \frac{255}{256}$$

The output is 1 LSB less than the full scale reference current of 2mA.

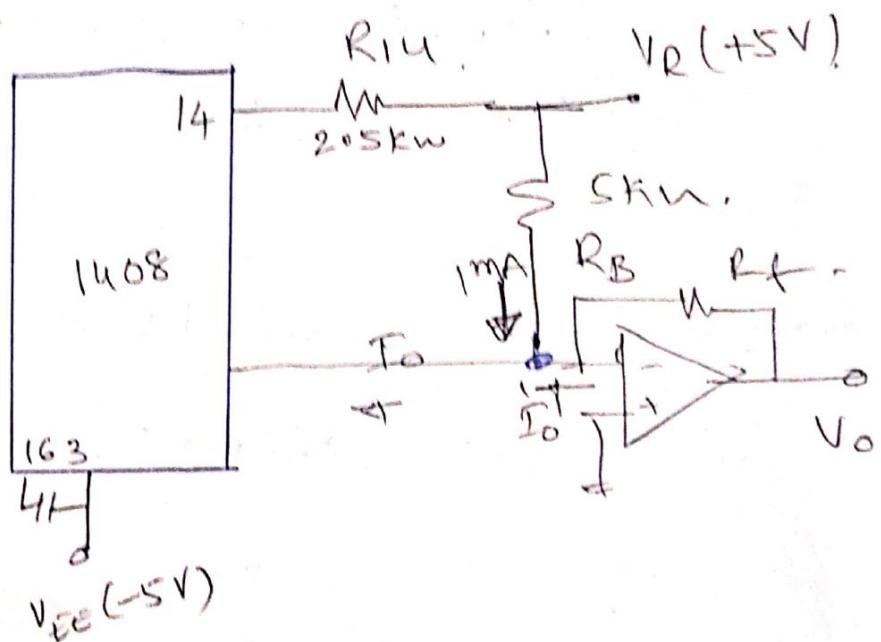
So, the output voltage  $V_o$  for the full scale I/P is -

$$V_o = 2mA \left( \frac{255}{256} \right) \times 5k\Omega = 9.961V.$$

In general after output voltage  
Vo is given by

$$V_o = \frac{V_R}{R_m} R_d \left[ \frac{d_1}{2} + \frac{d_2}{4} + \frac{d_3}{8} + \dots + \frac{d_8}{256} \right]$$

The 1408 DAC can be calibrated  
for bipolar range from -5V to +5V  
by adding resistor  $R_B$  (5kW) between  
 $V_R$  and opp Pin 4.



The resistor  $R_B$  supplies  $I_{mA}$  ( $\frac{V_R}{R_B}$ )

current to the output in the opposite  
direction of the current generated by I/P

$$\begin{aligned} I_o' &= I_o - \left( \frac{V_R}{R_B} \right) \\ &= \left( \frac{V_R}{R_{IN}} \right) \left( \sum_{i=1}^d d_i \frac{1}{2^i} \right) - \frac{V_R}{R_B}. \end{aligned}$$

For the Binary S/p word 00000000  
i.e zero S/p, the output becomes

$$\begin{aligned} V_o &= I_o' R_f \\ &= \left( I_o - \frac{V_R}{R_B} \right) R_f \\ &= \left( 0 - \frac{5V}{5kW} \right) 5kW. \end{aligned}$$

$$V_o = \underline{-5V} \quad \text{for } \underline{00000000}$$

For binary input word 10000000  
the  $V_o$  becomes

$$\begin{aligned} V_o &= \left( I_o - \frac{V_R}{R_B} \right) R_f \\ &= \left( \frac{V_R}{R_{IN}} \left( \frac{d_1}{2} \right) - \frac{V_R}{R_F} \right) R_f \\ &= \left( \frac{5}{205kW} \left( \frac{1}{2} \right) - \frac{5V}{5kW} \right) 5kW = \underline{0V} \end{aligned}$$

$$(1\text{mA} - 1\text{mA}) \times 5\text{k}\Omega = 0\text{V.}$$

(14)

For Binary I/p word = 1111 1111

The output voltage becomes.

$$V_o = \left[ \frac{VR}{R_{14}} \left( \frac{255}{256} \right) - 1\text{mA} \right] R_F$$

$$= (1.992 \text{ mA} - 1\text{mA}) \times 5\text{k}\Omega.$$

$$V_o = 0.992 \text{ mA} \times 5\text{k}\Omega = \underline{\underline{4.960\text{V}}}.$$

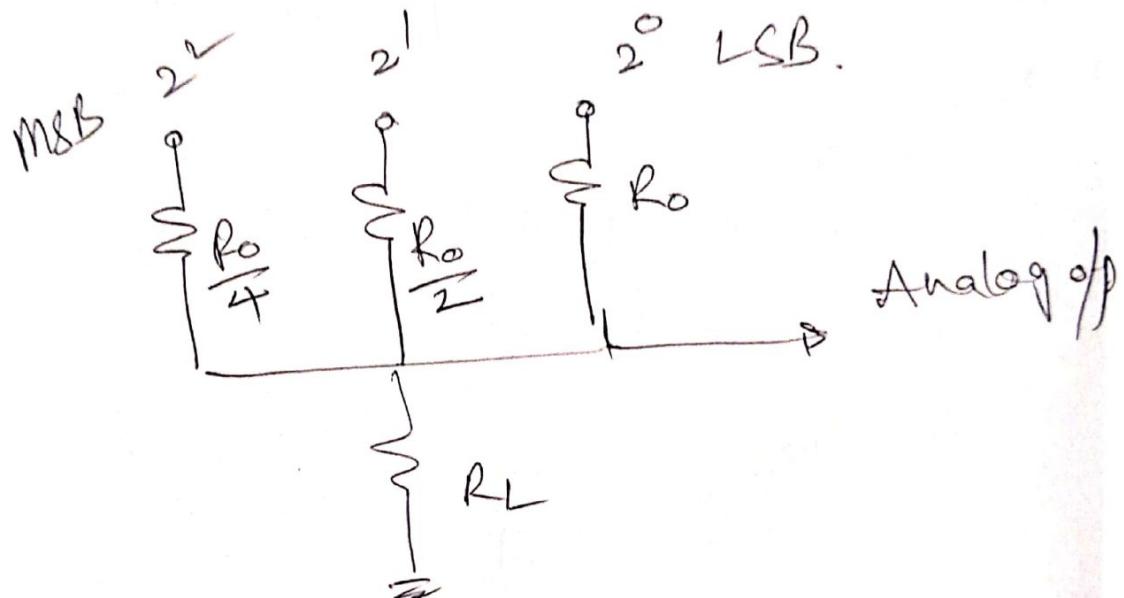
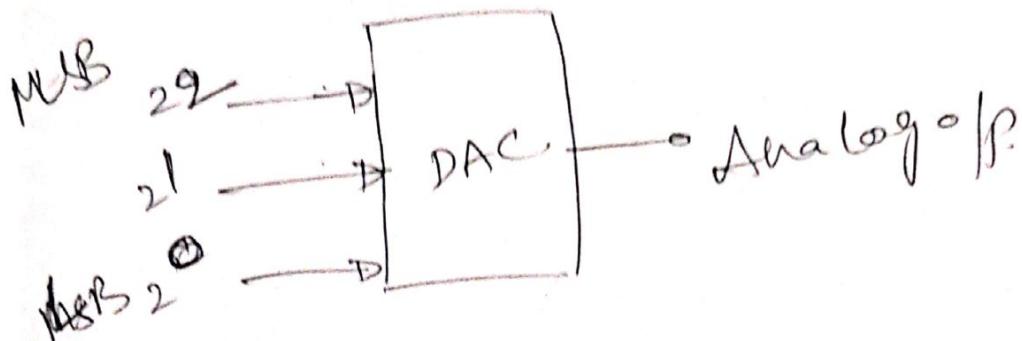
∴ 1111 1111

0000 0000  $\xrightarrow{-5\text{V}}$

1 000 0000  $\xrightarrow{0\text{V}}$

1.111 1111  $4.960\text{V} \approx +5\text{V}$

# Resistive N/w.

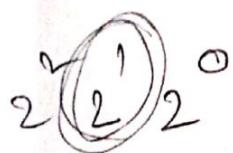


0 0 0	0 V
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	4
1 0 1	5
1 1 0	6
1 1 1	7 V

1 in the 2<sup>0</sup> position will cause

$$+7 \times \frac{1}{7} = 1V \text{ at the o/p.}$$

$$2^1 = 2 \text{ and } 2^0 = 1$$

2  2<sup>0</sup>

$$7 \times \frac{2}{7} = 2V.$$

In  
twice

$$7 \times \frac{4}{7} = \underline{\underline{4V}}.$$

$$\frac{V_R}{2^0 - 1} = \frac{V_D}{7}$$

$$\frac{\text{Bit}}{2^0} \rightarrow \frac{\text{weight}}{1/7}.$$

$$2^1 \rightarrow 2/7$$

$$2^2 \rightarrow 4/7$$

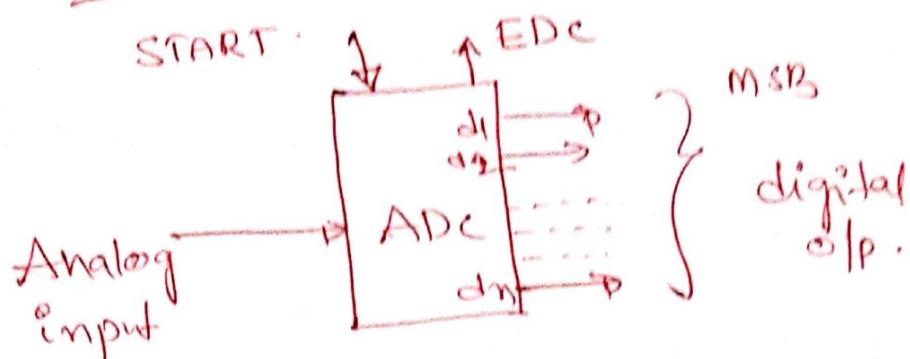
$$\text{Sum} \rightarrow 7/7$$

3-bit

Bit	weight
2 <sup>0</sup>	1/7
2 <sup>1</sup>	2/7
2 <sup>2</sup>	4/7
2 <sup>3</sup>	8/7
.	14/7
4-bit	14/7

(1)

## A-D Converters



The block diagram of ADC shown in Fig. It provides the function just opposite to that of a DAC. It accepts an analog input Voltage  $V_a$  and produces an output binary word  $d_1 d_2 \dots d_n$  of functional value  $D$ , so that

$$D = d_1 \bar{2}^1 + d_2 \bar{2}^2 + \dots + d_n \bar{2}^n.$$

where  $d_1$  is the most significant bit and  $d_n$  is the least significant bit  
 An ADC has two additional controls The START up to tell the ADC when to start the conversion and the EOC (end of conversion), output to tell when the conversion is complete.

ADCs can be classified broadly into two groups

## Direct type ADCs and Integrating type<sup>(2)</sup>

Direct type ADCs compare a given analog signal with the internally generated equivalent ref. signal.

### Direct type ADCs

- ① Flash (comparator) type converter,
- ② Counter type converter.
- ③ Tracking or servo converter.
- ④ Successive approximation type converter.

Integrating type ADCs perform conversion in an indirect manner, by first changing the analog input signal to a linear function of time or frequency and then to digital code.

- ① charge balancing ADC
- ② Dual slope ADC.

The most commonly used ADCs are successive approximation and the integrator type. The successive approximation ADCs are used in applications such as data loggers and instrumentation.

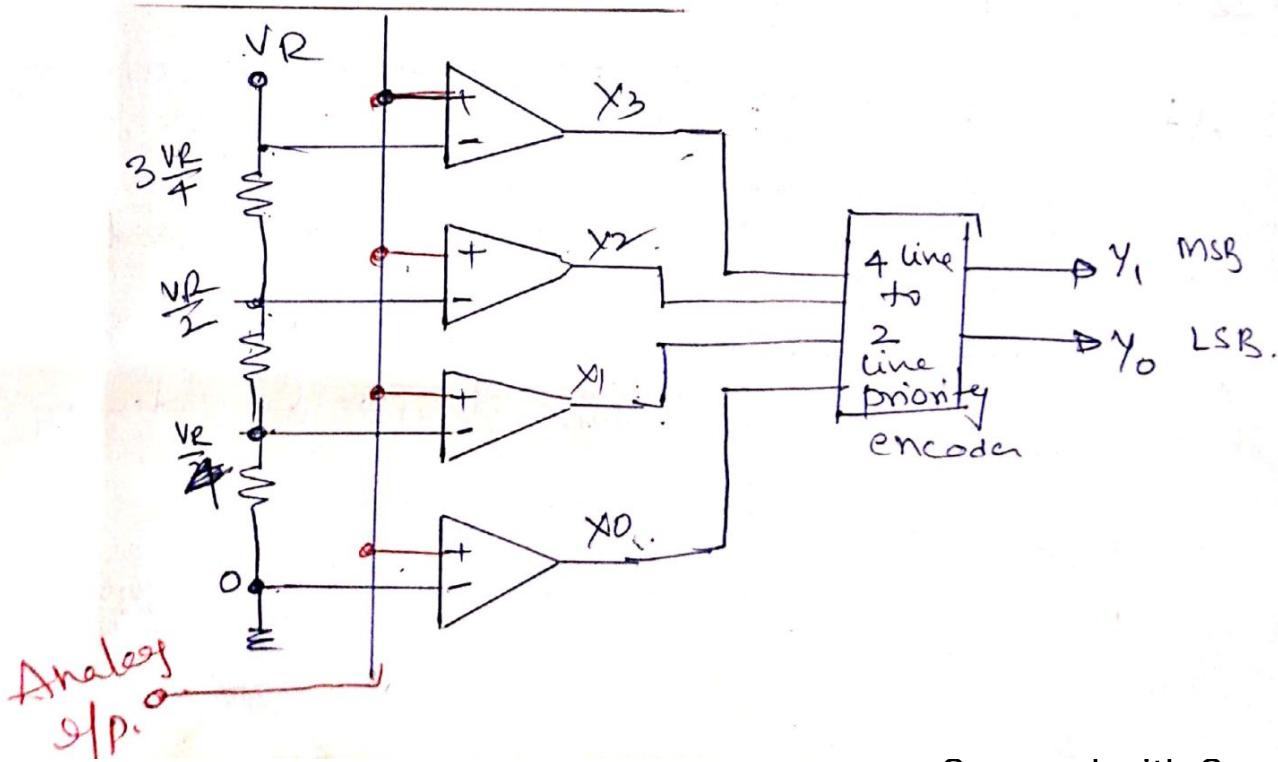
where conversion speed is important.  
 The successive approximation and  
 comparitor type are faster but generally  
 less accurate than integrating type  
 converters.

The integrating type converter is used  
 in applications such as digital meter,  
 panel meter and monitoring system  
 where the conversion accuracy is  
 critical.

### Direct type ADCs

The parallel comparitor (or) FLASH

ADC converter.



(4)

Input Voltage $V_a$	Output of comparators $X_2 \ X_1 \ X_0$	Digital output from priority encoder
$0 \text{ to } \frac{V_R}{4}$	0 0 0 1	0 0
$\frac{V_R}{4} \text{ to } \frac{V_R}{2}$	0 0 1 1	0 1
$\frac{V_R}{2} \text{ to } \frac{3V_R}{4}$	0 1 1 1	1 0
$\frac{3V_R}{4} \text{ to } V_R$	1 1 1 1	1 1

This is the simplest possible A/D converter. It is at the same time fastest and most expensive technique. Fig shows a 2-bit ADC. It consists of a resistive divider network, 4 ( $2^2$ ) comparators and 4 line to 2 line encoder (2-bit priority encoder).

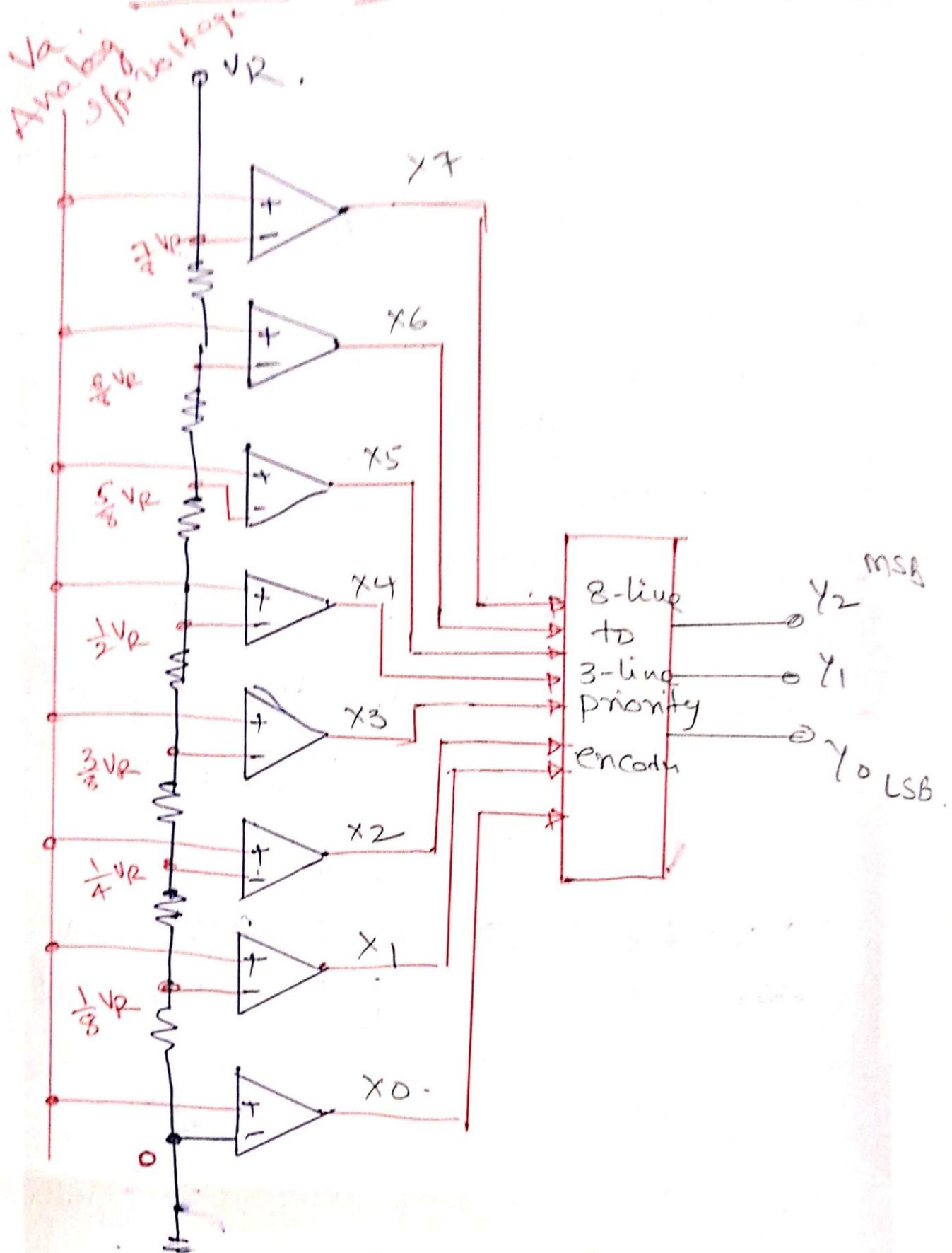
At each node of the resistive divider, a comparison voltage is available. Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between reference voltage  $V_R$  and ground. The purpose of the ckt is to compare

The analog input voltage  $V_A$  with each of the mode voltages. The truth table for the flash type AD converter is shown in Fig.

- \* The circuit has the advantage of high speed as the conversion take place simultaneously rather than sequentially.
- \* Typical conversion time is 100ns & less.
- \* Conversion time is limited only by the speed of comparators and of the priority encoder. By using an advanced Selection Micro Devices AMD 686A ~~comparators~~ and T1147 priority encoder conversion delays of the order of 20ns can be obtained.

The disadvantage of this converter is no of comparators required almost doubles for each added bit.

# 3-bit Flash type A/D converter



(7)

I/p Voltage	$x_7 \ x_6 \ x_5 \ x_4 \ x_3 \ x_2 \ x_1 \ x_0$	$y_2 \ y_1 \ y_0$
0 to $VR/8$	0 0 0 0 0 0 0 1	0 0 0
$VR/8$ to $VR/4$	0 0 0 0 0 0 1 1	0 0 1
$VR/4$ to $3VR/8$	0 0 0 0 0 1 1 1	0 1 0
$3VR/8$ to $VR/2$	0 0 0 0 1 1 1 1	0 1 1
$VR/2$ to $5VR/8$	0 0 0 1 1 1 1 1	1 0 0
$5VR/8$ to $3VR/4$	0 0 1 1 1 1 1 1	1 0 1
$3VR/4$ to $7VR/8$	0 1 1 1 1 1 1 1	1 1 0
$7VR/8$ to $VR$	1 1 1 1 1 1 1 1	1 1 1

Truth table for a Flash Type A/D  
Converter.

② The counter type A(D) converter.

(8)

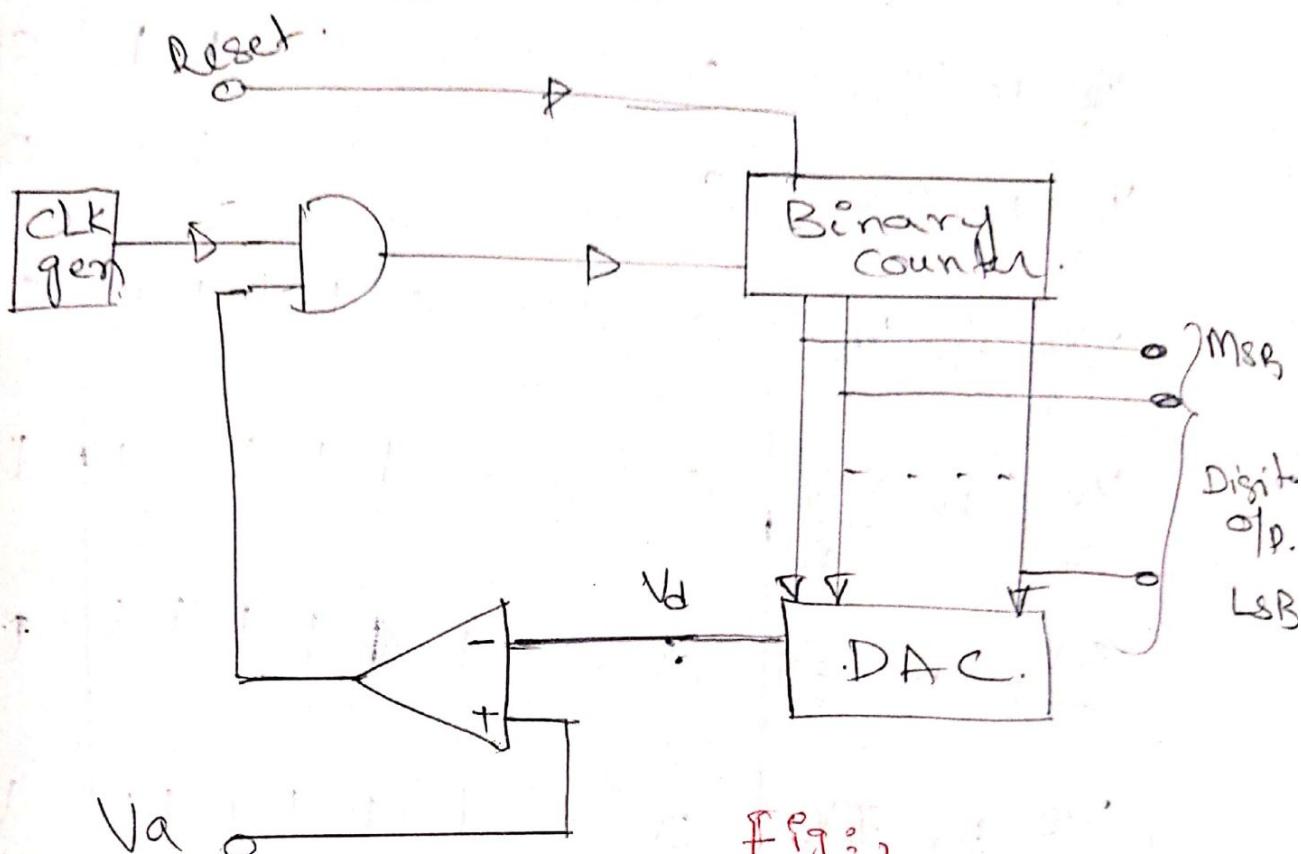


Fig: 2

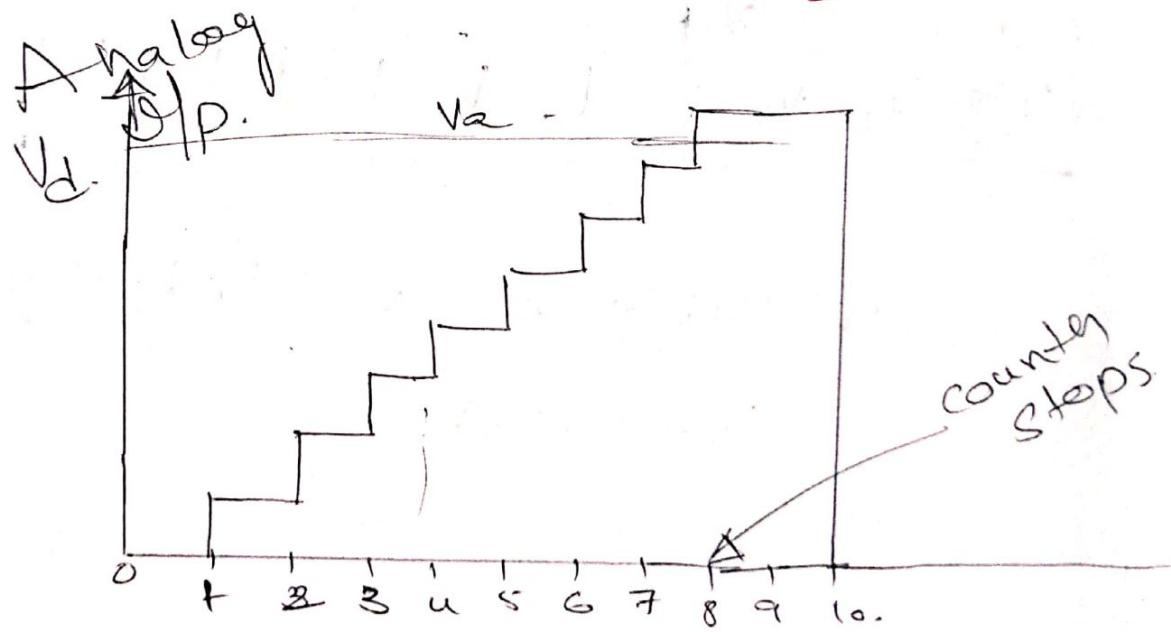


Fig: 2



D/A D/P Step response waveform for End test

(9)

A 3-bit counting ADC based on  
shown in Fig.

The counter is reset to zero out  
by reset pulse.

- \* upon the release of RESET,  
the clock pulses are counted by  
the binary counter.
- \* These pulses go through the AND  
gate which is enabled by the voltage  
Comparate high output.

- \* The number of pulses counted  
increase with time.

- \* The binary word representing this  
count is used as the I/p of a  
D/A converter whose output is a  
staircase of the type shown in  
Fig: 2.

- \* The analog output  $V_d$  of DAC is  
compared to the analog input  $V_a$   
by the comparitor.

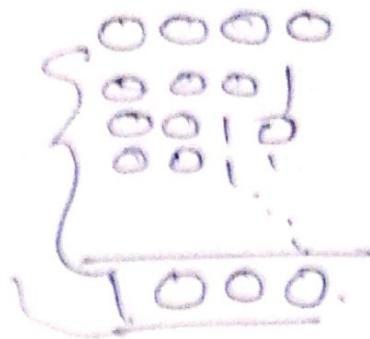
- \* If  $V_a > V_d$ , the output of the comparator becomes high and the AND gate is enabled to allow the transmission of the clock pulses to the counter.
- \* When  $V_a < V_d$ , the output of the comparator becomes low and the AND gate is disabled.
- \* This stops the counting at the time  $V_a \leq V_d$  and the digital output of the counter represents the analog I/P voltage  $V_a$ .
- \* Low speed is the most serious draw back of this method. The conversion time can be as long as  $(2^n - 1)$  clock periods depending upon the magnitude of I/P voltage  $V_a$ .

(11)

A 12-bit system with 1MHz clock freq., the counter will take  $(2^{12} - 1)$  clock pulses for full scale M.P.

For 1MHz clock  $T = 1 \text{ usec.}$

$$4095 \times 1 \text{ usec} = \underline{\underline{4.095 \text{ msec.}}}$$



$$\frac{8V}{V_a > V_d}$$

$$V_a = V_d.$$

o/p of the comparison = 0

stop clock pulse

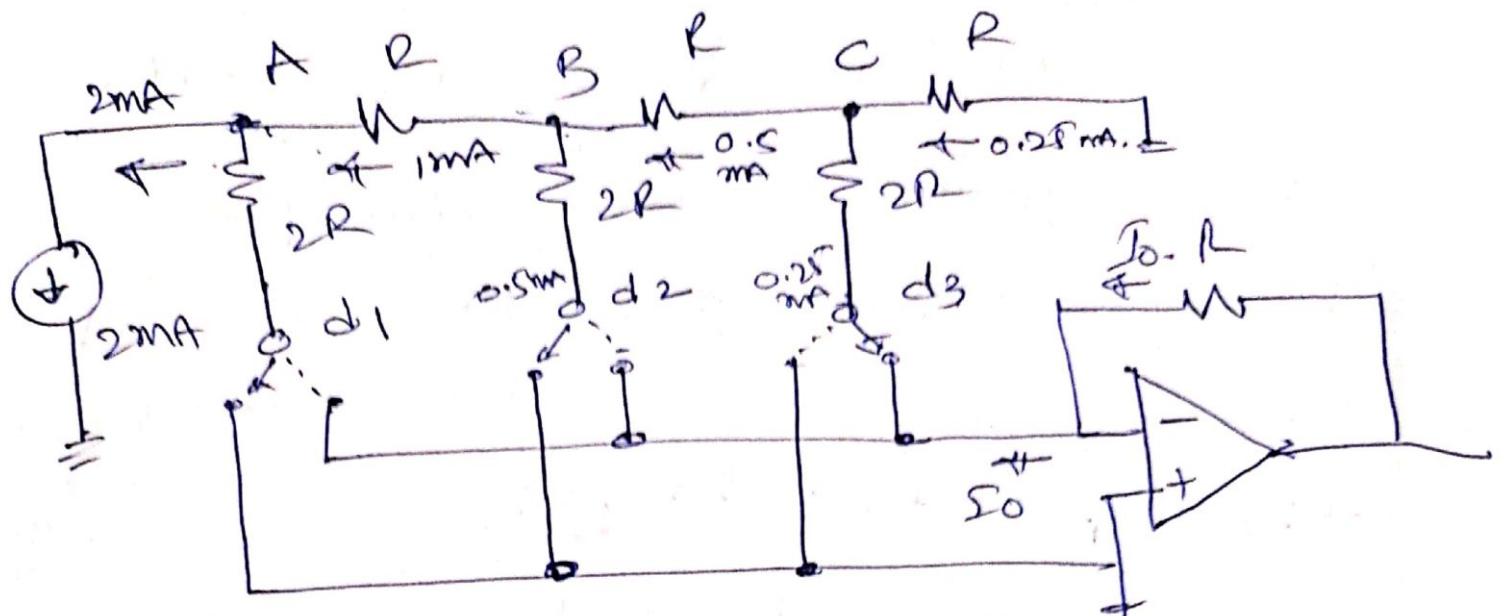
## Inverted R-2R ladder

In weighted resistor type DAC and R-2R ladder type DAC, current flowing in the resistor changes as the I/P data changes..

More power dissipation causes heating which in turn, creates non-linearity in DAC.

This problem can be avoided completely in Inverted R-2R ladder type DAC.

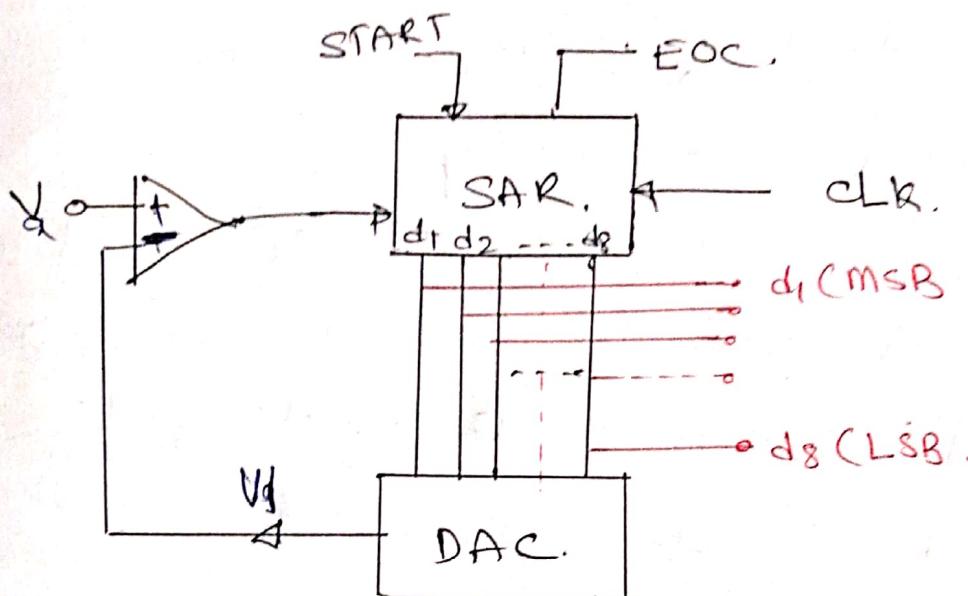
A 3-bit Inverted R-2R ladder type DAC is shown in Fig. where the positions of MSB and LSB are Interchanged



(1)

## SUCCESSIVE APPROXIMATION

### CONVERTER



Functional diagram of the Successive Approximation ADC

- \* The successive approximation technique uses a very efficient code search strategy to complete  $n$ -bit conversion in just  $n$ -clock periods.
- \* An eight bit converter would require eight clock pulses to obtain a digital output.

The circuit uses a successive approximation register (SAR) to find the required value of each bit by trial and error. The circuit operates as follows:

(2)

with the arrival of the START Command the trial code is 10000000.

The output  $V_d$  of the DAC is now compared with analog input  $V_a$ .

If  $V_a$  is greater than the DAC, if  $V_d$  is greater than the DAC output  $V_d$  is less than the trial 10000000 in the

correct digital representation.

The MSB is left at '1' and the next lower significant bit is made 1 and further tested.

However if  $V_a$  is less than the DAC output, then 10000000 is greater than the correct digital representation. So reset MSB to '0' and go on to next lower significant bit.

This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested.

Whenever the DAC output crosses  $V_a$  the comparator changes state and thus can be taken as the end of conversion (EOC).

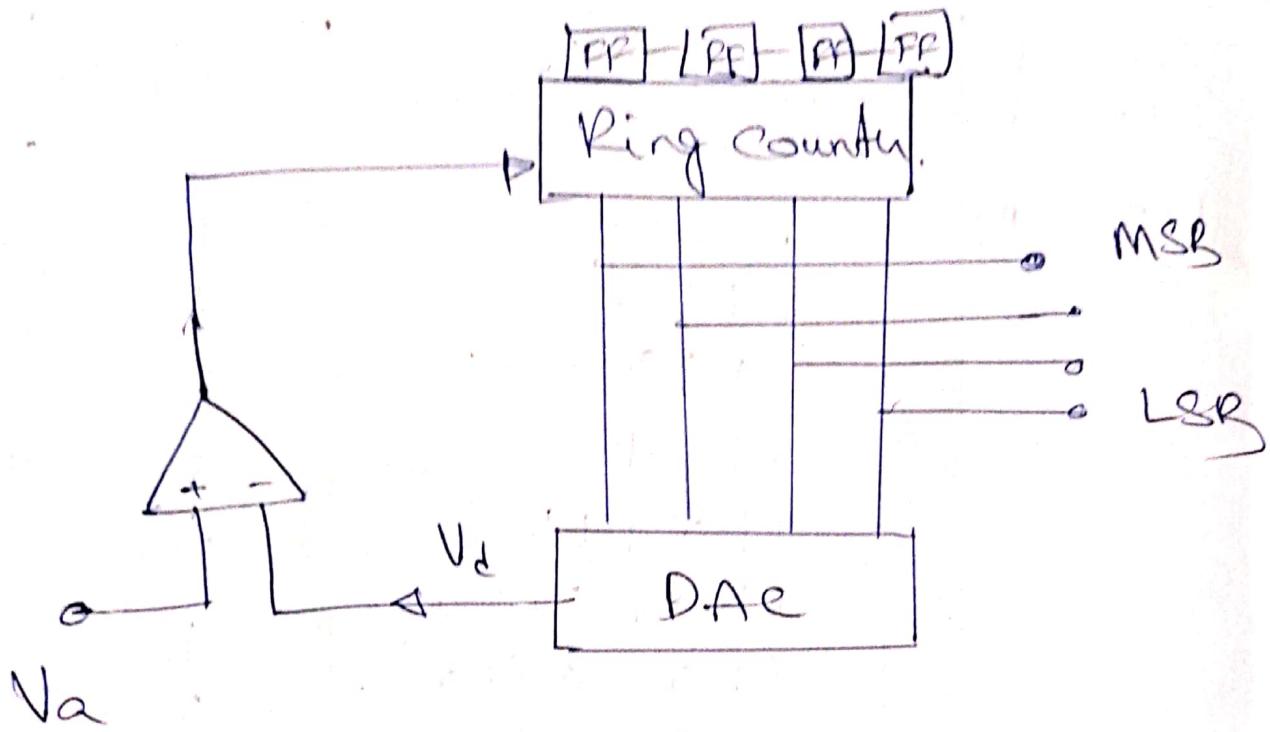
Correct representation	Successive approximation register output $V_d$ at different stages in conversion	Comparator out
11010100	1 0000000	1
	1 1000000	1
	1 1100000	0
	1 1010000	1
	1 1011000	0
	1 10110100	1
	1 1010101	0
	1 1010100	0

It can be seen that the D/A output voltage becomes successively closer to the actual analog I<sub>pp</sub> voltage. It requires eight pulses to establish the accurate output regardless of the value of the analog I<sub>pp</sub>.

one additional clock pulse is used to load the output register and reinitialize the clk.

4-bit Successor appr.

(4)



1st clock  
puls

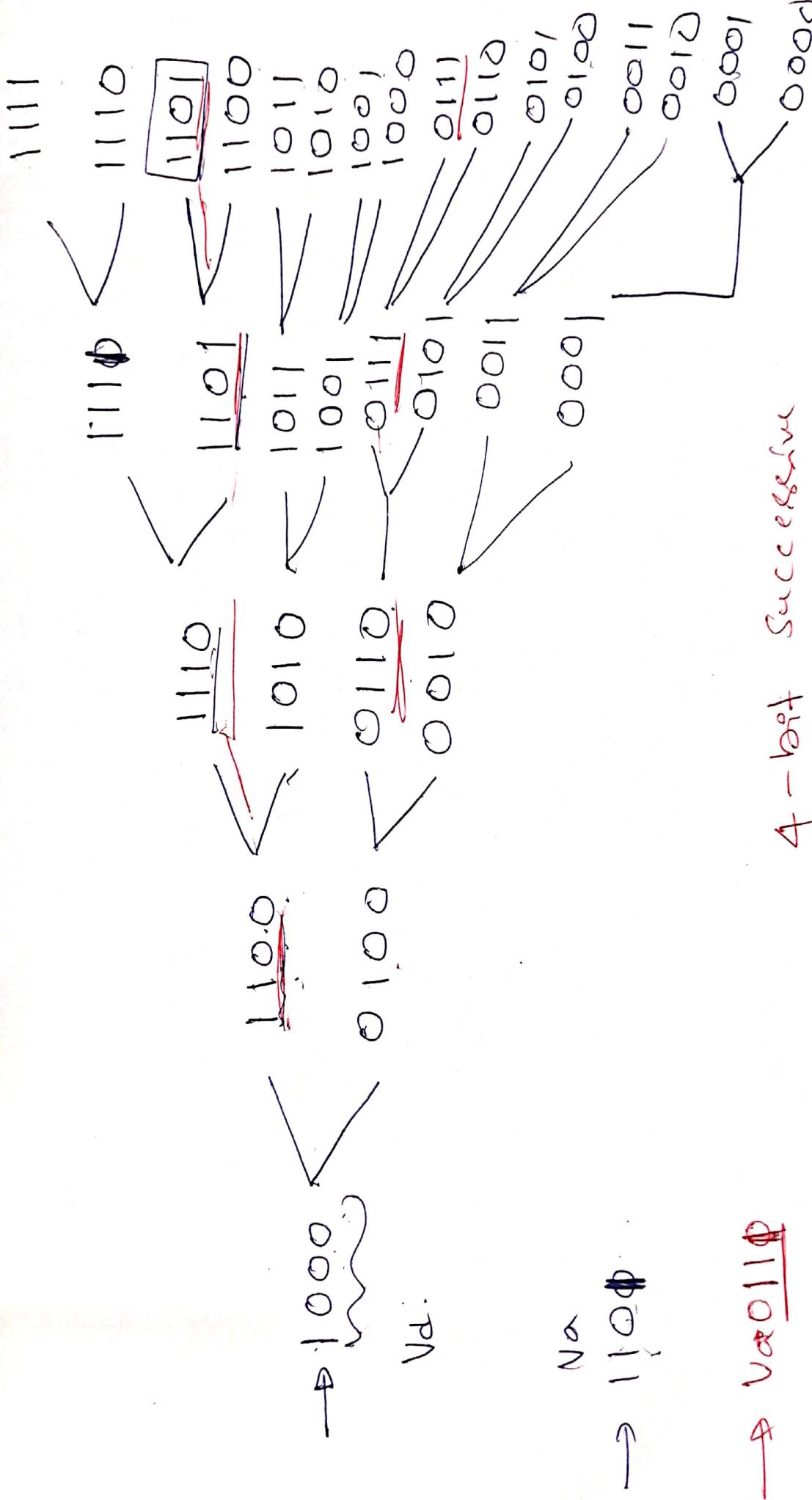
1 0 0 0

2nd clk 0 1 0 0

3rd clk 0 0 1 0

4th clk. 0 0 0 1

⑤



## Specification of DACs & ADCs ⑥

### ① Resolution-

The resolution of a converter is the smallest change in voltage which may be produced at the output of the converter.

For example, an 8-bit D/A Converter has  $2^m - 1 = 255$  equal intervals. Hence the smallest change in the output voltage is  $(1/255)$  of the full scale output range.

$$\text{Resolution in mV} = \frac{V_{FS}}{2^m - 1} = \frac{1LSB}{2^m}$$

Resolution is stated in no of ways.

An 8-bit DAC is said to have

: 8-bit resolution

: a resolution of 0.392 Percent of full scale.

: a resolution of 1 part in 255.

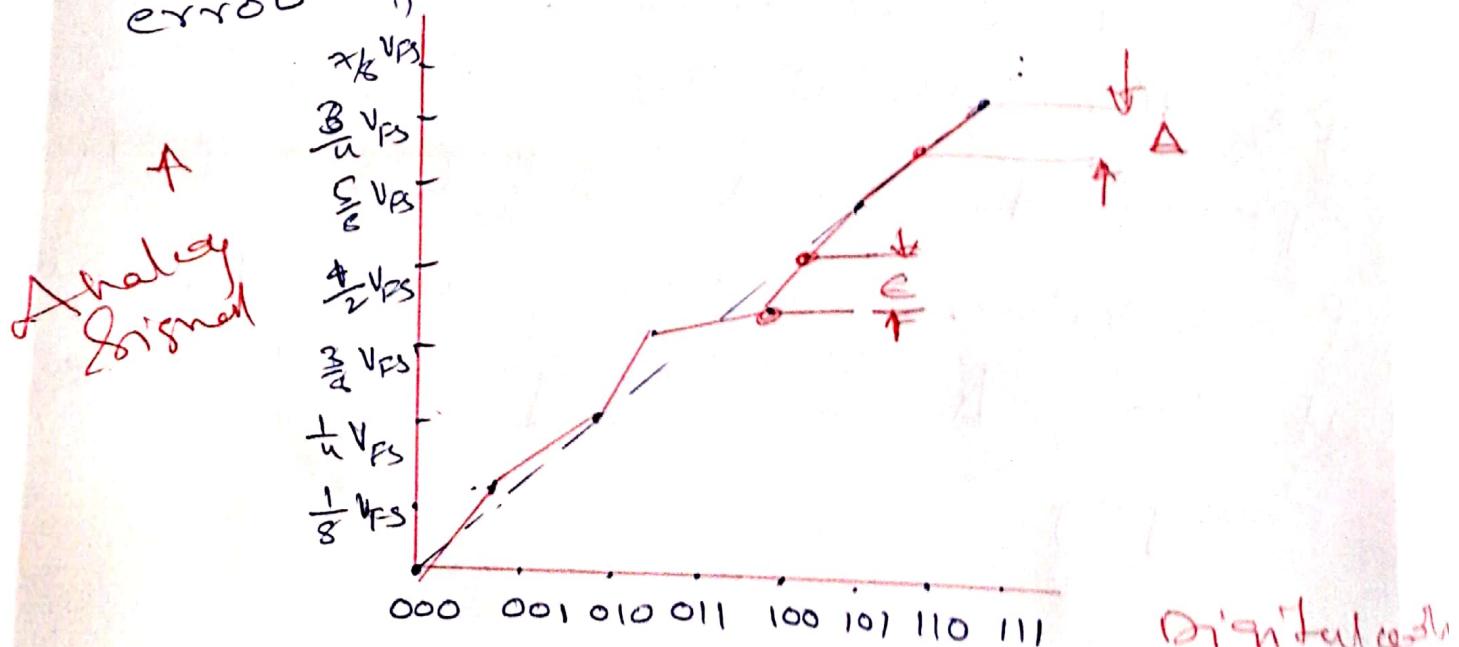
# Resolution for 6-16 bit DACs ⑦

Bits	Intervals	LSB size (% of full scale)	LSB size (10V Fullscale)
6	63	1.588%	158.8mV.
8	255	0.392%	39.2mV.
10	1023	0.0978%	9.78mV.
12	4095	0.0244%	2.44mV.
14	16383	0.0061%	0.61mV.
16	65535	0.0015%	0.15mV.

Similarly, the resolution of an A/D converter is defined as the smallest change in ~~the~~ analog I/p for a one bit change at the o/p.

Linearity: The linearity of an A/D or D/A converter is an important measure of its accuracy, and tells how close the converter O/p is to its ideal transfer characteristic. In an ideal DAC, equal increment in the digital I/p should produce equal increment in the analog output and the transfer curve should be linear.

The linearity error measures the deviation of the actual O/p from the fitted line and is given by  $\epsilon/\Delta$ . The error is usually expressed as a fraction of LSB increment or percentage of full scale voltage. A good converter exhibits a linearity error of less than  $\pm \frac{1}{2}$  LSB.



Absolute Accuracy - Accuracy is the maximum deviation between the actual converted output and the ideal converted output.

Relative accuracy is the maximum deviation after gain and offset errors have been removed.

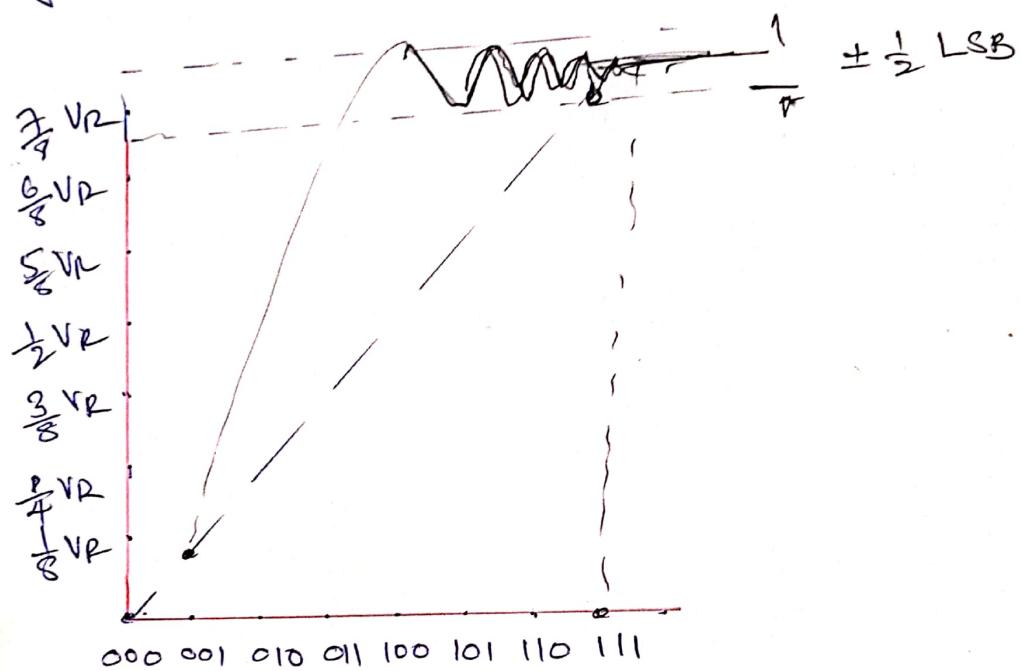
Data sheets normally specify relative accuracy rather than absolute accuracy.

The accuracy of a converter is also specified in terms of LSB increments or percentage of full scale voltage.

### settling time

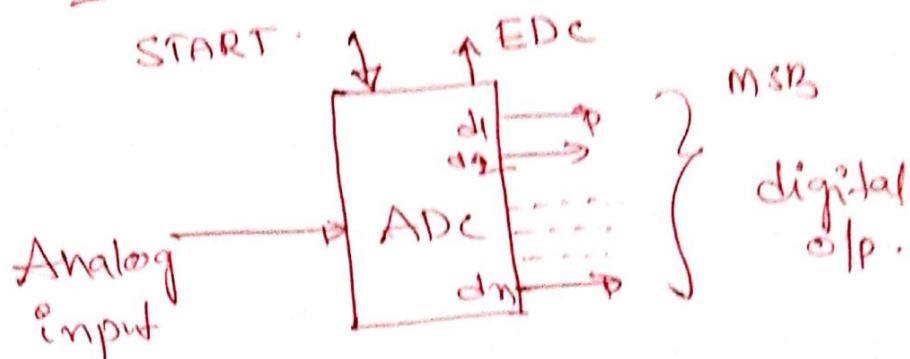
The most important dynamic parameter is the settling time. It represents the time it takes for the output to settle within specified band  $\pm \frac{1}{2}$  LSB of its final value following a code change at the IP (usually a full scale change).

It depends upon the switching time of the logic circuitry due to internal parasitic capacitances and inductances. Settling time ranges from 100ns to 10usec depending on width and type of circuit used.



(1)

## A-D Converters



The block diagram of ADC shown in Fig. It provides the function just opposite to that of a DAC. It accepts an analog input Voltage  $V_a$  and produces an output binary word  $d_1 d_2 \dots d_n$  of functional value  $D$ , so that

$$D = d_1 \bar{2}^1 + d_2 \bar{2}^2 + \dots + d_n \bar{2}^n.$$

where  $d_1$  is the most significant bit and  $d_n$  is the least significant bit  
 An ADC has two additional controls  
 The START up to tell the ADC when to start the conversion and the EOC (end of conversion), output to tell when the conversion is complete.

ADCs can be classified broadly into two groups

## Direct type ADCs and Integrating type<sup>(2)</sup>

Direct type ADCs compare a given analog signal with the internally generated equivalent ref. signal.

### Direct type ADCs

- ① Flash (comparator) type converter,
- ② Counter type converter.
- ③ Tracking or servo converter.
- ④ Successive approximation type converter.

Integrating type ADCs perform conversion in an indirect manner, by first changing the analog input signal to a linear function of time or frequency and then to digital code.

- ① charge balancing ADC
- ② Dual slope ADC.

The most commonly used ADCs are successive approximation and the integrator type. The successive approximation ADCs are used in applications such as data loggers and instrumentation.

(3)

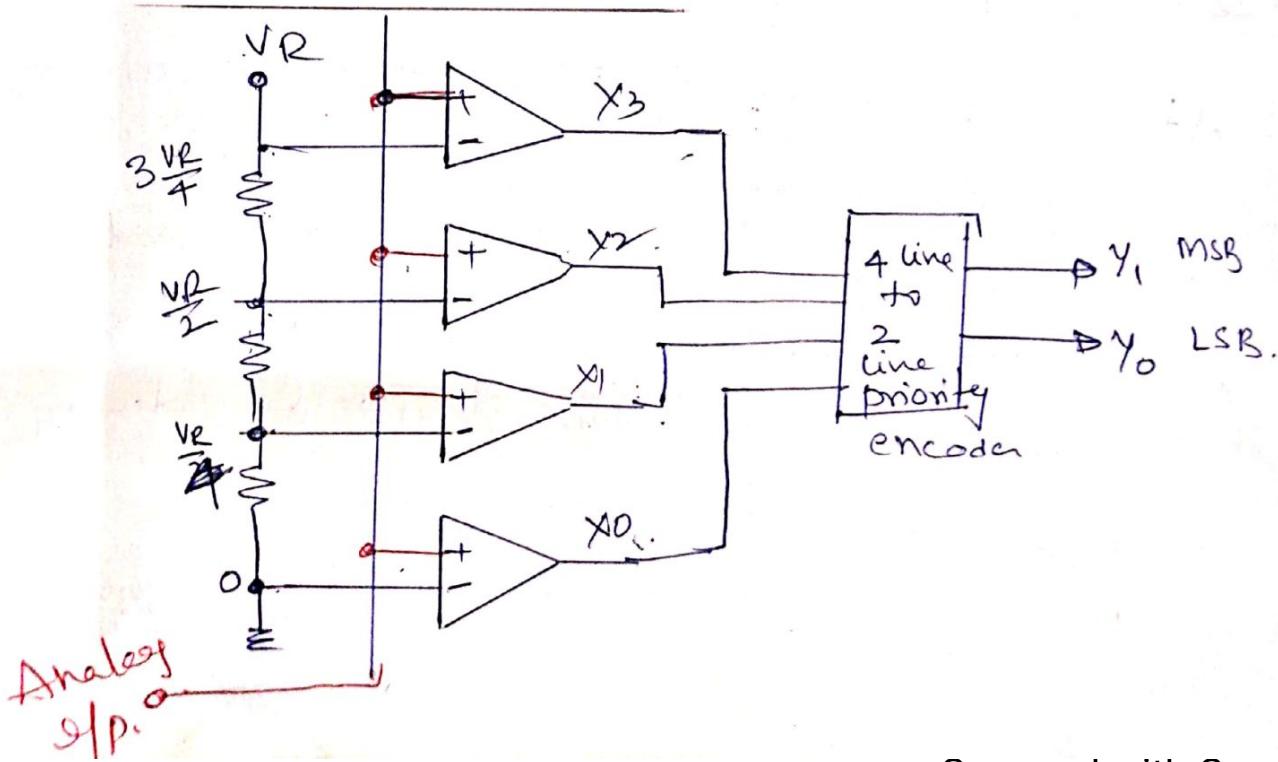
where conversion speed is important.  
 The successive approximation and  
 comparitor type are faster but generally  
 less accurate than integrating type  
 converters.

The integrating type converter is used  
 in applications such as digital meter,  
 panel meter and monitoring system  
 where the conversion accuracy is  
 critical.

## Direct type ADCs

The parallel comparitor (or) FLASH

ADC converter.



(4)

Input Voltage $V_a$	Output of comparators $X_2 \ X_1 \ X_0$	Digital output from priority encoder
$0 \text{ to } \frac{V_R}{4}$	0 0 0 1	0 0
$\frac{V_R}{4} \text{ to } \frac{V_R}{2}$	0 0 1 1	0 1
$\frac{V_R}{2} \text{ to } \frac{3V_R}{4}$	0 1 1 1	1 0
$\frac{3V_R}{4} \text{ to } V_R$	1 1 1 1	1 1

This is the simplest possible A/D converter. It is at the same time fastest and most expensive technique. Fig shows a 2-bit ADC. It consists of a resistive divider network, 4 ( $2^2$ ) comparators and 4 line to 2 line encoder (2-bit priority encoder).

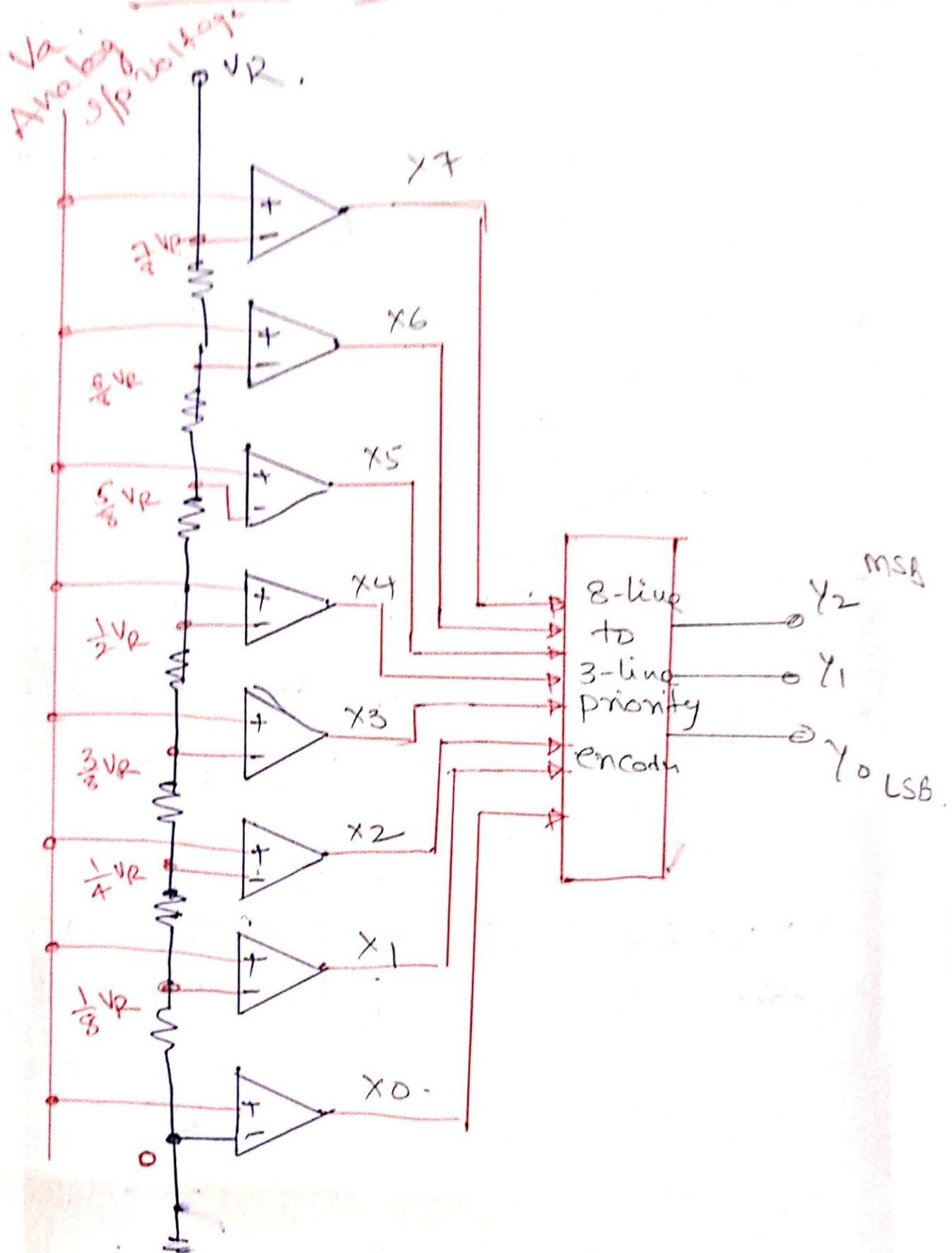
At each node of the resistive divider, a comparison voltage is available. Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between reference voltage  $V_R$  and ground. The purpose of the ckt is to compare

The analog input voltage  $V_A$  with each of the mode voltages. The truth table for the flash type AD converter is shown in Fig.

- \* The circuit has the advantage of high speed as the conversion take place simultaneously rather than sequentially.
- \* Typical conversion time is 100ns & less.
- \* Conversion time is limited only by the speed of comparators and of the priority encoder. By using an advanced Selection Micro Devices AMD 686A ~~comparators~~ and T1147 priority encoder conversion delays of the order of 20ns can be obtained.

The disadvantage of this converter is no of comparators required almost doubles for each added bit.

# 3-bit Flash type A/D converter



(7)

I/p Voltage	$x_7 \ x_6 \ x_5 \ x_4 \ x_3 \ x_2 \ x_1 \ x_0$	$y_2 \ y_1 \ y_0$
0 to $\frac{VR}{8}$	0 0 0 0 0 0 0 1	0 0 0
$\frac{VR}{8}$ to $\frac{VR}{4}$	0 0 0 0 0 0 1 1	0 0 1
$\frac{VR}{4}$ to $\frac{3VR}{8}$	0 0 0 0 0 1 1 1	0 1 0
$\frac{3VR}{8}$ to $\frac{VR}{2}$	0 0 0 0 1 1 1 1	0 1 1
$\frac{VR}{2}$ to $\frac{5VR}{8}$	0 0 0 1 1 1 1 1	1 0 0
$\frac{5VR}{8}$ to $\frac{3VR}{4}$	0 0 1 1 1 1 1 1	1 0 1
$\frac{3VR}{4}$ to $\frac{7VR}{8}$	0 1 1 1 1 1 1 1	1 1 0
$\frac{7VR}{8}$ to VR	1 1 1 1 1 1 1 1	1 1 1

Truth table for a Flash Type A/D  
Converter.

② The counter type A(D) converter.

(8)

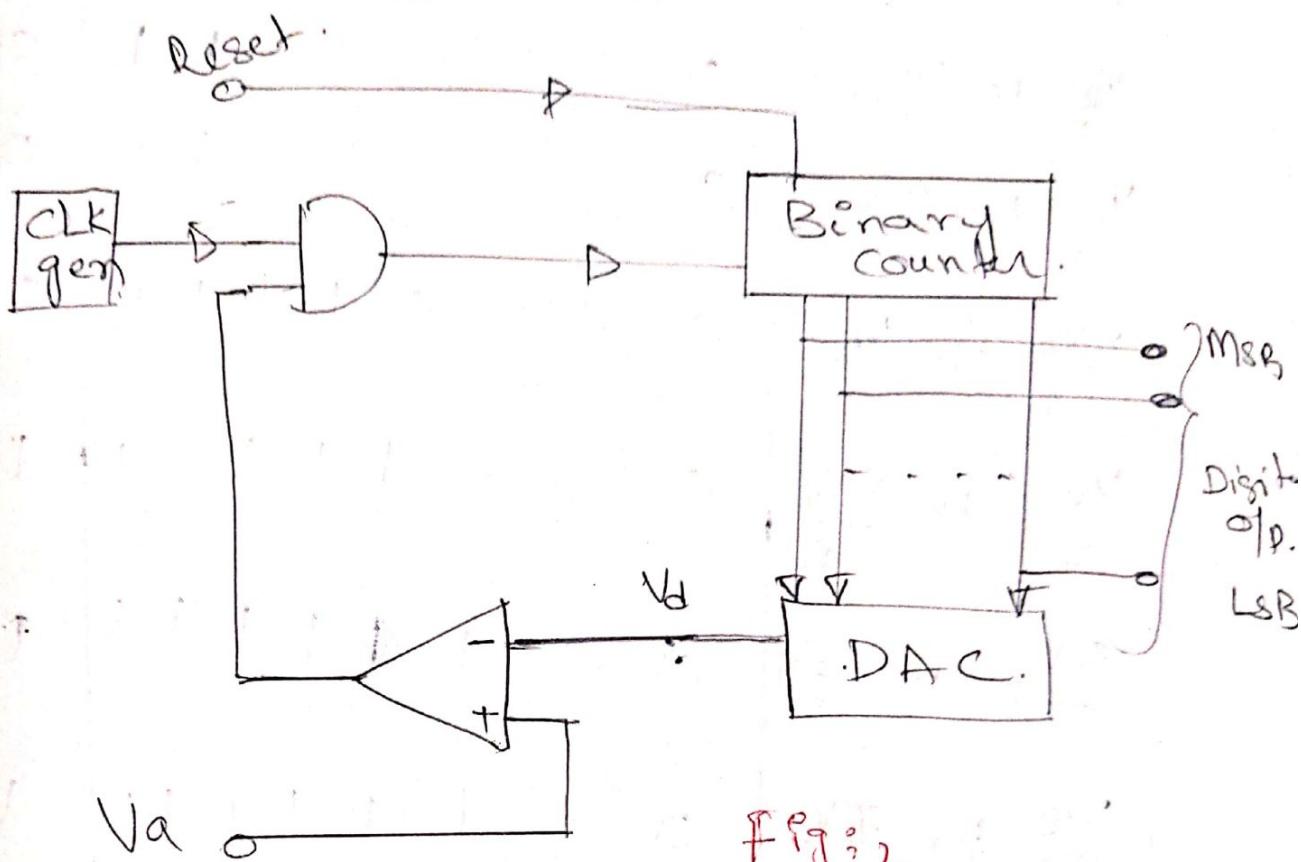


Fig: 2

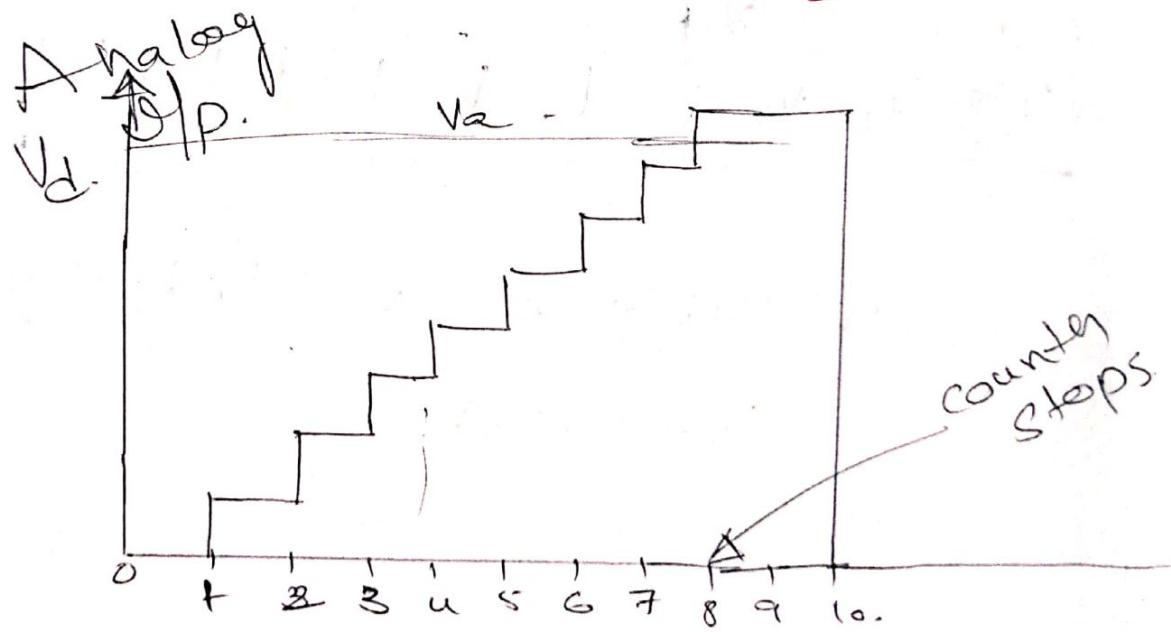


Fig: 2



D/A O/P Staircase wave for End result

(9)

A 3-bit counting ADC based on  
shown in Fig.

The counter is reset to zero out  
by reset pulse.

- \* upon the release of RESET,  
the clock pulses are counted by  
the binary counter.
- \* These pulses go through the AND  
gate which is enabled by the voltage  
Comparate high output.

- \* The number of pulses counted  
increase with time.

- \* The binary word representing this  
count is used as the I/p of a  
D/A converter whose output is a  
staircase of the type shown in  
Fig: 2.

- \* The analog output  $V_d$  of DAC is  
compared to the analog input  $V_a$   
by the comparitor.

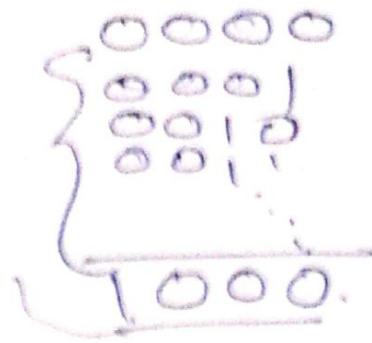
- \* If  $V_a > V_d$ , the output of the comparator becomes high and the AND gate is enabled to allow the transmission of the clock pulses to the counter.
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(11)

A 12-bit system with 1MHz clock freq., the counter will take  $(2^{12} - 1)$  clock pulses for full scale M.P.

For 1MHz clock  $T = 1 \text{ usec.}$

$$4095 \times 1 \text{ usec} = \underline{\underline{4.095 \text{ msec.}}}$$



8V

$V_a > V_d$

$V_a = V_d$

o/p of the comparison = 0

stop clock pulse

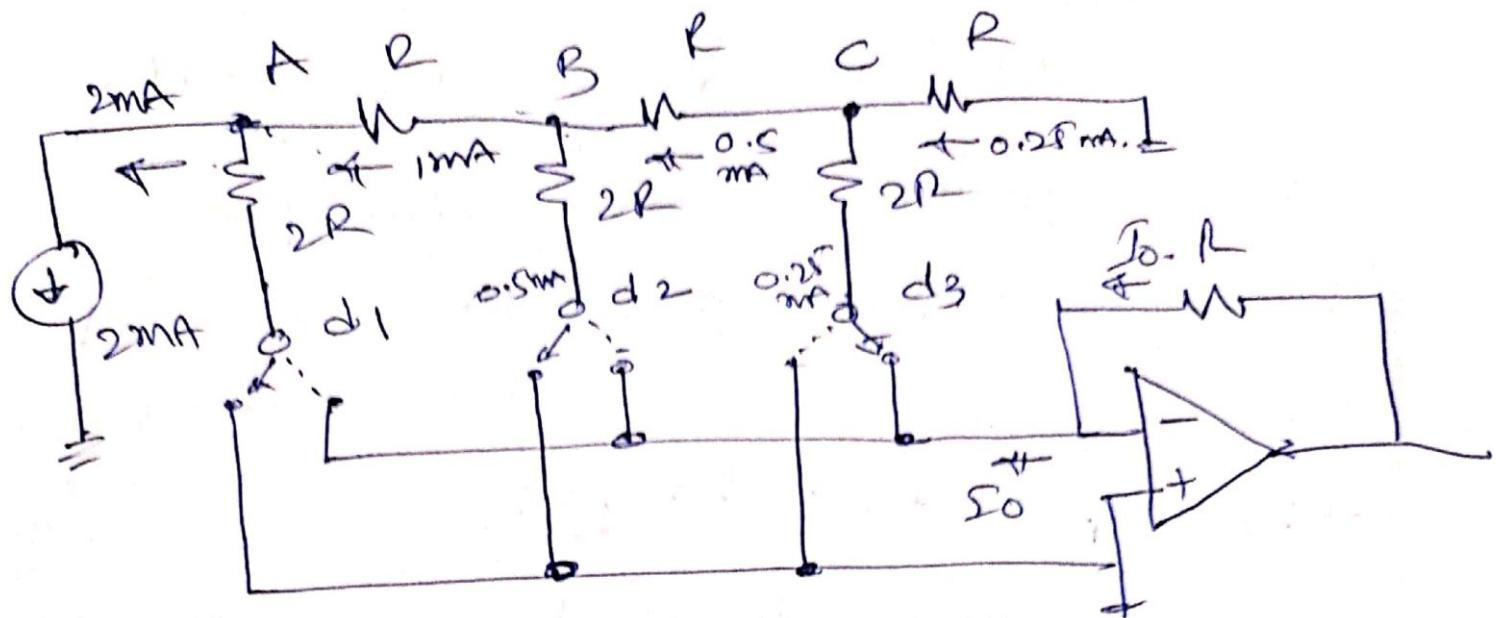
## Inverted R-2R ladder

In weighted resistor type DAC and R-2R ladder type DAC, current flowing in the resistor changes as the I/P data changes..

More power dissipation causes heating which in turn, creates non-linearity in DAC.

This problem can be avoided completely in Inverted R-2R ladder type DAC.

A 3-bit Inverted R-2R ladder type DAC is shown in Fig. where the positions of MSB and LSB are Interchanged



UNIT - 1

1. what are the different linear IC packages?
2. Define CMRR and Thermal drift.
3. Draw the pin configuration of an OP-amp 741IC.
4. what are the ideal op-amp characteristics?
5. Draw the equivalent circuit of an op-amp.
6. Draw an ideal voltage transfer curve of an op-amp.
7. How fast can the output of an op-amp change by 10V, if its slew rate is  $10 \text{ V/us}$ .
8. Draw the block diagram of an op-amp.
9. What is meant by Virtual ground.
10. Define the following terms.
  - (a) Input offset voltage.
  - (b) Input offset current
  - (c) Supply voltage rejection ratio.
  - (d) offset voltage adjustment range.
  - (e) Large-Signal voltage gain.

## UNIT - 2

1. what are the important features of an Instrumentation amplifier.
2. what are the limitations of basic Integrator circuit using opamp
3. what are the limitations of basic differentiator circuit using op-amp.
4. what are applications of Integrator.
5. Mention any two applications of a Differentiator.
6. what is a zero crossing detector.
7. What is the difference between Comparator and a ~~stable~~ Schmitt trigger.
8. Draw the circuit diagram of an Astable multivibrator using op-amp.
9. Mention the applications of a Sample and hold circuit.
10. How the Noninverting amplifier can be used as a voltage to current converter

## UNIT - 3

1. what are the advantages of Active filters over passive filters.
2. Draw the frequency response characteristic of various filters
3. How electric filters can be classified.
4. what is meant by frequency scaling technique.
5. what is a notch filter.
6. Draw the circuit diagram of an Allpass filter.
7. Design an active Butterworth LPF with a cutoff freq of  $2\text{kHz}$  and passband gain of 2.
8. write short notes on three terminal voltage regulators.
9. what is the roll off rate of a first order filter.
10. why do we use higher order filters? what is a Sallen-key filter.

## UNIT - 4

- ① what are the important features of a 555IC timer.
- ② Draw the pin configuration of a 555IC.
- ③ what is meant by ON load and OFF load
- ④ Give methods for obtaining Symmetrical Square wave.
- ⑤ Explain the function of Reset pin in 555IC
- ⑥ Define duty cycle 'D' of timer in astable mode.
- ⑦ Mention some applications of timer in monostable mode.
- ⑧ Design a Symmetrical square wave form generator of 10KHz.
- ⑨ Draw the circuit of a Schmitt trigger using 555 timer and explain its operation.
- ⑩ How is an astable multivibrator connected into a PPM (Pulse position modulation).

## UNIT - 5

- ① Define Resolution, linearity, accuracy of a DAC
- ② List the various A/D conversion techniques
- ③ Which is the fastest ADC and why?
- ④ What is the disadvantage of the dual slope ADC
- ⑤ What are the disadvantages of weighted resistor Digital to analog converter (DAC)
- ⑥ The basic step of a 9 bit DAC is  $10.3\text{ mV}$ . If 000000000 represents 0V, what output is produced if the input is 101101111?
- ⑦ How many levels are possible in a two-bit DAC? What is the effective resolution if the output range is 0 to 3V.
- ⑧ Draw the block diagram of a PLL (phased locked loop).
- ⑨ Define Lock-in-Range, capture range, pull-in-time of a PLL.
- ⑩ Draw the pin configuration of 566 IC which is used as a VCO (Voltage controlled oscillator).

Code No: RR-310404

III B.Tech I-Semester Regular Examinations, November 2004

## LINEAR IC APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours

Max Marks: 80

Answer any FIVE questions

All questions carry equal marks

1. a) What are the different linear IC packages?  
b) What is the input impedance of a non-inverting op-amp amplifier?  
c) Design an inverting amplifier with an input resistance of  $10K\Omega$  and a gain of -5.
2. a) Explain the effect of frequency on the behavior of the virtual ground in an inverting configuration of an op-amp.  
b) Mention some applications of an instrumentation amplifier.
3. a) What is the effect of finite gain of the op-amp on the output of an active integrator?  
b) Design a differentiator that will differentiate an input signal with  $f_{max}=100 \text{ Hz}$ .
4. a) Design a first order high pass filter at a cutoff frequency of 400Hz and a pass band gain of 1.  
b) What is the Butter worth response?
5. Write short notes on:  
a) Frequency of oscillation of a square wave generator.  
b) Triangular wave generator using a square wave generator.
6. Draw the functional diagram of a 555 times IC and explain the function of each internal block to obtain astable multivibrator operation.
7. a) Explain the operation of an op-amp based weighted resistor Digital to Analog Converter through a neat circuit diagram.  
b) Design a 4-bit weighted resistor DAC whose full-scale output voltage is -10Volts. Assume  $R_f = 10 \text{ k}\Omega$  logic '1' level as + 5volts and logic '0' level as 0 volts. What is the output voltage when the input is 1011.
8. a) Define the terms, 'Resolution', 'Linearity' and 'Conversion time' of an Analog to Digital converter.  
b) Describe in detail the operation of a dual slope Analog to digital converter.

###



Set No:

2

Code No: RR-310404

III B.Tech I-Semester Regular Examinations, November 2004  
LINEAR IC APPLICATIONS  
(Electronics and Communication Engineering)

Max. Marks: 80

Time: 3 hours

Answer any FIVE questions

All questions carry equal marks

1. a) Explain the open loop and closed loop operations of an op-amp.  
b) Explain different methods to increase the input resistance of an op-amp.
2. a) What are the advantages of instrumentation amplifier? Derive an expression for the transfer function of an instrumentation amplifier.  
b) Explain the use of reference terminal provided in an integrated circuit instrumentation amplifiers.
3. a) Design a practical integrator circuit to process the sinusoidal input waveform up to 1 KHz. The input amplitude is 10mv.  
b) What are the different modes of operation of an active integrator?
4. a) What is an all pass filter? Where and why is it needed?  
b) Design and obtain the frequency response of a band pass filter with  $f_L = 400\text{Hz}$ ,  $f_H = 1\text{KHz}$  and the pass band gain = 1.
5. Write short notes on:
  - a) Sawtooth waveform generator
  - b) Voltage-to-Frequency converter.
6. a) Draw the block schematic of 555 times IC.  
b) Derive an expression for the output pulse width 'T' when the timer is operated in a stable multivibrator configuration.
7. a) Explain the operation of a multiplying DAC and mention its applications.  
b) A 12-bit D to A converter has a full-scale range of 15 volts. Its maximum differential linearity error is  $\pm \frac{1}{2} \text{ LSB}$ .
  - i) What is the percentage resolution?
  - ii) What are the minimum and maximum possible values of the increment in its output voltage?
8. a) Define the terms 'Aperture time' and 'Droop rate' of a sample & hold circuit.  
b) With a neat circuit diagram explain the operation of an OP-amp based sample & hold circuit.  
c) Indicate one monolithic sample & hold IC of any manufacturer.

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27

Code No: RR-310404

**III B.Tech I-Semester Regular Examinations, November 2004**  
**LINEAR IC APPLICATIONS**  
**(Electronics and Communication Engineering)**

Time: 3 hours

Max. Marks: 80

Answer any FIVE questions  
 All questions carry equal marks

---

1. a) Define common mode rejection ratio (CMRR)? Explain why  $CMRR \rightarrow \infty$  for an emitter coupled differential amplifier where  $R_E \rightarrow \infty$ .  
 b) Why is cascade configuration used in an op-amp?  
 c) Explain with the figures how two supply voltages  $V^+$  and  $V^-$  are obtained from a single supply.
2. a) Explain with a neat circuit diagram the working of voltage to current converter with floating load.  
 b) Design a circuit to convert a 4 mA-to 20mA input current to a 0V-to-10V output voltage. The circuit is powered from  $\pm 15V$  regulated supplies.
3. a) In the differentiator circuit the input is a sine wave with a peak-to-peak amplitude of 3V at 200 Hz. Sketch the output waveform.  
 b) Determine the output voltage produced by the cascaded integrator at  $t = 0.5$  sec.
4. a) A certain narrow band-pass filter has been designed to meet the following specification:  $f_C = 2\text{KHz}$ ,  $Q = 20$ , and  $A_F = 10$ . What modifications are necessary in the filter design to change  $f_c$  to 1KHz keeping gain and bandwidth constant?  
 b) What are the advantages of active filter over passive ones?
5. Write short notes on:  
 a) Asymmetric square wave generator.  
 b) Monostable multivibrator.
6. a) Draw the block schematic of a 566 voltage controlled oscillator IC.  
 b) Derive an expression for the voltage to frequency conversion factor of 566 VCO.
7. a) Explain how the deficiencies of weighted resister type DAC can be overcome through an R-2R ladder type network. Explain the conversion procedure in R-2R ladder type DAC  
 b) The logic levels used in an 8-bit R-2R ladder type DAC are logic '1' = +5 volts and logic '0' = 0 volts. Find the output voltage for an input of 10110110.
8. a) Define the terms 'Accuracy' and 'settling time' of an Analog to Digital converter.  
 b) Explain in detail with a neat circuit diagram the operation of a parallel comparator type Analog to Digital converter.

# # #

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**III B.Tech I-Semester Regular Examinations, November 2004**  
**LINEAR IC APPLICATIONS**  
**(Electronics and Communication Engineering)**

Time: 3 hours

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Answer any FIVE questions  
 All questions carry equal marks

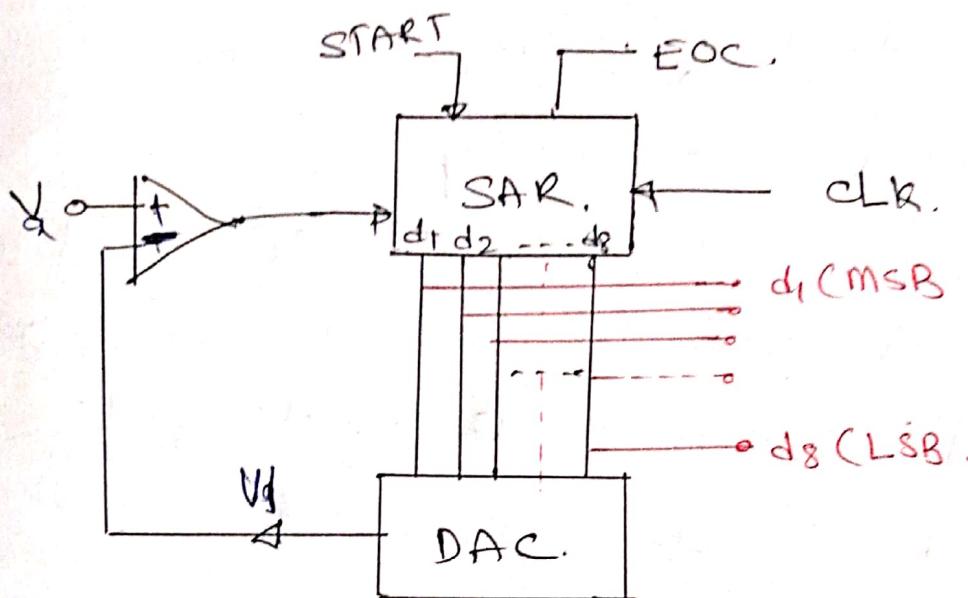
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1. a) Explain how the input off-set voltage compensated for?  
 b) How fast can the output of an op-amp change by 10V, if its slew rate is  $1V/\mu s$ .  
 c) Define thermal drift.
2. a) With the help of a neat circuit diagram explain the working of a logarithmic amplifier.  
 b) Derive the output voltage of an antilog amplifier.
3. a) Discuss important characteristics of a comparator and the limitations of op-amps as comparators.  
 b) Explain the operation of Schmitt trigger circuit.
4. a) For the all-pass filter, determine the phase shift  $\phi$  between the input and output at  $f = 2\text{KHz}$ . To obtain a positive phase shift  $\phi$ , what modifications are necessary in the circuit?  
 b) What is a pass band and a stop band for a filter? How are filters classified?
5. Write short notes on the operation of any two:  
 a) Quadrature oscillator      b) RC phase shift oscillator  
 c) Wien- bridge oscillator.
6. a) Draw the block schematic of a PLL describing the function of each block briefly.  
 b) What is the purpose of low pass filter in a phase locked loop? Describe different types of law pass filters used in a PLL.
7. a) Explain the basic technique utilized in Digital to Analog conversion using suitable mathematical expressions.  
 b) In an inverted R-2R ladder type Digital to Analog Converter  $R = 10k\Omega$   $V_{REF} = +20$  volts. Find the current in each  $20 k\Omega$  resister and the maximum current passing into the feedback resistor of the op-amp.
8. a) Define the terms 'Resolution', 'Conversion time' and 'Linearity' of an Analog to Digital converter.  
 b) Indicate the fastest Analog to Digital converter specifying its conversion time with a representative example.  
 c) What is the resolution of a 11 bit Analog to Digital converter for a full scale input voltage of 10.24 volts?

# SUCCESSIVE APPROXIMATION

(1)

## CONVERTER



## Functional diagram of the Successive Approximation ADC

- \* The successive approximation technique uses a very efficient code search strategy to complete  $n$ -bit conversion in just  $n$ -clock periods.
- \* An eight bit converter would require eight clock pulses to obtain a digital output.

The circuit uses a successive approximation register (SAR) to find the required value of each bit by trial and error. The circuit operates as follows:

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with the arrival of the START Command the trial code is 10000000. The output  $V_d$  of the DAC is now compared with analog input  $V_a$ . If  $V_a$  is greater than the DAC, if  $V_d$  is greater than the DAC output  $V_d$  is less than the ~~10000000~~ 10000000 in the corrected digital representation.

The MSB is left at '1' and the next lower significant bit is made 1 and further tested.

However if  $V_a$  is less than the DAC output, then 10000000 is greater than the corrected digital representation. So reset MSB to '0' and go on to next lower significant bit.

This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested.

Whenever the DAC output crosses  $V_a$  the comparator changes state and thus can be taken as the end of conversion (EOC).

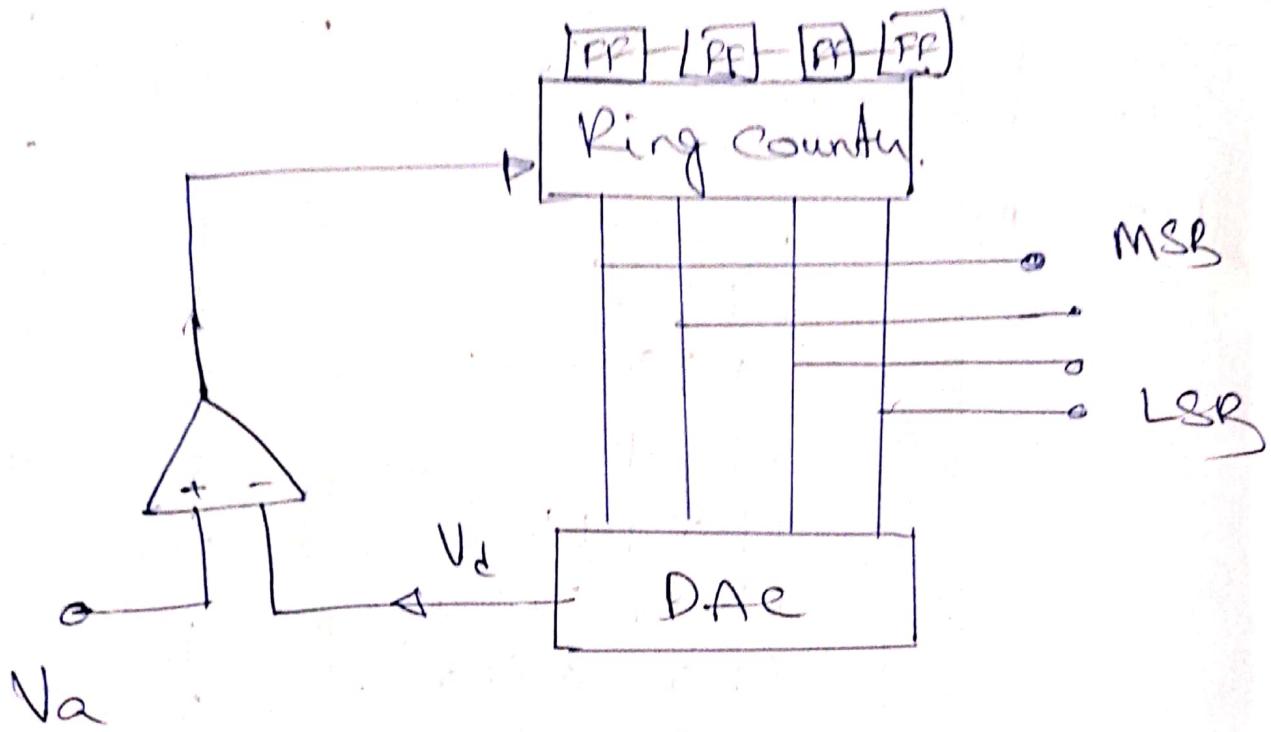
Correct representation	Successive approximation register output $V_d$ at different stages in conversion	Comparator out
11010100	1 0000000	1
	1 1000000	1
	1 1100000	0
	1 1010000	1
	1 1011000	0
	1 1010100	1
	1 1010110	0
	1 1010101	0
	1 1010100	0

It can be seen that the D/A output voltage becomes successively closer to the actual analog I<sub>pp</sub> voltage. It requires eight pulses to establish the accurate output regardless of the value of the analog I<sub>pp</sub>.

one additional clock pulse is used to load the output register and reinitialize the clk.

4-bit Successor appr.

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1st clock  
puls

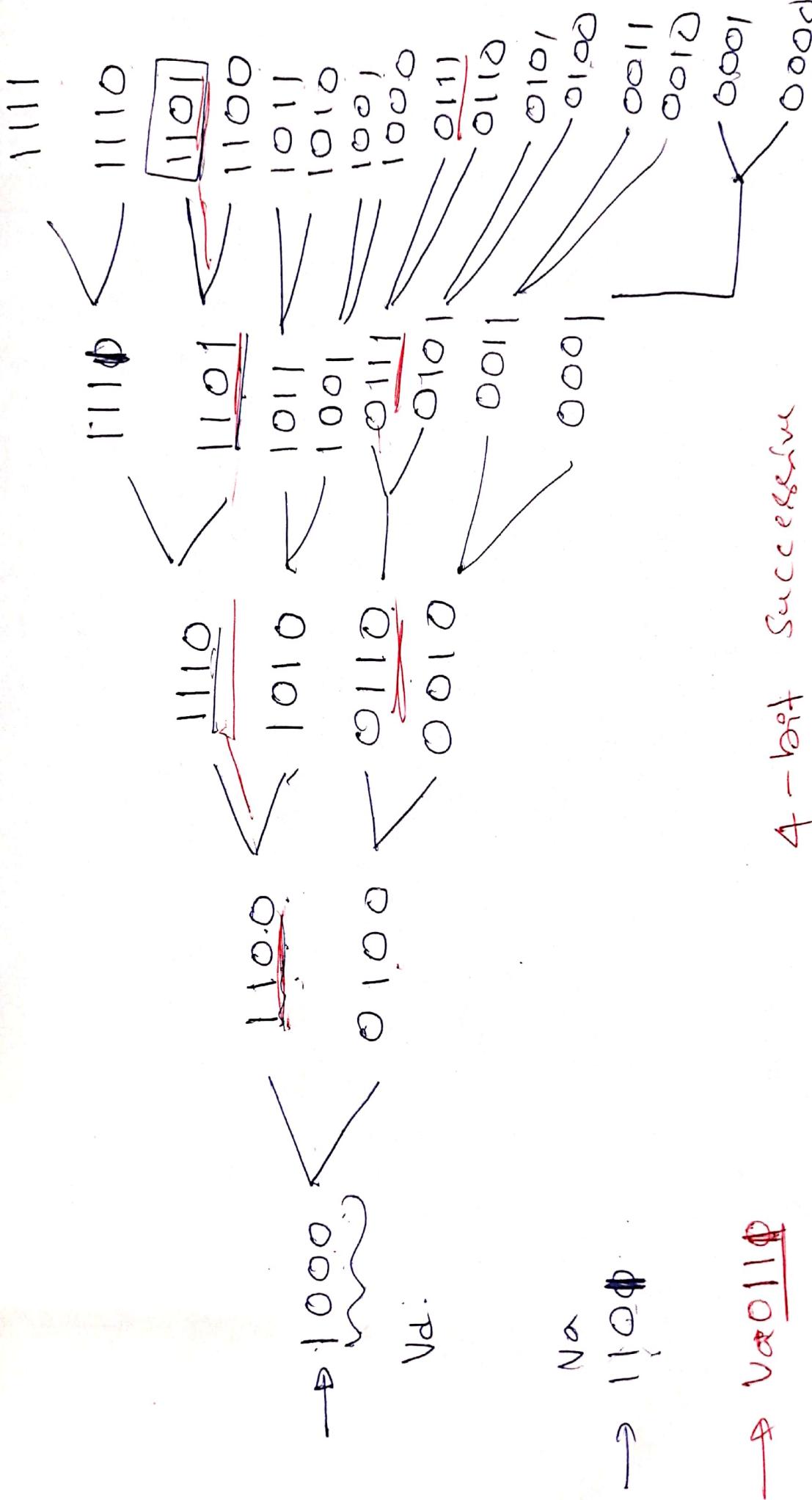
1 0 0 0

2nd clk 0 1 0 0

3rd clk 0 0 1 0

4th clk. 0 0 0 1

⑤



## Specification of DACs & ADES ⑥

### ① Resolution-

The resolution of a converter is the smallest change in voltage which may be produced at the output of the converter.

For example, an 8-bit D/A Converter has  $2^m - 1 = 255$  equal intervals. Hence the smallest change in the output voltage is  $(1/255)$  of the full scale output range.

$$\text{Resolution in mV} = \frac{V_{FS}}{2^m - 1} = \frac{1LSB}{2^m}$$

Resolution is stated in no of ways.

An 8-bit DAC is said to have

: 8-bit resolution

: a resolution of 0.392 Percent of full scale.

: a resolution of 1 part in 255.

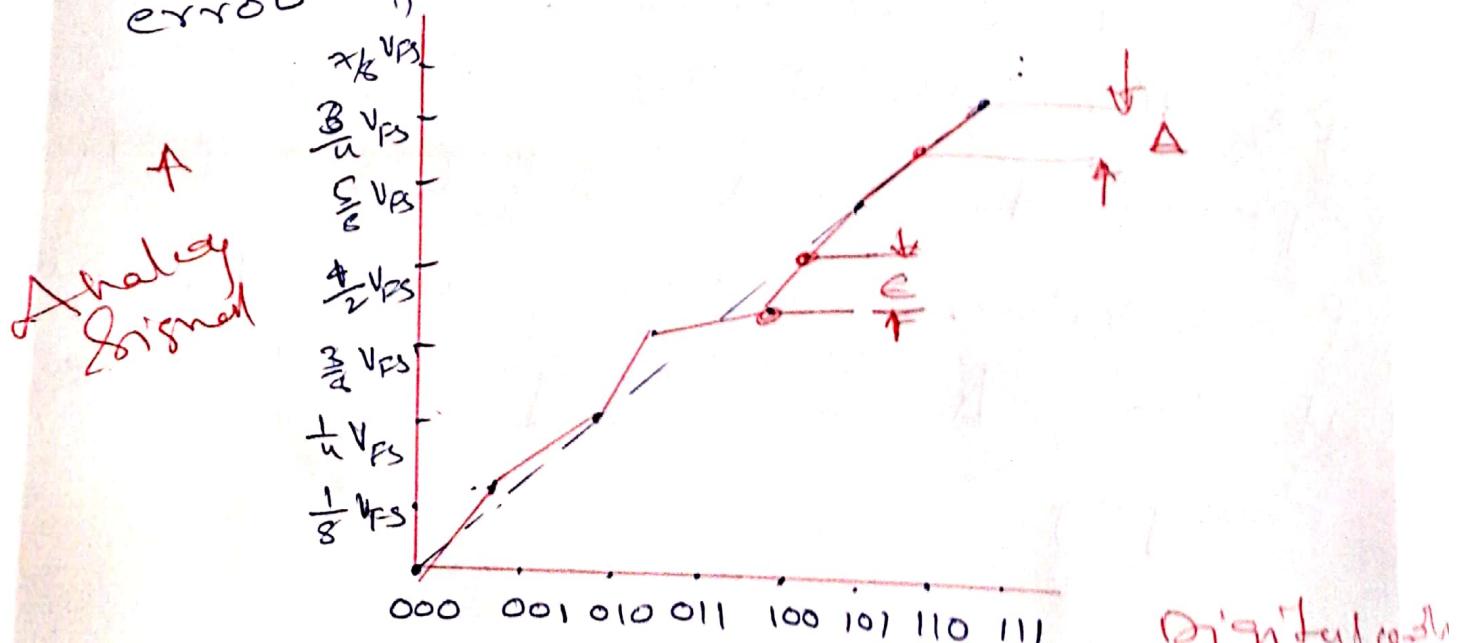
# Resolution for 6-16 bit DACs ⑦

Bits	Intervals	LSB size (% of full scale)	LSB size (10V Fullscale)
6	63	1.588%	158.8mV.
8	255	0.392%	39.2mV.
10	1023	0.0978%	9.78mV.
12	4095	0.0244%	2.44mV.
14	16383	0.0061%	0.61mV.
16	65535	0.0015%	0.15mV.

Similarly, the resolution of an A/D converter is defined as the smallest change in ~~the~~ analog I/p for a one bit change at the o/p.

Linearity : The linearity of an A/D or D/A converter is an important measure of its accuracy, and tells how close the converter O/p is to its ideal transfer characteristic. In an ideal DAC, equal increment in the digital I/p should produce equal increment in the analog output and the transfer curve should be linear.

The linearity error measures the deviation of the actual O/p from the fitted line and is given by  $\epsilon/\Delta$ . The error is usually expressed as a fraction of LSB increment or percentage of full scale voltage. A good converter exhibits a linearity error of less than  $\pm \frac{1}{2}$  LSB.



Absolute Accuracy - Accuracy is the maximum deviation between the actual converted output and the ideal converted output.

Relative accuracy is the maximum deviation after gain and offset errors have been removed.

Data sheets normally specify relative accuracy rather than absolute accuracy.

The accuracy of a converter is also specified in terms of LSB increments or percentage of full scale voltage.

### settling time

The most important dynamic parameter is the settling time. It represents the time it takes for the output to settle within specified band  $\pm \frac{1}{2}$  LSB of its final value following a code change at the IP (usually a full scale change).

It depends upon the switching time of the logic circuitry due to internal parasitic capacitances and inductances. Settling time ranges from 100ns to 10usec depending on word length and type of circuit used.

