

Counter Basics and Asynchronous counter

A special type of sequential circuit used to count the pulse is known as a counter, or a collection of flip flops where the clock signal is applied is known as counters.

The counter is one of the widest applications of the flip flop. Based on the clock pulse, the output of the counter contains a predefined state. The number of the pulse can be counted using the output of the counter.

Truth Table

Clock	Counter output		State number	Decimal counter output
	Q _B	Q _A		
Initially	0	0	-	0
1 st	0	1	1	1
2 nd	1	0	2	2
3 rd	1	1	3	3
4 th	0	0	4	0

There are the following types of counters:

- Asynchronous Counters(Ripple counter) or(serial counter)
- Synchronous Counters(Parallel counter)

Synchronous counter	Asynchronous counter
Have a common clock for all the flip flops.	No common clock for all the flip flops In Asynchronous counter, for the first flip flop We need to apply clock. Output of First flip flop is given as the clock for the next flip flop
All flip flops change their states simultaneously	All flip flops won't change their states simultaneously

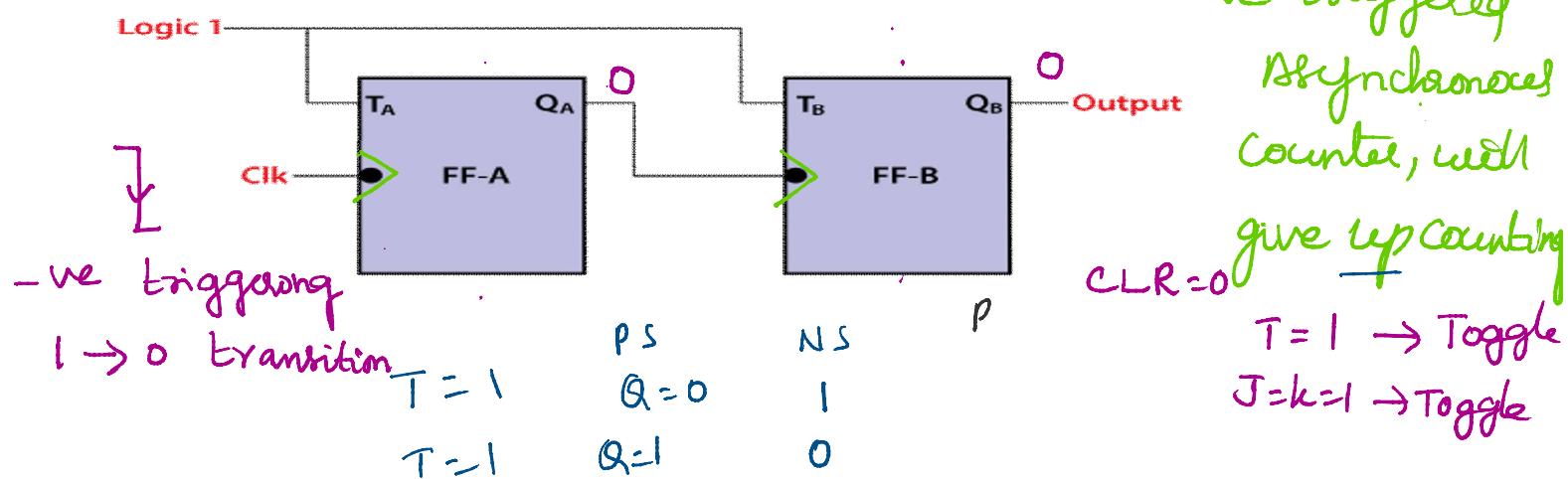
Asynchronous or ripple counters

The **Asynchronous counter** is also known as the **ripple counter**. Below is a diagram of the 2-bit **Asynchronous counter** in which we used two T flip-flops. Apart from the T flip flop, we can also use the JK flip flop by setting both of the inputs to 1 permanently.

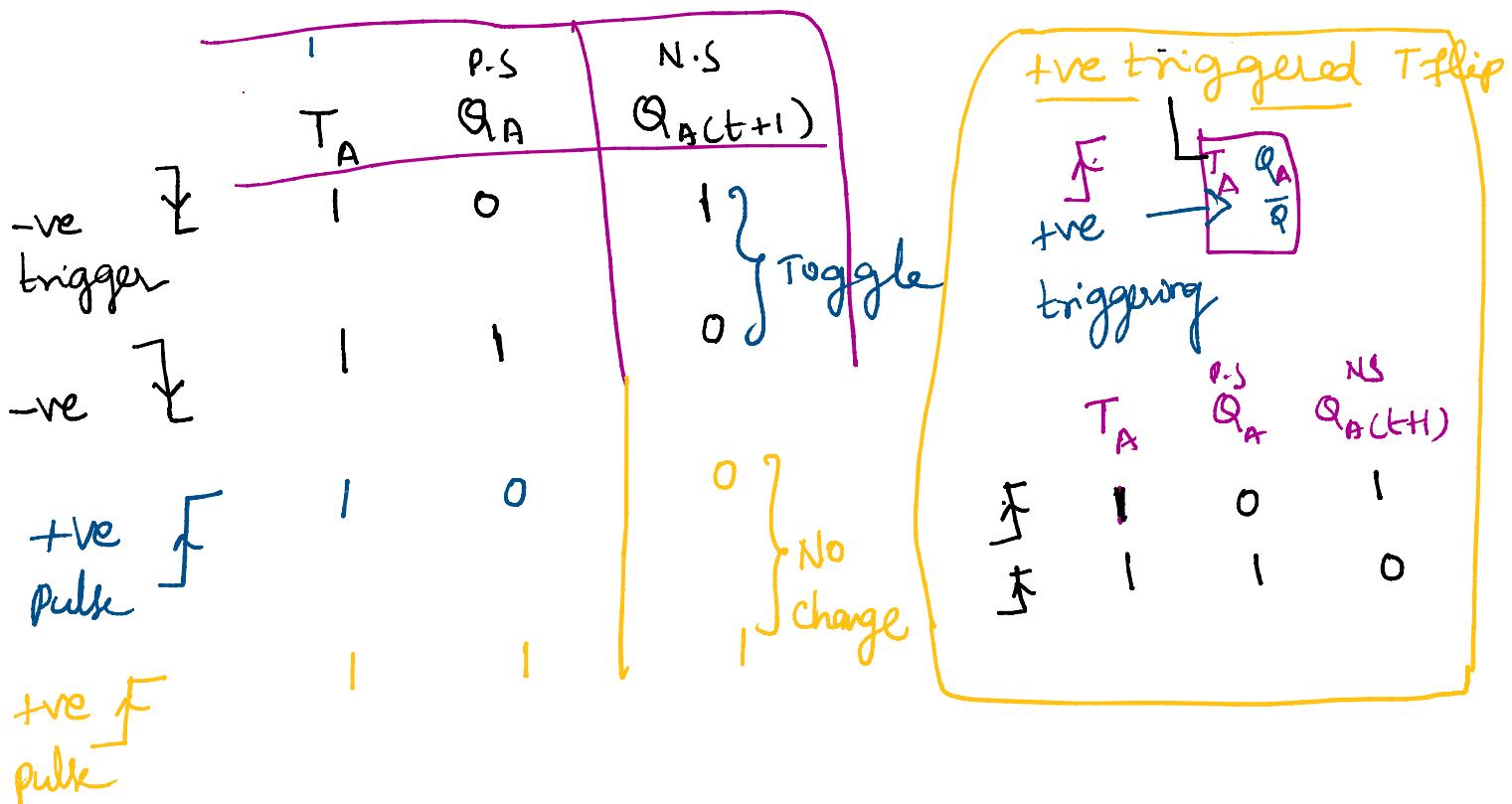
The external clock pass to the clock input of the first flip flop, i.e.,

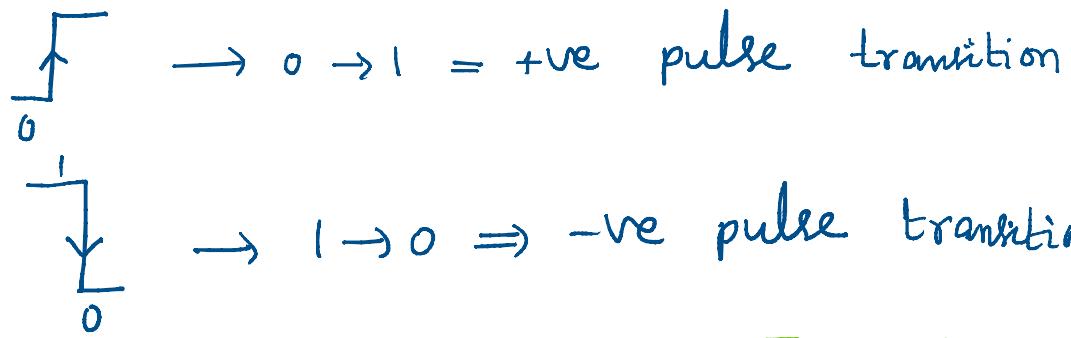
FF-A and its output, i.e., is passed to clock input of the next flip flop, i.e., FF-B.

Block Diagram



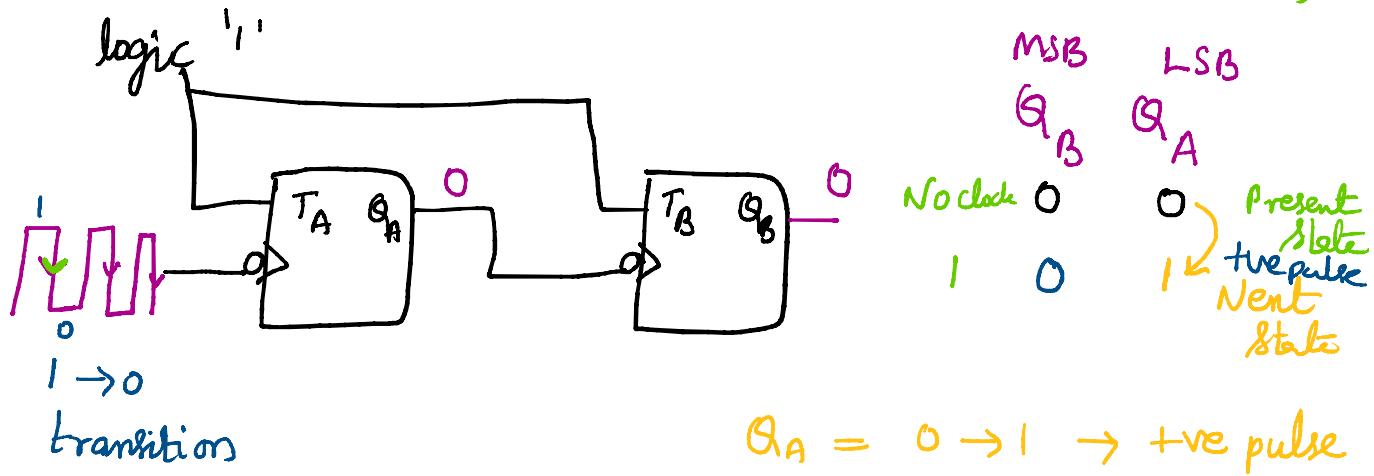
-ve triggered T flip flop





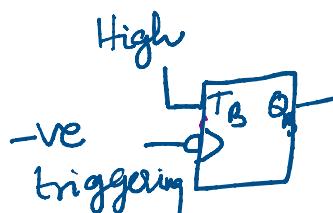
$\rightarrow 1 \rightarrow 0 \Rightarrow -ve$ pulse transition

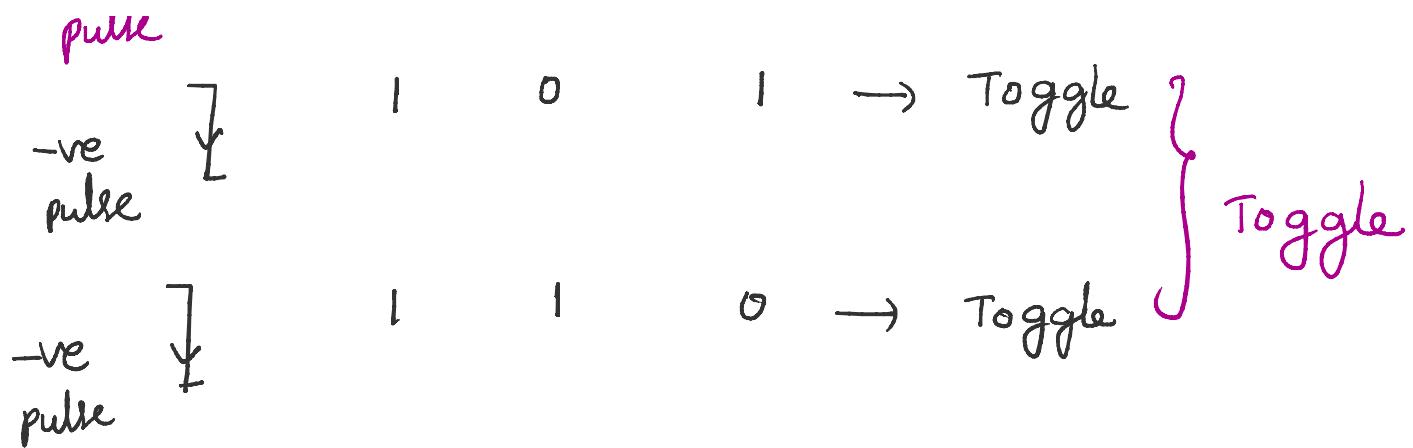
$$T_A = 1, Q_A = 0 \Rightarrow Q_{A(t+1)} = 1$$



-ve triggered T flip flop

	T_B	Q_B	$Q_{B(t+1)}$	
+ve pulse	F	1	0 → 0	{ No change state
+ve pulse	F	1	1 → 1	{ Toggle ?





① clock is applied to FF-A (first flip flop)

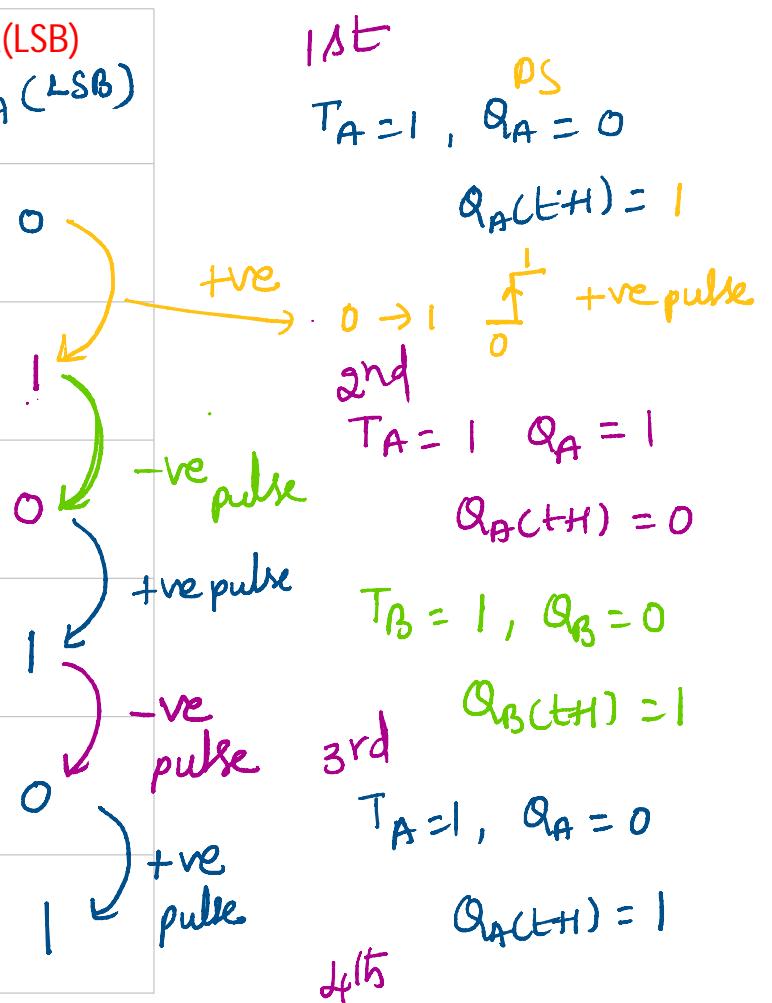
② output of FF-A (Q_A) = clock of FF-B

Since the flip flop is -ve edge triggered
 flip flop will toggle only when Q_A makes
 transition $1 \rightarrow 0$

No other transitions ($0 \rightarrow 0$, $0 \rightarrow 1$, $1 \rightarrow 1$) has no effect

Note :- A standard Asynchronous counter can be realized by JK flip flop (or) T flip flop
 but not by SR (or) D flip flop

No. of negative edge Clock pulses	QB(MSB) $Q_B(\text{MSB})$	QA(LSB) $Q_A(\text{LSB})$
NO clock	0	0
1	0	0
2	1	0
3	1	1
4	0	0
5	0	1



① Q_A changes for every negative triggered clock pulse

② Q_B changes whenever Q_A transition is from $1 \rightarrow 0$

1. **Condition 1:** When both the flip flops are in reset condition.

Operation: The outputs of both flip flops, i.e., Q_A Q_B , will be 0.

2. **Condition 2:** When the first negative clock edge passes.

Operation: The first flip flop will toggle, and the output of this flip flop will change from 0 to 1. The output of this flip flop will be taken by the clock input of the next flip flop. This output will be taken as a positive edge clock by the second flip flop. This input will not change the second flip flop's output state because it is the negative edge triggered flip flop.

So, $Q_A = 1$ and $Q_B = 0$

3. **Condition 3:** When the second negative clock edge is applied.

Operation: The first flip flop will toggle again, and the output of this flip flop will change from 1 to 0. This output will be taken as a negative edge clock by the second flip flop. This input will change the second flip flop's output state because it is the negative edge triggered flip flop.

So, $Q_A = 0$ and $Q_B = 1$.

4. **Condition 4:** When the third negative clock edge is applied.

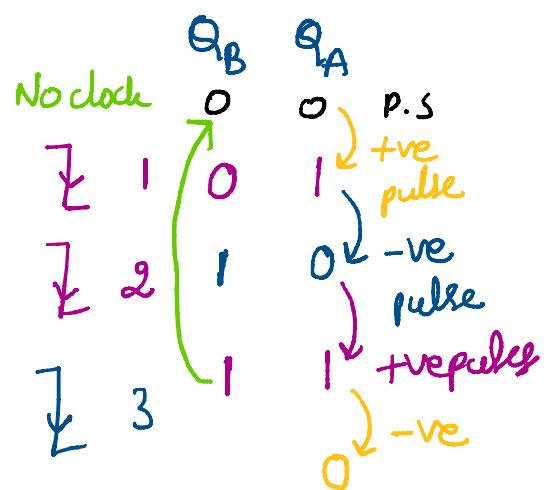
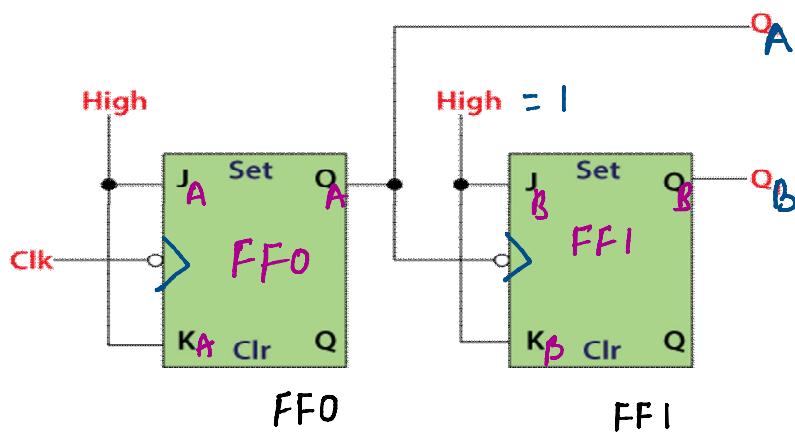
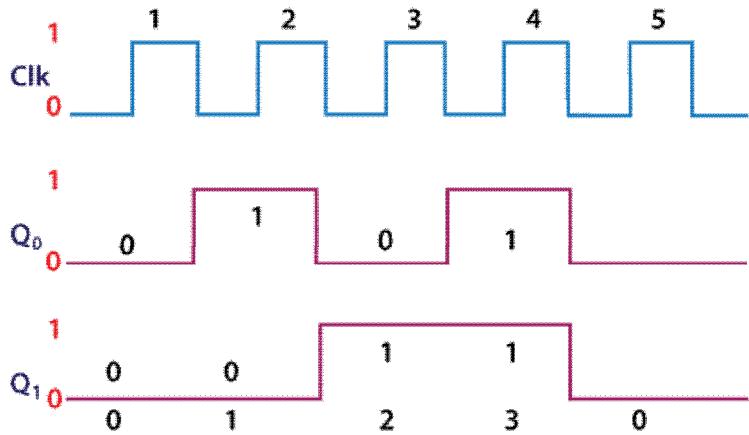
Operation: The first flip flop will toggle again, and the output of this flip flop will change from 0 to 1. This output will be taken as a positive edge clock by the second flip flop. This input will not change the second flip flop's output state because it is the negative edge triggered flip flop.

So, $Q_A = 1$ and $Q_B = 1$

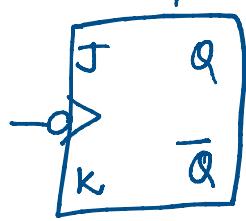
5. **Condition 5:** When the fourth negative clock edge is applied.

Operation: The first flip flop will toggle again, and the output of this flip flop will change from 1 to 0. This output will be taken as a negative edge clock by the second flip flop. This input will change the output state of the second flip flop.

So, $Q_A = 0$ and $Q_B = 0$



-ve triggered JK flip flop



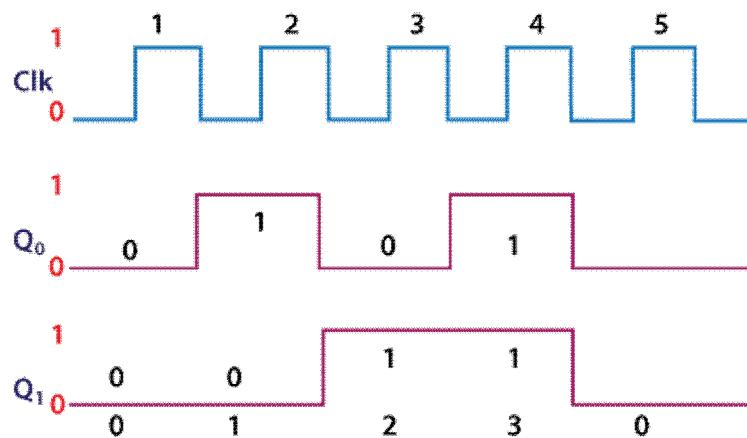
	clock	J	K	Q	$Q(t+1)$
F	+ve	0	0	0	0
F	+ve	0	1	1	1
J	+ve	1	0	0	0
F	+ve	1	1	0	0
J	+ve	1	1	1	1
		0	0	0	0 → NC
J	-ve	1	1	0	1 } Toggle
J	-ve	1	1	1	0
J	-ve	0	1	0	0 } Reset
J	-ve	0	1	1	0
J	-ve	1	0	0	1 } Set
J	-ve	1	0	1	1 } State

The table shows the state transitions of a -ve triggered JK flip flop. The columns represent the clock edge (F for falling edge, J for rising edge), the J input, the K input, the current Q state, and the next state Q(t+1). The rows show various combinations of inputs and clock edges. Annotations include:

- A yellow bracket groups the first four rows (F+ve, J+ve, F+ve, J+ve) with a curly brace labeled "No change state".
- A yellow bracket groups the next two rows (J-ve, J-ve) with a curly brace labeled "Toggle".
- A curly brace on the right side groups the last four rows (J-ve, J-ve, J-ve, J-ve) with labels "Reset" and "Set state" respectively.
- A curly brace on the far right groups the last two rows (J-ve, J-ve) with a label "State".
- A yellow bracket groups the last two rows (J-ve, J-ve) with a label "No change state".
- A curly brace on the far right groups the last two rows (J-ve, J-ve) with a label "No change state".

- ① clock applied to FFO
 - ② output of FF_{i-1} = clock of FF_i
- Since here flip flops are negative edge triggered
for asynchronous upcounter operation.
- ③ flip flop will toggle only when Q_{i-1} makes transition $1 \rightarrow 0$
 - ④ No other transitions ($0 \rightarrow 0$, $0 \rightarrow 1$, $1 \rightarrow 1$) have no effect

Signal Diagram



Operation

1. **Condition 1:** When both the flip flops are in reset condition.
Operation: The outputs of both flip flops, i.e., Q_A Q_B , will be 0.
2. **Condition 2:** When the first negative clock edge passes.
Operation: The first flip flop will toggle, and the output of this flip flop will change from 0 to 1. The output of this flip flop will be taken by the clock input of the next flip flop. This output will be taken as a positive edge clock by the second flip flop. This input will not change the second flip flop's output state because it is the negative edge triggered flip flop.
So, $Q_A = 1$ and $Q_B = 0$

- 3. Condition 3:** When the second negative clock edge is applied.

Operation: The first flip flop will toggle again, and the output of this flip flop will change from 1 to 0. This output will be taken as a negative edge clock by the second flip flop. This input will change the second flip flop's output state because it is the negative edge triggered flip flop.

So, $Q_A = 0$ and $Q_B = 1$.

- 4. Condition 4:** When the third negative clock edge is applied.

Operation: The first flip flop will toggle again, and the output of this flip flop will change from 0 to 1. This output will be taken as a positive edge clock by the second flip flop. This input will not change the second flip flop's output state because it is the negative edge triggered flip flop.

So, $Q_A = 1$ and $Q_B = 1$

- 5. Condition 5:** When the fourth negative clock edge is applied.

Operation: The first flip flop will toggle again, and the output of this flip flop will change from 1 to 0. This output will be taken as a negative edge clock by the second flip flop. This input will change the output state of the second flip flop.

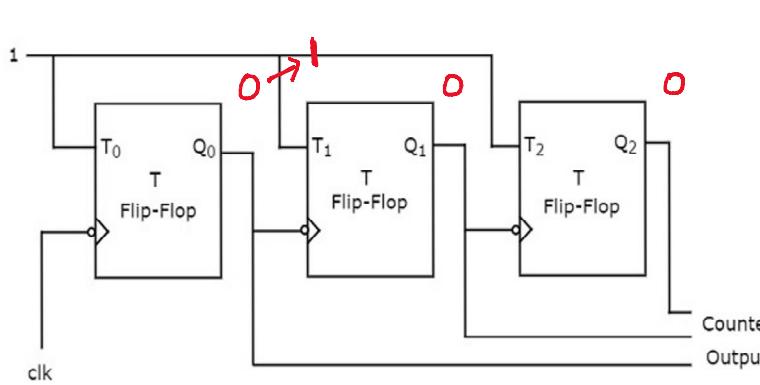
So, $Q_A = 0$ and $Q_B = 0$

3 bit Asynchronous Binary Up Counter (Mod 8 up counter)

$$\begin{aligned} N &= 3 \\ 2^N - 1 &= 2^3 - 1 = \underline{\underline{0101}} \end{aligned}$$

An 'N' bit Asynchronous binary up counter consists of 'N' T flip-flops.

It counts from 0 to $2^N - 1$. The block diagram of 3-bit Asynchronous binary up counter is shown in the following figure.



clock	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

Annotations on the right side of the table:

- Row 1: +ve pulse (red)
- Row 2: -ve pulse (blue)
- Row 3: +ve pulse (purple)
- Row 4: -ve pulse (red)
- Row 5: +ve pulse (blue)
- Row 6: +ve pulse (purple)
- Row 7: -ve pulse (red)
- Row 8: -ve pulse (blue)

The 3-bit Asynchronous binary up counter contains three T flip-flops and the T-input of all the flip-flops are connected to '1'. All these flip-flops are negative edge triggered but the outputs change asynchronously. The clock signal is directly applied to the first T flip-flop. So, the output of first T flip-flop toggles for every negative edge of clock signal.

The output of first T flip-flop is applied as clock signal for second T flip-flop. So, the output of second T flip-flop toggles for every negative edge of output of first T flip-flop.

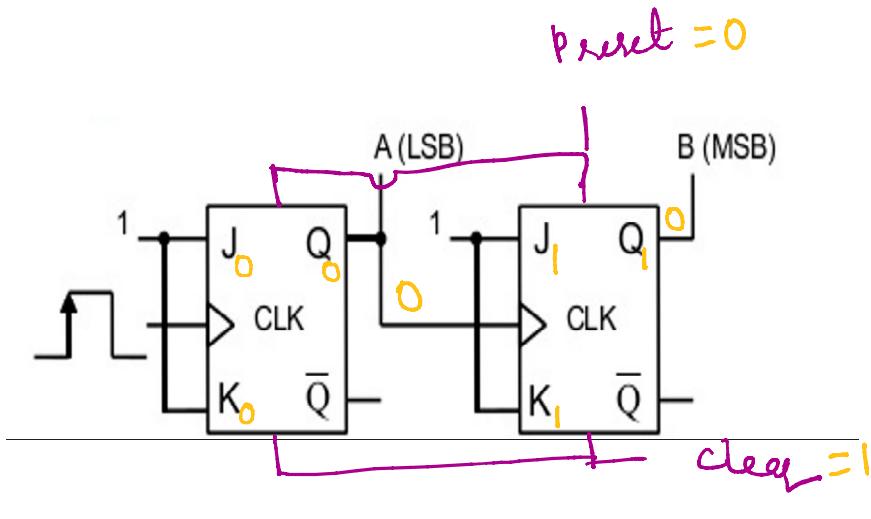
Similarly, the output of third T flip-flop toggles for every negative edge of output of second T flip-flop, since the output of second T flip-flop acts as the clock signal for third T flip-flop.

Assume the initial status of T flip-flops from rightmost to leftmost is Q2Q1Q0=000. Here, Q2 & Q0 are MSB & LSB respectively. We can understand the working of 3-bit asynchronous binary counter from the following table.

No of negative edge of Clock	Q2(MSB)	Q1	Q0(LSB)
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

1. Here Q0 toggled for every negative edge of clock signal.
2. Q1 toggled for every Q0 that goes from 1 to 0, otherwise remained in the previous state.
3. Similarly, Q2 toggled for every Q1 that goes from 1 to 0, otherwise remained in the previous state.

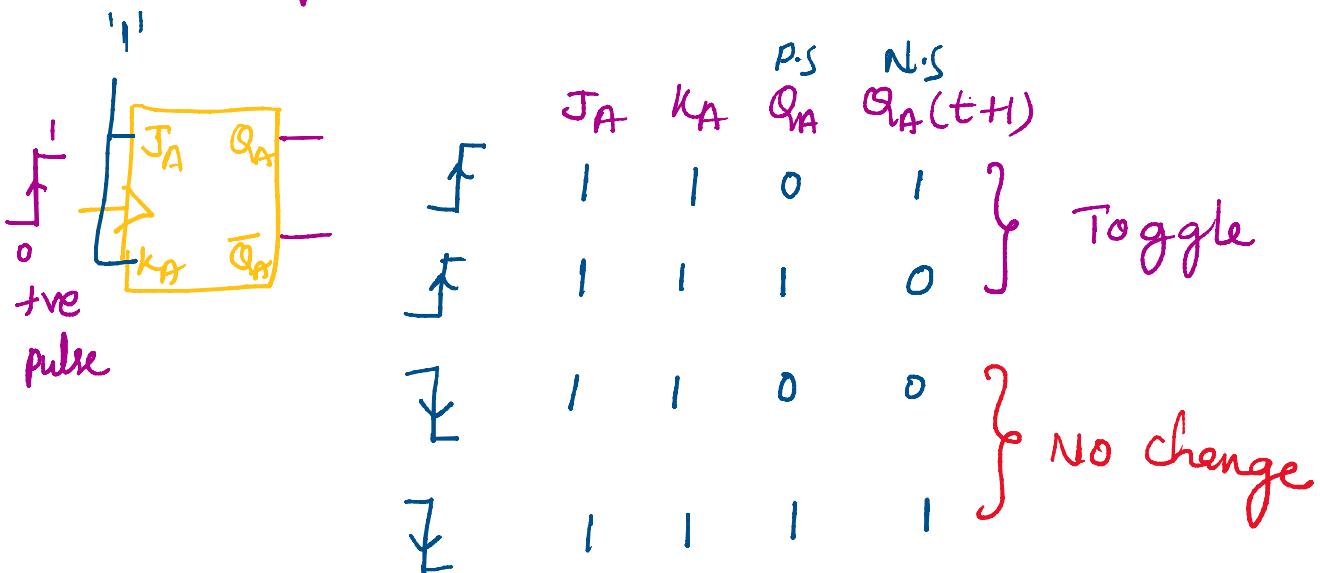
The initial status of the T flip-flops in the absence of clock signal is Q2Q1Q0=000. This is incremented by one for every negative edge of clock signal and reached to maximum value at 7th negative edge of clock signal. This pattern repeats when further negative edges of clock signal are applied.



Initially clear all flip flops using Asynchronous i/p

Active high
Asynchronous
 $Preset = 0$
 $clear = 1$

+ve triggered JK flip flop



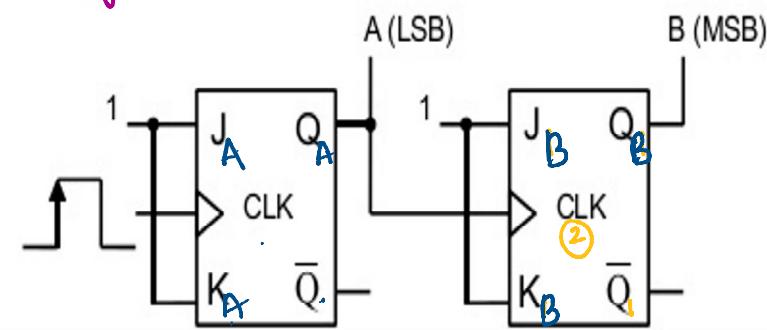
+ve triggering means 0 to 1 transition

-ve triggering means 1 to 0 transition

Asynchronous down counter design, we

Asynchronous down counter design, we must +ve triggered clock pulse.

2 bit Asynchronous Down Counter (Mod 4 down counter)



	clock		Q_B	Q_A
No clock	0	0		
\uparrow ①	1	1	1	0
\uparrow ②	1	0	0	1
\uparrow ③	0	1	1	0
\uparrow ④	0	0	0	1

P.S +ve pulse

-ve pulse

+ve pulse

-ve pulse

