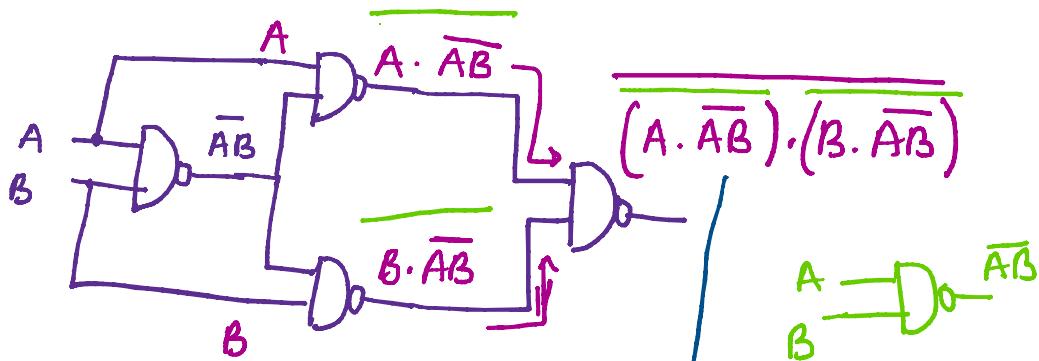


# NAND and NOR Realization

Implementation of EX-OR gate using NAND



$$\text{EX-OR} \rightarrow A \oplus B = \bar{A}B + A\bar{B}$$

$$\begin{aligned} & (A \cdot \bar{A}B) \cdot (B \cdot \bar{A}\bar{B}) \\ & \quad \text{① } A \quad \text{② } B \\ & (A \cdot \bar{A}B) + (B \cdot \bar{A}\bar{B}) \end{aligned}$$

$$\bar{A} \cdot \bar{B} = \bar{A} + \bar{B}$$

$$\therefore \bar{\bar{A}} = A$$

$$A \cdot \bar{A}B + B \cdot \bar{A}\bar{B}$$

$$\bar{A}B(A+B)$$

$$(\bar{A}+\bar{B})(A+B)$$

$$\bar{A} \cdot A + \bar{A}B + \bar{B}A + \bar{B} \cdot \bar{B}$$

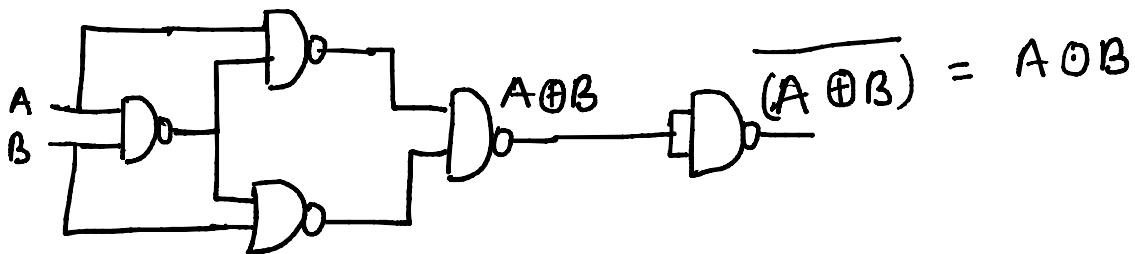
$$\therefore \bar{B} \cdot B = 0$$

$$\therefore \bar{A} \cdot A = 0$$

$\bar{A}B + A\bar{B}$   
EX-OR gate needs 4 NAND gate

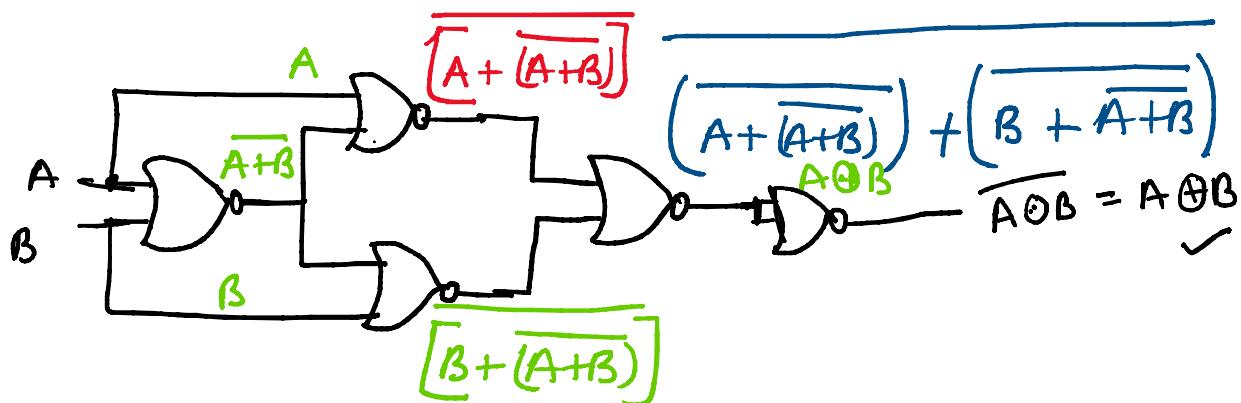
Implementation of EX-NOR gate using NAND

$$\text{EX-NOR} \rightarrow A \ominus B = \overline{A \oplus B}$$



To design Ex-NOR, we need 5 minimum NAND gate

### Implementation of Ex-OR gate using NOR gates



$$\overline{\left( \overline{A + \overline{A+B}} \right)} + \overline{\left( \overline{B + \overline{A+B}} \right)}$$

$$A \cdot B$$

$$\overline{A + \overline{A+B}} \cdot \overline{B + \overline{A+B}}$$

$$A + (\overline{A+B}) \cdot B + \overline{A+B}$$

$$A + (\overline{A} \cdot \overline{B}) \cdot B + (\overline{A} \cdot \overline{B})$$

$$(A + \overline{A}) (A + \overline{B}) \cdot (\overline{A} + B) \cdot (B + \overline{B})$$

$$(A + \overline{B}) (\overline{A} + B)$$

$$\therefore = \perp \Delta \perp \perp \overline{A \cdot B} + B \cdot \overline{B}$$

$$\because \overline{A + B} = \overline{A} \cdot \overline{B}$$

$$\therefore \overline{\overline{A}} = A$$

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

$$\therefore A \cdot \overline{A} = 0$$

$$(A + \bar{B})(\bar{A} + B) = A \cdot \bar{A} + AB + \bar{A} \cdot \bar{B} + \underbrace{\bar{B} \cdot \bar{B}}_0$$

$\therefore A \cdot \bar{A} = 0$   
 $\therefore \bar{B} \cdot \bar{B} = 0$

$$= AB + \bar{A} \bar{B}$$

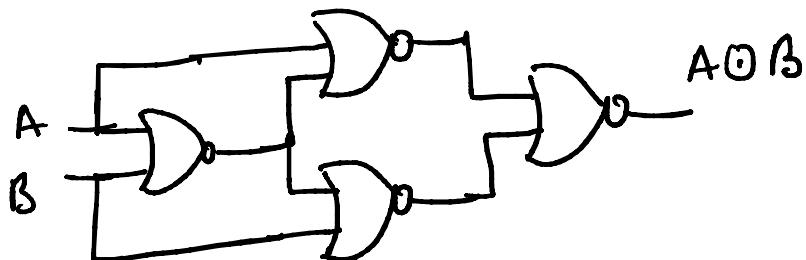
EX-NOR

$$\overline{AB + \bar{A} \bar{B}} = \bar{A} B + A \bar{B}$$

EX-OR

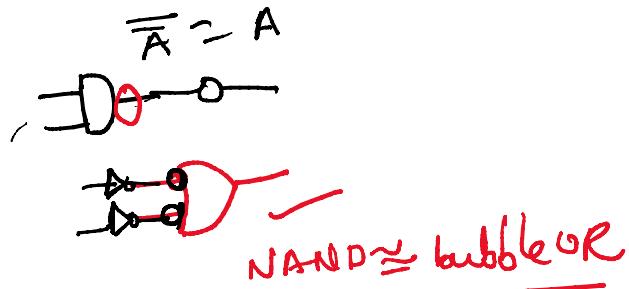
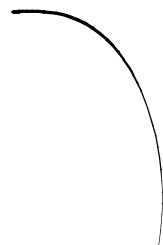
To design EX-OR using NOR gates, we need '5' NOR gates

### Implementation of EX-NOR using NOR gates

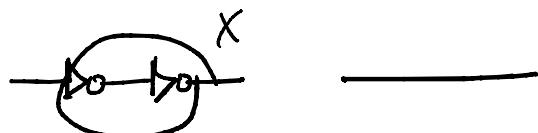


'4' NOR gates are sufficient to design EX-NOR

### NAND Realization



1. Implement given function using basic gates.
2. Convert AND to NAND gates with AND invert symbol
3. Convert OR to NAND gates with bubbled OR symbol
4. Where ever received an Inverter (step 2 and step 3)  
followed by inverter use another inverter
5. Double inversions cancel out



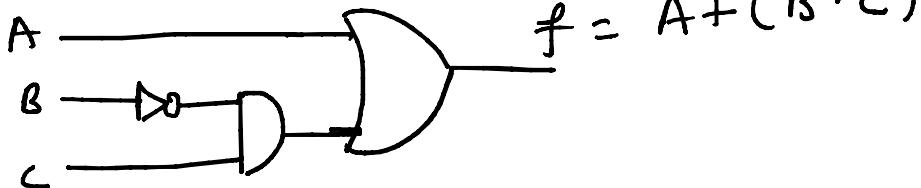
$$f = A + (\bar{B} \cdot C)$$

↑ OR      AND

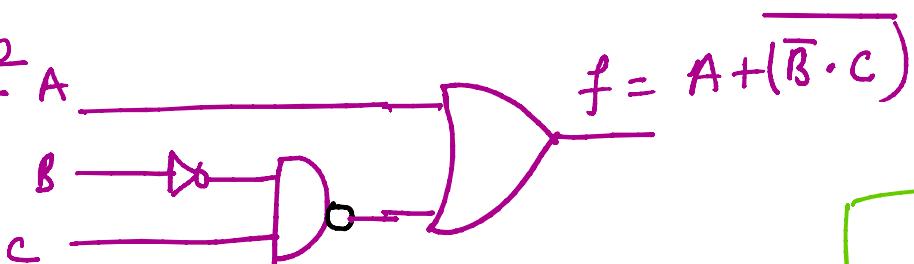
i NOT  
i AND  
i OR

Basic

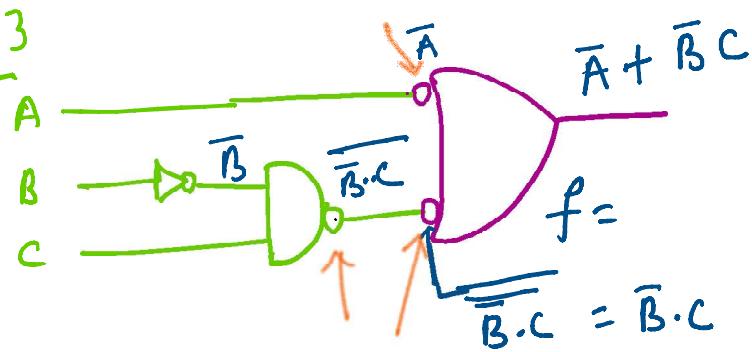
Step 1



Step 2



Step 3



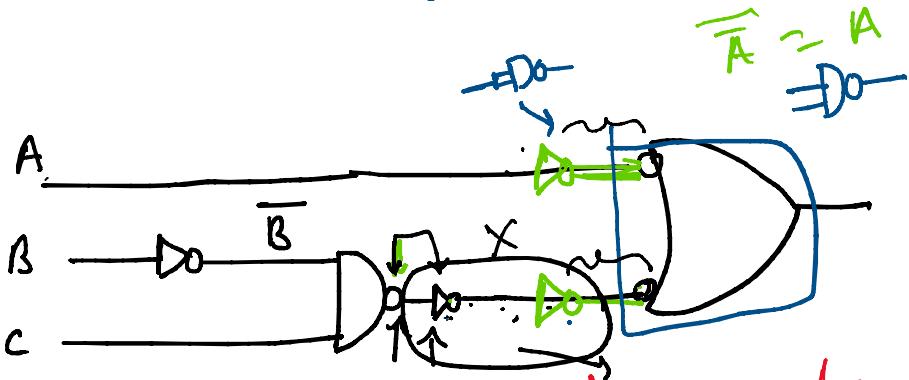
$$\bar{AB} = \bar{A} + \bar{B}$$

$\neg \neg \equiv$

A diagram showing a NAND gate with inputs A and B. The output is labeled  $\neg \neg$ . To its right is an equivalent circuit consisting of an AND gate followed by an inverter. The inputs to the AND gate are labeled  $\bar{A}$  and  $\bar{B}$ . The output of the AND gate is connected to the inverter.

NAND is equivalent to  
bubbled OR

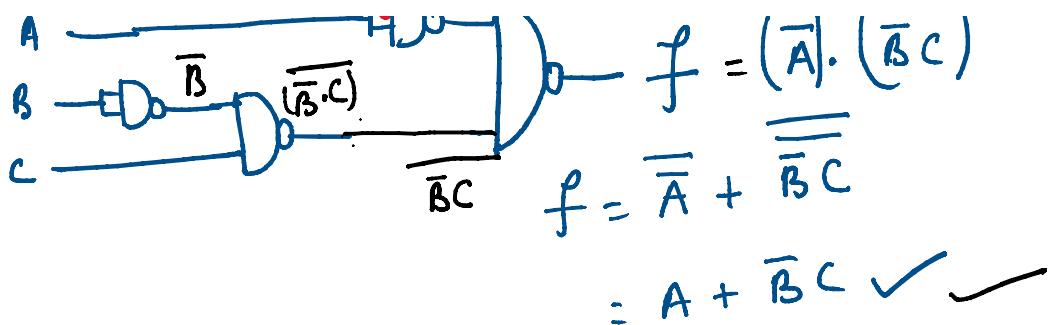
Step 4



Step 5

to replace bubbled OR gate  
by NAND and inverter by  
single 3p NAND gate





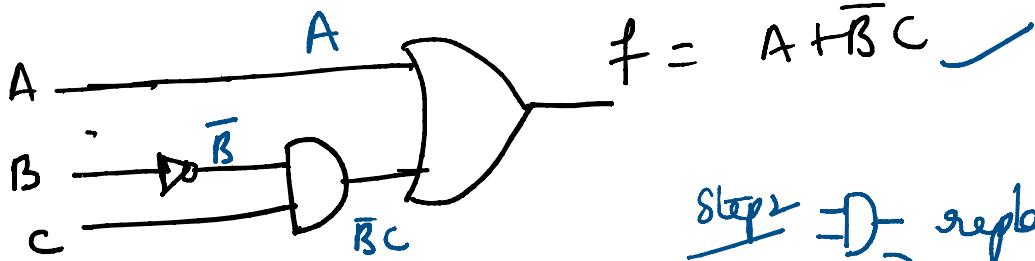
### NOR Realization

1. Implement given function using basic gates.
2. Convert AND to NOR gates with bubbled input AND symbol
3. Convert OR to NOR gates with OR followed by invert symbol
4. Where ever received an Inverter (step 2 and step 3) followed by inverter use another inverter.

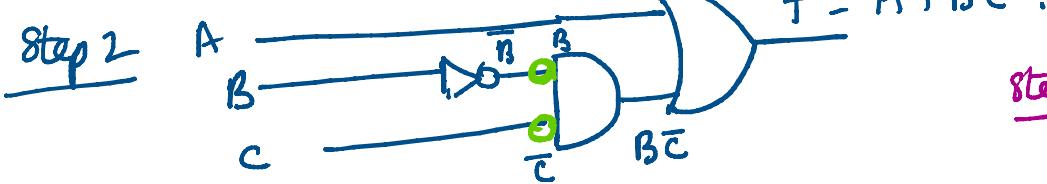
5. Double inverters can be cancelled out

$$f(A, B, C) = A + \bar{B}C \text{ using only NOR gates}$$

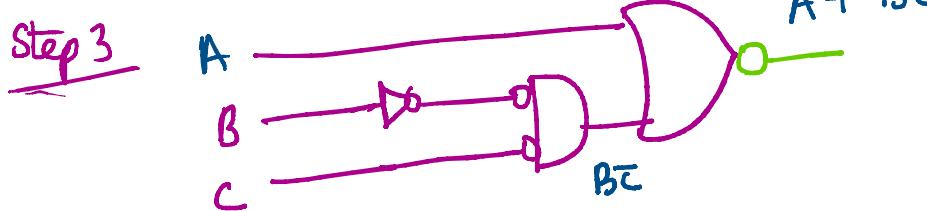
Step 1



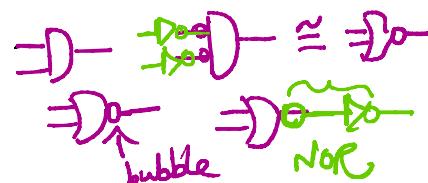
Step 2  $\Rightarrow$  replaced by



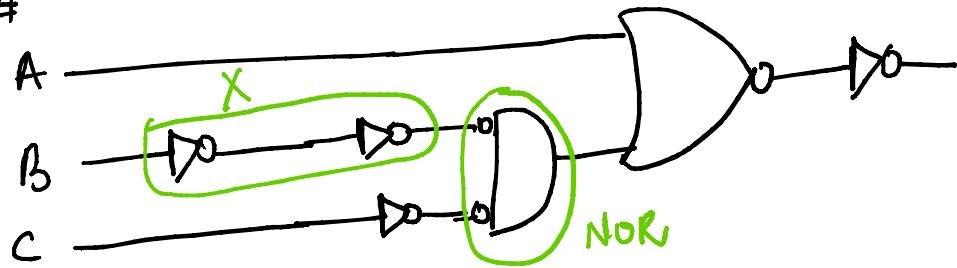
Step 3 OR gate replaced by NOR gate



Step 4

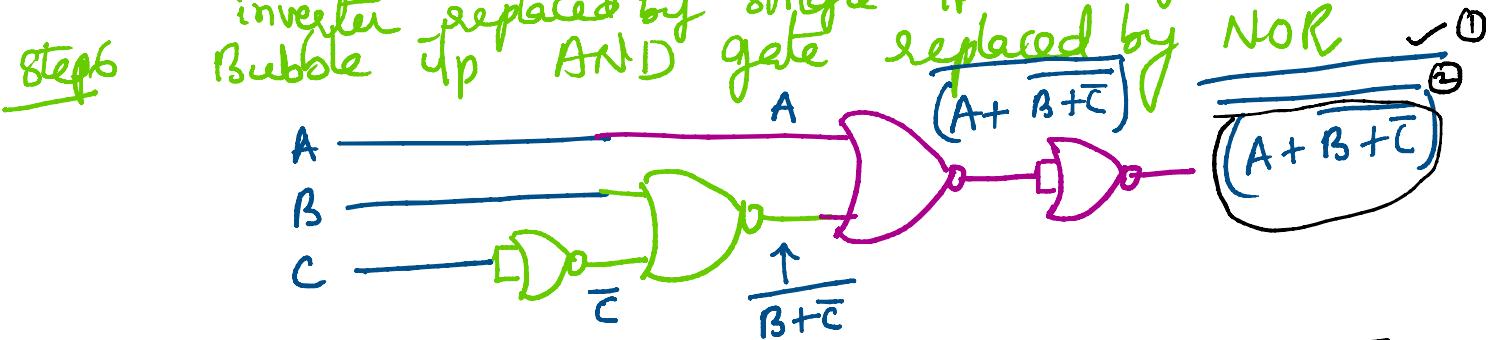


Step 4



Step 5 Double inversions Cancel out

inverter replaced by single up NOR gate  
Bubble up AND gate replaced by NOR



$$\begin{aligned} & A + \overline{B + \overline{C}} \\ & A + \overline{B} \cdot \overline{\overline{C}} \\ & A + \overline{B} \cdot C \quad \checkmark \end{aligned}$$

$$\begin{aligned} \overline{A+B} &= \overline{A} \cdot \overline{B} \\ \overline{\overline{C}} &= C \end{aligned}$$

① Design  $B + A\overline{B}C$  using minimum no. of NAND gates

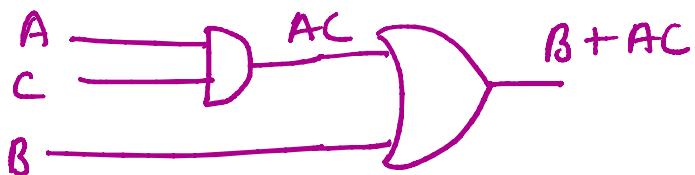
$$B + \overline{B} AC$$

$$A + \overline{A} B = A + B$$

$$f = B + AC \quad \checkmark$$

$$B + \overline{B} AC = B + AC$$

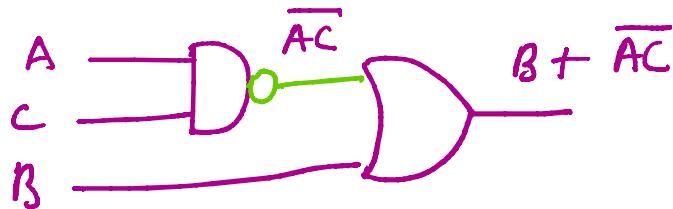
Step 1 Design using basic gates



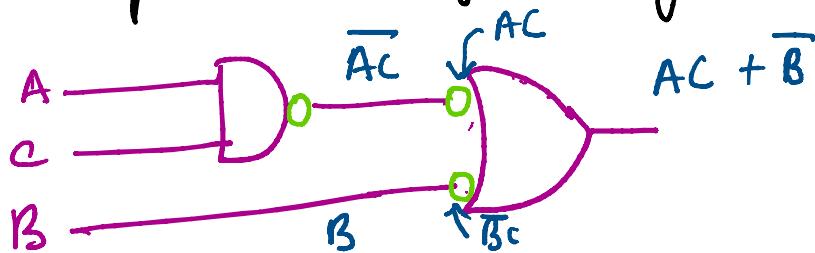
$B \rightarrow$

step 2 Replace AND gate by NAND

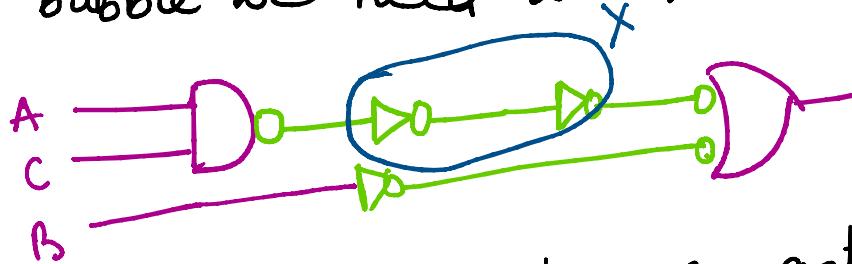
AND + NOT



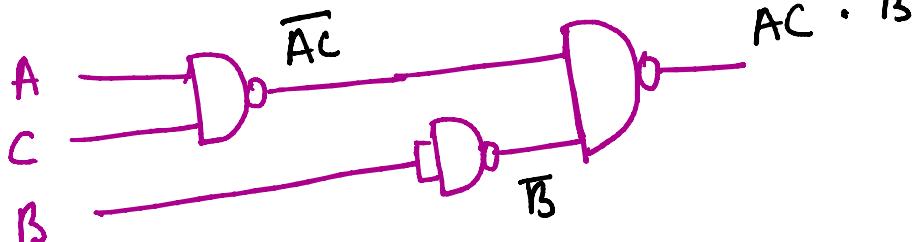
step 3 Replace OR gate by bubble if OR gate



step 4 whenever, we received bubble followed by bubble we need to use NOT (inverter)  $\overline{\overline{A}} = A$



step 5 Replace bubble if OR gate by NAND and NOT by single if NAND



$$\begin{aligned} \overline{\overline{AC} \cdot \overline{B}} &\Rightarrow \overline{\overline{AC}} + \overline{\overline{B}} \\ &= AC + B \end{aligned}$$

$$\overline{AB} = \overline{A} + \overline{B}$$

$$\overline{\overline{A}} = A$$