

UNIT-I

Integrated Circuits

Integrated circuits (IC):-

- * An integrated circuit (IC) is a miniature, low cost electronic circuit consists of active and passive components fabricated together on a single crystal of silicon.
- * The active components are transistors and diodes and passive components are resistors and capacitors.

Advantages of integrated circuits:

1. Miniaturization [very small size] and hence increased equipment density.
2. cost is low.
3. Increased system reliability due to the elimination of soldered joints.
4. power consumption is low.
5. Highly matched devices to give high degree of accuracy.
6. The speed of operation is high.

Classification of IC's:-

Based on the applications the integrated circuits can be classified into two types

1. Linear or Analog IC

2. Digital IC

1. Analog IC:- Analog ICs such as sensors, power management circuits, and operational amplifiers work by processing continuous signals. They perform functions like amplification, active filtering, demodulation, mixing, etc.
2. Digital IC:- Digital integrated circuits can contain millions of logic gates, flip-flops, multiplexers, and other circuits in a few square millimeters.
 - * The small size of these circuits allows high speed, low power dissipation and reduced manufacturing cost.
 - * These digital ICs typically microprocessors, DSPs, and micro controllers work using binary mathematics to process "one" and "zero" signals.

Based on chip size and complexity the integrated circuits (IC) can be classified into:

1. small scale integration (SSI)
2. medium scale integration (MSI)
3. Large scale integration (LSI)
4. very Large scale integration (VLSI)
5. ultra large scale integration (ULSI)
6. Giant scale integration (GSI)

The chip size and level of integration depends on the no. of components to be fabricated on chip.

SNO	Technology	Year of Invention	Active device count	Typical Functions
1.	SSI (small scale Integration)	1960	1-100 Transistors/chip	Logic gates, flip flops, op-amps.
2.	MSI (medium scale Integration)	1966	100-1000 (100) subcircuit	Counters, Adders, MUX
3.	LSI (large scale Integration)	1971	1000-20,000 TTL CMOS 1976 1978 1980	8 bit microprocessor RAM, ROM
4.	VLSI (very large scale integration)	1980	20000 - 1M bit rate boost	16 bit M.P., 32 bit M.P.
5.	ULSI (Ultra large scale integration)	1990	1M - 10M SR (SR) no longer SR	special purpose processors, Sensors.
6.	GSI (Giant scale integration)	2000	(910) SR until >10M lawa	Embedded systems, System-on-chip.

Based on fabrication techniques the integrated circuits can be classified into

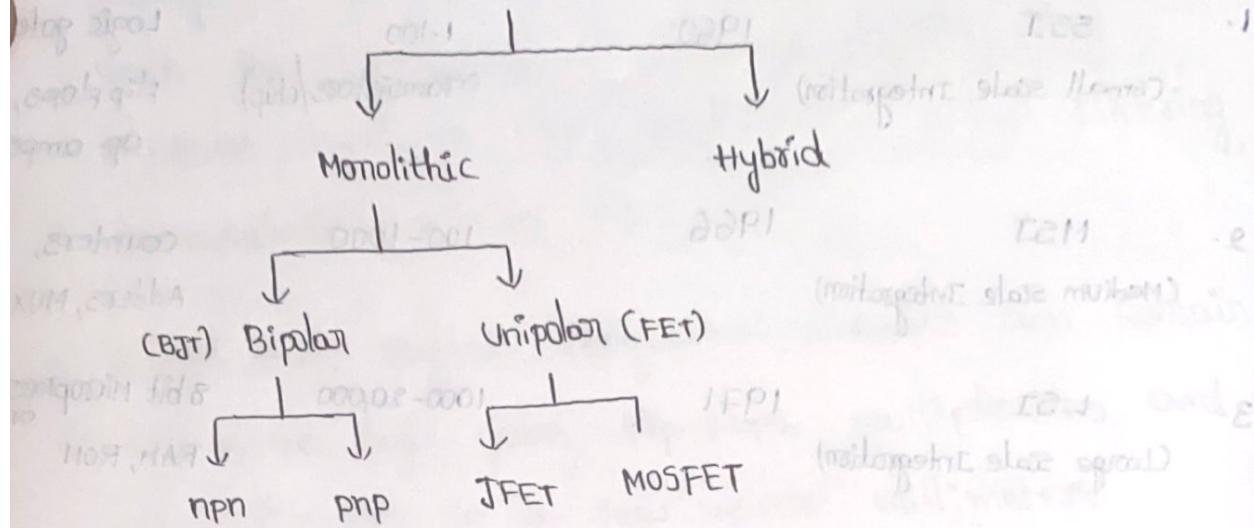
1. Monolithic IC
2. Hybrid IC

In Monolithic IC, all circuit components both active and passive elements connected in a single chip.

Based on requirement, in this ICs we are using Unipolar or Bipolar components like BJT or FET.

In hybrid IC, separate components are attached and interconnected by means of either

metallization pattern or, wire bonds - ie combining two or more ICs through wires.



Based on the packages the integrated circuits are classified into three types.

1. The metal can (TO) IC

2. Dual-in-line IC (DIP)

3. flat IC

1. The metal can (TO) IC :-

- * Available in 3, 5, 8, 10 & 12 pins.
- * Also called Transistor pack.
- * plane is effective for heat dissipation,

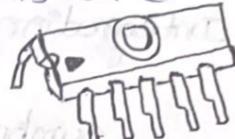
hence used in power amplifiers.



The Metal can IC

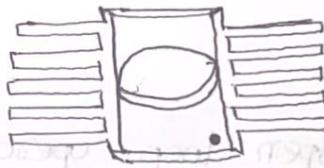
2. Dual-in-line IC:

- * popular for commercial applications.
- * chip mounted inside a plastic or ceramic case.
- * Easy to handle & mount, widely used.
- * Available with 12, 14, 16, 20, 40 pins etc.
- * 8pin DIP is called Mini-DIP.

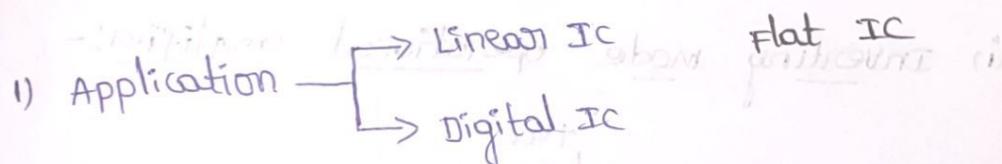


3. Flat IC:

- * used in the circuits where space is critical.
- * chip is enclosed in a rectangular ergonomic case.
- * terminals taken out through the sides and ends.



Classification of IC's



2) Integration

- SSI
- MSI
- LSI
- VLSI
- ULSI
- GSI

3) Fabrication Techniques

- Monolithic
- Hybrid

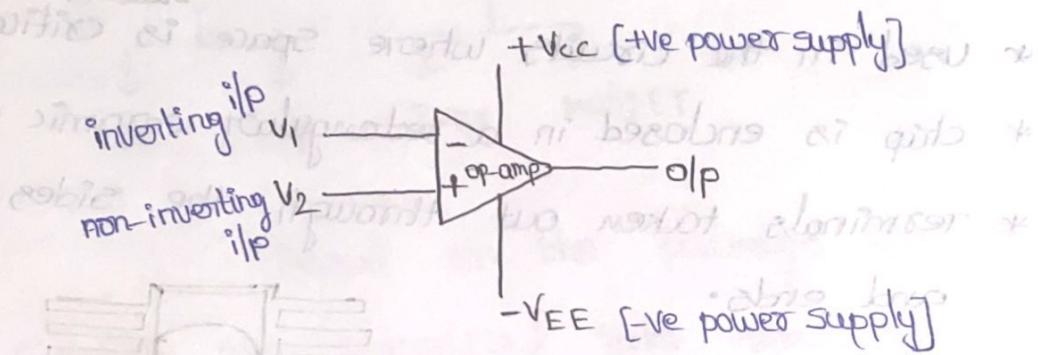
4) Packaging

- The Metal Can IC
- Dual-in-line IC
- Flat IC

* operational Amplifiers:-

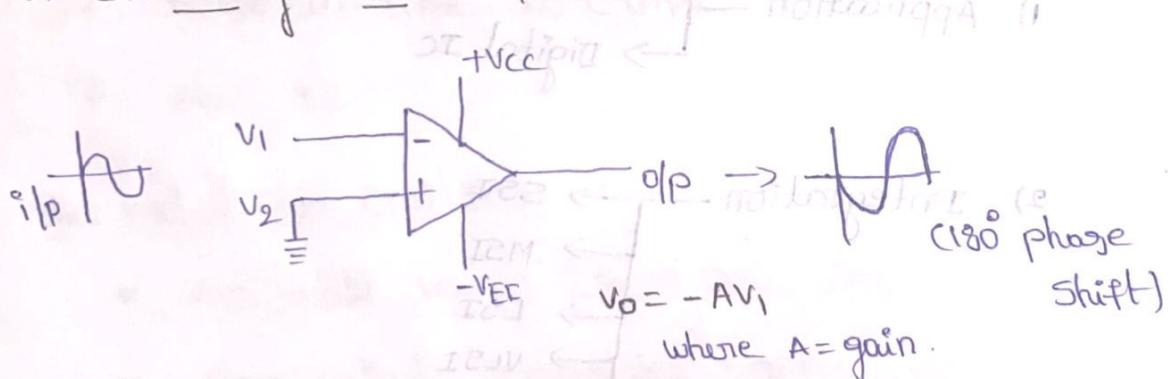
The operational amplifier is a high gain differential amplifier. It can do the multiple operations like Addition, subtraction, differentiation and integration.

symbol of operational amplifier:-

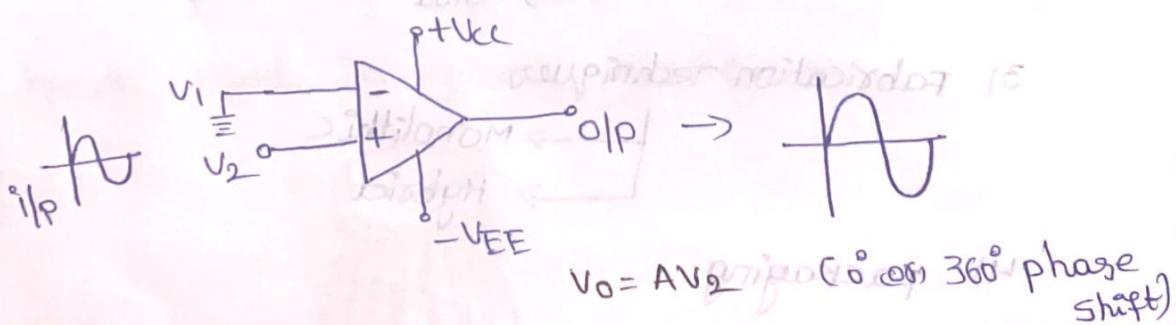


open loop operational amplifier:-

i) Inverting mode operational amplifier:-

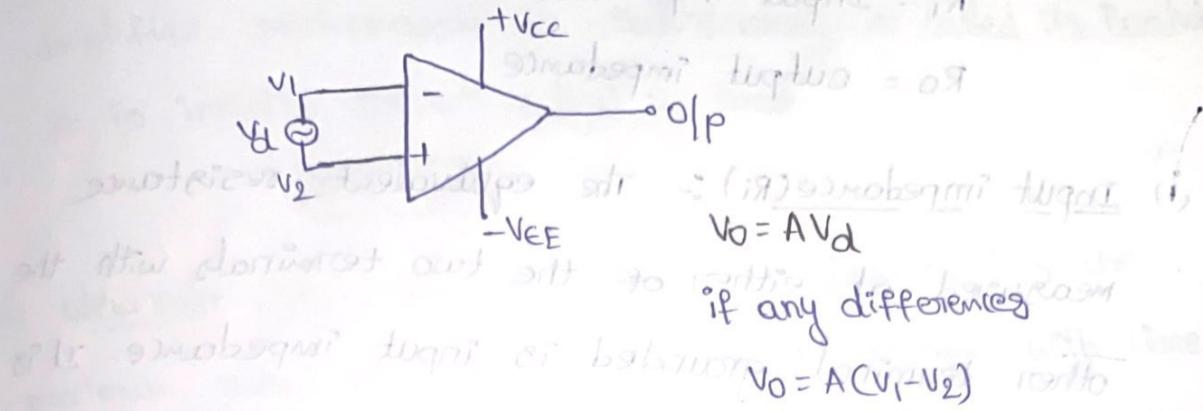


ii) Non-inverting mode operational amplifier:-

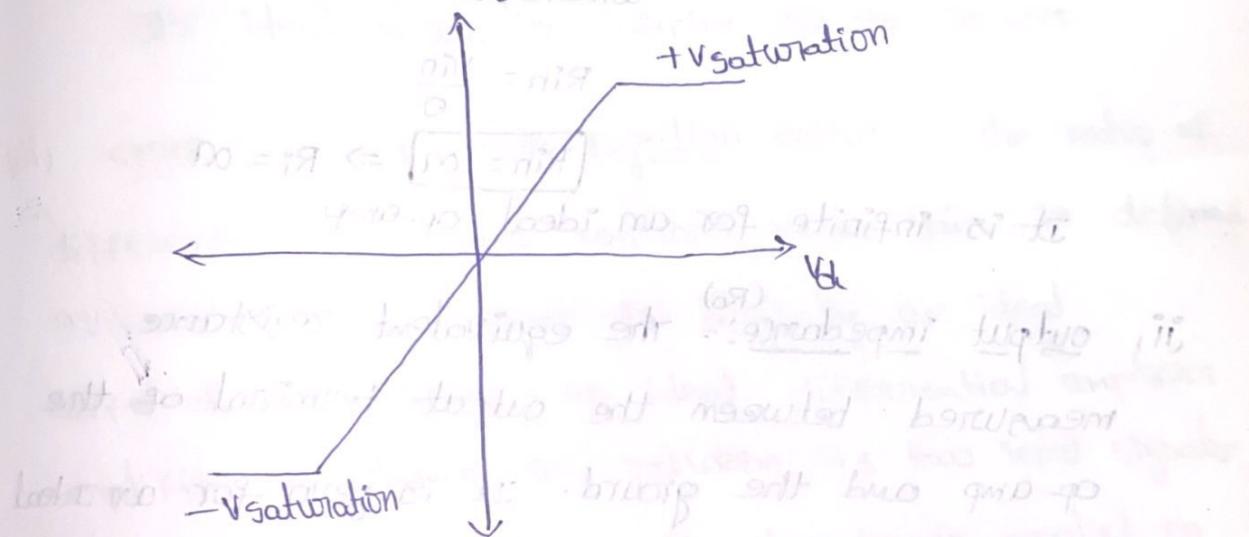


where A = gain of the non-inverting amplifier.

iii) common mode operational amplifier:-



voltage Transfer characteristics of open loop operational amplifier:-

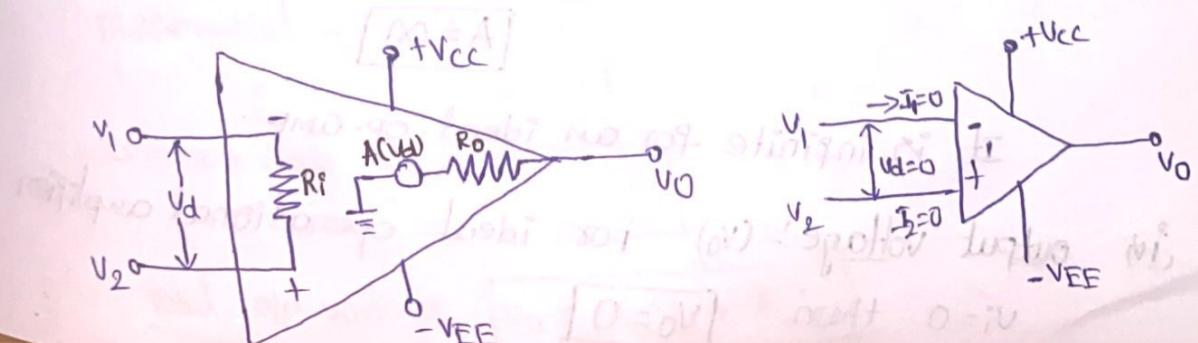


disadvantage of open loop operational amplifier:-

In open loop operational amplifier we are getting linear values, at some point it becomes constant.

* Ideal operational amplifier characteristics:-

i) Equivalent circuit for op-amp symbol of op-amp



where,

R_i = Input impedance.

R_o = output impedance.

- i) Input impedance (R_i) :- The equivalent resistance measured at either of the two terminals with the other terminal grounded is input impedance. It is denoted as R_{in} .

$$R_{in} = \frac{V_{in}}{I_{in}}$$

where, $I = 0$ then

$$R_{in} = \frac{V_{in}}{0}$$

$$R_{in} = \infty \Rightarrow R_i = \infty$$

It is infinite for an ideal op-amp.

- ii) output impedance (R_o) :- The equivalent resistance measured between the output terminal of the op-amp and the ground. It is zero for an ideal op-amp.

$$R_o = 0$$

- iii) open loop voltage gain (A) :- It is the ratio of output voltage and difference voltage of inputs.

$$\text{i.e. } A = \frac{V_o}{V_d}$$

$$\text{where } V_d = 0 \text{ then } A = \frac{V_o}{0}$$

$$A = \infty$$

- iv) output voltage (V_o) :- For ideal operational amplifier $V_i = 0$ then $V_o = 0$

v) Bandwidth:- The range of frequency over which the amplifier performance is satisfactory is called its Bandwidth. It is infinite for an ideal op-amp.

$$B.W = \infty$$

vi) slew rate (S):- The slew rate is defined as the maximum rate of change of output voltage with time.

$$\therefore S = \frac{dV_o}{dt} \Big|_{\text{max}} \Rightarrow S = \infty$$

Its ideal value is infinite for the op-amp.

vii) CMRR (Common mode Rejection Ratio):- The ratio of differential gain and common mode gain is defined as CMRR. Ideal op-amp is basically an ideal differential amplifier. An ideal differential amplifier amplifies the difference between its two input signals.

* The difference between the two inputs applied to inverting and noninverting input terminals of op-amp i.e. $(V_1 - V_2)$ is called differential voltage (V_d)

* An average level of the two input signals is called common mode voltage denoted as (V_c)

$$V_d = V_1 - V_2$$

$$V_c = \frac{V_1 + V_2}{2}$$

Differential gain, $A_d = \frac{V_o}{V_d}$

$$A_c = \frac{V_o}{V_c}$$

Total op voltage $V_o = A_d V_d + A_c V_c$

* But ideally A_{VC} must be zero. i.e., op-amp must reject the common mode voltage.

* The ability of an op-amp to reject a common mode signal is expressed by a ratio called Common mode Rejection Ratio denoted as CMRR.

* It is defined as the ratio of the differential voltage gain (A_d) to common mode voltage gain (A_c).

$$CMRR = \frac{A_d}{A_c}$$

where $A_c = 0$ nominal bias point

$$\therefore CMRR = \frac{A_d}{A_c} = \infty$$

$$CMRR = \infty$$

* Characteristics of practical operational amplifier:-

(i) Input impedance $R_i = \text{upto } M\Omega$

(ii) Output impedance $R_o = \text{it maintains few ohms}$

(iii) Gain $A = 10^5 - 10^6$

offset voltage in millivolts

* IC 741 specifications Standard :-

$$R_i = 2 M\Omega$$

$$\text{offset voltage} = 1 \text{mV}$$

$$R_o = 75 \Omega$$

$$\text{slew rate} \rightarrow 0.5 \text{ V/}\mu\text{s}$$

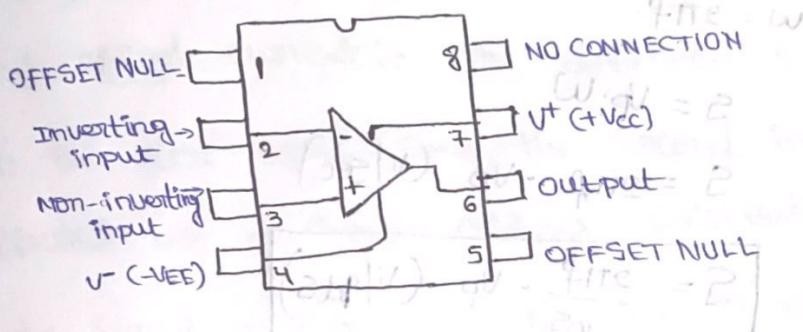
$$A \rightarrow 10^5$$

$$CMRR = 70-90 \text{ dB}$$

These are standard values

IC 741 op-amp:-

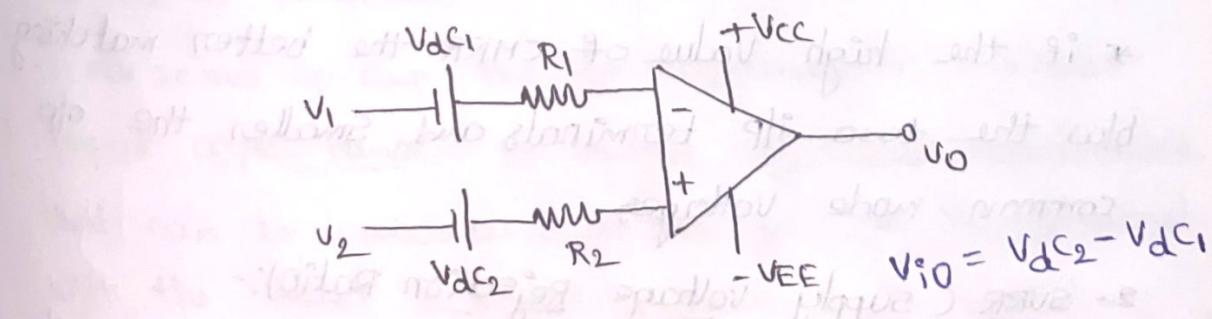
A very popular IC version of op-amp is IC 741. The IC 741 is a pin IC available in dual-in-line package (DIP). The pin diagram of IC 741 op-amp is shown below.



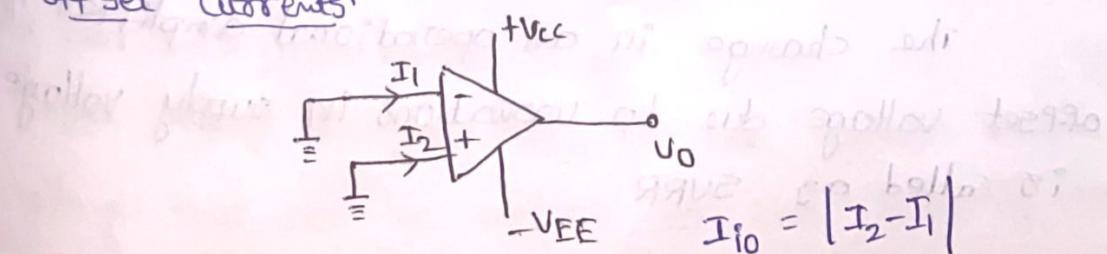
pin diagram of IC 741 opamp.

The pins 1 and 5 are offset null pins. These are used to nullify offset voltages and provide offset voltage compensation. Pin 2 is inverting input while pin 3 is non-inverting input terminal. The output is to be taken from pin 6. Pin 4 is for -VEE supply while pin 7 is for +VCC supply. The pin 8 is the dummy pin and no connection are to be made to this pin externally.

Offset voltages:-



offset currents:



Slew Rate (S) :-

$$S = \frac{dV_o}{dA} \quad \text{max}$$

or Slew rate or voltage per Aor Slew rate or V/F or V/A

$$S = V_p \cdot W$$

W or the peak output voltage in Volts

$V_p \rightarrow$ peak value of the output voltage

$$W = 2\pi f$$

$$S = V_p \cdot W$$

$$S = 2\pi f \cdot V_p \quad (\text{V/sec})$$

$$S = \frac{2\pi f \cdot V_p}{10^5} \quad (\text{V/us})$$

Common mode Rejection Ratio (CMRR) :-

$$\text{CMRR} = \frac{A_d}{A_c}$$

$$A_d = \frac{V_{od}}{V_{id}}$$

$$A_c = \frac{V_{oc}}{V_{ic}}$$

Features of IC 741 op-amp :-

1. CMRR :- For the IC 741 op-amp the CMRR is 90dB

under the test conditions of input resistance $R_s = 10k\Omega$

* if the high value of CMRR the better matching

between the two input terminals and smaller the op-amp

common mode voltages

2. SVRR (Supply Voltage Rejection Ratio) :-

The change in an operational amplifier's offset voltage due to variations in supply voltage is called as SVRR.

for IC 741 op-amp the SVRR = 150 μ V/V

3. Input offset voltage:-

It is the voltage that must be applied between the i/p terminals of op-amp to nullify the o/p.

→ For IC 741 the max. value of IC 741 i/p offset voltage is 6mV.

4. Input offset current:- The differences b/w the currents

into the first input and the second input current is referred as a input offset current.

→ The input offset current for IC 741 op-amp the

max. value is 200 nAmpere.

5. Input Bias current:- The average of the input currents

that are entering into the two i/p terminals.

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

→ For IC 741 op-amp the i/p bias current is 500 nAmpere.

6. Input Resistance:- This is the differential i/p Resistance

at the i/p terminals.

→ For IC 741 op-amp the i/p Resistance (R_i) = 2 M Ω

7. Input capacitance:- It is the equivalent capacitance that can be measured either of the i/p terminal with the other terminal connected to Ground.

→ For IC 741 op-amp $C_{eq} = 1.4 \text{ pF}$

8. Input voltage Range:- This is the common mode

voltage that can be applied to the both i/p terminals

without disturbing the OLP of op-amp

→ for IC 741 op-amp the range of common mode voltage is $\pm 13V$.

9. Large signal voltage gain:- An op-amp amplifies the differences voltages b/w the two input terminals.

so, voltage gain $A_{V+} = \frac{V_o (\text{Op voltage})}{\text{differential input voltage}}$

→ for IC 741 to get better voltage gain, we must keep the differential input voltage is low.

→ for IC 741 op-amp the voltage gain is 2,00,000

under the test condition of load resistance greater than or equals to $2k\Omega$ ($R_L \geq 2k\Omega$), $V_o = \pm 100V$ (Op voltage)

10. Output Resistance (R_o):-

The output resistance is measured b/w the op terminal of op-amp and ground.

→ for IC 741 op-amp the $R_o = 75\Omega$

11. Power Consumption:-

For IC 741 op-amp the power consumption is 85 mW.

12. Slew Rate:-

For IC 741 op-amp the slew rate is $0.5V/\mu s$

→ toward of maximum terminal testo will occur

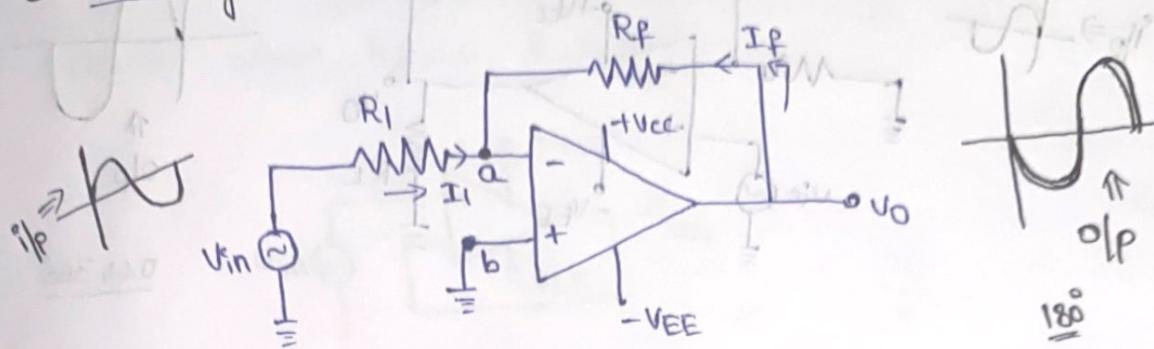
→ $100V - 100V = 200V$ (Op voltage)

→ $200V / 0.5V/\mu s = 400\mu s$ (slew rate)

→ toward of minimum terminal testo will occur

* Closed Loop Operational Amplifier:-

① Inverting Closed Loop Operational Amplifier:-



Virtual Ground Concept:-

According to virtual ground concept the potentials at the inverting terminal and non-inverting terminal both are equal. So, $V_a = 0 = V_b$

$$\text{thus } I_1 = -I_F$$

$$I_1 + I_F = 0 \\ I_1 = -I_F$$

$$\frac{V_{in} - V_a}{R_I} = -\left[\frac{V_O - V_a}{R_F} \right]$$

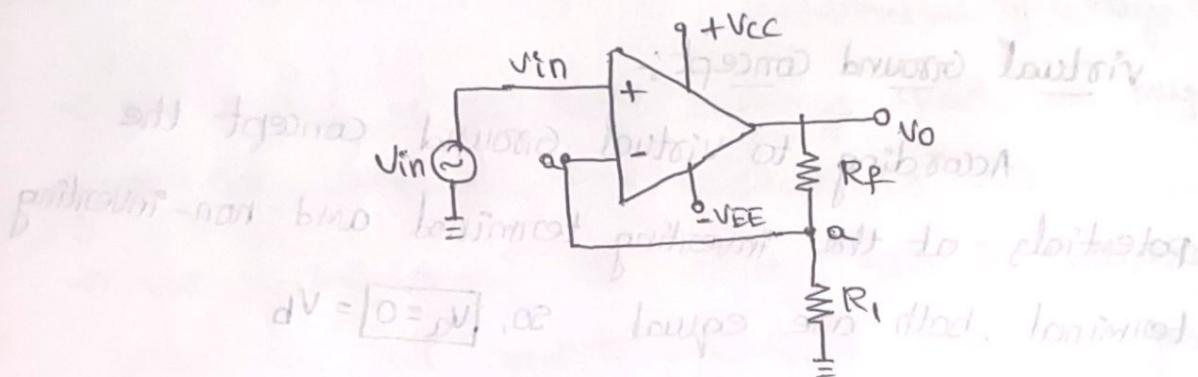
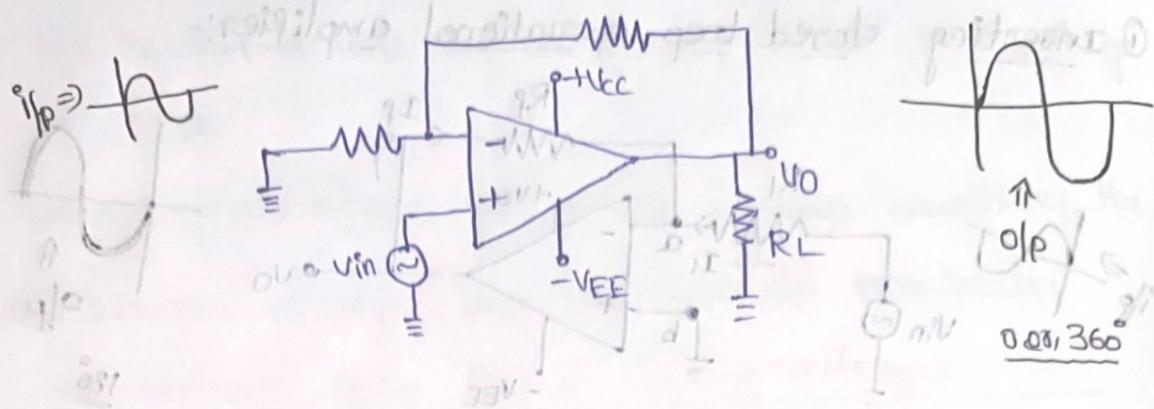
$$\frac{V_{in} - 0}{R_I} = -\left[\frac{V_O - 0}{R_F} \right]$$

$$\frac{V_{in}}{R_I} = -\frac{V_O}{R_F}$$

$$\text{Gain } A = \frac{V_O}{V_{in}} = -\frac{R_F}{R_I} \Rightarrow A = -\frac{R_F}{R_I}$$

The negative sign indicates that the polarity of o/p is opposite to that of input. Hence it is called inverting amplifier. The o/p waveform of inverting amplifier has 180° of phase shift.

* Non-inverting closed loop operational amplifier:



According to voltage division rule

$$V_o = \left(\frac{R_f}{R_1 + R_f} \right) V_{in}$$

According to virtual ground concept

$$V_{in} = V_o$$

$$V_{in} = \frac{R_f}{R_1 + R_f} \times V_{out}$$

$$\text{Gain } A = \frac{V_{out}}{V_{in}} = \frac{R_f}{R_1} = 1 + \frac{R_f}{R_1}$$

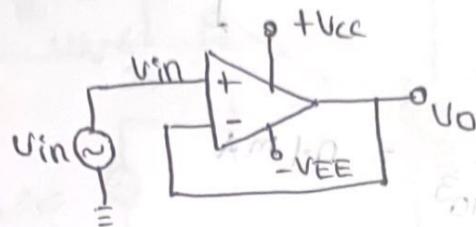
$$A = 1 + \frac{R_f}{R_1}$$

* Inverting op-Amp

1. o/p and i/p signals are out of phase with each other.
2. $\text{Z}_{in} = \infty$

Applications of Non-inverting :-

The non-inverting amplifier acts as a voltage follower circuit when $R_f = 0$, $R_i = \infty$.



$$\text{where, } V_{\text{out}} = V_{\text{in}}$$

when we compare the two circuits we use voltage follower circuit. It is also called unity gain amplifier, buffer amplifier.

problems:-

- ① Design a closed loop op-amp with a gain of -10 and input resistance $= 10k\Omega$

Sol:- Given $R_i = 10\Omega$

$$A = -10$$

$$A_{CL} = -\frac{R_f}{R_i} \times (1 + A)$$

$$+10 = +\frac{R_f}{10 \times 10^3}$$

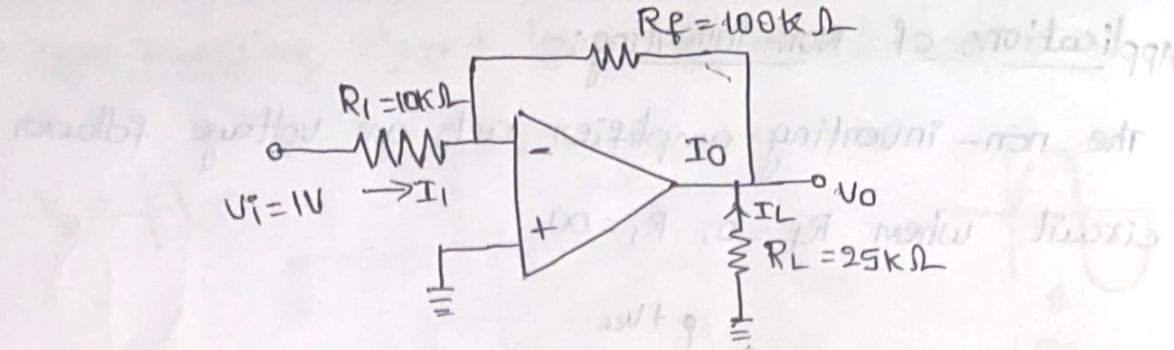
$$R_f = 10 \times 10 \times 10^3 = 10^5$$

$$R_f = 100k\Omega$$

- ② For the given circuit calculate

i) $I_L = [i_{in} V_o] \times 10^3$ ii) $I_L = [i_{in} V_o] \times 10^3$ iii) Total current I_o

$$I_o = \frac{V_o}{10 \times 10^3} = 20$$



Sol:-

$$\text{i)} \quad I_1 = \frac{V_i}{R_1} = \frac{1}{10 \times 10^3} = 0.1 \text{ mA}$$

$$I_1 = 0.1 \text{ mA}$$

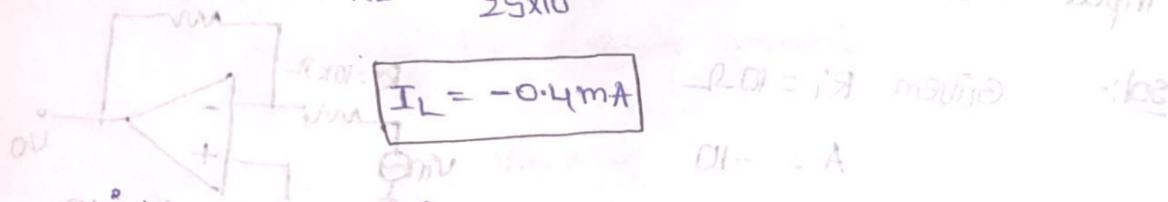
$$\text{ii)} \quad \frac{V_o}{V_{in}} = -\frac{R_f}{R_1} \Rightarrow V_o = -\frac{R_f V_{in}}{R_1}$$

$$V_o = -\frac{(100 \times 10^3)}{10 \times 10^3} \times 1$$

$$V_o = -10 \text{ V}$$

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$$\text{iii)} \quad I_L = \frac{V_o}{R_L} = \frac{-10}{25 \times 10^3} = -0.4 \text{ mA}$$



$$I_L = -0.4 \text{ mA}$$

$$\text{iv)} \quad I_o = I_1 + I_L \\ = (0.1 + 0.4) \text{ mA}$$

$$= -0.3 \text{ mA}$$

$$I_o = -0.3 \text{ mA}$$

- ③ Design a closed loop operational amp with a gain of +5 using with $R_1 = 10\text{ k}\Omega$

$$A_{CL} = 1 + \frac{R_f}{R_1}$$

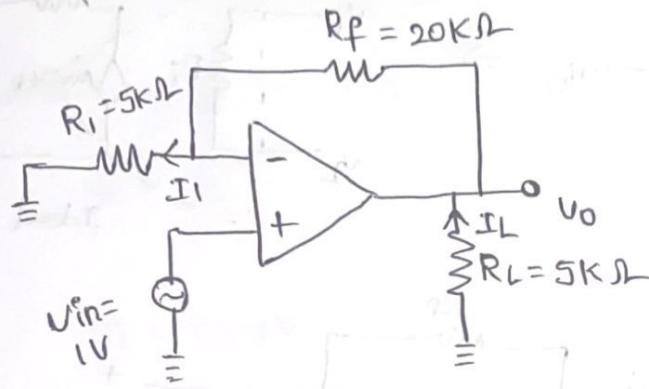
$$\text{of design } 5 = 1 + \frac{R_f}{10 \times 10^3} \Rightarrow 5 \times [10] \times 10^3 = 10 \times 10^3 + R_f$$

$$R_f = 50 \times 10^3 - 10^4$$

$$R_f = 40 \text{ k}\Omega$$

Q) For the given circuit calculate

iii) V_o iv) A_{CL} v) I_L vi) I_O



Sol:-

$$\text{iii) } \frac{V_o}{V_{in}} = 1 + \frac{R_f}{R_1} \Rightarrow V_o = V_{in} \left[1 + \frac{R_f}{R_1} \right] \\ = 1 \left[1 + \frac{20}{5} \right]$$

$$V_o = 5V$$

$$\text{iii) } A_{CL} = \frac{V_o}{V_{in}} = \frac{5}{1} = 5$$

$$A_{CL} = 5$$

$$\text{v) } I_L = \frac{V_o}{R_L} = \frac{5}{5 \times 10^3} = \frac{1}{10^3} = 10^{-3}$$

$$I_L = 1mA$$

$$\text{vi) } I_L = I_O + I_1 \quad I_1 = \frac{V_o}{R_1} = \frac{1}{5 \times 10^3} = 0.2mA$$

$$I_O = I_L - I_1$$

$$I_O = 1 - 0.2$$

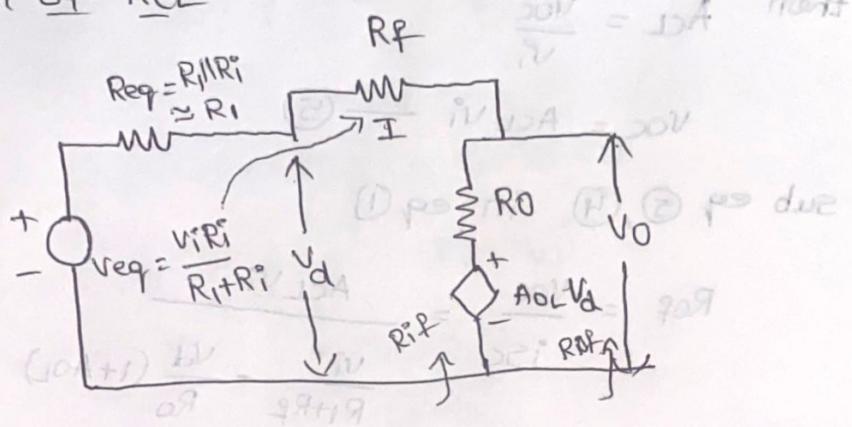
$$I_O = 0.8mA$$

$$(Q) 0.2 + 0.8 = 1.0mA + 1.0A + 1.0A + 1V$$

$$Q = 0.2mA + (0.8 + 1A)I = 0V$$

* practical inverting amplifier:-

calculation of A_{CL} :-



From fig the ~~alpha loop equation.~~

$$V_o = iR_o + AOL V_d \quad \text{--- (1)}$$

$$V_d + iR_f + V_o = 0 \quad \text{--- (2)}$$

$$V_d = -(iR_f + V_o) \quad \text{--- (3)}$$

Sub (3) in (1)

$$V_o - iR_o = AOL [-(iR_f + V_o)]$$

$$V_o - iR_o = -V_o AOL - AOL iR_f$$

$$V_o + V_o AOL = +i[R_o - R_f AOL]$$

$$V_o (1 + AOL) = i [R_o - R_f AOL] \quad \text{--- (4)}$$

At i/p side

$$V_i = i(R_i + R_f) + V_o \quad \text{--- (5)}$$

from (4)

$$i = \left[\frac{1 + AOL}{R_o - AOL R_f} \right] V_o$$

Sub in eq (5)

$$V_i = V_o \left[\frac{1 + AOL}{R_o - AOL R_f} (R_i + R_f) + 1 \right]$$

Gain

$$A_{CL} = \frac{V_o}{V_{in}} = \left[\frac{R_o - AOL R_f}{R_o + R_f + R_i (1 + AOL)} \right]$$

practical

If $AOL \gg 1$ then $AOL R_i \gg R_o R_f$ so

Neglecting R_o

$$A_{CL} = -\frac{AOL R_f}{R_i AOL} = -\frac{R_f}{R_i}$$

$$A_{CL} = -\frac{R_f}{R_i}$$

Ideal

Input Resistance (R_{if}) :-

$$R_{if} = \frac{V_d}{I} \times \frac{V_o}{(R_f + R_o) i} = \frac{V_o}{(R_f + R_o) i} = 909$$

From eq ②

$$V_d + i(R_f + R_o) + AOL V_d = 0$$

$$V_d (1 + AOL) = -(R_f + R_o) i$$

$$\frac{V_d}{(1 + AOL)} = -\frac{(R_f + R_o) i}{(1 + AOL)} = 909$$

$$R_{if} = \frac{(R_f + R_o)}{1 + AOL} = 909$$

Output Resistance (R_{of}) :-

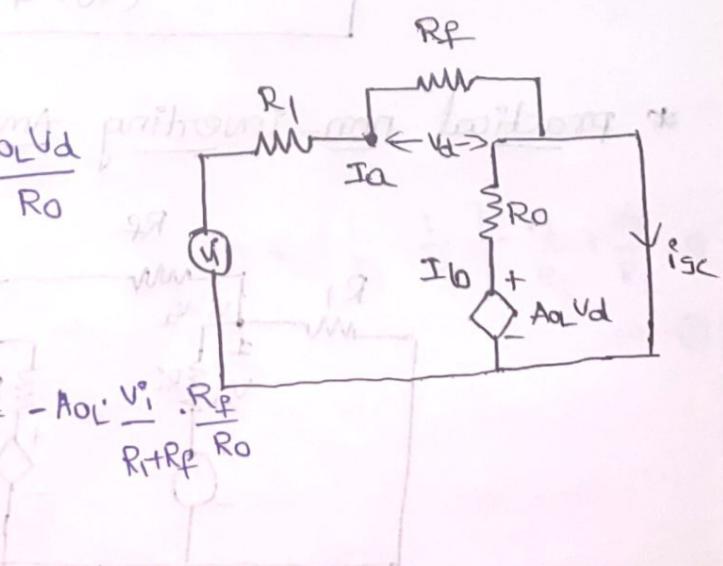
$$i_a = \frac{V_i}{R_i + R_f}, \quad i_b = \frac{AOL V_d}{R_o}$$

$$V_d = -i_a R_f$$

$$i_b = -\frac{AOL i_a R_f}{R_o} = -AOL \frac{V_i \cdot R_f}{R_i + R_f \cdot R_o}$$

$$i_{sc} = i_a + i_b$$

$$= \frac{V_i}{R_i + R_f} - \frac{AOL V_i R_f}{R_o (R_i + R_f)}$$



$$i_{SC} = \frac{V_i R_o - AOL V_i R_f}{R_o (R_i + R_f)}$$

$$i_{SC} = \frac{V_i (R_o - AOL R_f)}{R_o (R_i + R_f)}$$

$$R_{of} = \frac{V_{oc}}{i_{SC}}$$

$$A_{CL} = \frac{V_{oc}}{V_i} \Rightarrow V_{oc} = A_{CL} \cdot V_i$$

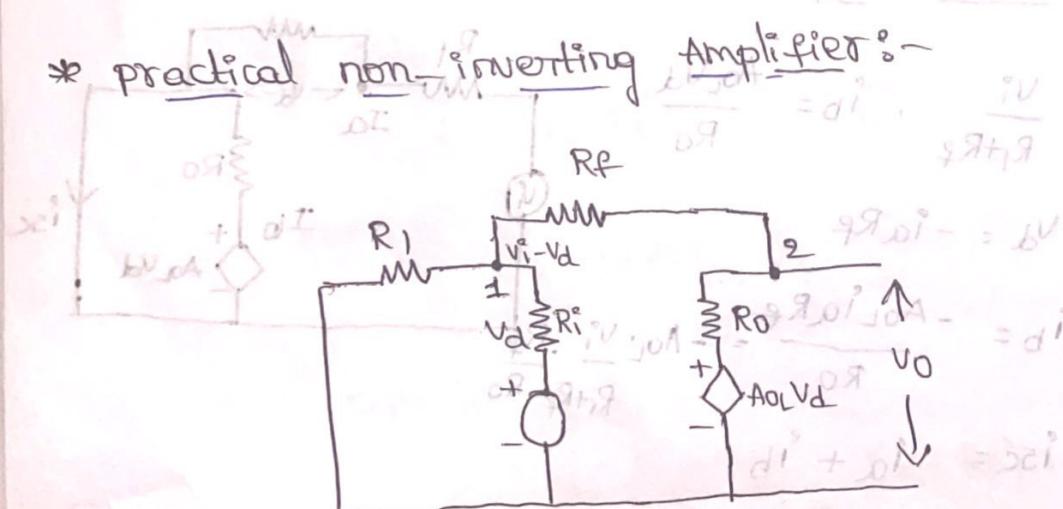
$$R_{of} = \frac{A_{CL} V_i}{V_i (R_o - AOL R_f)} \times \frac{R_o (R_i + R_f)}{R_o (R_i + R_f)}$$

where $A_{CL} = \frac{R_o - AOL R_f}{(R_o + AOL R_f) + R_i (1 + AOL)}$

$$R_{of} = \frac{\frac{R_o - AOL R_f}{(R_o + AOL R_f) + R_i (1 + AOL)}}{(R_o + AOL R_f) + R_i (1 + AOL)} \times \frac{R_o (R_i + R_f)}{(R_o - AOL R_f)}$$

$$R_{of} = \frac{(R_o + AOL R_f)}{(R_o + AOL R_f) + R_i (1 + AOL)}$$

* practical non-inverting Amplifier :-



$$\text{where } R = \frac{1}{Y} \quad \frac{V_o}{(R_f + R_o) R_f} = \frac{V_o}{R_o}$$

$$\text{At node 1} \quad (V_i - V_d) Y_1 + V_d Y_i^* + (V_i - V_d - V_o) Y_f = 0 \quad \text{--- 1}$$

$$-V_d (Y_1 - Y_i^* + Y_f) + V_i (Y_1 + Y_f) = Y_f V_o \quad \text{--- 1}$$

At node 2:

$$(V_i^* - V_d - V_o) Y_f + (A_{OL} V_d - V_o) Y_o = 0$$

$$V_d (A_{OL} Y_o - Y_f) + Y_f V_i^* = V_o (Y_o + Y_f) \quad \text{--- 2}$$

$$A_{CL} = \frac{Y_o}{Y_i^*} = \frac{A_{OL} Y_o (Y_1 + Y_f) + Y_f Y_i^*}{(A_{OL} + 1) Y_o Y_f + (Y_1 + Y_i^*) (Y_f + Y_o)}$$

practical.

$$[V_o - V_f] \frac{1}{R_f} = 0V$$

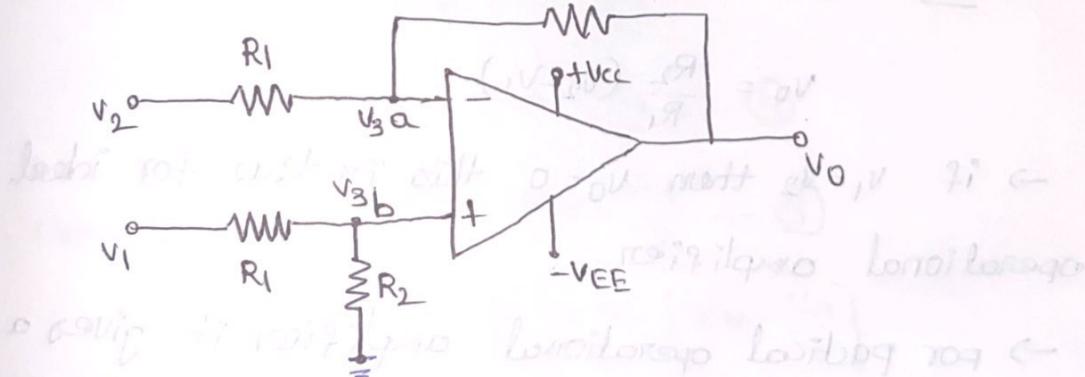
$$A_{OL} \gg 1$$

$$A_{CL} \approx \frac{Y_1 + Y_f}{Y_f} \approx 1 + \frac{Y_1}{Y_f} \approx 1 + \frac{R_f}{R_1}$$

$$A_{CL} \approx 1 + \frac{R_f}{R_1}$$

Ideal

* Differential Amplifier:-



Apply KCL at node 'a'

$$\frac{V_3 - V_2}{R_1} + \frac{V_o - V_3}{R_2} = 0 \Rightarrow V_3 \left[\frac{1}{R_1} - \frac{1}{R_2} \right] - \frac{V_2}{R_1} + \frac{V_o}{R_2} = 0 \quad \text{--- 1}$$

At node 'b'

$$\frac{V_3 - V_1}{R_1} - \frac{V_3}{R_2} = 0$$

$$V_3 \left[\frac{1}{R_1} - \frac{1}{R_2} \right] - \frac{V_1}{R_1} = 0 \quad \text{--- 2}$$

$$① - ② \quad 0 = qV(0V - BV - IV) + qVBV + qV(BV - IV)$$

$$① - V_3 \left[\frac{1}{R_1} - \frac{1}{R_2} \right] - \frac{V_2}{R_1} + \frac{V_0}{R_2} - V_3 \left[\frac{1}{R_1} - \frac{1}{R_2} \right] + \frac{V_1}{R_1} = 0$$

$$0 = qV(0V - BV - 10A) + qV(0V - BV - IV)$$

$$③ - \left(\frac{V_1}{R_1} - \frac{V_2}{R_1} + \frac{V_0}{R_2} + qV \frac{R_2}{R_1} (qV - qV - 10A) \right) = 0$$

Laboratory

$$\frac{V_0}{R_2} = \frac{V_2}{R_1} - \frac{V_1}{R_1} = \frac{IV}{qV} = 10A$$

$$V_0 = \frac{R_2}{R_1} [V_2 - V_1]$$

The differential amplifier amplifies the differences of the two signals this type of circuits are used in instrumentation amplifiers and verify the small signal changes in the circuits.

* Common mode and differential mode gain

$$V_0 = \frac{R_2}{R_1} (V_2 - V_1)$$

→ if $V_1 = V_2$ then $V_0 = 0$ this is true for ideal operational amplifier.

→ for practical operational amplifier it gives a small response to the common mode component of the input voltages.

→ In some cases, when we take different inputs signals we are getting some differential voltage so, the op voltage is also depends up on the average of the two input signals.

$$V_o = V_d = (V_1 - V_2) \quad \text{--- (1)}$$

$$V_{cm} = \frac{V_1 + V_2}{2} \quad \text{--- (2)}$$

Because of the mismatching of the op-amp gain at the output w.r.t. to the positive terminal is slightly different from w.r.t. to the -ve terminal.

$$V_o = A_1 V_1 + A_2 V_2 \quad \text{--- (3)}$$

From eq (2)

$$V_1 = 2V_{cm} - V_2$$

from eq (1)

$$V_2 = V_1 - V_d$$

NTF

$$\text{Then } V_{cm} =$$

$$\frac{V_1 + V_1 - V_d}{2}$$

$$V_{cm} = \frac{2V_1 - V_d}{2}$$

$$V_{cm} = V_1 - \frac{V_d}{2}$$

$$V_1 = V_{cm} + \frac{V_d}{2} \quad \text{--- (4)}$$

$$V_2 = V_{cm} - \frac{V_d}{2} \quad \text{--- (5)}$$

From (3)

$$V_o = A_1 \left[V_{cm} + \frac{V_d}{2} \right] + A_2 \left[V_{cm} - \frac{V_d}{2} \right]$$

$$V_o = V_{cm} (A_1 + A_2) + V_d \left(\frac{A_1 - A_2}{2} \right)$$

$$\text{assume } ADM = \frac{A_1 - A_2}{2}$$

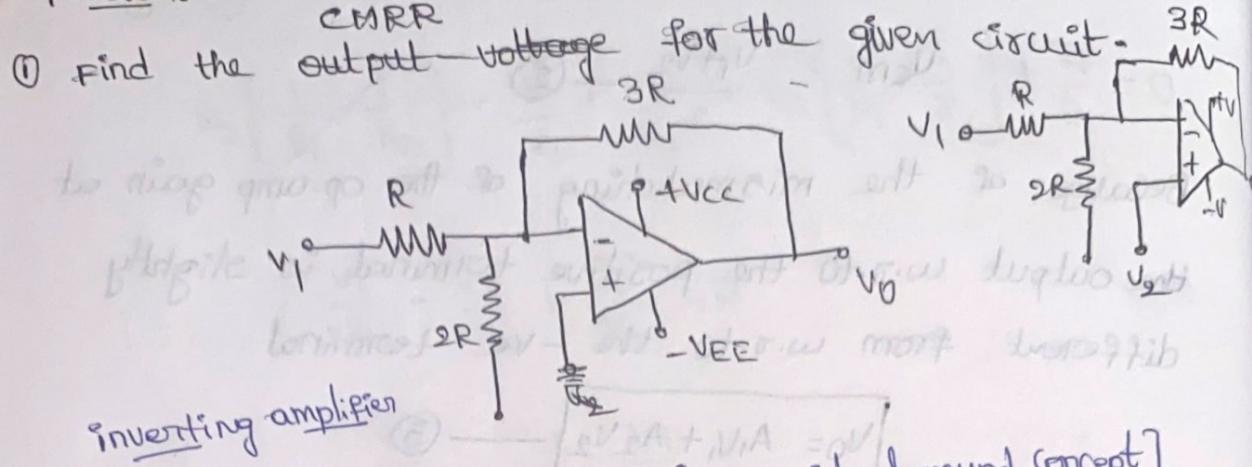
$$ACM = A_1 + A_2$$

$$\therefore V_o = V_{cm} \cdot ACM + V_d \cdot ADM$$

CMRR :-

$$\text{CMRR} = \frac{ADM}{ACM}$$

problems:



Inverting amplifier

$$R_1 = R, \quad R_f = 3R. \quad [\text{from virtual ground concept}]$$

$$A_{CL} = -\frac{R_f}{R_1}$$

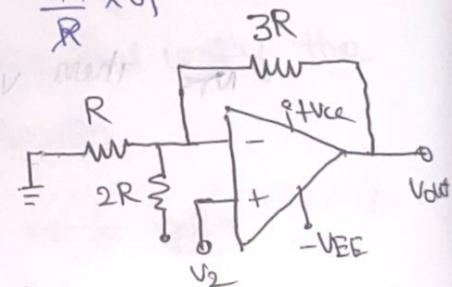
$$\frac{V_O}{V_{in}} = -\frac{R_f}{R_1}$$

$$V_O = -\frac{R_f}{R_1} (V_{in}) = -\frac{3R}{R} \times V_1$$

$$V_O = -3V_1$$

Non-inverting amp

$$\text{where } R_{eq} = R \parallel 2R$$



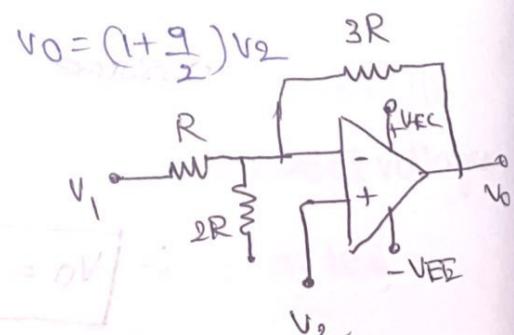
$$R_{eq} = \frac{R \times 2R}{R+2R} = \frac{2R^2}{3R} = \frac{2}{3}R$$

$$A_{CL} = 1 + \frac{R_f}{R_{eq}}$$

$$\frac{V_O}{V_{in}} = 1 + \frac{R_f}{R_{eq}}$$

$$V_O = \left(1 + \frac{R_f}{R_{eq}}\right) V_{in} = \left(1 + \frac{3R}{\frac{2}{3}R}\right) V_{in}$$

$$V_O = \left(\frac{9}{2}\right) V_{in}$$



Differential amplifier

$$V_O = A_1 V_1 + A_2 V_2$$

$$V_O = -3V_1 + \frac{11}{2}V_2$$

$$ADM = \frac{A_1 - A_2}{2} = \frac{-3 + \frac{11}{2}}{\frac{2}{2}} = \frac{-6 - 11}{4} = -\frac{17}{4}$$

$$ACM = A_1 + A_2$$

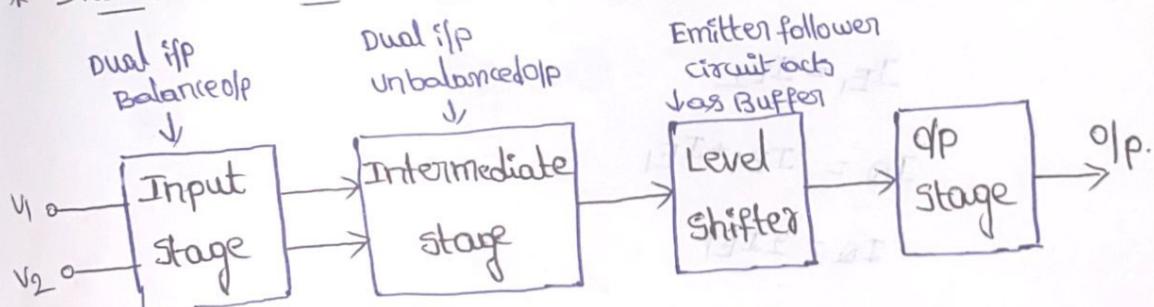
$$= -3 + \frac{11}{2} = -\frac{6 + 11}{2} = \frac{5}{2}$$

$$CMRR = \frac{ADM}{ACM}$$

$$CMRR = \frac{-\frac{17}{4}}{\frac{5}{2}} = \frac{-\frac{17}{4} \times \frac{2}{5}}{2} = -1.7 \text{ dB}$$

$$CMRR = -\frac{17}{10} = -1.7 \text{ dB}$$

* Internal circuits of operational amplifier:-



Block diagram of op-amp

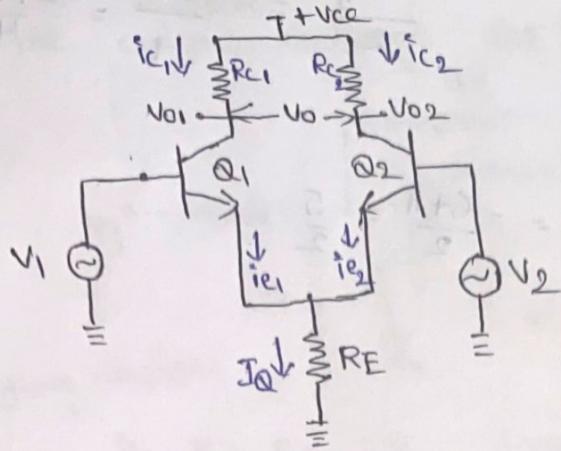
The input stage and intermediate stage, we are using differential amplifier.

* Differential amplifier:-

The differential amplifiers are 4 types.

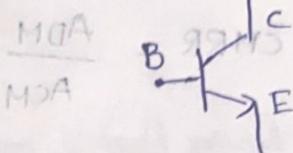
1. Dual i/p balanced output differential amplifier.
2. Dual i/p unbalanced output differential amplifier.
3. Single i/p, balanced output differential amplifier.
4. Single i/p unbalanced output differential amplifier.

3) Dual i/p Balanced o/p:-



$$I_{C1} = I_{C2} = MDA$$

Balanced



If we give common i/p

$$V_1 = V_2$$

$$\frac{f_1}{P}$$

$B=1$ then short circuit, ON switch

$$\frac{B}{P}$$

$B=0$ then open circuit, OFF switch

The two transistors are emitter coupled.

So, All the transistors are identical.

$$I_Q = I_{E1} + I_{E2}$$

result of addition

$$I_{E1} = I_{E2}$$

Different but same

$$I_Q = I_{E1} + I_{E2}$$

$$I_Q = 2IE_1$$

q/i laws

of operation

of operation

of operation

q/i laws

of operation

of operation

$$IE_1 = \frac{I_Q}{2}$$

$$\text{so, spot } IE_2 = \frac{I_Q}{2} \Rightarrow IE_1 = IE_2 = \frac{I_Q}{2} \quad \text{--- ①}$$

$$\frac{I_C}{IE} = \alpha \Rightarrow I_C = \alpha IE$$

$$I_{C1} = \alpha \frac{I_Q}{2}$$

$$I_{C1} = I_{C2} = \alpha \frac{I_Q}{2} \quad \text{--- ②} \text{ reb str}$$

$$V_{O1} = V_{CC} - I_{C1} R_{C1} \text{ two terminals q/i laws}$$

$$V_{O1} = V_{CC} - \alpha \frac{I_Q}{2} R_{C1} \text{ reb str q/i laws}$$

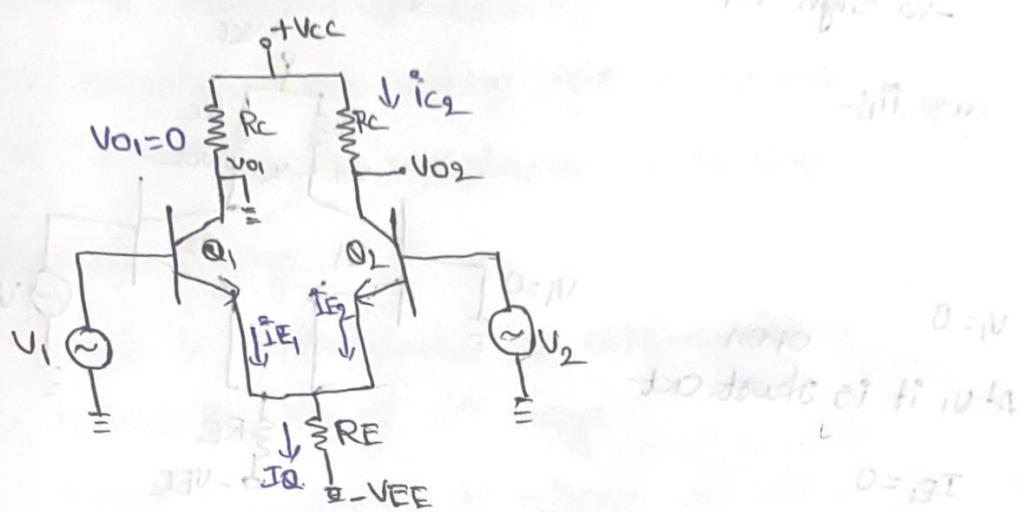
$$V_{O2} = V_{CC} - I_{C2} R_{C2} \text{ two terminals q/i laws}$$

$$V_{O2} = V_{CC} - \alpha \frac{I_Q}{2} R_{C2} \text{ reb str q/i laws}$$

$$V_{O1} - V_{O2} = 0$$

The differential amplifier does not respond to the common-mode signals.

iii) Dual i/p, unbalanced o/p:



$$I_{E1} = I_{E2} = \frac{I_Q}{2} \quad \text{--- ①}$$

$$I_{C1} = I_{C2} = \alpha \frac{I_Q}{2} \quad \text{--- ②}$$

where $V_{O1} = 0$

$$V_{O2} = V_{CC} - I_{C2} R_C$$

$$V_{CC} - \alpha \frac{I_Q}{2} R_C$$

$$V_O = V_{O1} - V_{O2} = 0 - V_{CC} + \alpha \frac{I_Q}{2} R_C$$

$$V_O = \alpha \frac{I_Q}{2} R_C - V_{CC}$$

iii) single i/p, Balanced o/p:

case ii:

$$V_1 = \text{i/p}$$

$$Q_1 = \text{ON}$$

$$I_{E1} = I_Q$$

$$I_{E2} = 0$$

$$V_{O1} = V_{CC} - I_{C1} R_C$$

$$V_{O2} = V_{CC} - I_{C2} R_C$$

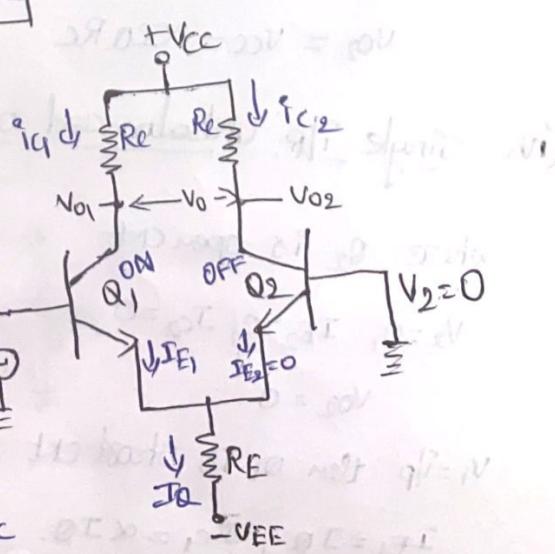
$$V_2 = 0$$

$$Q_2 = \text{OFF}$$

$$I_{C2} = 0$$

$$V_{O2} = V_{CC} - I_{C2} R_C$$

$$V_{O2} = V_{CC}$$



$$V_0 = -\alpha I_Q R_C$$

-ve sign represent inverting.

Cage diode

$$V_i = 0$$

open

At Q₁, it is short ckt

$$I_{E1} = 0$$

$$I_{C1} = 0$$

$$V_{O1} = V_{CC} - I_{C1} R_C$$

$$V_{O1} = V_{CC}$$

$$V_2 = iLp$$

At Q₂ it is short ckt

$$I_{E2} = I_Q$$

$$I_{C2} = \alpha I_Q$$

$$V_{O2} = V_{CC} - I_{C2} R_C$$

$$V_{O2} = V_{CC} - \alpha I_Q R_C$$

(iv) single iLp, unbalanced op:

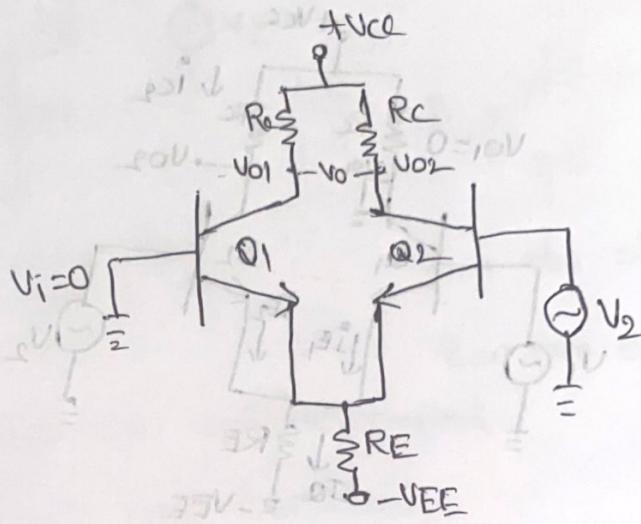
where Q₂ is open ckt

$$V_2 = 0, I_{B2} = 0, I_{C2} = 0$$

$$V_{O2} = 0$$

V_i = iLp then Q₁ is short ckt

$$I_{E1} = I_Q, I_{C1} = \alpha I_Q$$



$$\textcircled{1} - \frac{\partial I}{\partial E} = \beta T = \beta T$$

$$\textcircled{2} - \frac{\partial I}{\partial E} = \beta I = \beta T$$

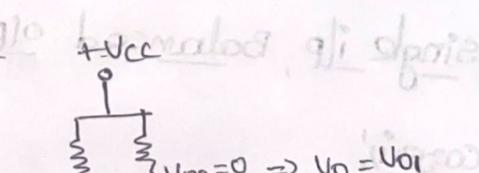
$$V_0 = V_{O1} - V_{O2}$$

$$= V_{CC} - V_{CC} + \alpha I_Q R_C$$

$$V_0 = \alpha I_Q R_C$$

+ve sign represent non-inverting

$$V_0 = \alpha I_Q R_C$$



$$V_0 = V_{O1}$$

$$V_{O2} = 0 \Rightarrow V_0 = V_{O1}$$

$$V_0 = V_{O1}$$

$$V_{O1} = V_{CC} - I_{C1} R_C$$

$$V_O = V_{O1} = V_{CC} - \alpha I_Q R_C$$

1. Input stage:-

- Dual i/p, Balanced op-amp Amplifier
- It provides most voltage gain of op-amp.
- It provides i/p resistance of op-amp

2. Intermediate stage:-

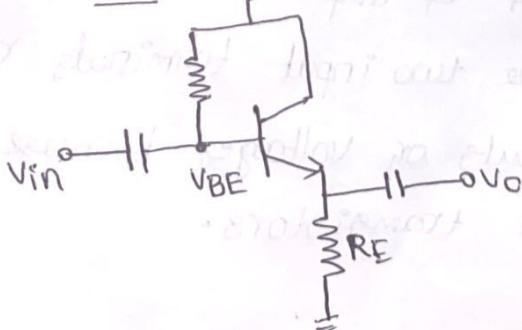
- Dual i/p, unbalanced op diff-amp
- Drives the op of 1st stage
- Direct coupling \rightarrow dc voltage well above ground level.

3. Level Translator or, shifting stage:-

- To adjust the dc levels on dc voltages we used level translator ckt's.

In op-amp we are using direct coupling b/w the differential amplifier because of this operating point moves above the Ground level by using level translator [emitter follower ckt] we can bring down that dc level to zero level of source with minimum distortion.

Emitter follower circuit:-



For Si, $V_{BE} = 0.7V$, For Ge, $V_{BE} = 0.3V$.

$$V_{in} - V_{BE} = V_O$$

Compare to V_{in} & V_o , V_{BE} voltages are very small

$$\text{so, } V_{in} = V_o$$

so, it acts as a Buffer.

→ In this circuit we are taking the op at the emitter node and the input voltage V_{in} is followed the emitter node op. that's why we are calling this circuit as a emitter follower circuit.

4. Output stage:

• It design to provide the low output impedance.

• The push-pull complementary amplifier meets all these requirements and hence used as an output stage.

* DC and AC characteristics of op-amp:

→ An ideal op-amp does not take current or voltage from the source because of ilp impedance is ∞ .

→ For practical op-amp it has some currents or

voltages delivered from the source to the ilp terminal of op-amp.

→ Here the two input terminals response differently to the currents or voltages because of mismatching between the transistors.

The DC characteristics are:

1. Input Bias current
2. Input offset current
3. Input offset voltage
4. Total output offset voltage
5. Thermal drift.

1. Input Bias current:-

→ The op. Amplifier ilp is a differential amplifier which may be made from BJT or FET.

→ In the case of BJT the ilp transistors are work when the external supply voltage given to base of the transistors.

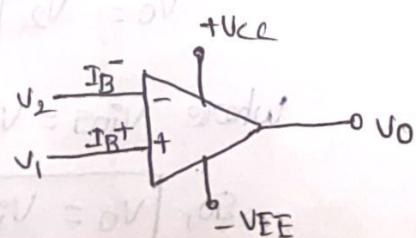
→ For practical op.amp the input terminals supply a little bit of DC current into the operational amplifier because of this the output voltage does not equals to zero.

→ Both the transistors are identical with each other but mismatching of the transistors. The two bias currents are different from each other.

→ So, Here we are taking bias current for inverting terminal as I_B^- and for non-inverting terminal as I_B^+ ($I_B^- \neq I_B^+$)

→ Here manufacturing takes the ilp bias current as the average of the 2 bias currents.

$$I_B = \frac{I_B^- + I_B^+}{2}$$



2. Input offset currents

- The Bias current compensation will work when the both bias currents i_B^+ & i_B^- are equal. Since the i/p transistors cannot be made identical.
- There will be a some small difference between i_B^+ & i_B^- this difference is called as i/p offset current.

$$I_{ios} = |i_B^+ - i_B^-|$$

R_f

3. Input offset voltage :-

→ By using above compensation techniques, it is found that

the output voltage still not be zero.

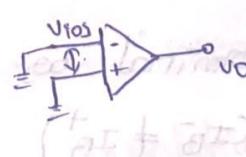
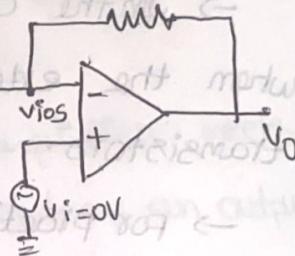
with zero i/p voltage

→ This is due to imbalances inside the op.amp and one may have to apply a small voltage at i/p terminals to make the o/p voltage is zero.

→ This voltage is known as input offset voltage

$$V_{ios} = |V_2 - V_1| \quad ①$$

Apply voltage division rule.



$$N_2 = \left(\frac{R_f}{R_1 + R_f} \right) V_o$$

$$V_o = V_2 \left[\frac{R_f + R_i}{R_i} \right]$$

$$\text{where } V_{ios} = V_2 \quad [\because V_i = 0V]$$

$$\text{So, } V_o = V_{ios} \left[1 + \frac{R_f}{R_i} \right]$$

4. Total output offset voltage:-

→ The total output offset voltage (V_{OT}) is the ~~V_{OOF}~~ addition of i_{LP} offset voltage and i_{LP} offset current of output $\frac{V_O}{I_{LP}}$

$$V_{OT} = V_0 \ll i_{LP} \text{ offset voltage} + V_0 \ll i_{LP} \text{ offset current}$$

$$V_{OT} = \left(1 + \frac{R_F}{R_I}\right) V_{IO} + R_F I_{IO}$$

5. Thermal Drift:-

The op-amp depends upon the temperature also. Because of the variation in temperature, the i_{LP} offset current and i_{LP} offset voltage is also changed.

→ This variation is called as the thermal drift.

AC characteristics of op-amp:-

i) Frequency response

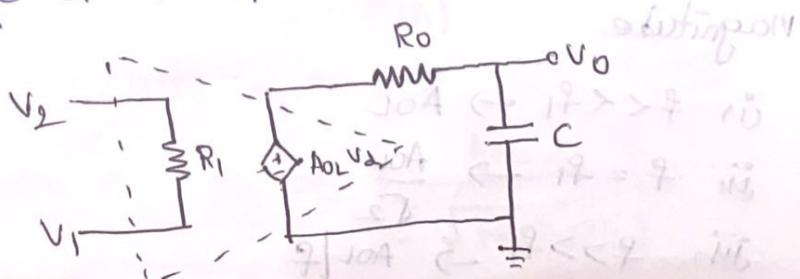
ii) slew rate.

iii) Frequency response

→ For ideal operational amplifier the B-W is ∞ and it maintains constant gain over all the frequencies.

→ For practical operational amplifier at higher frequencies the gain of the op-amp is decreases.

Because of that, internal capacitor is added at the op-amp stage of the op-amp.



$$V_0 = \frac{X_C}{R_o + j\omega C} \times A_{OL} V_d$$

$$V_0 = \frac{\frac{1}{j\omega C}}{R_o + \frac{1}{j\omega C}} \times A_{OL} V_d$$

$$V_0 = \frac{\frac{1}{j\omega C}}{R_o + j\omega C} \times A_{OL} V_d$$

$$\frac{V_0}{V_d} = \frac{A_{OL}}{1 + j\omega R_o C}$$

$$A = \frac{V_0}{V_d} = \frac{A_{OL}}{1 + j2\pi f R_o C} \quad [\text{where } \omega = 2\pi f]$$

$$\text{Let } f_l = \frac{1}{2\pi R_o C}$$

$$A = \frac{A_{OL}}{1 + j(f/f_l)}$$

$$|A| = \sqrt{\frac{A_{OL}}{(1 + (f/f_l)^2)}}$$

$$\phi = -\tan^{-1}(f/f_l)$$

Magnitude

$$\text{i)} f < f_l \rightarrow A_{OL}$$

$$\text{ii)} f = f_l \rightarrow \frac{A_{OL}}{\sqrt{2}}$$

$$\text{iii)} f > f_l \rightarrow A_{OL}/f$$

$$i) f = f_1$$

$$\phi = -\tan^{-1}(1) = -45^\circ \text{ or } -\pi/4$$

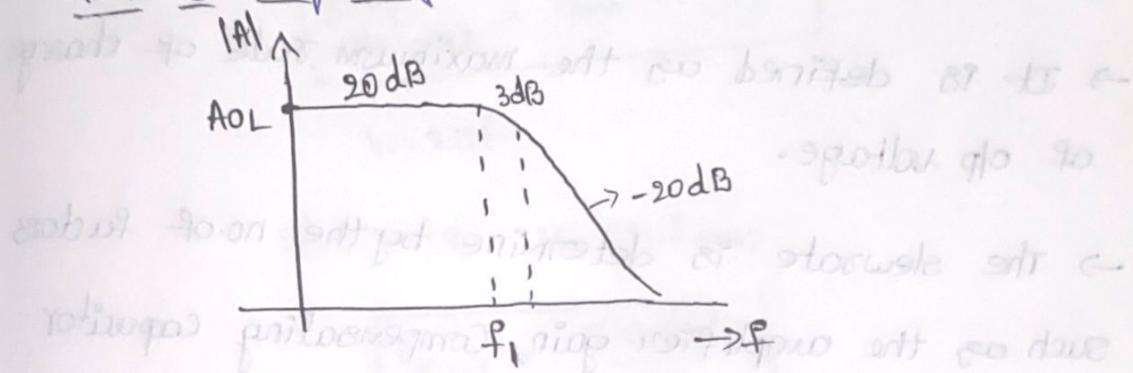
$$ii) f \ll f_1$$

$$\phi = 0^\circ$$

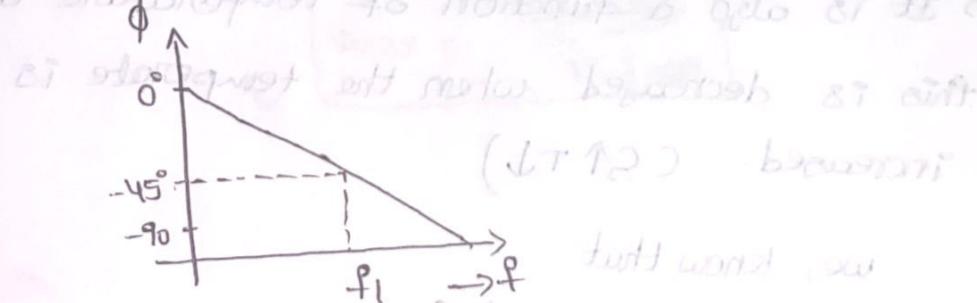
$$iii) f \gg f_1$$

$$\phi = -\pi/2 \text{ or } -90^\circ$$

Gain vs Frequency:



Phase vs Frequency:



The frequency response curve of op-amp. The gain is decreased by 20dB per decade after reaching the upper cut-off frequency.

$$|A| = \frac{\text{AOL}}{\sqrt{1 + (\frac{f}{f_1})^2}}$$

Apply log on b/s

$$\log |A| = \log \frac{\text{AOL}}{\sqrt{1 + (\frac{f}{f_1})^2}}$$

$$20 \log |A| = 20 \log (A_{OL}) - 20 \log \left(\sqrt{1 + \left(\frac{f}{f_p} \right)^2} \right)$$

FOR 741 IC, $A_{OL} = 2 \times 10^5$

iii, slew Rate :-

- slew rate is an important parameter which limits the bandwidth for large signals and it indicates how fast its output voltage can change.
- It is defined as the maximum rate of change of opv voltage.
- The slew rate is determined by the no. of factors such as the amplifier gain, compensating capacitor and the changing polarity of output voltage.
- It is also a function of temperature and this is decreased when the temperature is increased. ($C \uparrow T \downarrow$)

we, know that

$$V_{C} = \frac{1}{C} \int i dt$$

$$\text{at } t=0 \text{ to } V_{C} = \frac{i_{\max}}{C}$$

$$\therefore S = \left. \frac{dV_C}{dt} \right|_{\max}$$

→ For IC 741 i_{\max} is 15mA for $C = 30pF$

$$\left[\frac{dV_C}{dt} \right]_{\max} = \frac{i_{\max}}{C} = \frac{15 \times 10^{-6}}{\frac{30 \times 10^{-12}}{2}} = 0.5 M(V/\mu s)$$

* Effect of Sine wave on slew Rate:-

$$V_i = V_m \sin \omega t$$

$$V_o = V_m \sin \omega t$$

$$\frac{dV_o}{dt} = V_m \cos \omega t \cdot \omega \\ = V_m \omega \cos \omega t$$

at $\cos \omega t = 1$

$$\left. \frac{dV_o}{dt} \right|_{\max} = V_m \omega \text{ (V/Sec)}$$

$$\omega = 2\pi f$$

$$\text{slew rate} = V_m 2\pi f_{\max}$$

$$f_{\max} = \frac{\text{slew rate}}{2\pi V_m}$$

$$V_{\max} = \frac{\text{slew rate}}{2\pi f_{\max}}$$