Serial Adder-29-01-2021

4 bit adder

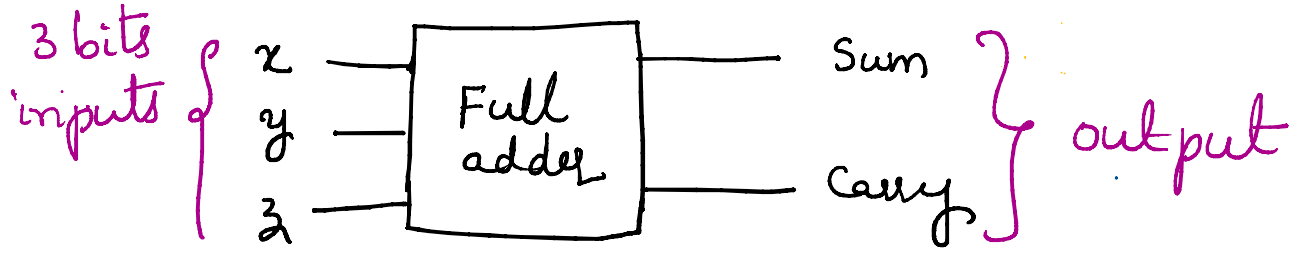
MSB ← LSB

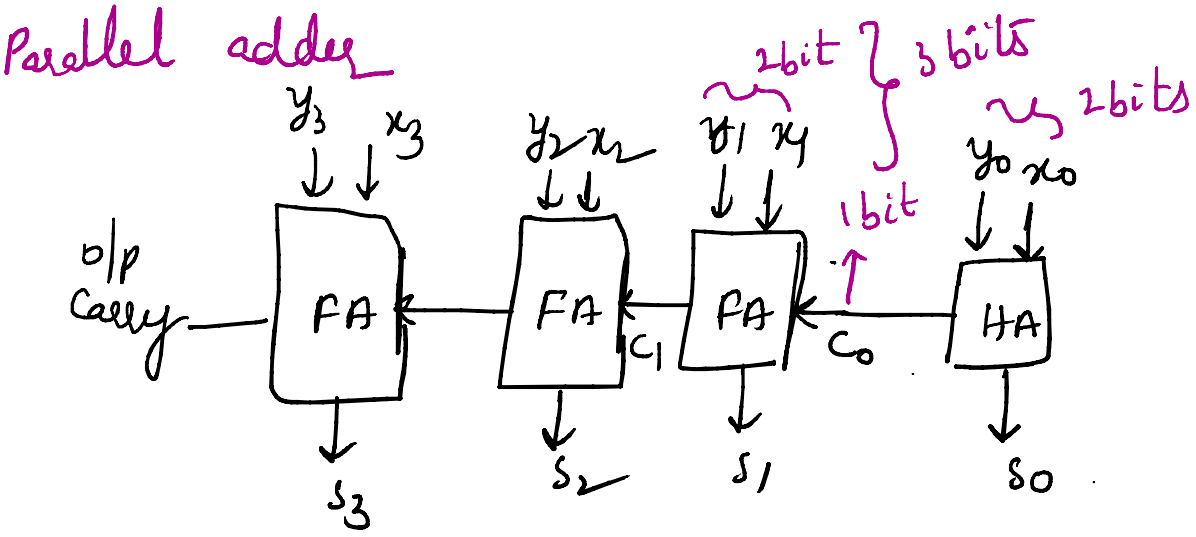
Carry: 1 1

x = 1 0 0 1

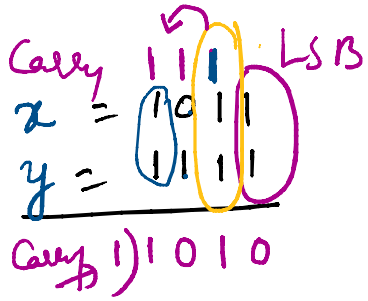
y = 1 0 1 1

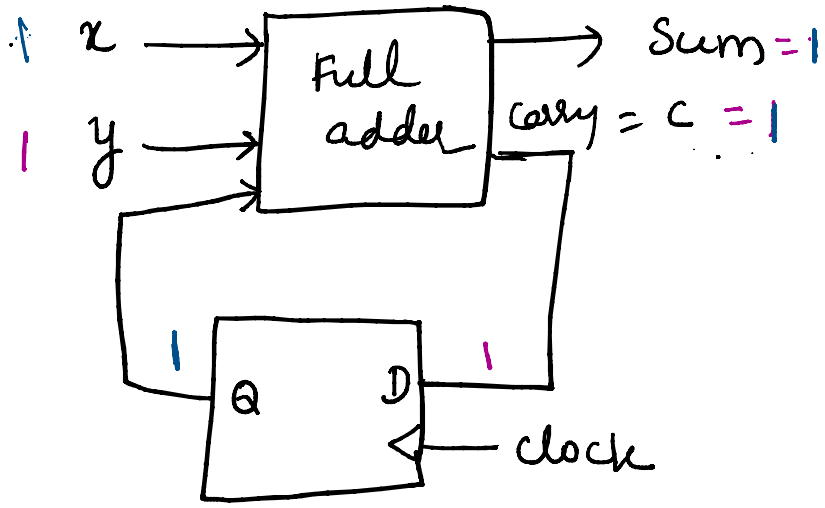
Carry → 1) 0 1 0 0





Serial adder





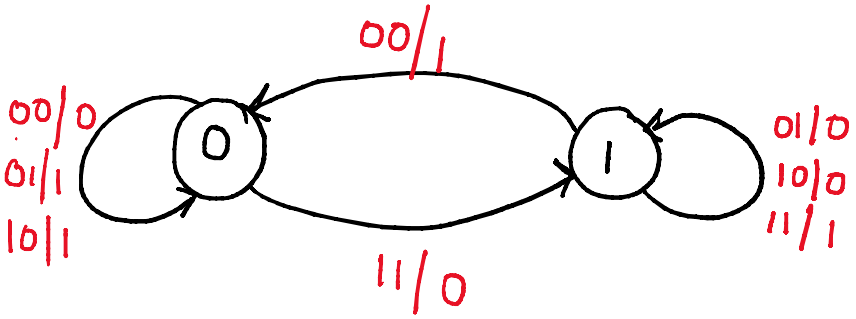
D	N.S Q(t+1)
0	0
1	1

① Design Serial adder Sequential ckt using D flip flop.

State table

Present state	x	y	Next State Carry=D	Output Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

State diagram

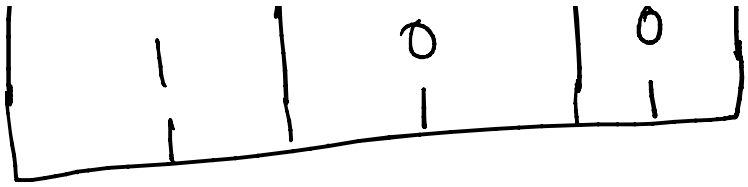


To design sequential ckt, need to follow these steps

1. State diagram
2. State table
3. Excitation table for sequential ckt
4. from excitation table, need to determine reduced form of boolean expres.
5. Draw logic diagram for the boolean expression.

D flip flop excitation table

Q Present State	Q(t+1) Next State	D
0	0	0
0	1	1
1	0	0
1	1	1



Excitation table for Serial adder (Sequential ckt)

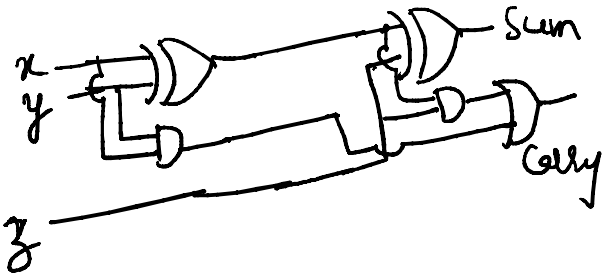
Decimal	Present state Z	x	y	Next State Carry=D	Output Sum	Excitation D flip flop
0	0	0	0	0	0	0
1	0	0	1	0	1	0
2	0	1	0	0	1	0
3	0	1	1	1	0	1
4	1	0	0	0	1	0
5	1	0	1	1	0	1
6	1	1	0	1	0	1
7	1	1	1	1	1	1

D

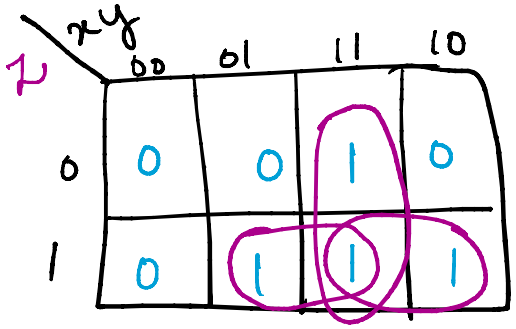
Full Adder

$Carry = Zx + Zy + xy$

$Sum = Z \oplus x \oplus y$



K map for D



ABC

Carryout = AB+BC+CA

$D = zx + xy + zy$

logic diagram