

# RTL Logic family

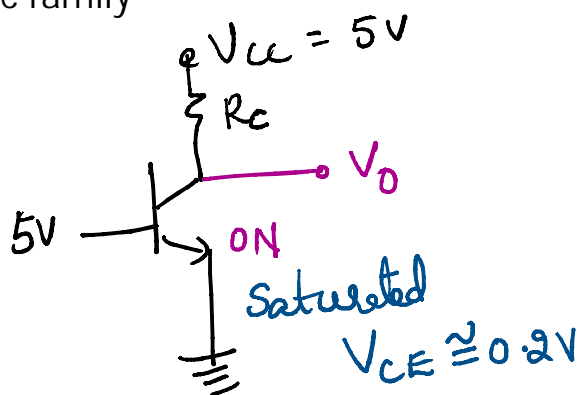


Fig: ON transistor

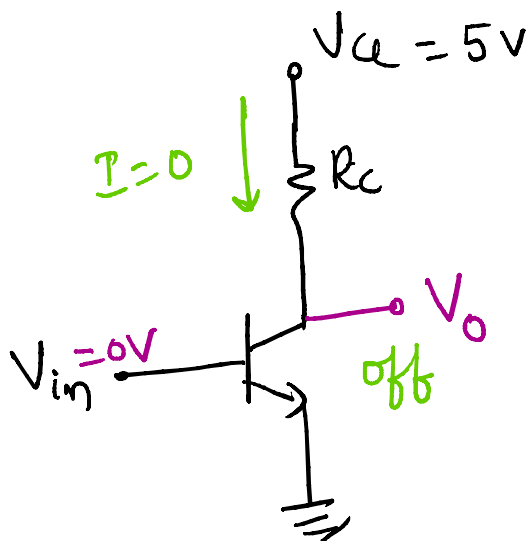
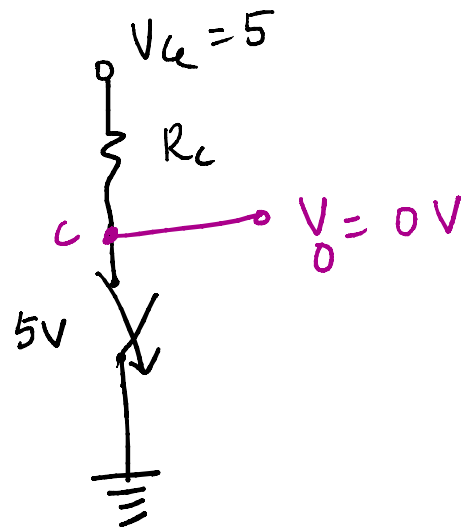
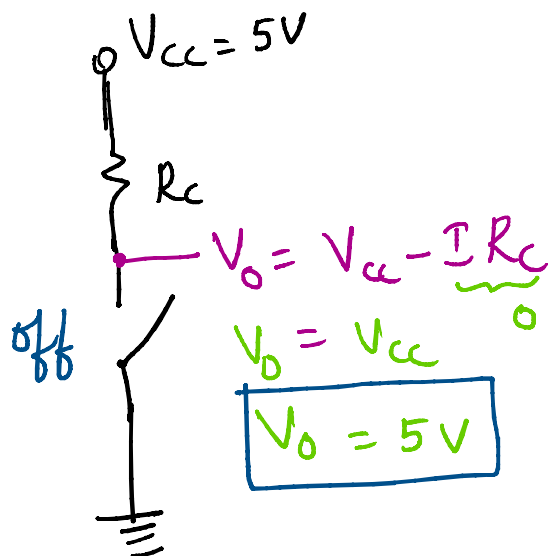
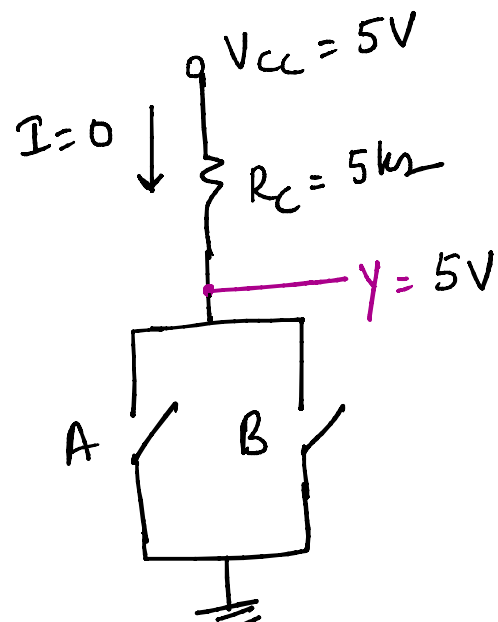
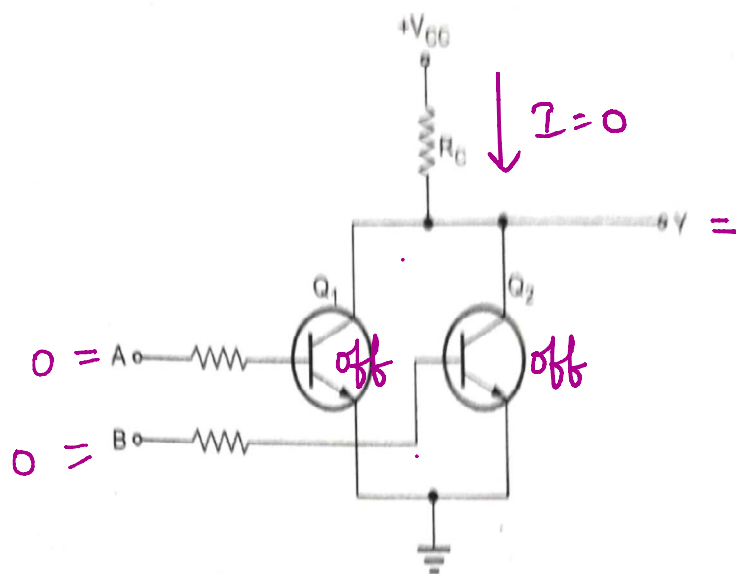
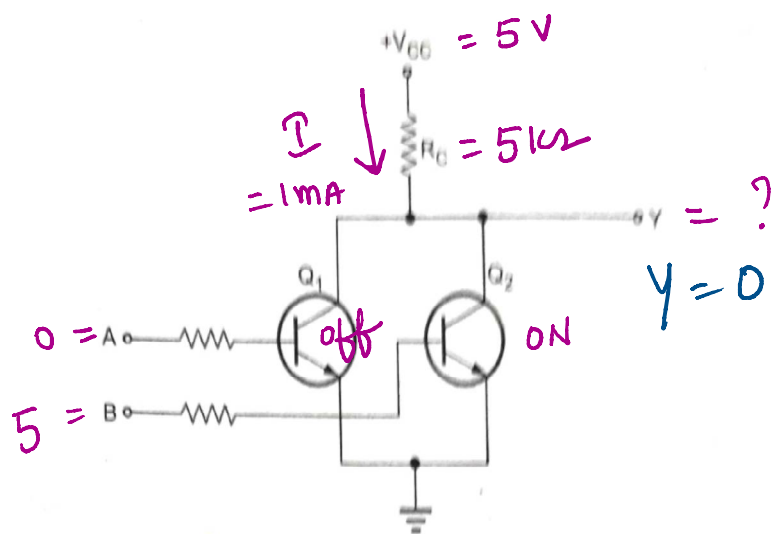


Fig: off transistor

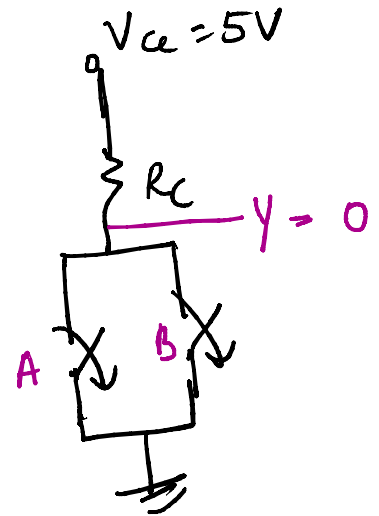
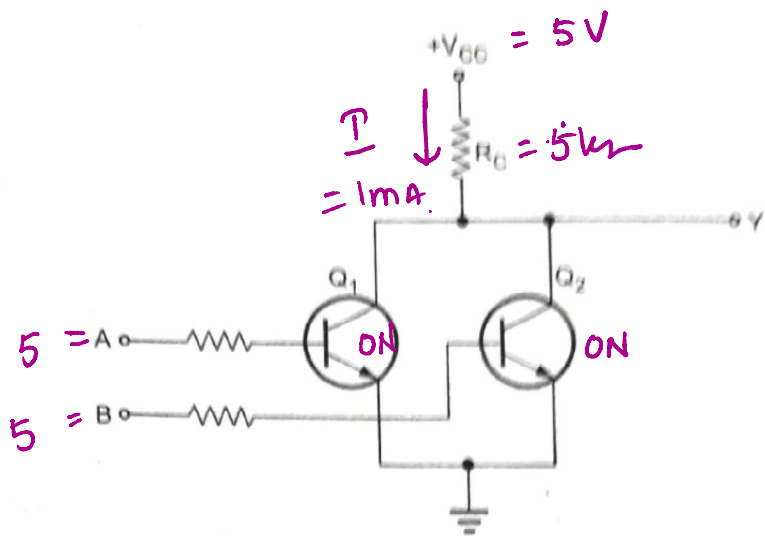
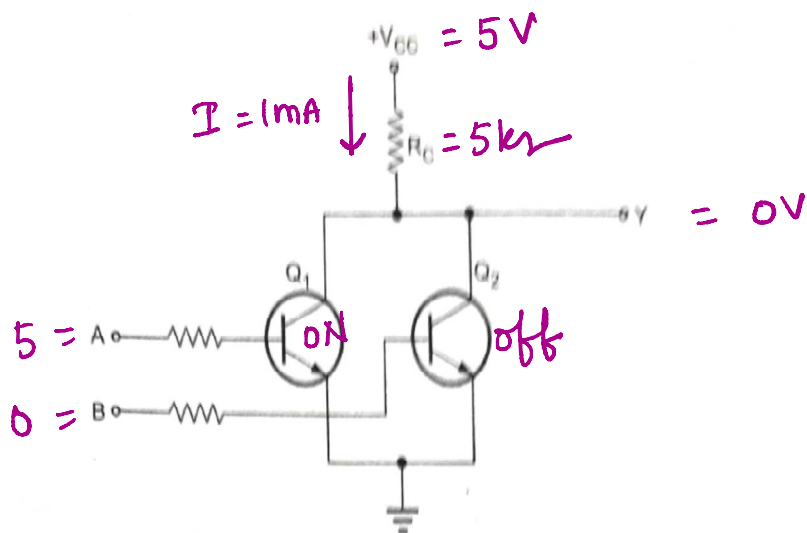




$$Y = V_{CC} - \underbrace{I_C R_C}_{= 0} = 5V$$



$$Y = V_{CC} - I R_C = 5 - 1mA \times 5k = 0$$



A	B	Y
0	0	5V
0	5	0
5	0	0
5	5	0

$\cong$  NOR gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Parameter	Value
Propagative Delay	12 nsec
Power Dissipation	30-100 mW
Noise Margin	0.2 volts
Fan-out	4

min  $P_d \rightarrow$  Speed  $\uparrow$   
 less  $P_{diss}$   
 High  
 4

Table 7.3 Specifications for RTL gate

### 7.3.4 Wire-AND Connection

The RTL has a capacity called **wire - AND**. Since the output is effectively a transistor, two outputs can be wired together. This is illustrated in Fig. 7.6.

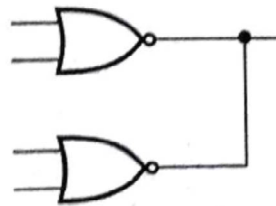


Fig. 7.6 Wired AND RTL NOR gates