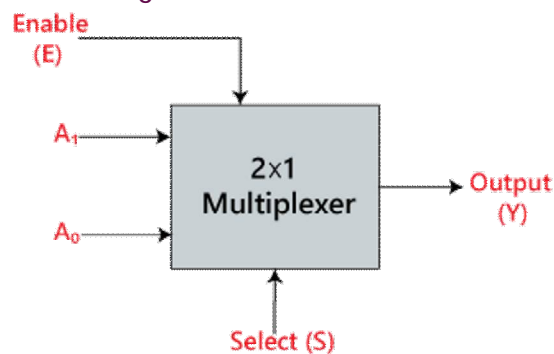# Multiplexer

## Multiplexer

A multiplexer is a combinational circuit that has $2^n$ input lines and a single output line. Simply, the multiplexer is a multi-input and single-output combinational circuit. The binary information is received from the input lines and directed to the output line. On the basis of the values of the selection lines, one of these data inputs will be connected to the output.

Unlike encoder and decoder, there are n selection lines and $2^n$ input lines. So, there is a total of $2^N$ possible combinations of inputs. A multiplexer is also treated as **Mux**.

## 2×1 Multiplexer:

In 2×1 multiplexer, there are only two inputs, i.e., $A_0$ and $A_1$, 1 selection line, i.e., $S_0$ and single outputs, i.e., Y. On the basis of the combination of inputs which are present at the selection line $S^0$, one of these 2 inputs will be connected to the output. The block diagram and the truth table of the 2×1 multiplexer are given below.
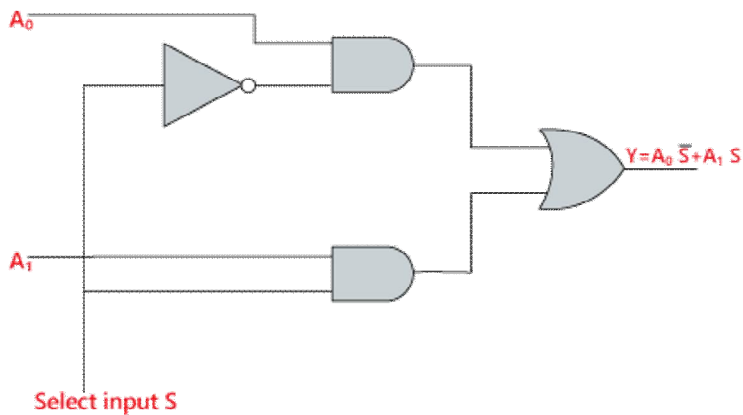
Block Diagram:



Truth Table:

| INPUTS | Output |
|--------|--------|
| $S_0$ | Y |
| 0 | $A_0$ |
| 1 | $A_1$ |

The logical expression of the term Y is as follows:
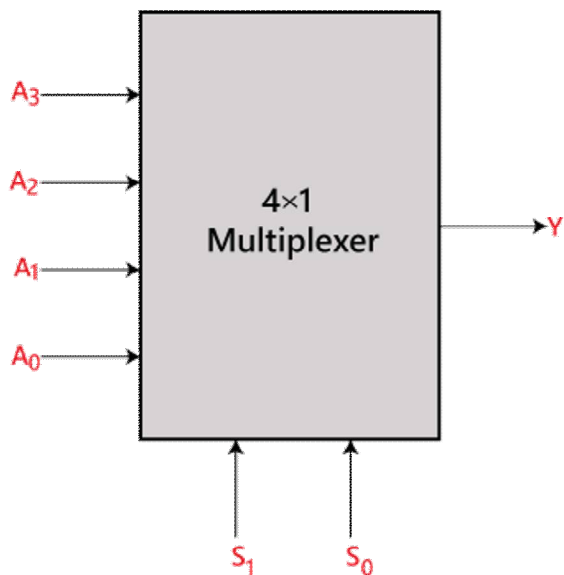
$Y = S_0'.A_0 + S_0.A_1$

Logical circuit of the above expression is given below:



4×1 Multiplexer:

In the 4×1 multiplexer, there is a total of four inputs, i.e., $A_0$, $A_1$, $A_2$, and $A_3$, 2 selection lines, i.e., $S_0$ and $S_1$ and single output, i.e., Y. On the basis of the combination of inputs that are present at the selection lines $S^0$ and $S_1$, one of these 4 inputs are connected to the output. The block diagram and the truth table of the 4×1 multiplexer are given below.
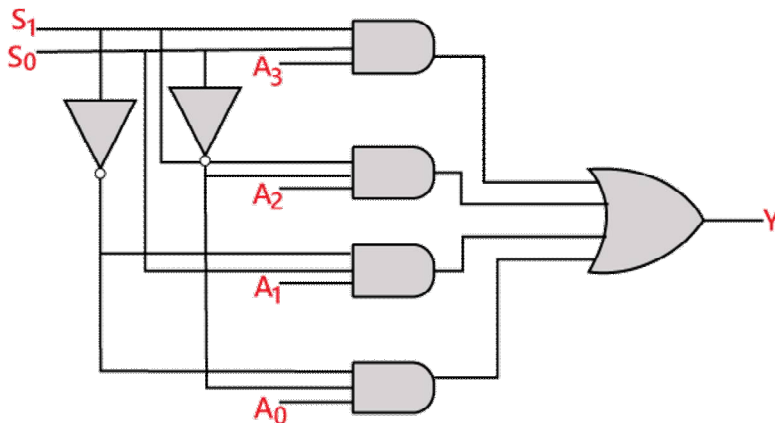
Block Diagram:



Truth Table:

| INPUTS | | Output |
|---|---|---|
| $S_1$ | $S_0$ | Y |
| 0 | 0 | $A_0$ |
| 0 | 1 | $A_1$ |
| 1 | 0 | $A_2$ |
| 1 | 1 | $A_3$ |

The logical expression of the term Y is as follows:

$Y = S_1' \ S_0' \ A_0 + S_1' \ S_0 \ A_1 + S_1 \ S_0' \ A_2 + S_1 \ S_0 \ A_3$

Logical circuit of the above expression is given below:



## 8 to 1 Multiplexer

In the 8 to 1 multiplexer, there are total eight inputs, i.e., $A_0$, $A_1$, $A_2$, $A_3$, $A_4$, $A_5$, $A_6$, and $A_7$, 3 selection lines, i.e., $S_0$, $S_1$ and $S_2$ and single output, i.e., Y. On the basis of the combination of inputs that are present at the selection lines $S^0$, $S^1$, and $S_2$, one of these 8 inputs are connected to the output. The block diagram and the truth table of the 8 ×1 multiplexer are given below.

Block Diagram:



$Y = A_7$

NOT = 3

AND = 8

no $-(8 \ \text{ila}) \ OR$

$AND = 8$

$OR = (8\ i/p)\ OR$

Select lines
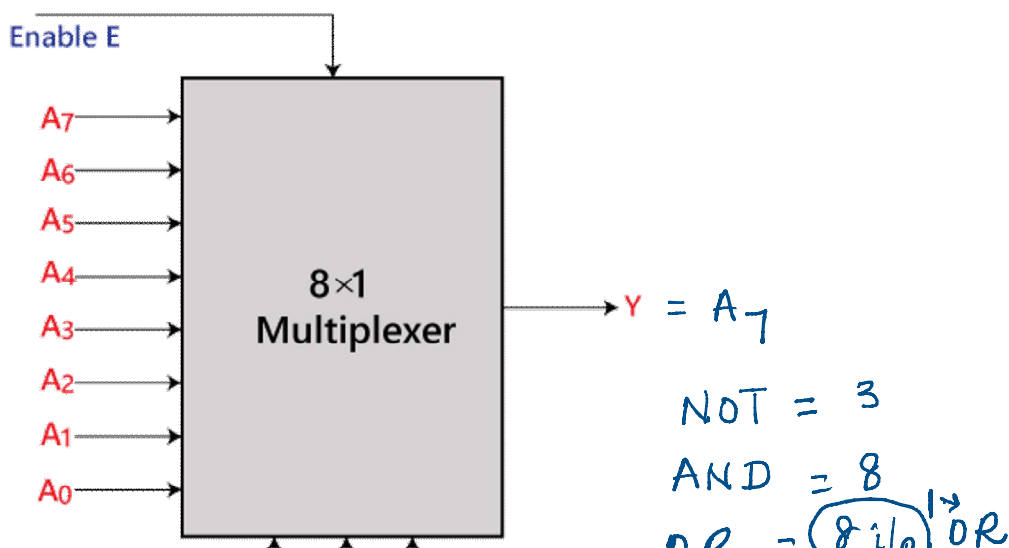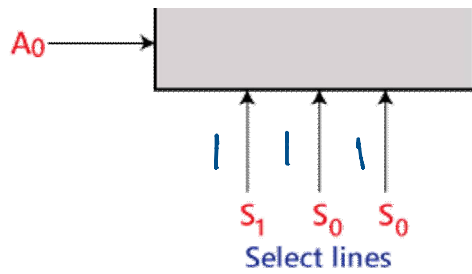
Truth Table:

| INPUTS | | | Output |
|---|---|---|---|
| $S_2$ | $S_1$ | $S_0$ | Y |
| 0 | 0 | 0 | $A_0$ |
| 0 | 0 | 1 | $A_1$ |
| 0 | 1 | 0 | $A_2$ |
| 0 | 1 | 1 | $A_3$ |
| 1 | 0 | 0 | $A_4$ |
| 1 | 0 | 1 | $A_5$ |
| 1 | 1 | 0 | $A_6$ |
| 1 | 1 | 1 | $A_7$ |

The logical expression of the term Y is as follows:

$Y = S_0'.S_1'.S_2'.A_0 + S_0.S_1'.S_2'.A_1 + S_0'.S_1.S_2'.A_2 + S_0.S_1.S_2'.A_3$
$+ S_0'.S_1'.S_2\ A_4 + S_0.S_1'.S_2\ A_5 + S_0'.S_1.S_2\ .A_6 + S_0.S_1.S_3.A_7$

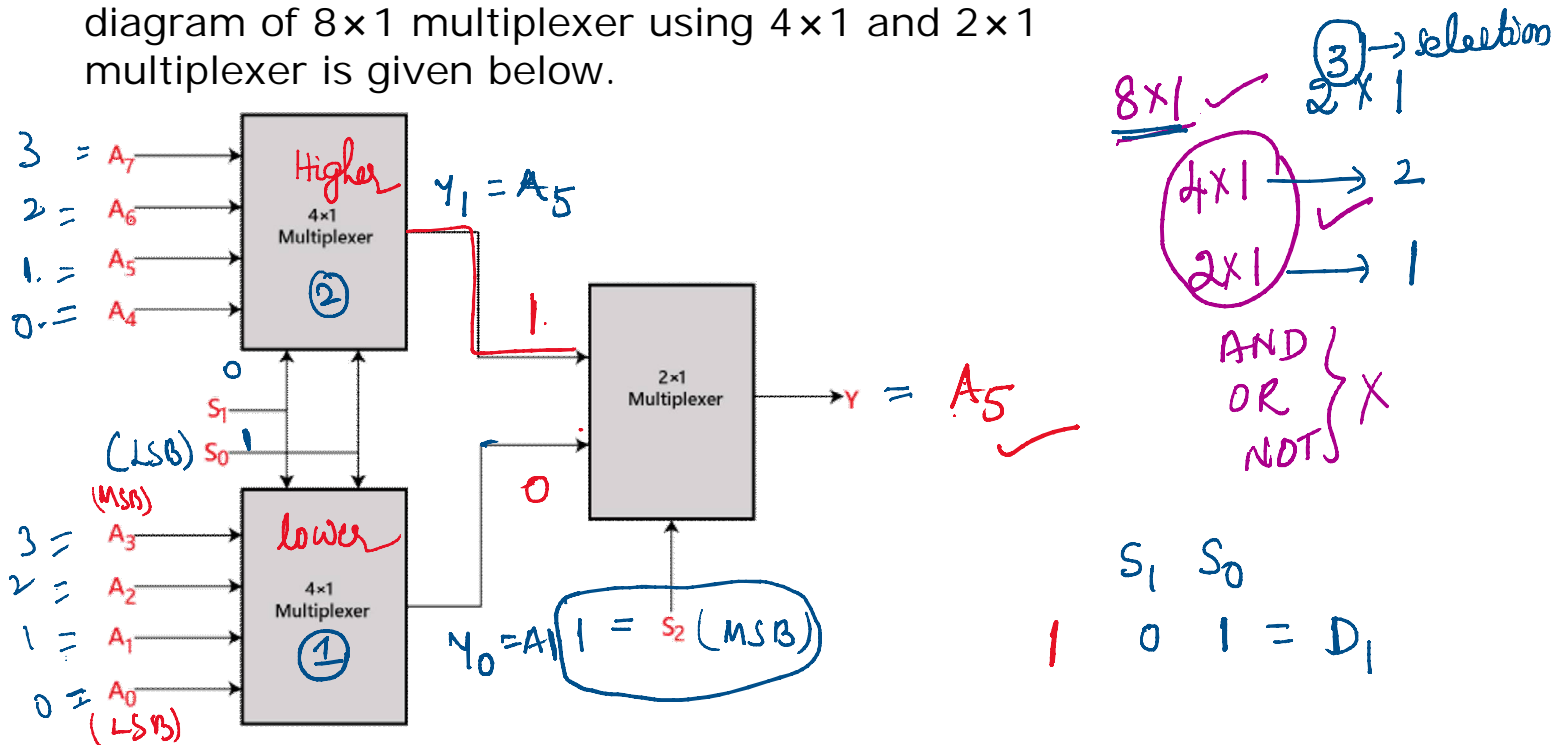Logical circuit of the above expression is given below:



$Y = A_5$
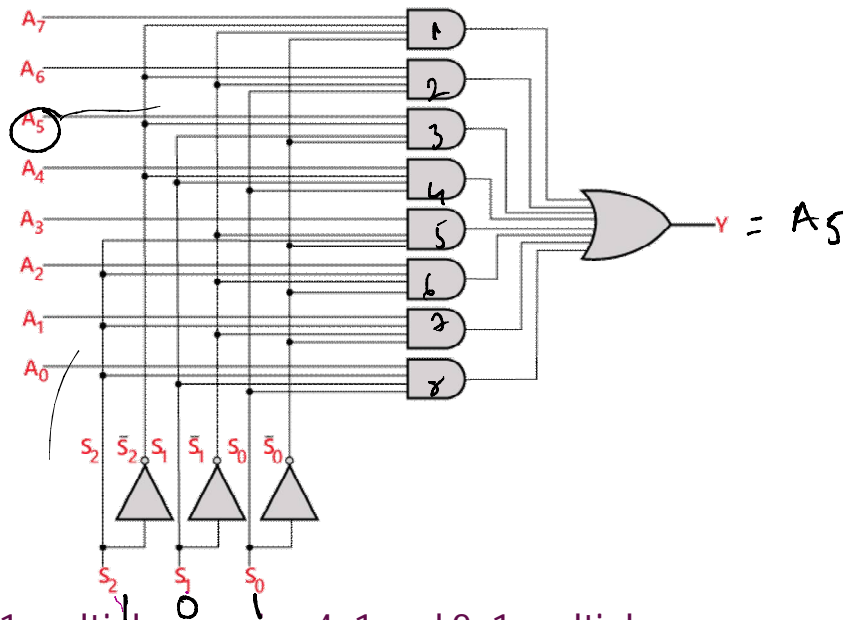
8×1 multiplexer using 4×1 and 2×1 multiplexer

We can implement the 8×1 multiplexer using a lower order multiplexer. To implement the 8×1 multiplexer, we need two 4×1 multiplexers and one 2×1 multiplexer. The 4×1 multiplexer has 2 selection lines, 4 inputs, and 1 output.

The 2×1 multiplexer has only 1 selection line.
For getting 8 data inputs, we need two 4×1 multiplexers.
The 4×1 multiplexer produces one output. So, in order to
get the final output, we need a 2×1 multiplexer. The block
diagram of 8×1 multiplexer using 4×1 and 2×1
multiplexer is given below.

8×1 ✓    3 → selection
         2×1

(4×1) → 2
        ✓
(2×1) → 1

AND ⎫
OR  ⎬ X
NOT ⎭

$3 = A_7$    Higher   $Y_1 = A_5$
$2 = A_6$    4×1 Multiplexer ②
$1. = A_5$
$0. = A_4$

$S_1$
(LSB) $S_0$ 1
(MSB)

$3 = A_3$    lower
$2 = A_2$    4×1 Multiplexer ①
$1 = A_1$    $Y_0 = A_1$ | 1 = $S_2$ (MSB)
$0 = A_0$
(LSB)

2×1 Multiplexer → Y = $A_5$

1.

O

$S_1$ $S_0$
1   0   1 = $D_1$

16 to 1 Multiplexer

In the 16 to 1 multiplexer, there are total of 16 inputs, i.e.,
$A_0$, $A_1$, ..., $A_{16}$, 4 selection lines, i.e., $S_0$, $S_1$, $S_2$, and $S_3$ and
single output, i.e., Y. On the basis of the combination of
inputs that are present at the selection lines $S^0$, $S^1$, and $S_2$,
one of these 16 inputs will be connected to the output. The
block diagram and the truth table of the 16×1
Block Diagram:

$S_0$ $S_1$ $S_2$ $S_3$

1 0 1 1 = 11

1 1 0 1 = 13

Y = $A_{11}$ $A_{13}$ ✓
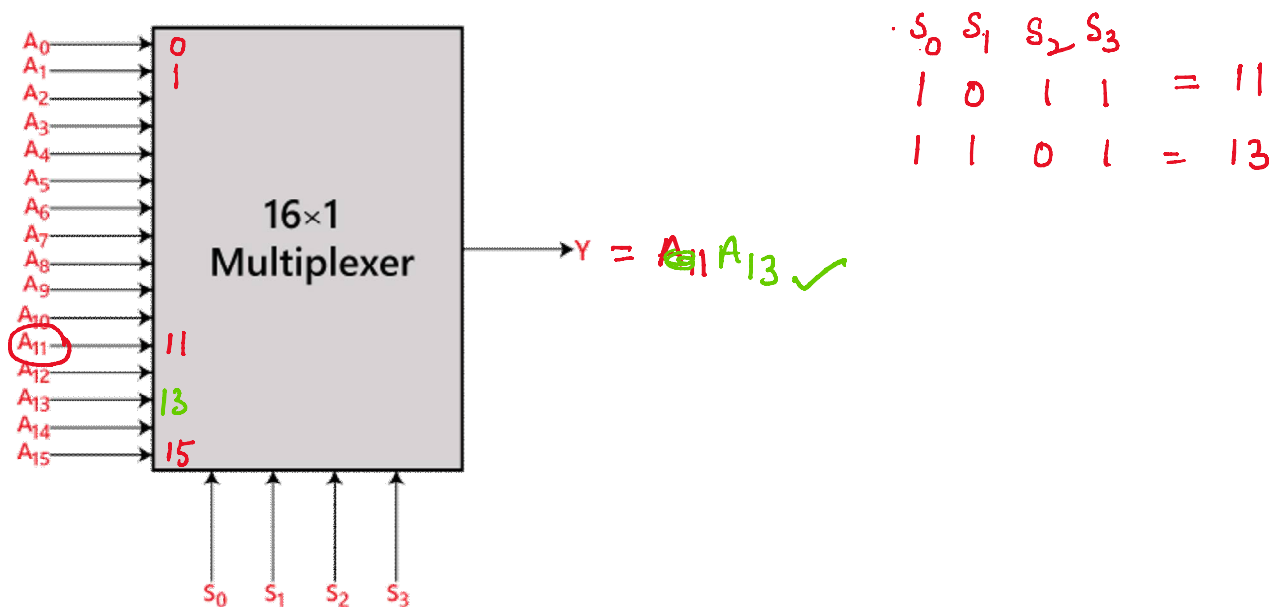
**Truth Table:**

| INPUTS | | | | Output |
|---|---|---|---|---|
| $S_0$ | $S_1$ | $S_2$ | $S_3$ | Y |
| 0 | 0 | 0 | 0 | $A_0$ |
| 0 | 0 | 0 | 1 | $A_1$ |
| 0 | 0 | 1 | 0 | $A_2$ |
| 0 | 0 | 1 | 1 | $A_3$ |
| 0 | 1 | 0 | 0 | $A_4$ |
| 0 | 1 | 0 | 1 | $A_5$ |
| 0 | 1 | 1 | 0 | $A_6$ |
| 0 | 1 | 1 | 1 | $A_7$ |
| 1 | 0 | 0 | 0 | $A_8$ |
| 1 | 0 | 0 | 1 | $A_9$ |
| 1 | 0 | 1 | 0 | $A_{10}$ |
| 1 | 0 | 1 | 1 | $A_{11}$ |
| 1 | 1 | 0 | 0 | $A_{12}$ |
| 1 | 1 | 0 | 1 | $A_{13}$ |
| 1 | 1 | 1 | 0 | $A_{14}$ |
| 1 | 1 | 1 | 1 | $A_{15}$ |

The logical expression of the term Y is as follows:

$Y=A_0.S_0'.S_1'.S_2'.S_3'+A_1.S_0'.S_1'.S_2'.S_3+A_2.S_0'.S_1'.S_2.S_3'+A_3.S_0'.S_1'.S_2.S_3$
$+A_4.S_0'.S_1.S_2'.S_3'+A_5.S_0'.S_1.S_2'.S_3+A_6.S_1.S_2.S_3'+A_7.S_0'.S_1.S_2.S_3$
$+A_8.S_0.S_1'.S_2'.S_3'+A_9.S_0.S_1'.S_2'.S_3+Y_{10}.S_0.S_1'.S_2.S_3'+A_11.S_0.S_1'.S_2.S_3+A_12$
$S_0.S_1.S_2'.S_3'+A_13.S_0.S_1.S_2'.S_3+A_14.S_0.S_1.S_2.S_3'+A_15.S_0.S_1.S_2'.S_3$
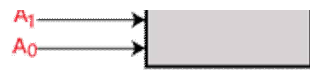
Logical circuit of the above expression is given below:
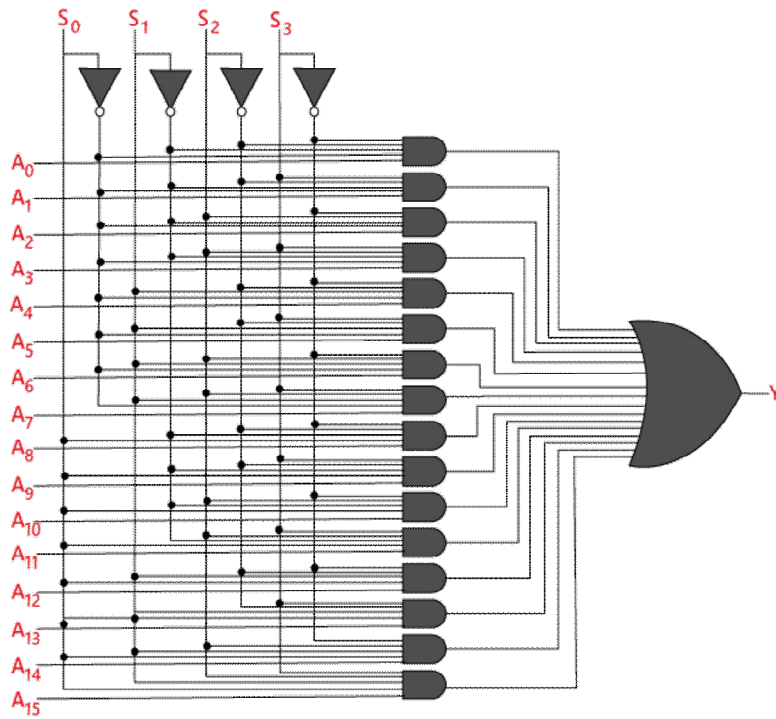
**16×1 multiplexer using 8×1 and 2×1 multiplexer**

We can implement the 16×1 multiplexer using a lower order multiplexer. To implement the 8×1 multiplexer, we need two 8×1 multiplexers and one 2×1 multiplexer. The 8×1 multiplexer has 3 selection lines, 4 inputs, and 1 output. The 2×1 multiplexer has only 1 selection line. For getting 16 data inputs, we need two 8 ×1 multiplexers. The 8×1 multiplexer produces one output. So, in order to get the final output, we need a 2×1 multiplexer. The block diagram of 16×1 multiplexer using 8×1 and 2×1 multiplexer is given below.



16X1 MUX

8X1 ⟶ 2

2X1 ⟶ 1

| $S_3$ | $S_2$ | $S_1$ | $S_0$ |
|---|---|---|---|
| 1 | 1 | 0 | 1 | = 13 |

**8X1**

$S_2$ $S_1$ $S_0$

1 0 1 = 5

2X1

$A_1$ $\longrightarrow$

$A_0$ $\longrightarrow$

$$\frac{2 \times 1}{}$$

| $S_3$ | $Y$ |
|-------|-----|
| 0 | $D_0 = A_5$ |
| 1 | $D_1 = A_{13}$ |