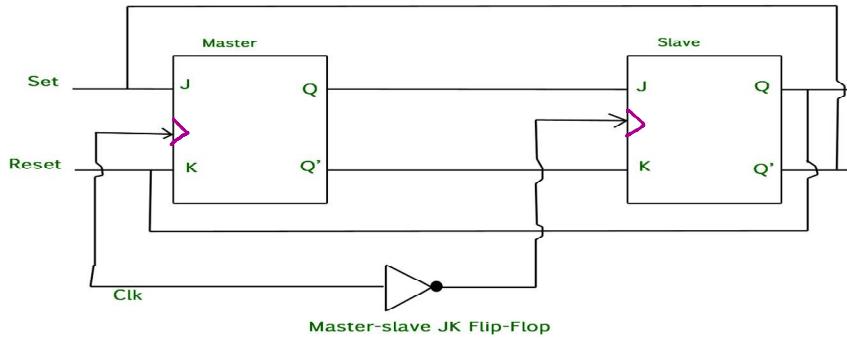


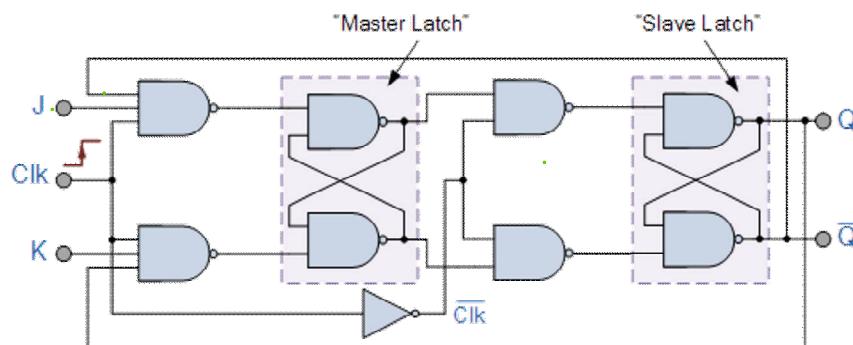
The Master-Slave JK Flip-flop



The Master-Slave Flip-Flop can be constructed for any type of FLIP FLOP

The **Master-Slave Flip-Flop** is basically two gated SR flip-flops connected together in a series configuration with the slave having an inverted clock pulse. The outputs from Q and Q' from the "Slave" flip-flop are fed back to the inputs of the "Master" with the outputs of the "Master" flip flop being connected to the two inputs of the "Slave" flip flop. This feedback configuration from the slave's output to the master's input gives the characteristic toggle of the JK flip flop as shown below.

The Master-Slave JK Flip Flop



The input signals J and K are connected to the gated "master" SR flip flop which "locks" the input condition while the clock (Clk) input is "HIGH" at logic level "1". As the clock input of the "slave" flip flop is the inverse (complement) of the "master" clock input, the "slave" SR flip flop does not toggle. The outputs from the "master" flip flop are only "seen" by the gated "slave" flip flop when the clock input goes "LOW" to logic level "0".

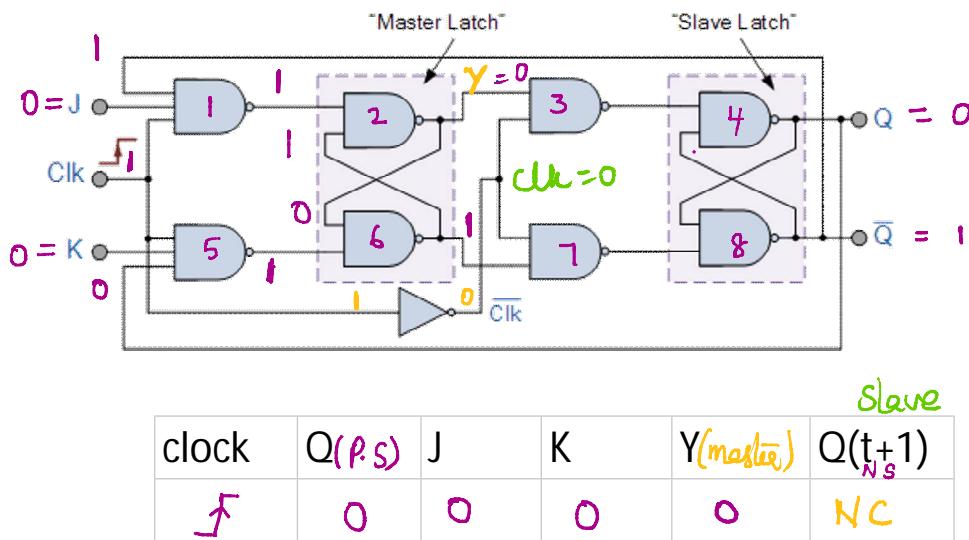
When the clock is "LOW", the outputs from the "master" flip flop

are latched and any additional changes to its inputs are ignored. The gated "slave" flip flop now responds to the state of its inputs passed over by the "master" section.

Then on the "Low-to-High" transition of the clock pulse the inputs of the "master" flip flop are fed through to the gated inputs of the "slave" flip flop and on the "High-to-Low" transition the same inputs are reflected on the output of the "slave" making this type of flip flop edge or pulse-triggered.

Then, the circuit accepts input data when the clock signal is "HIGH", and passes the data to the output on the falling-edge of the clock signal. In other words, the **Master-Slave JK Flip flop** is a "Synchronous" device as it only passes data with the timing of the clock signal.

In the next tutorial about **Sequential Logic Circuits**, we will look at *Multivibrators* that are used as waveform generators to produce the clock signals to switch sequential circuits.



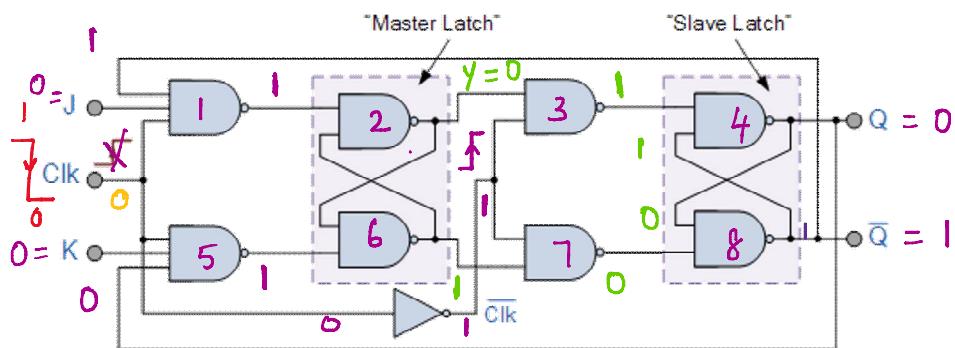
$\text{NC} = \text{No change state}$
 $\text{PS} = \text{Present state } Q$
 $\text{NS} = \text{Next state } Q(t+1)$

- ① +ve clock pulse applied to master then master is in active condition, but slave flip flop is in inactive (+ve pulse is passed through inverter then it becomes -ve pulse)

② -ve clock pulse is applied to master flip flop
 then master flip flop is in inactive condition
 but slave flip flop is in active condition
 (-ve clock pulse is passed through an inverter then
 it becomes +ve pulse).

Slave will copy the action of master.

clock	Q	J	K	Y	Q(t+1)

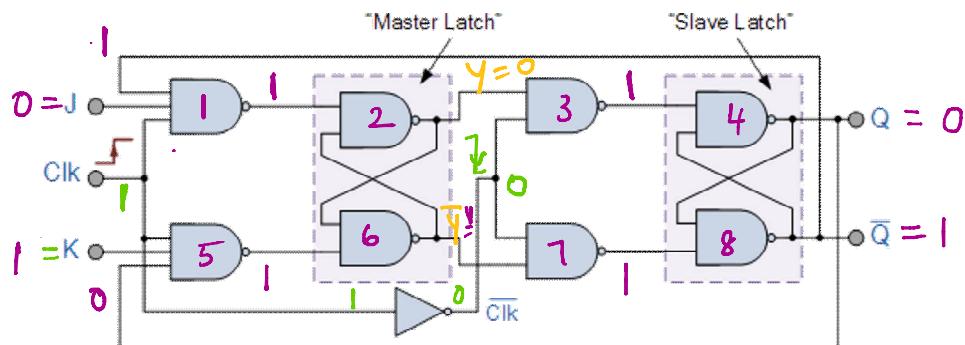


clock	Q (ps)	J	K	Y	Q(t+1)
+	0	0	0	NC	0

clock	Q	J	K	y	Q(t+1)
F	0	0	0	0	NC
E	0	0	0	NC	0

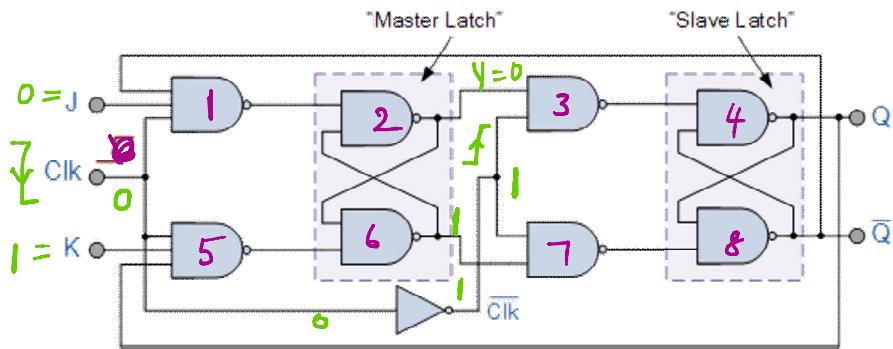
Master flip flop active & slave flip flop inactive

Master flip flop inactive but Slave will copy the action of master flip flop



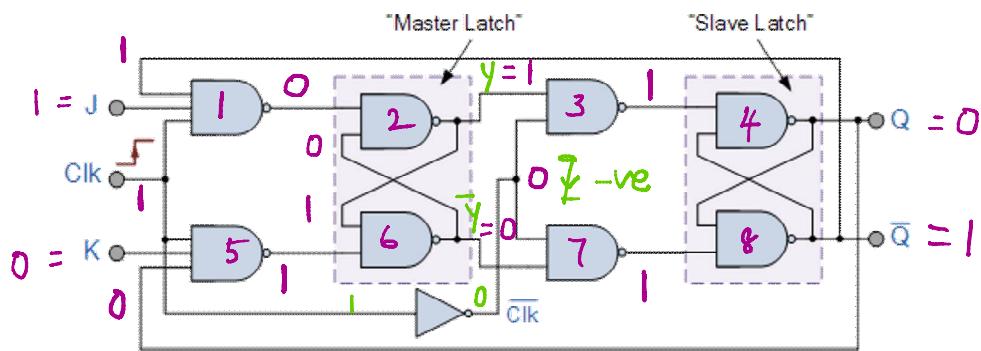
clock	Q	J	K	Y	Q(t+1)
F	0	0	1	0	NC
E	0	0	0	0	0

Master active & slave inactive because Master flip flop we apply +ve clock pulse but slave flip flop -ve clock pulse.

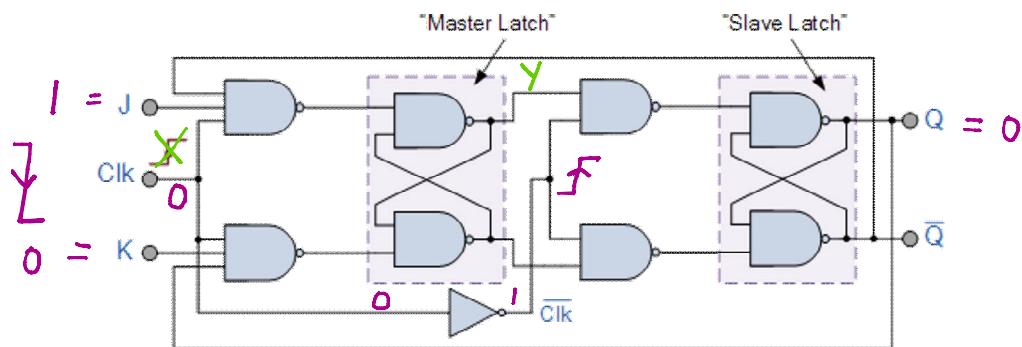


clock	$Q(P_S)$	J	K	$y(\text{master})$	$Q(t+1)$
↓	0	0	1	NC	0

clock	Q	J	K	y	$Q(t+1)$
↑	0	0	1	0	NC
↓	0	0	1	NC	0

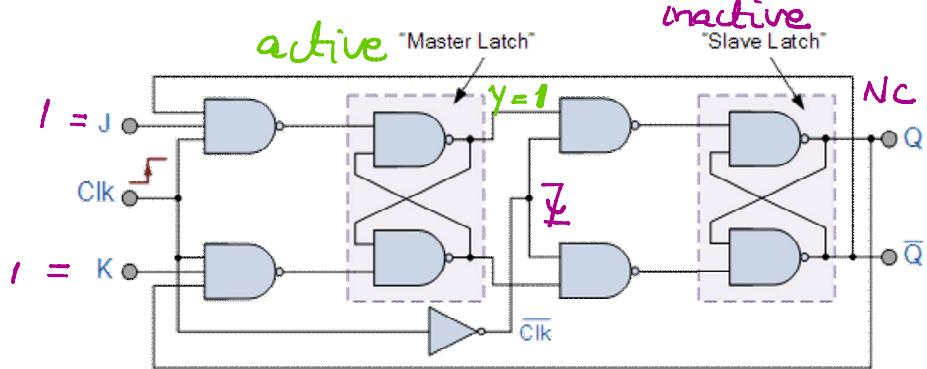


clock	Q	J	K	$y(\text{master})$	$Q(t+1)$ <i>slave</i>
\downarrow	0	1	0	1	NC



clock	$Q(p-s)$	J	K	$y(\text{master})$	$Q(t+1)$
\downarrow	0	1	0	NC	1

Present state $Q = 0$



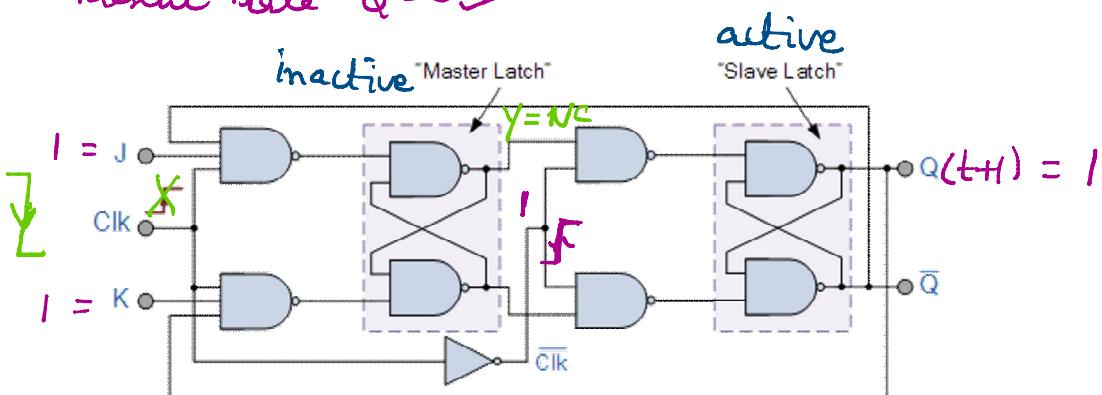
$$J=k=1 \quad Q=0$$

$$Q(t+1) = 1$$

$$J=k=1 \quad Q=1$$

$$Q(t+1) = 0$$

Present state $Q = 0$

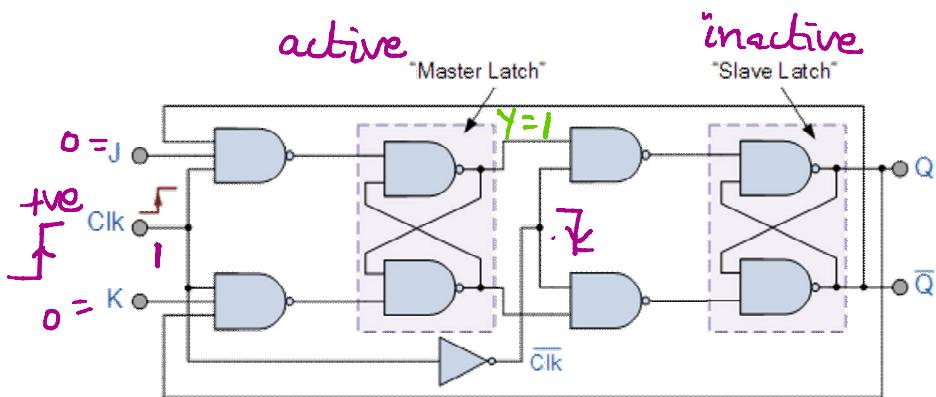


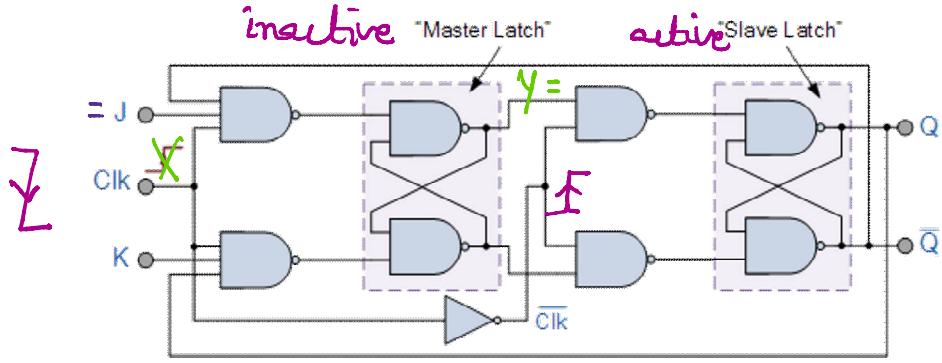
Present state (Q) = 1

$$J=0, K=0$$

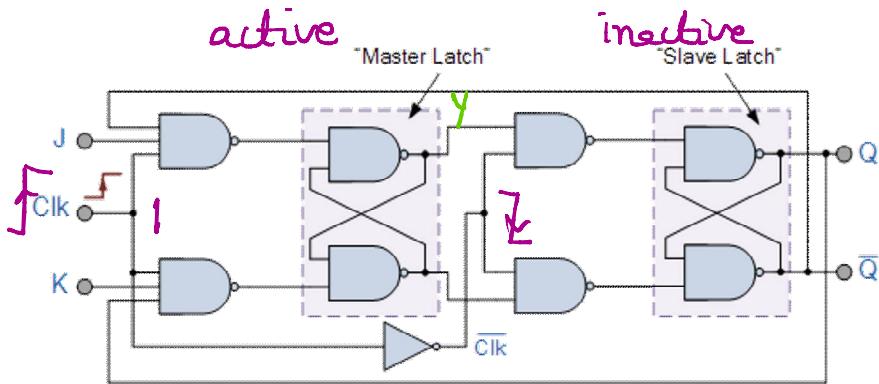
$$Y = 1:$$

$$Q(t+1) = NC$$

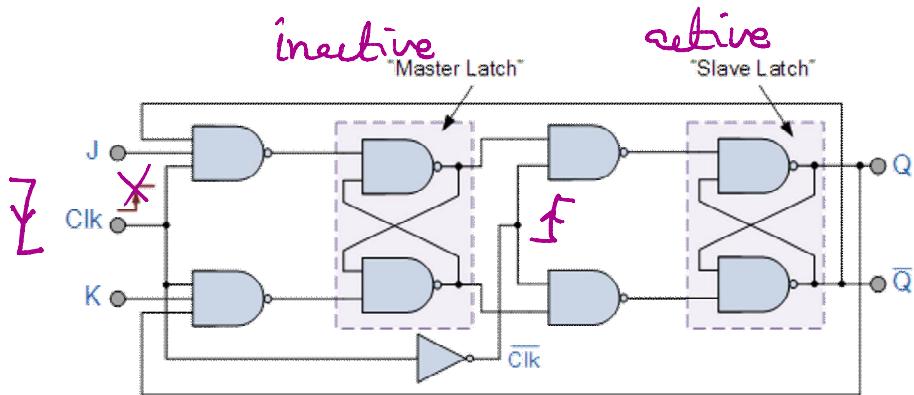




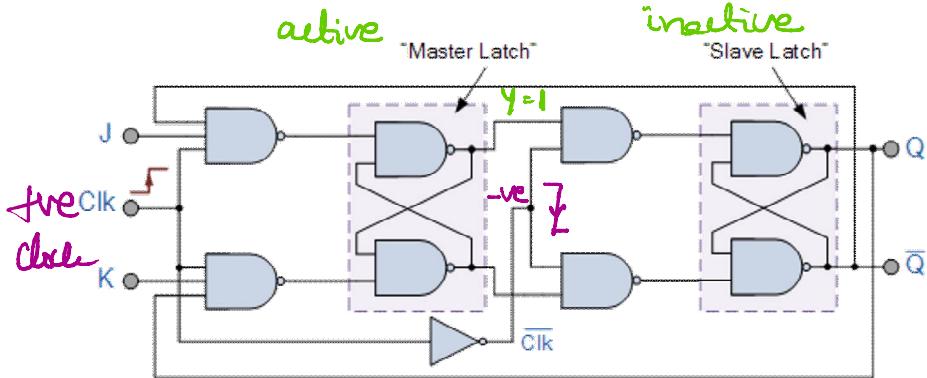
Present state ($Q = 0$)
 $J = 0, K = 0$
 $y = 1$
 $Q(t+1) = 1$



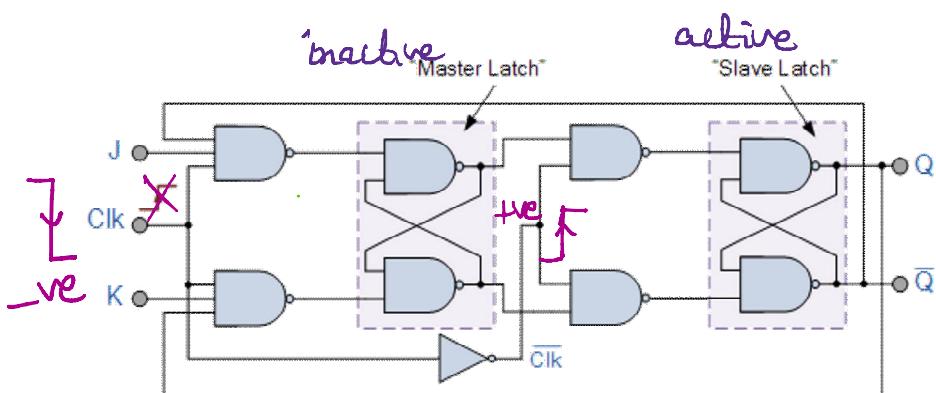
Present state $Q = 1$
 $J = 0, K = 1$
 $y = 0$
 $Q(t+1) = NC$



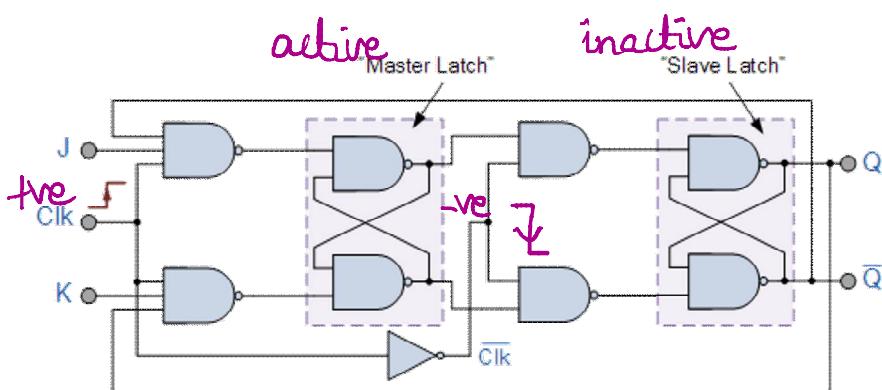
Present state $Q = 0$
 $J = 0, K = 1$
 $y = NC$
 $Q(t+1) = 0$



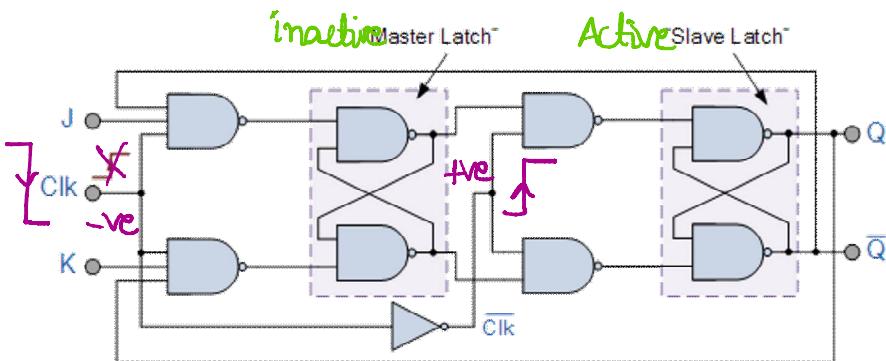
Present State $Q = 1$
 $J = 1, K = 0$
 $Y = 1$
 $Q(t+1) = NC$



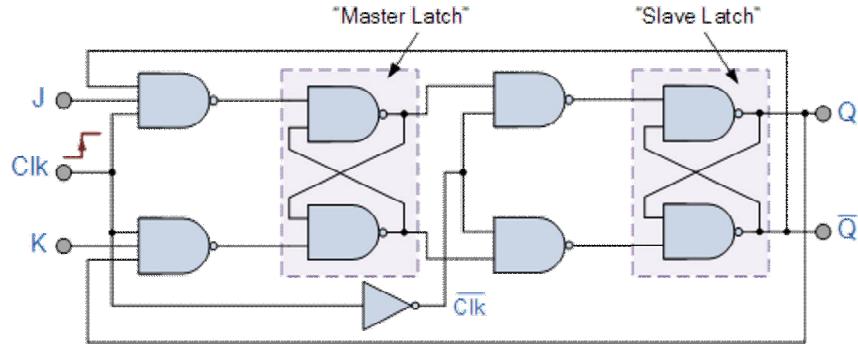
Present State ($Q = 1$)
 $, J = 1, K = 0$
 $Y = NC$
 $Q(t+1) = 1$



Present State ($Q = 1$)
 $J = 1, K = 1$
 $Y = 0$
 $Q(t+1) = NC$



Present State ($Q = 1$)
 $J = 1, K = 1$
 $Y = NC$
 $Q(t+1) = 0$



clock	Q	J	K	Y	Q(t+1)
↓	0	0	0	0	NC
↗	0	0	0	NC	0
↓	0	0	1	0	NC
↗	0	0	1	NC	0
↓	0	1	0	1	NC
↗	0	1	0	NC	1
↓	0	1	1	1	NC
↗	0	1	1	NC	1
↓	1	0	0	1	NC
↗	1	0	0	NC	1
↓	1	0	1	0	NC
↗	1	0	1	0	NC
↓	1	1	0	1	NC
↗	1	1	0	NC	1
↓	1	1	1	0	NC
↗	1	1	1	NC	0

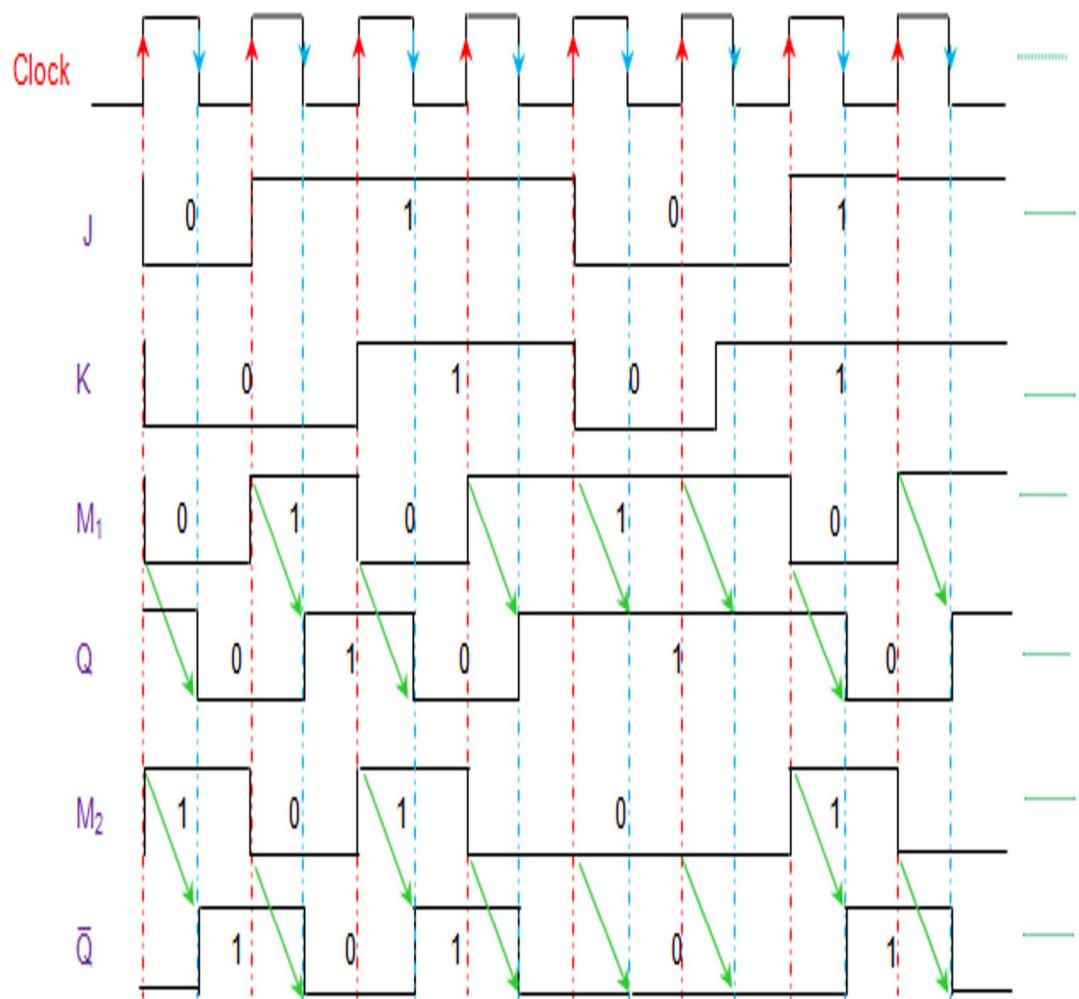


Figure 3 Timing diagram for master-slave JK flip-flop