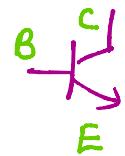
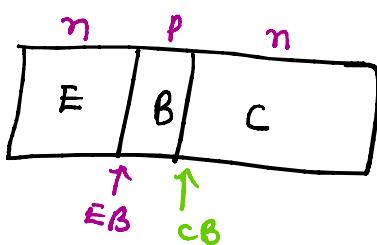


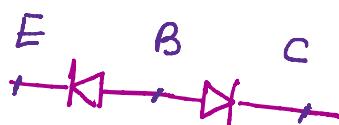
TTL Logic Family

Transistor (n-p-n) Transistor

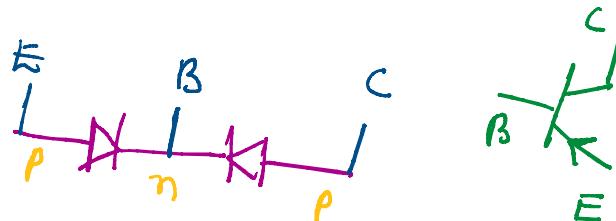
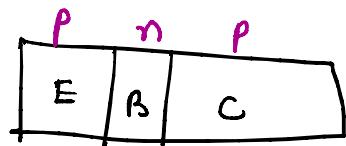


→ Arrow indicates
Conventional
current direction

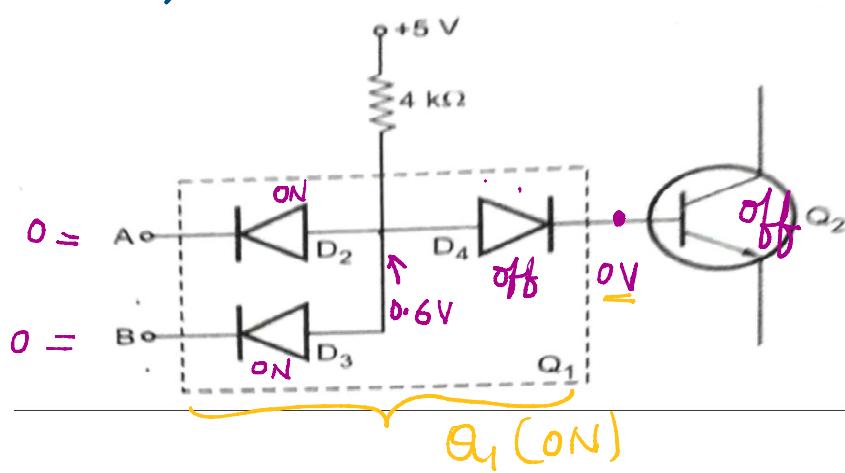
Transistor (n-p-n)



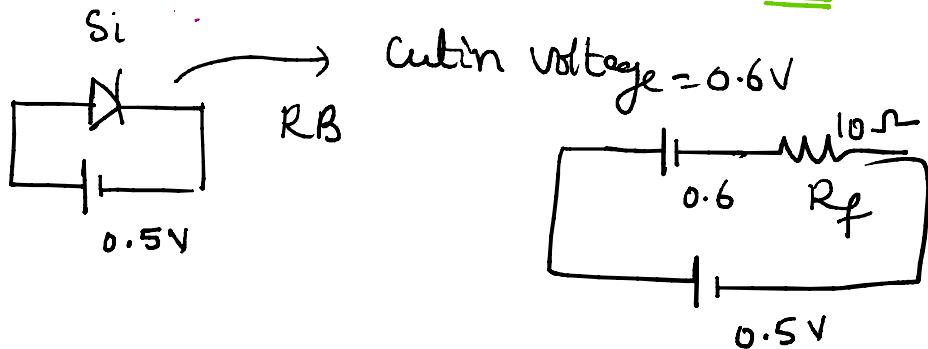
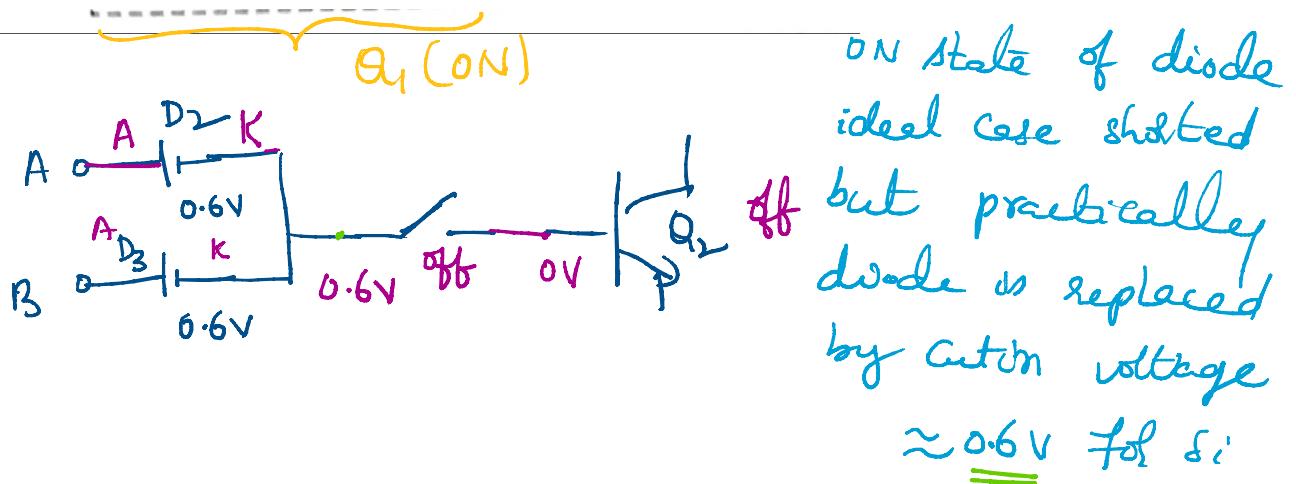
Pnp transistor



Diode equivalent of Q₁ transistor

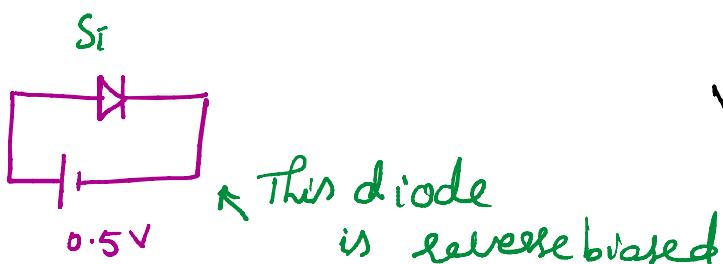


Diodes D₂ & D₃
represents Emitter
base junction of Q₁
and D₄ is collector
base junction of Q₁
ON state of diode

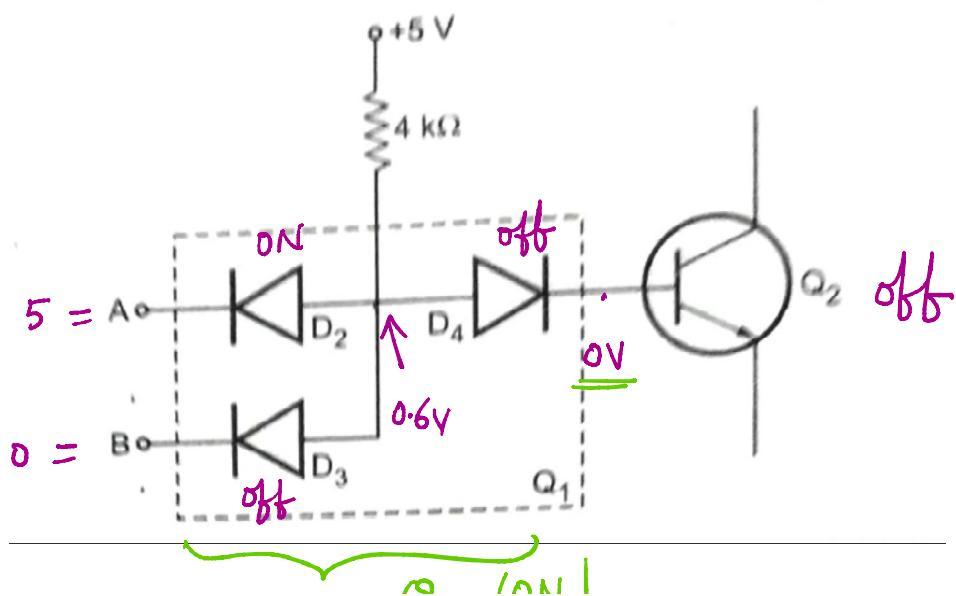
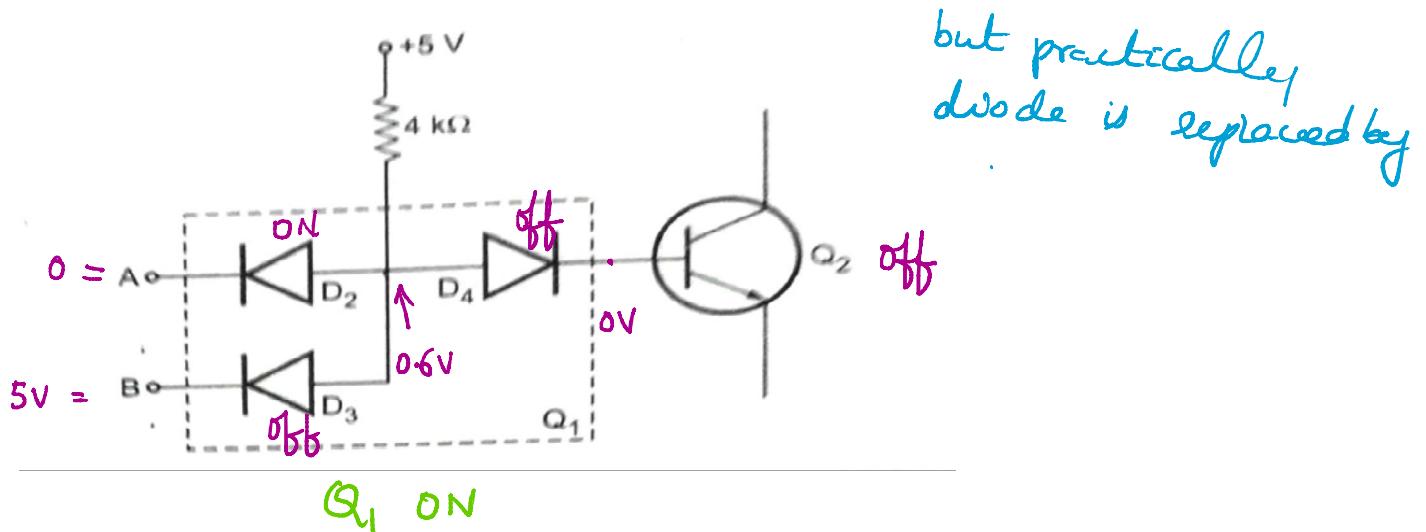
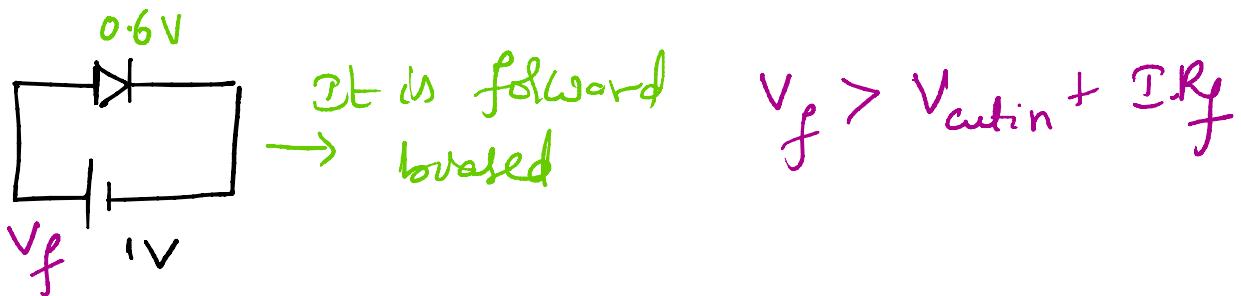


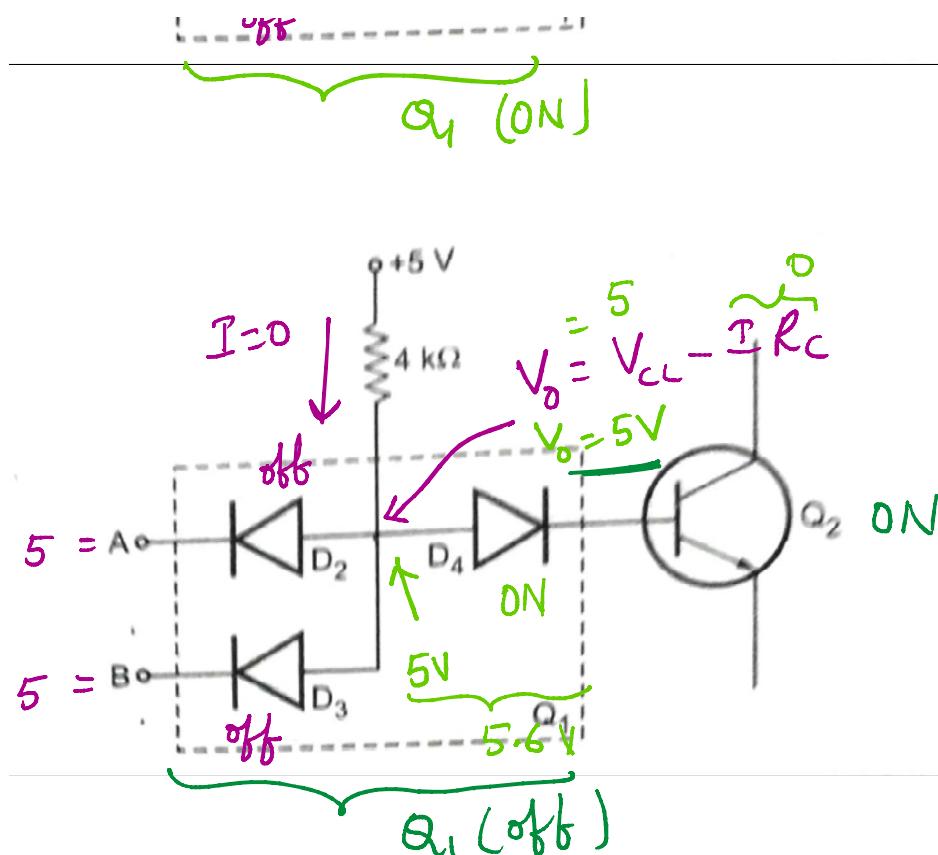
To Switch ON , we need to supply voltage must be greater than cut-in voltage and depends on internal resistance of the diode

$$\begin{aligned} V_f &\geq \text{Cut-in voltage} + I R_f \\ &\geq 0.6\text{V} + 0.2\text{V} \end{aligned}$$

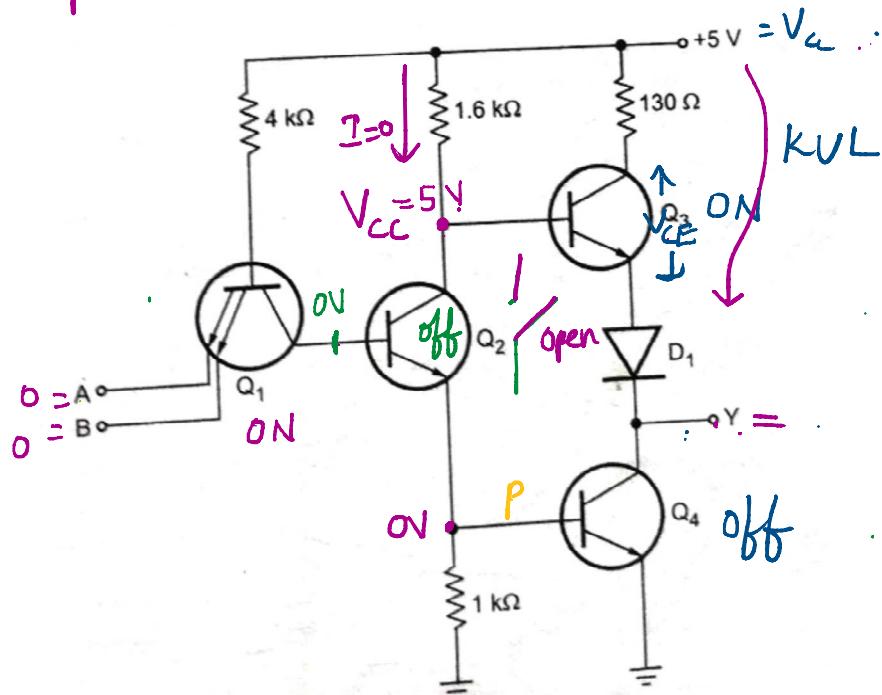


$$V_f < \text{cut-in voltage} + I R_f$$





Multiple emitter transistor



$$V_{cc} = I \times 130\Omega + V_{CE} + V_{cutter}$$

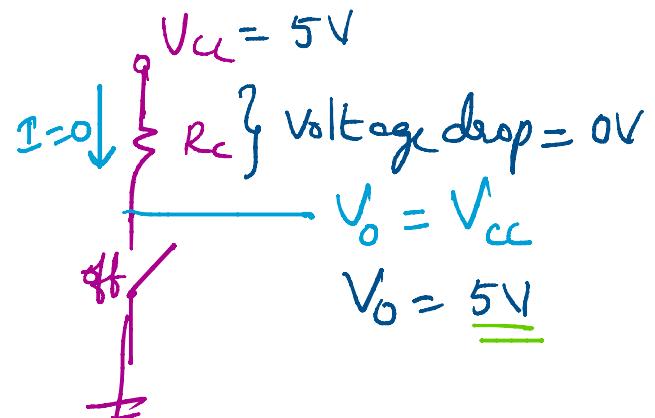
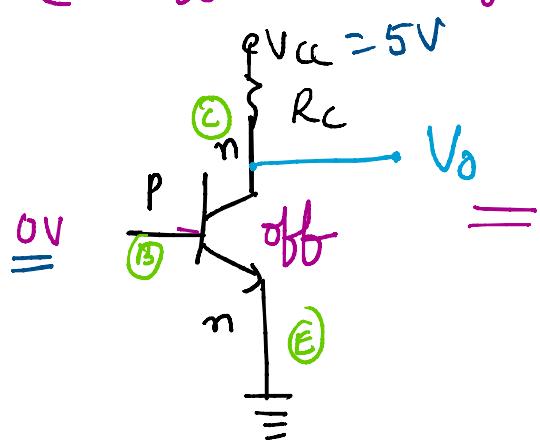
$$V_{CE} = V_{CC} - I \times 130\Omega - V_{CE(sat)}$$

$\underline{Q_2}$ is acting

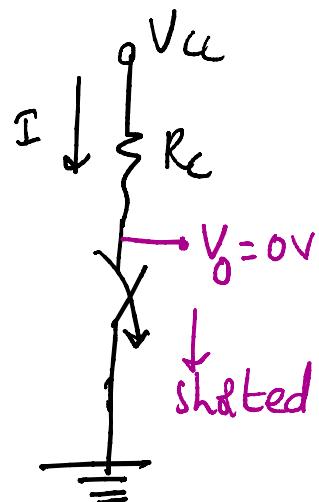
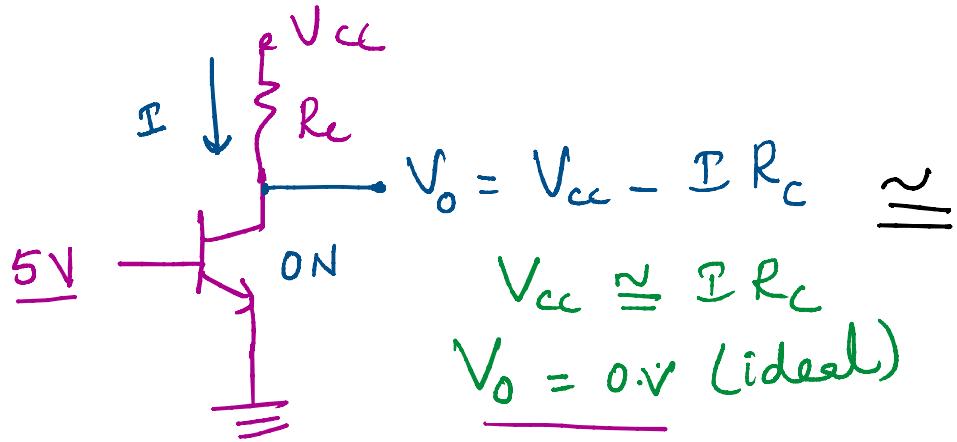
like emitter

follower (common collector)
(o/p voltage follows
the i/p voltage)

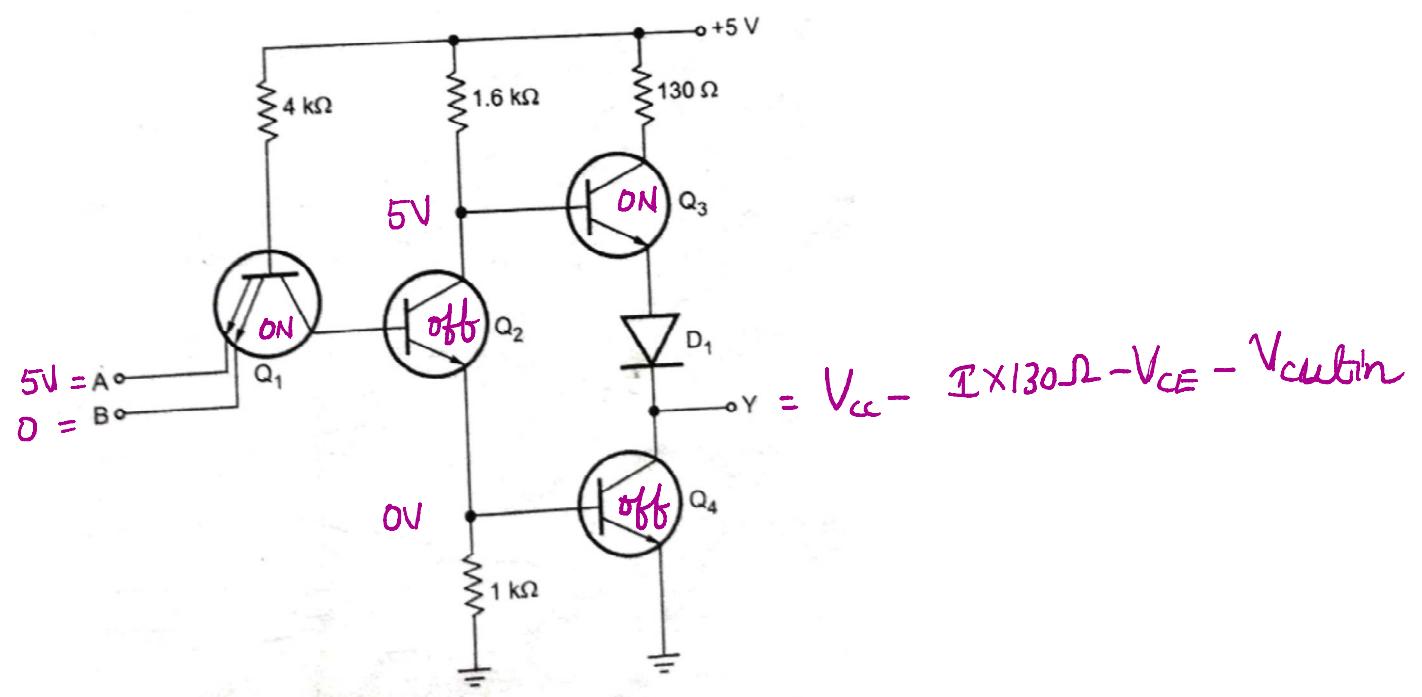
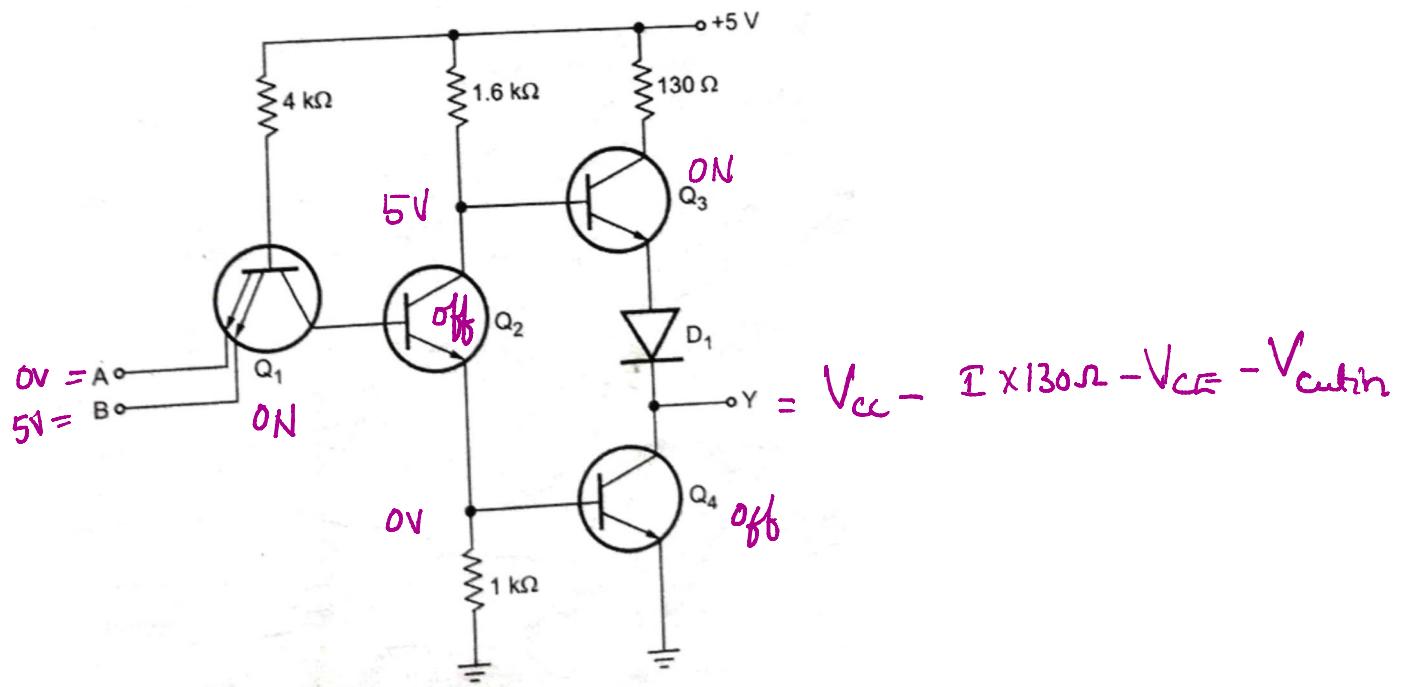
off State (cutoff mode) of Transistor

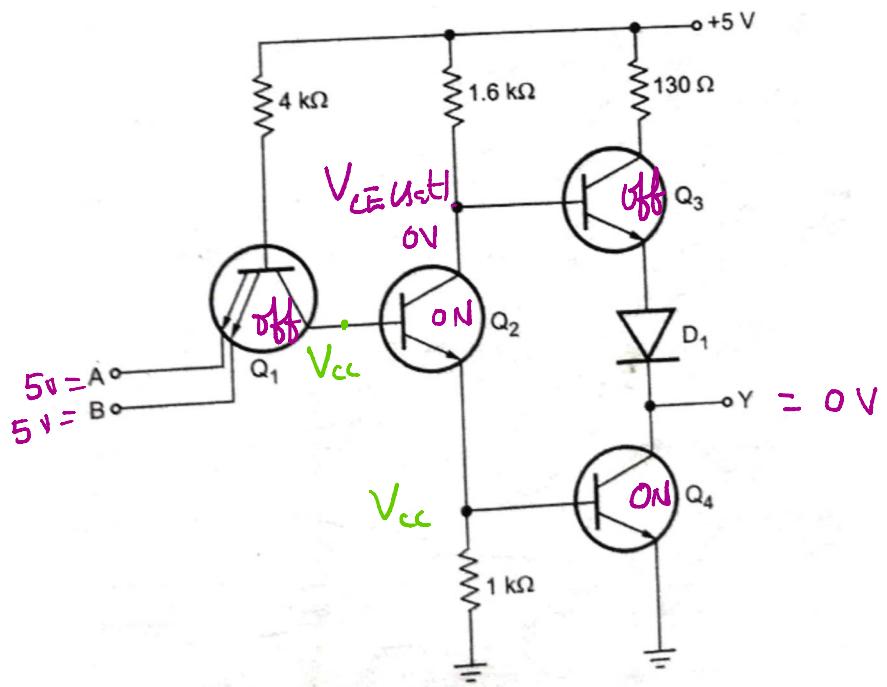


ON State (saturation mode) of Transistor

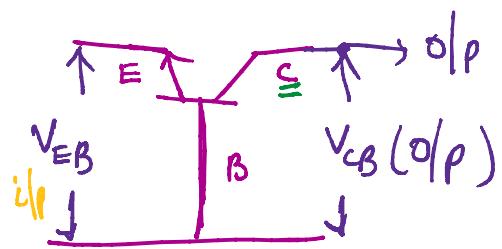


Practically once transistor is in saturation mode
Voltage b/w collector to emitter or $V_{CE} = 0.2V$

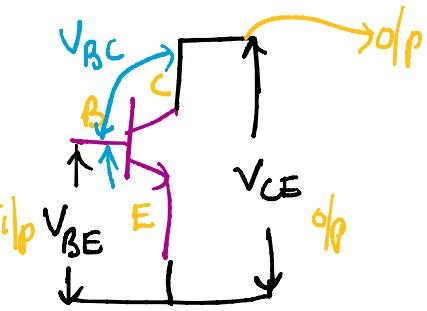




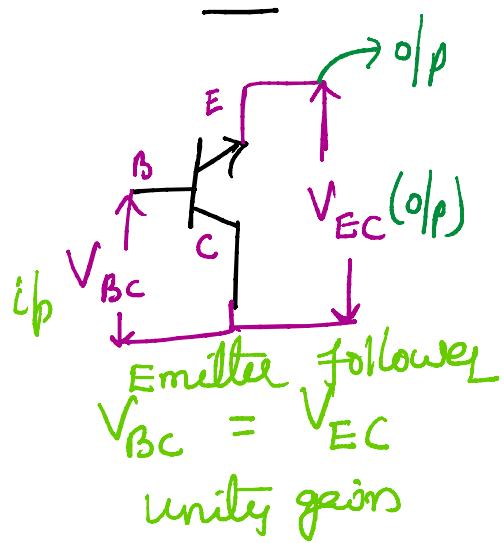
CB



CE



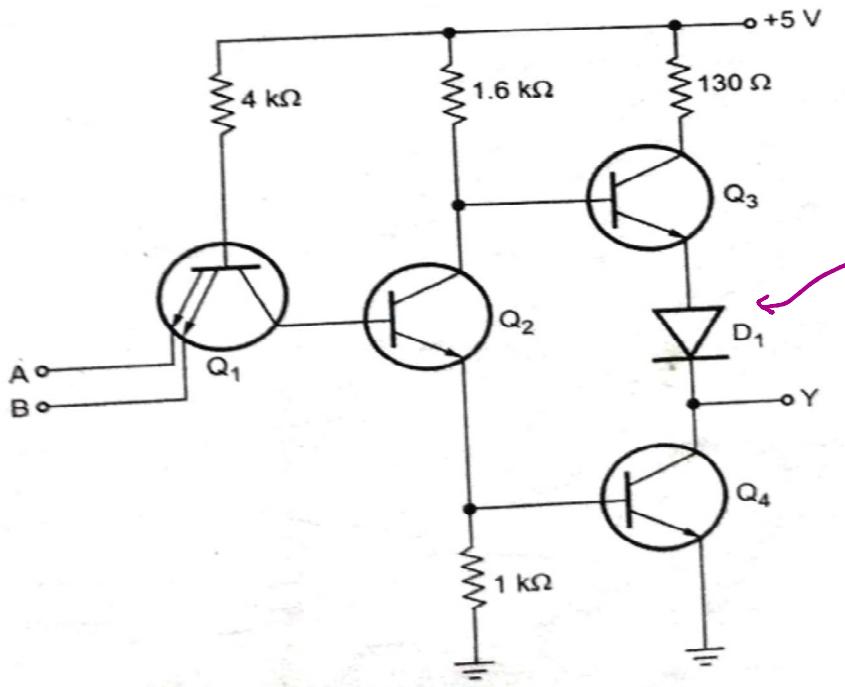
CC



$$V_{CE} = V_{BC} + V_{BE}$$

cathin voltage }
 $0.6V$ for Si
 $0.3V$ for Ge } small

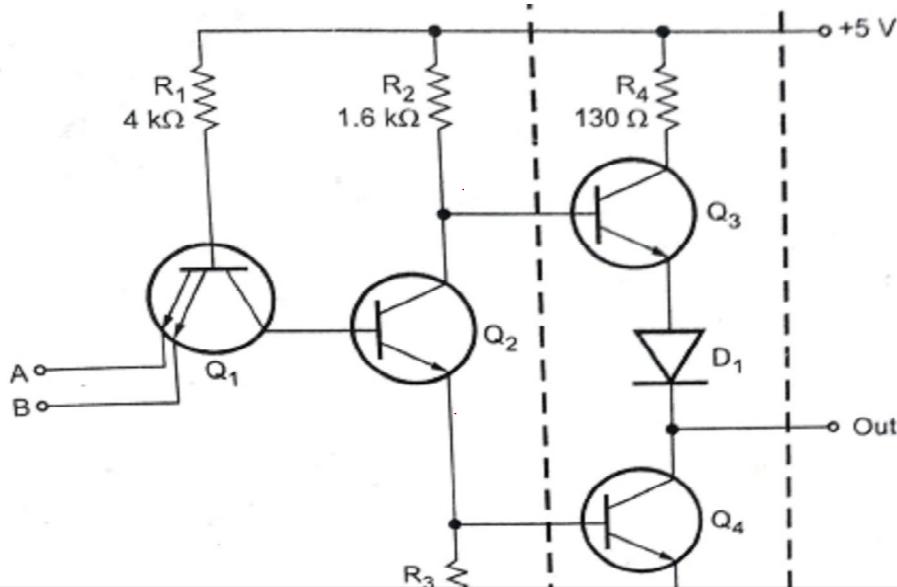
$V_{CE} \approx V_{BC}$



Diode D_1 does not allow base-emitter junction of Q_3 forward biased, so Q_3 off when Q_4 is ON

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Table 7.5 Truth table for 2-input NAND gate



Totem pole transistors produce low O/P impedance.
Either Q_3 act as emitter follower
(High output)
 $\& Q_4$ is saturated

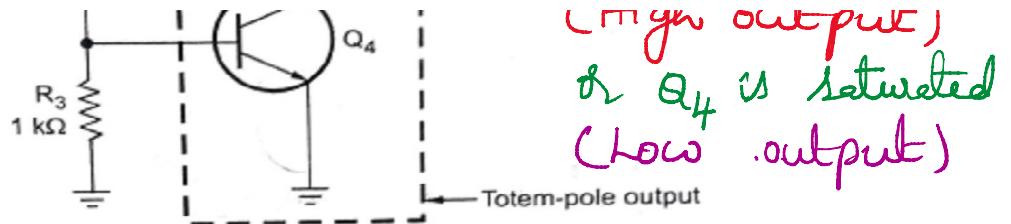
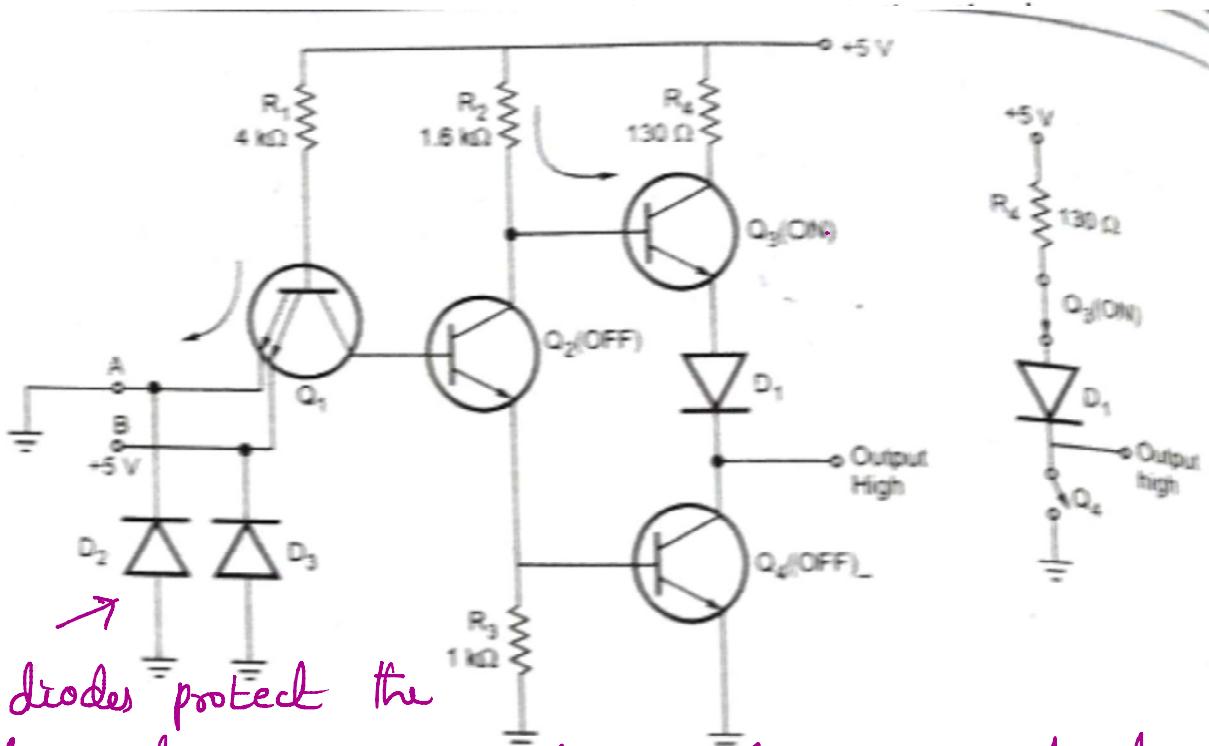


Fig. 7.11 Two input NAND gate with totem-pole output



These diodes protect the
ckt from large negative transients on input lines

Fig. 7.12 (a) Static analysis when output is HIGH

$$V_{OH} = V_{CC} - V_{CE(sat)} - V_D - I_L \times (130\Omega)$$

↑ ↑
 Sat cutin

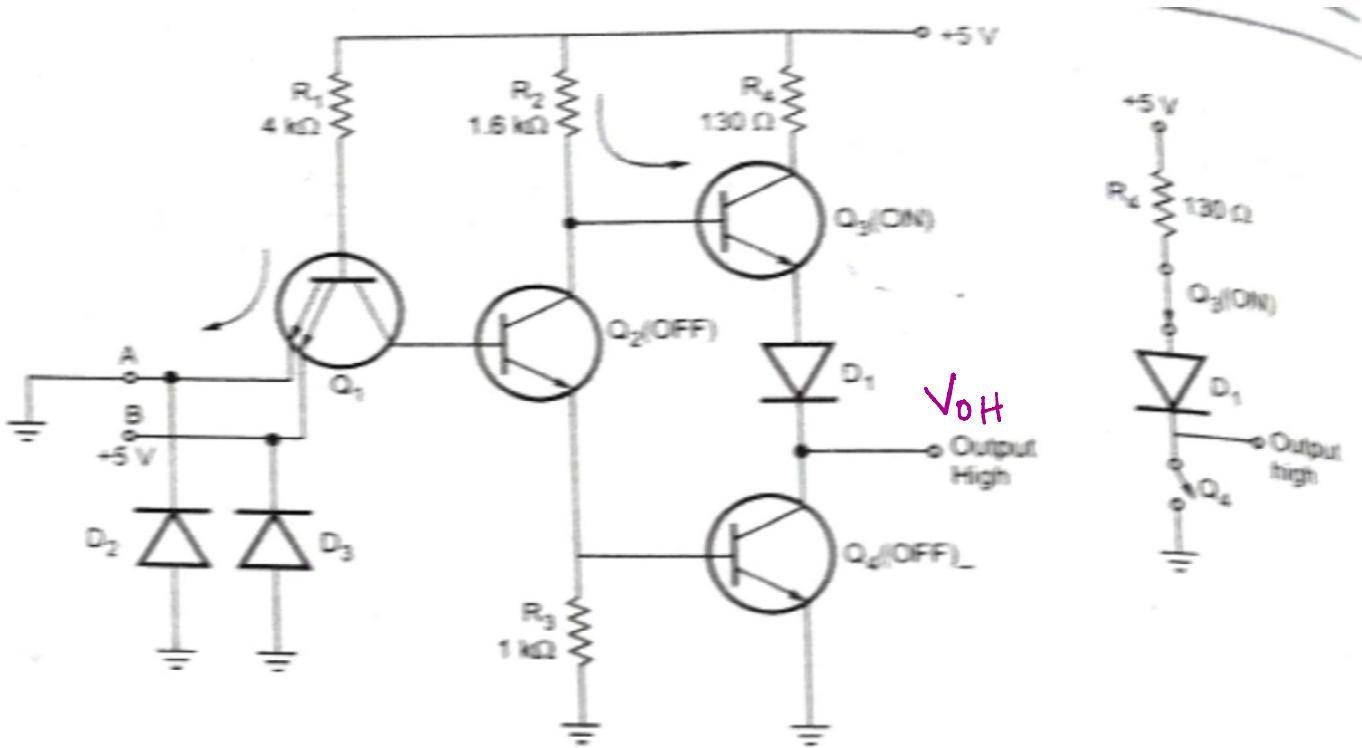
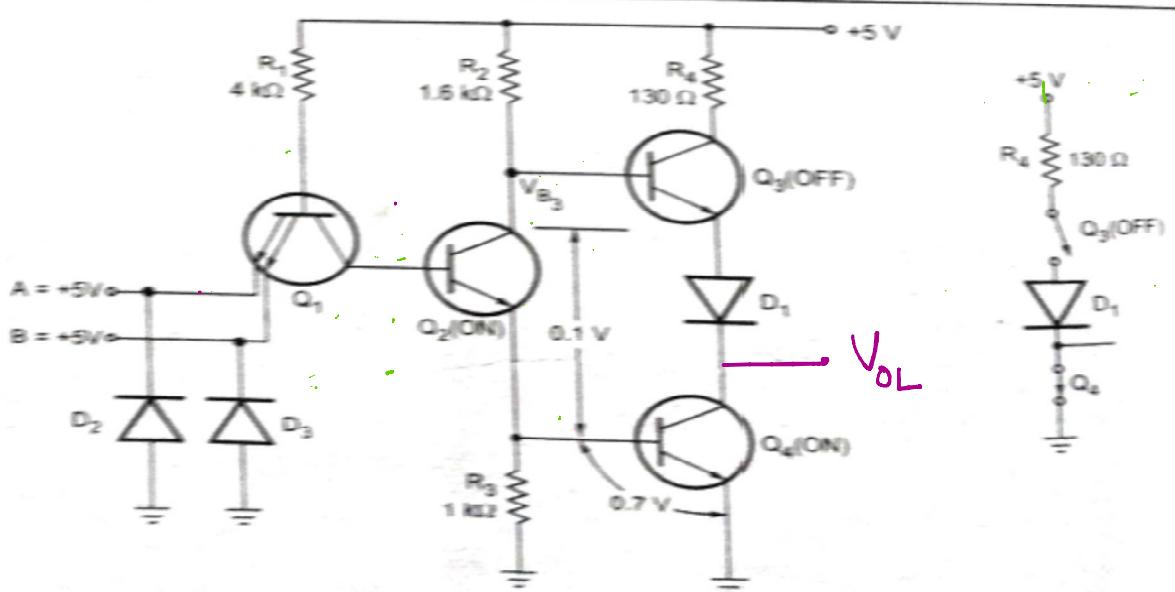


Fig. 7.12 (a) Static analysis when output is HIGH



$$\begin{aligned}
 V_{B_3} &= V_{BE}(Q_4) + V_{CE(sat)}(Q_2) \approx 0.7 \text{ V} + 0.1 \text{ V} \\
 &= 0.8 \text{ V}
 \end{aligned}$$

current sink when Q_3 is low

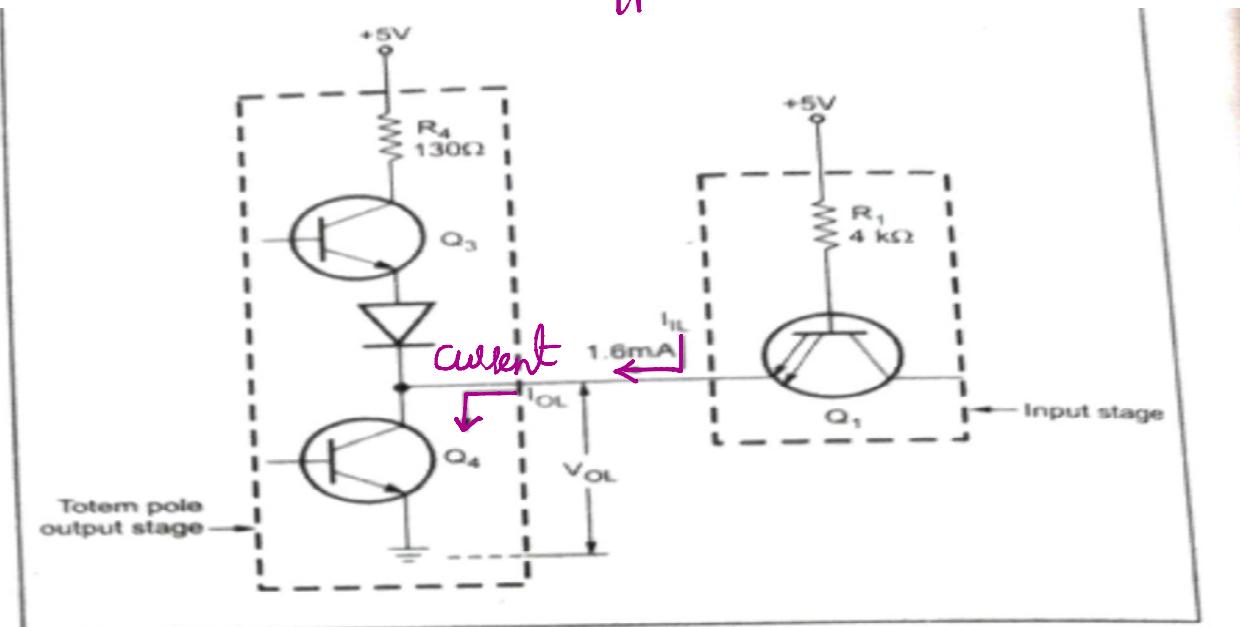


Fig. 7.13 (a) Q_4 acting as a current sink when output is LOW

current source when Q_3 is high

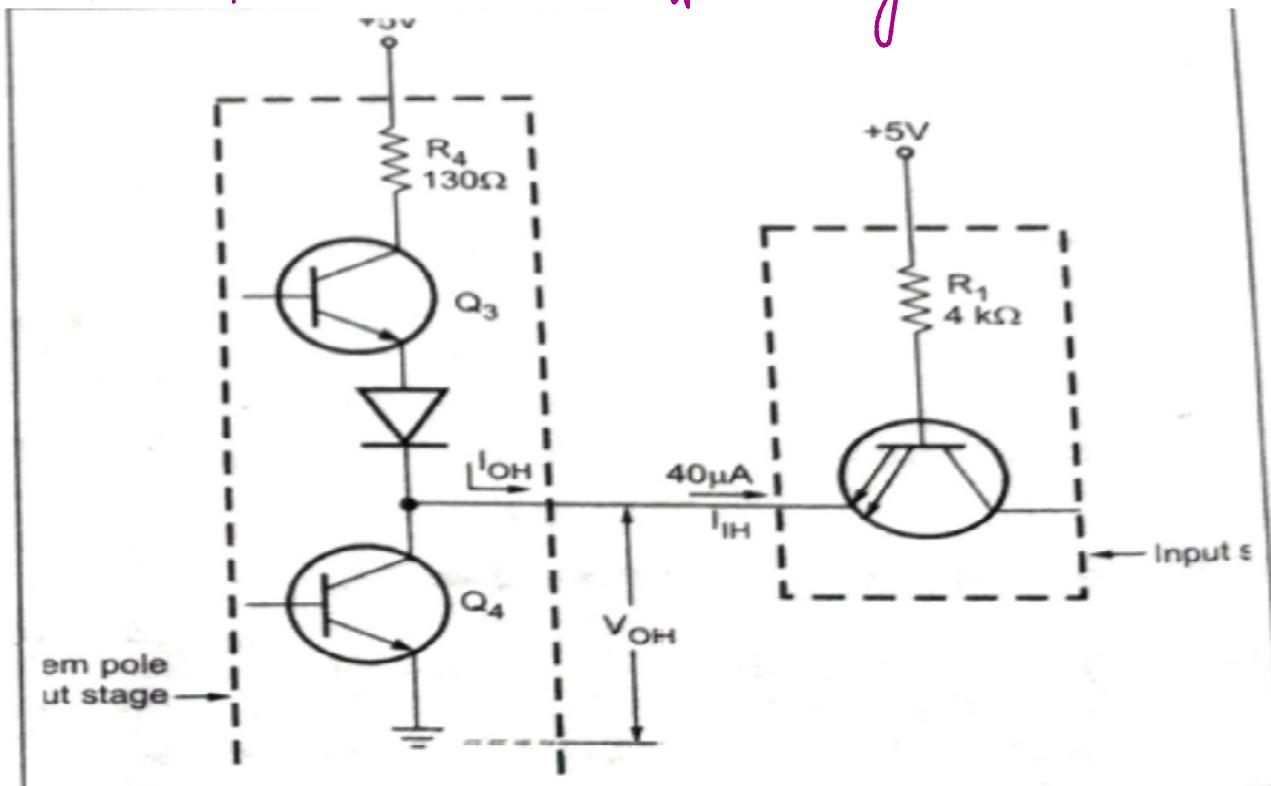


Fig. 7.13 (b) Q_3 acting as a current source when output is HIGH

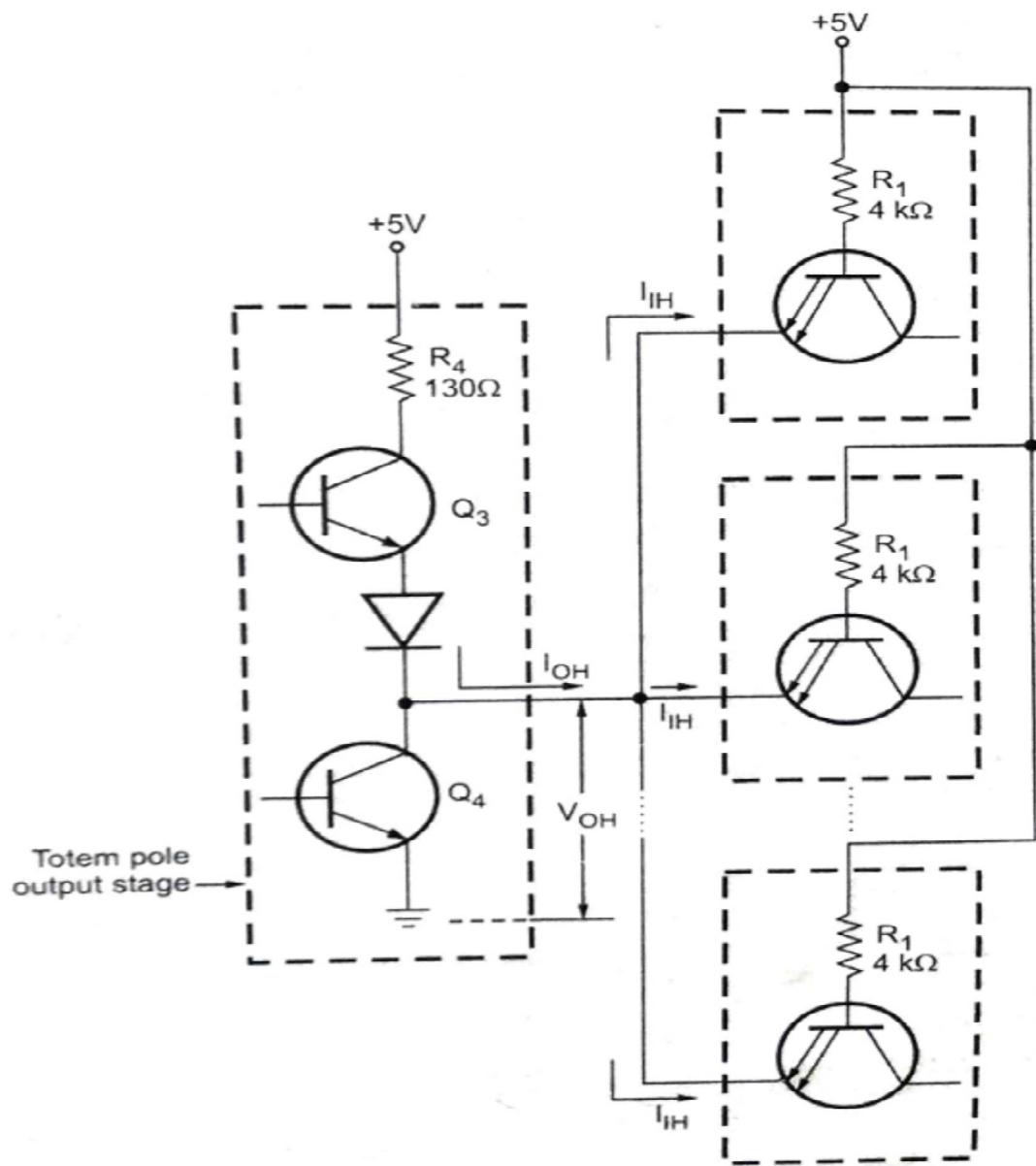


Fig. 7.14 (a) When output is HIGH

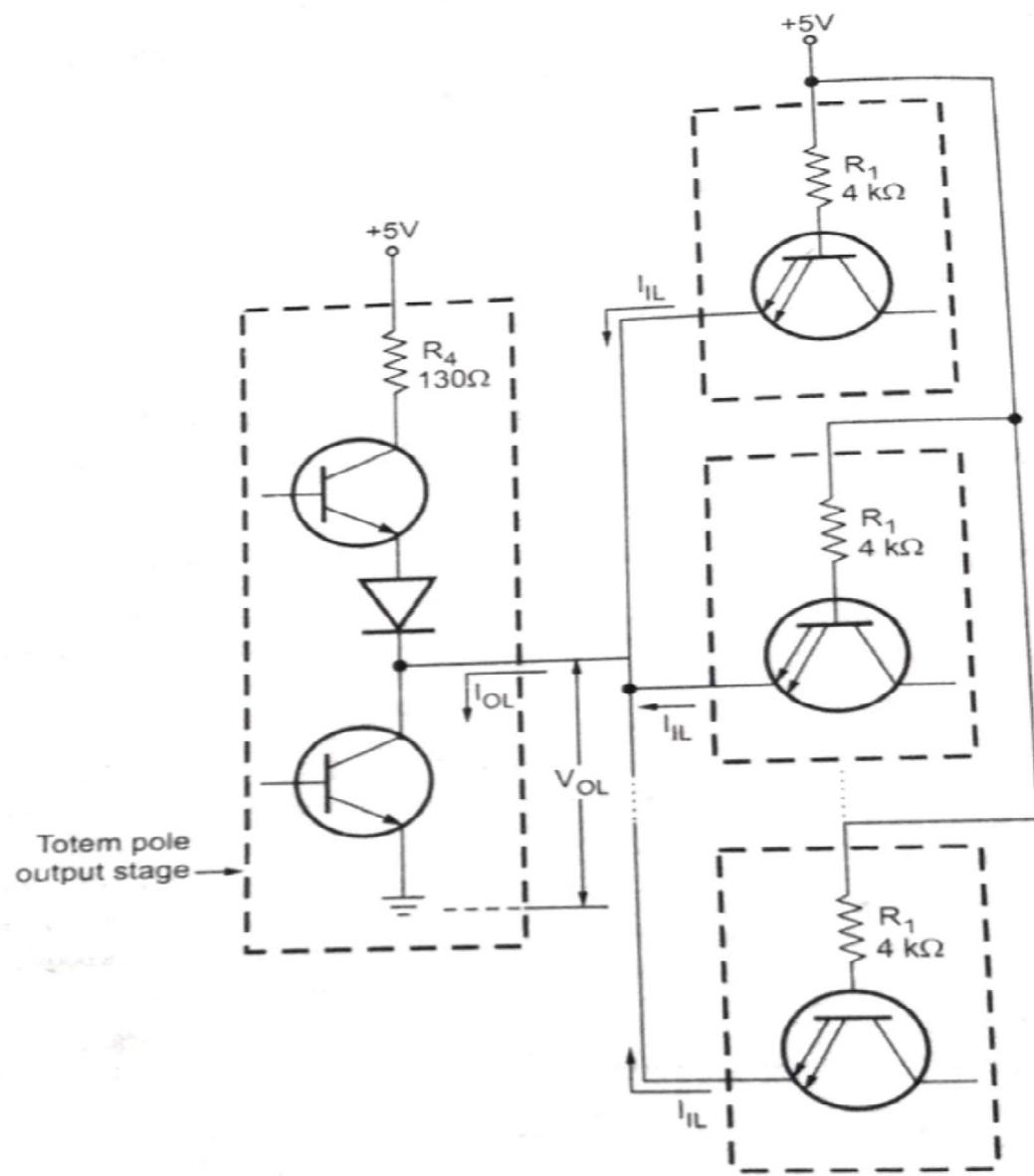


Fig. 7.14 (b) When output is LOW

Voltage Levels and Noise Margin :

Table 7.6 shows the input and output logic voltage levels for the standard 74 series. The minimum and maximum values shown in the Table 7.6 are for worst case conditions of power supply, temperature and loading conditions.

Voltages	Minimum	Typical	Maximum
V_{OL}	-	0.2	0.4
V_{OH}	2.4	3.4	-
V_{IL}	-	-	0.8
V_{IH}	2.0	-	-

Table 7.6 Voltage levels

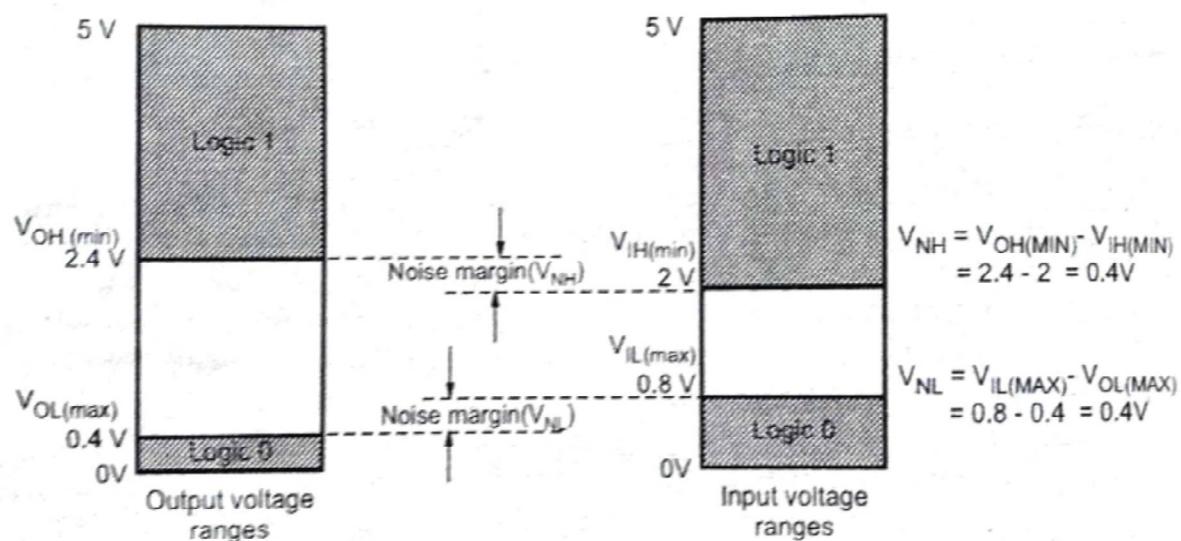


Fig. 7.15 TTL logic levels and noise margin

TTL Specifications

- ① Noise margin = 0.4 V
- ② power dissipation = 10mW per
- ③ Propagation delay = 10nsec
- ④ fan out = 10
- ⑤ voltage levels

$$V_{OH} = 2.4 \text{ V}$$

$$V_{IH} = 0.4 \text{ V}$$

$$V_{OL} = 0.4 \text{ V}$$

$$V_{IL} = 0.8 \text{ V}$$