

6/9/2019

UNITS - FET + UNITS - II

Friday

- There are 2 drawbacks in BJT.
 - (i) Its input impedance is low.
 - (ii) It is noisy.
- To eliminate the above drawbacks, we use FET (Field effect transistor).
- * Definition - FET :-
- It is a transistor in which the current controlled region is affected by electric field.
- It is a unipolar device (current is only due to majority charge carriers).
- There are 3 terminals in FET.
 - (i) Source
 - (ii) Drain
 - (iii) gate.

**
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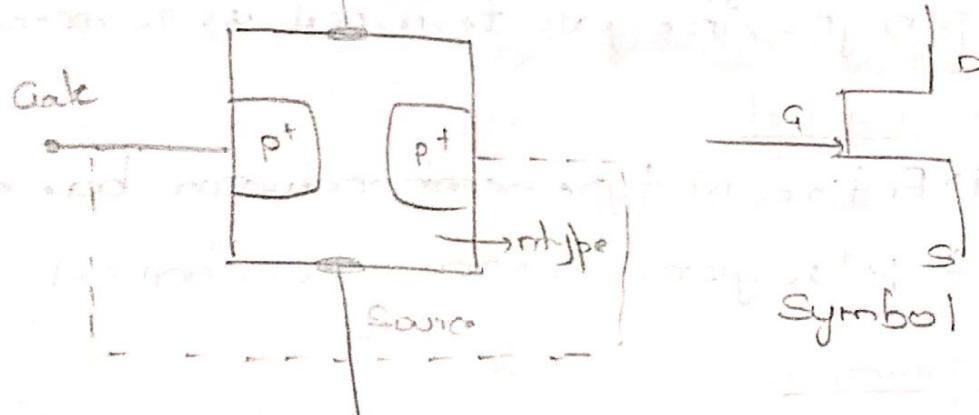
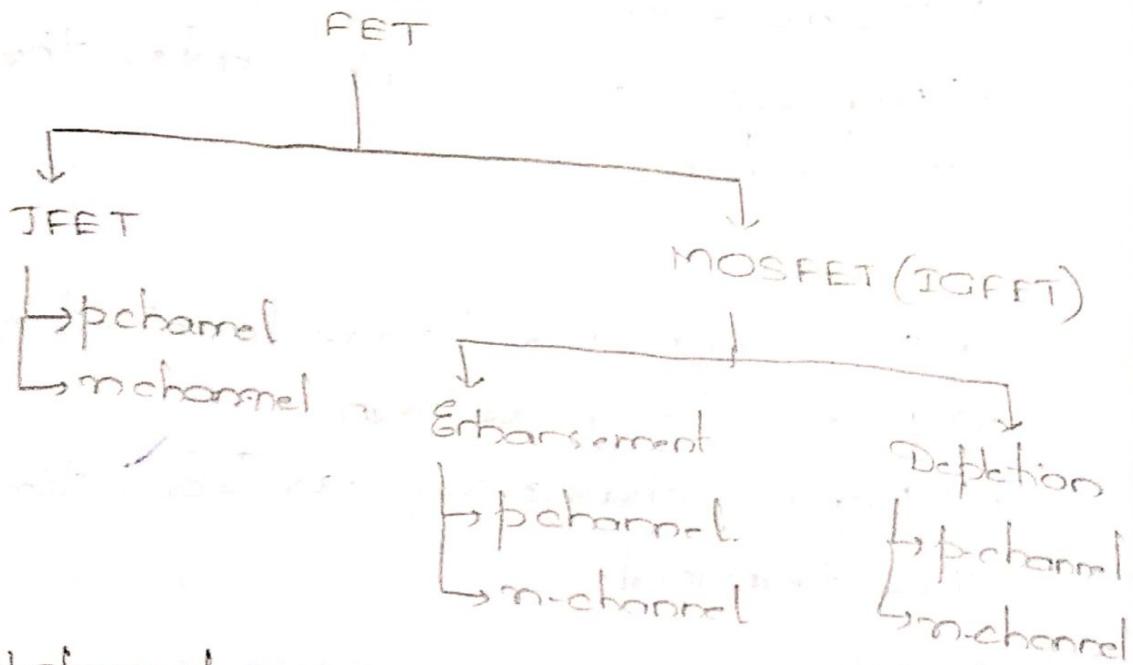
BJT

FET

- | | |
|---|--|
| 1. Bipolar (current is due to minor & major carriers) | 1. Unipolar (current is due to majority charge carriers) |
| 2. Current controlled device | 2. Voltage controlled device |
| 3. Input impedance is low. | 3. Input impedance is high. |
| 4. E, B, C terminals | 4. Source, drain, gate |
| 5. Noisy | 5. less noise. |
| 6. Gain band width product is high. | 6. Gain band width product is low. |
| 7. Thermally less stable | 7. Thermally more stable |

8. Small - large size

8. Small in size.



- Consider n-type semiconductor bar, two heavily doped p+ regions are diffused into n-type (on both sides).
- By diffusing p+ regions, 2 p-n jns are formed.
- Top and bottom 2 ohmic contacts are made which represent source and drain terminals.
 - (i) Source:
 - (i) Generally, source is connected to -ve

terminal of battery.

- (ii) Its resistance is less compared to drain.
- (iii) Majority charge carriers enter through this terminal.

(c) Drain :

- (i) It is connected to the terminal of battery.
- (ii) Its resistance is high.
- (iii) Majority charge carriers leave through this terminal.

(d) Gate :

- (i) Due to the internal connection b/w 2 p-n jns, the gate terminal is formed.

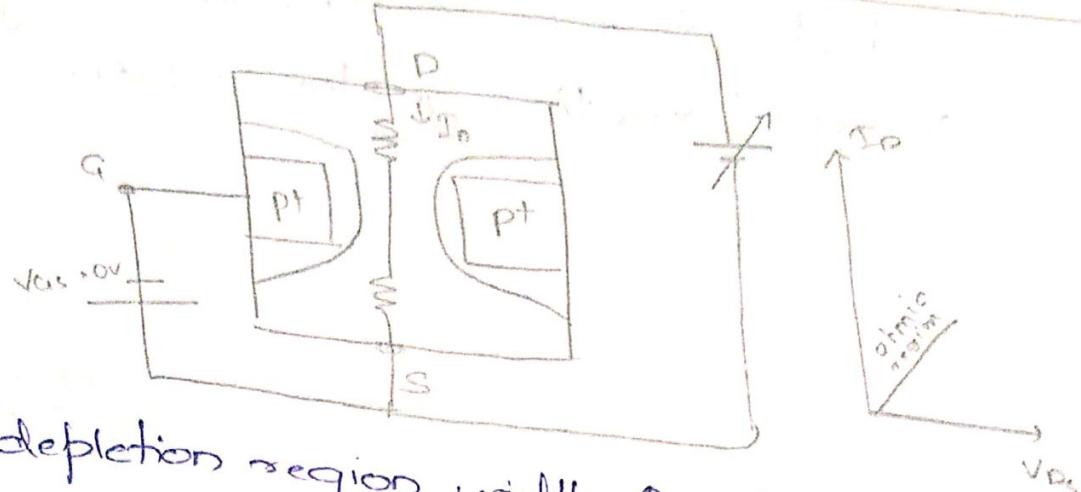
(e) Channel:

- (i) Entire N-type semiconductor bar except 2 p⁺ regions is known as channel.

(f) Operation:

→ Case-1: When $V_{GS} > 0$, $V_{DS} \leq 0$, no current exists, and the widths of depletion regions of 2 p-n jns are equal.

→ Case-2: When $V_{GS} = 0$ & V_{DS} slowly rises (> 0). By rising V_{DS} , more voltage drop occurs near the drain region. Since, the drain region has more resistance. Hence more reverse bias takes place. Thereby



depletion region width δ_s near the drain region. Since source has less resistance than drain. Less voltage drop occurs near the source. Hence, less reverse bias occurs & depletion region width δ_s . Therefore wedge shaped p-n jns are formed.

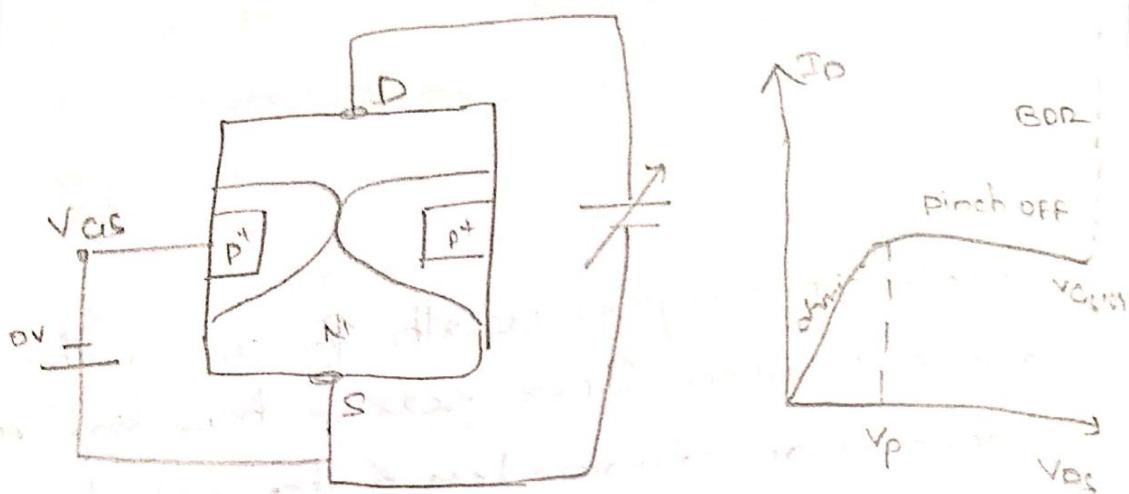
As $V_{DS} \uparrow$, slowly, the charge carriers flow from source to drain & drain current flows from drain to source. In this region of operation, FET acts as a voltage variable resistor.

- Case-3: When $V_{GS} = 0V$, V_{DS} further \uparrow . ($V_{DS} \gg > 0$). At a particular voltage V_p , the 2 p-n jns are contacted with each other. Hence, constant current flows through the device. This region of operation is called pinch off region or saturation region.

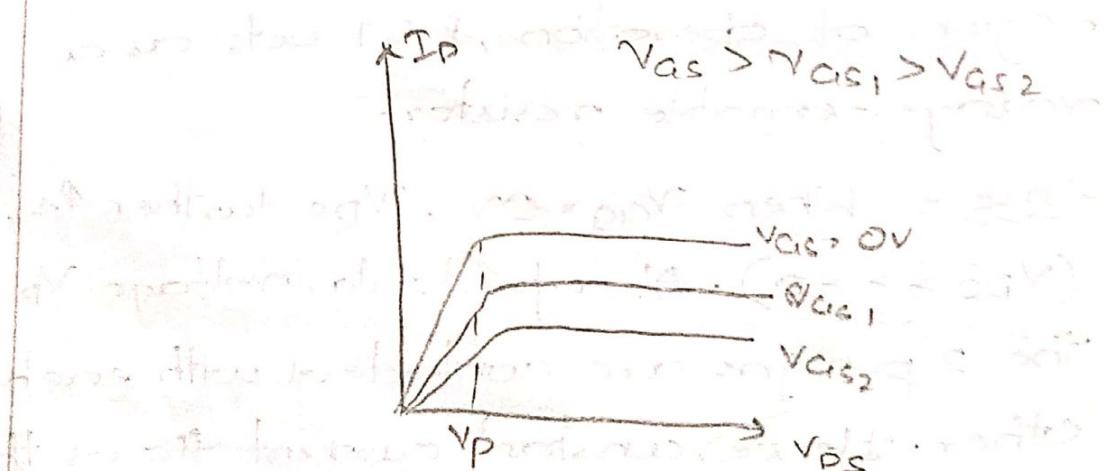
(c) Pinch off voltage

- The voltage at which 2 p-n jns are in

contact with "other" or constant voltage current flows through the region.

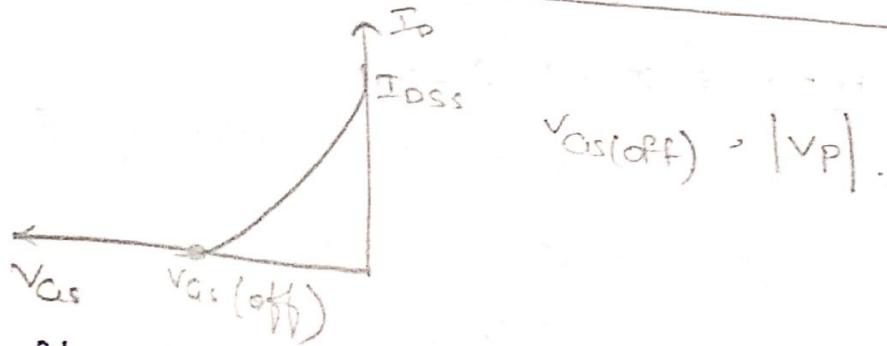


- Case-4: When $V_{GS} = 0V$, I_D is $\uparrow\uparrow\uparrow\uparrow$ then breakdown voltage region occurs.
- Case-5: When $V_{GS} = -ve$ & the above cases are repeated then graph shifts to the bottom.



(e) Transfer characteristics:

- It is graph plotted b/w off current I_D and i/p voltage V_{GS} keeping o/p voltage V_{DS} constant.



- When V_{DS} is constant and V_{GS} is in -ve values, the drain current decreases as above i.e., like a parabola.
- From the graph,

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(\text{off})}} \right]^2$$

i.e., William Shockley current equation.

9/9/2019

Monday

* Parameters of JFET:

1. Drain resistance : (r_d)

- It is defined as the ratio of small change in voltage to current.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} / V_{GS} \rightarrow \text{constant.}$$

2. Transconductance : (g_m)

- It is defined as the ratio of small change in drain current to the input voltage.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} / V_{DS} \rightarrow \text{constant.}$$

3. Amplification factor!
 → It is defined as the ratio of o/p current to i/p voltage.

$$m = \frac{\Delta V_{DS}}{\Delta V_{AS}} / I_D = \text{constant.}$$

- (4) Relation b/w τ_d , g_m , m :

$$m = \frac{\Delta V_{DS}}{\Delta V_{AS}} \times \frac{\Delta I_D}{\Delta I_B}$$

$$m = \tau_d g_m.$$

- Acc. to William - Shockley equation,

$$I_D = I_{DSS} \left[1 - \frac{V_{AS}}{V_P} \right]^2 \quad \rightarrow (1)$$

As we k.t., $g_m = \frac{\partial I_D}{\partial V_{AS}}$

$$\Rightarrow \frac{\partial I_D}{\partial V_{AS}} = I_{DSS} \left[-\frac{1}{V_P} \right]^2 \left(1 - \frac{V_{AS}}{V_P} \right) \quad \rightarrow (2)$$

$$\Rightarrow g_m = -\frac{2 I_{DSS}}{V_P} \left(1 - \frac{V_{AS}}{V_P} \right) \quad \rightarrow (3)$$

From eq (1) $\Rightarrow 1 - \frac{V_{AS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}} \quad \rightarrow (4)$

If $V_{AS} > 0$

$$g_m = -\frac{2 I_{DSS}}{V_P} = g_{m_0}$$

$$g_m = g_{m_0} \left[1 - \frac{V_{AS}}{V_P} \right]$$

$$g_m = g_{m0} \sqrt{\frac{I_D}{I_{DSS}}}$$

$$g_m = \frac{2I_{DSS}}{V_P} \sqrt{\frac{I_D}{I_{DSS}}}$$

- Q. An n-channel JFET has following parameters
 $V_{asoff} = -6V$, $V_{as} = -2V$, $I_{DSS} = 8mA$. Determine, I_D , V_P

Sol: $|V_{asoff}| = V_P = +6V$

$$\left(1 - \frac{V_{as}}{V_P}\right)^2 = \sqrt{\frac{I_D}{I_{DSS}}}$$

$$\left(1 - \frac{-2}{6}\right)^2 = \frac{I_D}{8 \times 10^{-3}}$$

$$\Rightarrow I_D = 8 \left[1 + \frac{1}{3}\right]^2 \times 10^3 = 8 \left[\frac{4}{3}\right]^2 \times 10^3 = \frac{8 \times 16}{9}$$

$$\Rightarrow I_D = 3.5mA$$

- Q. JFET has $V_{asoff} = -1V$, $I_D = 2mA$, determine I_{DSS} at $V_{as} = 0$.

Sol: $V_{as} = 0 \Rightarrow I_D = I_{DSS} = 2mA$

- Q. For what value of V_{as} , drain current is $\frac{1}{4}$ of its max value.

Sol: $\left(1 - \frac{V_{as}}{V_P}\right)^2 = \frac{I_{DSS}}{4I_{DSS}}$

$$1 - \frac{V_{as}}{V_P} = \frac{1}{2}$$

$$1 - \frac{1}{2} \cdot \frac{V_{as}}{V_P} \Rightarrow \frac{1}{2} \Rightarrow \frac{V_{as}}{V_P} \Rightarrow V_{as} = \frac{V_P}{2}$$

Q. N-channel JFET has $I_D \geq 10\text{mA}$, $I_{DSS} = 1\text{A}$
then $V_p = -1V$, find V_{AS}

$$1 - \frac{V_{AS}}{V_P} = \sqrt{\frac{10 \times 10^{-3}}{1}}$$

$$1 + \frac{V_{AS}}{1} = \sqrt{10^{-2}}$$

$$1 + V_{AS} = 10^{-1}$$

$$- (1 - 0.1) = V_{GS}$$

$$V_{AS} > -0.9V$$

Q. N-channel JFET has $V_p = 5V$, $V_{AS} = 4V$,
 $I_D = 4\text{mA}$, $I_{DSS} = 10\text{mA}$. Find g_m .

$$\begin{aligned} \text{Sol: } g_m &= \frac{-2I_{DSS}}{V_P} \sqrt{\frac{I_D}{I_{DSS}}} \\ &\Rightarrow \frac{-2 \times 10 \times 10^{-3}}{5} \sqrt{\frac{4}{10}} \\ &= \frac{-2 \times 10^{-2}}{5} \sqrt{\frac{2}{5}} \\ &= -0.252 \times 10^{-2} \text{V} \\ &= -0.00252 \text{V} \end{aligned}$$

17/9/2019 Tuesday

* MOSFET:

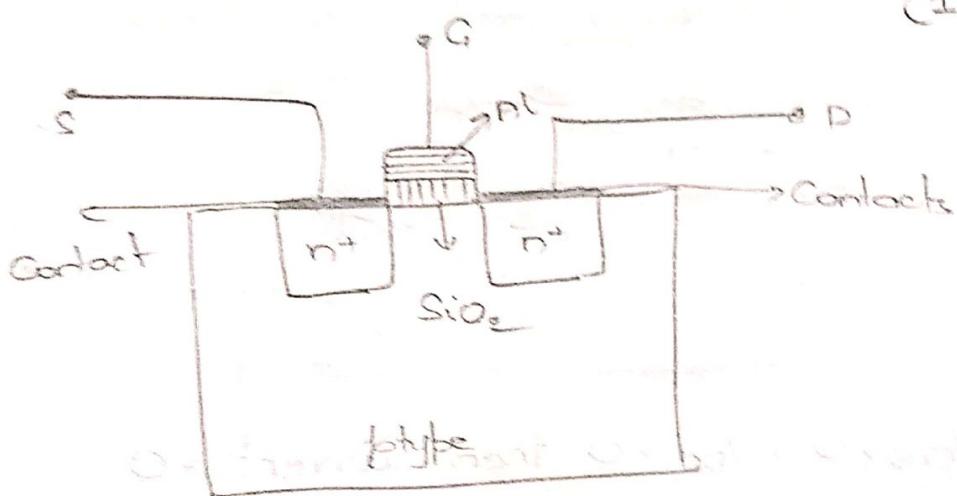
→ Metal oxide semiconductor field effect transistor.

* N-channel enhancement mode MOSFET:

→ Consider p-type semiconductor /substrate/ body. The 2 heavily p^+ regions are

diffused into p-type semiconductor, two ohmic contacts are made for electric connection i.e., drain & source.

- SiO_2 layer is deposited over p-type substrate b/w 2 n^+ regions.
- Metal layer is deposited i.e., Al on SiO_2 layer.
- The conjunction/combination of Al & SiO_2 layer will form gate terminal.
- Here, the gate terminal is insulated by SiO_2 . An insulating layer is b/w gate & semiconductor.
- Hence, it is called an insulated gate FET.
(IGFET)



operation:

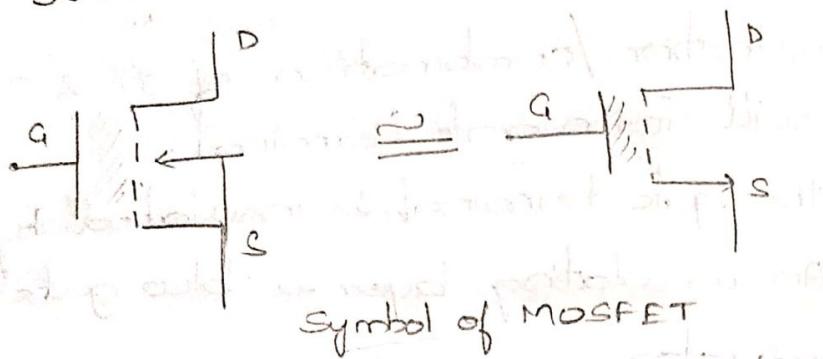
Case-1: When $V_{GS} = V_{DS} = 0$, no current exists b/w drain & source.

Case-2: When $V_{GS} = +V_C$ (To enhance the n-channel b/w source & drain), $V_{DS} = +V_D$ & V_{GS} slightly ↑, current exists b/w source & drain (channel is formed b/w S & D which

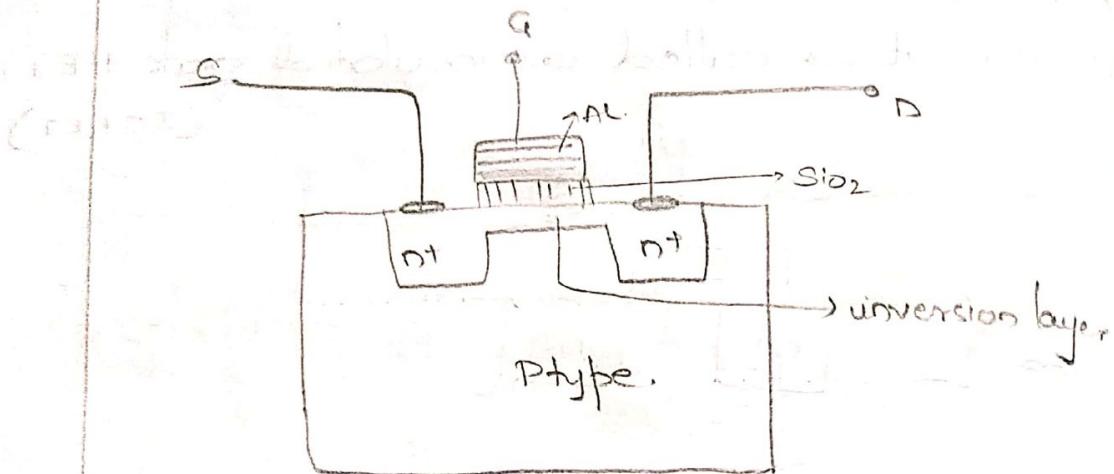
→ represents an inversion layer).
 → the min. required voltage (V_{GS}) to form the channel b/w source & drain is called threshold voltage (V_t).

20/9/2019

Friday

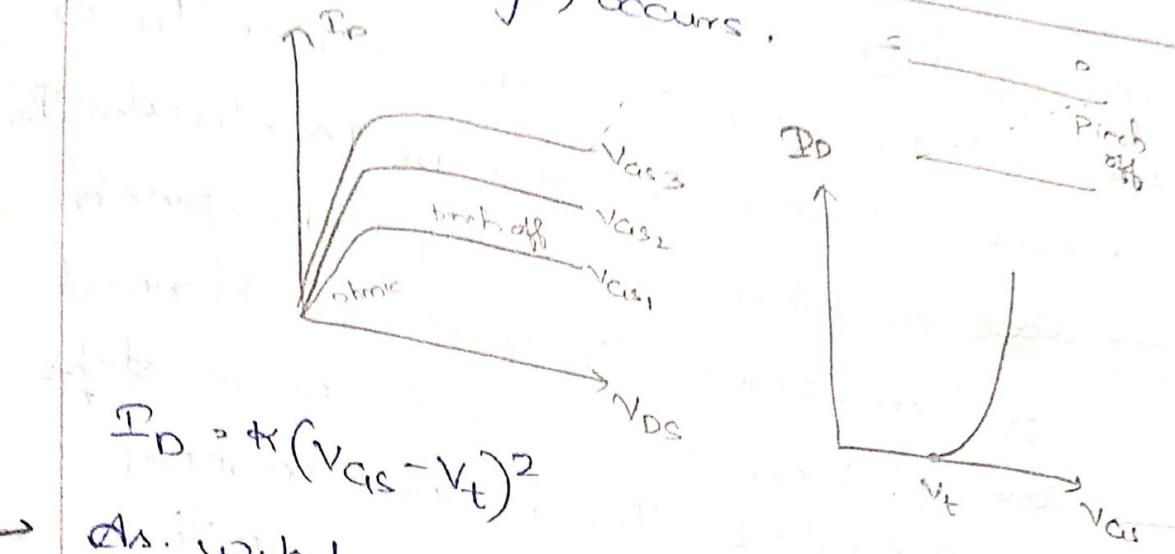


Symbol of MOSFET



1. $V_{GS} = 0, V_{DS} > 0$ then current = 0
2. $V_{GS} = 0, V_{DS} = \uparrow$ then current = 0 since no channel is present.
3. $V_{GS} = +ve. (V_{GS} < V_t)$ then current \uparrow slowly bcz channel formation takes place.
4. $V_{GS} = +ve. (V_{GS} > V_t, V_{GS} - V_t)$ then the channel width \uparrow and depletion layer width \downarrow near the drain region, at a particular voltage

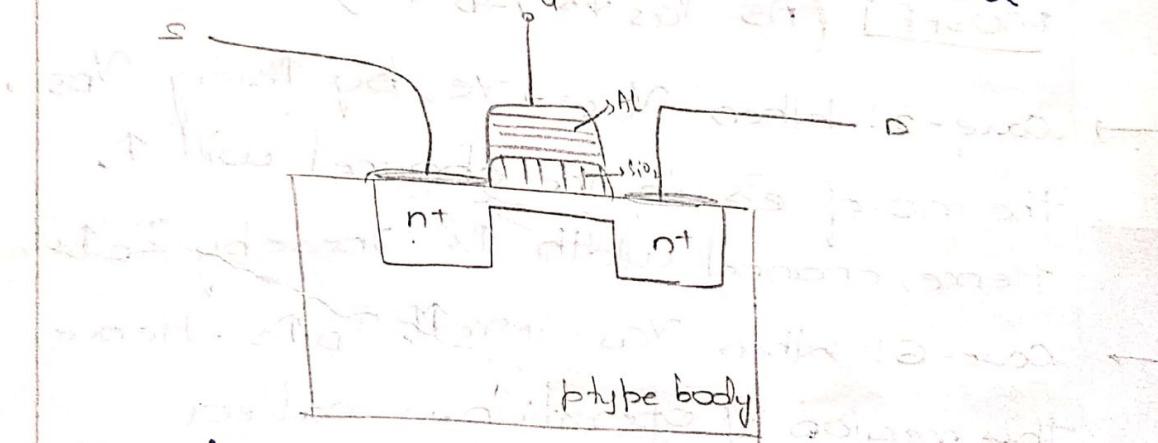
pinch off (voltage) occurs.



$$I_D = k(V_{GS} - V_t)^2$$

- Ans. w.r.t. when $V_{GS} < V_t$ then there is no channel present. Hence $I_D = 0$.
- When $V_{GS} > V_t$ the current $I_D \uparrow$ is as shown in graph.

* N-channel depletion mode MOSFET:



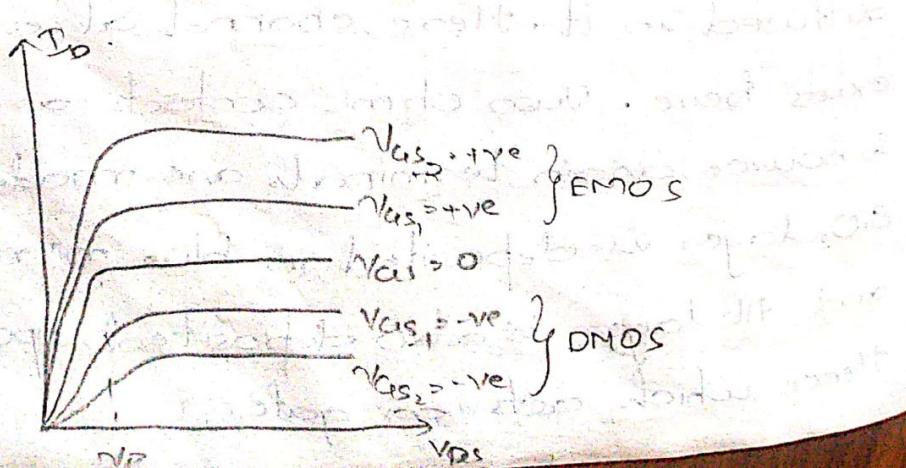
Consider p-type body with n+ regions diffused in it. Here, channel already exists here. Two ohmic contacts are made & source, drain terminals are made.

SiO₂ layer is deposited in blue n+ regions and Al layer is also deposited upon it. Hence which acts as gate.

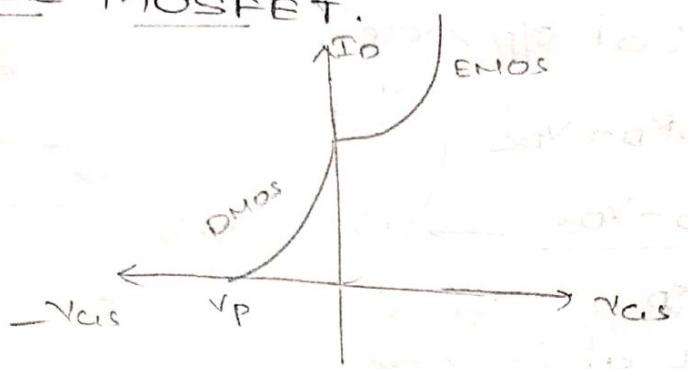
(c) Operation:

- Case - 1: When $V_{GS} = V_{DS} = 0$ then $I_D = 0$.
- Case - 2: When $V_{GS} = 0$, $V_{DS} \uparrow$, I_D also \uparrow .
- Case - 3: When $V_{GS} = 0$, $V_{DS} \uparrow I_S$, pinch off takes place, I_D max. is obtained.
- Case - 4: When $V_{GS} = -ve$ & above steps are repeated, $V_{DS} = \uparrow \uparrow$ then channel width $\downarrow s$. Hence, the no. of e⁻s in the channel will \downarrow , thereby $I_D \downarrow s$.
Hence due to the -ve V_{GS} , depletion of charge carriers takes place in the channel.
This mode is called depletion mode MOSFET (As $V_{GS} \downarrow s$, $I_D \downarrow s$).

- Case - 5: When $V_{GS} = +ve$, by \uparrow ing V_{DS} , the no. of e⁻s in the channel will \uparrow , Hence, channel width $\uparrow s$. Thereby $I_D \uparrow s$.
- Case - 6: When $V_{GS} = +ve \uparrow \uparrow$, $I_D \uparrow s$. Hence this region of operation is called enhancement mode MOSFET.



From the above cases, it can be concluded that DMOSFET can work in both depletion and enhancement modes. Hence, it is also called as depletion enhancement mode MOSFET.



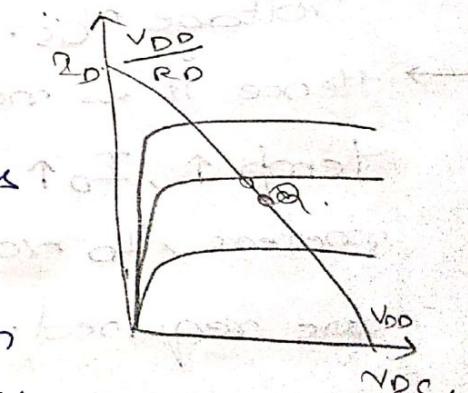
N-channel JFET is operated in depletion mode only, characteristics are similar to depletion mode MOSFET.

23/9/2019

* FET biasing:

- Q-point $\Rightarrow Q_f(V_{DS}, I_D)$
- The biasing is same as BJT biasing.
- As we know, Q-pt is the fn of V_{DS} & I_D , for the better performance of amplifier, Q-pt is located in the middle of load line but following factors affecting the Q-pt
 - (i) Temp.
 - (ii) Transistor parameters.
 To overcome these, we use biasing techniques.
- There are 3 types of biasing,

Monday



(i) Fixed bias

(ii) Self bias (iii) Voltage divider bias.

* Fixed bias method:-

→ Apply ∂V_L at o/p side,

$$V_{DD} = I_D R_D + V_{DS}$$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D} \rightarrow (1)$$

Apply ∂V_L at i/p side,

$$-V_{AG} = I_D R_G + V_{GS}$$

$$\therefore I_D \approx 0$$

$$\rightarrow V_{GS} \approx -V_{AG} \quad (2)$$

From (1) & (2), It can be concluded that o/p current I_D is not dependent on i/p voltage V_{GS} .

→ Hence it is not a good method. i.e., temp \uparrow , $I_D \uparrow$, due to variation in parameters, I_D varies & also 2 power supplies are required.

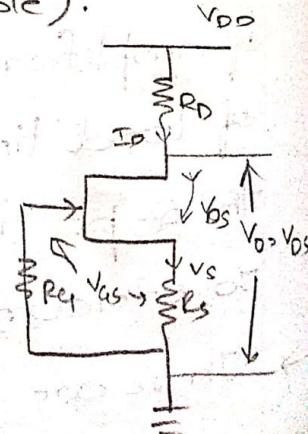
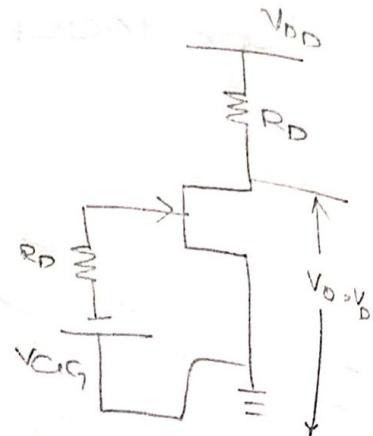
* Self bias method:- (self stable).

→ By applying ∂V_L at o/p side,

$$V_{DD} = I_D R_D + V_{DS} + V_S$$

$$[\because V_S > I_S R_S > I_D R_S \quad [I_S \approx 0]]$$

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$



$$I_D = \frac{V_{DD} - V_{DS}}{R_D + R_S} \quad (1)$$

Apply KVL at i/p side,

$$0 = I_A R_A + V_{AS} + V_S$$

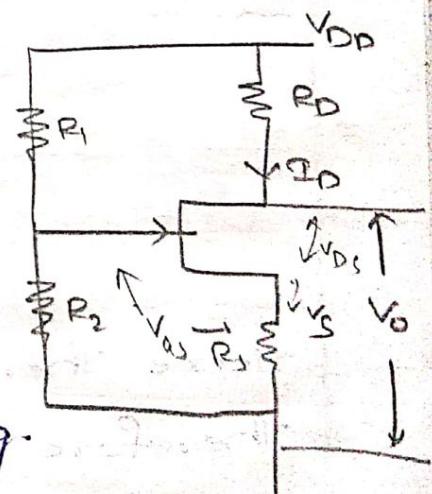
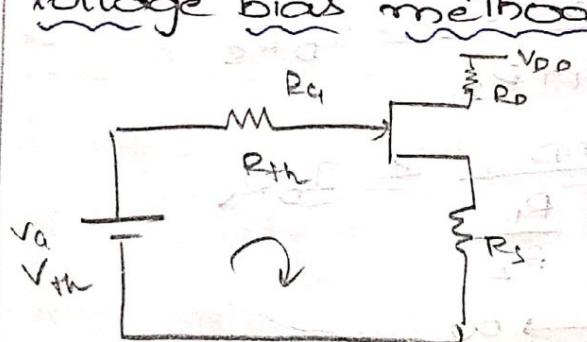
$$0 = I_A R_A + V_{AS} + I_D R_S$$

$$\Rightarrow V_{AS} = -I_D R_S \quad (2)$$

From eq (2), it can be concluded that when temp \uparrow , $I_D \uparrow$ then $V_{AS} \downarrow$. Due to this $I_D \downarrow$. thereby compensation takes place

- Due to the parameter changes if $I_D \downarrow$ then $V_{AS} \uparrow \Rightarrow I_D \uparrow$. Hence compensation takes place. Hence, it is self bias method.

* Voltage bias method:



→ R_1, R_2 provide proper biasing.

→ This can be simplified using Thevenin's th.

$$V_{th} \text{ or } V_A = \frac{V_{DD} \cdot R_2}{R_1 + R_2}$$

$$R_A \text{ or } R_{th} = R_1 \parallel R_2$$

→ Apply KVL at o/p side,

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D + R_S} \quad (1)$$

Apply KVL at input side,

$$V_{TH} \text{ or } V_A = I_A R_{TH} + V_{AS} + V_S$$

$$V_{AS} = V_A - I_D R_S \quad (2)$$

Based on eq(2), it can be concluded that the voltage drop across R_S provides stability against temp. & parameter variation.

- If you want to implement N-channel JFET $V_{AS} = -V_E$, to get $V_{AS} = -V_E$ then consider,

$$V_A < I_D R_S \Rightarrow \frac{V_{DD} \cdot R_2}{R_1 + R_2} < I_D R_S$$

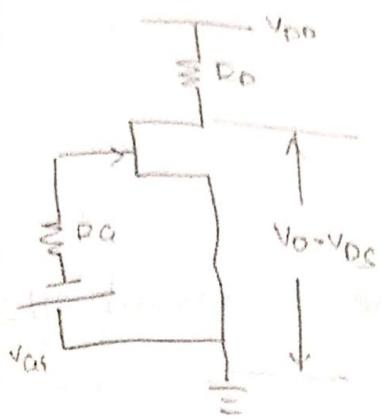
$$\Rightarrow \frac{\frac{V_{DD}}{1 + \frac{R_1}{R_2}}}{R_2} < I_D R_S$$

if $R_1 \rightarrow \infty$

Hence there is no R_1 in self bias circuit. Therefore, it acts as self bias method.

* Compassion table :

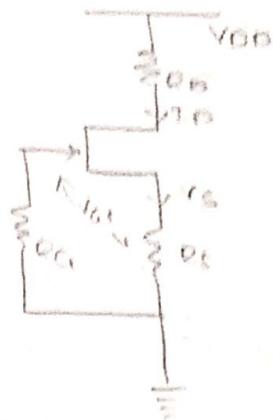
Fixed bias



$$I_D = \frac{V_{DD} - V_{DS}}{R_D}$$

$$V_{AS} = -V_{GS}$$

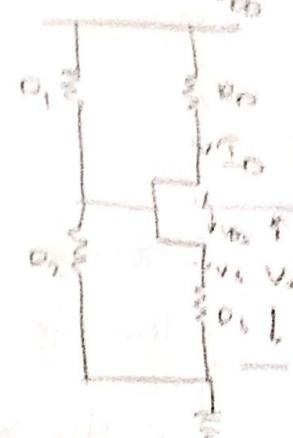
Self bias



$$I_D = \frac{V_{DD} - V_{DS}}{R_D + R_{FB}}$$

$$V_{AS} = -I_D R_S$$

Voltage bias



$$I_D = \frac{V_{DD} - V_{DS}}{R_D + R_{FB}}$$

$$V_{AS} = V_A - I_D R_S$$

* Amplifiers : (FET)

As we know FET's o/p current I_D is the fn of V_{AS}, V_D .

(a) Small signal model of FET:

→ This is applicable for JFET & MOSFET.

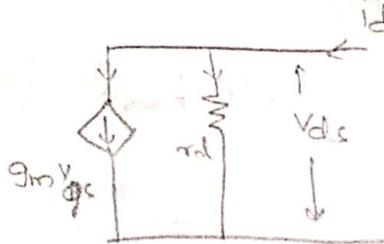
→ $i_d = f(V_{AS}, V_D)$

$$i_d = \frac{\partial i_d}{\partial V_{AS}} \cdot \Delta V_{AS} + \frac{\partial i_d}{\partial V_{DS}} \cdot \Delta V_{DS}$$

$$i_d = g_m V_{AS} + \frac{1}{r_d} V_{DS} \quad \text{--- (1)}$$

Eq(1) represent o/p current equation or current generator in which 2 current sources are added. Hence the \approx circuit

will be



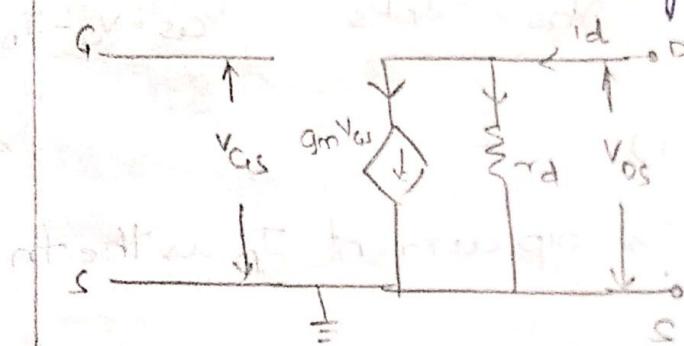
$$id = \frac{V_{ds}}{r_d} + gmV_{gs}$$

Above \approx circuit is o/p side \approx circuit then
the i/p \approx circuit is given as

\because i/p Resistance is high,

current is zero \Rightarrow open circuited

The \approx circuit is given by



(i) AC analysis of an amplifier:

→ To get AC analysis, following steps
to be considered.

(i) Short all the capacitors present in ckt.

(ii) Connect all dc power supplies to ground.

(iii) Replace the transistors with its \approx model.

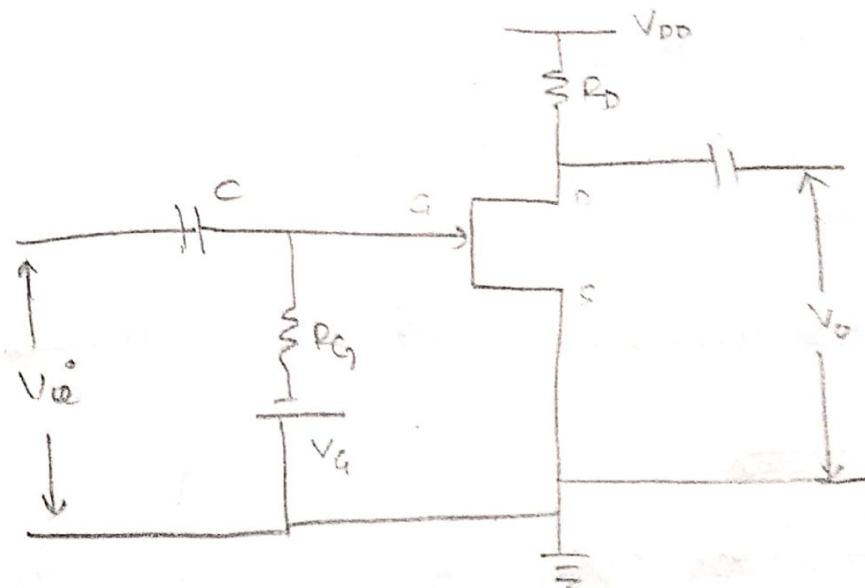
→ There are 3 types of FET amplifiers

(i) Common source (CS)

(ii) Common drain (CD)

(iii) Common gate (CG)

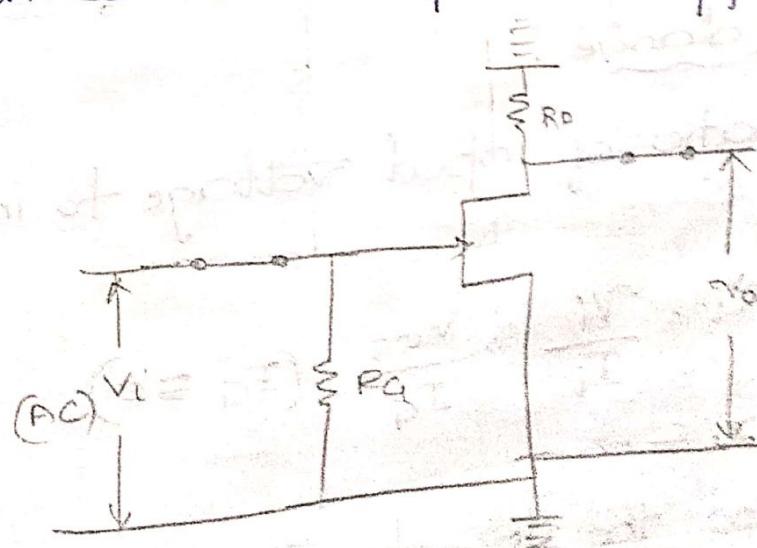
* Common source amplifier:



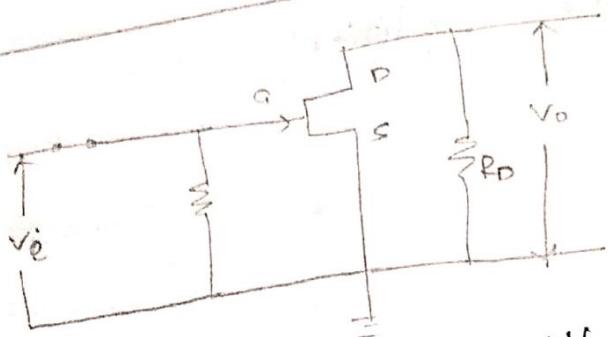
→ Above ckt shows CS amplifier, the i/p terminals are gate & source, the o/p terminals are drain & source where source is common for both i/p & o/p

(i) Analysis:

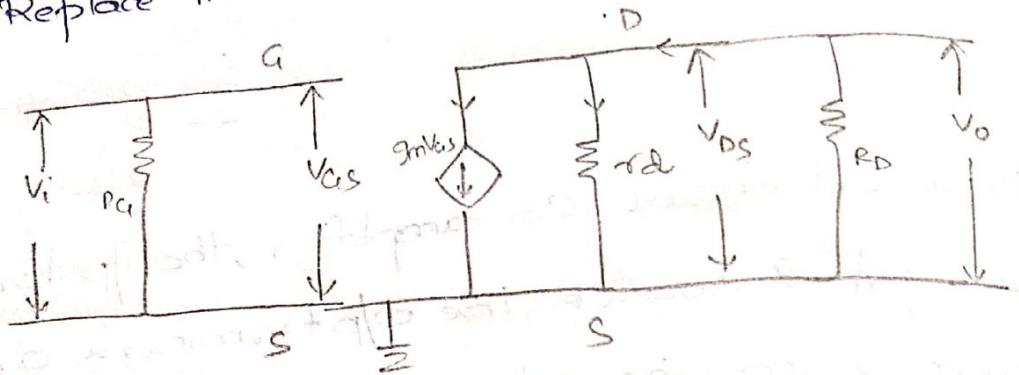
- Short circuit all the capacitors.
- Connect all dc power supplies to ground.



The equivalent circuit for step 2 is given as



Replace the transistor with its \approx model.



24/9/2019

Aft Thursday

	i/p	o/p
CS :-	GS	D,S
CD :-	G,D	S,D
CG :-	S,G	D,G

* Input impedance!

→ It is the ratio of input voltage to input current.

→ As w.r.t., $Z_i = \frac{V_i}{I_i} = \frac{V_{GS}}{I_G}$ ($I_G \approx 0$)

$$Z_i \approx \infty$$

→ By looking at the i/p side, Z_i is given as gate resistance $\Rightarrow Z_i = R_g$ (MΩ).

* Voltage gain:

→ It is defined as the ratio of output voltage to input voltage.

to o/p voltage.

$$\rightarrow A_V = \frac{V_o}{V_i}$$

$$V_o = -g_m V_{AS} (r_d \parallel R_D)$$

$$V_i = V_{AS}$$

$$A_V = -g_m (r_d \parallel R_D)$$

(-ve sign indicates 180° phase shift)

→ If $r_d \gg R_D$ then $A_V = -g_m R_D$.

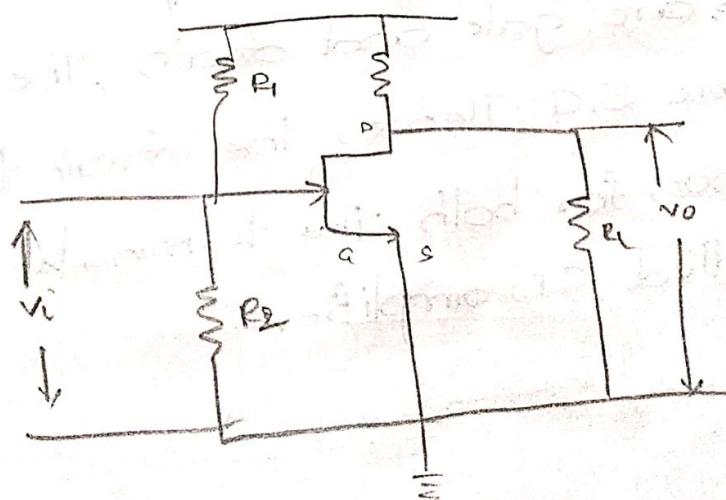
* Output impedance:

→ It is defined as the ratio of o/p voltage to o/p current when i/p voltage is zero & load resistance is high (∞).

$$\rightarrow Z_o = \frac{V_o}{I_o} / I_i = 0, R_L = \infty$$

$$Z_o = r_d \parallel R_D$$

→

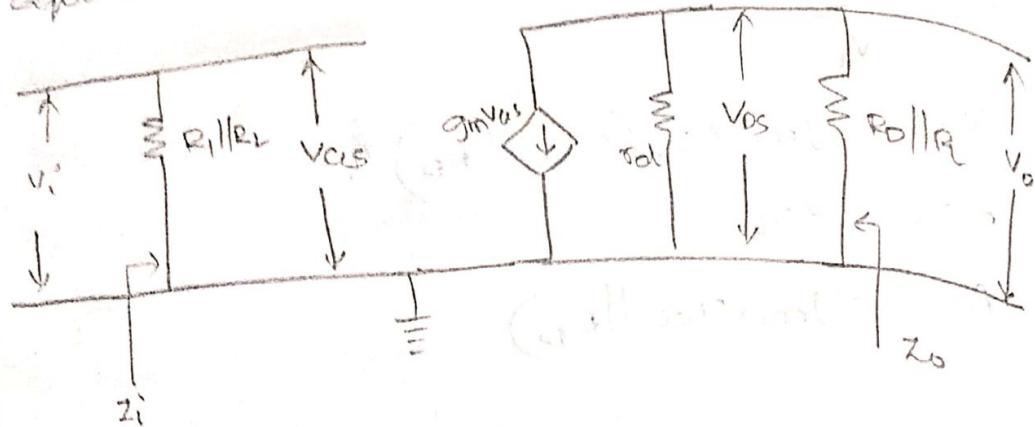


$$Z_i = R_1 \parallel R_2$$

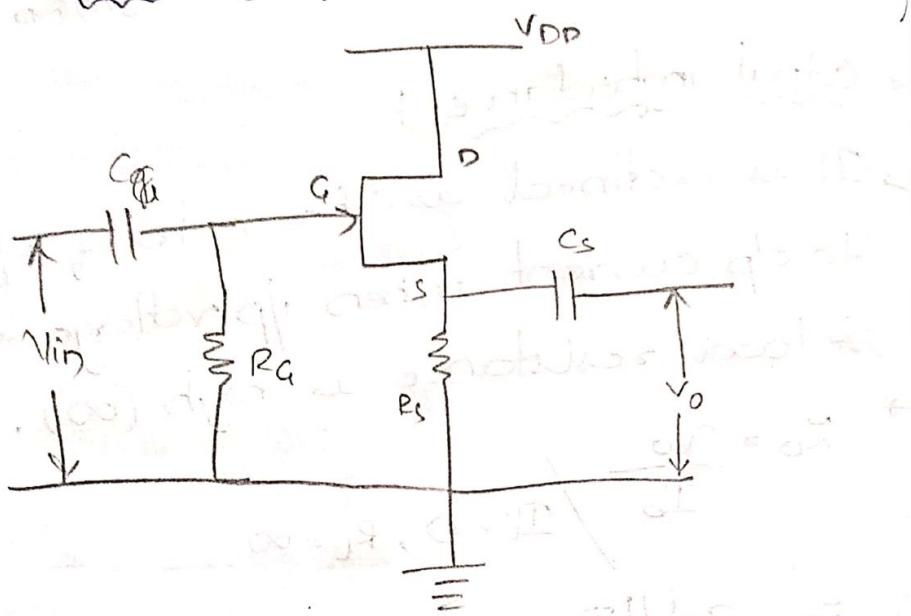
$$Z_o = R_D \parallel R_L$$

$$A_V = -g_m (R_D \parallel R_L)$$

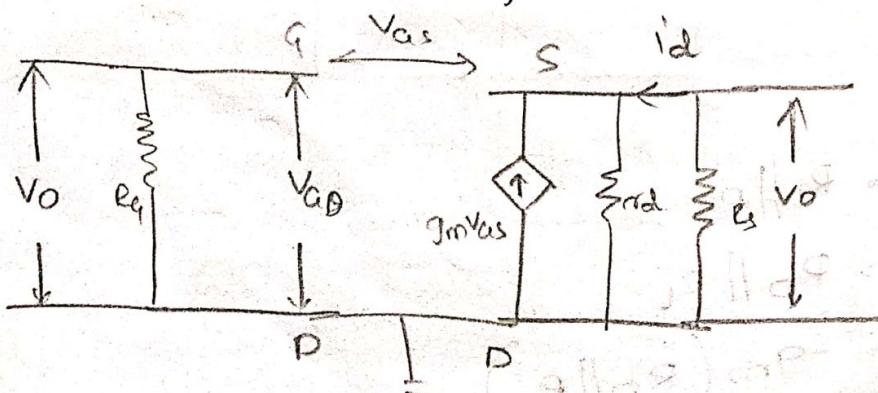
Equivalent circuit



* Common drain amplifier : (source follower)
(CDA)



→ The above ckt shows CD amplifier in which ip terms are gate and drain , the op terms are S,G . Hence , the drain terminal is common for both the terminals . So that it is called CD amplifier.



$\rightarrow Z_i \approx \infty$ since $I_o \approx \infty$

$$Z_i = R_A (M_{22})$$

$$\rightarrow A_v = \frac{V_o}{V_i}$$

$$V_o = g_m V_{AS} (\tau_d || R_S) \rightarrow (1)$$

$$V_{GS} = V_i - V_o \rightarrow (2)$$

$$V_o = g_m (V_i - V_o) (\tau_d || R_S)$$

$$V_o + g_m V_o (\tau_d || R_S) = g_m V_i (\tau_d || R_S)$$

$$V_o [1 + g_m (\tau_d || R_S)] = g_m V_i (\tau_d || R_S)$$

$$\frac{V_o}{V_i} = A_v = \frac{g_m (\tau_d || R_S)}{1 + g_m (\tau_d || R_S)}$$

If $\tau_d \gg R_S$

$$A_v = \frac{g_m R_S}{1 + g_m R_S}$$

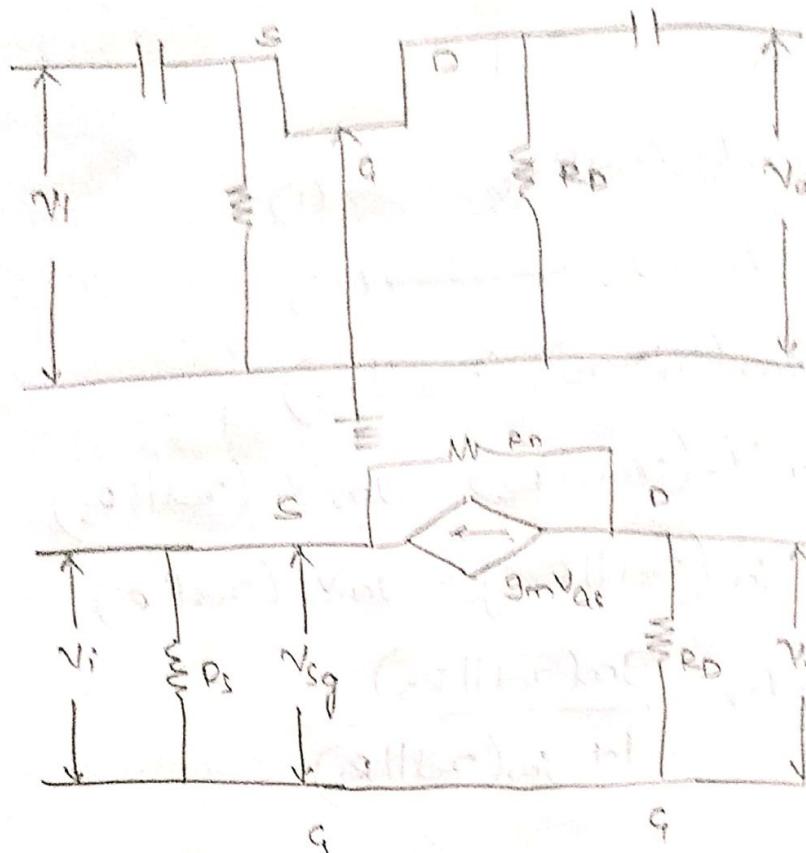
$$g_m R_S \gg 1$$

$$A_v \approx 1.$$

$$A_v = \frac{V_o}{V_i} \Rightarrow V_o \approx V_i$$

\therefore It means o/p voltage follows i/p voltage at source terminal. Hence, CDA is also called as 'source follower'.

* Common gate amplifier
 $(S.G. = \text{IP} \& D.G. = \text{O/P})$



Small signal equivalent model

$$\rightarrow Z_i = \frac{V_i}{I_i} \rightarrow \frac{V_i}{I_s} \rightarrow \frac{V_i}{I_d}$$

$$Z_i = -\frac{V_{gs}}{-g_m V_{ds}} \cdot \frac{1}{g_m}$$

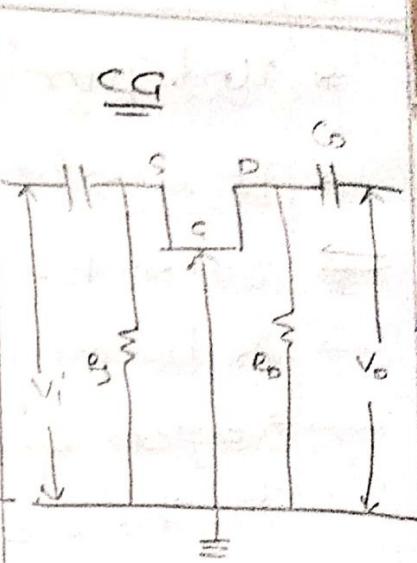
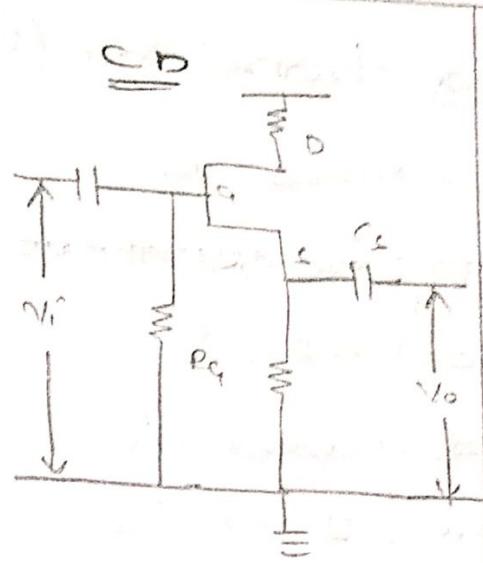
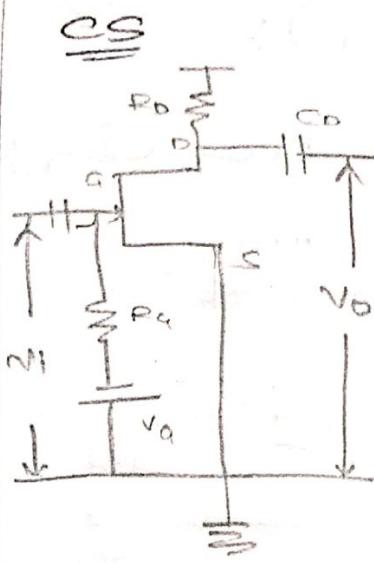
$$Z_i(\text{diagram}) = \frac{1}{g_m} \parallel R_s$$

$$\rightarrow Z_o \cdot \frac{V_o}{I_o} = -\frac{g_m V_{gs} R_D}{-g_m V_{ds}} \Rightarrow \frac{R_D}{g_m V_{ds}}$$

$$Z_o \approx R_D$$

$$\rightarrow A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs} R_D}{-V_{gs}} = g_m R_D$$

$$A_v = g_m R_D$$



1. Input impedance
 $Z_i = R_G \parallel R_s$

2. O/P impedance
 $Z_o = R_D \parallel R_D$

3. Voltage gain
 $A_v = -g_m(R_D \parallel R_s)$

1. IIP impedance
 $Z_i = R_G$

$$Z_o = R_s$$

3. Voltage gain

$$A_v = \frac{g_m(r_d \parallel e_s)}{1 + g_m(r_d \parallel e_s)}$$

1. IIP impedance
 $Z_i = \frac{1}{g_m} \parallel e_s$

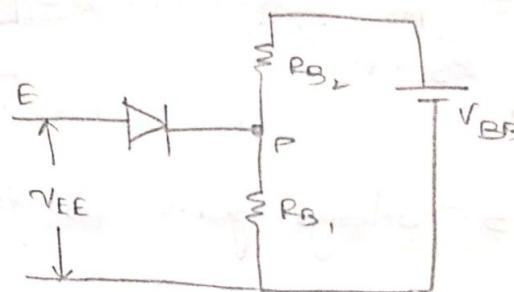
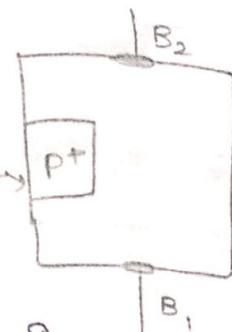
2. O/P impedance
 $Z_o \approx R_D$

3. Voltage gain.

$$A_v = g_m R_D$$

* unit junction transistor (UJT):

- It is also called as double base diode.
- Consider n-type substrate & heavily doped p⁺ region is diffused into it. Therefore, 1 PN Jn is formed. Top & bottom 2 ohmic contacts are made (B_1, B_2).
- This is the construction of UJT & it has 3 terminals emitter, base 1, base 2.



→ case 1: When $V_{EE} > 0$, $V_{BB} > 0$, the UJT is in off position, flow of current is 0.

Case-2: When $V_{EE} = 0$, $V_{BB} = +ve$, the UJT is in off position, the voltage at point P is given as

$$V_P = \frac{V_{BB} R_{B_1}}{R_{B_2} + R_{B_1}}$$

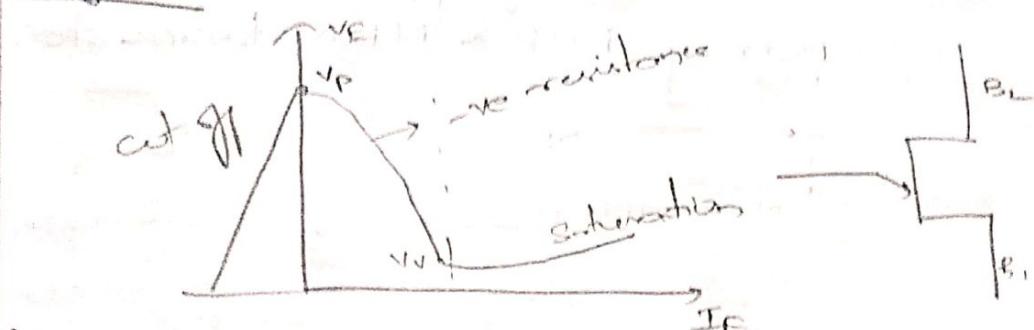
$$V_P = \eta V_{BB}$$

where η is intrinsic stand off ratio.

η varies b/w 0.5 to 0.8.

(This value of η varies on doping level)

Case-3: When $V_{BE} > V_{AV}$, the UJT is said to be in ON position. When UJT is ON, the holes from p+ region will inject into n-type region (due to V_{BE}). All the holes which are emitted from the emitter are repelled by V_{BB} . Hence, they accumulate into B_1 regions. Due to this, base 1 region resistance decreases. Hence voltage drop at emitter terminal (V_E) also will current to. Hence this region of operation is called negative resistance region.



- (e) Emitter Voltage decrease upto valley voltage (V_V)

Case-4: When $V_{BB} = 0$, $V_{ES} \neq 0$ then it is similar to PN diode.

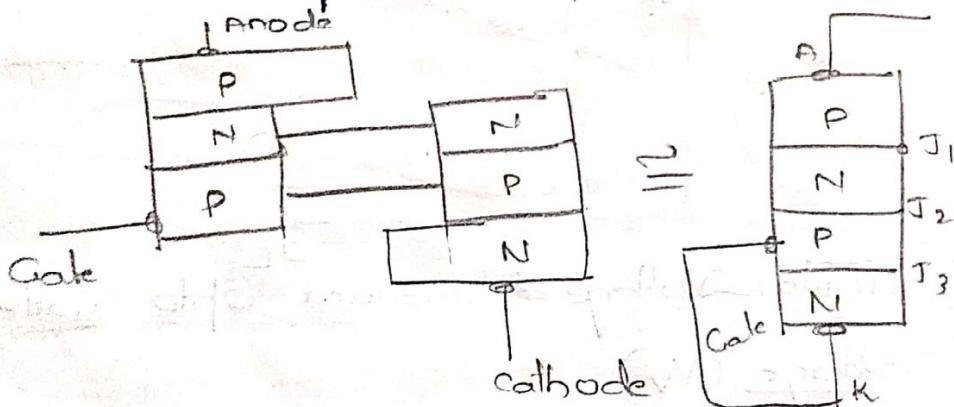
Case-5: When $V_{BB} \downarrow$ then the graph shifts downwards.

- (e) Applications of UJT:

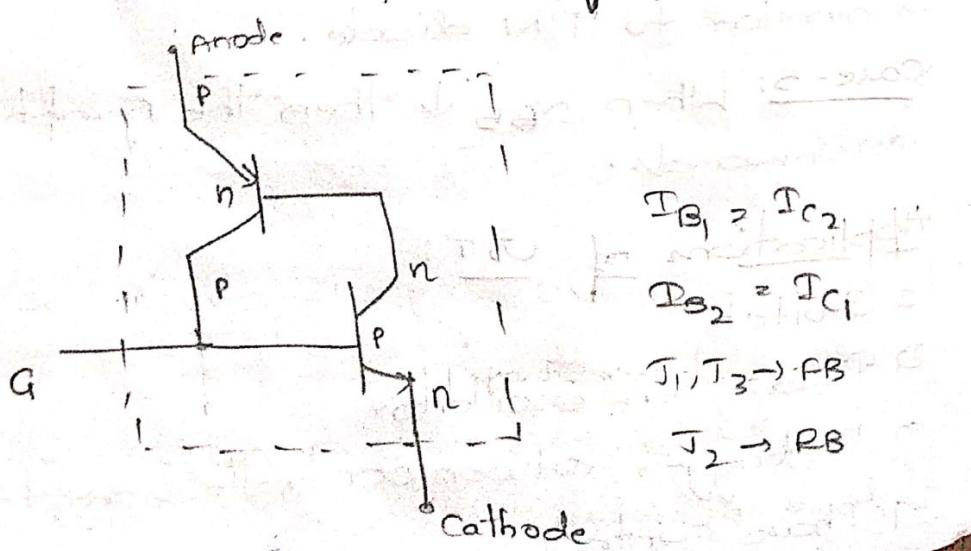
1. Switch
2. Relaxation oscillator
3. To trigger silicon controlled rectifier
4. Phase control.

5. In timing circuits.

- * Silicon controlled rectifier:
- SCR belongs to thyristor family.
- It is made up of silicon.
- The fn of SCR is similar to rectifier & its action is controlled by controlling terminal (gate).
- It is 4 layer 3 terminal 3 jns device.
- The 3 terminals are anode, cathode, gate.
- SCR is formed by the back to back connection of PNP & NPN transistors.



(c) Two transistor model of SCR:



→ SCR operates in 3 regions.

(i) Reverse blocking mode.

(ii) Forward blocking mode.

(iii) Forward conduction mode.

(a) Reverse blocking mode:

→ If Anode to cathode voltage is -ve, then T_1, T_3 get into RB mode & T_2 into FB. Hence SCR is turned off.

→ The characteristics are like to ordinary PN diode in reverse bias mode.

(b) Forward blocking mode:

→ By applying smaller +ve values b/w anode & cathode, Forward blocking mode is obtained.

→ In this, T_1 & T_3 are operated in FB mode whereas T_2 is RB mode.

→ In forward blocking mode also, SCR is said to be in turn off position only.

→ Minimum current is produced.

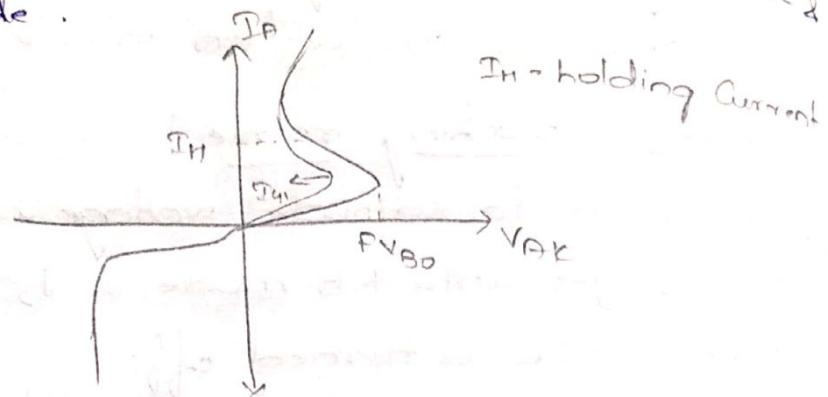
(c) Forward conduction mode:

→ It is obtained by forward blocking mode by applying $V_{AK} > V_{BO}$ (forward breakover voltage).

→ It is obtained by applying +ve gate pulse. In this region, T_1, T_3 are operated in

FB mode & T_2 is RB mode.

- When $V_{AK} > V_{BO}$, current suddenly I_A and voltage drop takes place b/w anode & cathode.



- The minimum current required to make SCR ON is called holding current.
→ When $I_{G1} > I_G$, the graph shifts towards left side

(c) Applications:

- Computer systems
→ tuning circuits
→ pulse generators
→ Oscillators
→ Voltage sensors

25/10/2019

Friday

* Zener diode!

- As a RB is applied to PN junction, reverse current flows from N-side to P-side.
→ If the reverse voltage is sufficiently large, current suddenly I_S & breakdown takes

place.

- Breakdown voltage is the voltage at which current suddenly \uparrow s (breaking the covalent bond)
- Breakdown mechanism is of 2 types.
 - (i) Zener breakdown
 - (ii) Avalanche breakdown
- Once breakdown occurs in ordinary PN diode, it never works but zener diode works.
- Zener diode is a specially designed diode which works under breakdown region also.
- Zener diode breakdown voltage varies from few volts to few hundreds of volts.
- Zener diode with low breakdown voltages made from heavily doped semiconductors & the breakdown takes place due to zener mechanism.
- Zener diode with high breakdown voltages made from lightly doped semiconductors & the breakdown is due to avalanche mechanism.

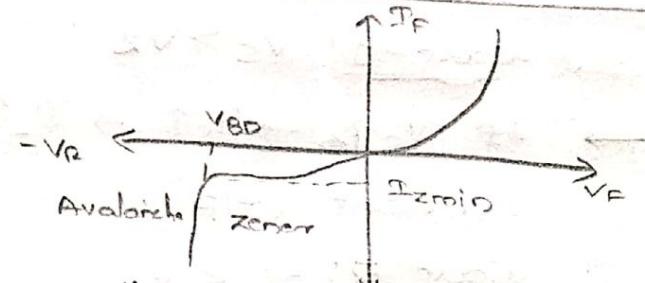
(c) Avalanche breakdown:

- It occurs in lightly doped diodes (The BD voltage may be $> 6V$)
- As a reverse voltage \uparrow , the minority charge carriers travel into the depletion region

- and acquire kinetic energy due to this speed. At that speed they collide with semiconductor atoms.
- During this process, part of kinetic energy is transferred to the semiconductor atoms & covalent bond breakdown.
- Due to this, generation of e^- s & holes are take place.
- The generated holes & e^- s acquire energy from source supplied (reverse voltage) & hit the semiconductor atom. Thereby - generation of holes & atoms takes place.
- The process is cumulative.
- This process is called avalanche breakdown or avalanche multiplication.
- Current is here.
- (c) Zener breakdown:
- It occurs in heavily doped diodes. (The BD Voltage is $< 6V$).
- In heavily doped diodes, strong electric field is produced in this region.
- Due to this, low voltages are required to break the covalent bond.
- It has a \perp temp coefficient.

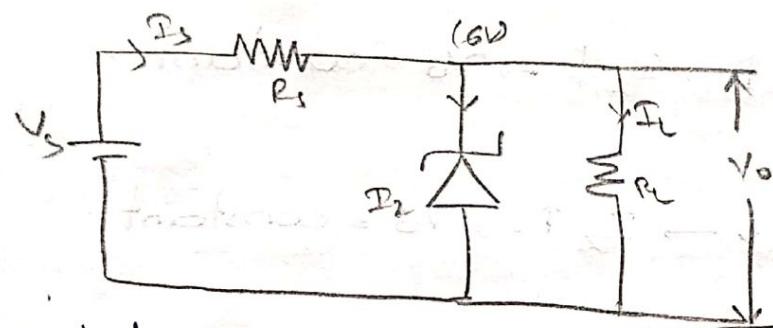
(e) Applications

- clippers
- voltage regulator.



(e) Zener diode as a voltage regulation:

- From the above graph, the voltage b/w I_{Zmin} to I_{Zmax} is constant. [Breakdown voltage]
- Hence, in a breakdown region zener diode works as an ideal voltage source.
- It can be used as a voltage regulator.



→ Regulator is a ckt which maintains constant o/p voltage irrespective of the changes in supply & load.

→ Regulation is of 2 types.

(i) line regulation:

→ Regulation of voltage irrespective of variations in supply voltage is called line regulation (load is fixed).

$$\text{From fig, } I_S = \frac{V_S - V_Z}{R_S} \quad \text{--- (1)}$$

$$I_S = I_Z + I_L \quad \text{--- (2)}$$

and acquire kinetic energy, due to this speed. So, with that speed they collide with semiconductor atoms.

- During this process, part of kinetic energy is transferred to the semiconductor atoms & covalent bond breakdown.
- Due to this, generation of e^- s & holes core take place
- The generated holes & e^- s acquire energy from source supplied (reverse voltage) & hit the semiconductor atom. Thereby generation of holes & atoms takes place.
- The process is cumulative.
- This process is called avalanche breakdown/ avalanche multiplication.
- Current is here.

(c) Zener breakdown:

- It occurs in heavily doped diodes. (The BD Voltage is $< 6V$).
- In heavily doped diodes, strong electric field is produced in this region.
- Due to this, low voltages are required to break the covalent bond.
- It has a +ve temp coefficient.

Case-1: $V_S > V_Z$

→ If $V_S \uparrow$ $\rightarrow I_S \uparrow \rightarrow I_Z \uparrow$ no the voltage is constant (o/p). (from ex ②)

Case-2: $V_S < V_Z$

→ If $V_S \downarrow \rightarrow I_S \downarrow \rightarrow I_Z \downarrow$ no constant output. (o)

(ii) load regulation:

→ Regulation of voltage irrespective of the variations in the load resistance.

(source is fixed $V_S > V_Z$) o. V_{BD}

Case-1:

→ $R_L \downarrow \rightarrow I_L \uparrow \rightarrow I_Z \downarrow \rightarrow V_o = \text{constant}$.

Case-2:

→ $R_L \uparrow \rightarrow I_L \downarrow \rightarrow I_Z \uparrow \rightarrow V_o = \text{constant}$.

Q. $V_S = 9V$, $R_S = 50\Omega$, $I_{Z\min} = 5mA$ find $R_{L\min}$

$$\frac{V_S}{R_S} = I_S \rightarrow I_S = \frac{9}{50} \text{ to maintain } V_o = 6V$$

$$\frac{9}{50} = \frac{9 - V_Z}{50}$$

$$\frac{9}{50} = \frac{9}{50} - \frac{V_Z}{50}$$

$$I_S = \frac{V_S - V_Z}{R_S}$$

$$I_S, I_Z + I_L \text{ and } (o)$$

$$V_o = I_L R_L$$

$$I_L R_L = I_Z R_Z$$

$$I_S = \frac{9 - 6}{50}, 0.06A$$

$$I_L = I_S - I_Z = 0.06 - 0.005 = 60 - 5, 55mA$$

$$I_L = 55mA$$

$$V_o = R_L I_L$$

$$R_{L\min} \Rightarrow \frac{V_o}{I_{L\max}} = \frac{6 \times 10^3}{55} = \frac{6000}{55} \approx 109.09 \Omega$$

(c) Note:

$$R_{L\min} \Rightarrow \frac{V_o}{I_{L\max}} \quad [I_{L\max} = I_S - I_{Z\min}]$$

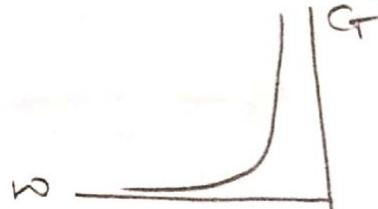
$$R_{L\max} \Rightarrow \frac{V_o}{I_{L\min}} \quad [I_{L\min} = I_S - I_{Z\max}]$$

* Vareactor diode:

- It exists when the diode operates in PBr mode.
- As reverse voltage is applied to PN jn, majority charge carriers move away from the jn, due to this there exists the change in charge w.r.t applied voltage.
- Hence, capacitance exists called junction capacitance or space charge region capacitance.

$$C_J = \frac{\epsilon A}{d}$$

- Hence, vareactor diode is also called varicap / variable capacitor / voltage variable voltage capacitor



(c) Applications:

- In tuning circuits
- FM radios

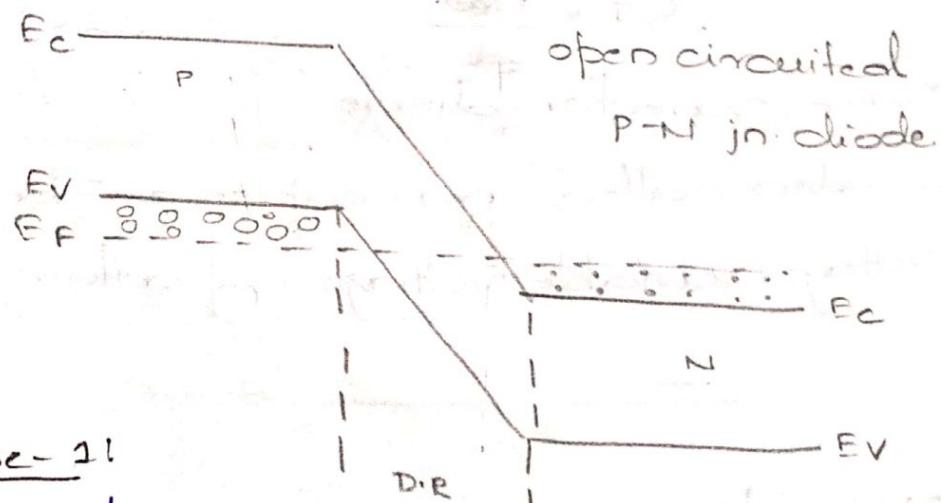
- Modulation
- TV receivers
- * Tunnel diode :- (Esaki diode)
- In the honour of Scientist Leo Esaki, it was named as Esaki diode.
- Tunnel diode is a heavily doped diode.
- As we know that, in heavily doped diode thin depletion layer is formed.
- Due to this, the charge carriers instead of crossing the jn, they penetrate through the depletion region.

→ This is known as tunneling effect.

→ The diode which exhibits tunneling property is called tunnel diode.



→



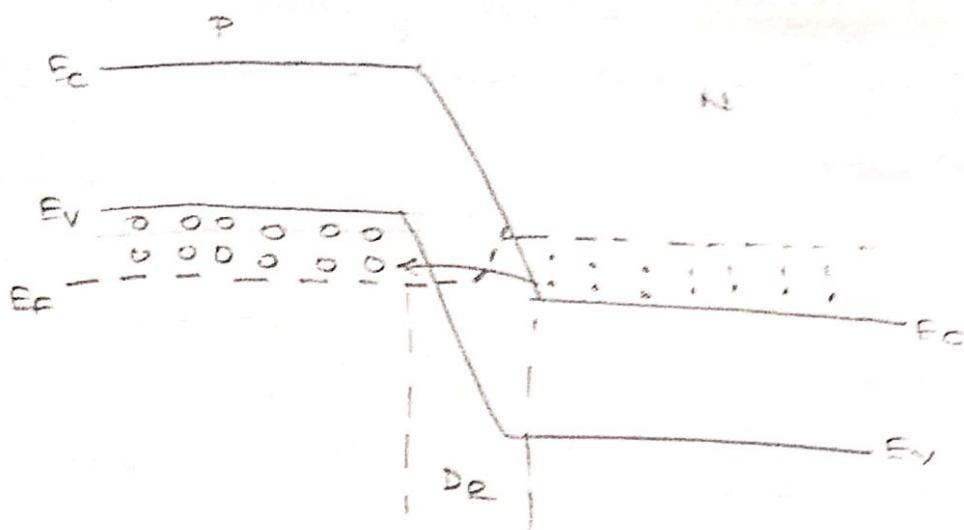
Case-1

→ Current = 0

Case-2:

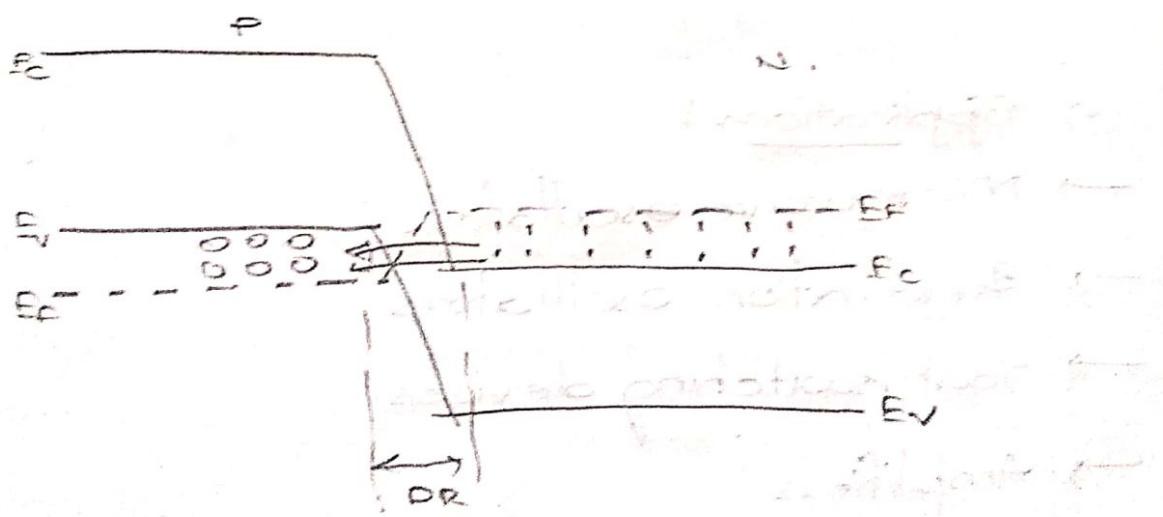
Small FB is applied (consider p-type is

grounded i.e. n-type is given forward bias).

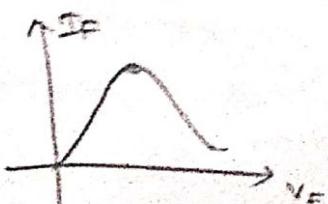


③ Few electrons penetrate through the tunnel i.e., through depletion region like as shown in fig. Hence small forward current exists.

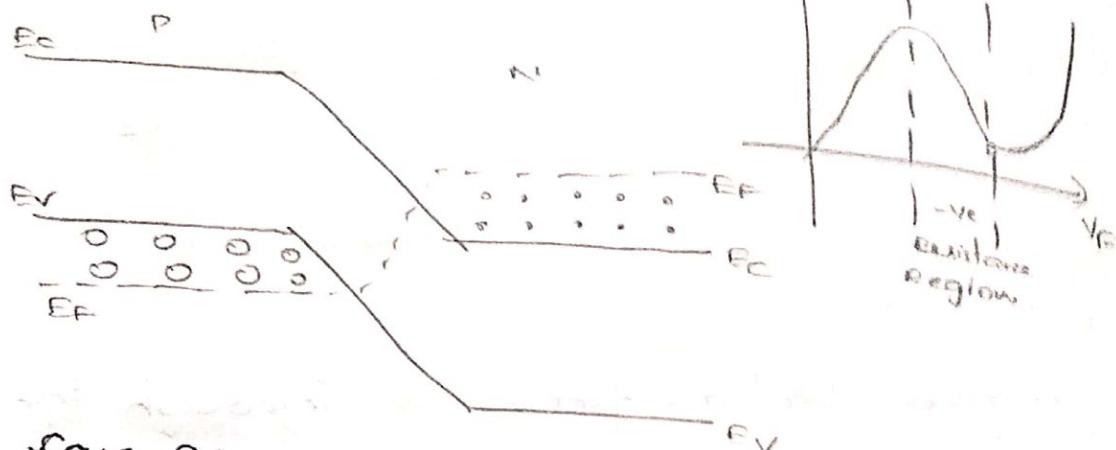
→ Case-3 : Forward voltage $V \approx V_a$.
More no. of e⁻s tunnel through the depletion region. Hence current $I \approx I_s$.



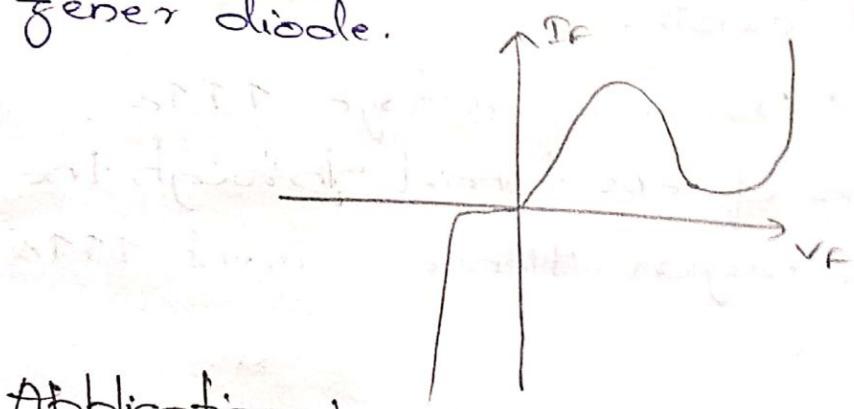
→ Case-4: As further forward voltage $V \gg V_a$. Tunneling of e⁻s is, current also is.



→ Case-5: If further the forward voltage is increased, tunneling effect is stopped & it acts like a ordinary diode.



→ Case-6: If reverse voltage is applied to tunnel diode, then it acts similar to zener diode.



(c) Applications:

- Microwave oscillators
- Relaxation oscillators
- Fast switching devices
- Amplifiers
- Logic memory devices

DESIGN AND ANALYSIS OF SMALL SIGNAL

LOW FREQUENCY AMPLIFIERS

- Amplifier is the ckt which is the amplitude of the i/p signal without any change in information.
- Strengthening of weak signal without any change in information is called amplification.
- The imp. characteristics of amplifier are voltage gain (A_v), current gain, i/p & o/p impedance.
- Amplifier uses both ac & dc signals
- DC is for proper biasing & AC is for amplification. (DC - providing stability).

* Types of amplifiers :-

I Based on configuration :

1. CE amplifier
2. CB
3. CC

II Based on signal :

1. Small signal amplifiers.
2. Large signal

III Based on o/p :

1. Voltage Amplifier 3. Power
2. Current

IV. Based on frequency:

1. Low freq. (audio freq.)
2. High freq. (radio freq.) \rightarrow Tuned Amplifiers

V. Based on type of coupling: (multistage amplifiers)

1. RC coupled
2. Transformer coupled
3. Direct coupled

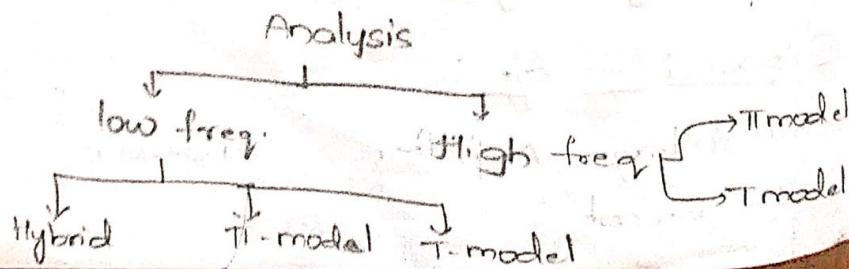
VI. Based on conduction angle: (power amplifiers)

1. class - A (360°)
2. class - B (180°)
3. class - AB ($180^\circ - 360^\circ$)
4. class - C ($< 180^\circ$)
5. class - D } switched mode
6. class - E } Amplifiers.
7. class - S }

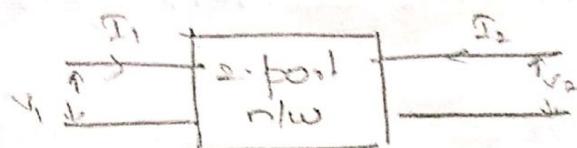
VII. Based on feedback:

1. Negative feedback
2. Positive feedback or oscillator

* Analysis of amplifiers:



- Hybrid/h-parameter model:
- As with z-parameter analysis can be done by a 2-port N/W (N/W having 2 ports) i/p & o/p port
- i/p port has 2 terminals - i/p voltage (v_1)
i/p current (I_1)
- o/p port has 2 terminals - o/p voltage (v_2)
o/p current (I_2)



- There are several parameters of a 2-port N/W - (1) Z parameters
(2) Y (3) h (4) g (5) ABCD (6) abcd.
- Among these, h-parameter model is preferred to analyze the transistor / amplifier.
- All the imp. characteristics of amplifier are obtained from the h-parameter model.
- $\begin{bmatrix} v_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ v_2 \end{bmatrix}$

$$v_1 = h_{11}I_1 + h_{12}v_2$$

$$I_2 = h_{21}I_1 + h_{22}v_2$$

$$v_2 = 0 \Rightarrow h_{11} = \frac{v_1}{I_1}; h_{21} = \frac{I_2}{I_1} \Rightarrow \text{port 2-s.c}$$

$$I_1 = 0 \Rightarrow h_{12} = \frac{v_1}{v_2}; h_{22} = \frac{I_2}{v_2} \Rightarrow \text{port 1-o.c}$$

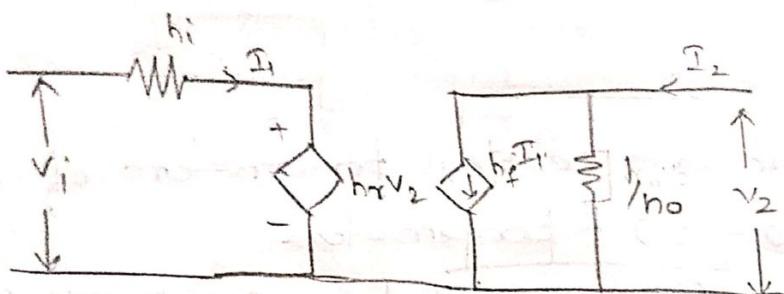
- $b_{11} \rightarrow i/p$ impedance $\rightarrow h_i$
- $b_{21} \cdot$ forward current gain $\rightarrow h_f$
- $b_{22} \cdot o/p$ admittance $\rightarrow h_o$
- $b_{12} \cdot$ Reverse voltage gain $\rightarrow h_{\pi}$

$v_1 = h_i I_1 + h_{\pi} v_2 \rightarrow i/p$ equation — ①

$I_2 = h_f I_1 + h_o v_2 \rightarrow o/p$ equation. — ②

Eq ① represents voltage generator

Eq ② represents current generator



b-parameter model of transistors.

v_1 = i/p voltage

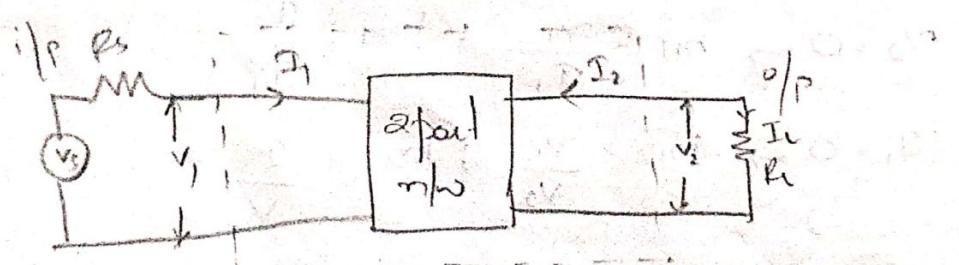
I_1 = i/p current

v_2 = o/p voltage

I_2 = o/p current

* Analysis of a transistor using b-param. : Wednesday

→ To get the analysis, i/p side source & o/p side load is added. (Exact model).



Current gain:

It is defined as the ratio of o/p current to i/p current.

$$A_I = -\frac{I_2}{I_1} = \frac{I_L}{I_1}$$

$$\text{As w.k.t, } I_2 = h_f I_1 + h_o V_2$$

$$I_2 = h_f I_1 + h_o (I_1 R_L)$$

$$I_2 = h_f I_1 + h_o (-I_2 R_L)$$

$$I_2 + I_2 h_o R_L = h_f I_1$$

$$I_2 [1 + h_o R_L] = h_f I_1$$

$$\frac{I_2}{I_1} = \frac{h_f}{1 + h_o R_L}$$

$$A_I = -\frac{h_f}{1 + h_o R_L} = \frac{h_f}{h_o R_L - 1}$$

Input impedance:

It is defined as the ratio of i/p voltage to i/p current.

$$Z_i = \frac{V_1}{I_1}$$

$$\text{As w.k.t, } V_1 = h_i I_1 + h_r V_2$$

$$V_1 = h_i I_1 + h_r (I_1 R_L)$$

$$V_1 = h_i I_1 - h_r I_2 R_L$$

$$V_1 = h_i I_1 + h_r A_I I_1 R_L$$

$$\left[\because A_I = -\frac{I_2}{I_1} \right] V_1 = I_1 [h_i + h_r A_I R_L]$$

$$\frac{V_1}{I_1} = h_i + h_r A_I R_L$$

$$Z_i = h_i + A_I h_o R_L$$

3. Voltage Gain:

$$A_V = \frac{V_2}{V_1}$$

As. w.k.t., $V_2 = I_L R_L$

$$A_V = \frac{I_L R_L}{V_1}$$

$$A_V = -\frac{I_2 R_L}{V_1}$$

$$A_V = \frac{A_I I_1 R_L}{V_1}$$

$$A_V = \frac{A_I R_L}{Z_i}$$

$$\therefore A_V = \frac{A_I R_L}{Z_i}$$

4. Output impedance / Admittance:

$$Y_o = \frac{I_2}{V_2}$$

$$Y_o = \frac{I_2}{+I_2 R_L}$$

$$Y_o = +\frac{1}{R_L}$$

$$Z_o = +R_L \quad [\text{Resistance is not -ve}]$$

$$Y_o = \frac{I_2}{V_2} \quad / V_S = 0, R_L = \infty$$

$$I_2 = h_f I_1 + h_o V_2$$

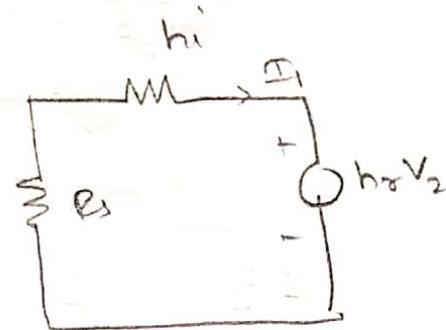
$$\frac{I_2}{V_2} \rightarrow Y_o = h_f \frac{I_1}{V_2} + h_o \longrightarrow ①$$

Apply KVL,

$$0 = (R_s + h_i) I_1 + h_o v_2$$

$$\frac{I_1}{v_2} = -\frac{h_o}{R_s + h_i} \quad (2)$$

$$A_v = \frac{I_2}{v_2} = h_o - \frac{h_f h_o}{R_s + h_i}$$



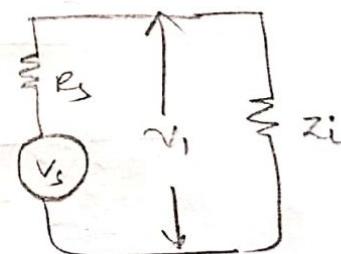
* Note:

Overall voltage gain (including source),

$$A V_S = \frac{V_2}{V_S} \rightarrow \frac{V_2}{V_1} \cdot \frac{V_1}{V_S}$$

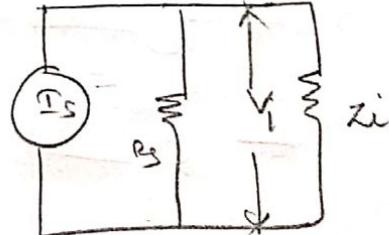
$$A V_S = A_v \cdot \frac{V_1}{V_S}$$

$$V_1 = \frac{V_S \cdot Z_i}{R_s + Z_i} \Rightarrow \frac{V_1}{V_S} = \frac{Z_i}{Z_i + R_s}$$

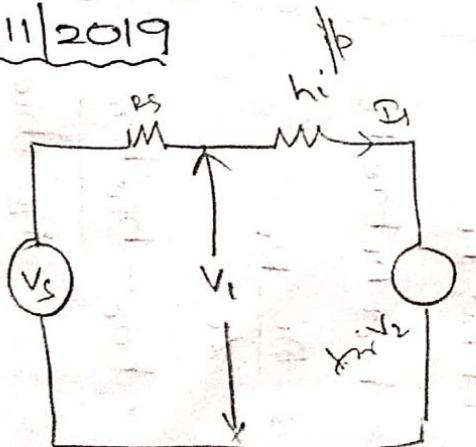


Overall current gain ($A I_S$),

$$A I_S = \frac{A_I \cdot R_S}{R_S + Z_i}$$

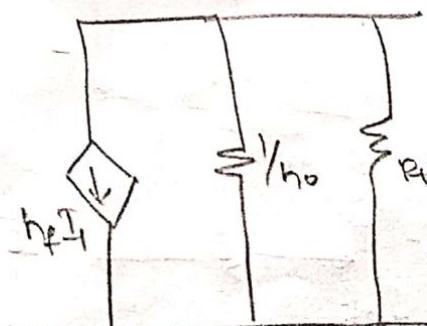


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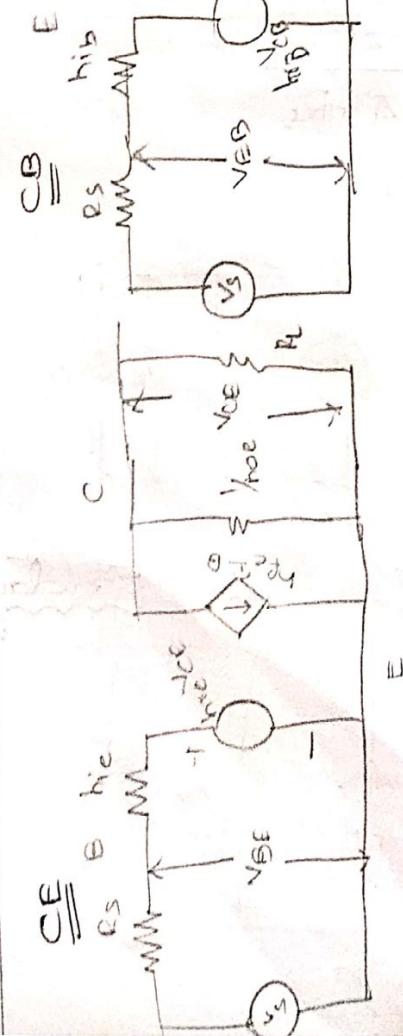


O/p

Friday



General model.

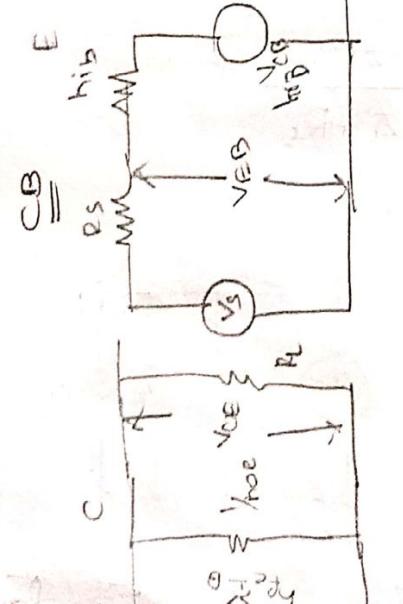


$$A_i = \frac{h_{fe}}{1 + h_{oe} R_L}$$

$$Z_i = h_{ie} + A_i h_{re} R_L$$

$$A_v = \frac{A_i R_L}{Z_i}$$

$$Y_0 = h_{oe} - h_{fe} h_{re} \frac{R_L + h_{ie}}{R_S + h_{ie}}$$

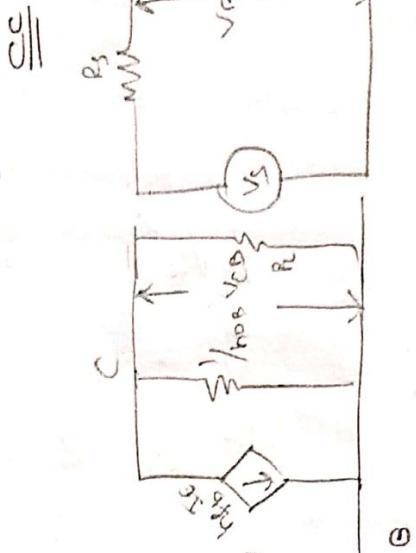


$$A_i = \frac{-h_{fb}}{1 + h_{oe} R_L}$$

$$Z_i = h_{ie} + A_i h_{re} R_L$$

$$A_v = \frac{A_i R_L}{Z_i}$$

$$Y_0 = h_{oe} - h_{fb} h_{re} \frac{R_L + h_{ie}}{R_S + h_{ie}}$$

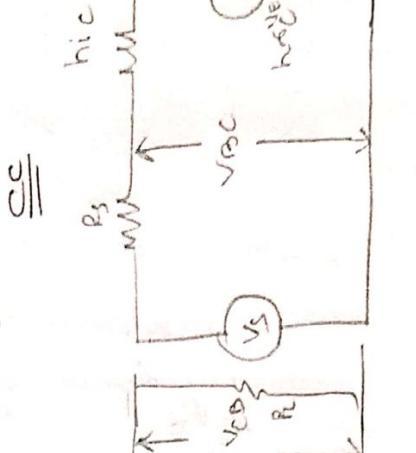
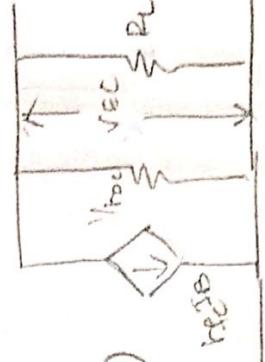


$$A_i = \frac{-h_{fc}}{1 + h_{oe} R_L}$$

$$Z_i = h_{ie} + A_i h_{re} R_L$$

$$A_v = \frac{A_i R_L}{Z_i}$$

$$Y_0 = h_{oe} - h_{fc} h_{re} \frac{R_L + h_{ie}}{R_S + h_{ie}}$$

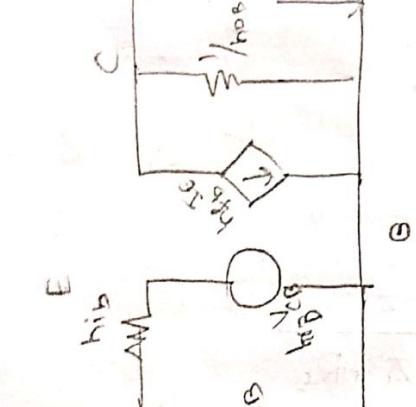


$$A_i = \frac{-h_{fe}}{1 + h_{oe} R_L}$$

$$Z_i = h_{ie} + A_i h_{re} R_L$$

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$$Y_0 = h_{oe} - h_{fe} h_{re} \frac{R_L + h_{ie}}{R_S + h_{ie}}$$

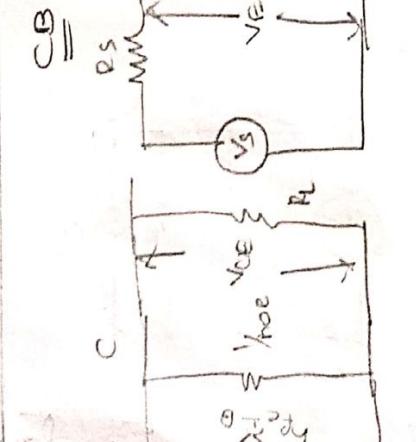


$$A_i = \frac{-h_{fb}}{1 + h_{oe} R_L}$$

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$$Y_0 = h_{oe} - h_{fb} h_{re} \frac{R_L + h_{ie}}{R_S + h_{ie}}$$



$$A_i = \frac{-h_{fc}}{1 + h_{oe} R_L}$$

$$Z_i = h_{ie} + A_i h_{re} R_L$$

$$A_v = \frac{A_i R_L}{Z_i}$$

$$Y_0 = h_{oe} - h_{fc} h_{re} \frac{R_L + h_{ie}}{R_S + h_{ie}}$$

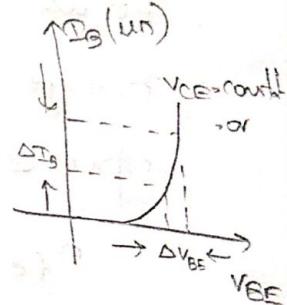
* Determination of h-parameters from characteristics

1: CE: i/p \rightarrow B, E, o/p \rightarrow C, E.

(i) h_{ie} : Input impedance
It is defined as the ratio of small change in input voltage to the input current.

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} / V_{CE} = \text{constant}$$

Eg:
$$\frac{\Delta V_{BE}}{\Delta I_B} = \frac{0.68 - 0.66}{(40 - 20) \mu\text{A}} \approx 1 \text{k}\Omega$$

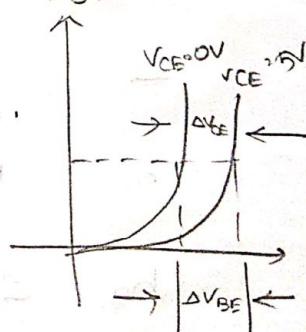


$h_{ie} = 1100 \Omega \Rightarrow$ standard value.

(ii) h_{re} : Reverse voltage gain
It is defined as the ratio of small change in input voltage to that of output voltage. $h_{re} = 2.5 \times 10^4$, st. value $I_B (\mu\text{A})$

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}} / I_B = \text{constant}$$

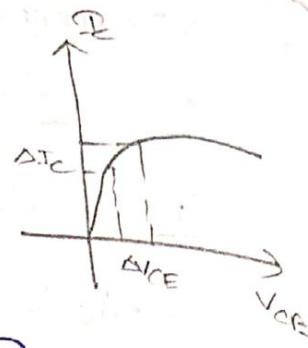
Eg: $h_{re} = \frac{0.68 - 0.60}{5.0} \approx 0$



(iii) h_{oe} : Output admittance

It is defined as the ratio of small change in output current to that of output voltage.

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}} / I_B = \text{constant}$$



Eg. $h_{oe} = 25 \frac{\mu A}{V} \Rightarrow \text{st. value}$

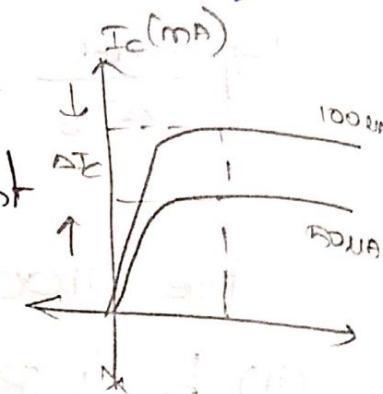
$$h_{oe} = (4-2) \mu A / (4-2) \approx 0.$$

(iv) h_{fe} : Forward current gain

It is defined as the ratio of small change in output current to that of input current.

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B} / V_{BE} = \text{constant}$$

Eg. $h_{fe} = \frac{(8-4) \times 10^{-3}}{50 \times 10^{-6}} = 80$



$$h_{fe} = 50 \Rightarrow \text{st. value.}$$

* Typical h-parameters!

	CE	CB	CC
h_i	1100Ω	21.6Ω	1100Ω
h_{re}	2.5×10^{-4}	2.9×10^{-4}	≈ 1
h_f	50	-0.98	-51
h_o	$25 \frac{\mu A}{V}$	$0.49 \frac{\mu A}{V}$	$25 \frac{\mu A}{V}$

Q. In a CE configuration, $R_S = 1\text{ k}\Omega$, $R_L = 2\text{k}\Omega$,
 $h_{ie} = 1\text{ k}\Omega$, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 50$, $h_{oe} =$
 $25 \mu\text{A/V}$ then determine A_i , Z_i , A_v , Z_o & Y_o .

For a ca configuration, $R_s = 18\text{ nm}$, $R_L = 2\mu\text{m}$

$h_{fb} = 0.1\text{ nm}$, $b_{fb} = 0.9 \times 10^{-9}$, $b_{sf} = -0.9$

$b_{sf} = 0.49 \times 10^{-9}$ after determine $A_1 Z_1 A_2$

65

In a CC configuration, $R_s = 1k\Omega$, $R_L = 2k\Omega$.
 $h_{ie} = 1k\Omega$, $h_{re} = 1$, $h_{fe} = 50$, $h_{oc} = 25 \frac{mV}{V}$
 Then determine A_i , Z_i , A_v , γ_o .

$$A_i = \frac{-h_{fe}}{1 + h_{oc} R_L}$$

$$= \frac{50}{1 + 25 \times 10^{-6} \times 10^3 \times 2}$$

$$= \frac{50}{1 + 25 \times 10^{-3} \times 2} = \frac{50}{1 + 50 \times 10^{-3}}$$

$$\Rightarrow 47.61$$

$$Z_i = 10^3 + 47.61 \times 1 \times 2 \times 10^3$$

$$= 10^3 [1 + 47.61 \times 2]$$

$$= 96.22 \times 10^3 \Omega$$

$$= 96.22 k\Omega.$$

$$A_v = \frac{A_i R_L}{Z_i}$$

$$= \frac{47.61 \times 2 \times 10^3}{96.22 \times 10^3}$$

$$= 0.989.$$

$$\gamma_o = \frac{h_{oc} - h_{fe} h_{re}}{R_s + h_{ic}}$$

$$= \frac{25 \times 10^{-6} + 50 \times 1}{10^3 + 10^3}$$

$$= 25 \times 10^{-6} + \frac{50}{2000}$$

$$= 25 \times 10^{-6} + 0.025 = \frac{25 \times 10^{-6} + 25 \times 10^{-3}}{25 [10^{-6} + 10^{-3}]}$$

$$Z_o = \frac{1}{Y_o} = \frac{1}{25 \times 10^6 + (0^3)} = \frac{1}{39.96 \times 10^3} = 13.306$$

	CE	CB	CC
A _i	-47.61	0.919	47.61
Z _i	976.1952	20.5852	96.22
A _v	-97.5	95.10	0.989
Z _o	53.3k ₂	≈ 1M ₂	39.96 ₂

* Comparison table:

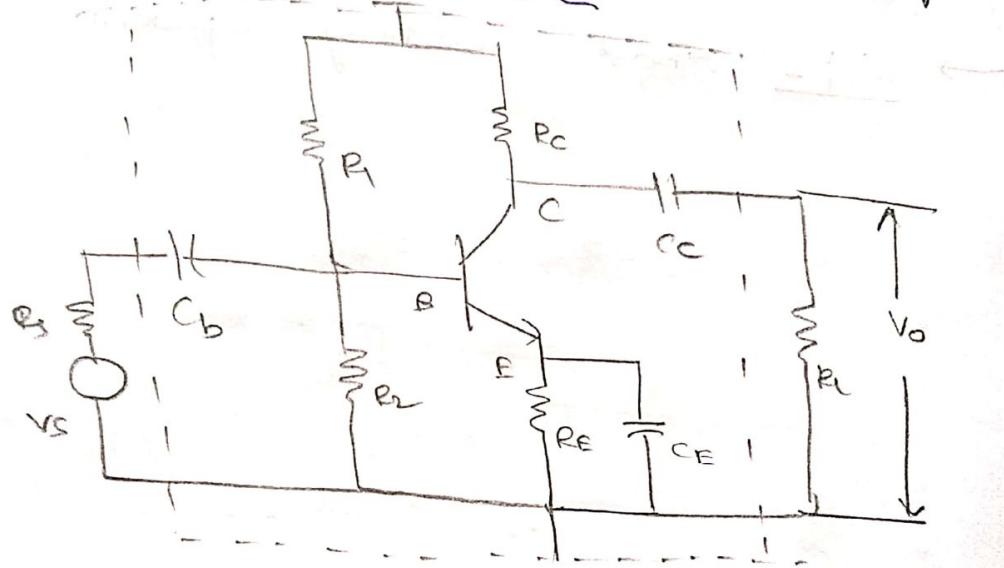
	CE	CB	CC
A _v	High	High	Unity
A _i	High	Unity	High
Z _i	Moderate	Low	High
Z _o	High	High	Low
Phase Shift	-180°	0°	0°
Application	Audio	Radio	Buffer
	Freq.	Freq.	

→ From the above table, it can be concluded that the CE amplifier can amplify both voltage and current.

and current signals. It also has moderate Z_o , Z_i . But CB, CC amplifiers amplify voltage & current signals respectively. Hence CE amplifier is preferred.

4/11/2019

- * CE amplifier - AC analysis: Monday



→ AC analysis can be obtained by following steps —

1. Short all the capacitors in the ckt.
2. DC power supplies are grounded.
3. Replace the transistor with its \approx model.

→ Above ckt shows CE amplifier in which base is a i/p terminal, collector is o/p terminal. Emitter is common.

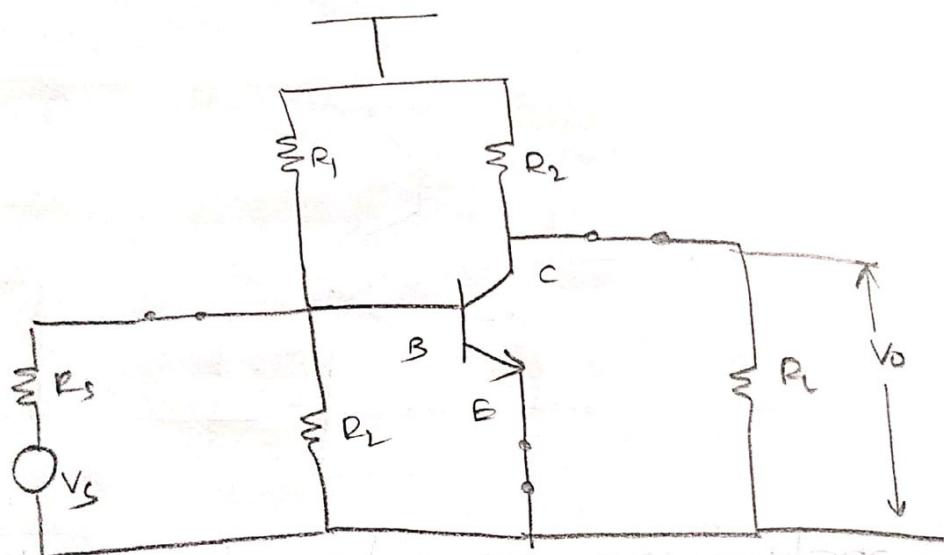
→ R_B & R_C provides proper biasing, R_E provides stability.

C_B , C_C are called blocking or coupling

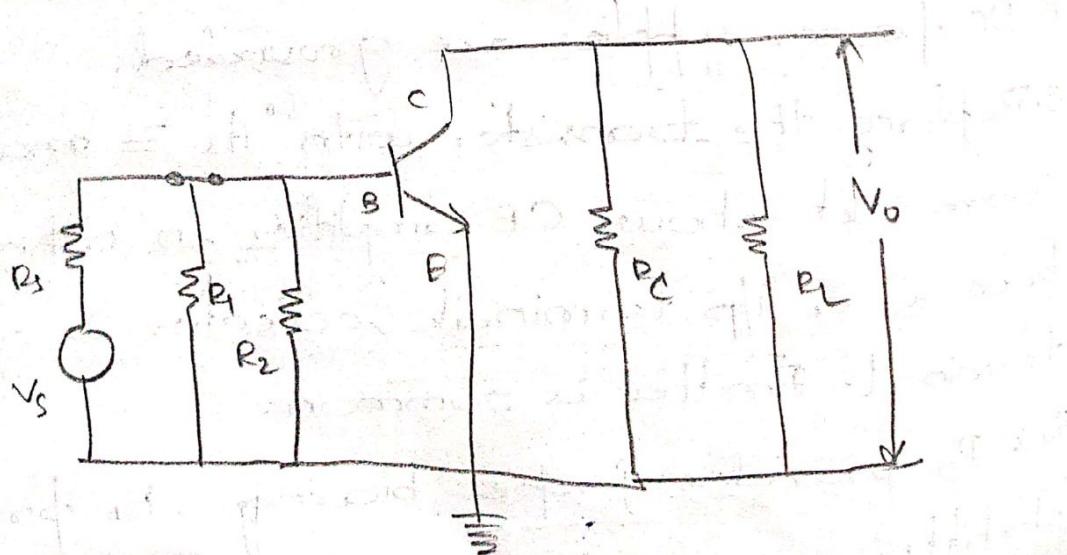
capacitors which block dc voltage & allow only ac signal. They can couple with the source signal to the amplifier or to the load.

→ C_E is called bypass capacitor which is used to \downarrow the voltage gain of amplifier (which is the degenerative effect \downarrow in the -ve feed back).

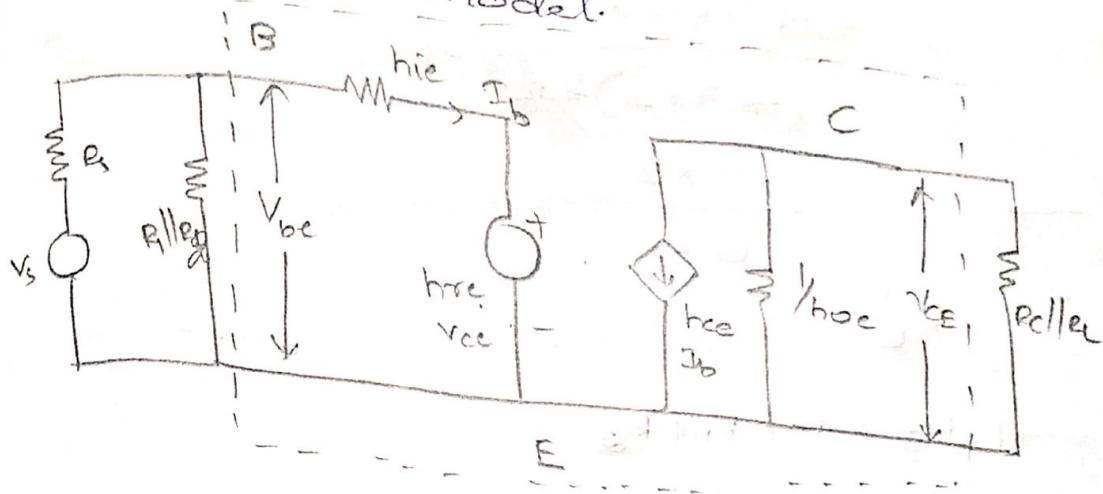
→ Step 1: Short circuiting capacitors



Step 2: Grounding DC sources.



Step-3: Replacing transistor with = least h-parameter model.



$$\rightarrow A_i = \frac{h_{fe}}{1 + h_{oe} R_L'}$$

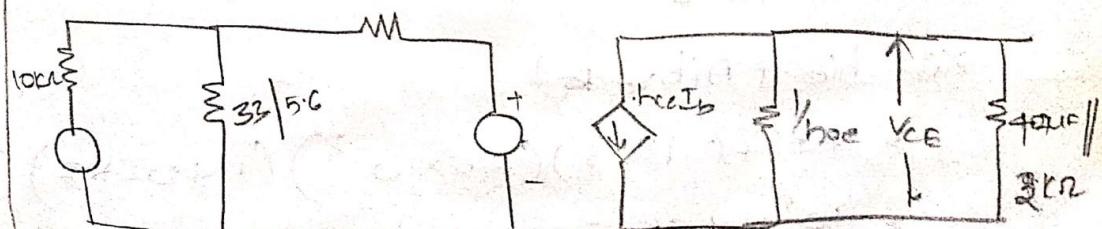
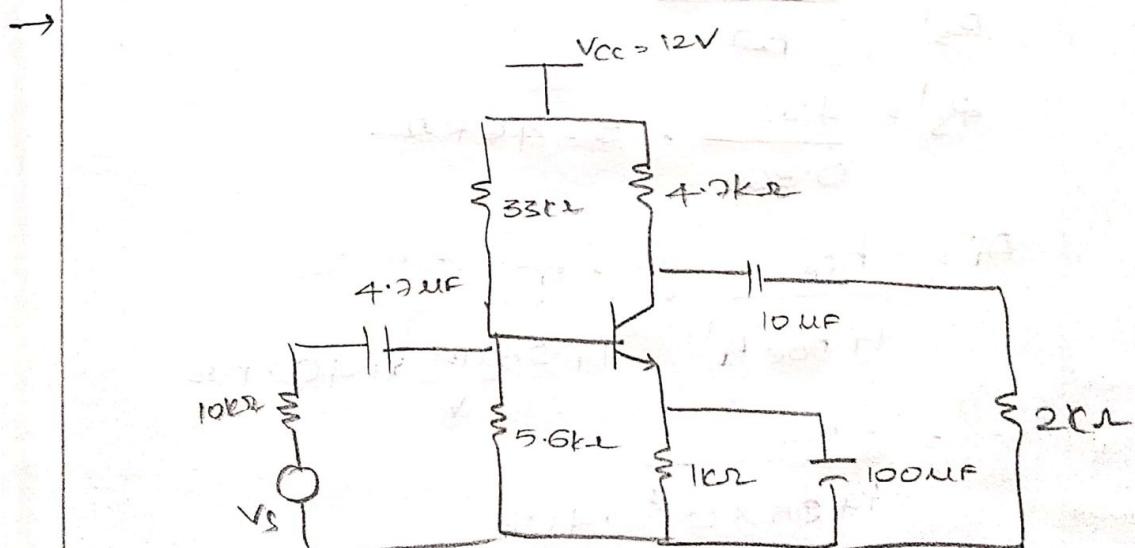
$$R_L' = R_C || R_L$$

$$Z_i = h_{ie} + A_i h_{re} R_L'$$

$$A_V = \frac{A_i R_L'}{Z_i}$$

$$Y_o = h_{oe} - \frac{h_{fe} h_{re}}{R_s' + h_{ie}}$$

$$R_s' = R_s || R_1 || R_2$$



$$R_L' = R_C \parallel R_L$$

$$\Rightarrow \frac{4.7 \text{ k}\Omega \times 2 \text{ k}\Omega}{(4.7 + 2) \text{ k}\Omega}$$

$$\Rightarrow \frac{4.7 \times 2}{6.7} \text{ k}\Omega$$

$$R_L' = 1.402 \text{ k}\Omega$$

$$R_S' = R_S \parallel R_1 \parallel R_2$$

$$\frac{1}{R_S'} = \frac{1}{R_S} + \frac{1}{R_1} + \frac{1}{R_2}$$

$$\frac{1}{R_1} = \frac{1}{10 \text{ k}\Omega} + \frac{1}{33 \text{ k}\Omega} + \frac{1}{56 \text{ k}\Omega}$$

$$\Rightarrow \frac{10^3}{10} + \frac{10^3}{33} + \frac{10^3}{56}$$

$$\Rightarrow \frac{0.1}{\text{k}\Omega} + \frac{0.0303}{\text{k}\Omega} + \frac{0.178}{\text{k}\Omega}$$

$$\frac{1}{R_S'} = \frac{0.308}{\text{k}\Omega}$$

$$R_S' = \frac{\text{k}\Omega}{0.308} = 3.246 \text{ k}\Omega$$

$$A_i = -\frac{h_{fe}}{1 + h_{fe} R_L'} = \frac{-50}{1 + 25 \frac{\mu\text{A}}{\text{V}} \times 1.402 \text{ k}\Omega}$$

$$= \frac{-50}{1 + 25 \times 10^{-3} \times 1.402}$$

$$= -48.3$$

$$Z_i = h_{ie} + A_i h_{re} R_L'$$

$$\Rightarrow 1 \text{ k}\Omega + (-48.3)(2.5 \times 10^{-4})(1.402 \text{ k}\Omega)$$

$$\Rightarrow 10^3 = 169.29 \times 10^{-2}$$

$$Z_i = 1000 - 16 \cdot 929$$

$$\Rightarrow 983.71 \text{ } \Omega$$

$$A_{v'} = \frac{A_i}{Z_i} R_L' = \frac{-48.3}{983.71} \times 1.402 \times 10^3$$

$$\Rightarrow -68.83$$

$$Z_o = h_{oe} - \frac{h_{fe} h_{re}}{R_s' + h_{ie}}$$

$$\Rightarrow 25 \times 10^{-6} - \frac{50 \times 2.5 \times 10^{-4}}{3.246 \times 10^3 + 10^3}$$

$$\Rightarrow 25 \times 10^{-6} - \frac{50 \times 2.5 \times 10^{-4}}{(4.246) \times 10^3}$$

$$\Rightarrow 25 \times 10^{-6} - \frac{50 \times 2.5}{4.246} \times 10^{-7}$$

$$\Rightarrow 25 \times 10^{-6} - 29.43 \times 10^{-7}$$

$$\Rightarrow 10^{-6} [25 - 29.43]$$

$$\Rightarrow 10^{-6} [25 - 2.943]$$

$$\Rightarrow 22.057 \times 10^{-6} \text{ } \Omega$$

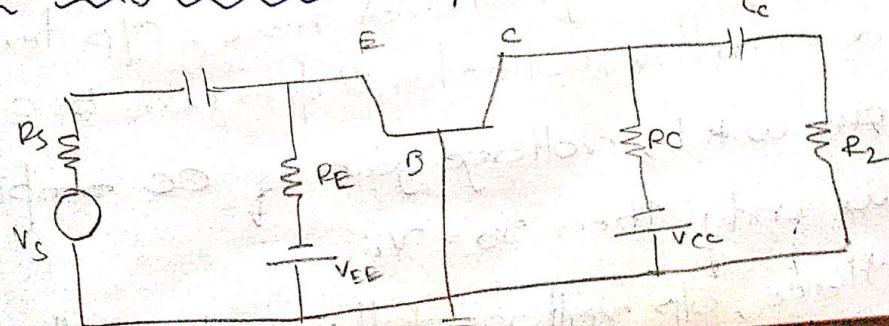
$$Z_o = \frac{10^6}{22.057} = 45337 \text{ } \Omega$$

$$\Rightarrow 45.33 \text{ k}\Omega$$

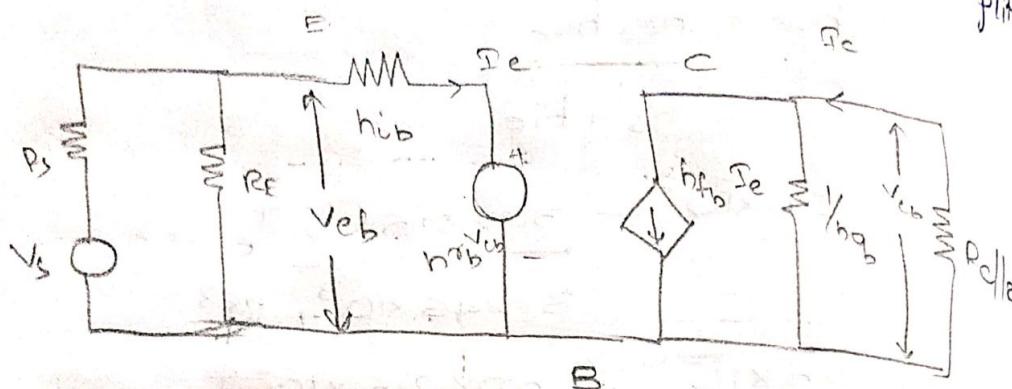
8/11/2019

Friday

* CB Configuration amplifier:



- It is CB amplifier with i/p terminals as base, emitter & o/p terminals base, collector.
- AC analysis is done like to CE amplif



$$A_i = -\frac{h_{FB}}{R_E}$$

$$= \frac{1 + h_{FB} R_L}{R_E}$$

$$Z_i = h_{bb'} + A_i h_{FB} R_L$$

$$A_V = \frac{A_i R_L}{Z_i}$$

$$\gamma_o = h_0 = \frac{h_{FB} h_{RE}}{R_E + h_{ie}}$$

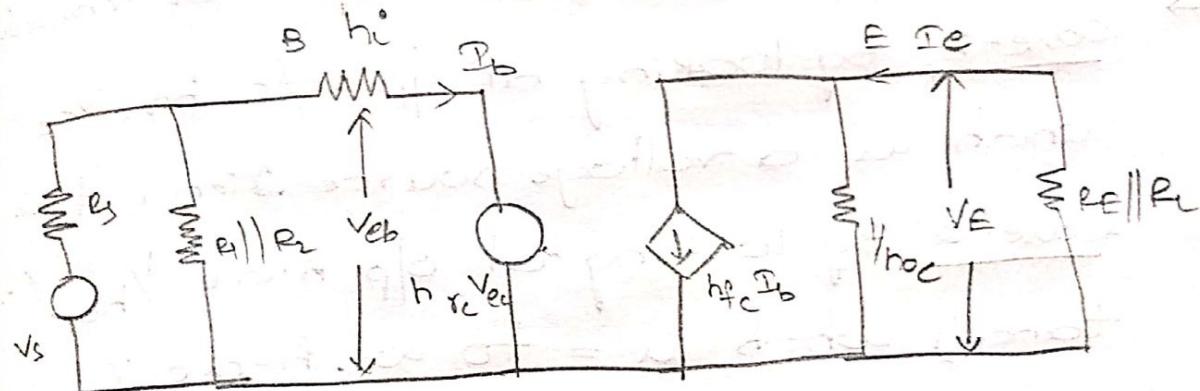
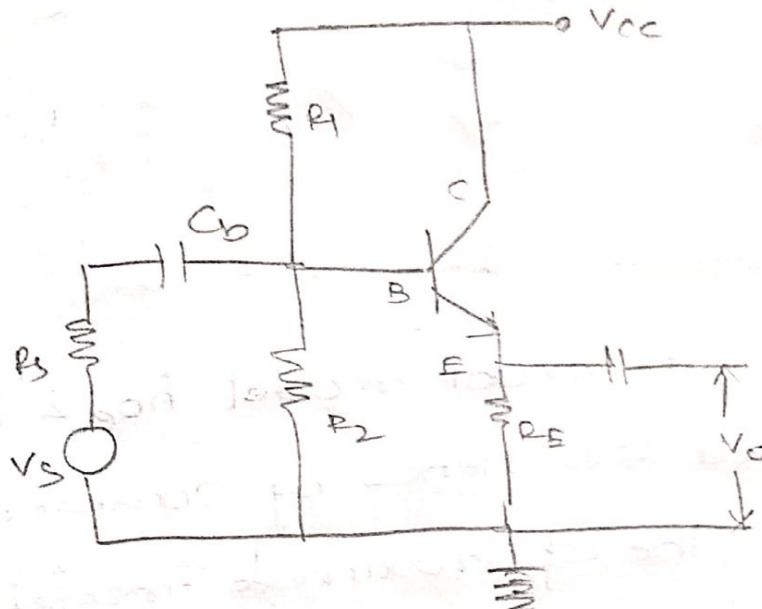
$$\text{where } R_S' = R_S \parallel R_E$$

$$R_L' = R_C \parallel R_L$$

* CC amplifier

- Collector is grounded here. O/p terminals are emitter, collector & i/p's are B, C.
- If w.r.t. voltage gain of CC amplifier is unity then $\gamma_o = V_o$.
- Hence, o/p voltage follows i/p voltage.

Therefore, CC amplifier is also called emitter follower.



$$A_i = \frac{-h_{fe}}{1 + h_{fe} R_L'}$$

$$Z_i = h_{fe} R_b + A_i h_{fe} R_L'$$

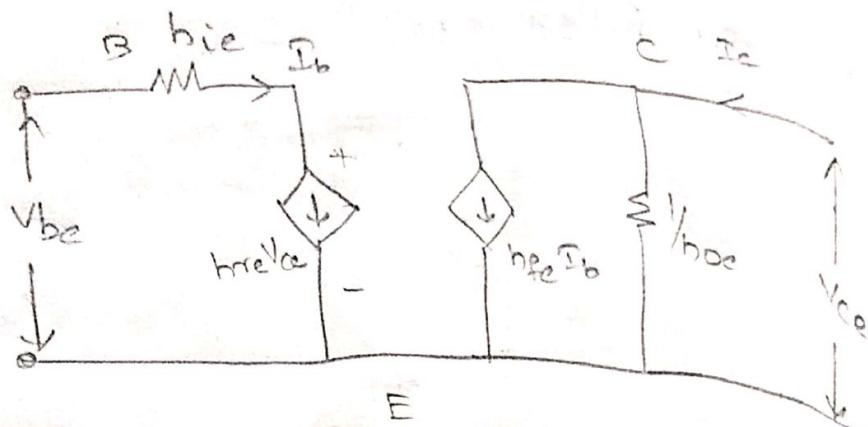
$$A_v = \frac{A_i R_L'}{Z_i}$$

$$Y_o = h_{oc} - \frac{h_{fe} R_L'}{R_g' + h_{ic}}$$

$$\text{where } R_L' = R_E \parallel R_L$$

$$R_g' = R_1 \parallel R_2 \parallel R_s$$

* Approximate or simplified model:

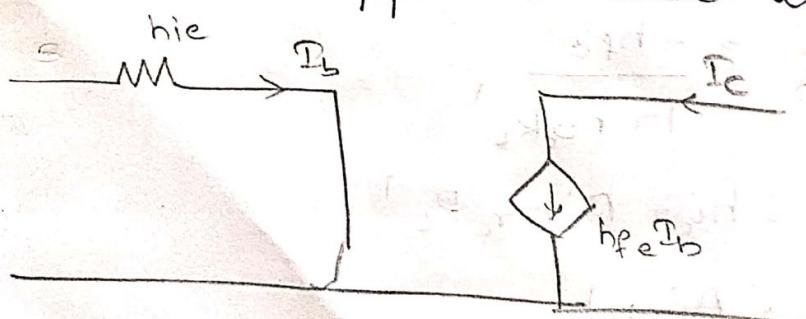


* CE

→ As w.k.t. an exact model h_{oe} & h_{re} values are ≈ 0 . Hence by considering $h_{re} = 0$, the approximate model is implemented which is simplified model.

→ Case-1: By looking at i/p side $h_{re}V_{ce} \gg 0$ which is a voltage source. Hence it is,

Case-2: By looking at o/p side Y_{hoe} (\Rightarrow tance) which is $= \infty$, hence Y_{hoe} is 0.C then the approx. model is,

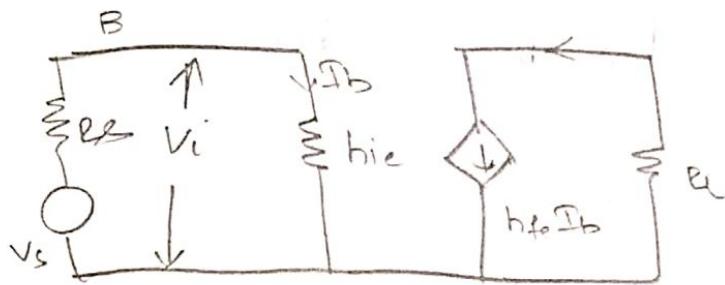


o
s
⇒

* C

→ Above model is applicable for CB, CC, CF configurations also. Hence, it is known as generalized mode.

* CE approximate model:



$$A_i = \frac{I_o}{I_i} = \frac{-h_{fe} I_b}{I_b} = -h_{fe}$$

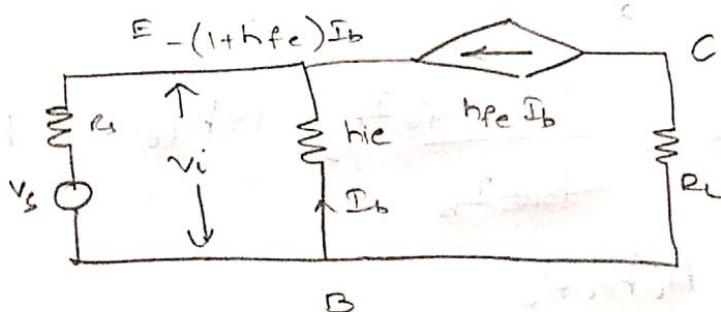
$$Z_i = \frac{V_i}{I_i} = \frac{h_{ie} I_b}{I_b} = h_{ie}$$

$$A_v = \frac{V_o}{V_i} = \frac{-h_{fe} I_b R_L}{h_{ie} I_b} = -\frac{h_{fe} R_L}{h_{ie}}$$

$$Y_o = \frac{I_o}{V_o} = \frac{-h_{fe} I_b}{-h_{fe} I_b R_L} = \frac{1}{R_L} = 0 \quad [\because R_L = \infty]$$

→ o/p admittance is obtained by keeping source voltage zero. ($V_s = 0$). Hence, $I_b > 0$
 \Rightarrow o/p current also zero. Therefore, $Y_o = 0$.

* CB approximate model:



$$A_i = \frac{I_o}{I_i} = \frac{-h_{fe} I_b}{-(1+h_{fe}) I_b} = \frac{h_{fe}}{1+h_{fe}} = -h_{fb}$$

$$Z_i = \frac{V_i}{I_i} = \frac{-h_{ie} I_b}{-(1+h_{fe}) I_b} = \frac{h_{ie}}{1+h_{fe}} = h_{ib}$$

$$A_V = \frac{V_o}{V_i} = \frac{-h_{fe} I_b R_L}{-h_{ie} I_b} = \frac{+h_{fe} R_L}{h_{ie}}$$

$$Y_o = \frac{I_o}{V_o} \Big|_{V_S=0} > 0.$$

CB Exact

$$A_i = -\frac{h_{fb}}{1+h_{ob}R_L}$$

$$Z_i = h_{ib} + A_i h_{rb} R_L$$

$$A_V = \frac{A_i}{Z_i} R_L$$

$$Y_o = h_{ob} - \frac{h_{fb} h_{rb}}{R_s + h_{ib}}$$

CB Approx.

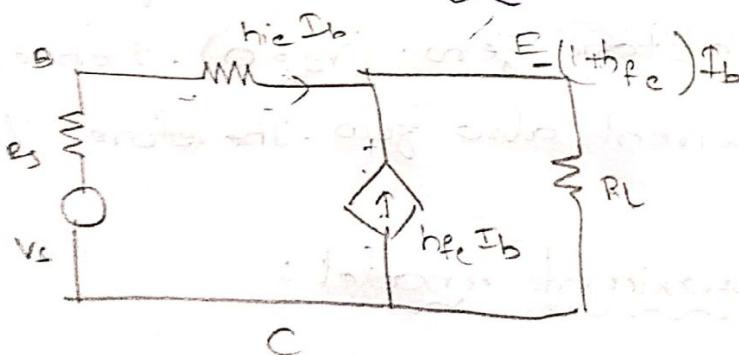
$$A_i = -h_{fb} = \frac{h_{fe}}{1+h_{fe}}$$

$$Z_i = h_{ib} = \frac{h_{ie}}{1+h_{fe}}$$

$$A_V = \frac{h_{fe}}{h_{ie}} R_L$$

$$Y_o = 0$$

* CC approximate model:



$$A_i = \frac{I_o}{I_i} = \frac{I_b + h_{fe} I_b}{I_b} = \frac{1 + h_{fe}}{1} = -h_{fe}$$

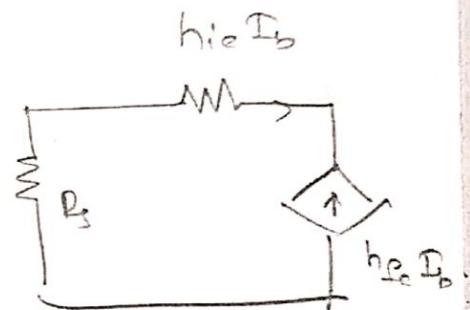
$$Z_i = h_{ie} + A_i h_{rb} R_L$$

$$\begin{aligned} &\Rightarrow \frac{V_i}{I_i}, \frac{h_{ie} I_b + (h_{fe}) I_b R_L}{I_b} \\ &= h_{ie} + (1 + h_{fe}) R_L \end{aligned}$$

$$\begin{aligned}
 A_V &= \frac{V_o}{V_i} = +\frac{(1+h_{fe}) R_L I_b}{h_{ie} I_b + (1+h_{fe}) I_b R_L} \\
 &\rightarrow \frac{(1+h_{fe}) R_L I_b}{(h_{ie} + (1+h_{fe}) R_L) I_b} \\
 &\rightarrow \frac{(1+h_{fe}) R_L}{h_{ie} + (1+h_{fe}) R_L} \approx 1
 \end{aligned}$$

$$Y_0 = \frac{I_0}{V_o} / V_s = 0$$

$$\begin{aligned}
 &\rightarrow \frac{I_b (1+h_{fe})}{(1+h_{fe}) R_L I_b} \\
 &= \frac{(R_s + h_{ie}) I_b}{(R_s + h_{ie}) I_b}
 \end{aligned}$$



$$Y_0 = \frac{I_0}{V_o} = \frac{(1+h_{fe}) I_b}{(R_s + h_{ie}) I_b} = \frac{1+h_{fe}}{R_s + h_{ie}}$$

CC Exact

$$A_i = -\frac{h_{fe}}{1+h_{oc} R_c}$$

$$Z_i = h_{ic} + A_i h_{oc} R_c$$

$$A_V = \frac{A_i}{Z_i} R_L$$

$$Y_0 = h_{oc} = \frac{h_{fe} h_{rc}}{R_s + h_{ic}}$$

Approx

$$A_i = -h_{fe} = 1+h_{fe}$$

$$Z_i = h_{ie} + (1+h_{fe}) R_L$$

$$A_V = \frac{(1+h_{fe}) R_L}{h_{ie} + (1+h_{fe}) R_L} \approx 1$$

$$Y_0 = \frac{1+h_{fe}}{R_s + h_{ie}}$$