Ex. 9.10 : *Design a MOD-5 synchronous counter using JK flip-flops and implement it. Also construct a timing diagram.*

Sol. : Flip-flops required are

$$2^n \geq N$$

Here $N = 5$

$\therefore$ $n = 3$

i.e. three flip-flops are required.

Excitation table for JK

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Table 9.25

State table

Present State			Next State			Flip-flop Inputs					
Q_C	Q_B	Q_A	Q_{c+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X

K-map Simplification

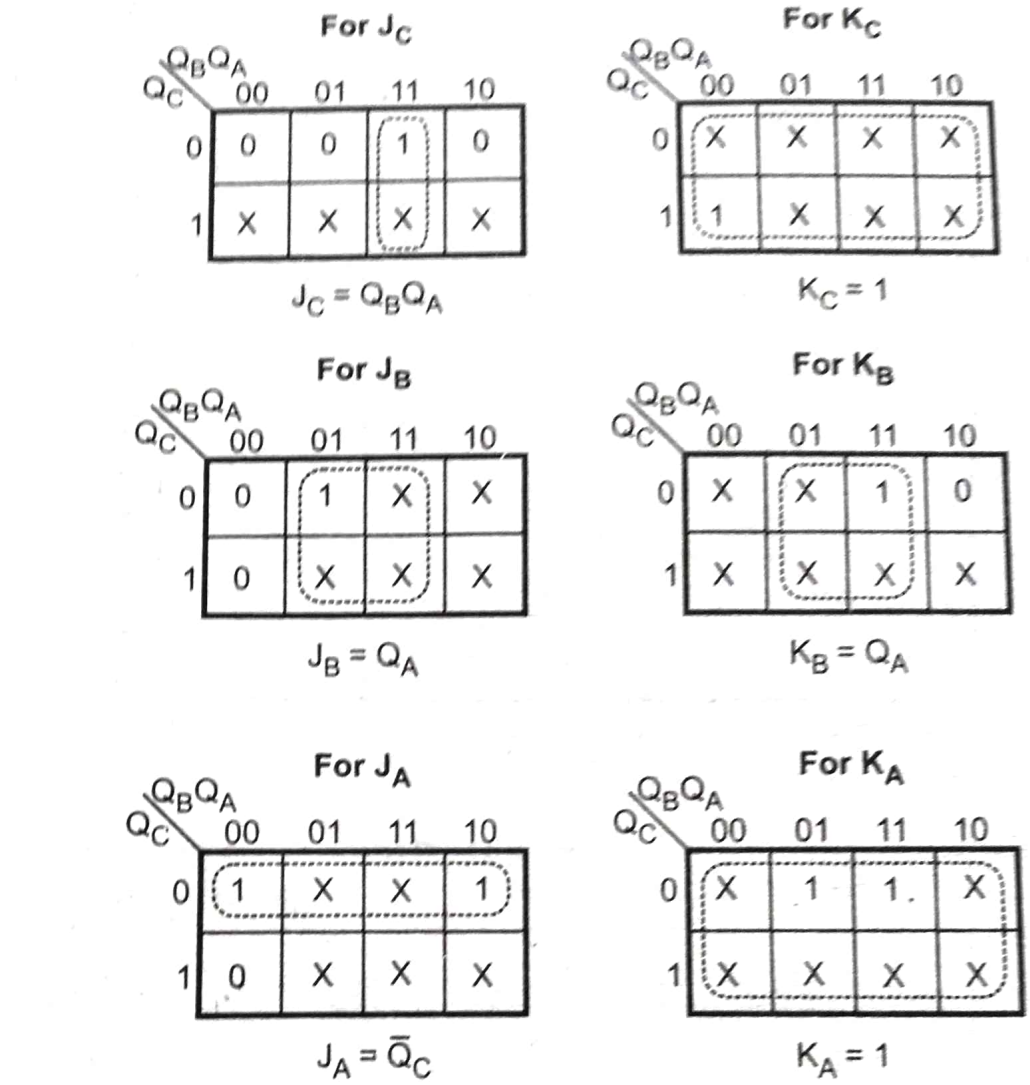
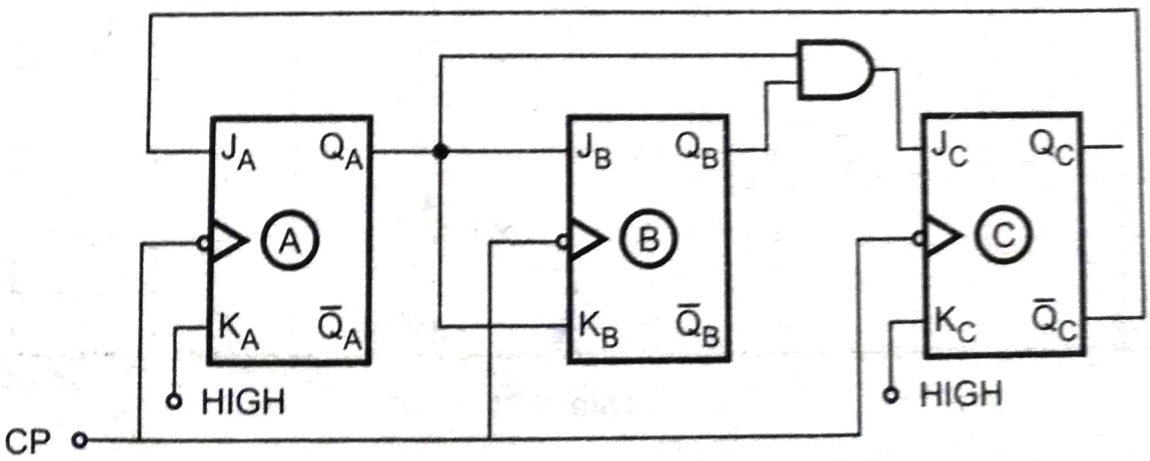


Fig. 9.75

Logic Diagram



Timing Diagram

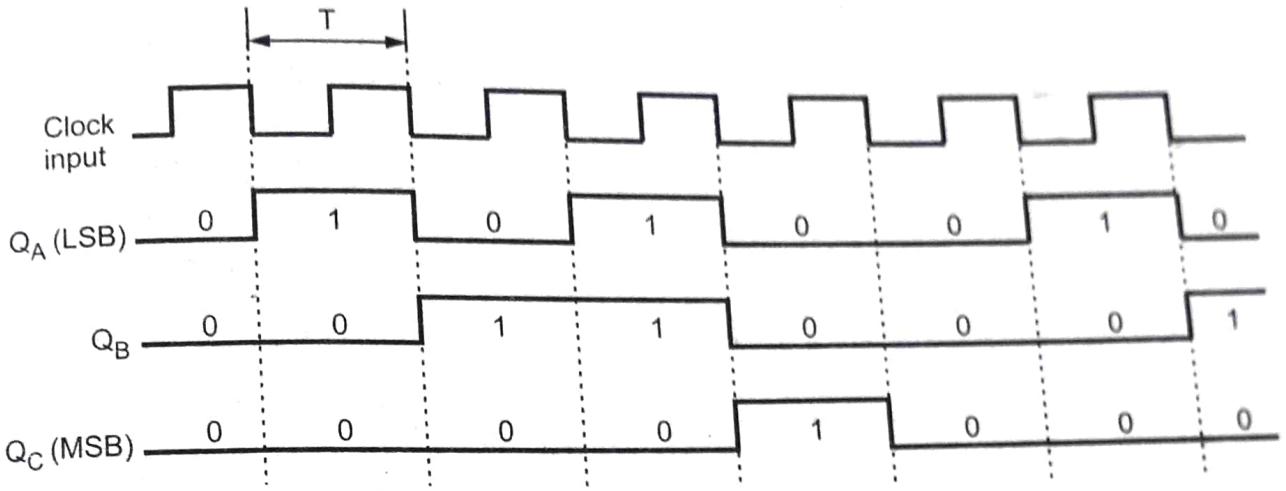


Fig. 9.77 Timing diagram

Ex. 9.11 : *Design divide by 6 counter using T-flip-flop. Write state table and reduce the expression using K-map.*

Sol. : For designing mod 6 counter using the formula

$$2^n \geq N$$

Here $N = 6$

$\therefore$ $n = 3$ i.e. 3 flip-flops are required.

Excitation table for T-flip-flop

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Table 9.27

State Table

CP	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_C	T_B	T_A
0	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
2	0	1	0	0	1	1	0	0	1
3	0	1	1	1	0	0	1	1	1
4	1	0	0	1	0	1	0	0	1
5	1	0	1	0	0	0	1	0	1

Table 9.28

K-map Simplification

For T_C

Q_C \ Q_BQ_A	00	01	11	10
0	0	0	1	0
1	0	1	X	X

$T_C = Q_CQ_A + Q_BQ_A$

For T_B

Q_C \ Q_BQ_A	00	01	11	10
0	0	1	1	0
1	0	0	X	X

$T_B = \overline{Q}_CQ_A$

For T_A

Q_C \ Q_BQ_A	00	01	11	10
0	1	1	1	1
1	1	1	X	X

$T_A = 1$

Logic Diagram

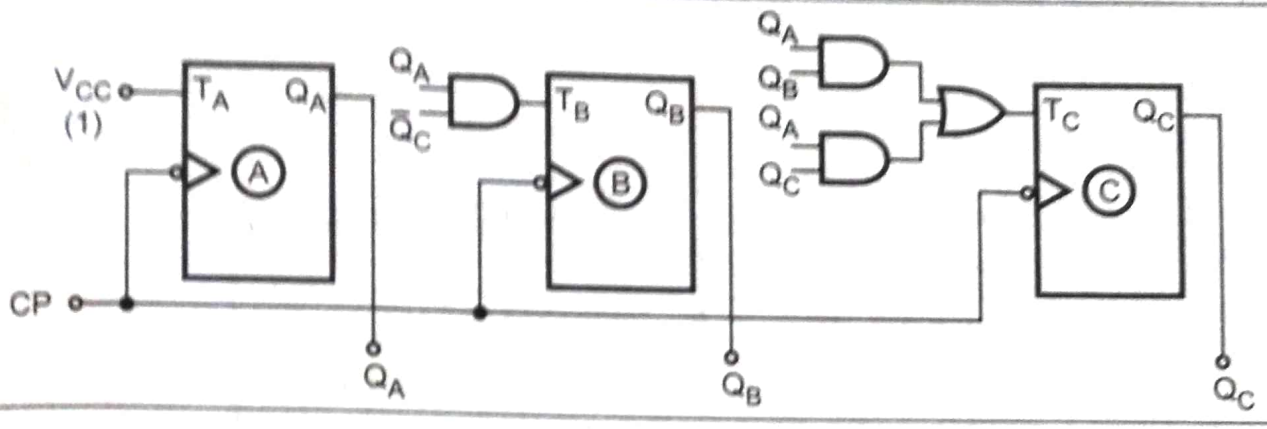


Fig. 9.79

Synchronous Decade Counter

We know that in the decade counters we have to truncate normal counter sequence. Therefore, it is also called MOD-10 counter. Let us design the synchronous decade counter. Here, we will not use clear input to reset the counter after state 1010. Table 9.29 shows the excitation table for synchronous decade counter using T flip-flops.

Excitation Table

Present State				Next State				Flip-flop Inputs			
Q_D	Q_C	Q_B	Q_A	Q_{D+1}	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_D	T_C	T_B	T_A
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1
1	0	1	0	X	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X	X

K-map Simplification

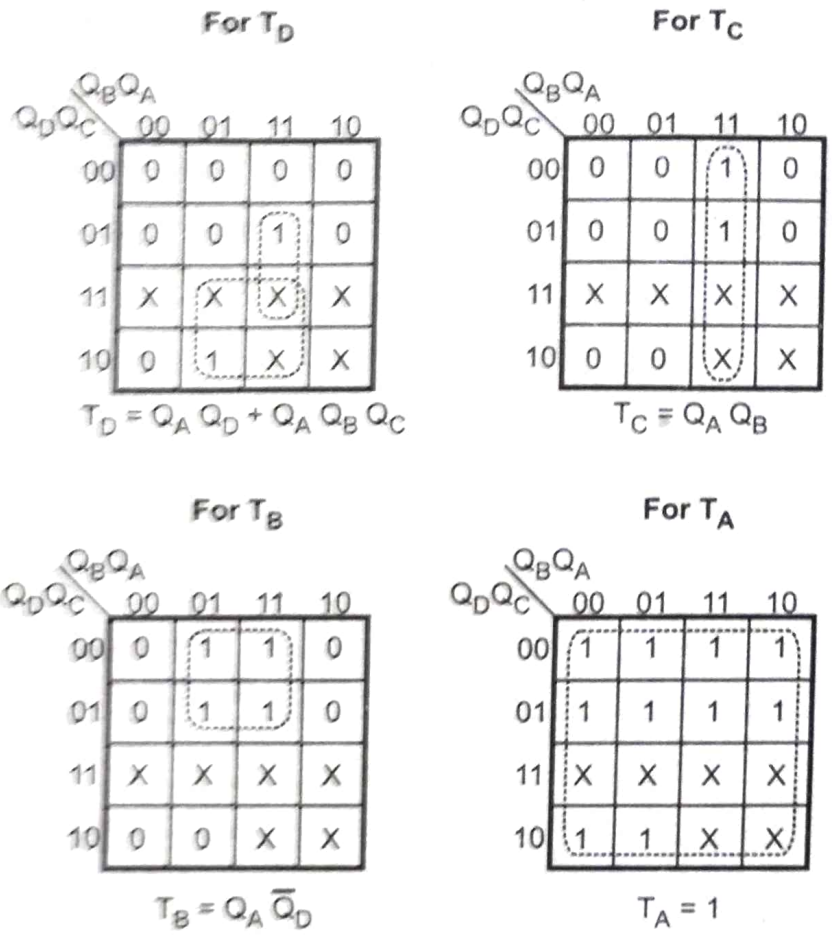
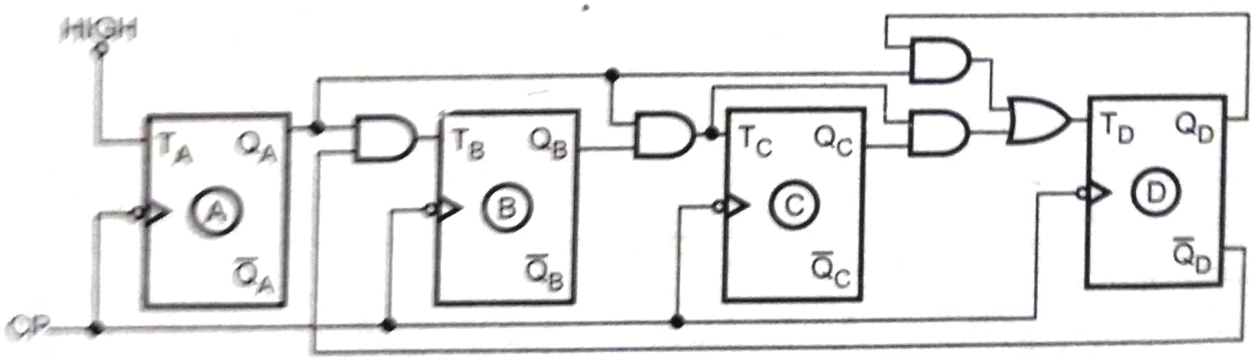


Fig. 9.80

Logic Diagram



An up/down counter is one that is capable of progressing in increasing order or decreasing order through a certain sequence. An up/down counter is also called bidirectional counter. Usually up/down operation of the counter is controlled by UP/$\overline{\text{DOWN}}$ signal. When this signal is HIGH, counter goes through UP sequence, i.e. 0, 1, 2, 3, ..., n. When UP/$\overline{\text{DOWN}}$ signal is LOW counter follows reverse sequence i.e. n, n-1, n-2,....., 1, 0. For 3-bit counters these sequences are : 0, 1, 2, 3, 4, 5, 6, 7 for up operation and 7, 6, 5, 4, 3, 2, 1, 0 for DOWN operation. This is illustrated in Table9.31. The arrows in the Table 9.31 indicate the state-to-state movement of the counter for both its UP and its DOWN modes of operation.

State Table

CP	UP	Q_C	Q_B	Q_A	DOWN
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

Table 9.31

Let us design the 3-bit UP/ $\overline{\text{DOWN}}$ synchronous counter, using T flip-flops. Table 9.32 shows the excitation table for 3-bit UP/ $\overline{\text{DOWN}}$ synchronous counter.

Excitation Table

Input	Present State			Next State			Flip-flop Inputs		
UP/$\overline{\text{DOWN}}$ (UD)	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_C	T_B	T_A
0	0	0	0	1	1	1	1	1	1
0	0	0	1	0	0	0	0	0	1
0	0	1	0	0	0	1	0	1	1
0	0	1	1	0	1	0	0	0	1
0	1	0	0	0	1	1	1	1	1
0	1	0	1	1	0	0	0	0	1
0	1	1	0	1	0	1	0	1	1

0	1	1	1	1	1	0	0	0	1
1	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
1	0	1	0	0	1	1	0	0	1
1	0	1	1	1	0	0	1	1	1
1	1	0	0	1	0	1	0	0	1
1	1	0	1	1	1	0	0	1	1
1	1	1	0	1	1	1	0	0	1
1	1	1	1	0	0	0	1	1	1

Table 9.32

K-Map Simplification

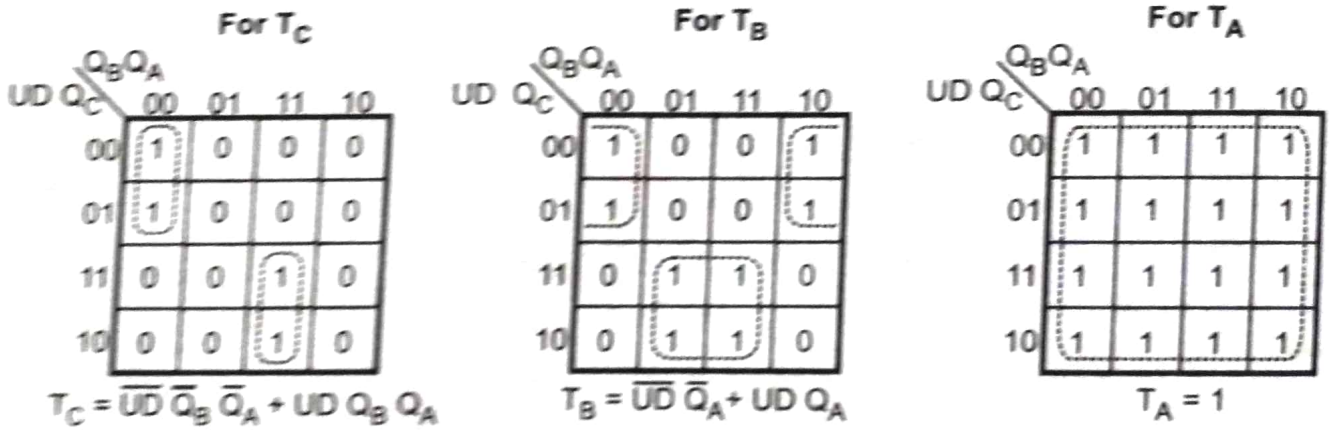
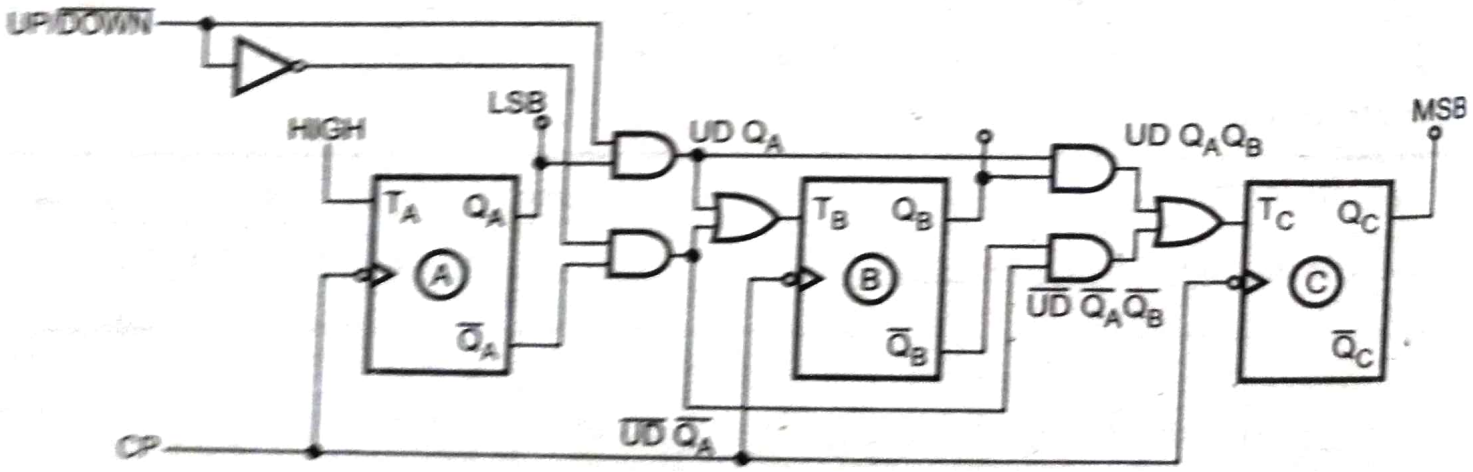


Fig. 9.87

Logic Diagram



Design a synchronous mod-6 gray code counter using T flip flops.

$2^n \geq N$

$2^3 \geq 6$

Decimal	present state Q_2	Q_1	Q_0	Next state Q_{2+1}	Q_{1+1}	Q_{0+1}	Excitation i/ps of T_2	T_1	T_0
0	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	1	0	1	0
3	0	1	1	0	1	0	0	0	1
2	0	1	0	1	1	0	1	0	0
6	1	1	0	1	1	1	0	0	1
7	1	1	1	0	0	0	1	1	1

101, 100 states are invalid i.e dont cares

for T_2

Q_2 \ Q_1Q_0	00	01	11	10
0	0	0	0	1
1	X	X	1	0

$T_2 = Q_2 \bar{Q}_0 + \bar{Q}_2 Q_1 \bar{Q}_0$

for T_1

Q_2 \ Q_1Q_0	00	01	11	10
0	0	1	0	0
1	X	X	1	0

$T_1 = Q_2 Q_0 + \bar{Q}_1 Q_0$

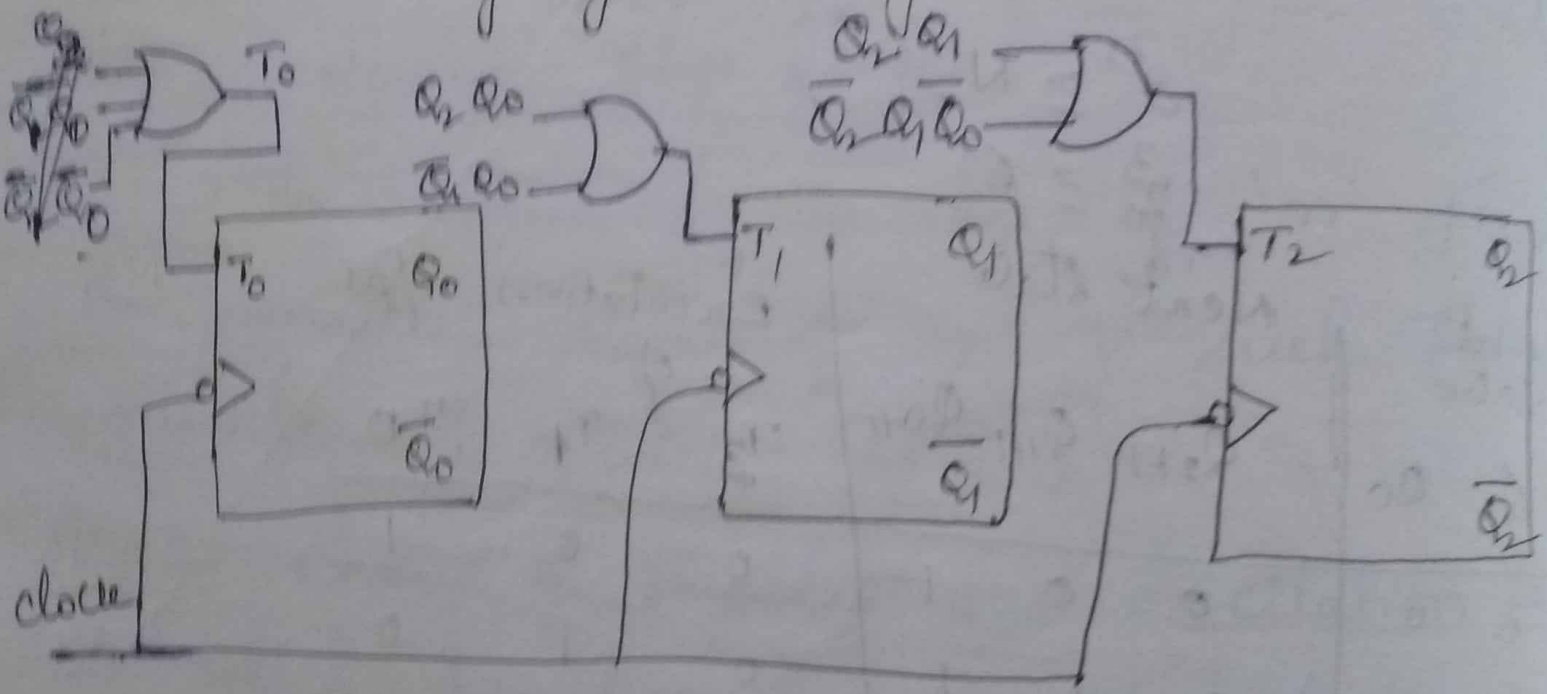
for T_0

Q_2 \ Q_1Q_0	00	01	11	10
0	1	0	1	0
1	X	X	1	1

$T_0 = Q_2 + \bar{Q}_1 \bar{Q}_0 + Q_1 Q_0$

$Q_2 + Q_1 \odot Q_0$

Mod - 6 gray code synchronous counter



Parity bit generator

odd parity bit generator

a	b	c	Parity bit (odd)
0	0	0	1

Ex. 9.37 : *Design a 4-bit counter that counts either in binary or BCD depending on control line MODE. When MODE = 0, the counter is to count in binary, and when MODE = 1, the counter is to count in BCD. Select any flip-flops for implementation. Draw the logic diagram for realization.*

Sol. : Table 9.40 shows the excitation table for BCD/Binary counter.

Input	Present State				Next State				Flip-flop Inputs							
M	Q_A	Q_B	Q_C	Q_D	Q_{A+1}	Q_{B+1}	Q_{C+1}	Q_{D+1}	J_A	K_A	J_B	K_B	J_C	K_C	J_D	K_D
0	0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
0	1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
0	1	0	0	1	1	0	1	0	X	0	0	X	1	X	X	1
0	1	0	1	0	1	0	1	1	X	0	0	X	X	0	1	X
0	1	0	1	1	1	1	0	0	X	0	1	X	X	1	X	1
0	1	1	0	0	1	1	0	1	X	0	X	0	0	X	1	X
0	1	1	0	1	1	1	1	0	X	0	X	0	1	X	X	1
0	1	1	1	0	1	1	1	1	X	0	X	0	X	0	1	X
0	1	1	1	1	0	0	0	0	X	1	X	1	X	1	X	1
1	0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
1	0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
1	0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
1	0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
1	0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
1	0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
1	0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
1	0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	1	0	0	1	0	0	0	0	X	1	0	X	0	X	X	1

Table 9.40

For J_A

M = 0

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

M = 1

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

$J_A = Q_B Q_C Q_D$

For K_A

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	0	1	0
10	0	0	0	0

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10	0	1	X	X

$K_A = Q_B Q_C Q_D + Q_D M$

For J_B

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	0	0	1	0
01	X	X	X	X
11	X	X	X	X
10	0	0	1	0

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	0	0	1	0
01	X	X	X	X
11	X	X	X	X
10	0	0	X	X

$J_B = Q_C Q_D$

For K_B

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	X	X	X
01	0	0	1	0
11	0	0	1	0
10	X	X	X	X

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	X	X	X
01	0	0	1	0
11	X	X	X	X
10	X	X	X	X

$K_B = Q_C Q_D$

For J_C

M = 0

$Q_A Q_B$ \ $Q_C Q_D$	00	01	11	10
00	0	1	X	X
01	0	1	X	X
11	0	1	X	X
10	0	1	X	X

M = 1

$Q_A Q_B$ \ $Q_C Q_D$	00	01	11	10
00	0	1	X	X
01	0	1	X	X
11	X	X	X	X
10	0	0	X	X

$$J_C = Q_D\overline{M} + \overline{Q_A}\,Q_D$$

For K_C

$Q_A Q_B$ \ $Q_C Q_D$	00	01	11	10
00	X	X	1	0
01	X	X	1	0
11	X	X	1	0
10	X	X	1	0

$Q_A Q_B$ \ $Q_C Q_D$	00	01	11	10
00	X	X	1	0
01	X	X	1	0
11	X	X	X	X
10	X	X	X	X

$$K_C = Q_D$$

For J_D

$Q_A Q_B$ \ $Q_C Q_D$	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	1	X	X	1
10	1	X	X	1

$Q_A Q_B$ \ $Q_C Q_D$	00	01	11	10
00	1	X	X	1
01	1	X	X	1
11	X	X	X	X
10	1	X	X	X

$$J_D = 1$$

For K_D

$Q_A Q_B$ \ $Q_C Q_D$	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	1	1	X
10	X	1	1	X

$Q_A Q_B$ \ $Q_C Q_D$	00	01	11	10
00	X	1	1	X
01	X	1	1	X
11	X	X	X	X
10	X	1	X	X

$$K_D = 1$$

Logic Diagram

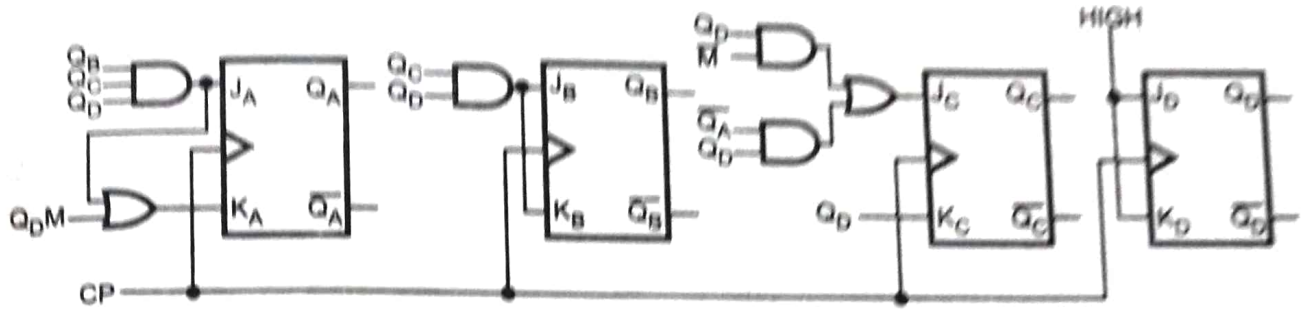


Fig. 9.103

Ex. 9.38 : *Design a synchronous Gray code up counter. Derive the expressions for the inputs of JK flip-flops.*

Sol. : Table 9.41 shows the excitation table for synchronous Gray code up counter.

Present State				Next State				Flip-flop Inputs							
Q_A	Q_B	Q_C	Q_D	Q_{A+1}	Q_{B+1}	Q_{C+1}	Q_{D+1}	J_A	K_A	J_B	K_B	J_C	K_C	J_D	J_D
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	1	0	X	0	X	1	X	X	0
0	0	1	0	0	1	1	0	0	X	1	X	X	0	0	X
0	0	1	1	0	1	1	0	0	X	0	X	X	0	X	1
0	1	0	0	1	1	0	0	1	X	X	0	0	X	0	X
0	1	0	1	0	1	0	0	0	X	X	0	0	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	0	1	0	1	0	X	X	0	X	1	X	0
1	0	0	0	0	0	0	0	X	1	0	X	0	X	0	X
1	0	0	1	1	0	0	0	X	0	0	X	0	X	X	1
1	0	1	0	1	0	1	1	X	0	0	X	X	0	1	X
1	0	1	1	1	0	0	1	X	0	0	X	X	1	X	0
1	1	0	0	1	1	0	1	X	0	X	0	0	X	1	X
1	1	0	1	1	1	1	1	X	0	X	0	1	X	X	0
1	1	1	0	1	0	1	0	X	0	X	1	X	0	0	X
1	1	1	1	1	1	1	0	X	0	X	0	X	0	X	1

Table 9.41

K-Map Simplification

For J_A

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	X	X	X	X
10	X	X	X	X

$J_A = Q_B \overline{Q_C}\,\overline{Q_D}$

For K_A

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	0	0	0	0
10	1	0	0	0

$K_A = \overline{Q_B}\,\overline{Q_C}\,\overline{Q_D}$

For J_B

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	0	0	0	1
01	X	X	X	X
11	X	X	X	X
10	0	0	0	0

$J_B = \overline{Q_A}\,Q_C\,\overline{Q_D}$

For K_B

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	X	X	X
01	0	0	0	0
11	0	0	0	1
10	X	X	X	X

$K_B = Q_A\,\overline{Q_C}\,Q_D$

For J_C

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	0	1	X	X
01	0	0	X	X
11	0	1	X	X
10	0	0	X	X

$J_C = \overline{Q_A}\,\overline{Q_B}Q_D + Q_AQ_BQ_D$

For K_C

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	X	0	0
01	X	X	1	0
11	X	X	0	0
10	X	X	1	0

$K_C = \overline{Q_A}Q_BQ_D + Q_A\overline{Q_B}Q_D$

For J_D

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	1	X	X	0
01	0	X	X	1
11	1	X	X	0
10	0	X	X	1

$J_D = \overline{Q_A}\,\overline{Q_B}\,\overline{Q_C} + Q_AQ_B\overline{Q_C} + \overline{Q_A}Q_BQ_C + Q_A\overline{Q_B}Q_C$

For K_D

Q_AQ_B \ Q_CQ_D	00	01	11	10
00	X	0	1	X
01	X	1	0	X
11	X	0	1	X
10	X	1	0	X

$K_D = \overline{Q_A}\,\overline{Q_B}Q_C + Q_AQ_BQ_C + \overline{Q_A}Q_B\overline{Q_C} + Q$

Fig. 9.104