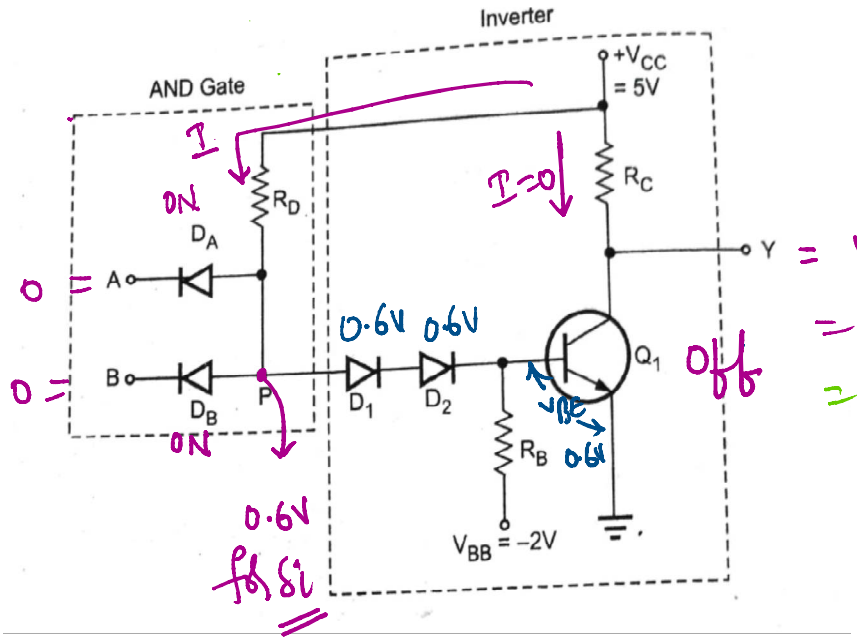
DTL Logic family



To switch ON Q_1 we need 1.8V

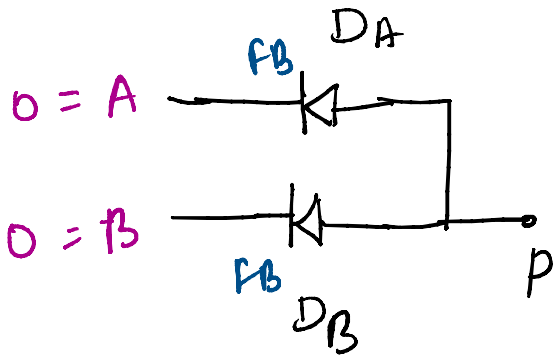
$Y = V_{cc} - I R_c$

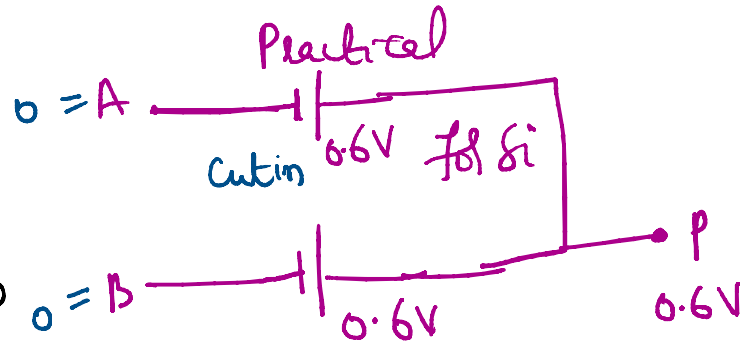
$= 5V - 0$

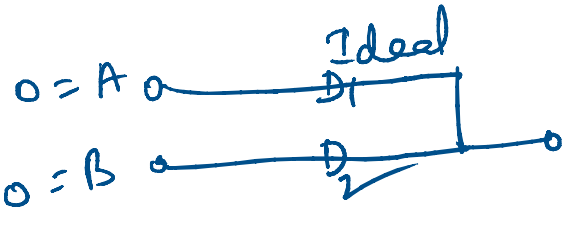
$= 5V$

$0.6V + 0.6V + 0.6$

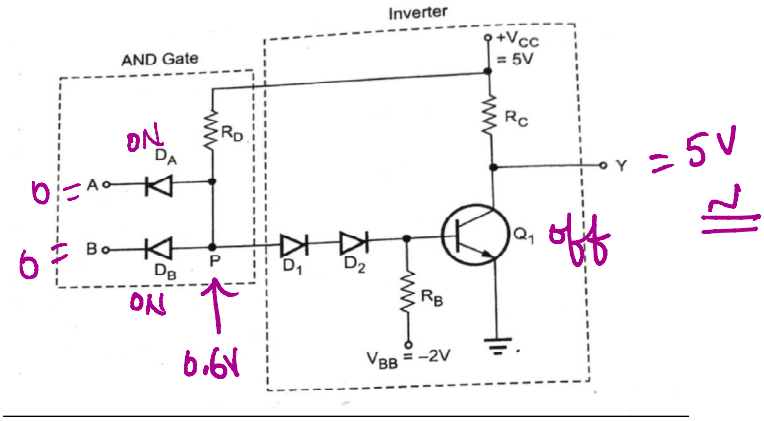
$1.2 + 0.6 \Rightarrow 1.8V$

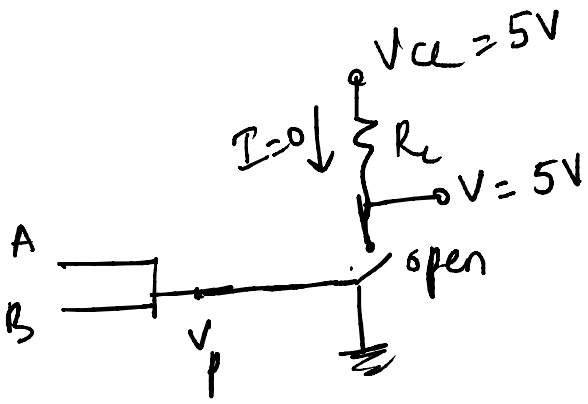


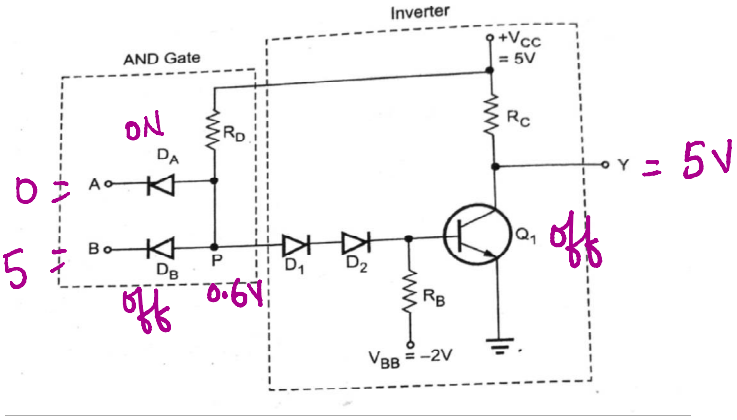


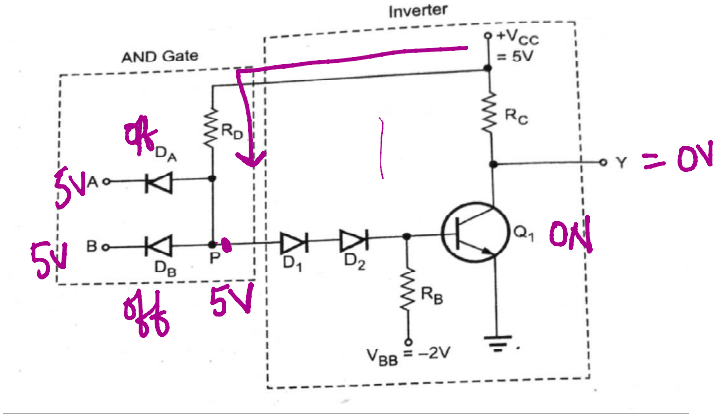


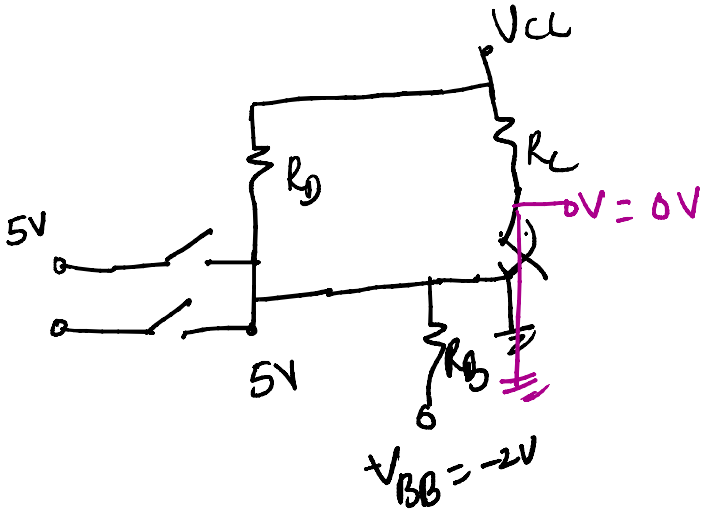
$V_p = 0V$


Inverter
AND Gate
+VCC = 5V
RC
RD
ON
DA
A
0
B
0
DB
P
D1
D2
Q1
off
RB
ON
0.6V
VBB = −2V
Y = 5V


Vcc = 5V
I = 0
RL
V = 5V
A
B
open
V

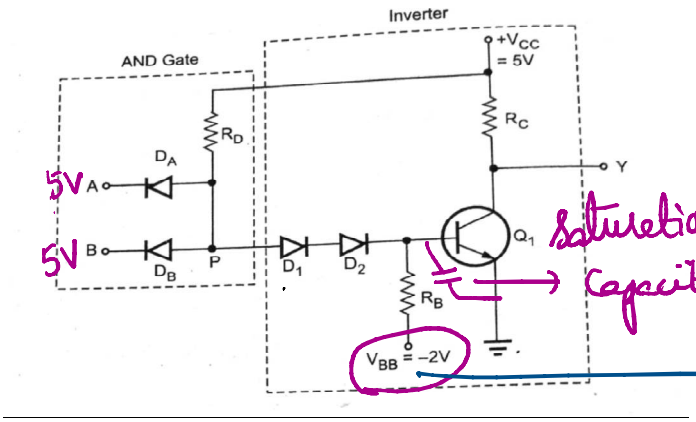

Inverter
AND Gate
+VCC = 5V
RC
RD
ON
DA
A
0
B
5
DB
P
D1
D2
Q1
off
RB
off
0.6V
VBB = −2V
Y = 5V


Inverter
AND Gate
+VCC = 5V
RC
RD
off
DA
5V
A
5V
B
DB
P
D1
D2
Q1
ON
RB
off
5V
VBB = −2V
Y = 0V


Vcc
RD
RL
5V
V = 0V
5V
RB
VBB = −2V

A	B	Y
0	0	5V
0	5	5V
5	0	5V
5	5	0

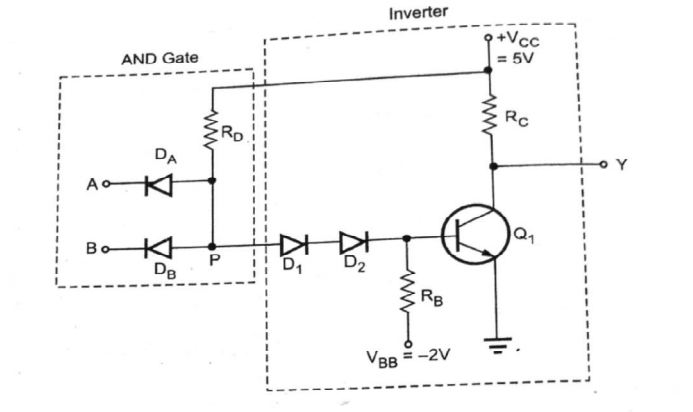
$\equiv$ NAND gate ✓



saturation → capacitor charges

D_1 & D_2 diodes improves noise margin

provides path for discharge capacitor



7.4.3 Specifications

Table 7.4 gives the specifications for DTL gate

Parameter	Value
Power dissipation	60 mW
Propagation Delay	30 nsec.
Noise Margin	0.7 volts
Fan out	8

Table 7.4 Specification for DTL gate

From the above specifi...

7.4.4 Wire-AND connection

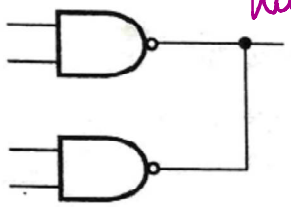


Fig. 7.8 Wired AND DTL NAND gates