NOR-SR latch

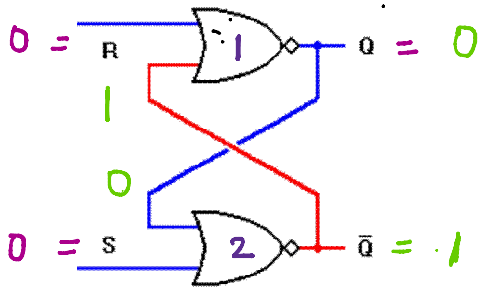
1. Non clocked flip flops.
2. They are not dependent on clock signal for their operation
3. Latch is a sequential device that checks all its inputs continuously and changes its outputs accordingly at any time independent of clock signal.

NOR gate truth table

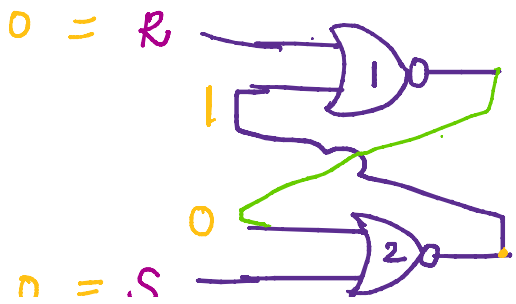
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Q = P.S ⇒ Present state

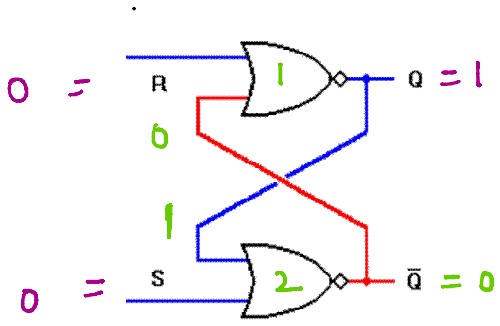
Q_{t+1} = N.S = Next state



S	R	Q	Q_{t+1}	State
0	0	0	0	No change state
0	0	1	1	

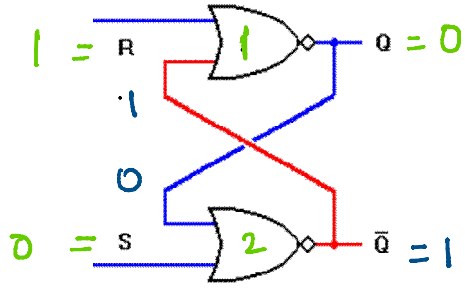


S	R	P.S Q	N.S $Q_{(t+1)}$
0	0	0	0

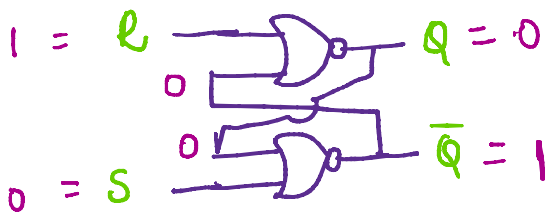


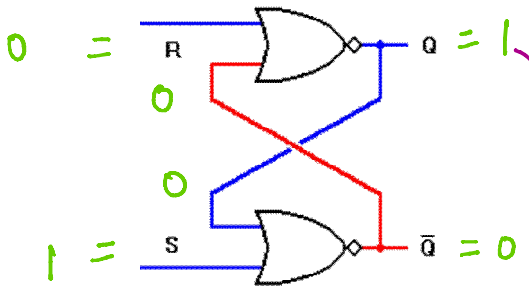
		P.S	N.S	
S	R	Q	Q_{t+1}	
0	0	1	1	

		P.S	N.S	
S	R	Q	Q_{t+1}	
0	0	0	0	} No change state
0	0	1	1	

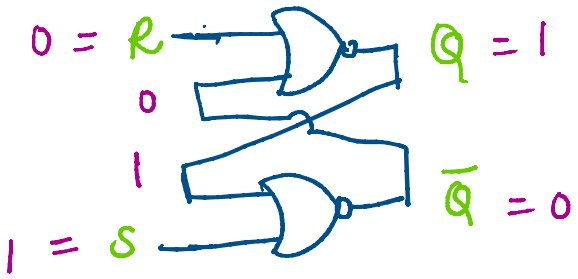


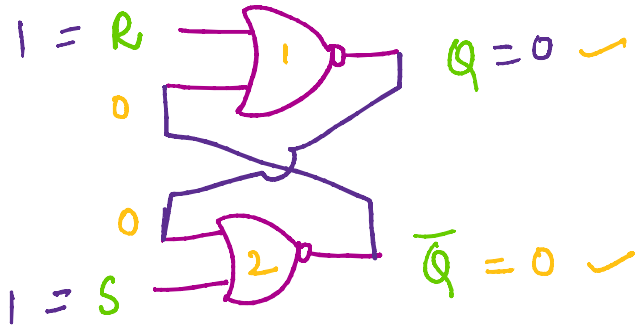
S	R	P.S Q	N.S Q_{t+1}	State
0	1	0	0	} Reset state
0	1	1	0	



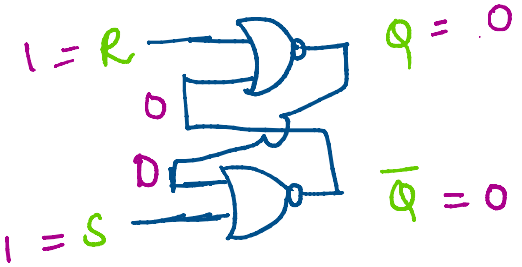


S	R	P.S Q	N.S Q_{t+1}	State
1	0	0	1	Set
1	0	1	1	



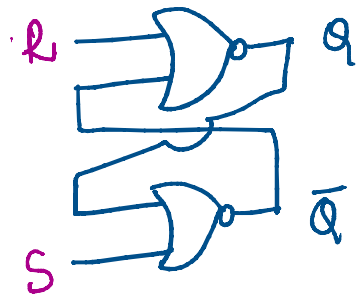


S	R	Q	Q_{t+1}	State
1	1	0	X	Not used
1	1	1	X	



NOR gate S-R latch (or) Active high S-R latch

NOR gate S-R latch



Truth table

S	R	P.S Q	N.S O/P Q(t+1)	State
0	0	0	0	No change
0	0	1	1	
0	1	0	0	Reset state
0	1	1	0	
1	0	0	1	Set state
1	0	1	1	
1	1	0	x	Not used
1	1	1	x	