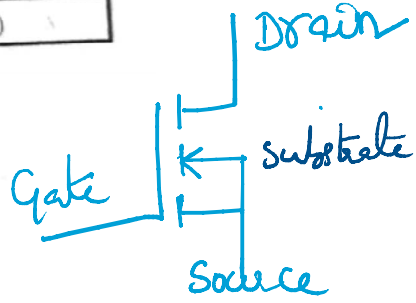
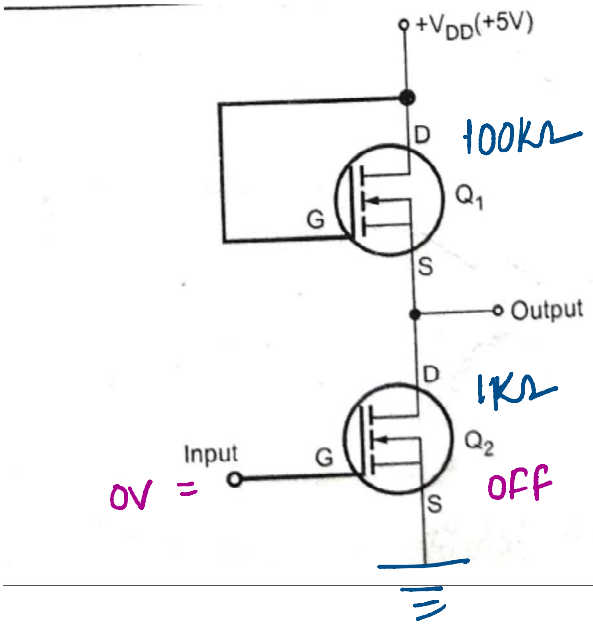
NMOS Logic Family

V_{GS}	NMOS
0V	OFF
5V	ON

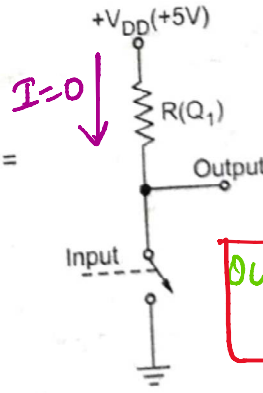
Table 6.9 summarizes the operation of NMOS inverter

V_{IN} (VGS)	Q_2	$V_0 = \overline{V_{IN}}$
0 V (logic 0)	OFF	+ 5 V (logic 1)
5 V (logic 1)	ON	0 V (logic 0)



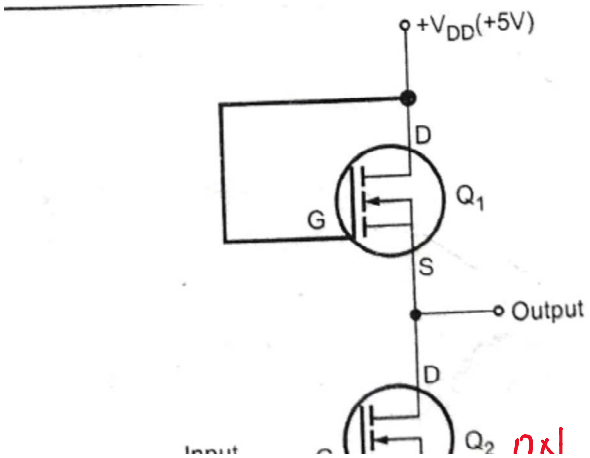


=

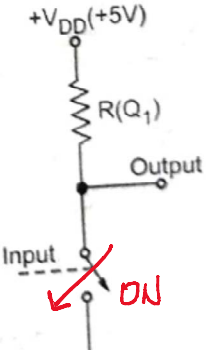


$= V_{DD} - I_D R$ ($I_D R \approx 0$)

Output $= V_{DD}$



=

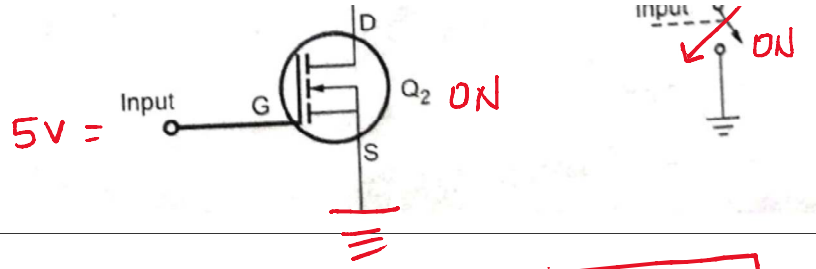


$V_{DD} \cong I R$

output $= V_{DD} - I R$

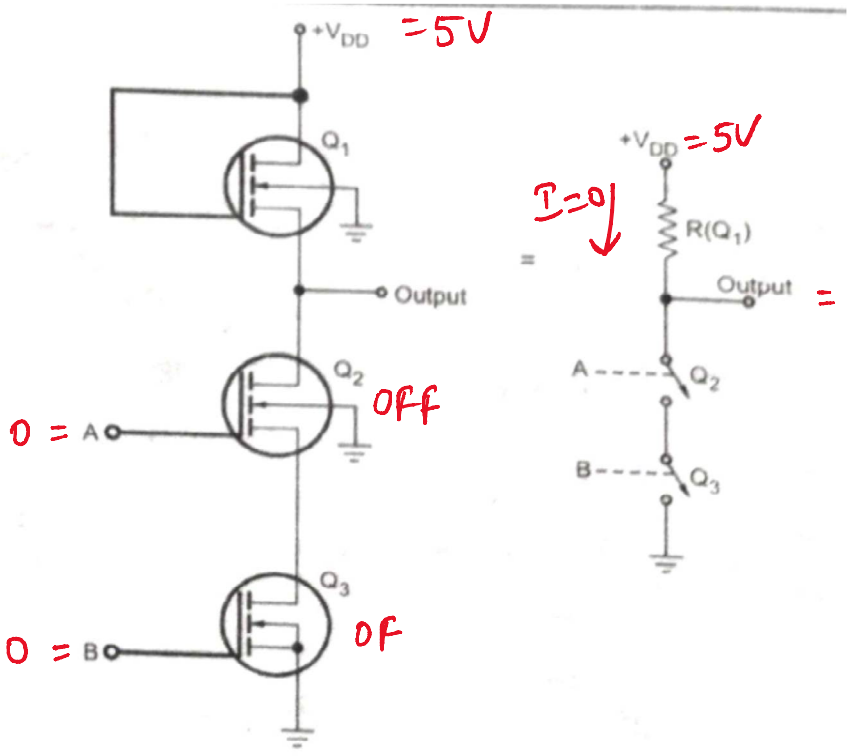
$= 0V$

$= 0V$



Input	output
0V	5V
5V	0V

≅ NOT gate

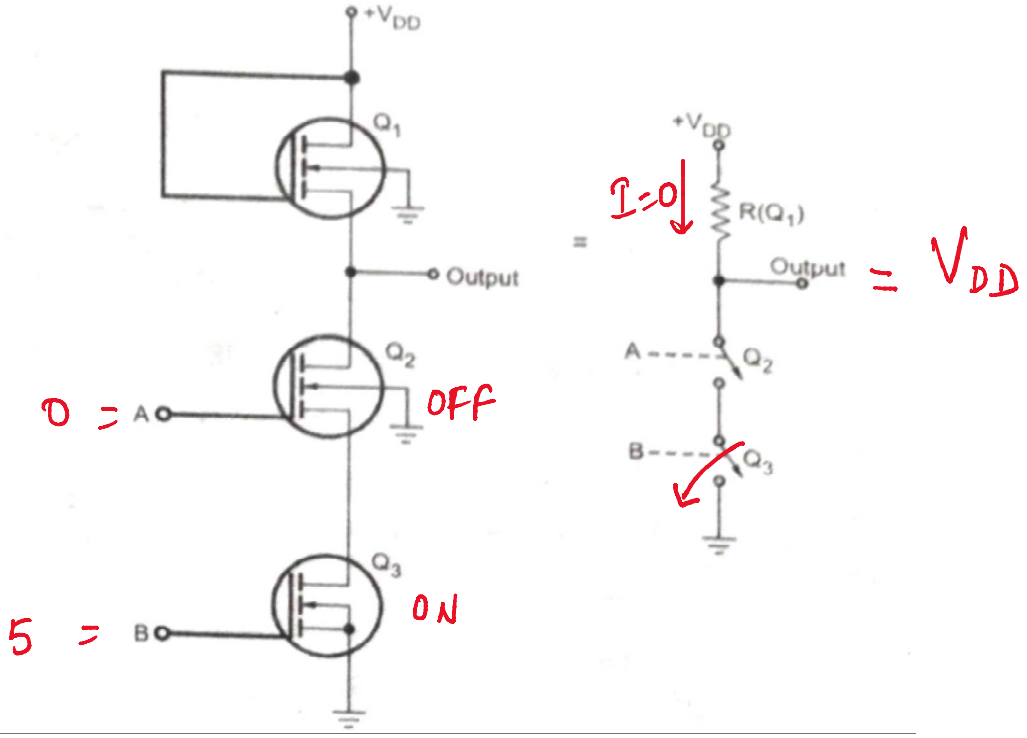


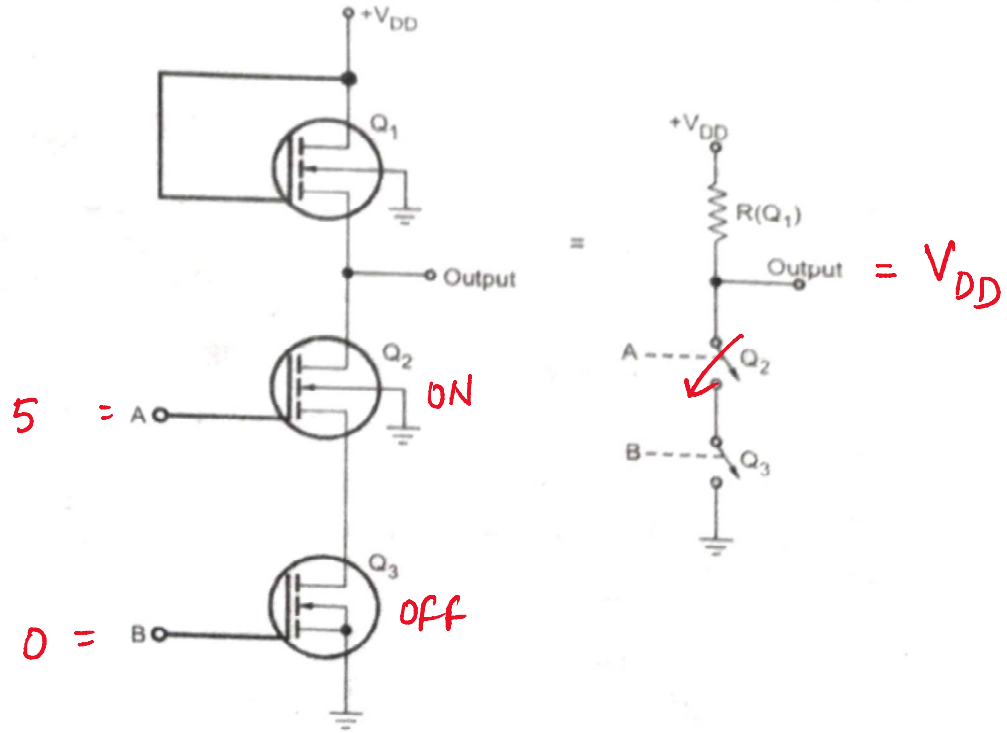
I=0

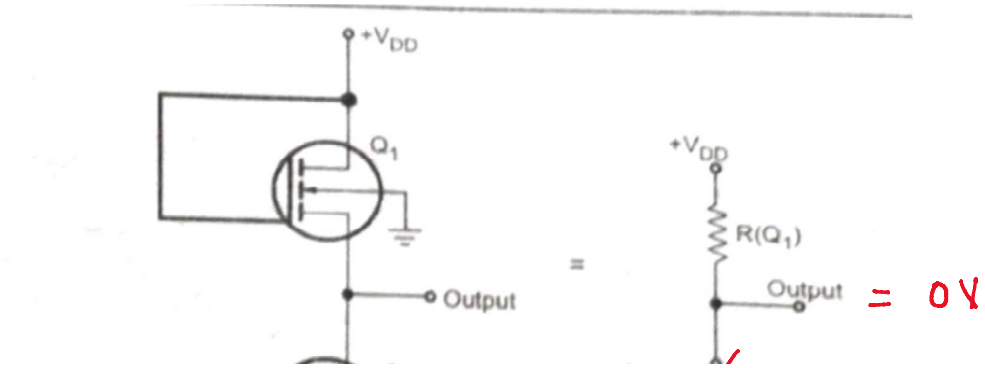
output = V_{DD} − I R

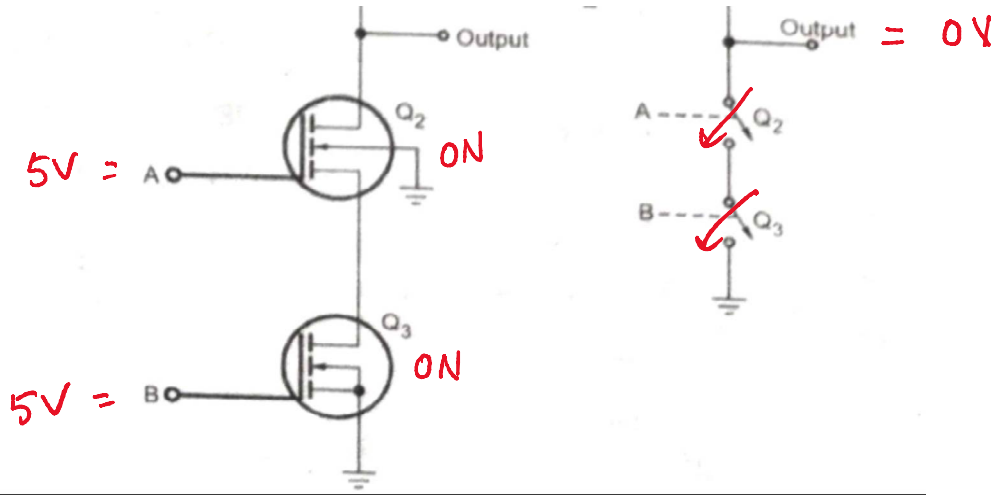
output = V_{DD}

= V_{DD} = 5V


+V_DD
Q1
Output
Q2
0 = A
OFF
Q3
5 = B
ON
=
+V_DD
I=0
R(Q1)
Output
= V_DD
A
Q2
B
Q3


+V_DD
Q1
Output
Q2
5 = A
ON
Q3
0 = B
off
=
+V_DD
R(Q1)
Output
= V_DD
A
Q2
B
Q3


+V_DD
Q1
Output
=
+V_DD
R(Q1)
Output
= 0 V



A	B	output
0	0	5V
0	5	5V
5	0	5V
5	5	0V

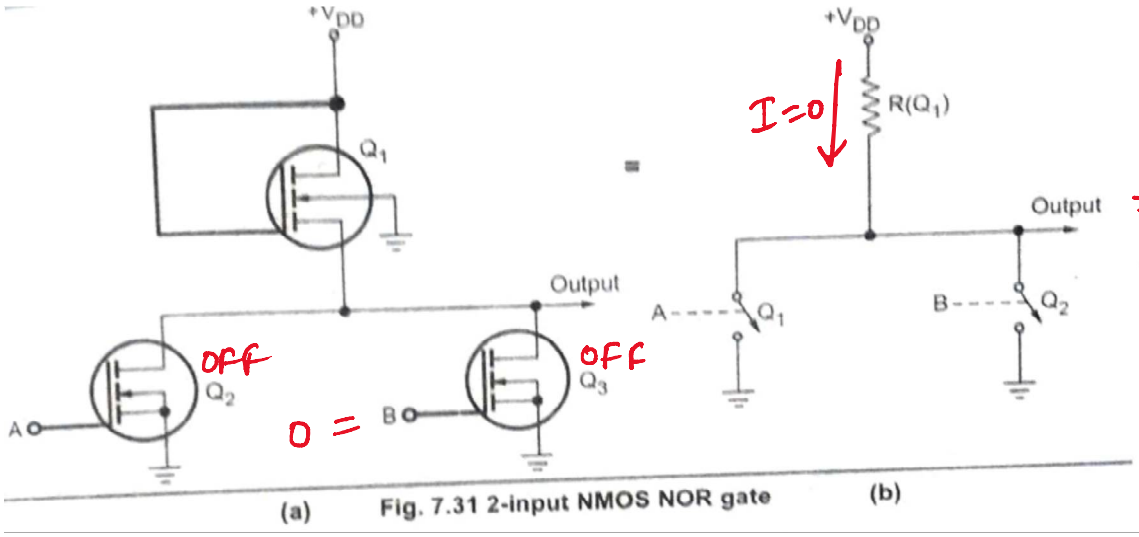
≅ NAND

Table 7.11 summarizes the operation of NMOS NAND gate

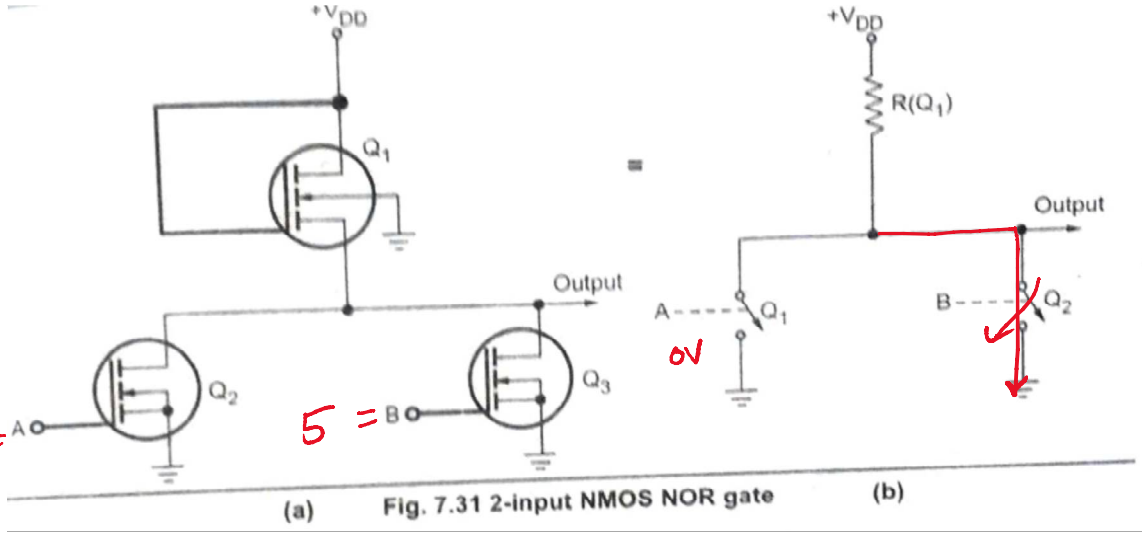
A	B	Q_2	Q_3	$V_0 = \overline{AB}$
0	0	OFF	OFF	1
0	1	OFF	ON	1
1	0	ON	OFF	1
1	1	ON	ON	0

Table 7.11

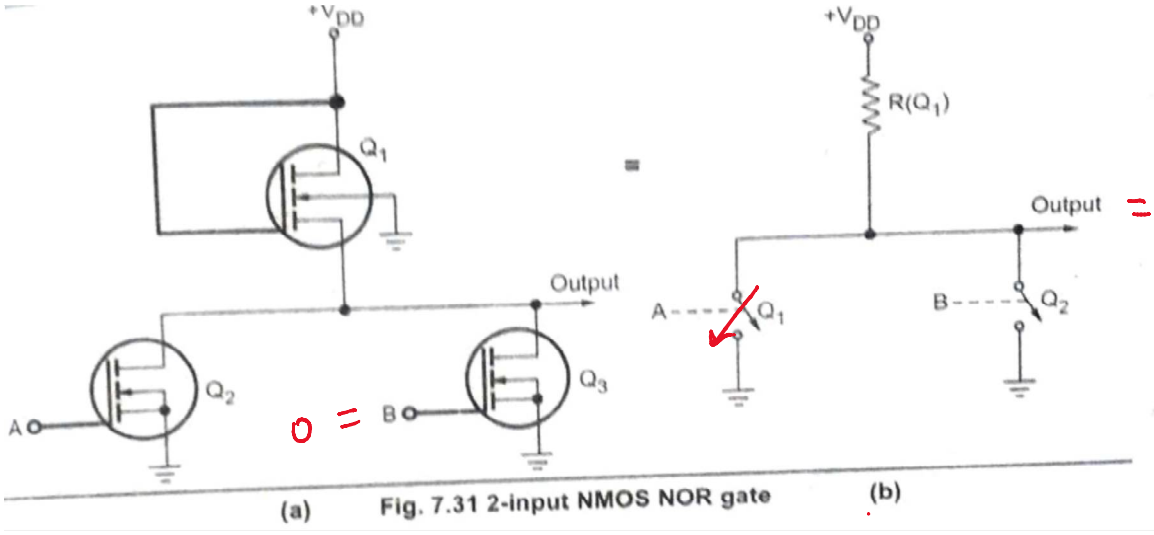
NMOS NOR GATE



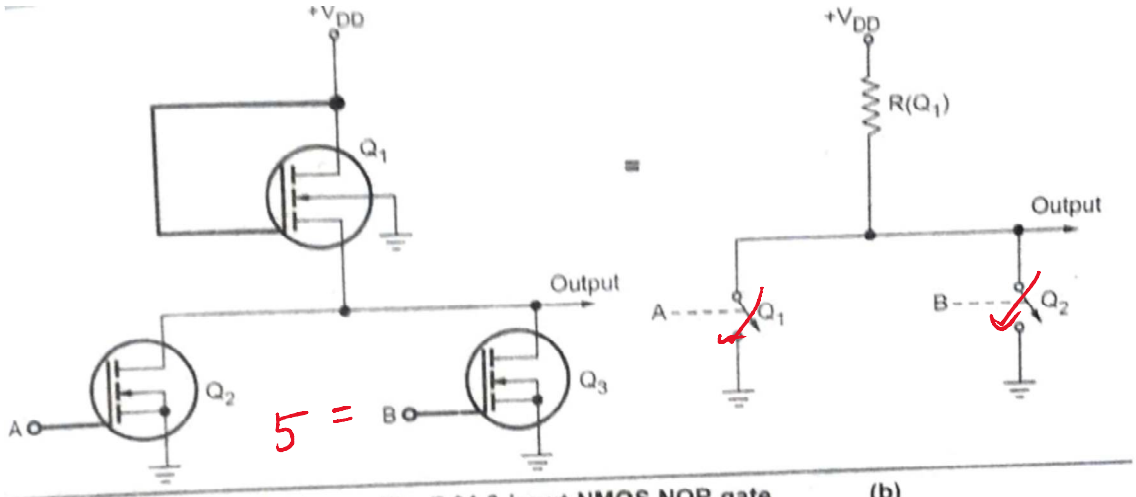
(a) Fig. 7.31 2-input NMOS NOR gate (b)



(a) Fig. 7.31 2-input NMOS NOR gate (b)



(a) Fig. 7.31 2-input NMOS NOR gate (b)



(a) Fig. 7.31 2-input NMOS NOR gate (b)

5 = A

5 = B

= 0 V

A	B	output
0	0	5V
0	5	0
5	0	0
5	5	0

≅ NOR gate

Table 7.12 summarizes the operation of NMOS NOR gate.

A	B	Q_2	Q_1	$V_0 = \overline{A + B}$
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	ON	0

Table 7.12

Characteristics of NMOS

Operating speed : Low operating speed with propagation delay time around 50ns. This is because it has high output resistance, very high input resistance and reasonably high input capacitance.

Noise Margin : Typically 1.5 V

Fan out : Typically 30

Power drain : Less, around 0.1 mW per gate.