JK Flip Flop

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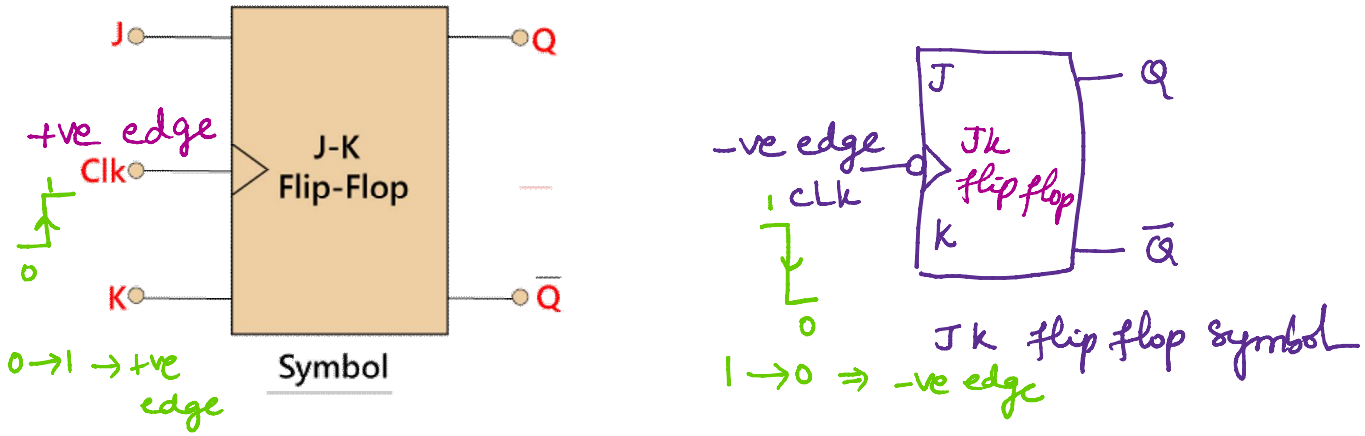
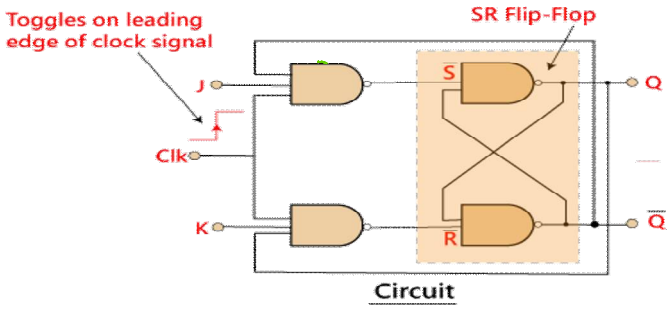
The JK Flip Flop removes these two drawbacks of SR Flip Flop.
The JK flip flop is one of the most used flip flops in digital circuits. The JK flip flop is a universal flip flop having two inputs 'J' and 'K'.

The JK flip flop work in the same way as the SR flip flop work. The JK flip flop has 'J' and 'K' flip flop instead of 'S' and 'R'. The only difference between JK flip flop and SR flip flop is that when both inputs of SR flip flop is set to 1, the circuit produces the invalid states as outputs, but in case of JK flip flop, there are no invalid states even if both 'J' and 'K' flip flops are set to 1.
The JK Flip Flop is a gated SR flip-flop having the addition of a clock input circuitry. The invalid or illegal output condition occurs when both of the inputs are set to 1 and are prevented by the addition of a clock input circuit. So, the JK flip-flop has four possible input combinations, i.e., 1, 0, "no change" and "toggle". The symbol of JK flip flop is the same as **SR Bistable Latch** except for the addition of a clock input.

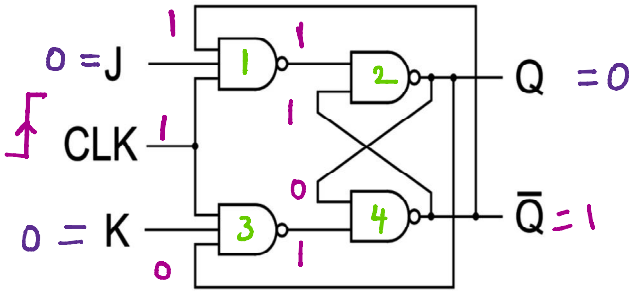
Block Diagram:



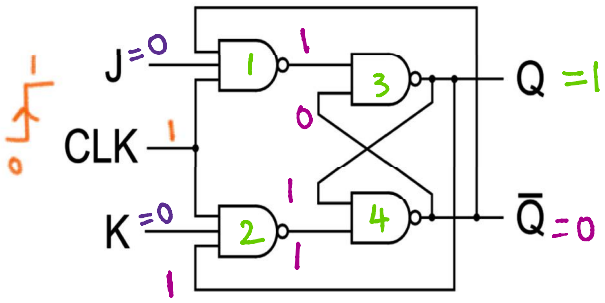
Circuit Diagram:



+ve edge triggered JK flip flop

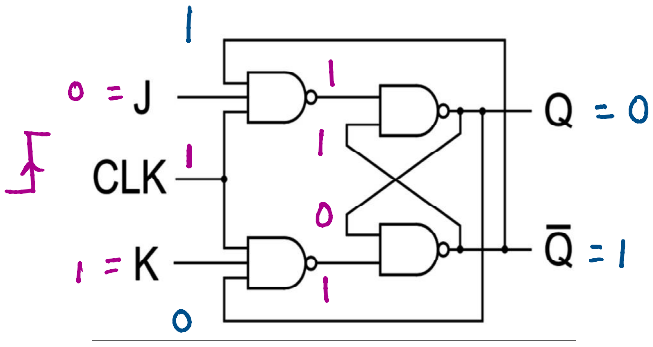


Clock	J	K	Q	Q(t+1)
1	0	0	0	0

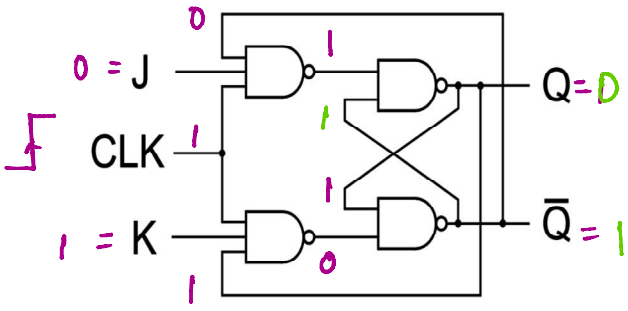


Clock	J	K	Q	Q(t+1)
↓	0	0	1	1

Clock	J	K	Q	Q(t+1)	
↓	0	0	0	0	} NO change
↓	0	0	1	1	



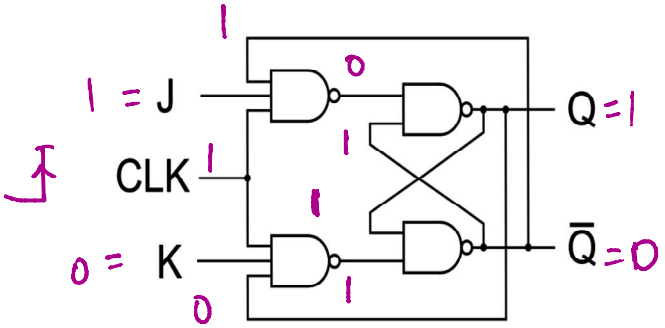
Clock	J	K	Q	Q(t+1)
↓	0	1	0	0



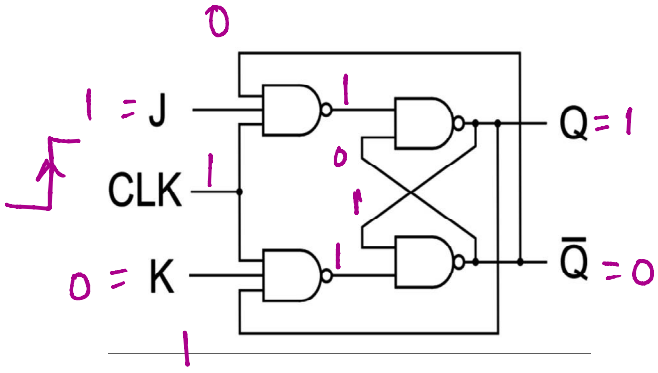
Clock	J	K	Q	Q(t+1)
↓	0	1	1	0

clock	J	K	Q	Q(t+1)
↓	0	1	0	0
↑	0	1	1	0

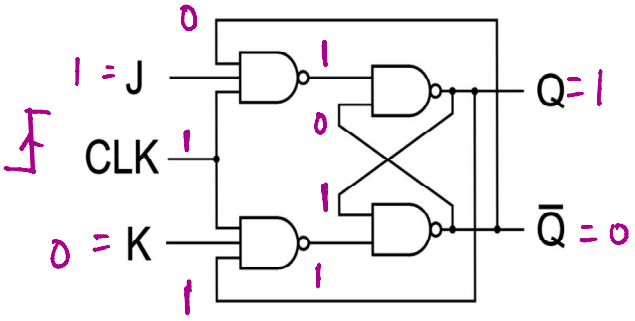
Reset



Clock	J	K	Q	Q(t+1)
↑	1	0	0	1



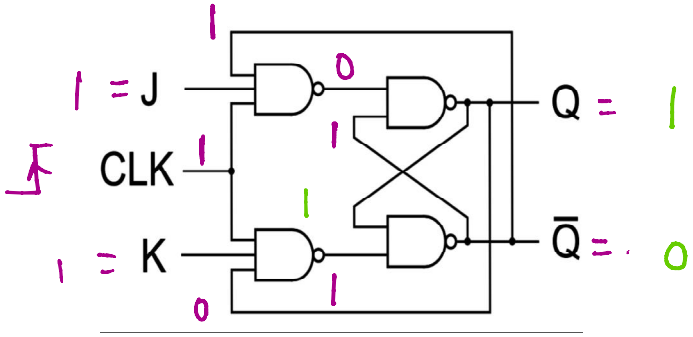
Clock	J	K	Q	Q(t+1)
↑	1	0	1	1



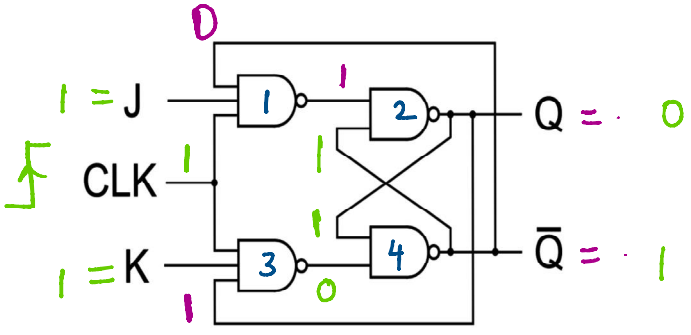
Clock	J	K	Q	Q(t+1)
↓	1	0	1	1

clock	J	K	Q	Q(t+1)
↑	1	0	0	1
↑	1	0	1	1

Set



Clock	J	K	Q	Q(t+1)
↓	1	1	0	1

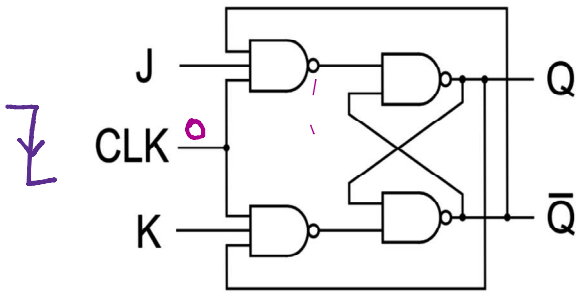


Clock	J	K	Q	Q(t+1)
↓	1	1	1	0

clock	J	K	Q	Q(t+1)
↓	1	1	0	1
↓	1	1	1	0

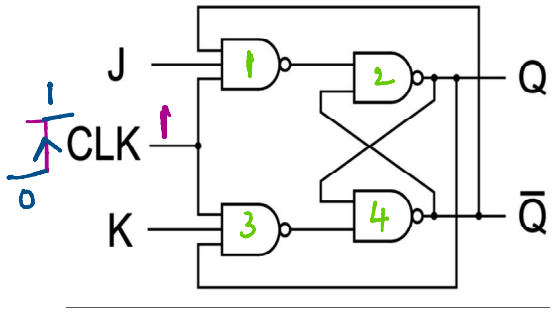
Toggle

+ve edge triggered JK flip flop



Clock	J	K	Q	Q(t+1)	State
↓	0	0	0	0	
↓	0	0	1	1	
↓	0	1	0	0	
↓	0	1	1	1	No change state
↓	1	0	0	0	
↓	1	0	1	1	
↓	1	1	0	0	
↓	1	1	1	1	

+ve edge triggered JK



Decimal	Clock	I/ps J	I/ps K	I/ps Q	O/p Q(t+1)	State
	↓	x	x	x	No change	
0	↑	0	0	0	0	No change
1	↑	0	0	1	1	
2	↑	0	1	0	0	Reset
3	↑	0	1	1	0	
4	↑	1	0	0	1	Set
5	↑	1	0	1	1	
6	↑	1	1	0	0 → 1	Toggle
7	↑	1	1	1	1 → 0	

$$Q(t+1) = J\bar{Q} + \bar{K}Q$$

Let us take $J=1$, $K=0$, $Q=0$

$Q(t+1) = ?$

$Q(t+1) = J\bar{Q} + \bar{K}Q$

$1 \cdot 1 + 1 \cdot 0$

$1 + 0 = 1$ ✓

Let us take $J=K=1$ & $Q=1$ then determine $Q(t+1)$

Characteristic equation for JK $\Rightarrow Q(t+1) = J\bar{Q} + \bar{K}Q$

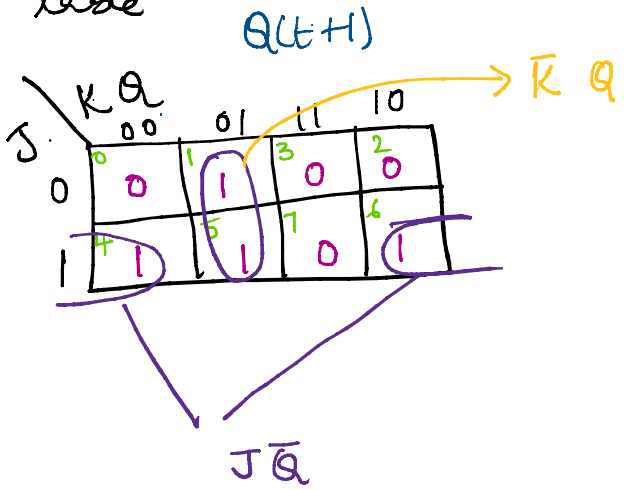
$1 \cdot 0 + 0 \cdot 1$

$0 + 0 = 0$

$Q(t+1) = 0$ ✓

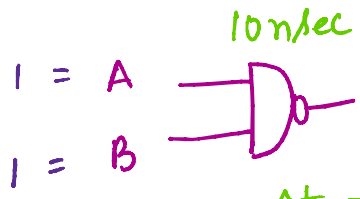
JK flip flop characteristic

Characteristic equation can be derived from the truth table



$Q(t+1) = J\bar{Q} + \bar{K}Q$ ✓

Propagation delay :- Time taken for the ckt to change its o/p, after application of i/p

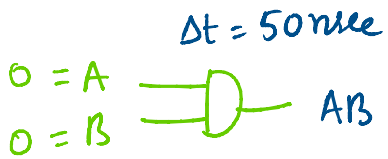


A=1, B=1 ⇒ $\overline{AB}$ = 0 ✓

Suddenly A=0, B=1

then I will get my o/p after 10 nsec

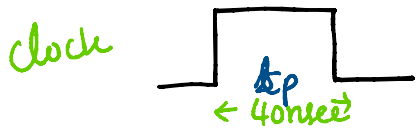
$\overline{AB}$ = 1

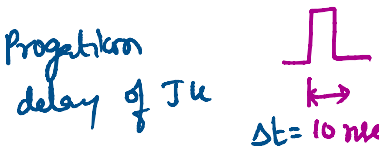


propagation time for AND is 50nsec

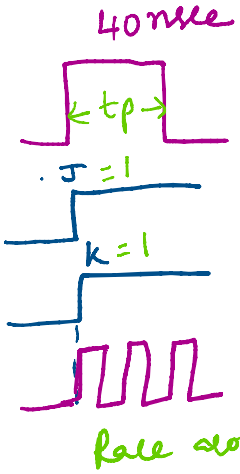
JK flip flop, propagation delay Δt = 10 nsec

clock pulse width t_p = 40 nsec





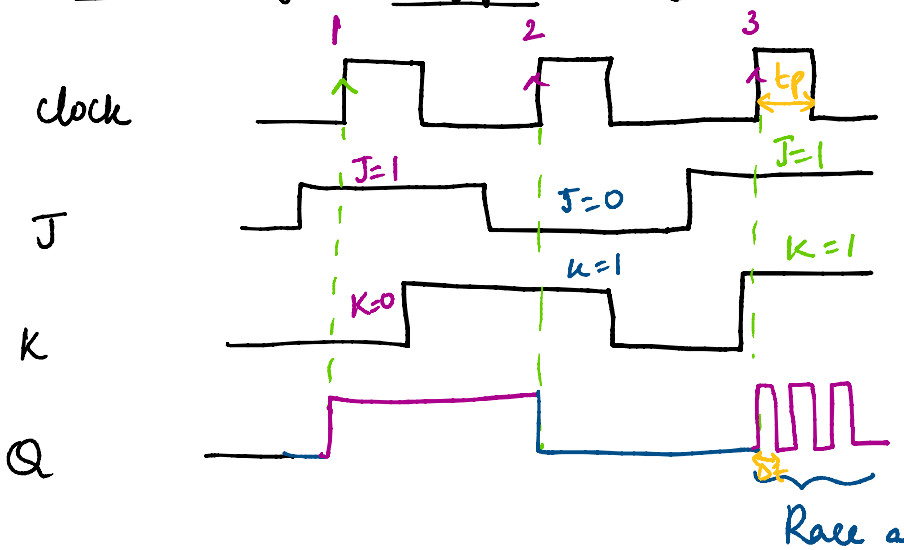
$t_p > \Delta t$ ✓



J = K = 1 &
Q = 0
Q(t+1) = 1

J = k = 1
Q = 1
Q(t+1) = 0

+ve edge triggered JK flip flop



1st → J=1, K=0, Q=0
Q(t+1) = 1

2nd clock
J=0, K=1, Q=1
Q(t+1) = 0

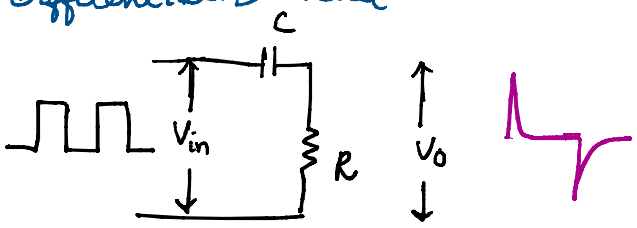
3rd clock
J=1, K=1, Q=0
Q(t+1) = · Toggle

If $t_p > \Delta t$ → Race around condition

$V_{in} = 5V \Rightarrow \frac{dV_{in}}{dt} = 0$

Spike waveform (Edge triggered clock)

Differentiator circuit



Race Around Condition

clock pulse width ↓ t_p >> Δt. → propagation delay

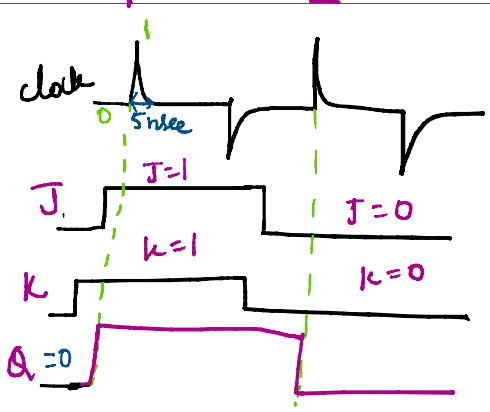
- The *race around condition* occurs if $t_P >> \Delta t$.

How we can avoid race-around condition?

We can avoid race around condition by the following way.

1. If $t_P < \Delta t$.
2. By using edge triggering flip-flop.
3. By using Master-Slave JK Flip-flop.

Edge triggered JK flip flop



Δt = 10nsec

t_p = 5nsec

1st clock

J=K=1 Q=0

Q(t+1) = 1

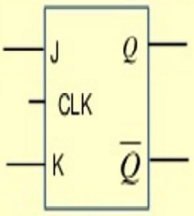
2nd clock

J=0, K=0, Q=1, Q(t+1)=0

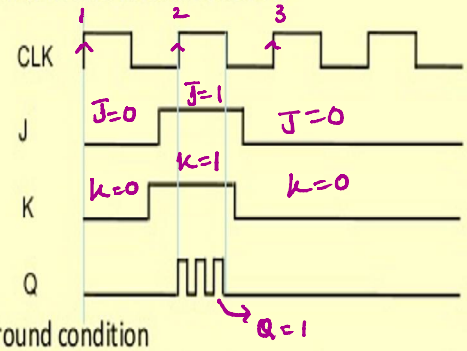
•when J=K=1, output toggles recursively during active period of clock pulse

•This leads to unpredictable output state after active period of clock pulse

• This condition is know as race around condition



JK Flip Flop symbol



•Solution to race around condition

• Master slave FF: that gives a single trigger at slave output. How ever race around condition occurs in Master.

•Edge triggered FF: flip-flop triggers the 'edge' of clock pulse

1st clock
J=0, k=0, Q=0
Q(t+1) = 0

2nd clock
J=k=1, Q=0
Q(t+1) = toggle

3rd clock
J=k=0, Q=0
Q(t+1) = 1