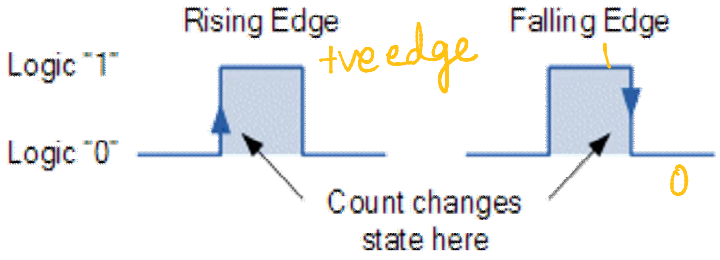
Synchronous Counter

① Synchronous counter design is same for both +ve edge triggered and -ve edge triggered



1 → 0 ⇒ -ve edge

② Same clock pulse for all flip flops

③ Synchronous counter can be realised using any type of flip flop

④ Order of flip flop arrangement is not important here, cause the excitation is independent for every flip flop

⑤ It is not necessary that all flip flops in a circuit has to be of the same type, can use any combination JK & D, JK & T, D & T, RS & T for realizing the circuit.

Design of synchronous counter

Step 1 No. of flip flops

Required no. of 'n' flip flops

The smallest value of 'n' such that no. of states $2^n \geq N$

Step 2 choice of flip flops and excitation table

Select the type of flip flops to be used and write the excitation table.

An excitation table is the table that lists the present state (PS), the next state (NS) and required excitations.

Step 3 Minimum expression for excitations

Using K-map obtain expressions in terms of present states and inputs

Step 4 Logic diagram

Draw logic diagram based on minimal expressions

① Design 3 bit synchronous counter (Mod 8) using JK flip flops.

Step 1 → No. of flip flops

3 bit synchronous means, 3 flip flops

$n = 3$

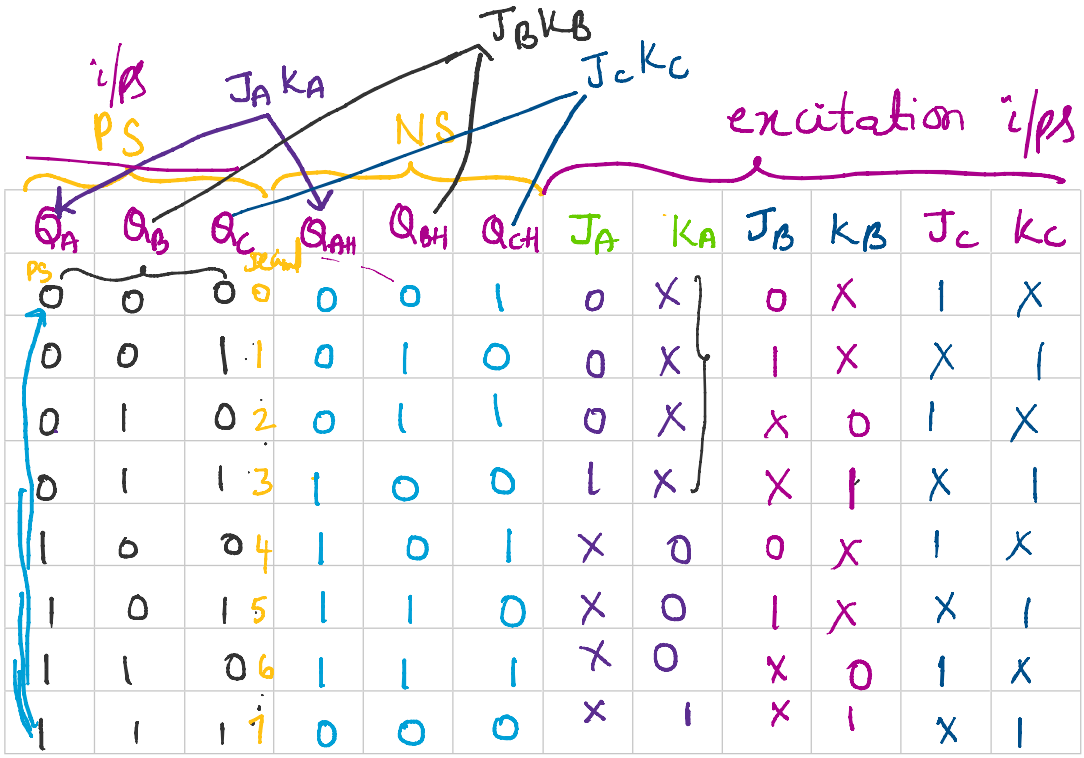
$2^n \geq N \implies 2^3 \geq N$

$2^3 = 8$ ✓

3 bit syn means 8 states

Step 2 choice of flip flop is JK, need to excitation table for JK

Excitation table for 3bit synchronous counter



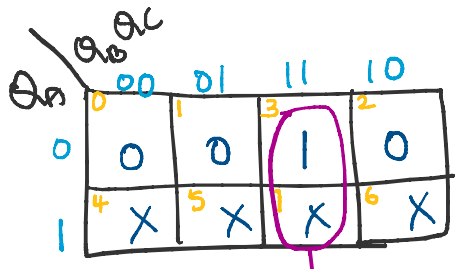
Q_A	Q_B	Q_C		Q_{AH}	Q_{BH}	Q_{CH}	J_A	K_A	J_B	K_B	J_C	K_C
PS			SCount									
0	0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	1	0	1	0	0	X	1	X	X	1
0	1	0	2	0	1	1	0	X	X	0	1	X
0	1	1	3	1	0	0	1	X	X	1	X	1
1	0	0	4	1	0	1	X	0	0	X	1	X
1	0	1	5	1	1	0	X	0	1	X	X	1
1	1	0	6	1	1	1	X	0	X	0	1	X
1	1	1	7	0	0	0	X	1	X	1	X	1

JK flip flop excitation

Q	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

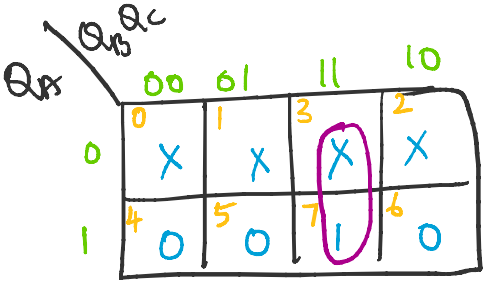
Step 3 minimal expressions for excitation i/p

for J_A



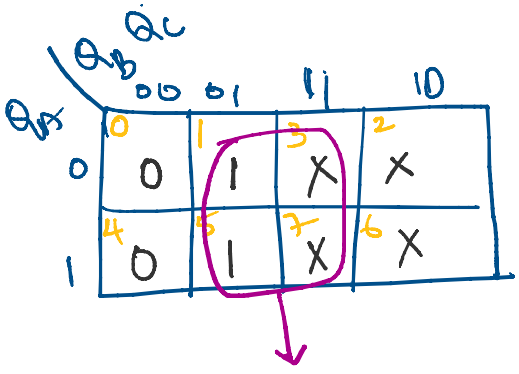
$J_A = Q_B Q_C$

for K_A



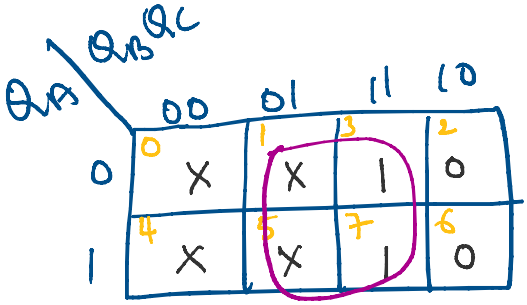
$K_A = Q_B Q_C$

for J_B



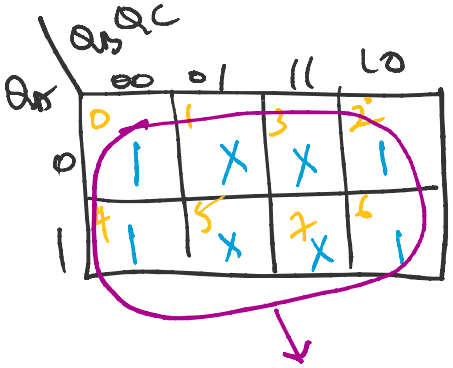
$J_B = Q_C$

for K_B



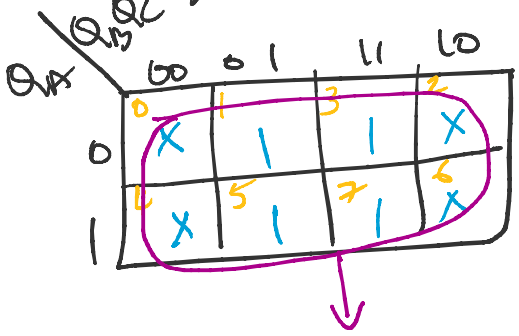
$K_B = Q_C$

for J_C



$J_C = 1$

for K_C



$K_C = 1$

Step 4 logic diagram

$J_A = K_A = Q_B Q_C$; $J_B = K_B = Q_C$; $J_C = K_C = 1$

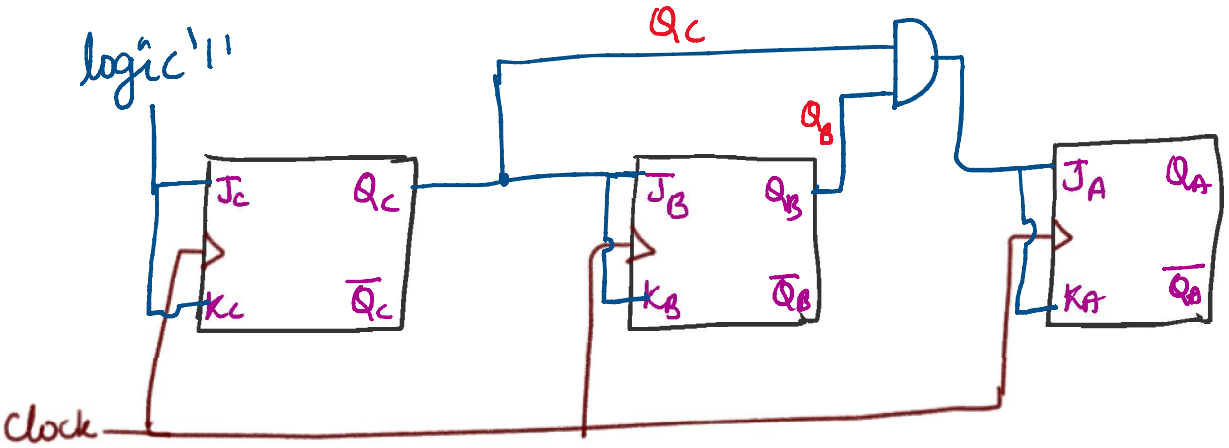


fig : 3 bit synchronous binary counter