

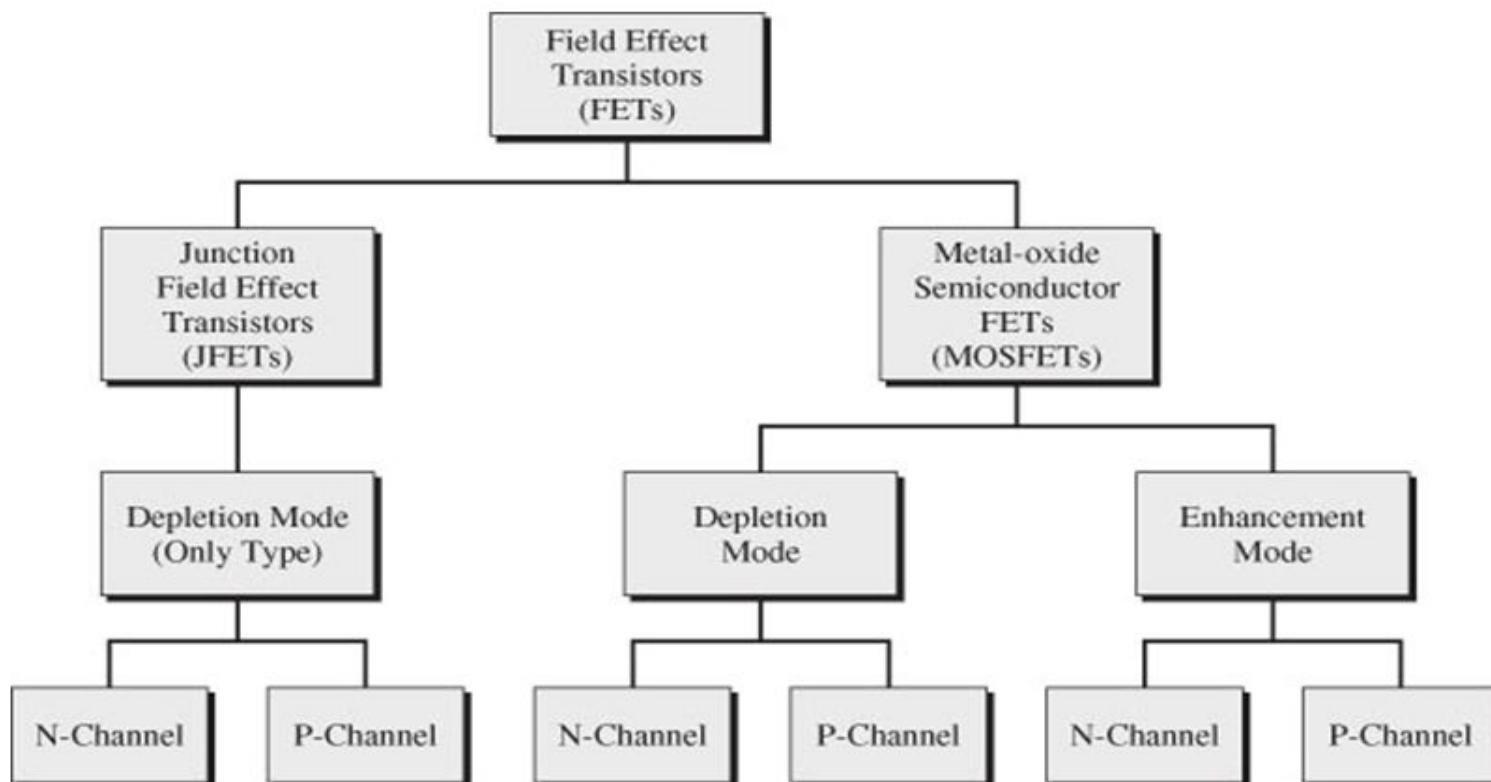
Field Effect Transistor(FET)

Field-Effect Transistor (FET)

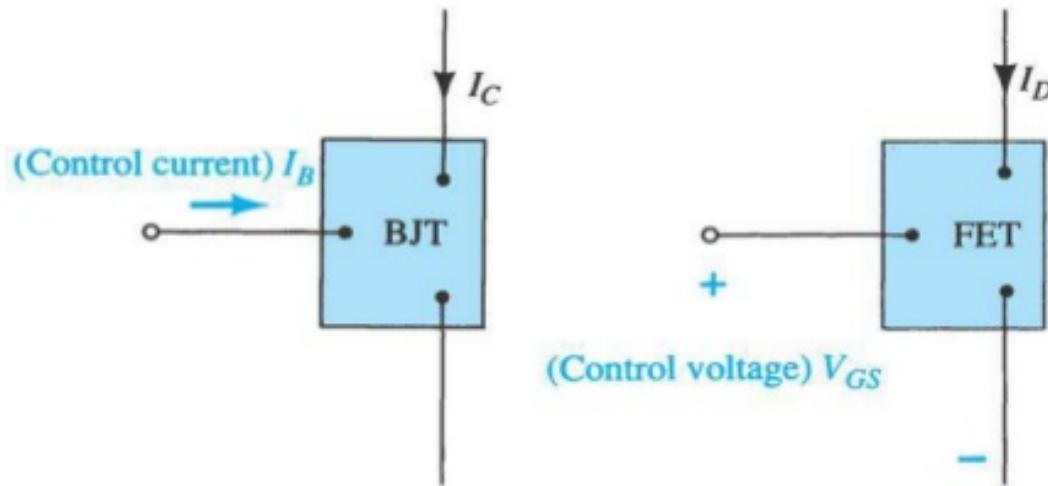
The field-effect transistor is a type of transistor that uses an electric field to control the flow of current. FETs are devices with three terminals: Source, Gate, and Drain. FETs control the flow of current by the application of a voltage to the gate, which in turn alters the conductivity between the drain and source.

FETs are also known as unipolar transistors since they involve single-carrier-type operation. That is, FETs use either electrons or holes as charge carriers in their operation, but not both.

Field Effect Transistor Family



FET's vs. BJT's



Similarities:

- Amplifiers
- Switching Device
- Impedance Matching Circuits

The Junction Field Effect Transistor (JFET)

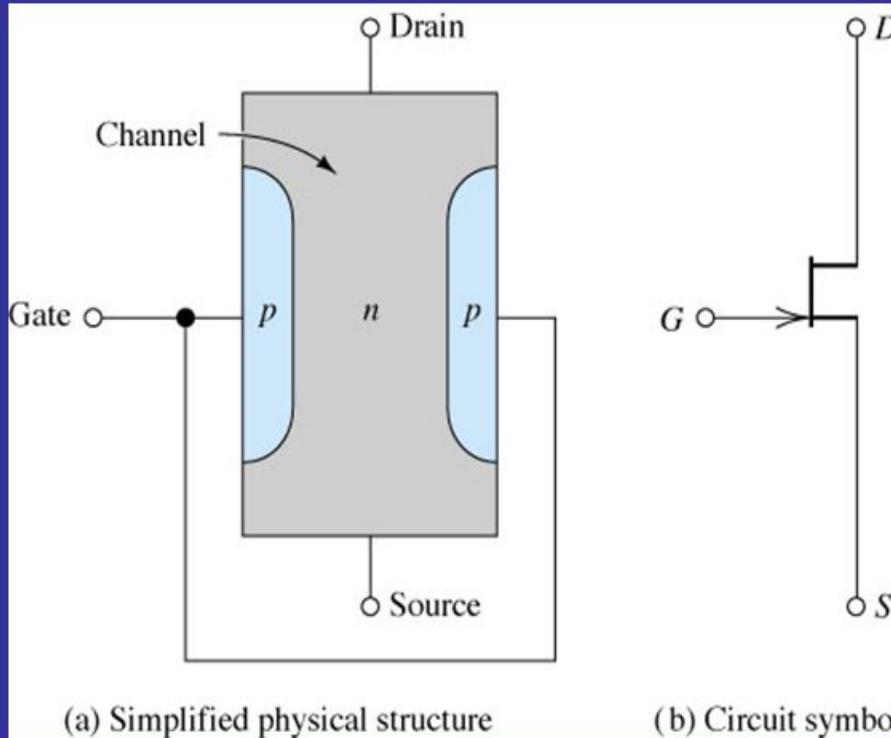
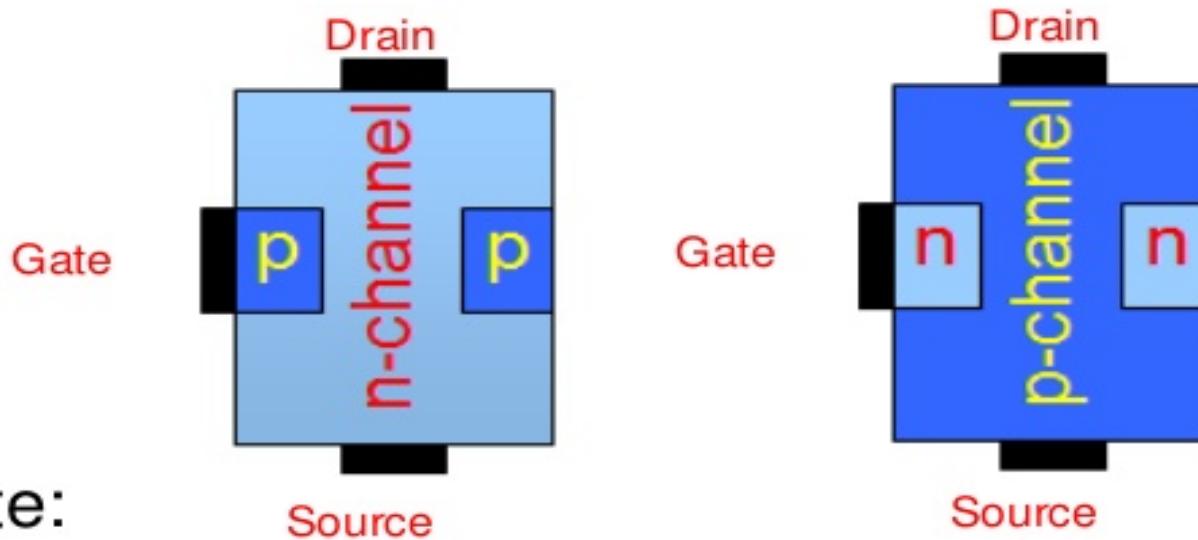


Figure: *n*-Channel JFET.

Two types of JFET

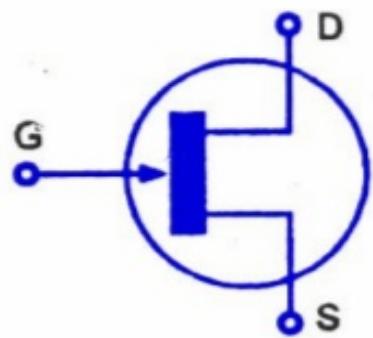
1. n-channel
2. p-channel



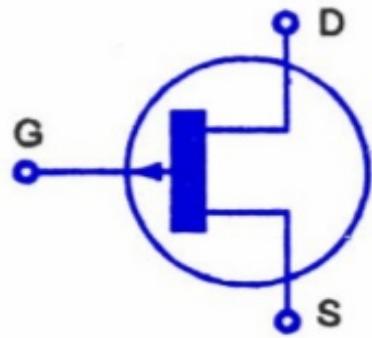
Note:

- n-channel is more widely used.

In n-channel , both side of the n-type bar, heavily doped P+ regions of acceptor impurities have been formed by alloying or diffusion for creating p-n junctions



N-Channel JFET



P-Channel JFET

Schematic Symbols For JFETs

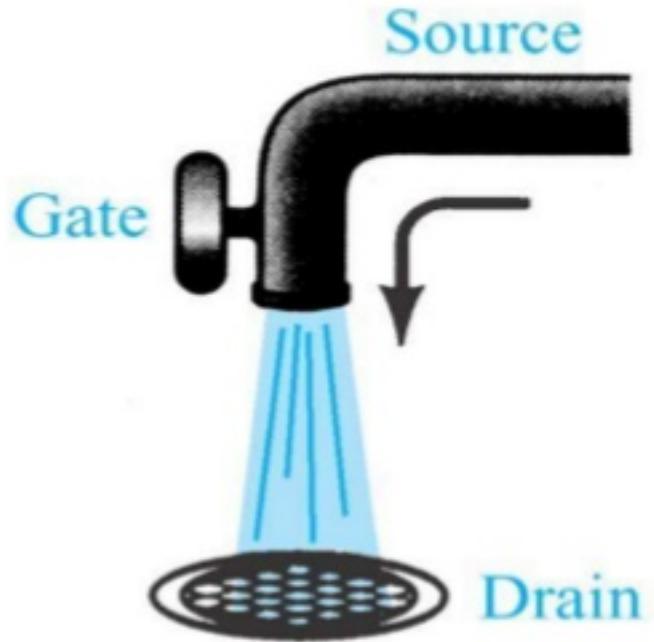
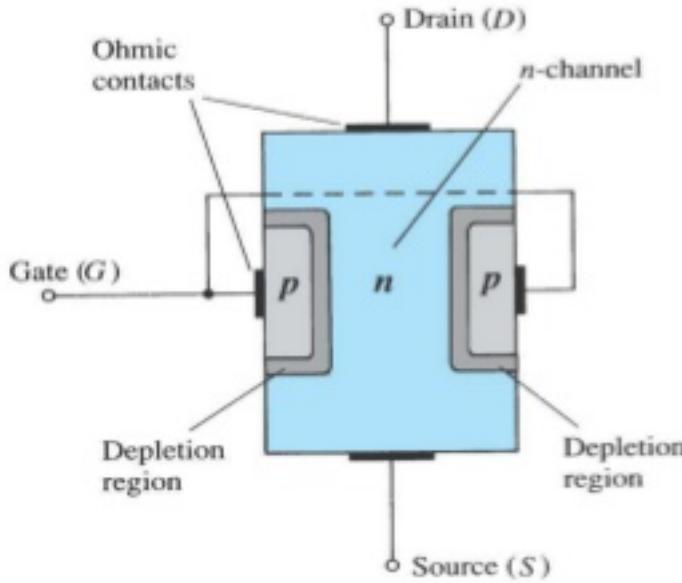
- JFET is always operated with the gate-source PN junction **reversed biased**.
- Reverse biasing of the gate source junction with the negative voltage produces a depletion region along the PN junction which extends into the n-channel and thus **increases its resistance** by restricting the channel width as shown in the preceding figure.

CONSTRUCTION AND CHARACTERISTICS OF JFET

- Is a three-terminal device with one terminal capable of controlling the current between the other two.

3 terminals are:

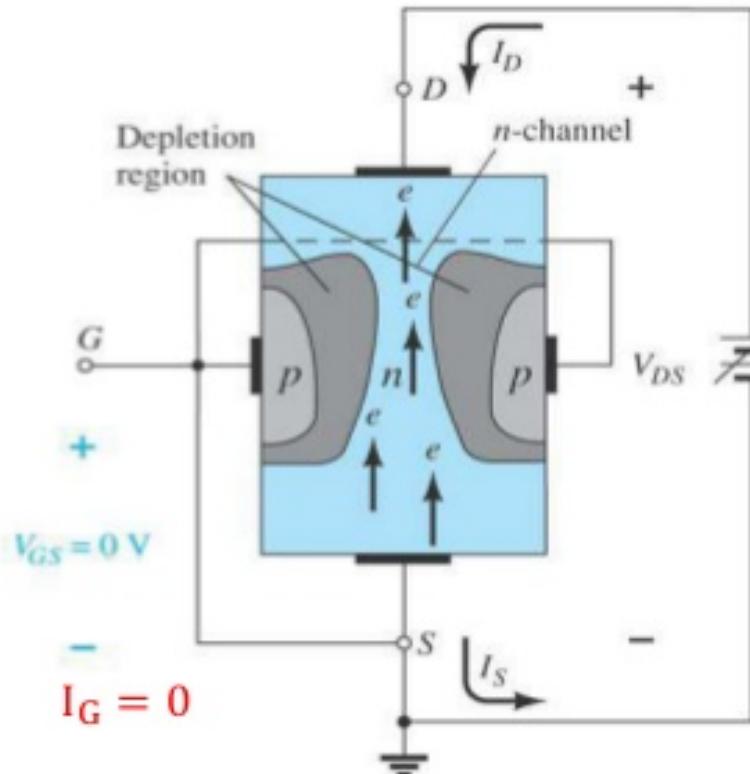
1. DRAIN (D)
2. SOURCE (S) – connected to n-channel
3. GATE (G) – connected to p-channel



- **Drain (D) and Source (S) are connected to the n-channel**
- **Gate (G) is connected to the p-type material**

$V_{GS} = 0, V_{DS}$ SOME POSITIVE VALUE

When $V_{GS} = 0$ and V_{DS} is increased from 0 to a more positive voltage.



- The depletion region between p-gate and n-channel increases
- Increasing the depletion region, decreases the size of the n-channel which increases the resistance of the n-channel.
- Even though the n-channel resistance is increasing, the current (I_D) from source to drain through the n-channel is increasing. This is because V_{DS} is increasing.

Recall from DIODE discussion:

- The greater the applied reverse bias, the wider is the depletion region.

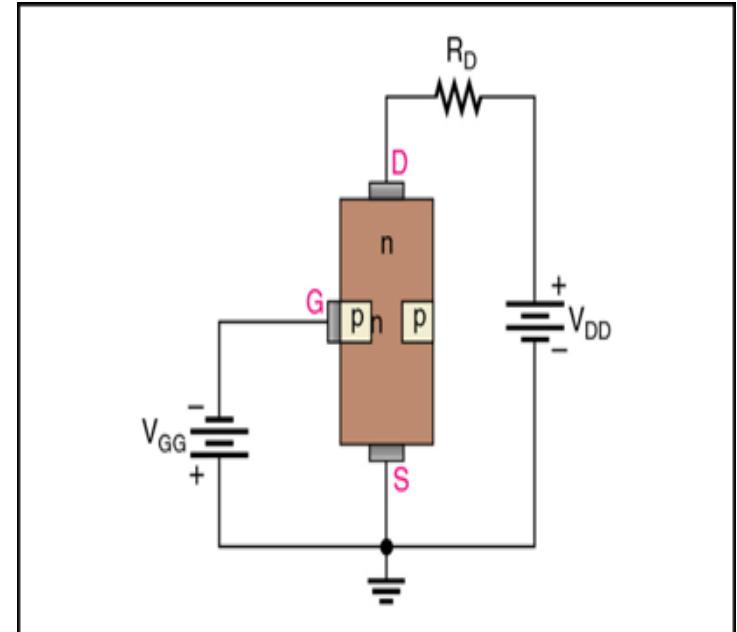
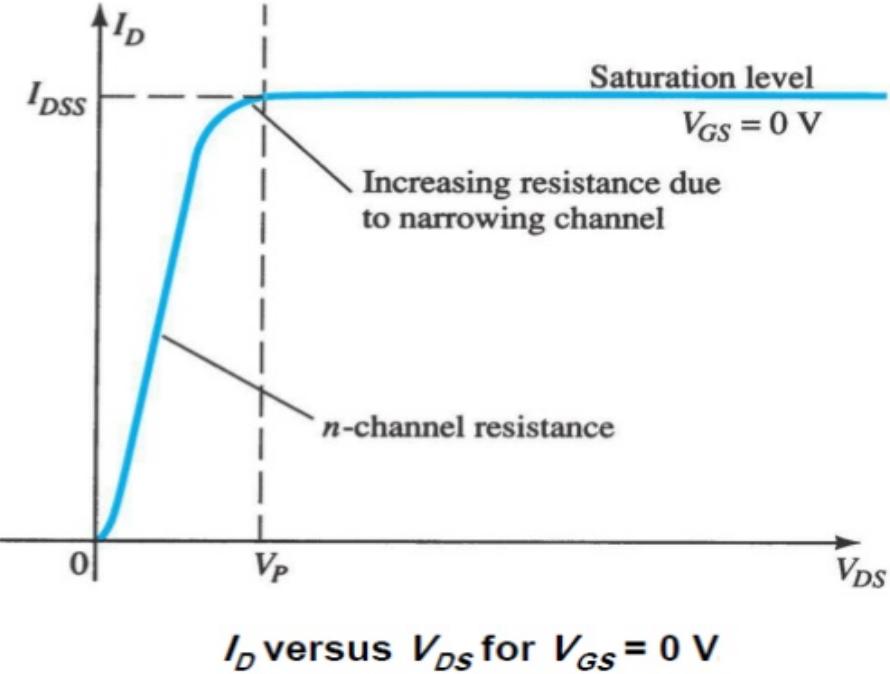
FET

1. FET is an unipolar semiconductor device because its operation depends upon the flow of majority carriers i.e., either holes or electrons as the case may be.
 2. The input impedance of FET is much more larger (ranging in Megaohms) than BJT. The reason behind this is that the input terminal i.e., gate to source of FET is reverse biased and reverse bias offers ideally infinite resistance.
 3. FET is a voltage controlled device.
 4. FET is less noisy. Because there are no junctions.
 5. Higher frequency response.
 6. Good thermal stability because of absence of minority carriers.
 7. Costlier than BJT.
 8. Small sized.
 9. In FET, relationship between input and output quantities is nonlinear due to square term in shockley's equations
- $$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$
10. No offset voltage; so it works better as a switch or chopper.
 11. Small gain bandwidth product.

BJT

1. BJT is a bipolar semiconductor device because the current constituting elements are both majority carriers as well as minority carriers in this case.
 2. The input impedance of BJT is very less in comparison to FET.
 3. BJT is a current controlled device.
 4. Much noisy than FET.
 5. Frequency variation affects the performance.
 6. Temperature dependent, thermal runaway may cause.
 7. Relatively cheaper.
 8. Comparatively bigger.
 9. The BJT is an almost linear device or we can say that BJT works linearly in active region as an amplifier.
10. There is always an offset voltage before switching.
 11. Greater than FET.

FET Characteristics: The Drain Characteristics



General Relationships

For all FETs:

$$I_G \approx 0A$$

$$I_D = I_{SS}$$

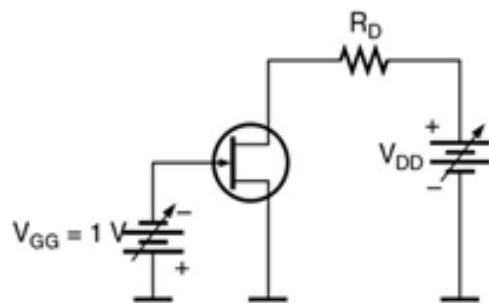
For JFETs and depletion-type MOSFETs:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

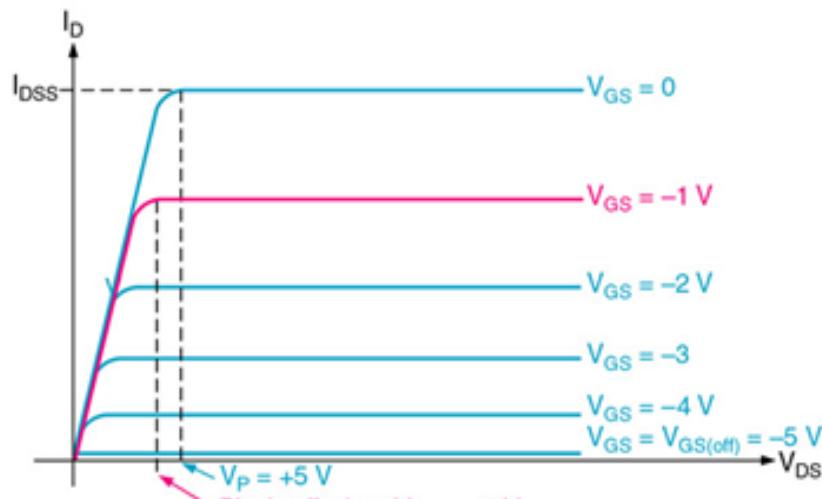
For enhancement-type MOSFETs:

$$I_D = k(V_{GS} - V_T)^2$$

JFET Common Source Drain Characteristics



(a) JFET biased at $V_{GS} = -1\text{ V}$



(b) Family of drain characteristic curves

REGIONS OF JFET ACTION

1. Ohmic Region – linear region
 - JFET behaves like an ordinary resistor
2. Pinch Off Region
 - Saturation or Amplifier Region
 - JFET operates as a constant current device because I_d is relatively independent of V_{ds}
 - I_{dss} – drain current with gate shorted to source.
3. Breakdown Region
 - If V_{ds} is increased beyond its value corresponding to V_a – avalanche breakdown voltage.
 - JFET enters the breakdown region where I_d increases to an excessive value.

4. Cut Off Region

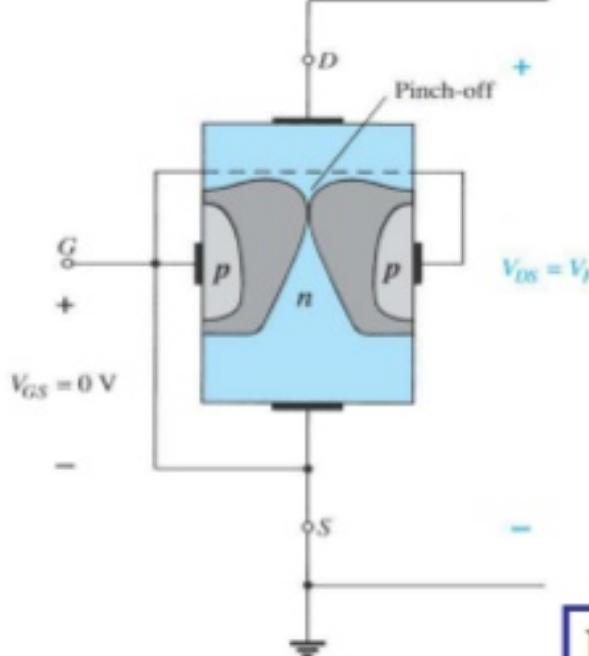
- As V_{gs} is made more and more negative, the gate reverse bias increases which increases the thickness of the depletion region.
- As negative value of V_{gs} is increased, a stage comes when the 2 depletion regions touch each other.

$$V_{gs\text{ (off)}} = -V_p$$

$$|V_p| = |V_{gsoff}|$$

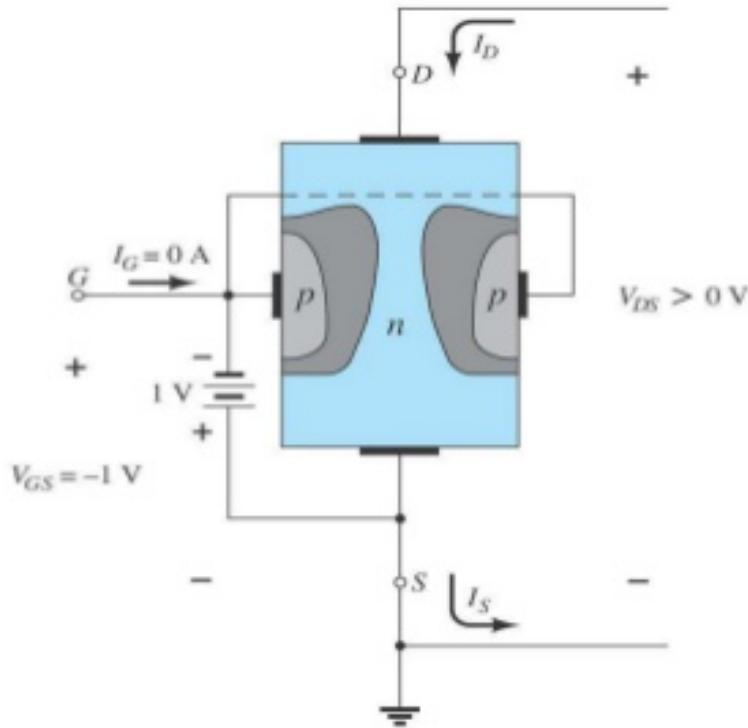


JFET OPERATING CHARACTERISTICS: PINCH OFF



- If $V_{GS} = 0$ and V_{DS} is further increased to a more positive voltage, then the depletion zone gets so large that it **pinches off** the n-channel.
- As V_{DS} is increased beyond $|V_P|$, the level of I_D remains the same ($I_D = I_{DSS}$)

I_{DSS} is the maximum drain current for a JFET and is defined by the conditions $V_{GS}=0$ and $V_{DS} > |V_P|$.



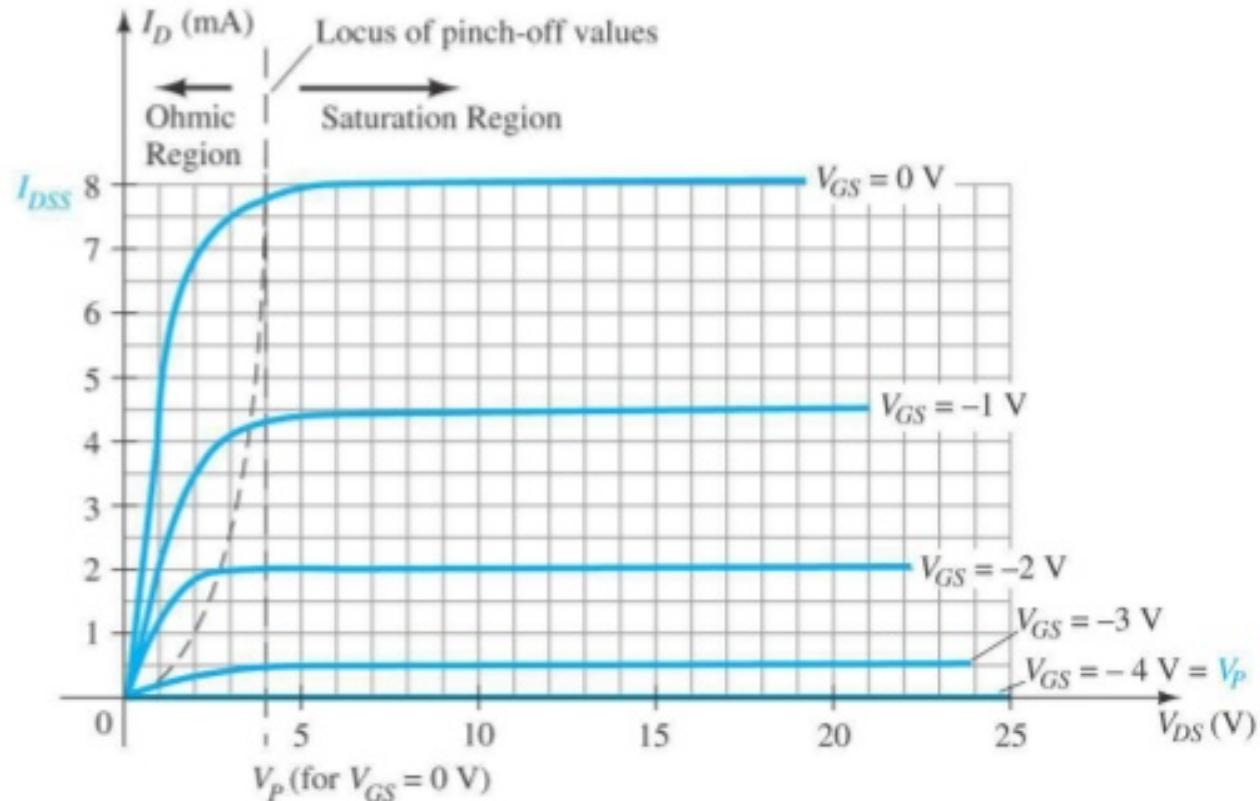
$$V_{GS} \geq 0$$

- Voltage from gate to source is controlling voltage of the JFET.
- As V_{GS} becomes more negative, the depletion region increases.
- The more negative V_{GS} , the resulting level for I_D is reduced.
- Eventually, when $V_{GS} = V_p$ [$V_p = V_{GS}$ (off)], I_D is 0 mA. (the device is “turned off”).

•The level of V_{GS} that results in $I_D=0$ mA is defined by $V_{GS}=V_p$, with V_p being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.

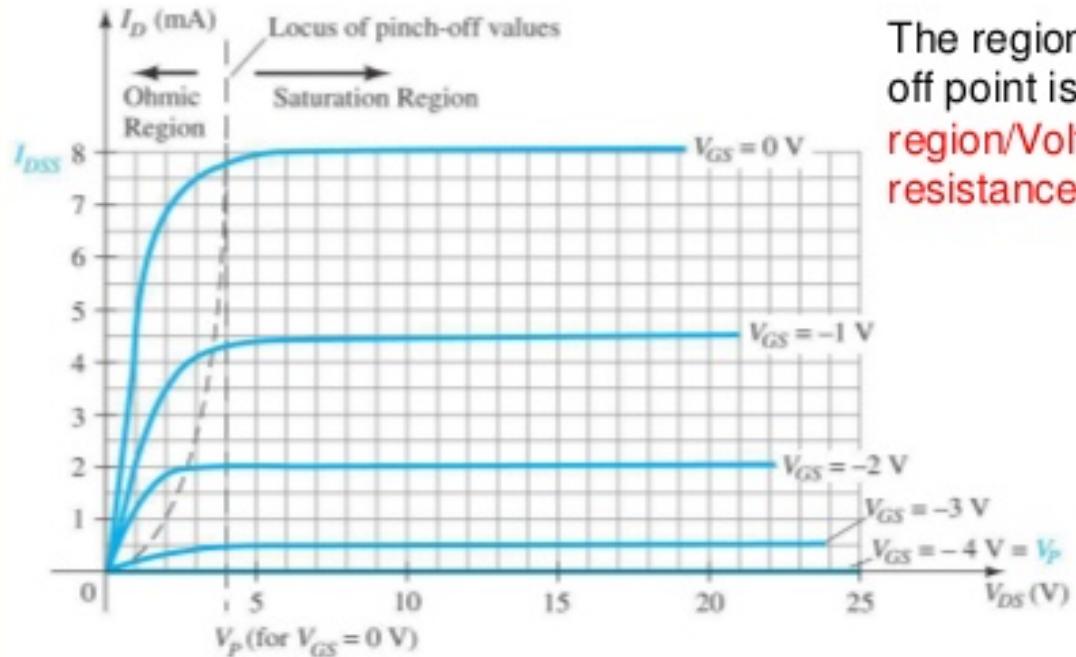
Application of a negative voltage to the gate of a JFET.

JFET OPERATING CHARACTERISTICS



n-Channel JFET characteristics with $ID_{SS} = 8 \text{ mA}$ and $V_P = -4 \text{ V}$.

JFET OPERATING CHARACTERISTICS: VOLTAGE-CONTROLLED RESISTOR



The region to the left of the pinch-off point is called the **ohmic region/Voltage controlled resistance region**.

The JFET can be used as a variable resistor, where V_{GS} controls the drain-source resistance (r_d). As V_{GS} becomes more negative, the resistance (r_d) increases.

$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_p}\right)^2}$$

where **r_o** is the resistance with VGS=0 and **r_d** is the resistance at a particular level of VGS.

FOR EXAMPLE:

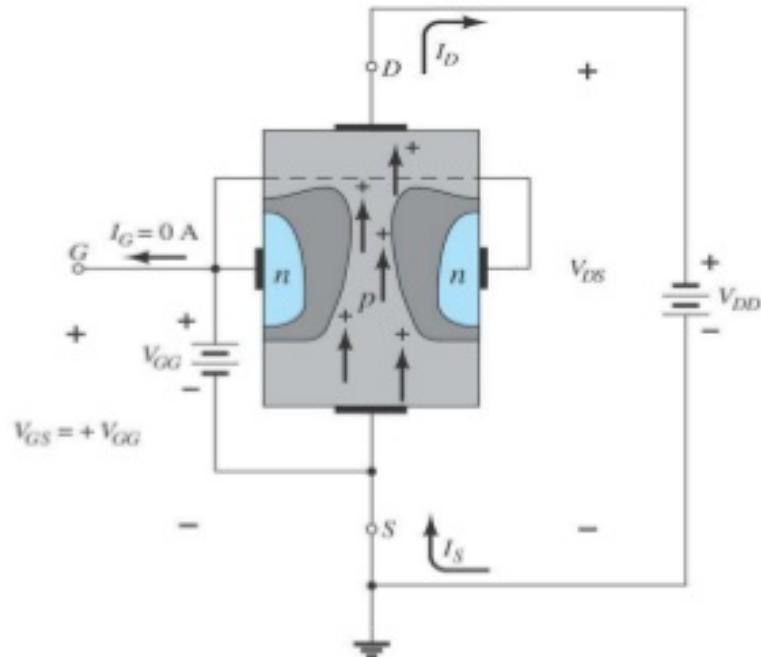
1. For an n-channel JFET with $r_o = 10k\Omega$ ($V_{GS} =$

$$r_d = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

$$r_d = \frac{10k\Omega}{\left(1 - \frac{(-3)}{(-6)}\right)^2}$$

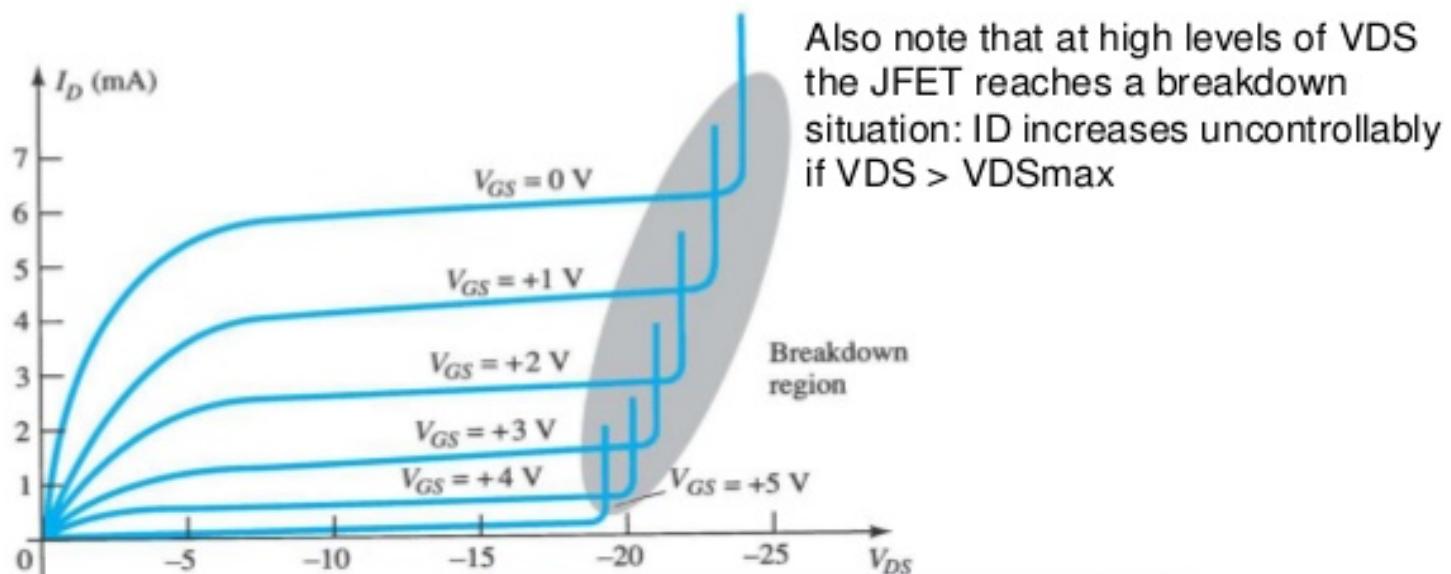
$$r_d = 40k\Omega$$

P-CHANNEL JFETS



The p-channel JFET behaves the same as the n-channel JFET, except the voltage polarities and current directions are reversed.

P-CHANNEL JFET CHARACTERISTICS



Also note that at high levels of V_{DS} the JFET reaches a breakdown situation: I_D increases uncontrollably if $V_{DS} > V_{DS\max}$

As V_{GS} increases more positively

- The depletion zone increases
- I_D decreases ($I_D < I_{DSS}$)
- Eventually $I_D = 0 \text{ A}$

JFET TRANSFER CHARACTERISTICS

In a **BJT**, β indicates the relationship between I_B (input) and I_C (output).

$$I_C = f(I_B) = \beta I_b$$

↓

Control variable

Constant

In a **JFET**, the relationship of V_{GS} (input) and I_D (output) is defined by Shockley's Equation

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

Constant

Control variable

PLOTTING THE JFET TRANSFER CURVE

Using I_{DSS} and V_p ($V_{GS}(off)$) values found in a specification sheet, the transfer curve can be plotted according to these **three steps**:

Step 1:

$$\text{Solving for } V_{GS} = 0, \quad I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2, \quad I_D = I_{DSS}$$

Step 2:

$$\text{Solving for } V_{GS} = V_p (V_{GS}(off)), \quad I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2, \quad I_D = 0 \text{ A}$$

Step 3:

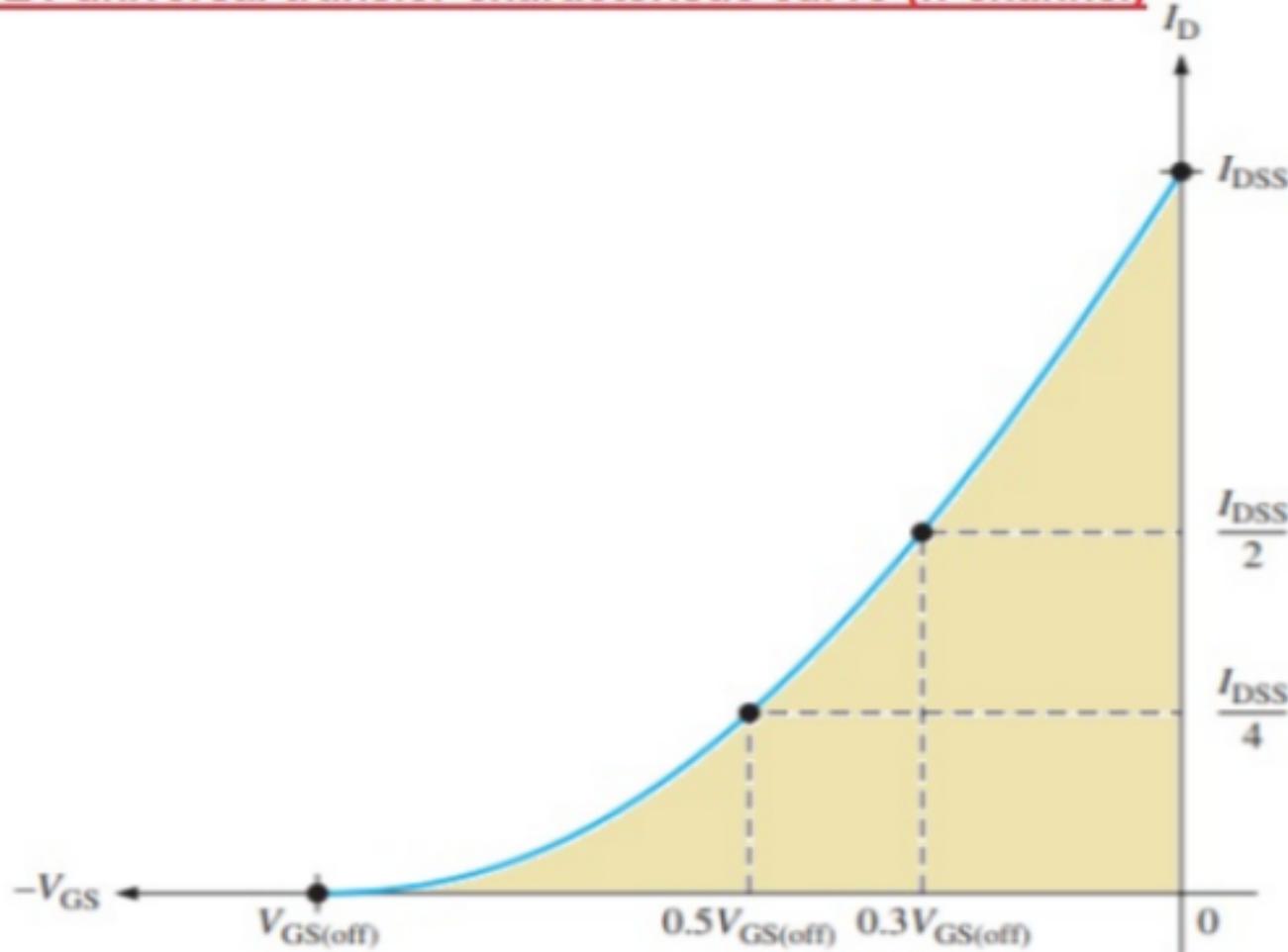
Solving for I_D if we substitute $V_{GS} = -1 \text{ V}$, $I_{DSS} = 8\text{mA}$ and $V_p = -4$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2, \quad I_D = 8\text{mA} \left(1 - \frac{(-1)}{(-4)} \right)^2,$$

$$I_D = 4.5\text{mA}$$

Transfer Characteristics

JFET universal transfer characteristic curve (n-channel)



$$V_{GS} = 0$$

$$V_{GS} = V_p$$

$$V_{GS} = 0.5 V_p$$

$$V_{GS} = 0.3V_p$$

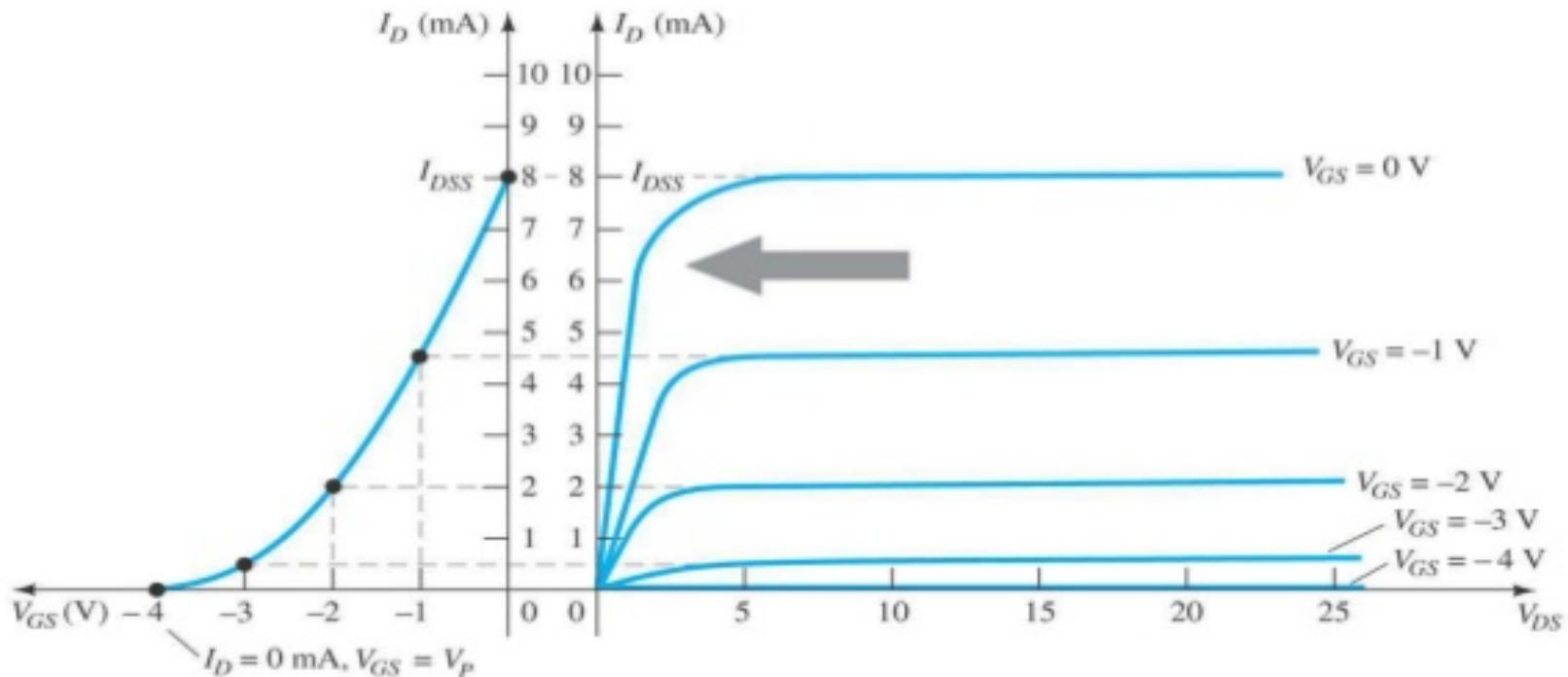
$$I_D = I_{DSS}$$

$$I_D = 0 \text{ mA}$$

$$I_D = I_{DSS}/4$$

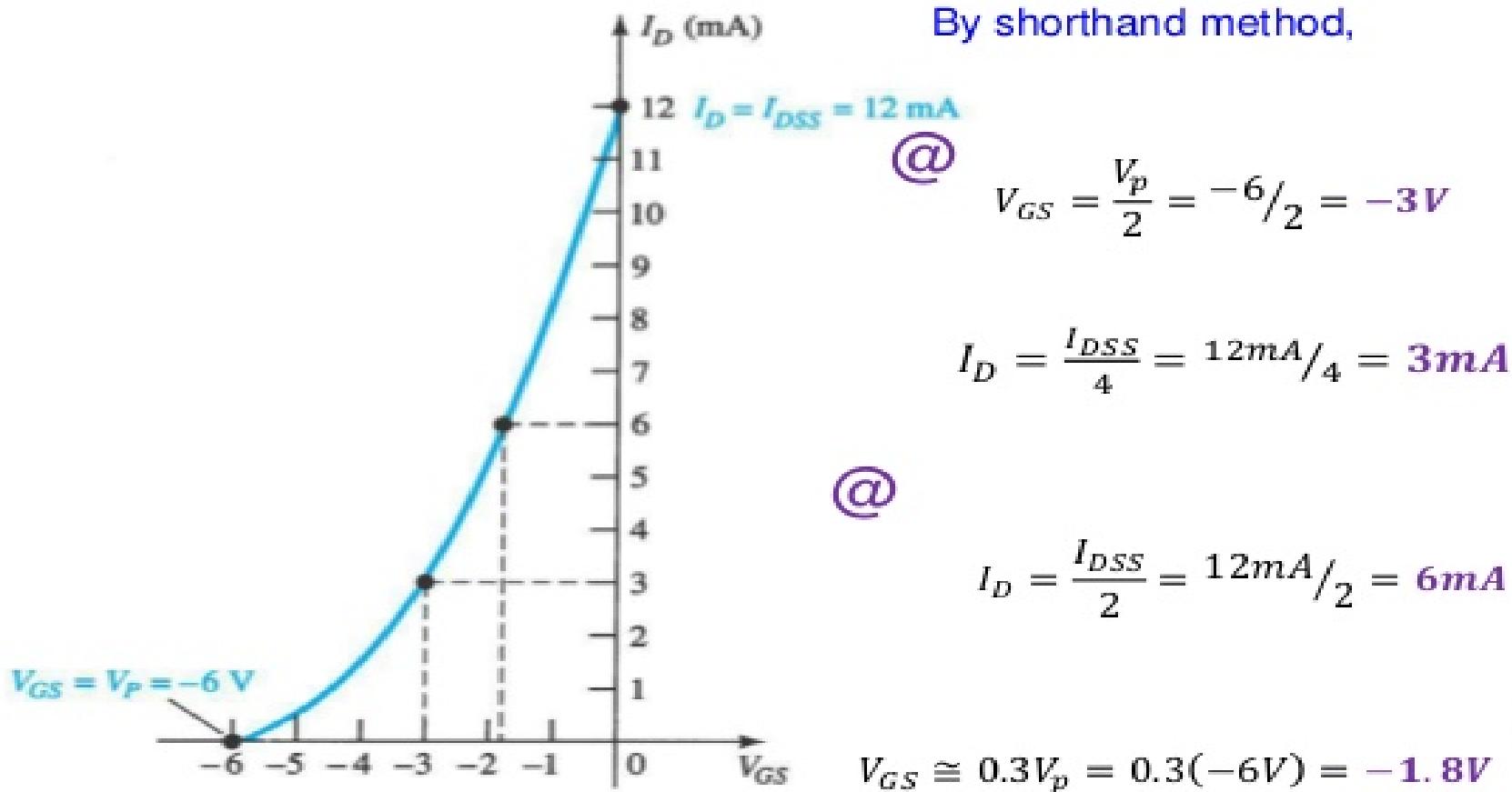
$$I_D = I_{DSS}/2$$

This graph shows the value of I_D for a given value of V_{GS} .

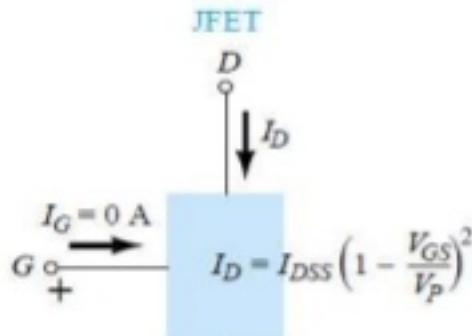


For Example:

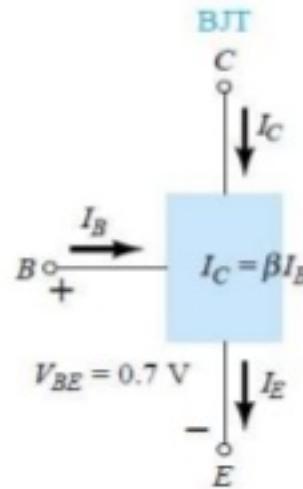
Sketch the transfer curve defined by $I_{DSS} = 12mA$ and $V_p = -6V$.



IMPORTANT RELATIONSHIPS



(a)



(b)

JFET

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \Leftrightarrow I_C = \beta I_B$$

$$I_D = I_S$$

$$\Leftrightarrow I_C \cong I_E$$

$$I_G \cong 0 \text{ A}$$

$$\Leftrightarrow V_{BE} \cong 0.7 \text{ V}$$

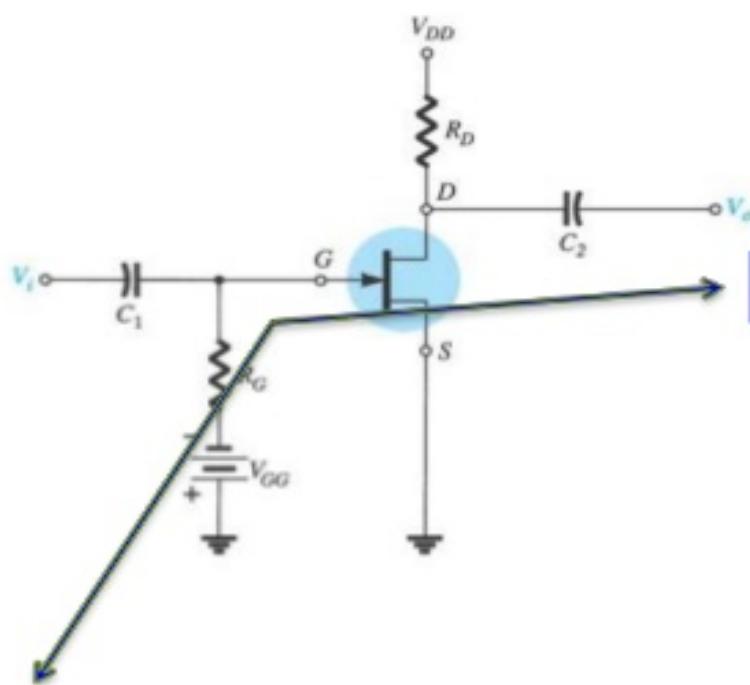
FET Biasing

Biasing of FET



- 1. Fixed Bias Configuration**
- 2. Self Bias Configuration**
- 3. Voltage Divider Configuration**

Fixed-Bias Configuration

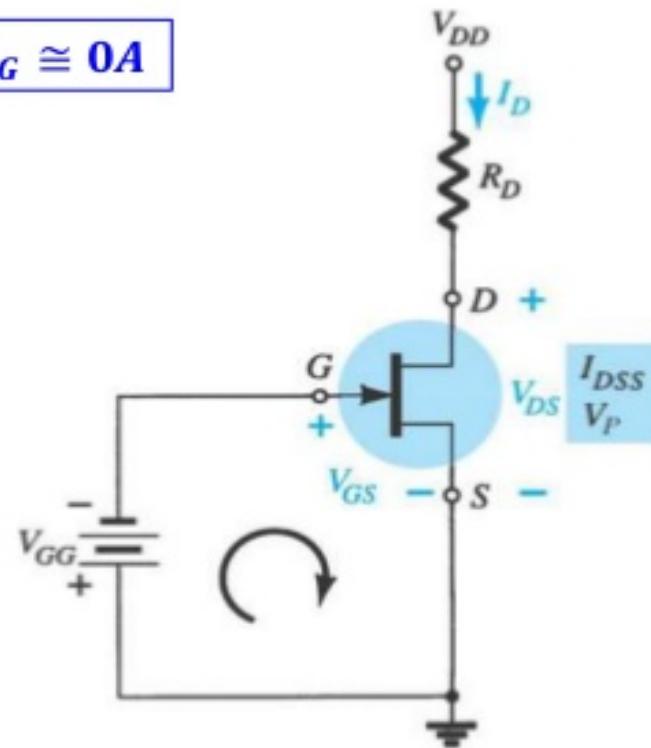


$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

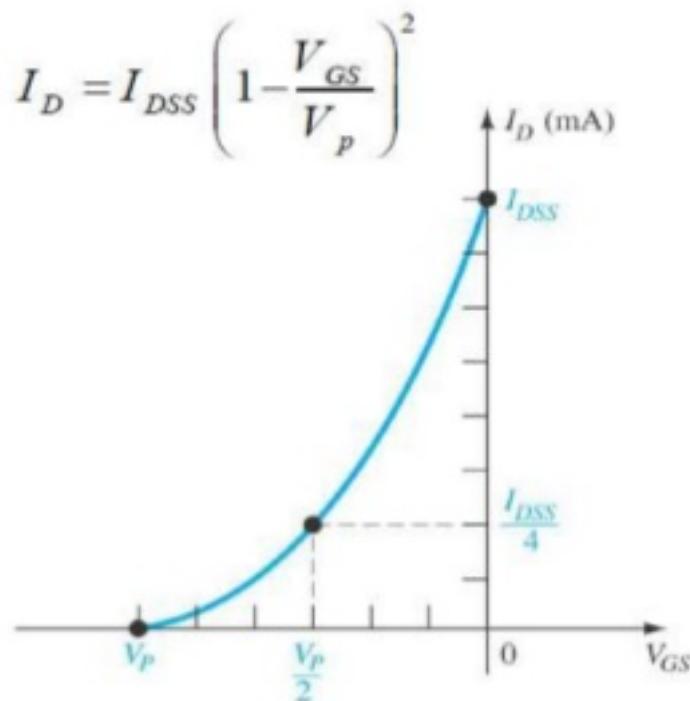
$$I_G \cong 0A$$

$$V_{Rg} = I_G(R_G) = (0) = R_G 0V$$

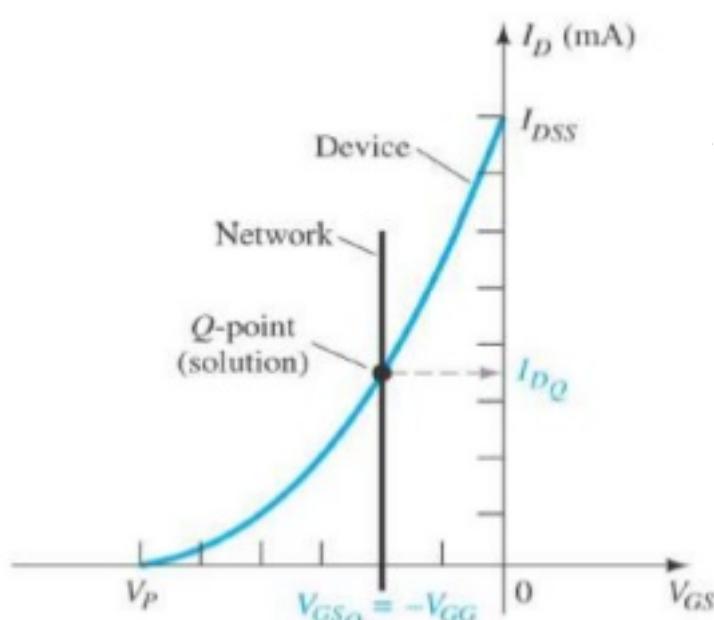
The zero volt drop across R_G permits replacing R_G by a short circuit equivalent.



Fixed-Bias Configuration –Graphical Solution



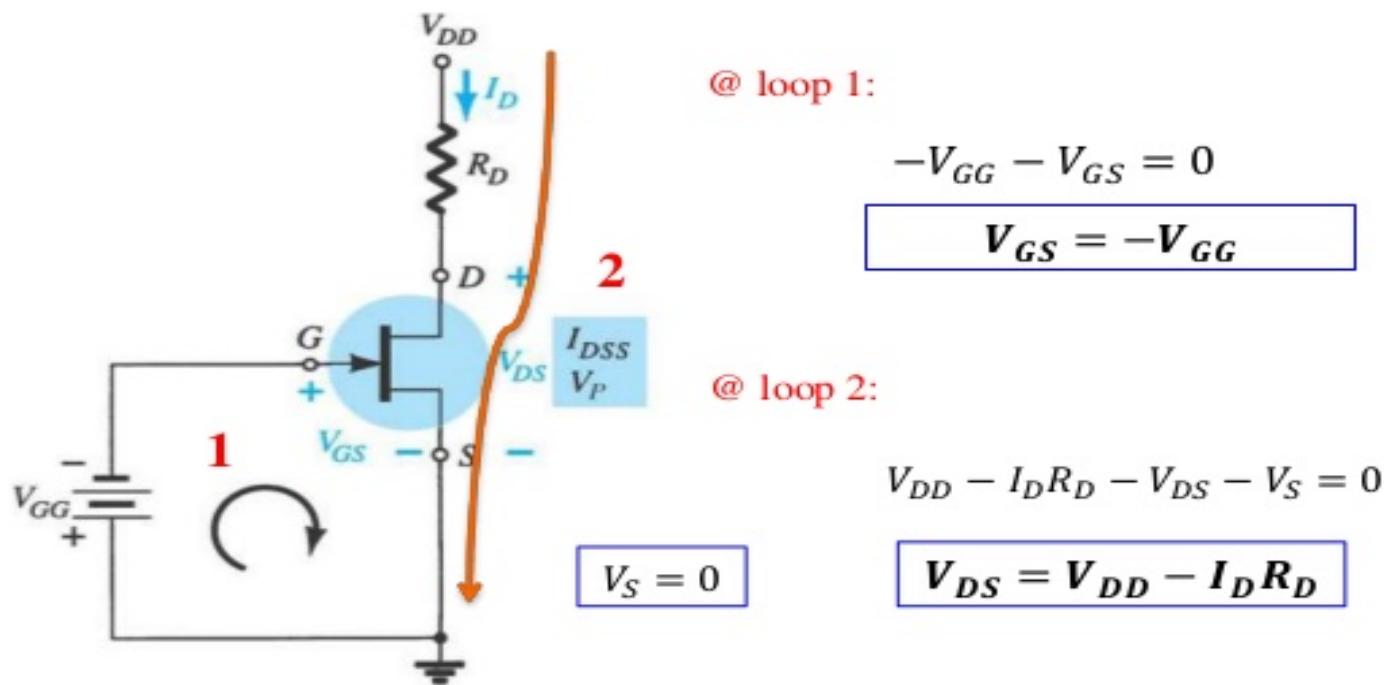
Plotting Shockley's equation.



Finding the solution for the fixed-bias configuration.

$$\begin{aligned}V_{GS} &= 0 \\V_{GS} &= V_p \\V_{GS} &= 0.5 V_p \\V_{GS} &= 0.3 V_p\end{aligned}$$

$$\begin{aligned}I_D &= I_{DSS} \\I_D &= 0 \text{ mA} \\I_D &= I_{DSS}/4 \\I_D &= I_{DSS}/2\end{aligned}$$



Using Double subscript notation:

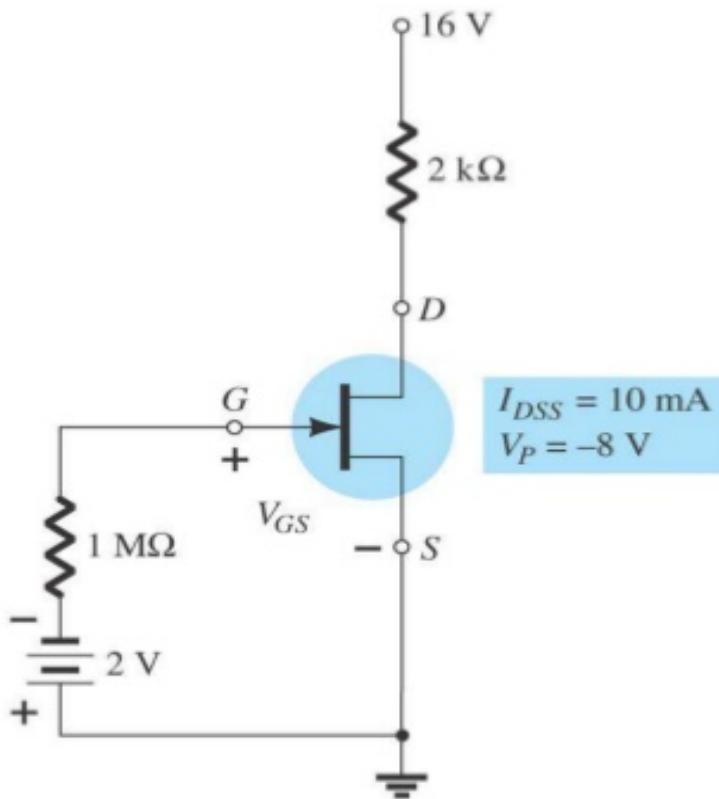
$$V_{DS} = V_D - V_S$$

$$V_{DS} = V_D$$

$$V_{GS} = V_G - V_S$$

$$V_{GS} = V_G$$

For



Find:

$$\begin{array}{ll} V_{GSQ} & V_{DSQ} \\ I_{DQ} & V_D \\ V_G & V_S \end{array}$$

$$\begin{array}{l} I_{DQ} = 5.6 \text{ mA} \\ V_{GSQ} = -2 \text{ V} \\ V_{DSQ} = 4.8 \text{ V} \end{array}$$

Conversely, for a given
 I_D, V_{GS} can be obtained:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

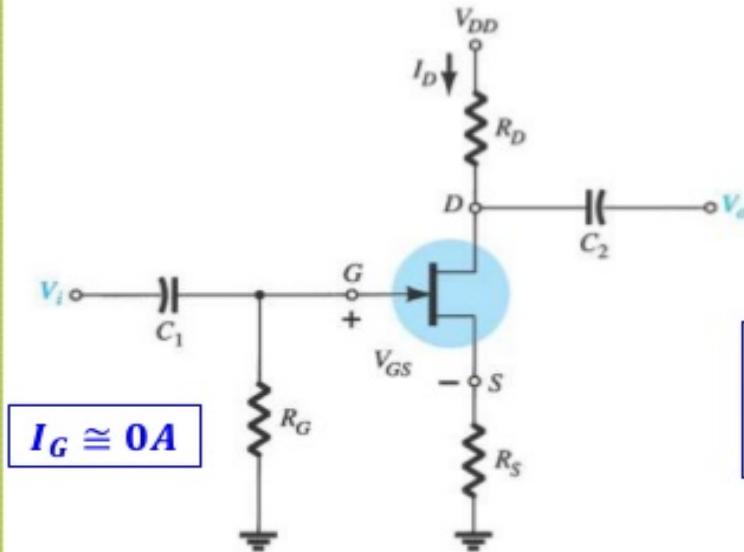
$$V_{GS} = V_p \left(1 - \sqrt{\frac{I_D}{I_{DSS}}} \right)$$

Shorthand Method:

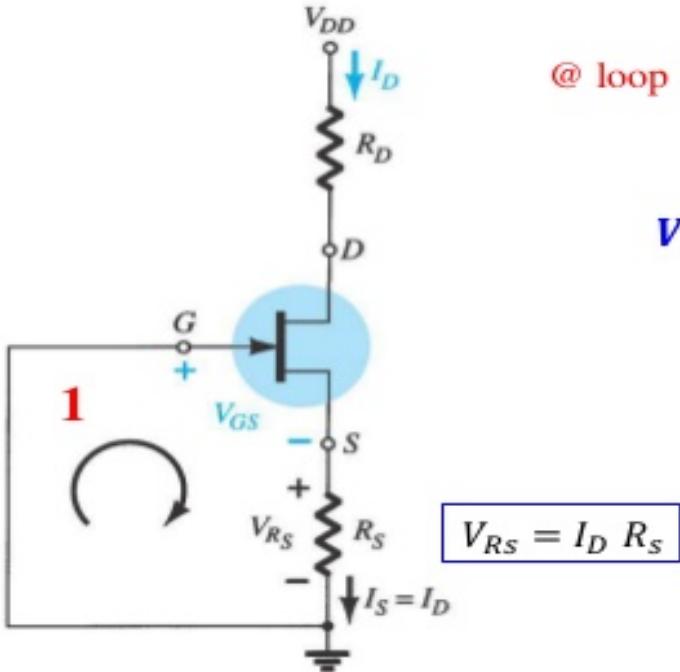
$$I_D = \frac{I_{DSS}}{4} \mid V_{GS} = \frac{V_p}{2}$$

$$V_{GS} \cong 0.3V_p \mid I_D = \frac{I_{DSS}}{2}$$

Self-Bias Configuration



$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$



Note that the current through R_S is the source current, I_S
 But

$$I_D = I_S$$

@ loop 1:

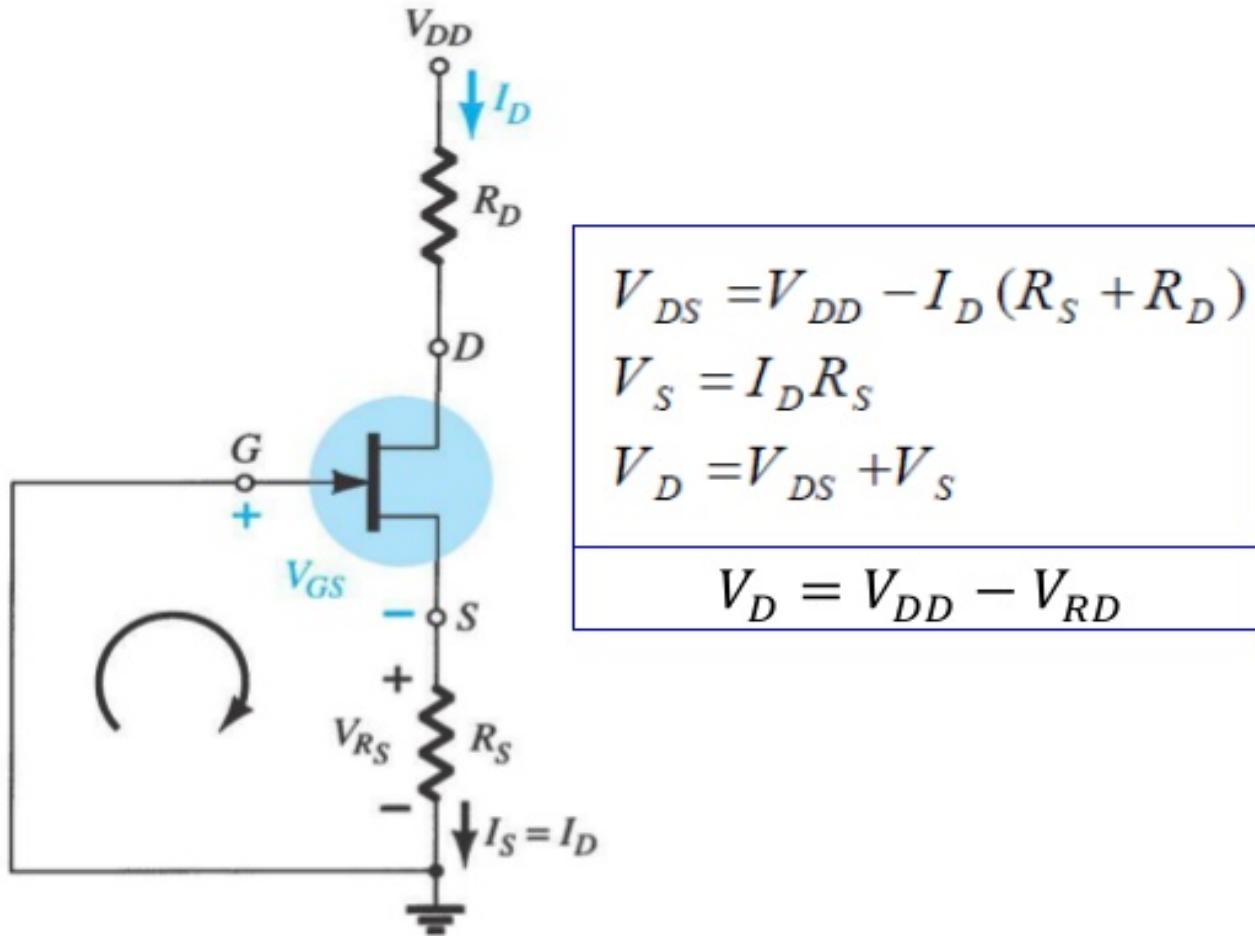
$$-V_{GS} - V_{RS} = 0$$

$$V_{GS} = -V_{RS} = -I_D R_S$$

$$I_D = I_{DSS} \left(1 - \frac{-I_D R_S}{V_p} \right)^2$$

$$I_D = I_{DSS} \left(1 + \frac{I_D R_S}{V_p} \right)^2$$

$$I_D^2 + k_1 I_D + k_2 = 0$$



Thank You