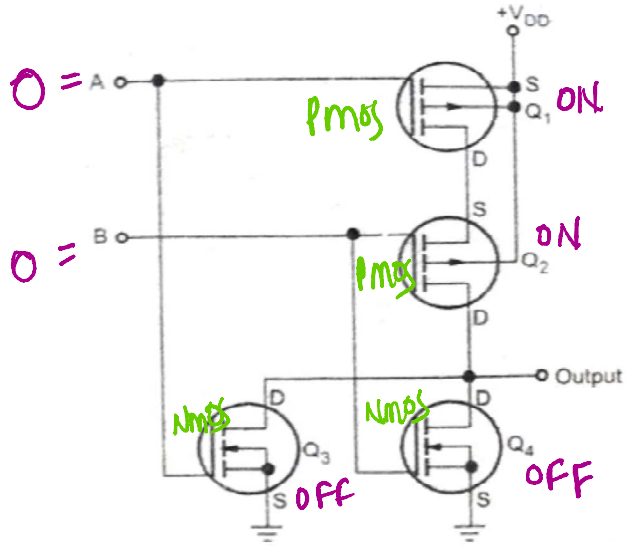
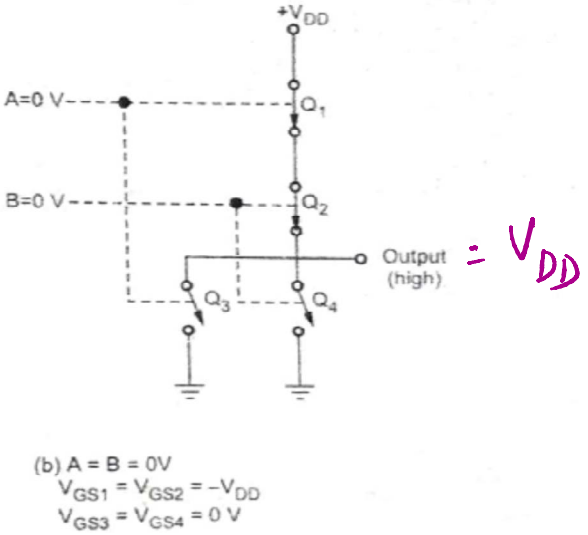
CMOS NOR GATE

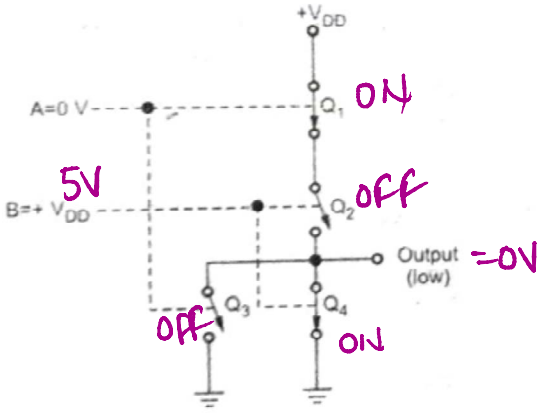


(a) Schematic

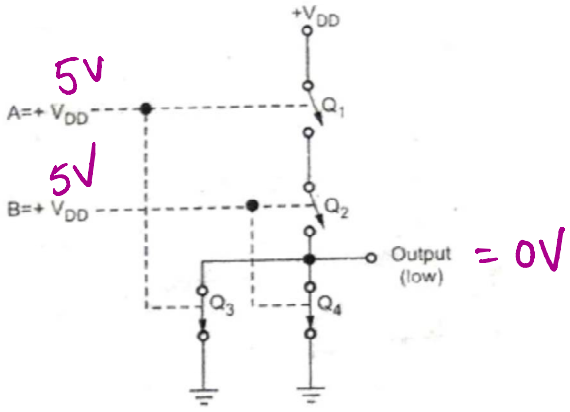


(b) A = B = 0V
$V_{GS1} = V_{GS2} = -V_{DD}$
$V_{GS3} = V_{GS4} = 0$ V

A	B	Q_1	Q_2	Q_3	Q_4
0	0	ON	ON	OFF	OFF
0	5	ON	OFF	OFF	ON
5	0	OFF	ON	ON	OFF
5	5	OFF	OFF	ON	ON



(c) A = 0V, B = $+V_{DD}$
$V_{GS1} = -V_{DD}$
$V_{GS2} = V_{GS3} = 0$ V
$V_{GS4} = +V_{DD}$



(d) A = B = $+V_{DD}$
$V_{GS1} = V_{GS2} = 0$ V
$V_{GS3} = V_{GS4} = +V_{DD}$

A	B	output
0	0	$V_{DD} = 5V$
0	5	0
5	0	0
5	5	0

$\Rightarrow$ NOR gate

CMOS NOR gate $\rightarrow$ PMOS $\rightarrow$ Series
NMOS $\rightarrow$ parallel

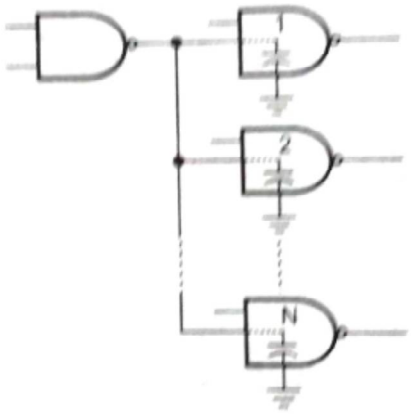


Fig. 7.36 One CMOS output driving several CMOS inputs