Ring Counter and Twisted Ring counter

shift register → D
ring counter
Johnson ring counter } D

Ring Counter

A ring counter is a special type of application of the **Serial IN Serial OUT** Shift register.

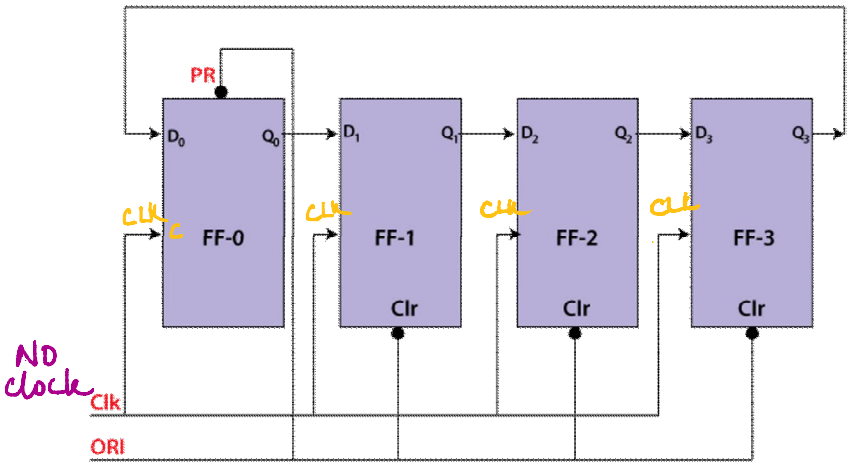
The only difference between the shift register and the ring counter is that the last flip flop outcome is taken as the output in the shift register.

But in the ring counter, this outcome is passed to the first flip flop as an input. All of the remaining things in the ring counter are the same as the shift register.

No. of states in Ring counter = No. of flip-flop used

Below is the block diagram of the 4-bit ring counter. Here, we use 4 **D flip flops**. The same clock pulse is passed to the clock input of all the flip flops as a synchronous counter. The **Overriding input(ORI)** is used to design this circuit.

The Overriding input(Asynchronous input) is used as **clear** and **pre-set**.



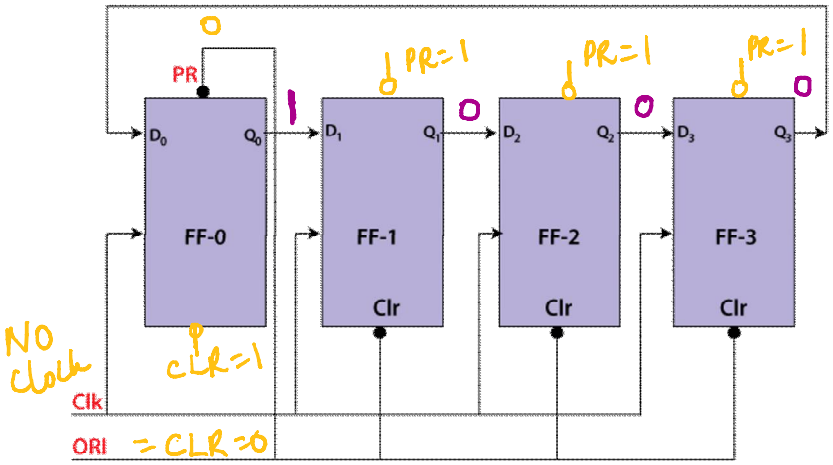
Active loco Asynchronous

FF1, FF2, FF3 } PRESET = 1, CLR = 0

FF0 → PRESET = 0, CLR = 1

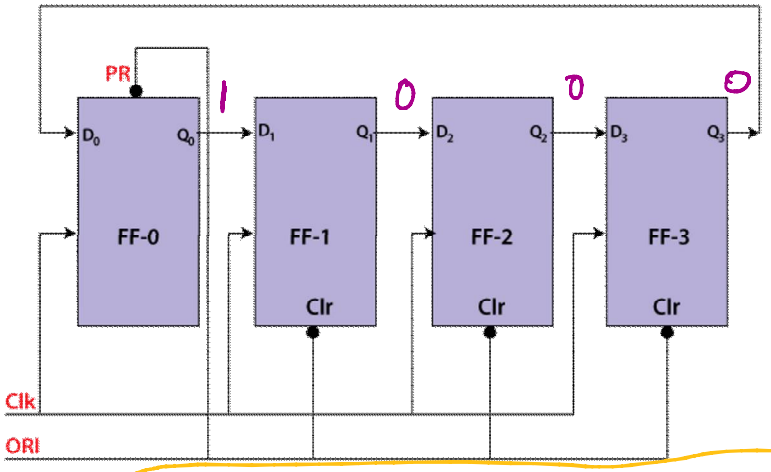
Q_0 Q_1 Q_2 Q_3

The output is 1 when the pre-set set to 0. The output is 0 when the clear set to 0. Both PR and CLR always work in value 0 because they are active low signals.



PR = 0, Q = 1

CLR = 0, Q = 0



D0=Q3	Clock	Q0	Q1	Q2	Q3
0	No clock	1	0	0	0

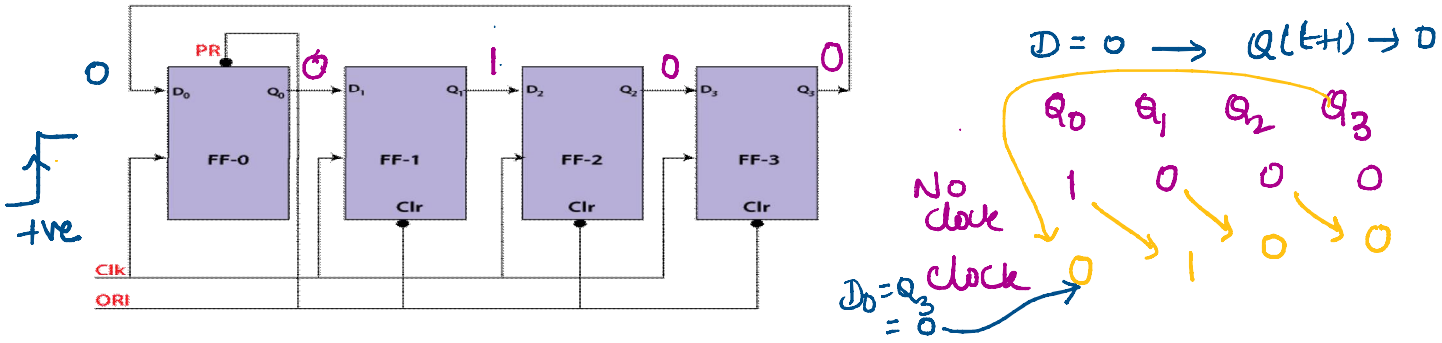
These two values(always fixed) are independent with the input D and the Clock pulse (CLK).

Working

The ORI input is passed to the PR input of the first flip flop, i.e., FF-0, and it is also passed to the clear input of the

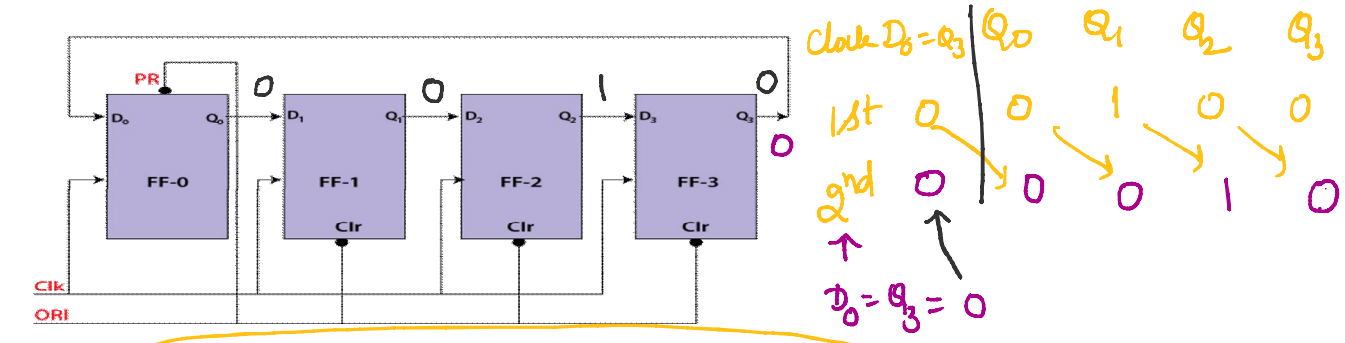
remaining three flip flops, i.e., FF-1, FF-2, and FF-3. The pre-set input set to 0 for the first flip flop. So, the output of the first flip flop is one, and the outputs of the remaining flip flops are 0. The output of the first flip flop is used to form the ring in the **ring counter** and referred to as **Pre-set 1**.

First Clock pulse



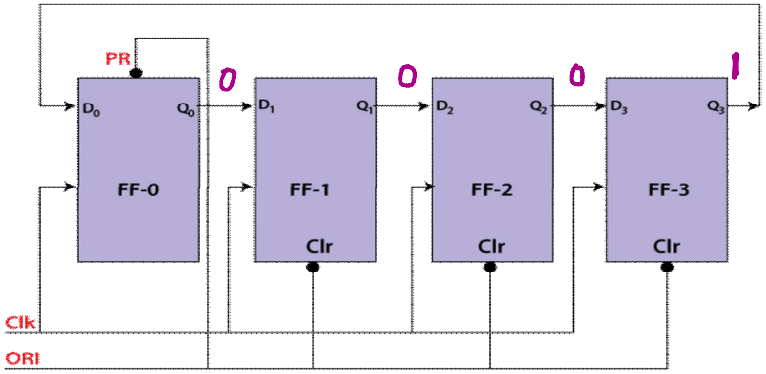
D0=Q3	Clock	Q0	Q1	Q2	Q3
0	↑	0	1	0	0

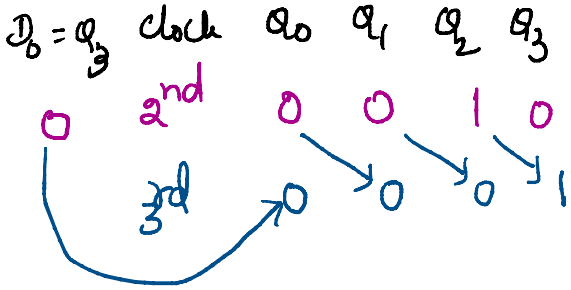
Second Clock pulse



D0=Q3	Clock	Q0	Q1	Q2	Q3
0	↑	0	0	1	0

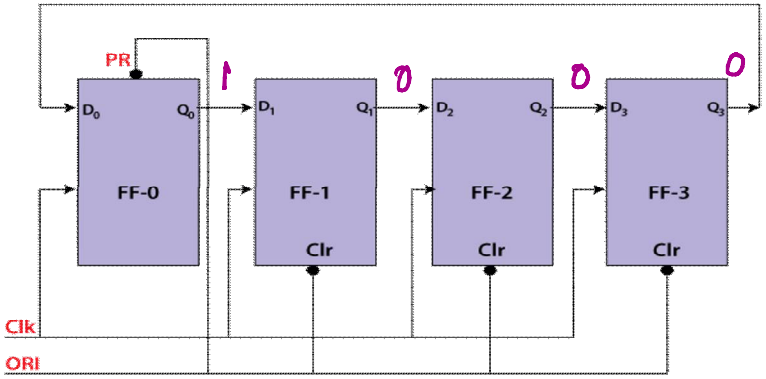
Third Clock pulse

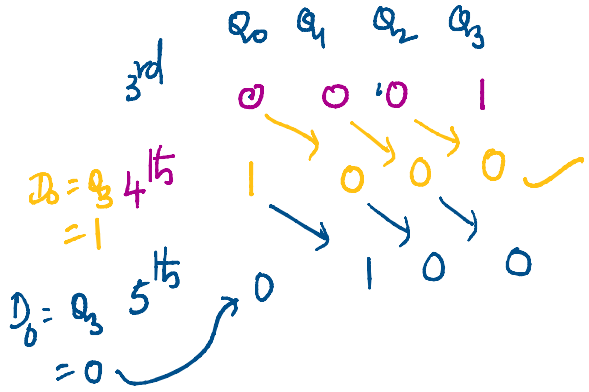




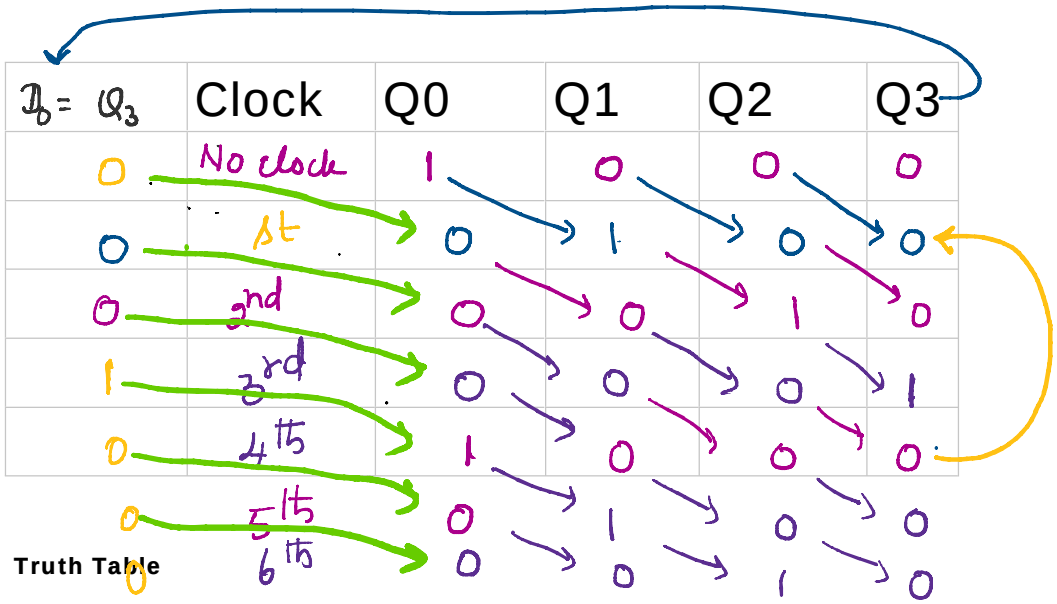
D0=Q3	Clock	Q0	Q1	Q2	Q3
0	3rd	0	0	0	1

Fourth Clock pulse





D0=Q3	Clock	Q0	Q1	Q2	Q3
1	5th	1	0	0	0



Truth Table

ORI	Clk	Q_0	Q_1	Q_2	Q_3
Low	X	1	0	0	0
High	Low	0	1	0	0
High	Low	0	0	1	0
High	Low	0	0	0	1
High	Low	1	0	0	0

Signal Diagram