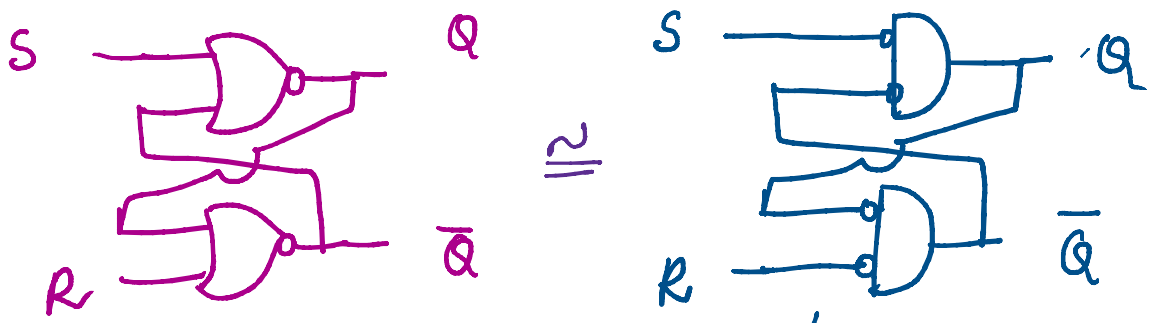
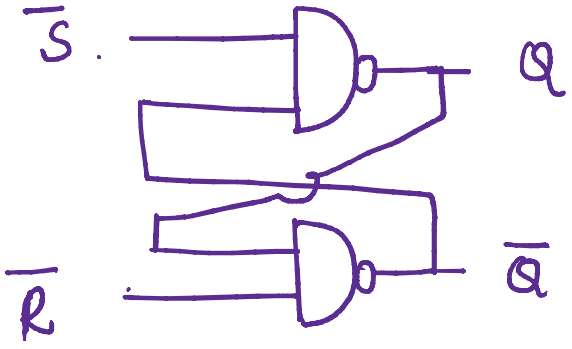
NAND latch and NOR latch

NOR gate

$\overline{A+B} = \overline{A} \cdot \overline{B}$ Demorgans

NOR latch





NOR latch

S	R	Q	Q(t+1)	
0	0	0	0	No change
0	0	1	0	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	x	Not used
1	1	1	x	