

- Electron mechanics is known as Electronics.
- The mechanics of movement of electrons can be done by applying external fields.
- External forces may be electric, magnetic or electromagnetic.
- The behaviour of an electron under the force of external fields is called electronics.
- Electronics is a branch of science & technology which deals with conduction of electricity through a semiconductor.

* Applications of electronics:

- Home appliances
- Entertainment
- Medical purposes
- Industrial purposes
- Communication
 - (a) Wline (b) Wireless
- Defence (DRDO, DRDL, ISRO)
- Satellite communication.

* Electronic device:

- The device in which current flows through a semiconductor is known as electronic device.
- As temp ↑, conductivity of semiconductor ↑

so semiconductor is preferred.

- * Electronic circuits:
 - Connection of elements is known as Circuit.
 - Elements are of 2 types (i) Active (ii) Passive
 - Passive elements are also called linear elements.
They dissipate energy. Eg: R, L, C
 - There is a linear relation b/w applied voltage and resulting current in passive elements. They store energy.
 - Active elements generate the energy and can act as switch, amplifiers etc. Eg: V, I source, diode, transistor, operational amplifier.
 - Electronic circuit is a circuit which contains atleast one electronic component (semiconductor).

- Based on the energy gap, materials are divided into 3 types (i) Insulator (ii) Conductor (iii) Semiconductor.
- Semiconductor is a material whose resistivity is b/w conductor & insulator.
- Semiconductors are of 2 types (i) Intrinsic (ii) Extrinsic
- Pure form of semiconductor is called intrinsic semiconductor.
- Impure form of semiconductor is called extrinsic semiconductor.
- Eg: Silicon, germanium

(c) Note:

- Generally, extrinsic semiconductors are preferred to intrinsic to draw more current.
- There are 2 types of extrinsic semiconductors.
(i) p-type (ii) n-type.
 - When trivalent impurities are added to pure silicon, 3 covalent bonds are formed and 1 covalent bond is left incomplete which represents a hole.
 - If we add more no. of trivalent impurities then more holes are created.
 - Similarly in n-type, adding pentavalent impurities electrons are formed after forming 4 CBs.

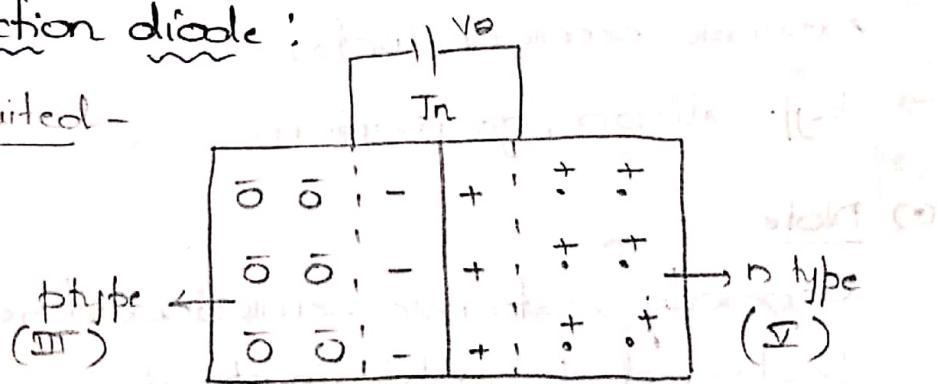
→ To stabilise the element, if CBs are to be formed so p-type acts as acceptor and n-type acts as donor.

(*) Note:

Individual p, n type semiconductors may not give sufficient current. So, they aren't suitable for more applications. To get more current we need to combine them.

* P-n junction diode:

→ open circuited -



→ P-n junction is formed by adding p-type & n-type such a way that resultant one is a single crystal.

→ The imaginary plane which separates p-type & n-type is called p-n junction.

→ While forming p-n junction there exists a conc. difference in crystal, ∴ charge carriers will move randomly.

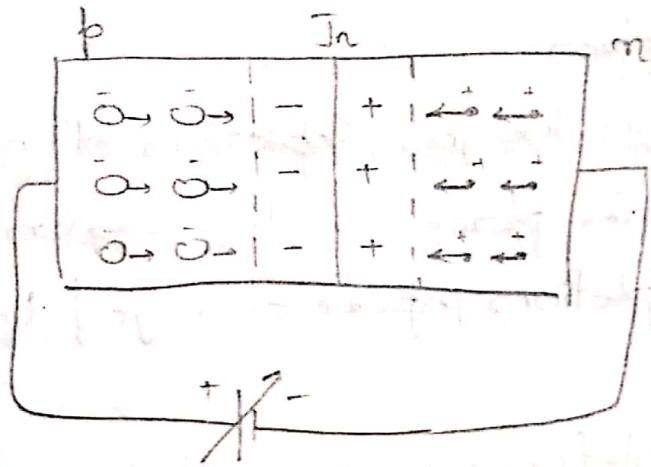
→ Due to the random movement of charge carriers near the junction, e^- & holes recombine

and disappear.

- Hence, near the jn, depletion of charge carriers take place. so the region is called depletion /space charge / transition region.
 - In the depletion region , left side of jn -ve side is present & right side is of +ve charge
 - Due this, voltage is developed. This voltage is called barrier voltage / potential.
 - Due to the charge present in depletion layer, there also exists electric field.

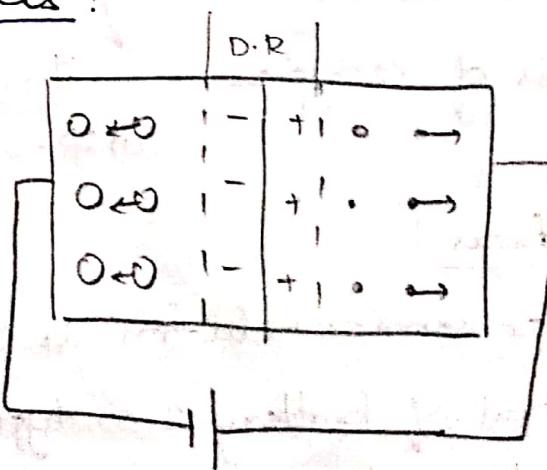
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Monday



- When forward bias is applied to p-n junction, due to the same polarity, repulsion (+ to p, - to n) takes place.
- Thereby, the charge carriers move towards the junction.
- This means, holes diffuse towards n-type, & e⁻s diffuse towards p-type material.
- Due to this (a) depletion layer width, Δs
 (b) Resistance R_s
 (c) Current I_s
- Barrier potential $-V_0$.

(d) Reverse bias:



- When p-type is connected to -ve terminal & n-type is connected to +ve terminal then it is called reverse bias.
- When reverse bias takes place, attraction takes place. So the charge carriers move away from the jn.
- Holes try to attract the -ve terminal & e⁻s try to attract the +ve terminal.
- Due to this, depletion layer width \propto , resistance \propto , current at jn \propto (~ 0)
- When reverse bias is applied, the minority charge carriers move towards the jn, so current exists that is called leakage / reverse / reverse saturation current.
- It is represented as I_0 or I_s .
- The diode current equation is $I = I_0(e^{\frac{V}{nV_T}} - 1)$

where I = diode current

I_0 = Reverse Current

V = Applied voltage

n = 1 for Ge, 2 for Si

V_T = Volt equivalent temperature
 $\approx 26mV$ or $25mV$

$$V_T = \frac{kT}{q}$$

* V-I characteristics:

As we know that diode equation,

$$I = I_0 (e^{\frac{V}{nV_T}} - 1)$$

Case-1:

$$V > 0 \Rightarrow I > 0$$

Case-2:

if $V > +V_e$ i.e., forward bias

$$I = I_0 (e^{+V_e} - 1)$$

$$e^{+V_e} \gg 1 \text{ (neglect } 1\text{)}$$

$$I = I_0 e^{+V_e}$$

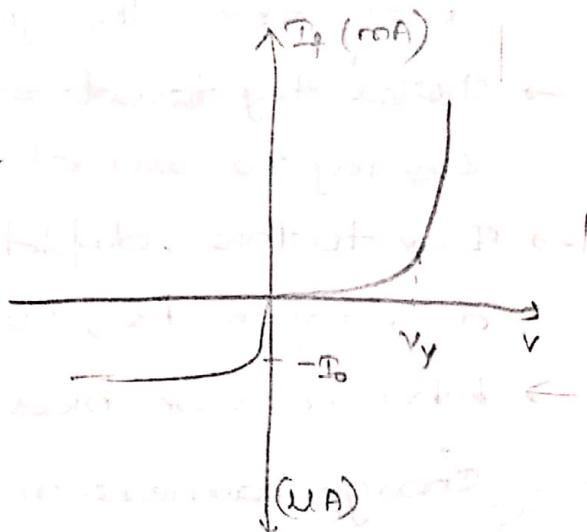
Case-3:

$V < -V_e$ i.e., reverse bias

$$I = I_0 (e^{-V_e} - 1)$$

$$e^{-V_e} \ll 1 \text{ (neglect } e^{-V_e}\text{)}$$

$$I \approx -I_0$$



* Diode Current equation:

→ When forward bias

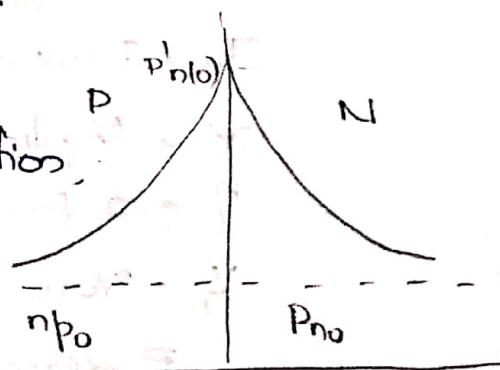
is applied onto PN junctions,

holes diffuse into n-type,

e's into p-type. Hence,

minority charge carrier

Conc. ↑s.



→ Before applying forward voltage, minority charge conc. is n_{n0} in n-type & after applying

is $P_n(0)$

$$\Rightarrow P_n(x) = P_{n0} + P'_n(x)e^{-x/L_p}$$

(As minority charge conc. Is as distance \uparrow)

At $x=0$,

$$P_n(0) = P_{n0} + P'_n(0)$$

$$P'_n(0) = P_n(0) - P_{n0} \quad \text{--- (1)}$$

The overall conc. in n-type material \uparrow exponentially,

$$\Rightarrow P_n(x) = P_{n0} \cdot e^{\frac{x}{L_p}} \quad \text{--- (2)}$$

As we know that, the diffusion current is directly \propto to the rate of change of charge carriers

$$I_{\text{pdif}} \propto \frac{dp}{dx} = -Aq_D p \frac{dp}{dx}$$

$$\Rightarrow I_{\text{pdif}} = \frac{A \cdot q_D p}{L_p} P'_n(0)$$

$$= \frac{A \cdot q_D p}{L_p} [P_n(0) - P_{n0}]$$

$$= \frac{A \cdot q_D p}{L_p} [P_{n0} e^{\frac{x}{L_p}} - P_{n0}]$$

$$= \frac{A \cdot q_D p}{L_p} P_{n0} [e^{\frac{x}{L_p}} - 1]$$

$$\text{Hence } I_{\text{ndif}} = \frac{A \cdot q_D p}{L_p} n_{p0} [e^{\frac{x}{L_p}} - 1]$$

$$I_{\text{total}} = I_{\text{pdif}} + I_{\text{ndif}}$$

$$I = c^{\frac{1}{V_{AT}} - 1} \left[\frac{A q D_p}{4p} P_{no} + \frac{A q D_n}{4n} n_{p_0} \right]$$

$$I \rightarrow I_o (e^{\frac{1}{V_{AT}} - 1})$$

The above eq. is valid for ideal diode only.

For the general diode $\Rightarrow I \rightarrow I_{fe} e^{\frac{1}{\eta V_{AT}} - 1}$

where $\eta > 1$ for Ge

= 2 for Si

26/5/2019

Friday

* Diode resistance:

- The ideal diode has zero forward resistance and ' ∞ ' reverse resistance.
- The practical diode will give minimum resistance in forward bias and maximum resistance in reverse bias.
- There are two types of resistances (i) forward (ii) Reverse resistance

(i) Forward resistance,

- The resistance offered by the diode when it is operated in FB.
- It is of 2 types .(i) Static forward
(ii) Dynamic forward

(i) Static forward resistance : $(R_f) = V/I$

- The resistance offered by the diode when it

is operated in forward bias with DC condition (constant or stable).

- (ii) Dynamic forward resistance:
- The resistance offered by the diode when it is operated in forward bias with DC changing condition. (Two points)

$$\gamma_F = \frac{\Delta V}{\Delta I} = \frac{V_2 - V_1}{I_2 - I_1}$$

$$\gamma_F = \frac{dv}{di}$$

As we know that,

$$I = I_0 (e^{V/nT} - 1) \quad \text{(1)}$$

By differentiating eq(1) w.r.t 'v';

$$\frac{dI}{dv} = I_0 e^{V/nT} \cdot \frac{1}{nT}$$

$$\frac{dv}{dI} = \frac{nT}{I_0 e^{V/nT}} = \gamma_F$$

$$\Rightarrow \gamma_F = \frac{nT}{I + I_0} \quad (\text{from eq(1)})$$

$I \ggg I_0$

$$\Rightarrow \boxed{\gamma_F = \frac{nT}{I}}$$

• Reverse resistance:

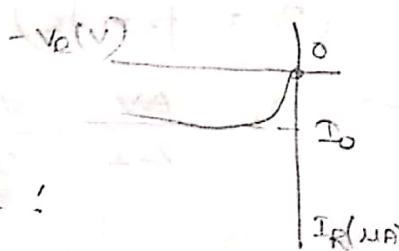
- The resistance offered by the diode when it is operated in RB is called reverse resistance.

→ It is of 2 types : (i) Static reverse
(ii) Dynamic reverse.

(i) Static reverse resistance :

→ The resistance offered by the diode when it is operated in RB with DC condition is called static reverse resistance.

$$R_s = \frac{V_r}{I_r} = M \Omega$$

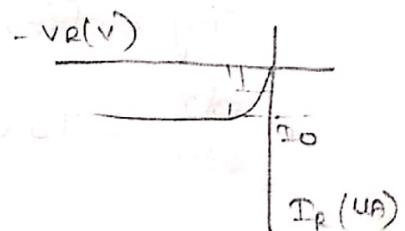


(ii) Dynamic reverse resistance :

The resistance offered by the diode when it is operated in RB with AC condition is called dynamic reverse resistance.

$$r_d = \frac{dV}{dI} = \frac{V_2 - V_1}{I_2 - I_1} \text{ mly}$$

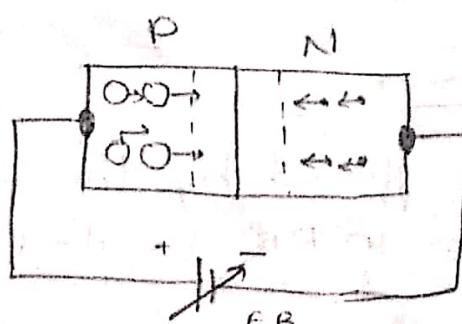
$$r_d \approx \infty$$



* Diode reverse capacitance :

→ There are 2 types of capacitance exist in a diode (i) Diffusion capacitance (C_D)
(ii) Transition capacitance (C_T)

(i) Diffusion capacitance :



- This is forward bias capacitance.
- If the p-n junction is forward biased, the majority charge carriers move towards the junction, then there exists a change in charge which represents capacitance.
- Hence, this is called FB capacitance (capacitance exists due to the diffusion of charge carriers).
- Represented with $C_D = \frac{dQ}{dv}$ — (1)

$$I = \frac{dQ}{dt}$$

$$dI = \frac{dQ}{dt} \quad (dt \rightarrow T)$$

$$\Rightarrow dI = \frac{dQ}{T}$$

$$\Rightarrow dQ = T \cdot dI \quad (2)$$

Sub eq(2) in eq(1)

$$C_D = T \cdot \frac{dI}{dv}$$

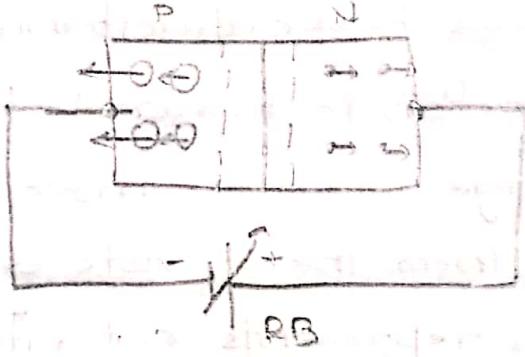
$$C_D = T \cdot \frac{d}{dv} [D_0 (e^{\frac{V}{nV_T}} - 1)]$$

$$C_D = T \cdot \frac{I}{\eta V_T} \Rightarrow C_D = \frac{T I}{\eta V_T}$$

→ Diffusion capacitance is directly \propto to current I and inversely \propto to temperature.

(ii) Transition Capacitance:

- If the p-n junction is reverse biased, the majority charge carriers move away from



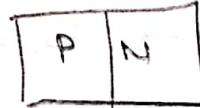
the jn. and change in charge takes place which represents capacitance.

- Hence, this is called RB capacitance.

$$C_R = \frac{dQ}{dv} \quad (1) \text{ Total charge in region is given by,}$$

$$Q = q \cdot N_D \cdot A \cdot W$$

$$\frac{dQ}{dv} = q \cdot N_D \cdot A \cdot \frac{dW}{dv} \rightarrow @$$



$$N_p \gg N_D$$

From poisson's equation, then $w_p \ll w_n$

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\epsilon} \quad (2)$$

$x = W$ = width of transition region

By integrating eq (2) w.r.t x

$$\text{we get } \frac{dV}{dx} = -\frac{\rho}{\epsilon} \cdot x$$

$$\Rightarrow \frac{dx}{dV} = -\frac{\epsilon}{\rho x}$$

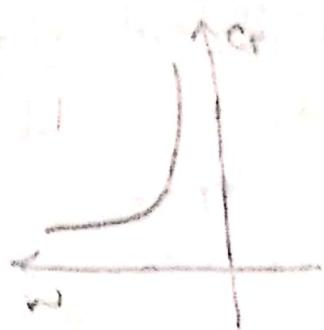
$$\Rightarrow \frac{dw}{dv} = -\frac{\epsilon}{\rho w}$$

$$\Rightarrow \frac{dw}{dv} = -\frac{\epsilon}{q N_D w} \quad (3)$$

sub (3) in ①

$$\frac{dQ}{dv} = C_T \approx q \cdot N_D \cdot N_S = \frac{-E}{q \cdot N_D \cdot W}$$

$$\left[C_T \approx \frac{EN}{W} \right] **$$



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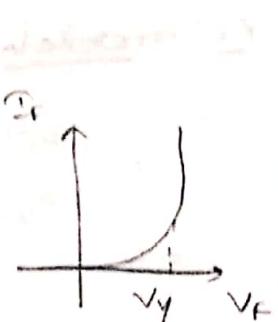
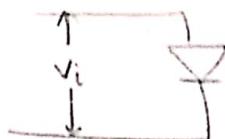
Tuesday

* Diode equivalent model:

DC models:

1. Exponential model :-

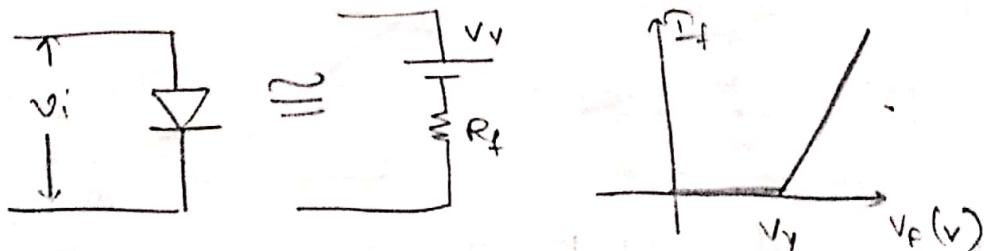
$$\text{on w.r.t. } T \rightarrow I_o e^{V/2kT}$$



2. Piecewise linear model:

→ It is obtained from exponential model.

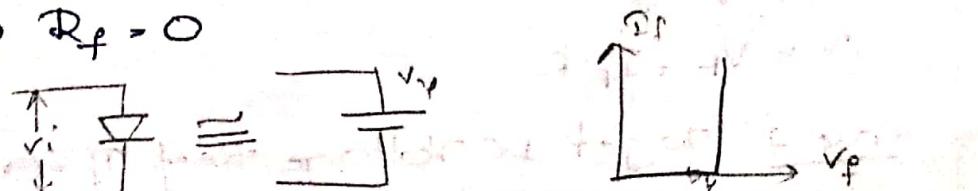
→ After cut-in voltage, the characteristics are linear but overall charac. are nonlinear.



3. Constant voltage drop model:

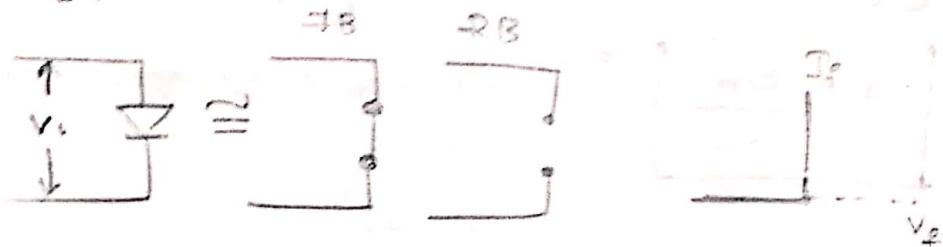
If it is obtained from piecewise linear model

with $R_f = 0$



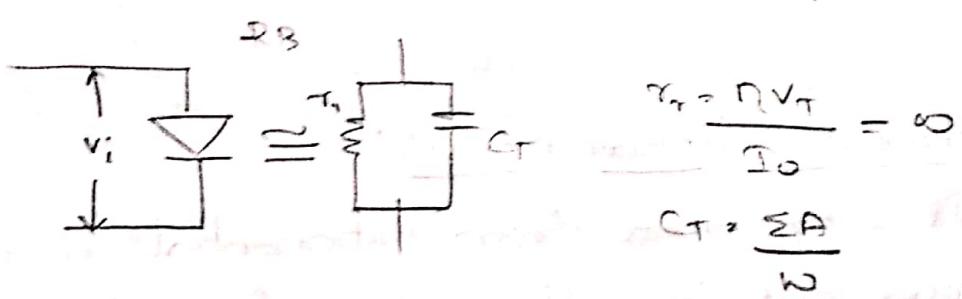
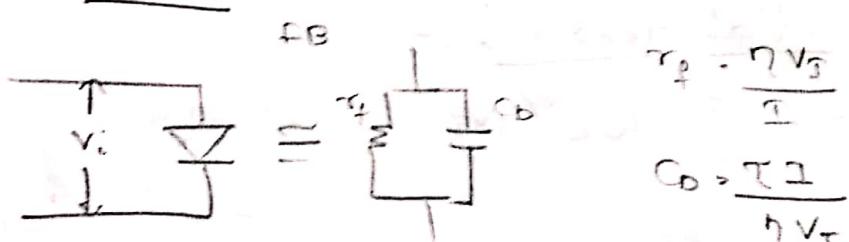
4. Ideal diode model:

→ It is obtained from the above model with $V_T = 0$.

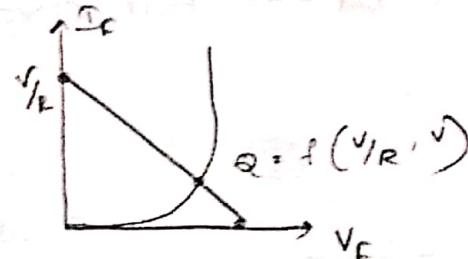
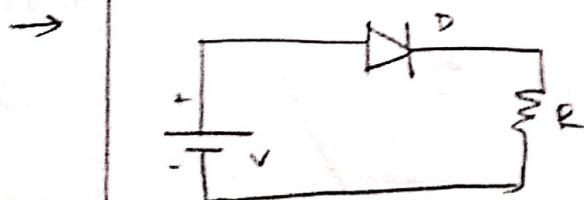


(*) Note: Among the above 4 models, we prefer constant voltage drop model to solve problems.

AC model:



* Load line analysis:



→ It is a straight line joins two DC points i.e., DC voltage, DC current.

→ By applying KVL to above circuit,

$$V = V_f + I_f \cdot R$$

Case-1: To get DC voltage keep $I_f = 0$

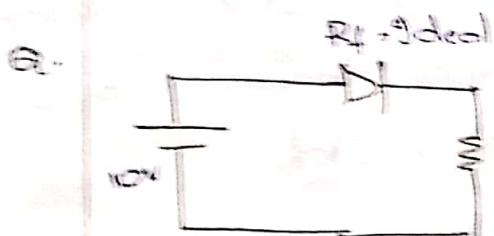
we get $V = V_F$

Ques - 2: To get DC current keep $V_F = 0$

$$V = I_F R$$

$$\Rightarrow I_F = \frac{V}{R}$$

- Q point is also known as operating point / quiescent point / optimum point.
- Q point is a pt. of intersection of DC load line and characteristic curve.



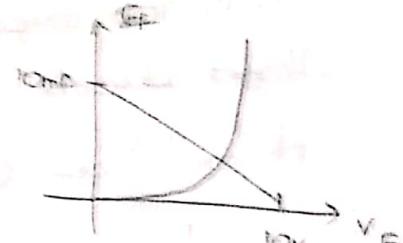
apply KVL,

$$10 = V_F + I_F(10^3)$$

$$\Rightarrow 10 = V_F + 1000I_F$$

put $V_F = 0$ then $I_F = 0.01 A$.

put $I_F = 0$ then $V_F = 10V$



- Q. Silicon diode is operated at room which gives $V_F = 0.7V$, $I_F = 4mA$ if voltage is changed to 0.74V then find I_F

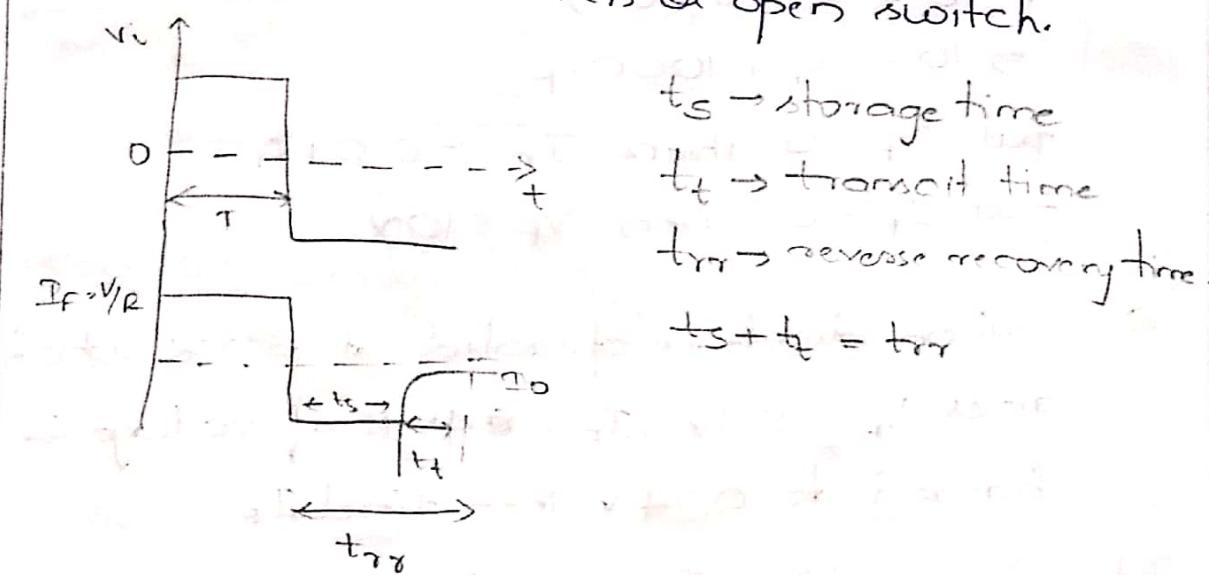
Sol: $V_F = 0.7V$ $I_F = 4mA$

$V_F^{\circ} = 0.74V$ $I_F^{\circ} = ?$

$$I = I_0(e^{\frac{V_F}{nV_T}} - 1)$$

$$4 \times 10^{-3} \cdot 20 \left(e^{\frac{0.74}{26 \times 10^{-3}}} - 1 \right)$$

- * Diode applications:
- 1. Diode as switch:
- If the input voltage is $>$ than cut in voltage (V_F), the diode D gets into forward bias mode and it acts as ON switch.
- When the diode input voltage is $<$ than V_F then diode D gets into R.B mode and it acts as OFF switch or open switch.



- During +ve cycle, diode D gets into FB mode and $I_F > V/R$
- At $t = T$, the input voltage suddenly falls down & becomes -ve, due to this the same current flows in opposite direction.

After some time it may reach to reverse current.

- (*) Storage time: Time taken to remove excess minority charge carriers is called storage time.
- (*) Turn-off time: Time elapsed in returning to reverse bias mode is called transit time.
- (*) Reverse recovery time: Time taken by the response to switch OFF state from ON state is called reverse recovery time / OFF time.
- (*) Forward recovery time: Time taken by the diode to reach OFF ON state from OFF state is called forward recovery time - (t_{fr}).

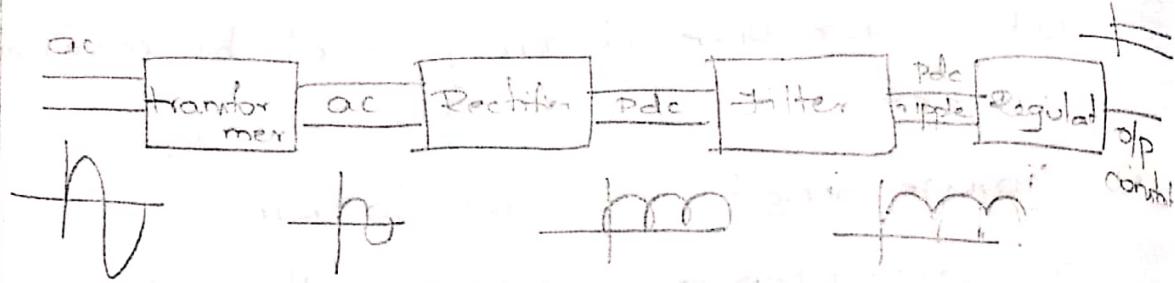
$$t_{rr} \gg t_{fr}$$

8/8/2019

Friday

② Diode as rectifier:

- Power is generated & distributed, transmitted in the form of AC, but most of electronic equipments use DC supply to operate. Hence AC supply can be utilised in a proper manner.
- This can be done by regulated power supply.
- There are 2 types of power supplies.
 - (i) Linear mode
 - (ii) Switched mode.
- (i) Linear mode power supply:
 - It consists of 4 blocks.



(c) Transformer:

- It transfers the ac signal.
- The output of transformer may be with fed amplitude or ↓ed amplitude.
- Based on this, transformers are divided into 2 types (i) Step up (ii) Step down.
 $(v_2 > v_1)$ $(v_2 < v_1)$

Note: In regulated power supplies, generally we prefer step down transformer.

(c) Rectifier:

- It is circuit which converts ac to pulsating dc (dc + ac - unwanted components)
- There are 2 types (i) half wave

(ii) Full wave → with
Centre tapped
transformer
bridge rectifier

(c) Filter:

- It removes unwanted components i.e., ac
- It allows only certain range of frequencies and attenuates other frequencies.
- In a regulated power supply, filters are constructed by passive elements (L, C)

- There are 4 types of filters. They are:
 - (i) Shunt capacitor
 - (ii) Series inductor
 - (iii) LC film filter or L-section filter
 - (iv) CLC filter or T-section filter

(c) Rectifiers Regulation:

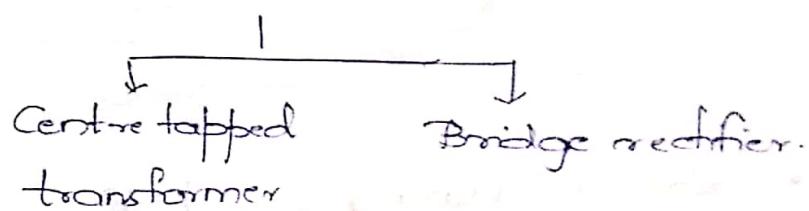
- It is a circuit that gives constant output voltage irrespective of voltage & load variations.

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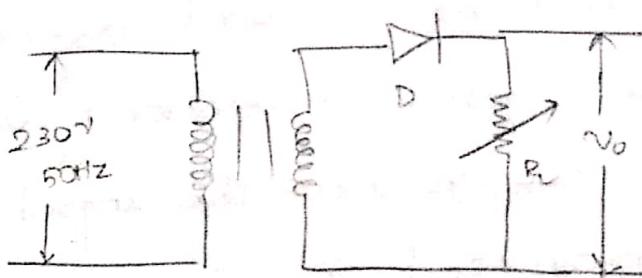
Tuesday

* Rectifier:

- AC → pulsating DC
- It is of 2 types (i) Half wave
(ii) Full wave



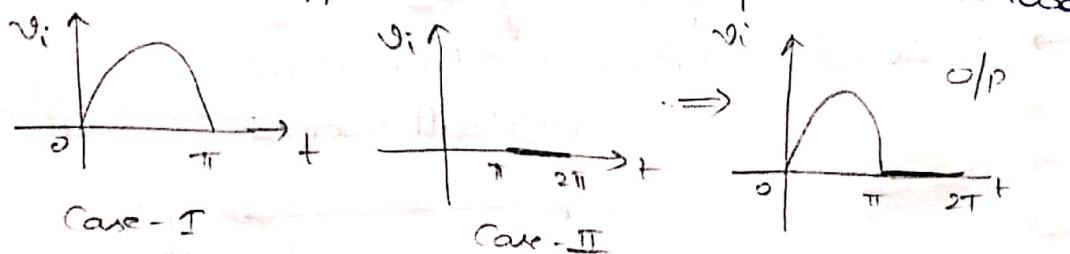
2. Half wave rectifier:



- It is a rectifier in which AC signal is converted to pulsating dc during half period of input sig.
- It consists of diode, step down

transformer, load resistance.

- (*) Case-I: During +ve cycle of input signal.
- When power supply is switched on, ac signal is transmitted to transformer and it appears at the secondary winding with decreased voltage or amplitude.
 - In this case, transformer secondary winding upper end is made +ve w.r.t lower end +ve;
 - Hence diode D gets into forward bias mode and it acts like ON switch or closed switch then the input signal can be transmitted through the diode & appears as an output at the load.



- (*) Case-II: During -ve half cycle of input.
- In this case, transformer secondary winding upper end is made -ve w.r.t lower end.
 - Hence, diode D gets into reverse bias & acts like a open switch then the input signal can't be transmitted. Therefore the output at the load is zero.

(c) Analysis:

(i) Peak current (I_m):

The maximum current is called peak current.

$$I_m = \frac{V_m}{R_L + R_f + R_s}$$

where V_m = peak voltage

R_f , R_s can be neglected.

(ii) Peak inverse voltage:

- The maximum reverse voltage at which the diode can withstand without destroying the junction is called peak inverse voltage (PIV).
- For half wave rectifier, PIV = V_m .

(iii) Average voltage or DC voltage:

- The average voltage can be calculated by

$$\begin{aligned} \frac{1}{2\pi} \int_0^{2\pi} V_i(t) dt &= \frac{1}{2\pi} \int_0^{2\pi} V_m \sin \omega t dt \\ &= \frac{V_m}{2\pi} [\cos \omega t]_0^{2\pi} \\ &= \frac{V_m}{2\pi} [0] = 0 \end{aligned}$$

- For full wave, Avg $V_d = 0$.

- For half wave,

$$V_{DC} = \frac{1}{2\pi} \left[\int_0^{\pi} V_m \sin \omega t dt \right]$$

$$V_{DC} = \frac{V_m}{\pi}$$

(iv) DC current or Average Current:

If we place DC ammeter in the circuit, it may not respond for the fluctuating current in AC supply.

Hence Avg. Current is calculated by

$$I_{DC} = \frac{1}{2\pi} \int_0^{2\pi} I_m \sin \omega t dt$$

$$I_{DC} = \frac{I_m}{\pi}$$

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Friday

(v) RMS Voltage (V_{rms}):

$$V_{rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} V_m^2 \sin^2 \omega t dt} \quad (\text{from } 0 \text{ to } 2\pi \text{ w.r.t. } \omega t \text{ is zero - for HWR})$$

$$= \sqrt{\frac{V_m^2}{2\pi} \left[\int_0^{\pi} \sin^2 \omega t d\omega t \right]}$$

$$= \sqrt{\frac{V_m^2}{2\pi} \cdot \frac{\pi}{2}} = \frac{V_m}{2}$$

(vi) RMS Current:

$$\text{Hence } I_{rms} = \frac{I_m}{2}$$

(vii) Efficiency (η):

It is defined as the ratio of DC power delivered to the AC power.

$$\eta \rightarrow \frac{P_{dc}}{P_{ac}} \times 100$$

$$\rightarrow \frac{P_{dc}}{P_{ac}} = \frac{V_{dc} \times I_{dc}}{\text{Vrms} \cdot I_{rms}} \times 100$$

$$= \frac{\frac{V_m}{\pi} \times \frac{I_m}{\pi}}{\frac{V_m}{2} \cdot \frac{I_m}{2}} \times 100$$

$$\Rightarrow \frac{4}{\pi^2} \times 100 = 40.6\%$$

- (c) Note: A half wave rectifier converts ac power to dc power with 40.6% efficiency and the remaining power is wasted. Hence, HWR is not preferred in power supplies.

(viii) TUF: Transformer utilization factor:

- It is used to determine the rating of transformer.
- It is defined as the ratio of dc power delivered to the load to the ac rated power.

$$\text{TUF} = \frac{P_{dc}}{P_{ac \text{ rated}}}$$

$$V_{ac \text{ rated}} = \frac{V_m}{\sqrt{2}}$$

$$I_{ac \text{ rated}} = \frac{I_m}{2}$$

$$= \frac{\frac{V_m}{\pi} \times \frac{I_m}{\pi}}{\frac{V_m}{\sqrt{2}} \times \frac{I_m}{2}} \times \frac{\frac{2\sqrt{2}}{\pi^2}}{100} = 0.2865$$

$$\Rightarrow 0.287 \times 100$$

$$\Rightarrow \boxed{28.7}$$

**

(*) Relation b/w η and TUF:

$$TUF = \frac{P_{dc}}{P_{ac\text{rated}}}$$

Disadvantages of HWR:

1) η is less.

2) γ is more.

3) TUF is less.

$$= \frac{P_{dc}}{P_{ac}} \times \frac{P_{ac}}{P_{ac\text{rated}}}$$

$$= \eta \cdot \frac{V_{rms} I_{rms}}{V_{ac\text{rated}} \cdot I_{ac\text{rated}}}$$

$$TUF = \frac{1}{\sqrt{2}} \eta$$

$$\rightarrow TUF = 0.707\eta$$

(ix) Ripple factor: (γ)

→ As we know that, rectifier output consists of ac and dc, ac components are unwanted components. These ac components can be measured by a factor known as ripple factor.

$$\gamma = \frac{I_{rms}}{I_{dc}}$$

Advantages of HWR:

1. Circuit is simple.

2. Less Cost.

$$I_{rms} = \sqrt{I_{dc}^2 + I_{ac}^2}$$

$$I_{rms} = \sqrt{I_{rms}^2 - I_{dc}^2}$$

$$\gamma = \sqrt{\frac{I_{rms}^2 - I_{dc}^2}{I_{dc}^2}}$$

$$= \sqrt{\frac{I_{rms}^2}{I_{dc}^2} - 1}$$

$$\gamma = \sqrt{\frac{\left(\frac{V_m}{2}\right)^2}{\left(\frac{V_m}{\pi}\right)^2} - 1} = \sqrt{\frac{\pi^2}{4} - 1} = 1.21$$

→ In a half wave rectifier, ripple content is 1.21 which is drawback.

(x) Form factor:

$$F.F = \frac{V_{rms}}{V_{avg}} = \frac{V_m}{\frac{V_m}{2}} = \frac{2}{\pi} = 1.57$$

(xi) Peak factor:

→ It is ratio of the peak value to the rms value. P.F. = $\frac{V_m}{V_{rms}} = \frac{V_m}{\frac{V_m}{2}} = 2$.

(xii) % Regulation:

$$\% R = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

$$V_{NL} = V_{DC} = \frac{V_m}{\pi}$$

$$V_{FL} = V_{DC} - I_{DC}(R_f + R_s)$$

$$\% R = \frac{V_{DC} - V_{DC} + I_{DC}(R_f + R_s)}{V_{DC} - I_{DC}(R_f + R_s)} \times 100$$

$$= \frac{I_{DC}(R_f + R_s)}{V_{DC} - I_{DC}(R_f + R_s)} \times 100$$

$$\% R = \frac{\frac{I_m}{\pi} (R_f + R_s)}{\frac{V_m}{\pi}} \times 100$$

$$\frac{V_m}{\pi} = \frac{I_m}{\pi} (R_f + R_s)$$

$$\% R = \frac{\frac{I_m (R_f + R_s)}{\pi}}{\frac{V_m - I_m (R_f + R_s)}{\pi}} \times 100$$

$$= \frac{\frac{I_m (R_f + R_s)}{\pi}}{\frac{I_m (R_f + R_s) + I_m R_L - I_m (R_f + R_s)}{\pi}} \times 100$$

$$\% R = \frac{\frac{R_f + R_s}{R_L}}{\pi} \times 100$$

- Q. FWR with $V_{input} = 220V$ uses a single diode with $R_s = 100\Omega$, $R_L = 2k\Omega$ then find (i) I_m
(ii) V_{DC} (iii) I_{DC} (iv)

Sol: $V_{rms} = 220V$

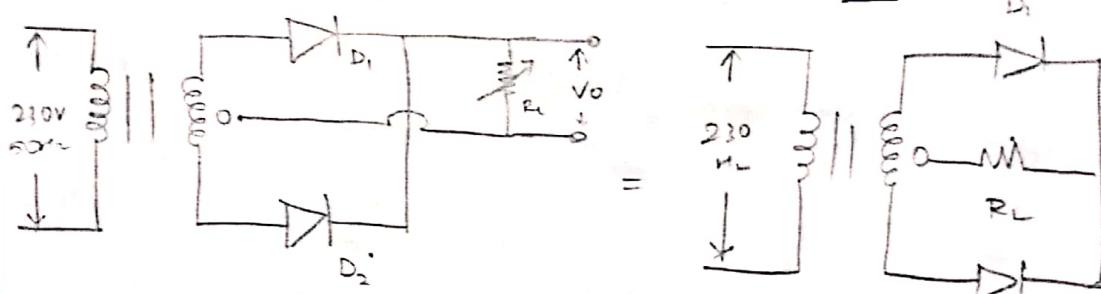
$$V_m = \sqrt{2} \times 220 = 311.12V$$

$$I_m = \frac{V_m}{R_s + R_L} = \frac{311.12}{2100} = 0.1481A$$

* Full wave rectifier:

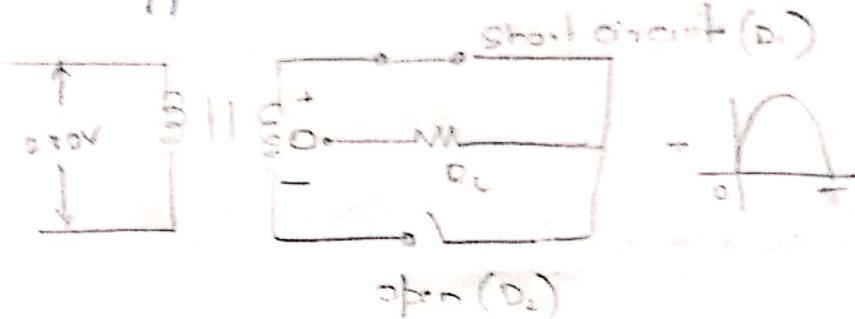
- Rectifier which converts ac to pulsating dc during full period of the ac signal.
- There are 2 types of FWR.
 - (i) With centre tapped transformer.
 - (ii) Bridge Rectifier.

(i) FWR with centre tapped transformer:

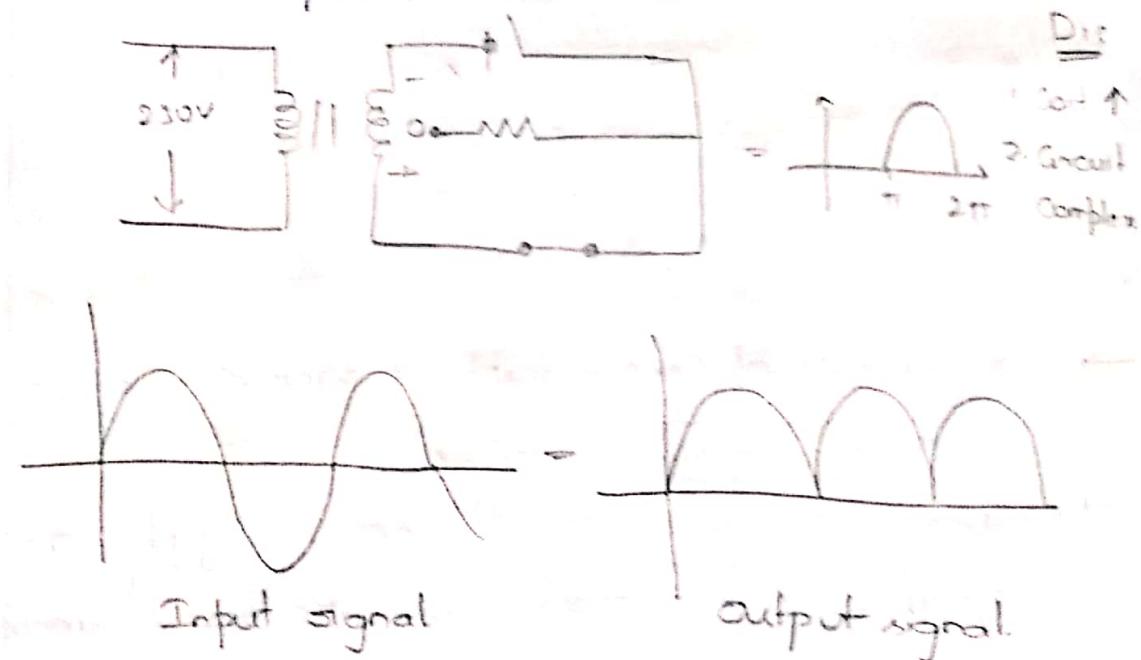


- It consists of centre tapped transformer, two diodes, load resistor.
- When we switch on the power supply, ac signal is transmitted from the transformer to the secondary winding.
- During +ve half cycle of the input signal waveform transformer secondary winding upper end is made +ve to the lower end. Hence D₁ gets forward biased and D₂ into reverse bias.
- So D₁ acts as ON switch, so input signal

$0-\pi$ is appeared at the output.



- During the -ve half cycle, the secondary winding upper end is made -ve w.r.t. lower end. Hence D_1 gets into forward bias and D_2 gets into reverse bias.
- So the input signal, $\pi - 2\pi$ +ve cycle appears at the output.



Analysis:

- (i) TUF: It is the ratio of dc power to the ac rated power.
- TUF of FWR is estimated by the average of secondary winding UF and $HWR \times 2$ UF.

$$TUF \text{ of FWR} \rightarrow \frac{\text{Sec WLF} - 2 \times \text{HWR UP}}{2}$$

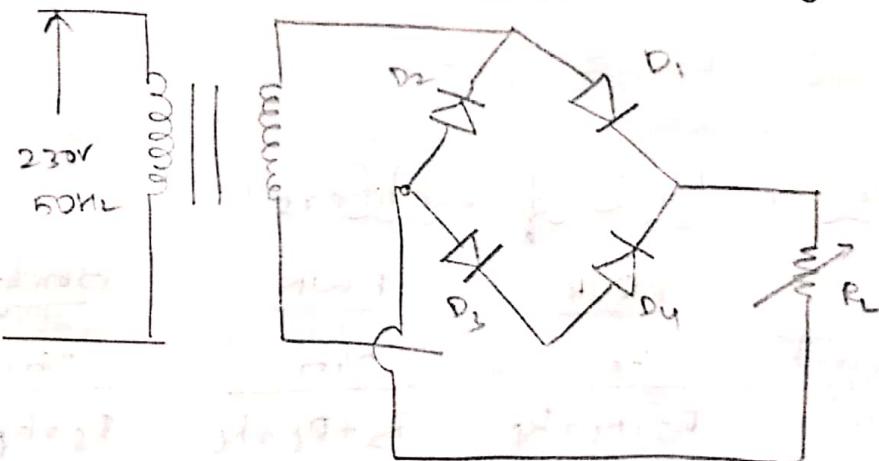
$$= \frac{0.81 + (2 \times 0.287)}{2}$$

$$\Rightarrow 0.69.$$

$\eta \uparrow$
 $\gamma \downarrow$
 $TUF \uparrow$

(ii) Bridge rectifier:

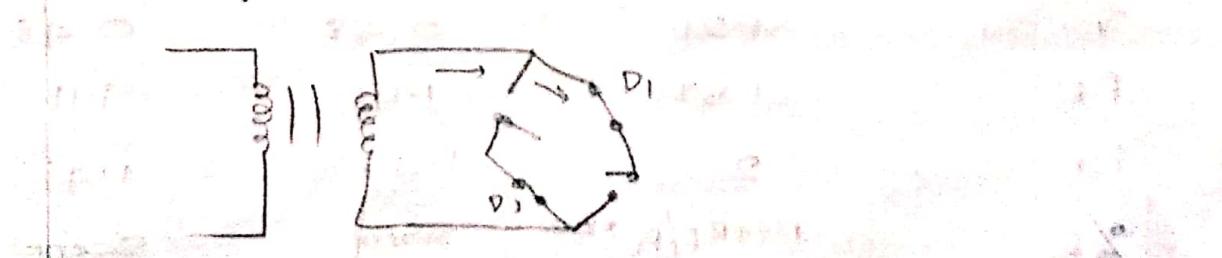
- To overcome the drawbacks of centre tapped transformer FWR, we use bridge rectifier.



- It consists of bridge of 4 diodes, load resistor.

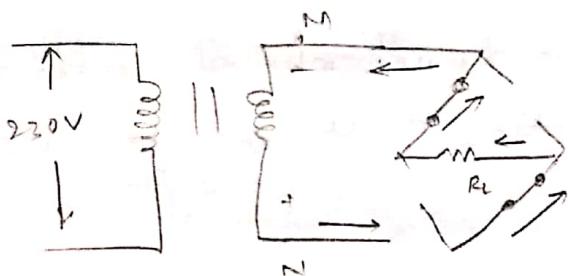
(c) Case-1:

- During +ve cycle of the input signal waveform the secondary winding upper end is made positive w.r.t lower end. Hence D₁, D₃ conduct and D₂, D₄ act as open switch.
- Therefore, the +ve cycle is rectified and appears at output from O to π.



(c) Case - 2:

- During -ve cycle of the input signal, the sec. winding upper end is made -ve w.r.t lower end. Hence D_2, D_4 conduct.
- Therefore, $\pi - 2\pi$ cycle output appears at the load resistor.



* Comparison table of rectifiers:

	<u>HWR</u>	<u>FWR</u>	<u>Bridge R</u>
Peak Current (I_m)	$\frac{V_m}{R_s + R_L + R_f}$	$\frac{V_m}{R_s + R_f + R_L}$	$\frac{V_m}{R_s + R_f + R_L}$
PDV	V_m	$2V_m$	V_m
DC current	$\frac{I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{2I_m}{\pi}$
DC Voltage	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$	$\frac{2V_m}{\pi}$
RMS I	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$
RMS V	$\frac{V_m}{\sqrt{2}}$	$\frac{V_m}{\sqrt{2}}$	$\frac{V_m}{\sqrt{2}}$
η	40.6%	81.2%	81.2%
TUF	0.287	0.69	0.81
γ	1.21	0.48	0.48
FF	1.57	1.11	1.11
PF	2	1.41	1.41
%R	$R_s + R_f / R_L \times 100$	Same	Same

No. of diodes	1	2	4
frequency	f	$2f$	f

(c) Adv. of bridge rectifier:

- No centre tapped transformer is used
- TUF is high than Centre tapped FWR.

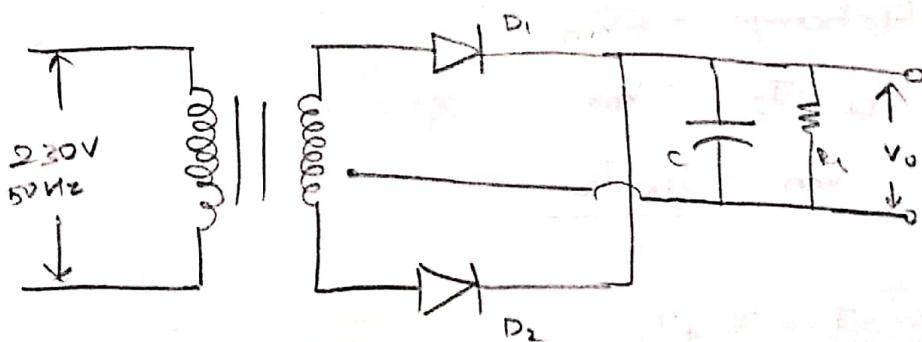
10/8/2019

Saturday

* Filters:

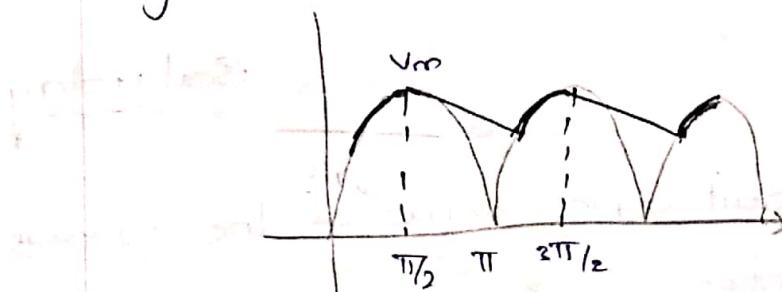
- Filter is a circuit which removes the unwanted components.
- Filters are made from passive components.
- There are 4 types of filters . (i) Shunt capacitor
 (ii) Series Inductor
 (iii) LC - L section
 (iv) CIC - π section.

(i) Shunt capacitor :



- Write the procedure of rectification of FWR.
- When rectified output is applied to shunt capacitor then filter reduces ac component
- Hence, the output is almost dc.

- When rectified output is applied about capacitor, during the $0-\frac{\pi}{2}$ cycle, input signal raises so the capacitor charges to the max. value.
- During $\frac{\pi}{2}-\pi$ cycle, input signal falls down so the capacitor discharges as shown in the figure.



$$\gamma = \frac{V_{rms}}{V_{dc}}$$

$$V_{rms} = \frac{V_m}{2\sqrt{3}}$$

$$Q_{discharge} = I_{dc} \cdot T_2$$

$$Q_{charge} = CV_m$$

$$I_{dc} \cdot T_2 = CV_m$$

$$V_m = \frac{I_{dc} T_2}{C}$$

$$T = \pi + T_2$$

$$T_2 = \frac{T}{2}$$

$$V_m = \frac{I_{dc} \cdot T}{2C}$$

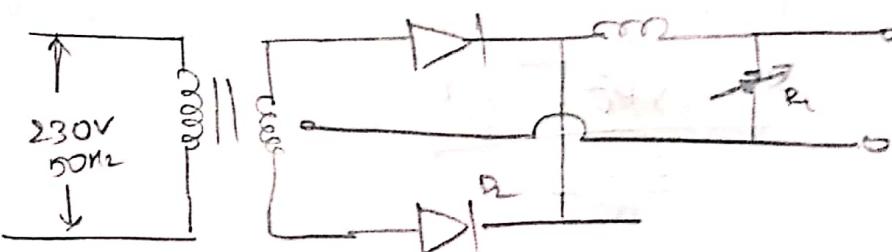
$$V_m = \frac{I_{dc}}{2fC} \left[T = \frac{1}{f} \right] \rightarrow (2)$$

$$\gamma = \frac{V_{rms}}{V_{DC}} \quad (4)$$

$$\gamma = \frac{\frac{I_{DC}}{2fC}}{\frac{2\sqrt{3}}{V_{DC}}} = \frac{\frac{I_{DC}}{4\sqrt{3}fC}}{V_{DC}} = \frac{2I_{DC}}{4\sqrt{3}V_{DC}}$$

$$\gamma = \frac{1}{4\sqrt{3}fCR_L}$$

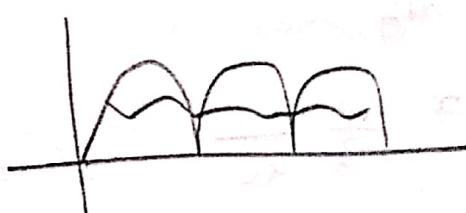
(ii) Series Inductor :



- When FWR output is applied to series capacitor then filter reduces ac component, Hence output is almost dc.
- Inductor will allow dc components hence the output is dc as shown in figure.

$$\text{Output voltage } - V_o = V_i - L \frac{di}{dt}$$

↑ ↑ ↓ ↓



By applying the 4yr series to the filter
 Output $i(t) = \frac{2I_m}{\pi} - \frac{4I_m}{\pi} \frac{\cos 2\omega t}{3} + \dots$

$$\gamma = \frac{I_{rms}}{I_{dc}}, I_{rms} = \frac{4Im}{3\pi\sqrt{2}}$$

$$\Rightarrow Im = \frac{Vm}{Z}$$

$$= \frac{Vm}{\sqrt{R_L^2 + \omega^2 L^2}}$$

$$\text{But } \omega = 2\pi f$$

$$\Rightarrow Im = \frac{Vm}{\sqrt{R_L^2 + 4\pi^2 C^2}}$$

$$\gamma = \frac{4 \cdot Vm}{\frac{3\pi\sqrt{2} \sqrt{R_L^2 + 4\pi^2 C^2}}{2\pi f}}$$

$$\gamma = \frac{4Vm}{\frac{3\pi\sqrt{2} \sqrt{R_L^2 + 4\pi^2 C^2}}{2\pi f}} = \frac{1}{3\sqrt{2}} \frac{R_L}{\omega_L}$$

13/8/2019

Tuesday

$$\rightarrow \text{For capacitor } \tau = \frac{1}{4\sqrt{3}\pi C R_L}$$

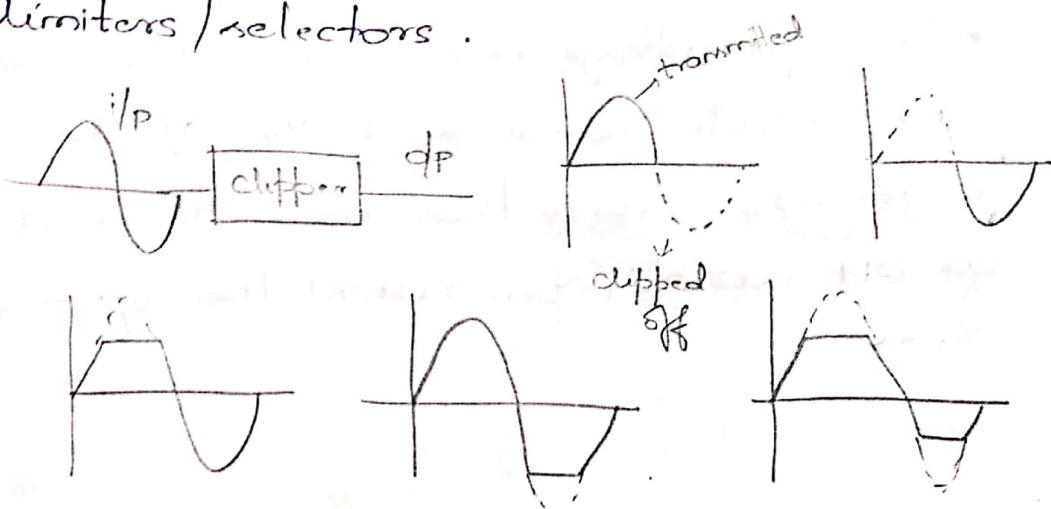
$$\rightarrow \text{For inductor } \tau = \frac{1}{3\sqrt{2}} \frac{R_L}{\omega_L}$$

$$\rightarrow \text{For 'L' section - LC } \tau = \frac{\sqrt{2}}{3} \cdot \frac{x_C}{x_L}$$

$$\rightarrow \text{For C-C - T-section } \tau = \frac{\sqrt{2}}{3} \cdot \frac{x_{C1}}{R_L} \cdot \frac{x_{C2}}{x_L}$$

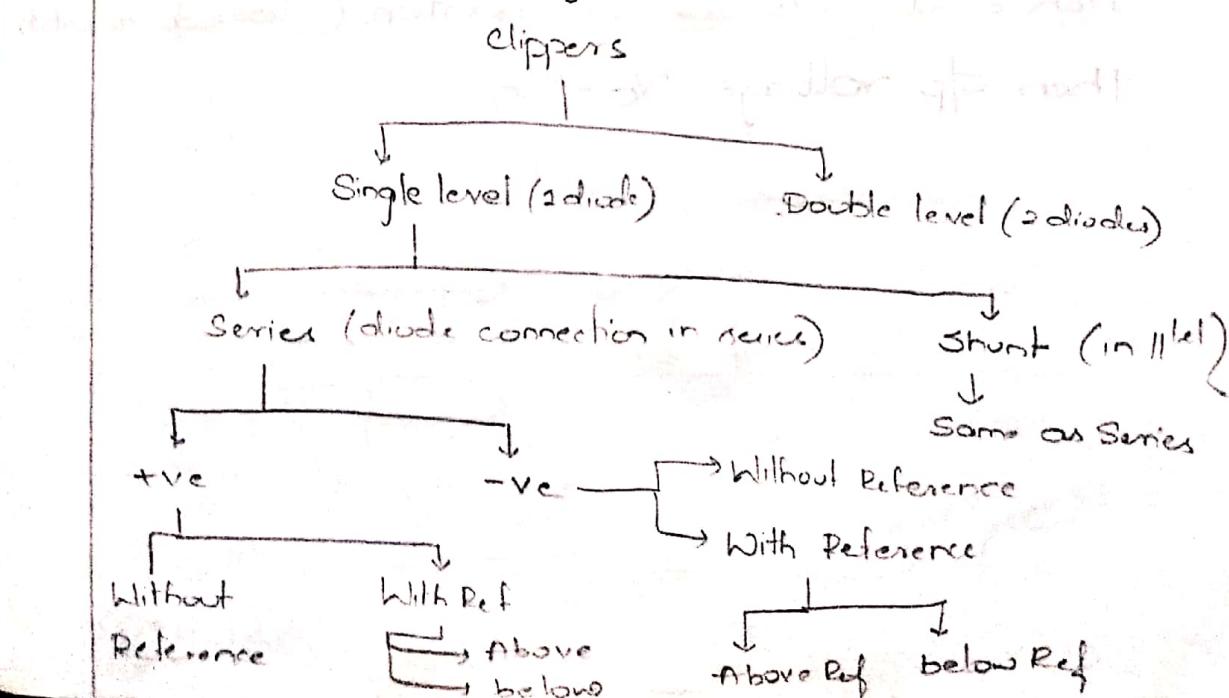
* Clippers:

- The process of selecting a portion of waveform from the input waveform is called clipping.
- It is a transmission circuit which transmits certain portion and other portion is discarded.
- Clippers are also called as amplitude slicers / limiters / selectors.



* Applications of Clippers:

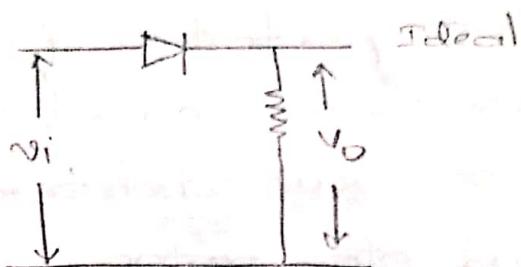
- To eliminate noise in communication.
- To select the synchronised signal from the composite video signal in television.



14/8/2019

Notes

- * Semic unbiassed -ve clipper:



$$Vi = V_D + V_o$$

$$V_o = Vi - V_D$$

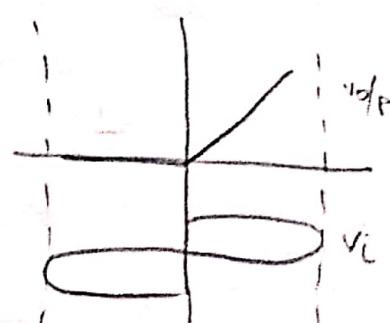
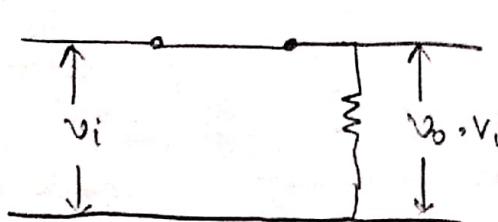
Case-1:

When i/p voltage is less than cut in voltage [i.e., consider ideal diode $V_D = 0$]. The diode D gets into reverse bias mode. Hence, it acts as off switch (open switch) then o/p voltage $V_o = 0$.

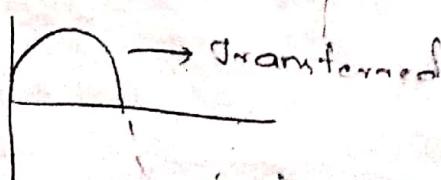


Case-2:

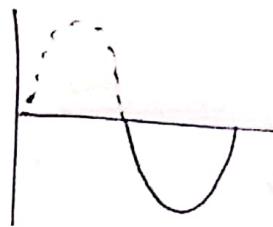
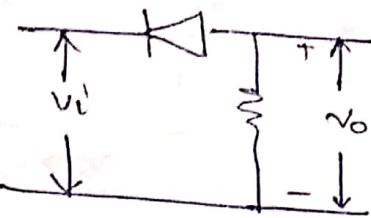
When i/p voltage is greater than cut in voltage, the diode gets into forward bias. Hence it acts as ON switch (closed switch) then o/p voltage $V_o = V_{in}$



Output \rightarrow



* Series unbiased +ve clipper:



Case-i:

$$V_i > V_y \text{ (ov)}$$

D = ON



Case-ii:

$$V_i < V_y$$

D = OFF



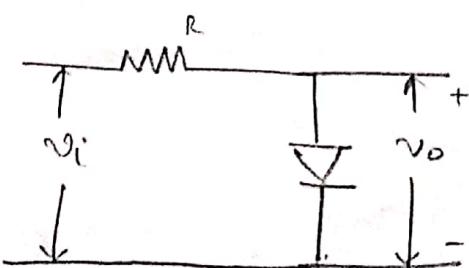
16/8/2019



Today

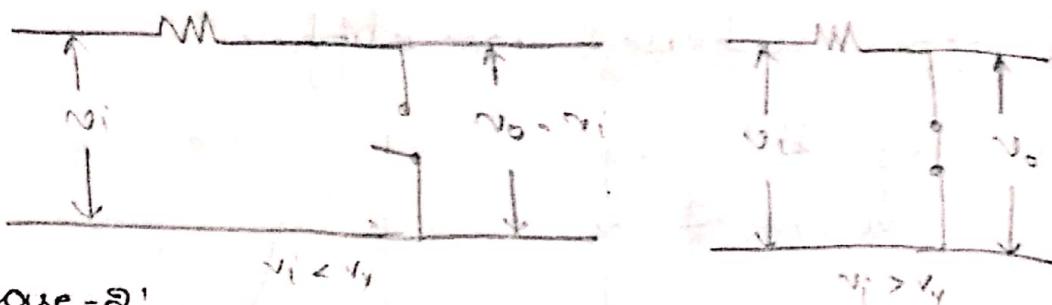
* Shunt clippers:

- In shunt clipper diode is connected in parallel to the output.
- In these clippers, ON position is clipped off and diode OFF position is transmitted. (portion).



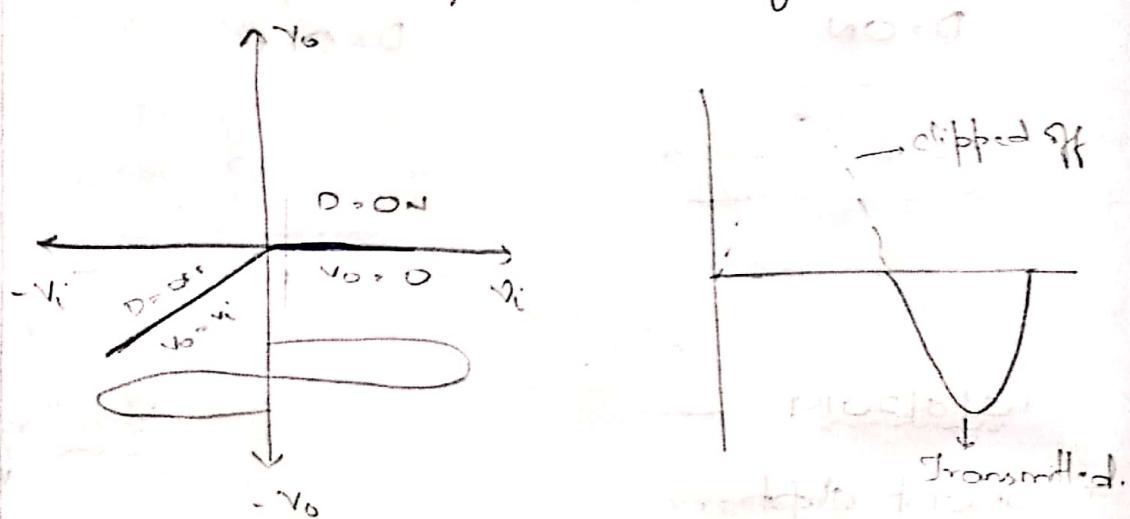
Case-i:

When i/p voltage is < cut-in voltage, diode D gets into reverse bias. Hence it acts as OFF switch. Then output voltage is = to i/p vol.

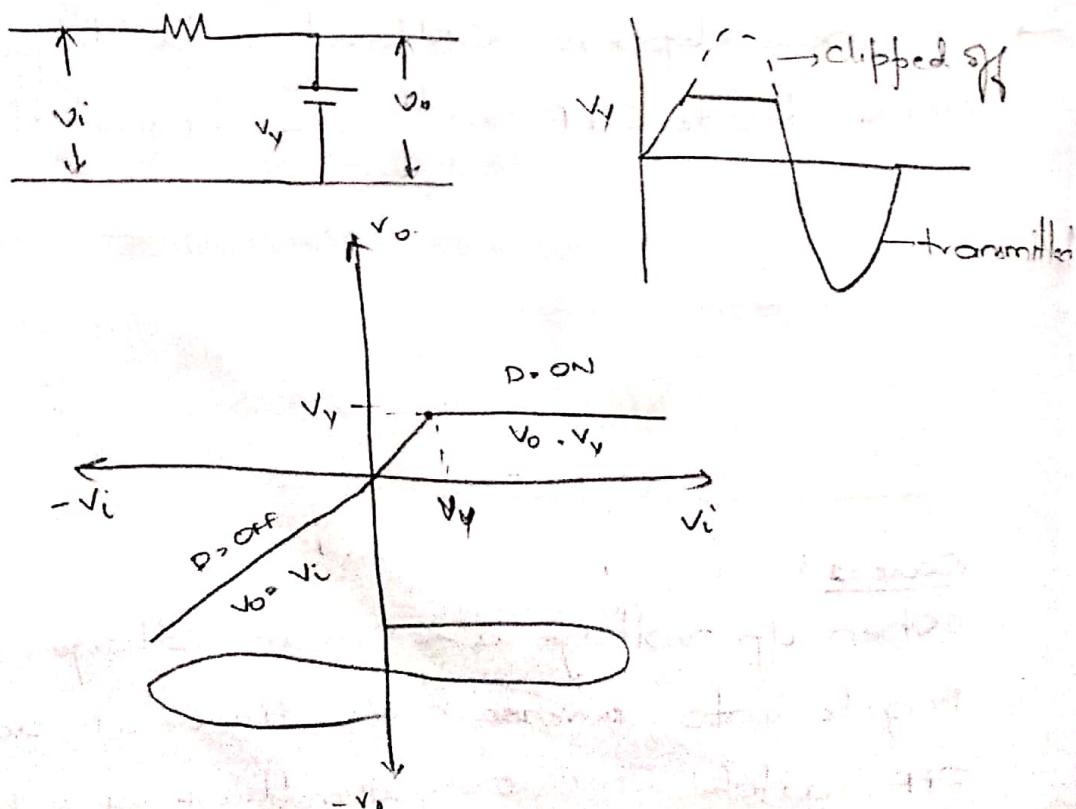


Case - 2:

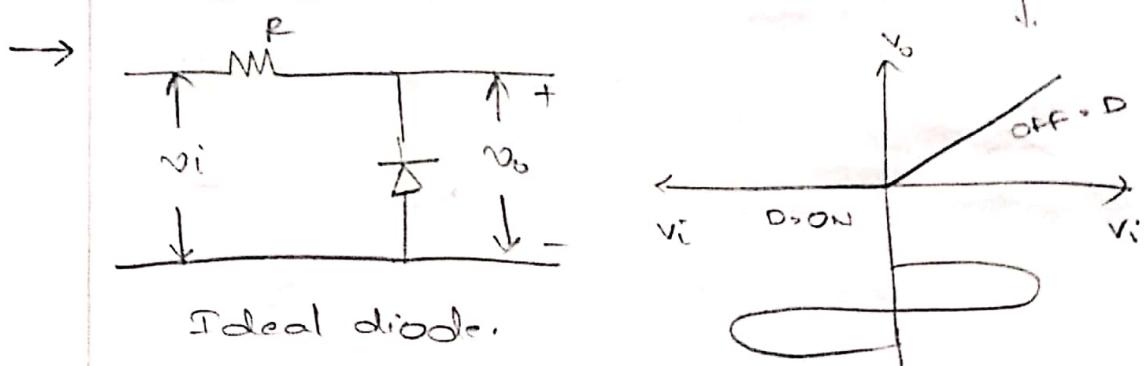
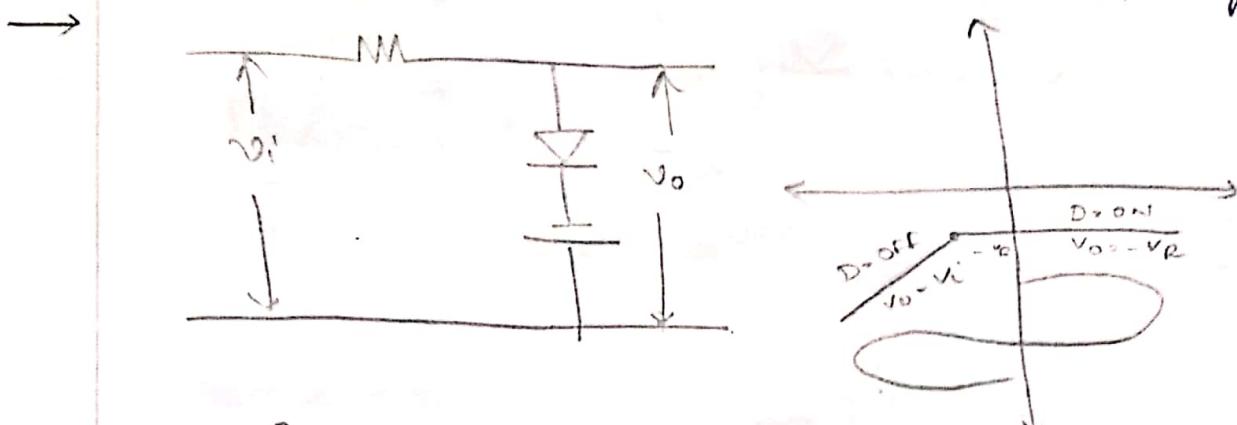
- When $v_i > v_y$, diode acts in ON position.
Therefore, the o/p voltage is zero.



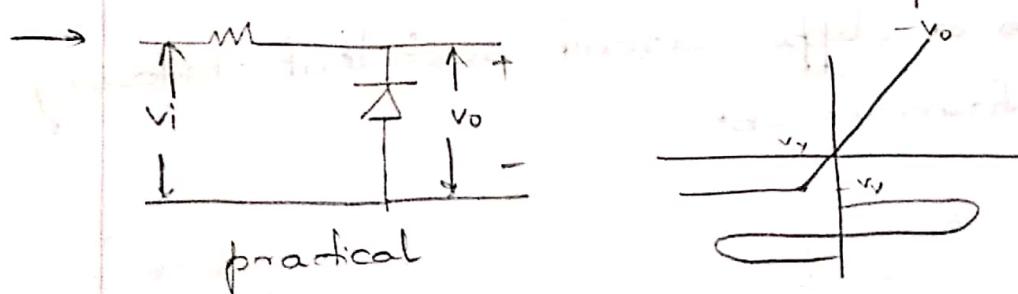
- If the diode is practical diode then the output voltage is $v_o = v_y$.



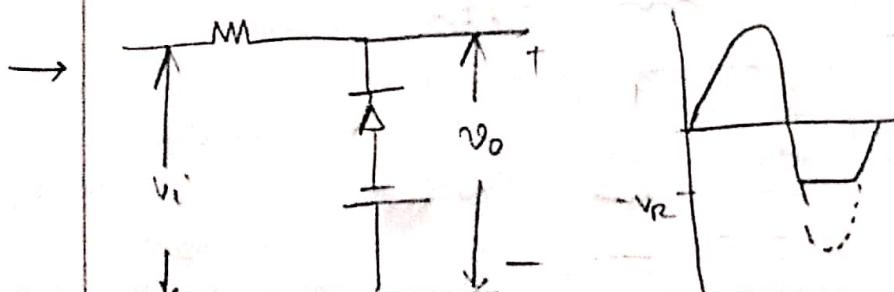
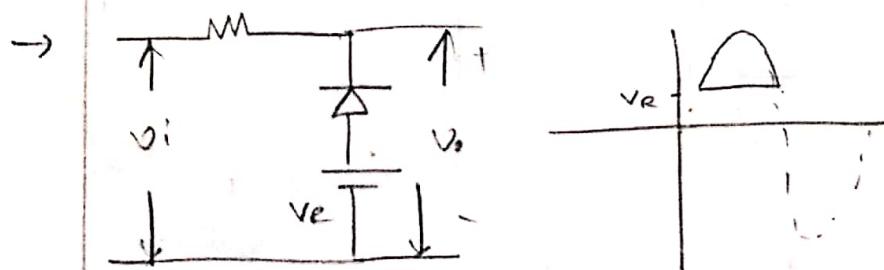
→ When a +ve reference is taken then the above +ve referenced portion is clamped off.



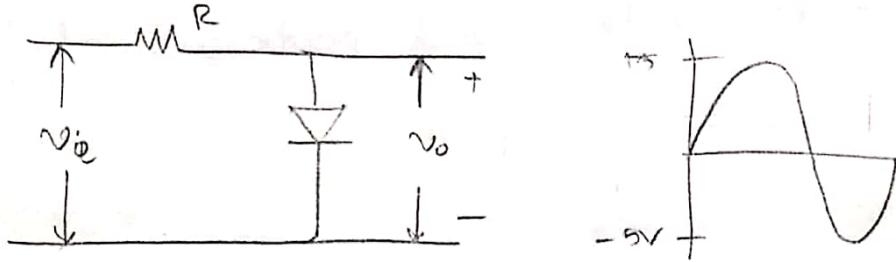
Ideal diode.



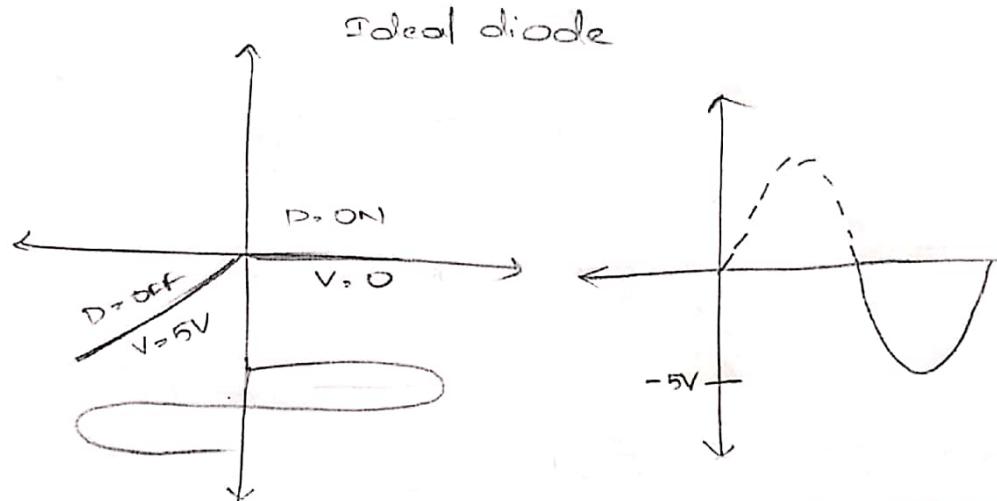
practical



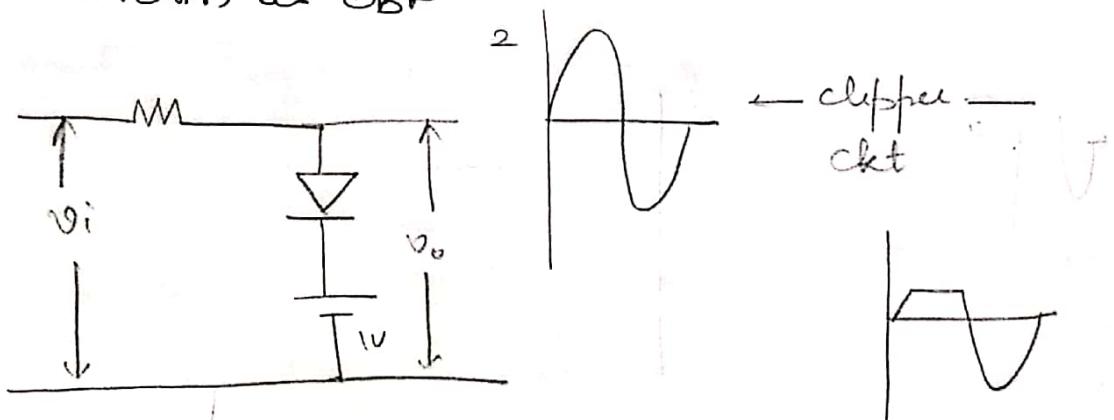
Q. Draw the transfer & o/p waveform.



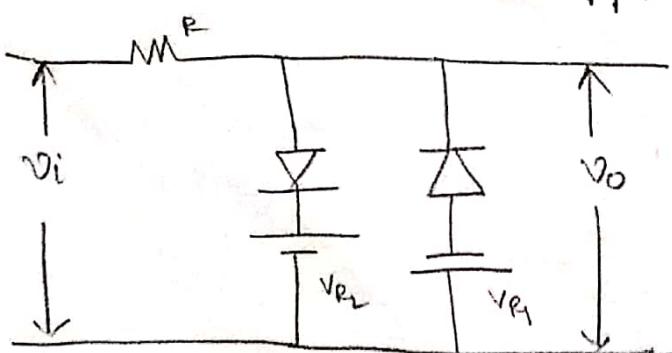
Sol:



Q. Design a clipper circuit such that following waveform is obt

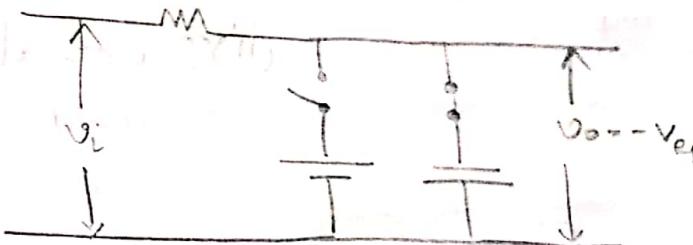


* Slicer or double diode clipper!



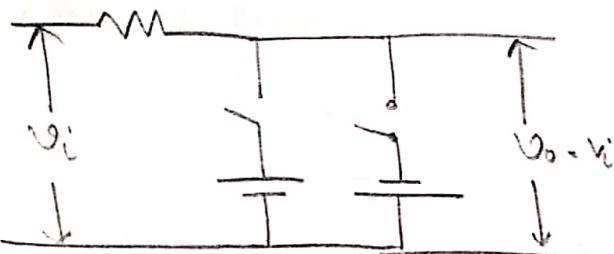
Case-1: In this case, voltage will depend on

$$V_i < V_{R_1} \text{, } D_1 = \text{ON}, D_2 = \text{OFF}, V_o = -V_{R_1}$$

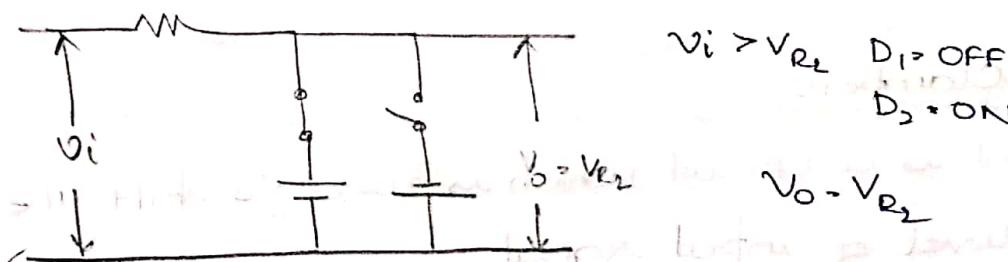


Case-2:

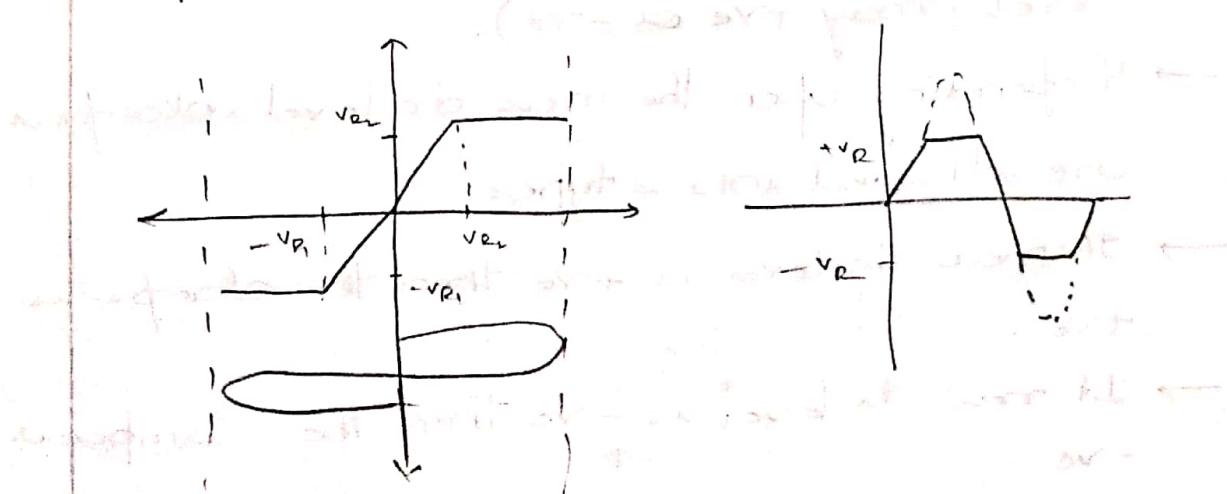
$$-V_{R_1} < V_i < V_{e_2}; D_1 = \text{OFF}, D_2 = \text{OFF} \quad V_o = V_i$$



Case-3:

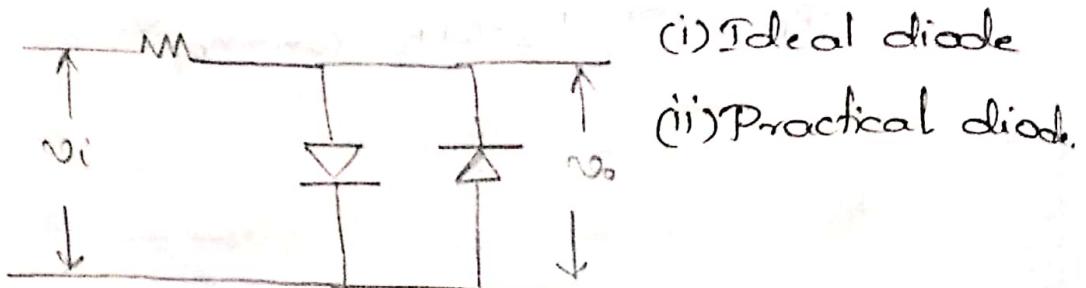


Output: In this case, there will be two reference voltages.

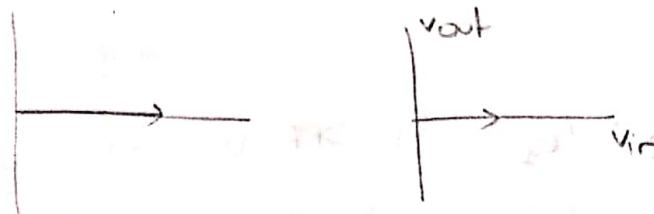


→ In a slicer, wave block two references are transmitted.

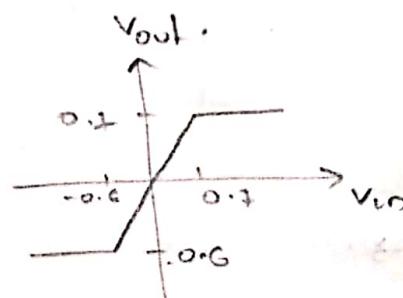
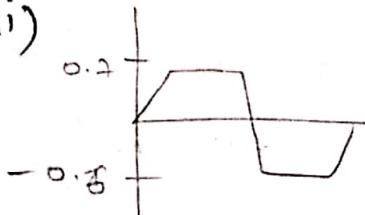
Q. Draw the transfer and output waveforms.



(i)



(ii)

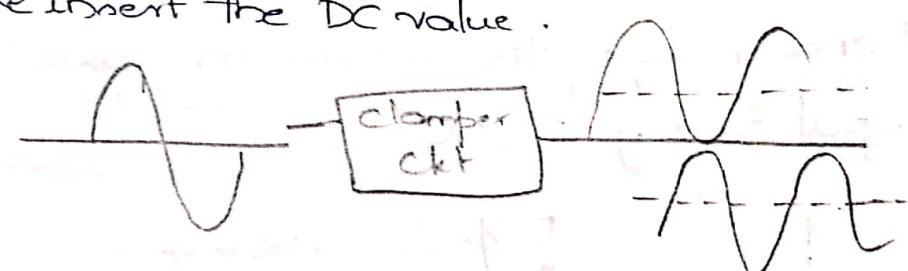


* Clampers!:

- It is a circuit which is used to shift the DC level of input signal.
- It is a circuit which introduces a new DC level (may +ve or -ve).
- Depending upon the new DC level, clampers are divided into 2 types.
- If new DC level is +ve then the clapper is +ve.
- If new DC level is -ve then the clapper is -ve.
- They are also called as DC restorers or DC reinserters.

* Applications of clamps:

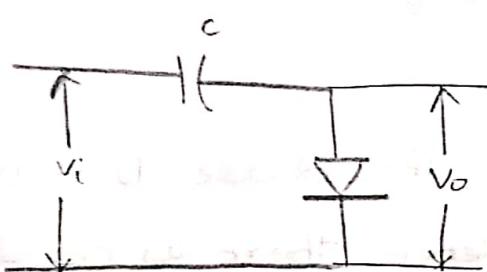
- In voltage multipliers.
- Level shifters
- Reinsert the DC value.



* Negative clamp:

17/8/2019

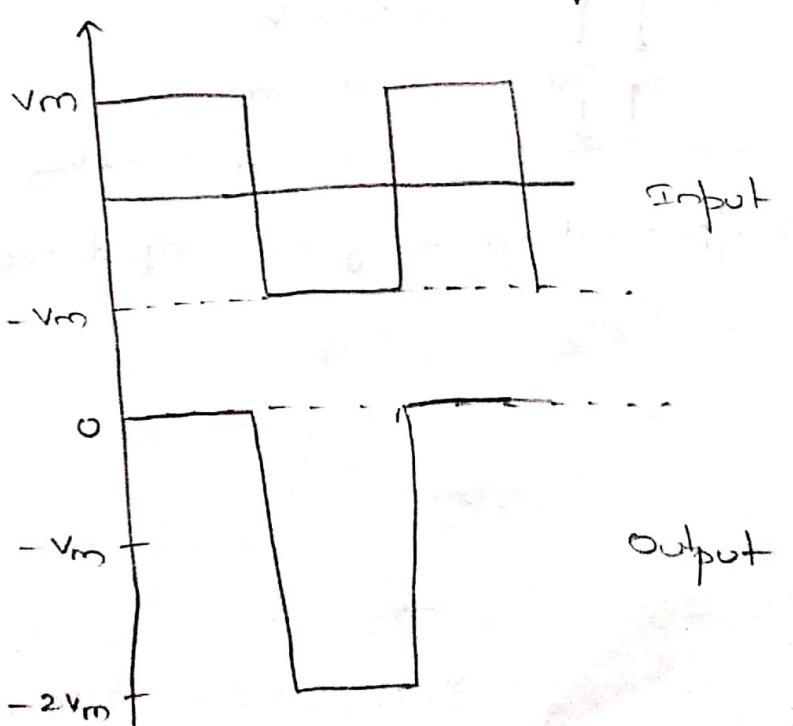
Saturday



$$V_i = V_C + V_o$$

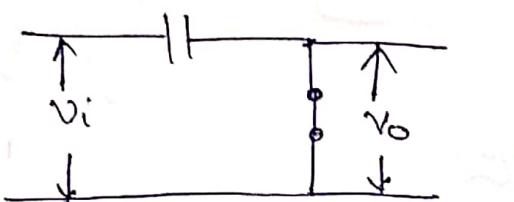
$$V_o = V_i - V_C$$

- Above ckt shows the negative clamp.
- It consists of capacitor and diode.
- It is also called as +ve peak clamp.



Case-1:

During 1st quarter cycle of input signal wave form the diode D will get into ON position (short circuit). Hence, capacitor will charge upto the maximum value V_m & output voltage $V_o = 0$.



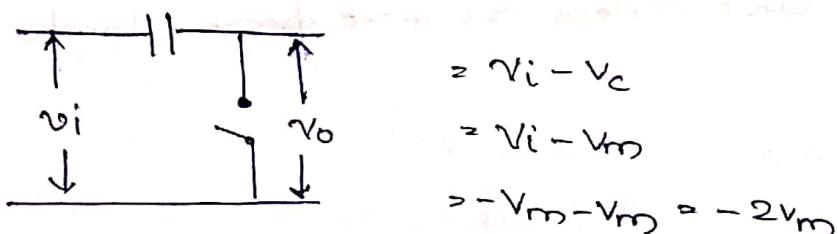
$$= V_i - V_c$$

$$= V_m - V_m$$

$$= 0$$

Case 2:

During $\pi/2$ to 2π , the diode D will get into off position. Hence, there is no discharging path. So capacitor attains some voltage V_m . Hence, the output voltage is $-2V_m$.

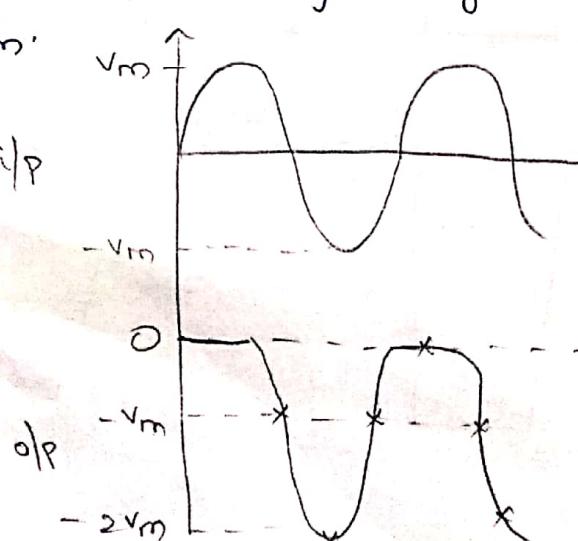


$$= V_i - V_c$$

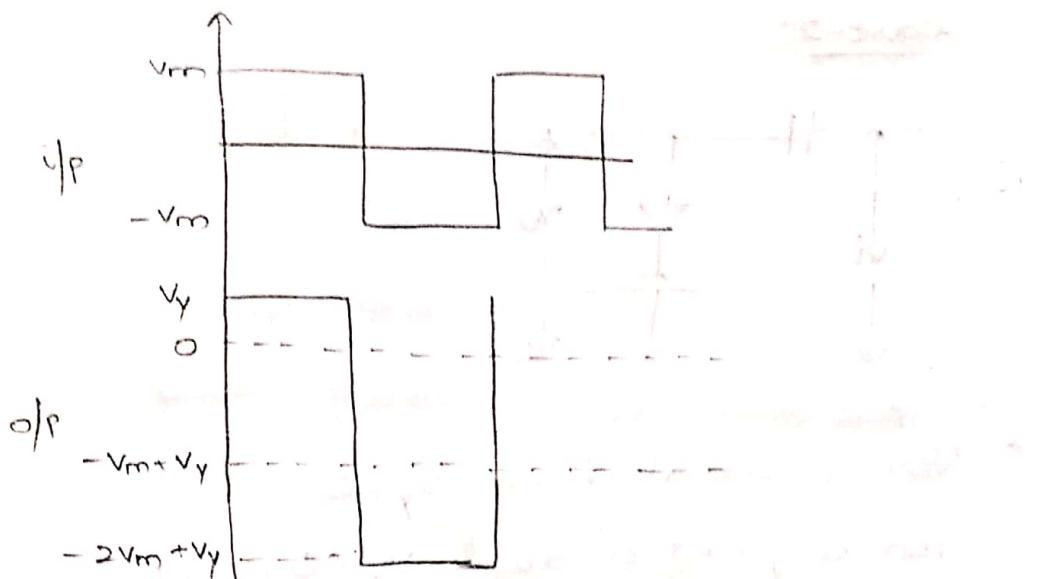
$$= V_i - V_m$$

$$= -V_m - V_m = -2V_m$$

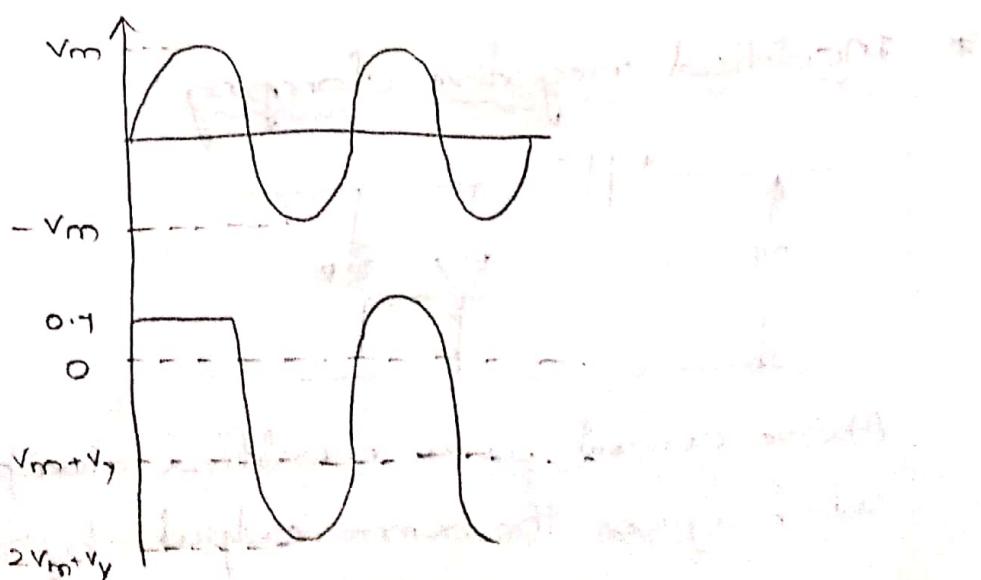
when i/p voltage is zero output voltage is $-V_m$.



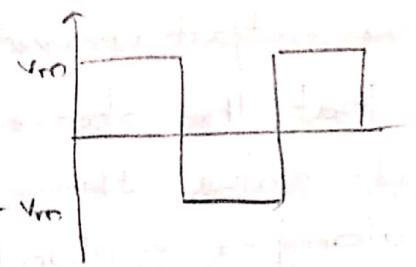
- * Note!
- By observing the above output waveforms it can be concluded that the above circuit introduces negative dc value. Hence, it is called as negative clammer or clamping.
- In this circuit positive peak of the i/p signal is clamped to zero value. Hence, it is also called as +ve peak clammer.
- If the diode is non ideal diode, the +ve peak clamped is from V_y .



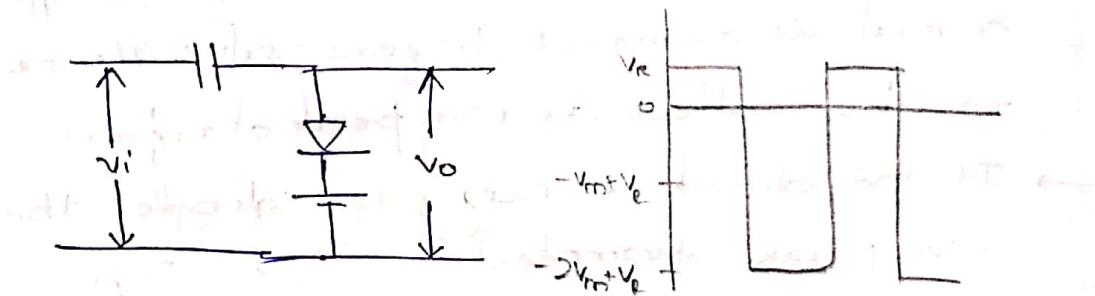
Sine wave:



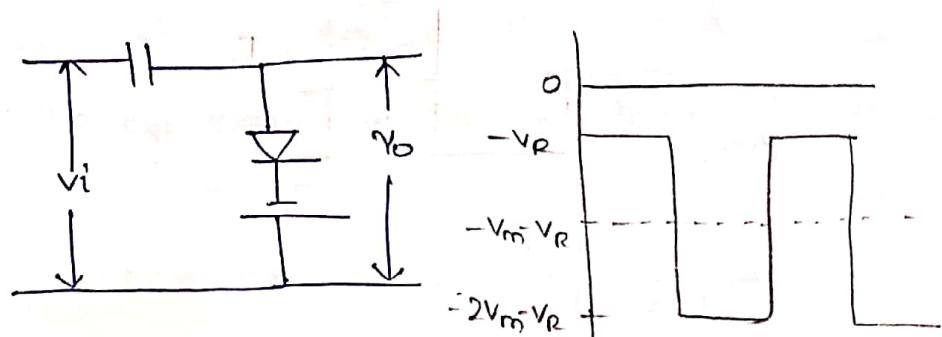
With reference:



case-1: +Ve reference



case-2:

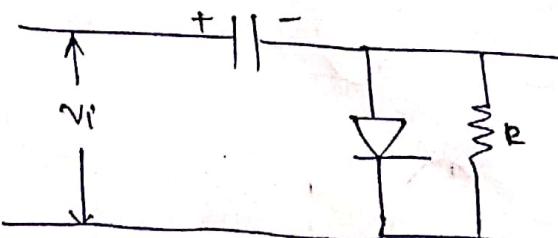


→ For a ideal diode $V_y = 0$

for a practical diode $V_y = 0.6 \text{ or } 0.7$

New dc level = $-V_m + V_y \pm V_R$.

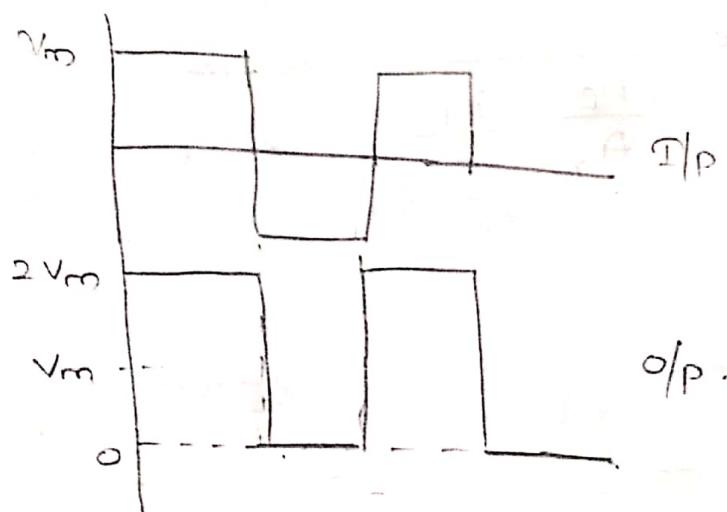
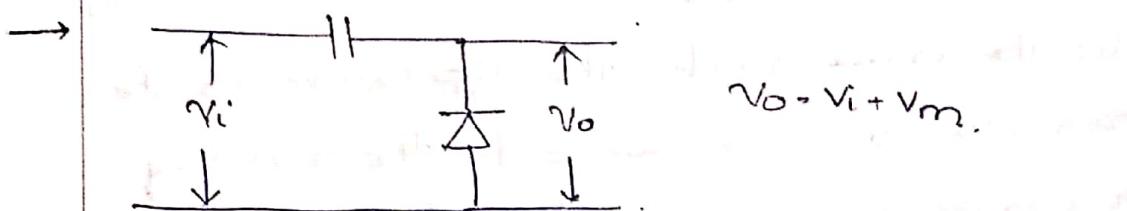
* Modified negative clamping:



Above circuit is a modified clamer circuit which gives the same output by considering

time constant $RC \gg T/2$.

* Aleg Positive clammer / negative peak clammer

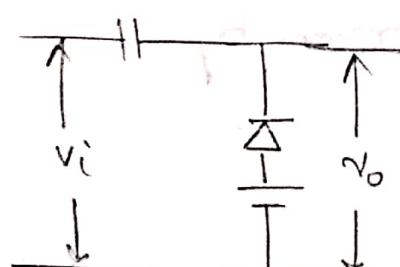


→ For an ideal diode $V_f = 0$

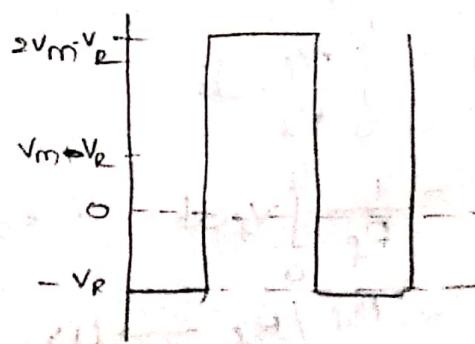
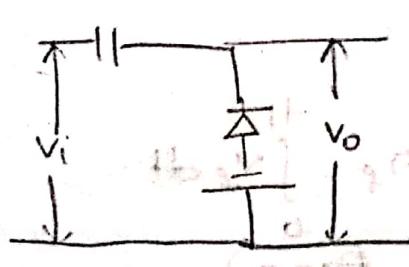
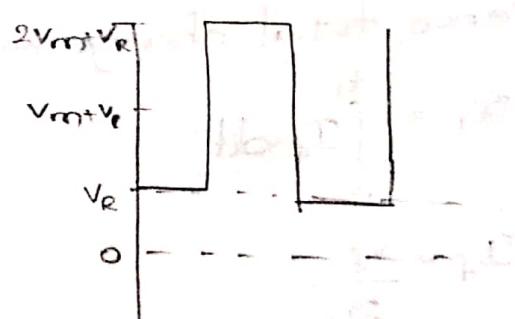
for a practical diode $V_f = 0.6 \text{ or } 0.7$

Reference Voltage = V_R

New dc level $\rightarrow V_m + V_f \pm V_R$.



+ve Reference

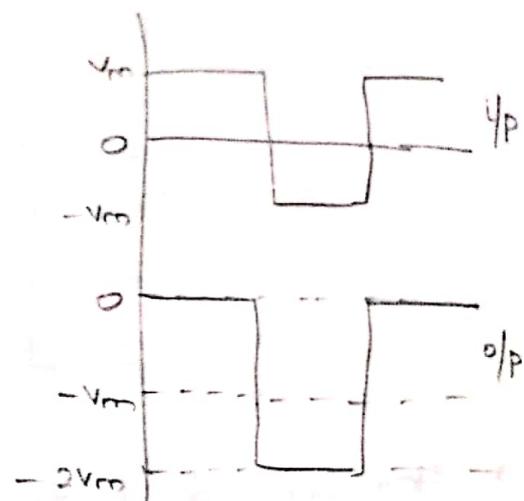
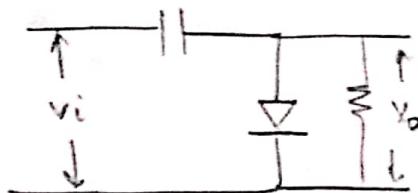


* Clamping circuit theorem:

→ This theorem states that the ratio of Area under the curve in the forward direction to the area under the o/p curve in the reverse direction is = to the ratio of forward resistance to the short or external resistance.

$$\frac{A_f}{A_r} = \frac{R_f}{R}$$

(i) Proof!



Case 1

During 0 to t_2 time interval, the diode acts as ON switch i.e., forward bias.

Hence total charge is given by

$$Q_1 = \int_0^{t_1} I_f dt$$

$$I_f = \frac{V_f}{R_f}$$

$$Q_1 = \int_0^{t_1} \frac{V_f}{R_f} dt$$

$$= \frac{1}{R_f} \int_0^{t_1} V_f dt \quad \text{i.e., } A_f = \int_0^{t_1} V_f dt$$

$$\Rightarrow (A_f / R_f \rightarrow (1), \text{ Area})$$

During time interval t_1 to t_2 , the diode gets into reverse bias. Hence the total charge is given by,

$$Q_2 = \int_{t_1}^{t_2} i_r dt.$$

$$i_r = \frac{V_r}{R}$$

$$Q_2 = \frac{1}{R} \int_{t_1}^{t_2} V_r dt \rightarrow \frac{A_r}{R} \quad (2)$$

During equilibrium, charging and discharging time periods are equal.

$$\Rightarrow Q_1 = Q_2$$

$$\Rightarrow \frac{Af}{R_f} = \frac{Ar}{R}$$

$$\Rightarrow \frac{Af}{Ar} = \frac{R_f}{R}$$

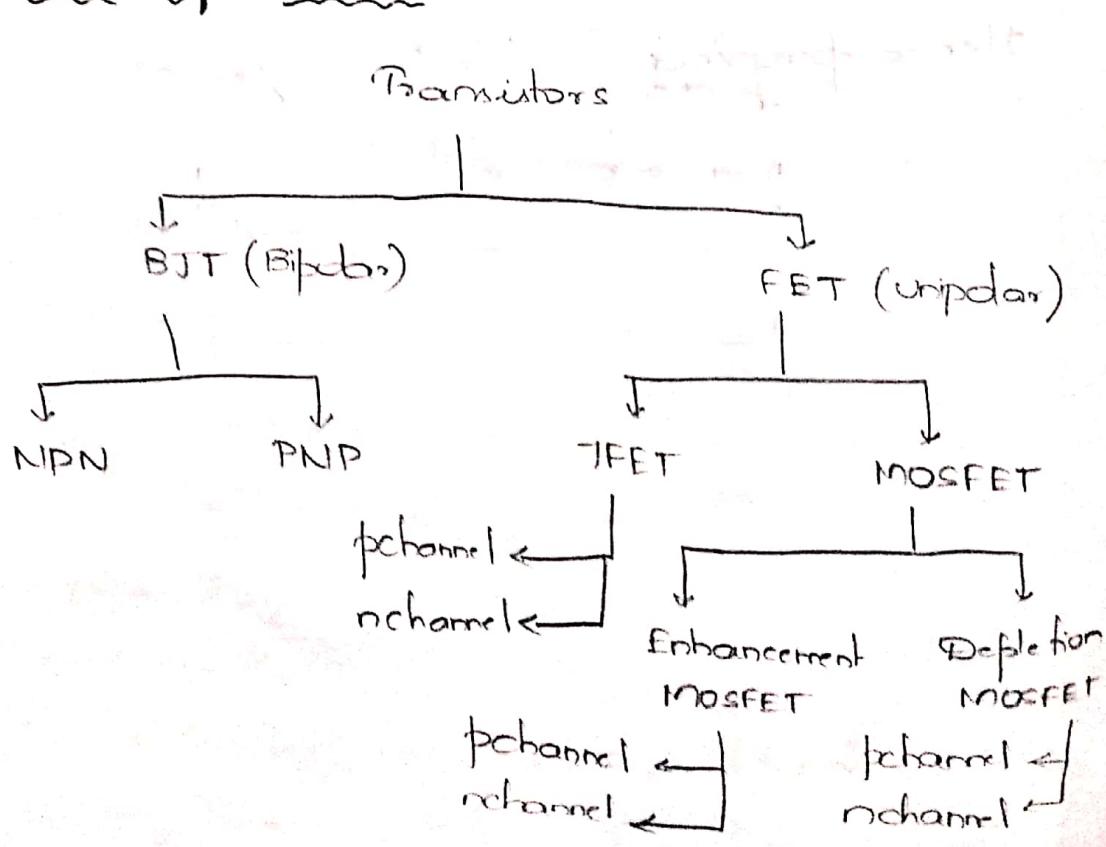
Hence proved.

TRANSISTORS

- Transfer of Resistor is called transistor.
- It transfers low resistance to high resistance.
- The V-I characteristics of semiconductor triode is called transistor.
- Back to back connection of 2 p-n junctions or diodes is known as transistor in which the middle layer should be lightly doped.
- Transistor has 3 layers (3 layers are PNP or NPN).
- It has 3 terminals and the terminals are emitter, base, collector (EBC).

It has 2 junctions (i) $J_1 = J_{EB}$ (input junction)
 (ii) $J_2 = J_{CB}$ (output junction).

* Types of transistors:



* Emitter:

- It is heavily doped & medium in size.
- The fn of emitter is to inject majority charge carriers.

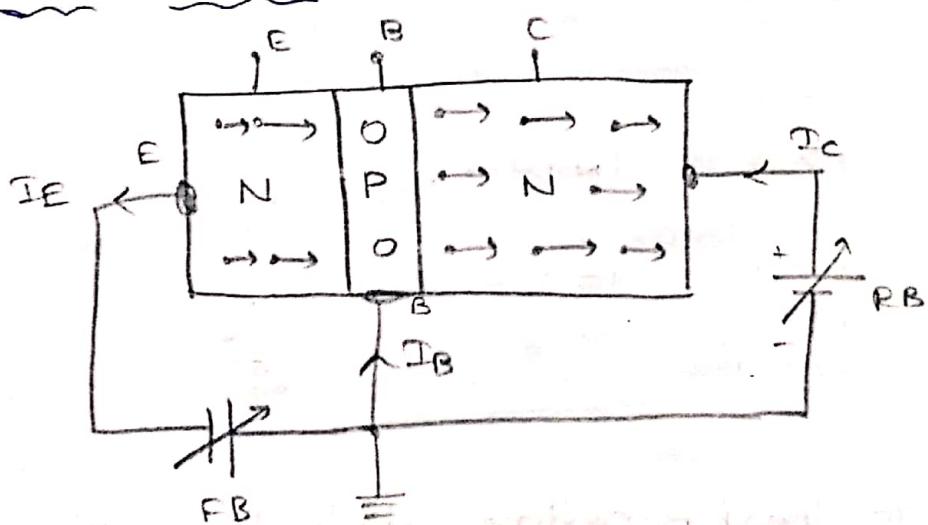
* Base:

- It is lightly doped & small in size.
- The fn is to transfer the majority charge carriers.

* Collector:

- It is moderately doped & large in size.
- The fn of collector is to collect the majority charge carriers.

* NPN transistor:

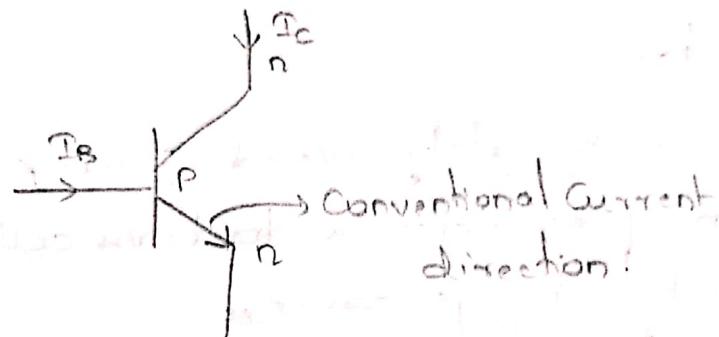


- Due to the FB voltage applied at the input side, the e⁻s are emitted from emitter region to base region due to repulsion.
- Since, the base is lightly doped & small in size, it has less no. of holes, these holes

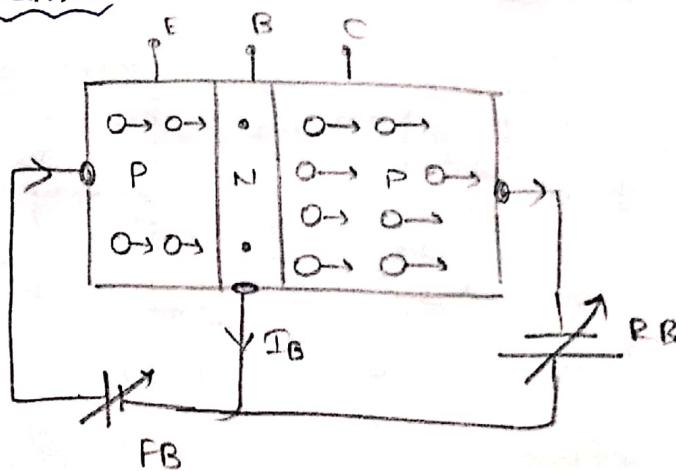
are recombined with the ejected electrons from emitter which constitute the base current I_B .

- The remaining ejected e^- s are transferred to collector terminal.
- The collector collects the majority charge carriers which constitutes collector current I_C .

$$\therefore I_E = I_B + I_C$$



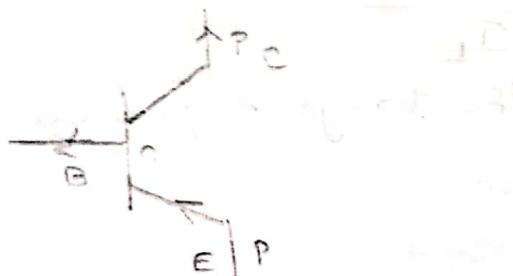
* PNP transistor:



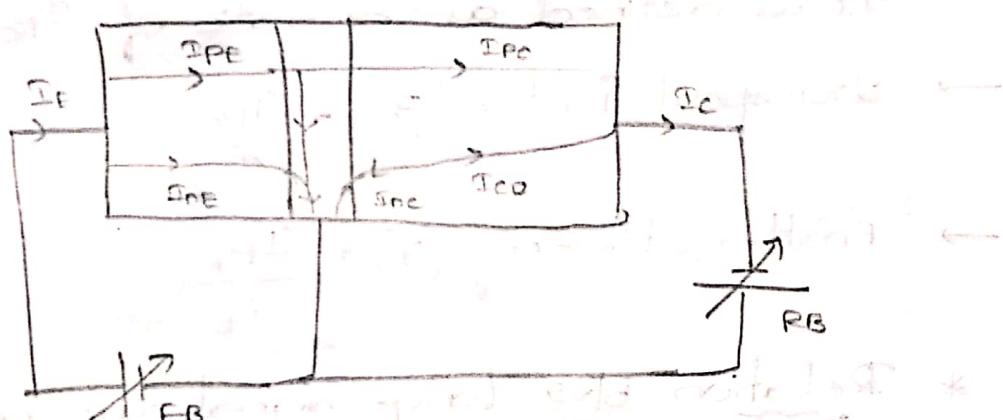
- Due to the FB voltage applied on the input side, the holes are emitted in the emitter region to the base region. This hole current constitutes I_E .
- The emitted holes recombine with the e^- in the base region and it constitutes I_B .

i.e., the base current.

- The remaining ejected holes are transferred to the collector terminal.
- The collector collects the holes and which constitutes collector current I_C .



* Current components in a transistor:



As we know that,

$$I_F = I_B + I_E$$

- all the holes that are emitted from emitter may not reach to the collector terminal due to recombination in the base region.
- Hence collector current is approximately equal to base current.

$$I_C \approx I_E$$

$$I_C = \alpha I_E \rightarrow \text{due to majority charge carriers}$$

where α is 0.995 to 0.999

$I_C = I_{CO} \rightarrow$ due to the minority charge carriers.

Total current in collector,

$$I_C = \alpha I_E + I_{CO}$$

$$\Rightarrow \alpha = \frac{I_C - I_{CO}}{I_E}$$

This ' α ' is the large signal current gain.

* Note:

$$\rightarrow \alpha = \frac{I_{PC}}{I_E}$$

It is defined as the ratio of I_{PC} to I_E .

$$\rightarrow \text{Transport factor } (\beta) = \frac{I_{PC}}{I_{PE}}$$

$$\rightarrow \text{Emitter efficiency } (\gamma) = \frac{I_{PE}}{I_E}$$

* Relation b/w large signal current gain, transport factor & emitter efficiency:

$$\alpha = \frac{I_C}{I_E} = \frac{I_{PC}}{I_E}$$

$$\alpha = \frac{I_{PC}}{I_E} \cdot \frac{I_{PE}}{I_E}$$

$$\alpha = \beta \times \gamma$$

\rightarrow	J _{EB} i/p Tr.	J _{CB} o/p Tr.	Mode of operation	Application	
	FB	RB	Active Region	Amplifier	
	RB	FB	Inverse Active Region	Attenuator	
	FB	FB	Saturation	ON switch	
	RB	RB	Cut off region	OFF switch	
\rightarrow	Si Cut off 0.0	V _{CE} Cut in 0.6	V _{CE} Active 0.7	V _{CE} Saturation 0.8	V _{CE} Sat. 0.2
	Ge -0.1	0.1	0.2	0.3	0.1

* Transistor configuration:

- \rightarrow As we know that there are 3 terminals in the transistor (EBC).
- \rightarrow Transistor analysis can be done by 2 port network.
- \rightarrow The network which has 2 ports is called 2-port network (input port & output port)
- \rightarrow Input port & O/P port has 2 terminals each.
- \rightarrow They are i/p current (I_1), i/p voltage (v_1), o/p current (I_2), o/p voltage (v_2).
- \rightarrow Since, the analysis of transistor can be done by 2 port network and the available terminals in transistor are 3, one terminal is considered as common for input and

output purpose.

Based on the common terminal, the transistor configurations are of 3 types.

(i) Common base configuration

(base terminal is common for i/p & o/p
or base is grounded)

(ii) Common emitter configuration

(Emitter terminal is grounded)

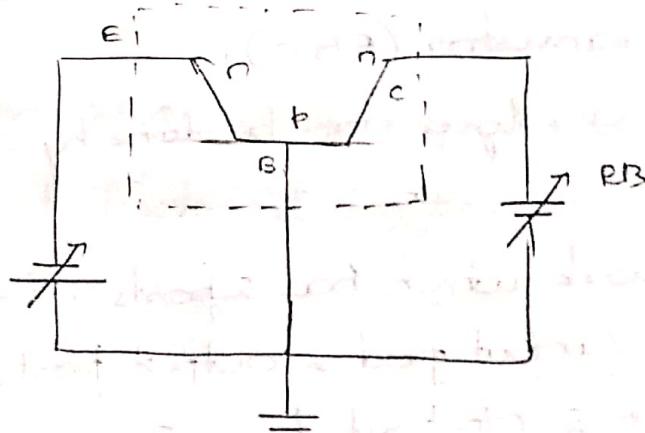
(iii) Common collector configuration

(Collector terminal is grounded)

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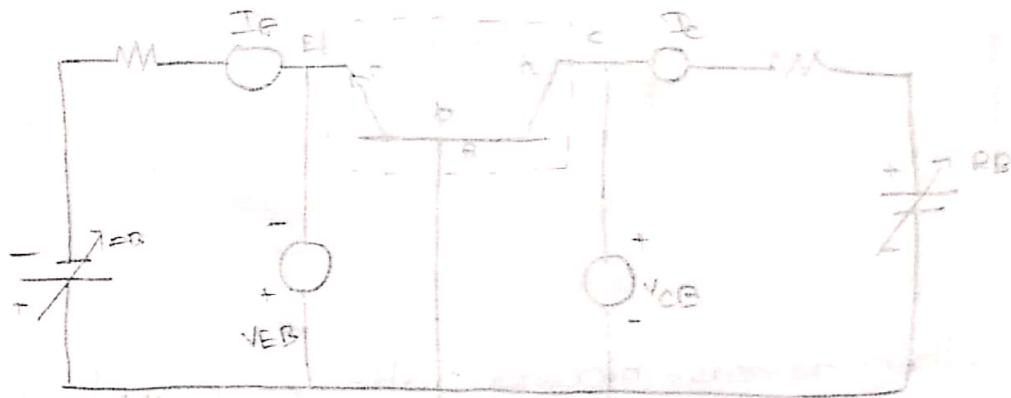
Friday

* Common base configuration:



- Above diagram shows CB configuration in which the i/p terminals are emitter and base, the o/p terminals are collector and base.
- Hence base is common for both i/p & o/p.
- This is called CB configuration.
- In this, base is connected to ground.

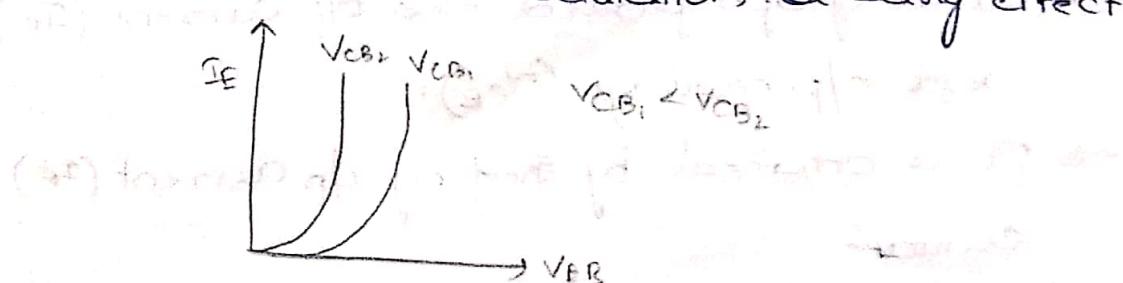
- This is also called as grounded base configuration.



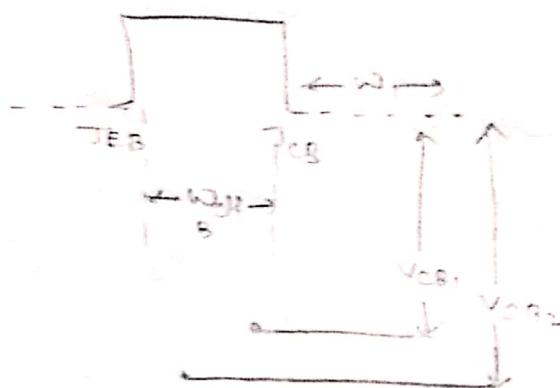
- (i) Input characteristics:
- It is a graph plotted b/w I_E current (I_E) and i/p voltage (V_{EB}).
 - These characteristics are obtained by keeping the o/p voltage (V_{CB}) constant.

Case-1: When $V_{CB} = 0$, by varying the power supply at the i/p side, we will observe that i/p current (I_E) ↑ exponentially. (since it is a forward biased diode).

Case-2: If we increase the reverse voltage (V_{CB}), the current shifts towards the left i.e., ν_I characteristics shift towards the left. This is due to base width modulation or Early effect.



⇒ Base width modulation!



- When reverse biased voltage is applied to CB junction, the depletion layer width W_B into the base region.
- Hence, effective base width decreases.
- This concept is called base width modulation or Early effect.
- As further $V_{CB} \uparrow s$, at a particular voltage value of V_{CB} , the basic width becomes zero.
- This is called as Reach through/punch through. ($W_B \approx 0$)

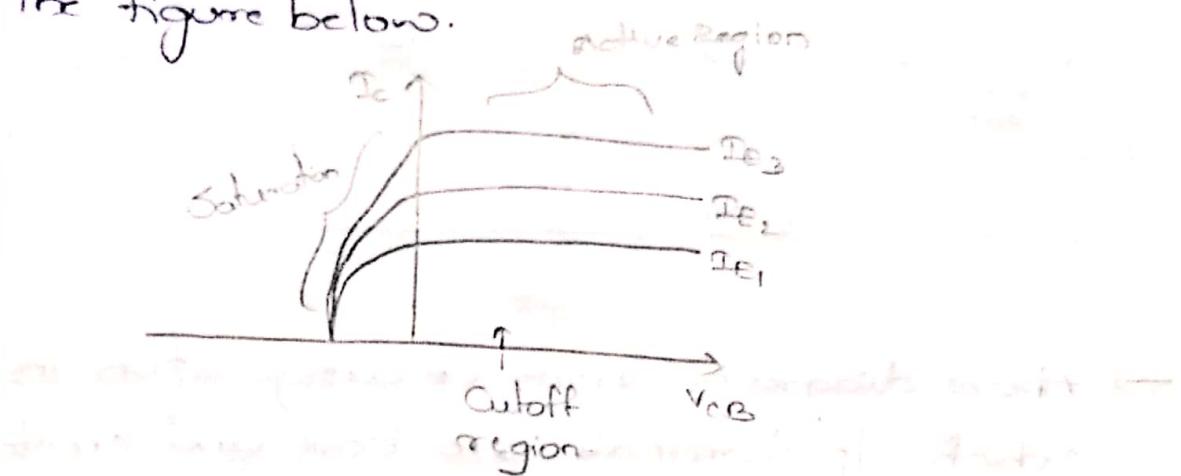
Consequences of base width modulation:

- Due to the base width modulation; $I_C \uparrow s$, $I_E \uparrow s$, $\alpha \uparrow s$, $I_B \uparrow s$.
- $I_B \uparrow s$ because width $\uparrow s$ $\left[I_E \uparrow \cdot \frac{dn}{dx_1} \right]$

(c) Output characteristic:

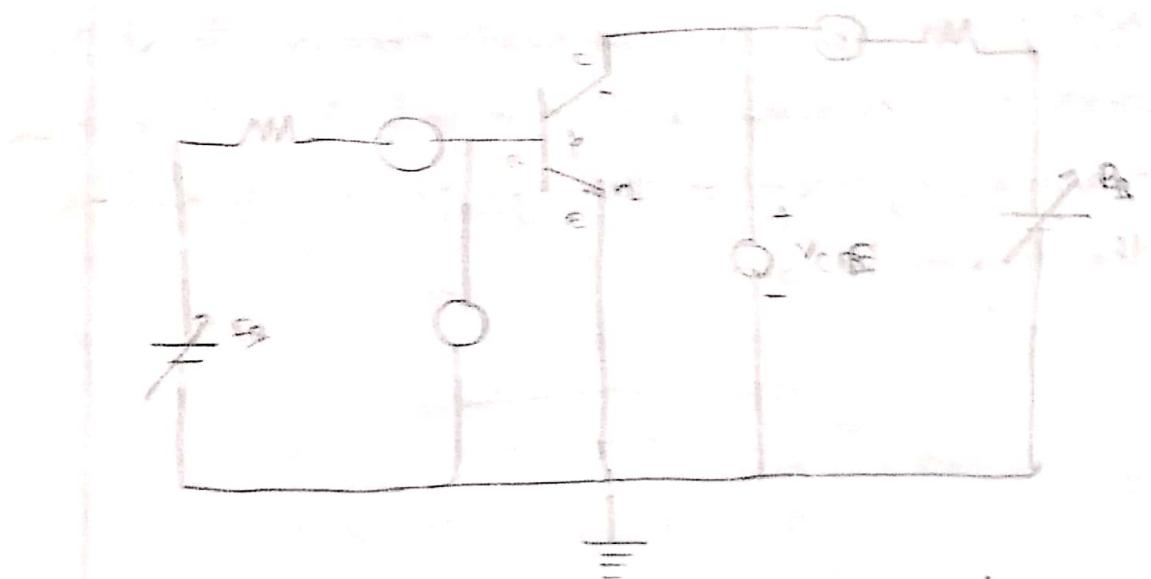
- It is graph plotted b/w o/p current (I_C) and o/p voltage (V_{CB}).
- It is obtained by keeping i/p current (I_E) constant.

Case-2: When $I_E = I_{E2}$, by varying the power supply at o/p side, we will observe that I_C and V_{CB} values are changed. Based on these values, if we plot the graph, it looks like the figure below.



- Saturation region :- Both i/p & o/p jns are operated in its FB.
- Active Region :- If i/pjn is operated in FB and the o/p jn is operated in RB, then the transistor is said to be in active region.
- Cut off region :- Both i/p & o/p jns are operated in RB.
- Amplification factor (α) :- It is defined as the ratio of output current to the i/p current.
- In CS configuration, this is denoted by α_{dc} .
- $$\alpha_{dc} = \frac{\Delta I_C}{\Delta I_E}$$

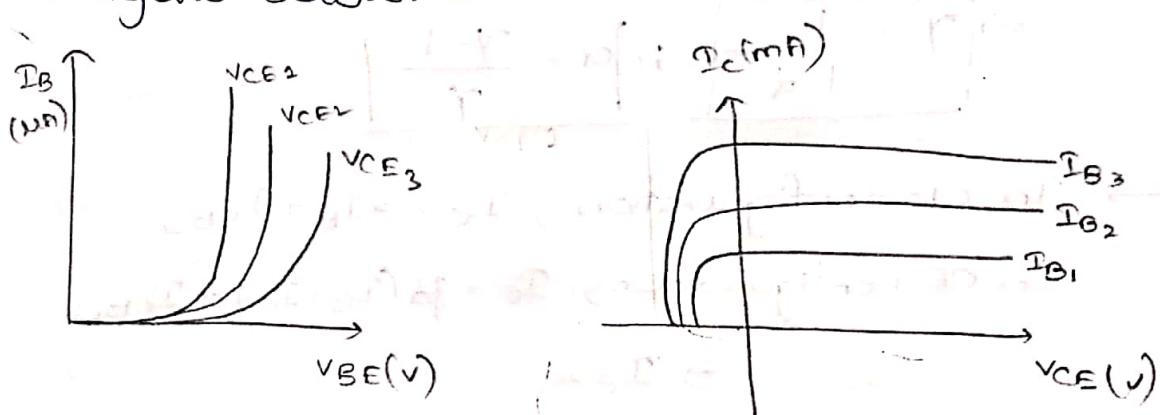
* Common emitter configuration



- Above diagram shows CE configuration in which i/p terminals are base and emitter, the o/p terminals are emitter & collector.
- Hence base or emitter is common for i/p & o/p.
- In this, emitter is grounded. Hence, it is also called as ground emitter configuration.
- ① Input characteristics:
- It is a graph plotted b/w i/p current (I_B) and i/p voltage (V_{BE}).
- These characteristics are obtained by keeping the o/p voltage (V_{CE}) constant.
- Case-1: When $V_{CE} > 0$, by varying the power supply at the i/p side, we will observe that i/p current (I_B) is exponentially. (Since it is F^B).
- Case-2: If we ↑ the reverse voltage V_{CE} , the current shifts towards the right. This is likely due to base width modulation.

(c) Output characteristics:

- It is graph plotted b/w o/p current (I_C) and o/p voltage (V_{CE}).
- It is obtained by keeping i/p current (I_B) constant.
- When $I_B = I_{B_0}$, by varying the power supply at o/p side, we will observe that I_C and V_{CE} values are changed. Based on these values, if we plot the graph, it looks like the figure below.



$$V_{CE\ 2} < V_{CE\ 2} \cdot (i/p) \quad I_{B_1} < I_{B_2} \quad (o/p)$$

$\beta = \frac{I_C}{I_B}$, this is amplification factor in CE configuration.

Why $\gamma = \frac{I_E}{I_B}$ in CC configuration

* Relation b/w α, β, γ :

$$\alpha > \frac{I_C}{I_E}, \beta = \frac{I_C}{I_B}, \gamma > \frac{I_E}{I_B}$$

We know that, $I_E = I_C + I_B$

$$\Rightarrow \alpha > \frac{I_C}{I_C + I_B} \Rightarrow \alpha > \frac{I_C}{I_C \left[1 + \frac{I_B}{I_C} \right]} \Rightarrow \alpha = \frac{1}{1 + \frac{1}{\beta}}$$

$$\Rightarrow \alpha = \frac{\beta}{\beta + 1}$$

$$\Rightarrow \beta = \alpha\beta + \alpha$$

$$\Rightarrow \beta = \alpha\beta + \alpha$$

$$\Rightarrow \beta(1 - \alpha) = \alpha$$

$$\Rightarrow \beta = \frac{\alpha}{1 - \alpha}$$

We know that $\gamma = \frac{I_E}{I_B} = \frac{I_C + I_B}{I_B} = \beta + 1$

$$\Rightarrow \beta = \gamma - 1 ; \gamma = \beta + 1$$

$$\Rightarrow \gamma = \frac{1}{1 - \alpha} ; \alpha = \frac{\gamma - 1}{\gamma}$$

\rightarrow In CB configuration, $I_C > \alpha I_E + I_{CO}$

In CE configuration, $I_C = \beta(I_B + I_C) + I_{BO}$

$$\Rightarrow I_C >$$

Q. In a transistor, $\alpha_{DC} = 0.98$, $I_C = 3\text{mA}$, $I_E = ?$

$$I_B = ?$$

$$\text{Sol: } \alpha_{DC} = 0.98$$

$$\frac{I_C}{I_E} = 0.98 \rightarrow \frac{3 \times 10^{-3}}{I_E} = 0.98$$

$$\rightarrow I_E = \frac{3 \times 10^{-3}}{0.98} = 3.06\text{mA}$$

$$\rightarrow I_E = I_C + I_B$$

$$\Rightarrow 3.06 = 3 + I_B$$

$$\rightarrow I_B = 0.06\text{mA}$$

Q. In a transistor configuration, $\beta = 50$, $I_E = 4\text{mA}$, find I_C & I_B

$$\text{Sol: } \beta = 50$$

$$\frac{I_C}{I_B} = 50$$

$$\alpha = \frac{\beta}{1+\beta} \rightarrow \frac{50}{51} = 0.98$$

$$\frac{I_C}{I_E} = 0.98 \rightarrow I_C = 0.98 \times 4 = 3.92\text{mA}$$

$$I_E = I_C + I_B$$

$$4 - 3.92 = I_B$$

$$I_B = 0.08\text{mA}$$

Q. In a transistor, $\beta = 50$, $I_B = 50\mu\text{A}$, $I_{CBO} = 5\mu\text{A}$. find I_C

$$\text{Sol: } I_C = \beta I_B + (1+\beta) I_{CBO}$$

$$I_C = 50(50 \times 10^{-6}) + (1+50 \times 10^{-6}) 5 \times 10^{-6}$$

$$\rightarrow 25 \times 10^{-4} + [5 \times 10^{-6} + 25 \times 10^{-11}]$$

$$\rightarrow 2.75\text{mA}$$

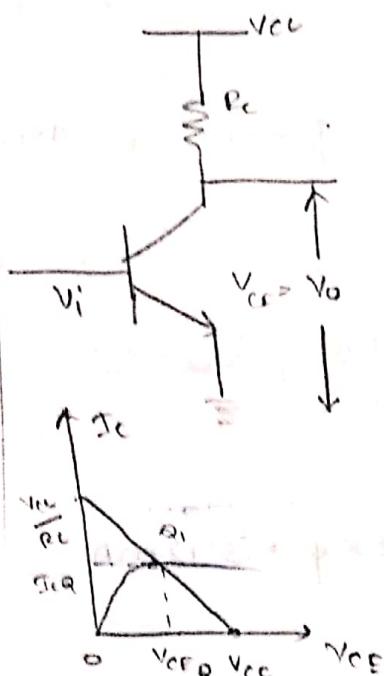
* Load line analysis:

It is a graphical representation of KVL.

It is of 2 types (i) dc load line
(ii) ac load line.

(i) DC load line:

- It is a straight line which joins dc current (I_C) and dc voltage (V_{CE}).



By applying KVL at the o/p side,

$$V_{CC} = I_C R_C + V_{CE} \quad \text{--- (1)}$$

$$I_C = \frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C}$$

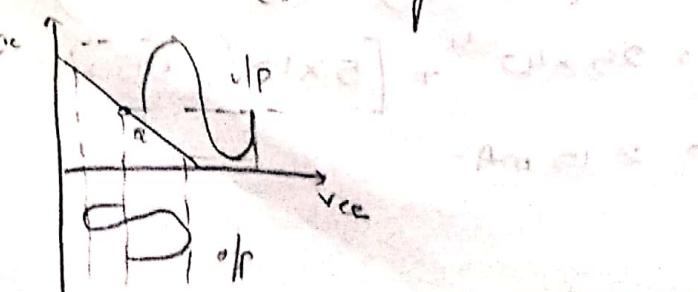
Case - 1: $V_{CE} = 0$ then $I_C = \frac{V_{CC}}{R_C}$

Case - 2: $I_C = 0$ then $V_{CE} = V_{CC}$

- 'Q' pt should be located in the linear active region or middle of dc load line.

(For better amplification).

- If we locate the Q. pt near to saturation region & cut off region, distorted waveform is obtained. (part of waveform is clipped off).



(ii) ac load line:



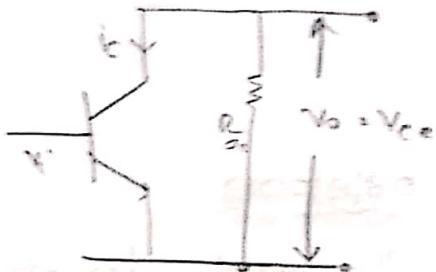
For ac analysis of transistor, the given steps are to be followed.

- (1) Connect all dc power supplies to ground.
- (2) Short all the capacitors present in the circuit.
- (3) Replace the transistor with its Ξ -h-parameter circuit.
- (4) V_{CC} should be grounded.

By applying KVL at the o/p side,

$$0 = i_C R_{AC} + V_{CE}$$

$$i_C = -\frac{V_{CE}}{R_{AC}} \quad (1)$$



as we know that, the total current is represented as

$$i_C = i_C^0 + I_C^{dc}$$

$$i_C = i_C - I_{CQ} \quad (2)$$

$$V_{CE} = V_{CE0} - V_{CEQ} \quad (3)$$

sub (2) & (3) in eq(1),

$$(i_C - I_{CQ}) = \frac{1}{R_{AC}} (V_{CE0} - V_{CEQ})$$

$$i_C = -\frac{V_{CE}}{R_{AC}} + I_{CQ} + \frac{V_{CEQ}}{R_{AC}} \quad (y = mx + c)$$

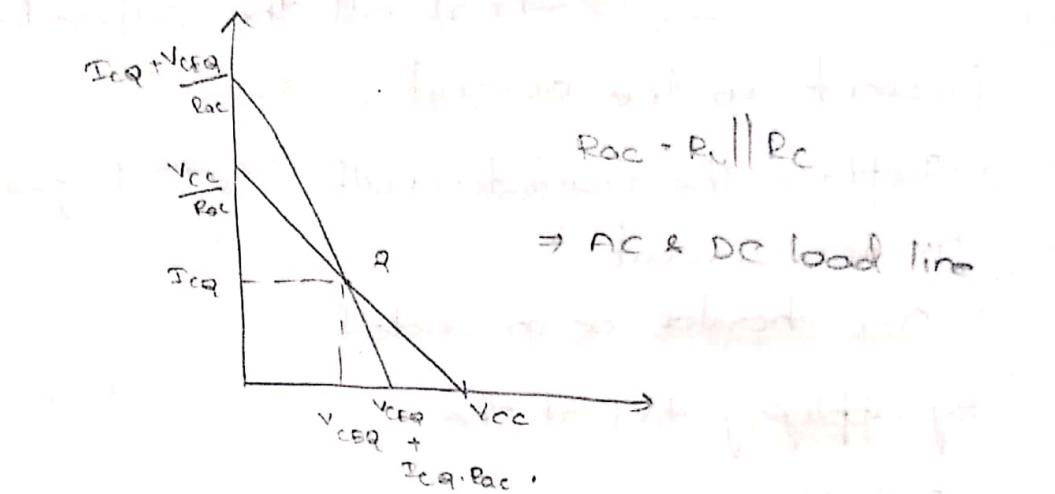
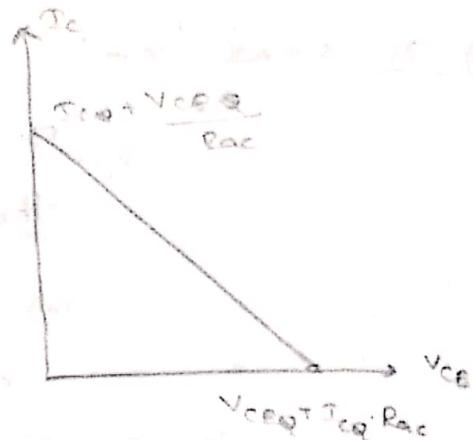
put $i_C = 0$

$$\text{then } V_{CE} = R_{AC} \left(I_{CQ} + \frac{V_{CEQ}}{R_{AC}} \right) = I_{CQ} R_{AC} + V_{CEQ}$$

$$\text{fact} \approx 0$$

$$I_C = I_{CQ} + \frac{V_{CEQ}}{R_L}$$

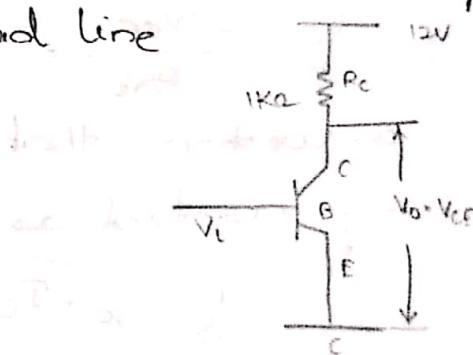
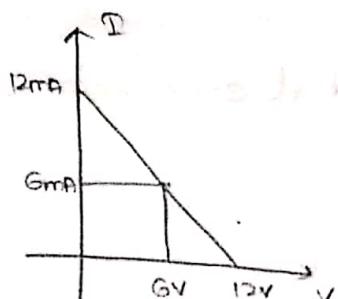
Worried about me Rac.



28/8/2019

Wednesday

Q. $I_C = 4\text{mA}$, Locate DC load line



* Stabilization and compensation techniques:

→ As we know that, for better amplification the 'Q' pt or operating pt should be located in linear active region only.

\rightarrow Q pt is fn of V_{CE} , $I_C \rightarrow Q = f(V_{CE}, I_C)$.

- * Factors affecting Q pt :
 1. Temperature.
 2. Replacement of one transistor with another.
- When temp T_A , the reverse current doubles for every 10° rise in temp. Due to this $I_c \propto T_A$ ($\because I_c = \beta I_B + (1+\beta) I_{CBO}$)
- If $I_c \propto T_A$, Q pt may shift towards saturation region & distorted output is obtained.
- As $I_c \uparrow$ power dissipation (P_d) also \uparrow which is "the form of heat".
- Hence self destruction takes place. This process is called thermal runaway.
- When 1 transistor is replaced with another transistor, β may not be same for the transistor. It may \uparrow or \downarrow so I_c also $\propto \beta$. Hence, Q pt is not stabilised, due to this distorted o/p is obtained.
- These drawbacks can be eliminated by stabilization & compensation techniques.

* Stabilization :

- This means fixing / stabilizing the operating pt irrespective of variation in temp. & replacement of transistor.

* Stability factor 's' :

It is defined as the ratio of small change in

collector current to the small change in reverse saturation current.

Note! $s' = \frac{\partial I_c}{\partial V_{BE}}$, $s'' = \frac{\partial I_c}{\partial \beta}$

(I_{c0} & β constant) (I_{c0} & V_{BE} are constant)

→ As we know that collector current expression

$$I_c = \beta I_B + (1+\beta) I_{cB0}$$

diff w.r.t I_c ,

$$1 = \beta \frac{dI_B}{dI_c} + (1+\beta) \frac{dI_{cB0}}{dI_c}$$

$$1 = \beta \frac{dI_B}{dI_c} + (1+\beta) \frac{1}{s}$$

$$s = \frac{1+\beta}{1 - \beta \frac{dI_B}{dI_c}}$$

* Note! the procedure to determine the stability factor s ,

Step 1: Apply KVL at i/p side, determine I_B

Step 2: Get $\frac{dI_B}{dI_c}$

Step 3: Sub $\frac{dI_B}{dI_c}$ in eq. $s = \frac{1+\beta}{1 - \beta \frac{dI_B}{dI_c}}$

Step 4: If s is independent of transistor parameter (β) it is a good method.

* Biasing techniques:

- There are 3 types of biasing techniques.
- (1) Fixed bias method (bias).
 - (2) Collector to base bias method.
 - (3) Voltage divider bias method or self bias method or emitter bias method.

(1) Fixed bias method:

Step-1:

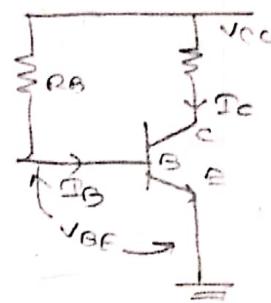
→ It consists of 2 resistors R_B & R_C .

→ Step-1:

By KVL at i/p side,

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



In above eq., V_{CC} , V_{BE} , R_B are fixed.

Hence I_B is also fixed. Therefore, it is called fixed bias technique.

Step-2: Diff. I_B w.r.t I_C ,

$$\Rightarrow \frac{dI_B}{dI_C} = 0$$

Step-3: By applying substituting $\frac{dI_B}{dI_C} = 0$ in

$$S = \frac{1 + \beta}{1 - \beta \frac{dI_B}{dI_C}} \Rightarrow 1 + \beta$$

→ Since, S is depending on β , it is a poor method.

(a) Advantages:

Simple circuit & cost is less.

(b) Disadvantages:

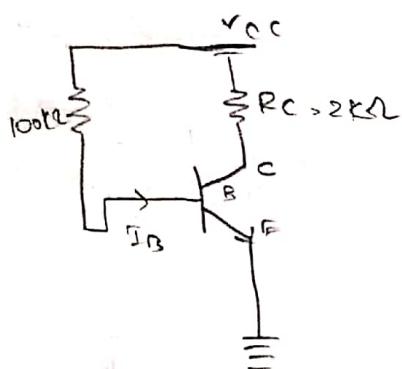
- Poor stability factor
- As $S \uparrow$, thermal stability is ↓.

→ By applying kV_L on o/p side,

$$V_{CC} = I_C R_C + V_{CE}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

a.



$B = 100$, find I_B , I_C , V_B , V_C , Q .

$$S = 1 + B$$

$$S = 101$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$= \frac{12 - 0.7}{100 \times 10^3} = 113 \mu A$$

$$I_C = 100 \times 113 \mu A$$

$$= 113 \times 10^{-4}$$

$$= 11.3 mA$$

$$V_{BE} = 0.7$$

$$V_B - V_E = 0.7$$

$$V_E = V_B - 0.7$$

$$V_B = 0.7 V$$

$$V_{CE} = ?$$

$$\Rightarrow I_C = \frac{V_{CC} - (V_{CE} + V_{CE(sat)})}{R_C}$$

$$\text{Hence } Q = (0.2 V, 5.9 V)$$

The transistor is operated in saturation reg.

$$V_{CE} = I_C R_C \quad I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$\Rightarrow V_{CC} - I_C R_C = V_{CE}$$

$$\Rightarrow 12 - (11.3 \times 10^{-3}) (2 \times 10^3) = V_{CE}$$

$$\Rightarrow V_{CE} = 12 - (11.3) 2$$

$$\Rightarrow V_{CE} = 12 - 22.6$$

$$\Rightarrow V_{CE} = -10.6 \text{ V}$$

$$\Rightarrow V_C = -10.6 \text{ V} \text{ since } V_E > 0.$$

$$Q = (-10.6, 11.3)$$

(2) Collector-base bias method :-

→ Here, feedback resistor is connected (R_B) to the collector & base terminals of transistor.

Step-1:

By applying KVL at i/p side,

$$V_{CC} = (I_B + I_C) R_C + I_B R_B + V_{BE}$$

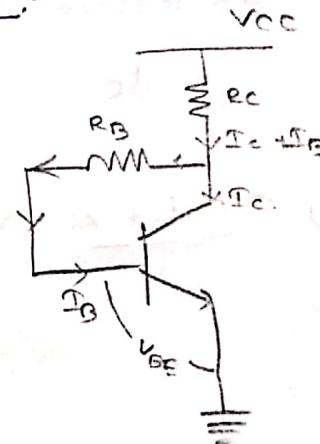
$$V_{CC} = I_B R_C + I_C R_C + I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B}$$

Step-2: Diff I_B w.r.t I_C ,

$$\frac{dI_B}{dI_C} = -\frac{R_C}{R_C + R_B}$$

Step-3: w.r.t $S = \frac{1+\beta}{1-\beta \left(\frac{-R_C}{R_C + R_B} \right)}$



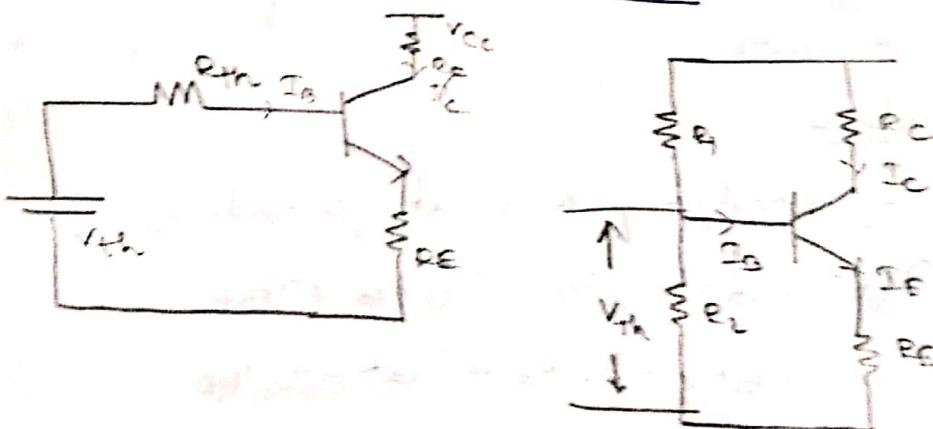
$$S = \frac{1 + \beta}{1 + \beta \frac{R_C}{R_C + R_B}}$$

$$\frac{1 + \beta \frac{R_C}{R_C + R_B}}{1 + \beta}$$

If $R_C \gg R_B \Rightarrow S \approx 1$

- Hence, comparatively C to B method is better than fixed bias method.
- This method is thermally stable.
- As we know that at temp T_0 , I_C is due to this $I_B \downarrow$ ($I_C + I_B$ is constant), hence $I_C \downarrow$. Therefore compensation takes place to stabilize I_C .

(3) Voltage divider bias method:



- R_1, R_2 provide proper biasing to circuit,
- R_E provides stability to the circuit.
- We need to get I_B first.
- To get I_B , the circuit can be modified by Thevenin's theorem (V_{th} is connected in series with R_{th}).

$$\gamma_{Th} = \frac{V_{cc} \cdot R_2}{R_1 + R_2}$$

$R_{Th} = R_1 \parallel R_2$ (V_{cc} is grounded, Hence R_1 & R_2 are grounded)

→ Step-1: By applying KVL at i/p side,

$$\gamma_{Th} = I_B R_{Th} + V_{BE} + I_E R_E$$

$$\gamma_{Th} = I_E R_{Th} + V_{BE} + I_B R_E + I_E R_E$$

$$I_B = \frac{\gamma_{Th} - V_{BE} - I_E R_E}{R_E + R_{Th}}$$

Step-2: Diff. I_B w.r.t I_C

$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_E + R_{Th}}$$

$$\text{Step-3: } S = \frac{1+\beta}{1-\beta\left(\frac{-R_E}{R_E+R_{Th}}\right)}$$

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E+R_{Th}}\right)}$$

If $R_E \gg R_{Th}$, $S \approx 1$.

- Hence, this method is the best one among the 3 methods.
- As temp ↑, I_C ↑, due to this $I_E \uparrow \Rightarrow V_E \uparrow$, this means $V_{BE} \downarrow$ (V_{BE}) Hence i/p current $I_B \downarrow$, I_C also ↓. Thereby, compensation takes place.
- Hence, it is also called self bias method, it is due to self stabilization occurred

at the emitter terminal.

- ** → If the transistor is operated in active region, consider $I_C = \beta I_B$ and if operated in saturated region ($V_{CEsat} < V_{CE} < V_{CC}$) consider $I_C + \beta I_B$. for active region

3/9/2019

Tuesday

* Compensation techniques:

- There are 3 types of compensation techniques.
- (1) Diode (2) Thermistor (3) Semistor.

(1) Diode compensation techniques:

- It consists of transistor, diode, R_E, R_C, R_E .

(a) → Here, the diode & transistor are made up of same material.

→ Hence, any losses in transistors, the same is applicable for diode.

$$\text{Eg. } I_{CO} = I_0$$

→ From fig, $I = I_B + I_0$

$$I_B = I - I_0 \rightarrow (1)$$

→ As temp \uparrow , the collector current I_C will \uparrow .

→ When the diode compensation technique is used, as temp \uparrow , reverse current I_{DR} due to this $I_B \uparrow$ (from (1)). Hence I_C also

$$[\because I_C = \beta I_B + (1+\beta) I_{CO}]$$
 thereby, compensation

takes place.

→ The above technique is known as diode compensation technique with variation in I_o .

(b) → As $T \uparrow$, $I_c \uparrow$ at the same time $\gamma_{BE} \downarrow$ so that

$I_B \downarrow$. Thereby I_c & compensation takes place. [$\because \gamma_{BE} \downarrow$ for every $^{\circ}\text{C} \Rightarrow \gamma_{BE} = -2.5 \text{ mV}/^{\circ}\text{C}$]

→ This method is known as diode compensation technique with variation in γ_{BE} .

(2) Thermistor compensation technique:

→ Thermistor is a -ve temperature coefficient device.

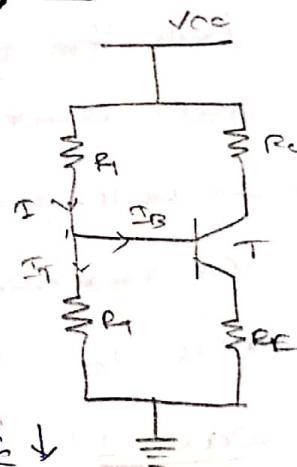
[As temp \uparrow , $R_T \downarrow$]

$$I = I_B + I_T$$

$$I_B = I - I_T$$

$$\rightarrow T \uparrow \xrightarrow{I_T \uparrow} R_T \downarrow \rightarrow I_T \uparrow \rightarrow I_B \downarrow \rightarrow I_c \downarrow$$

Hence compensation takes place.



(3) Sensistor compensation technique:

→ Sensistor is a +ve temperature coefficient device.

[As temp \uparrow , $R_s \uparrow$]

$$I_s = I + I_B$$

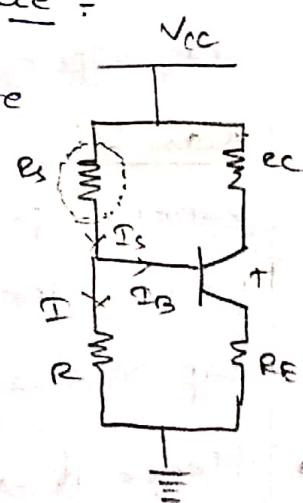
$$I_B = I_s - I$$

$$\rightarrow T \uparrow \rightarrow R_s \uparrow \rightarrow I_s \downarrow$$

\downarrow

$I_c \uparrow$ $I_c \downarrow \leftarrow I_B \downarrow$

Compensation.

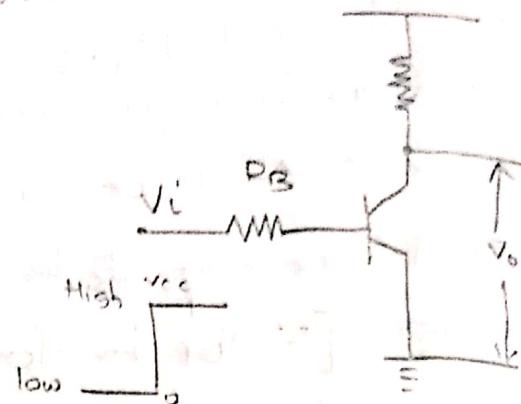


* Transistor as switch:

→ Apply ΔV_L ,
we get

$$V_{CC} = I_C R_C + V_O$$

$$V_O = V_{CC} - I_C R_C$$



→ As we know, there are 2 jns in a transistor,

(i) i/p jn (J_{FB}) (ii) o/p jn (J_{OB}) .

→ If both i/p & o/p jns are operated in FB mode, then the transistor is said to be in saturation region & acts as ON switch.

→ If both jns are operated in RB mode then the transistor is said to be in cutoff region & acts as OFF switch.

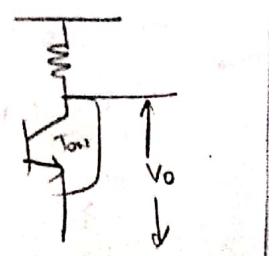
Case-1:

When i/p signal is operated in low level i.e., 0, the transistor gets into OFF position & the o/p voltage $V_O = V_{CC}$ $\because I_C = 0$

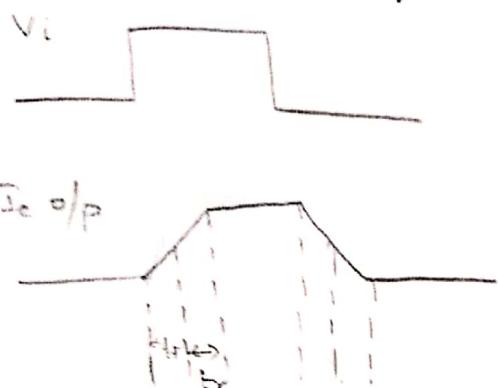
Case 2:

When i/p signal is operated in high level i.e., 1, the transistor gets into ON position o/p voltage $V_O = V_{CE(sat)}$

→ Hence it acts as an inverted switch.



* Transistor switching times:



(a) Delay time: (t_d)

Time taken by o/p current to reach 0 to 10% of its final value.

(b) Rise time: (t_r)

Time taken by o/p current to reach 10% to 90% of its final value.

(c) ON time: (t_{on})

Sum of rise time & delay time

(d) Storage time: (t_s)

Time required to remove excess minority charge carriers is called storage time.

(e) Fall time: (t_f)

Time required to reach 90% to 10% of its initial value.

(f) OFF time: (t_{off})

Sum of fall time & storage time