7.10 Interfacing CMOS and TTL Devices

Interfacing means connecting the output(s) of one circuit or system to the input(s) of another circuit or system that may have different electrical characteristics. When two circuits have different electrical characteristics direct connection cannot be made. In such cases driver and load circuits are connected through interface circuit. Its function is to take the driver output signal and condition it so that it is compatible with requirements of the load.

One must consider following important points while interfacing two circuits or systems.

- The driver output must satisfy the voltage and current requirements of the load circuit.
- The driver and load circuit may require different power supplies. In such cases the output of both circuit must swing between its specified voltage ranges.

7.10.1 TTL Driving CMOS

Here, TTL is a driver circuit and CMOS is a load circuit. The two circuits are from different families with different electrical characteristics. Therefore, we must check that the driving device can meet the current and voltage requirements of the load device.

Parameter	CMOS		TTL		
	4000B	74HC/HCT	74	74LS	74AS
$I_{IH \ (max)}$	1 μA	1 μA	40 μA	20 μA	200 μA
$I_{IL \ (max)}$	1 μA	1 μA	1.6 mA	0.4 mA	2 mA
$I_{OH \ (max)}$	0.4 mA	4 mA	0.4 mA	0.4 mA	2 mA
$I_{OL \ (max)}$	0.4 mA	4 mA	16 mA	8 mA	20 mA

Table 7.17 Input/output currents for standard devices with supply voltage of 5 V
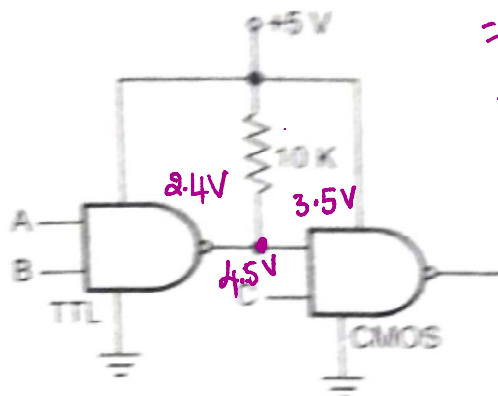
$$V_0 = V_{cc} - 10k \times I$$
$$= 5 - 10k\Omega \times \mu A$$
$$\approx '5V$$

$$V_{OH} (TTL) = 2.4 V$$
$$V_{IH} (CMOS) = 3.5 V$$

$$V_{OH}(TTL) < V_{IH} (CMOS)$$

TTL o/p must be raised to acceptable level.

TTL o/p raised by

Fig. 7.38 TTL driving CMOS using external pull-up resistor

level .
TTL o/p raised by
connecting pull up
resistor
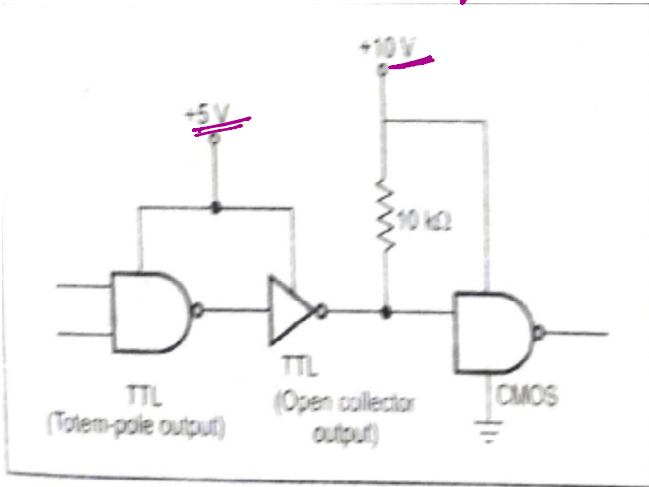
Method 1   open collector buffer as interface

Fig. 7.39 Open collector buffer used as interface circuit

$CMOS \rightarrow V_{DD} > 5V$

$TTL \rightarrow V_{cc} \le 5V$

TTL o/p can not be pulled
up to V_{DD}, so we can use
open collector buffer as an
interface between Totempole TTL
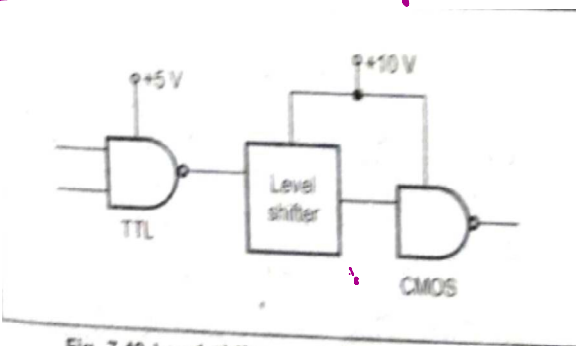and CMOS

Method 2   level shifter used as interface

Fig. 7.40 Level shifter used as interface circuit

Level translator take low voltage
input (TTL) and translate it to
high voltage o/p for CMOS

7.10.2 CMOS Driving TTL

Before we consider the problem of interfacing CMOS outputs to TTL inputs, it wil be helpful to review the CMOS output and TTL input characteristics for the two logi states.

For CMOS (4000B)	For TTL
$V_{OH(min)}$: 4.95 V	$V_{IH(min)}$: 2.0 V
$V_{OL(max)}$: 0.05 V	$V_{IL(max)}$: 0.8 V
$I_{OH(max)}$: 0.4 mA	$I_{IH(max)}$: 40 µA
$I_{OL(max)}$: 0.4 mA	$I_{IL(max)}$: 1.6 mA

Table 7.18

CMOS Driving TTL in the HIGH state : Above voltage parameters show that CMOS outputs can easily supply enough voltage (V_{OH}) to satisfy the TTL input requirement in the HIGH state (V_{IH}). The parameters also show that CMOS outputs can supply more than enough current (I_{OH}) to meet the TTL input current requirements (I_{IH}). Thus no special consideration is required for CMOS driving TTL in the HIGH state.
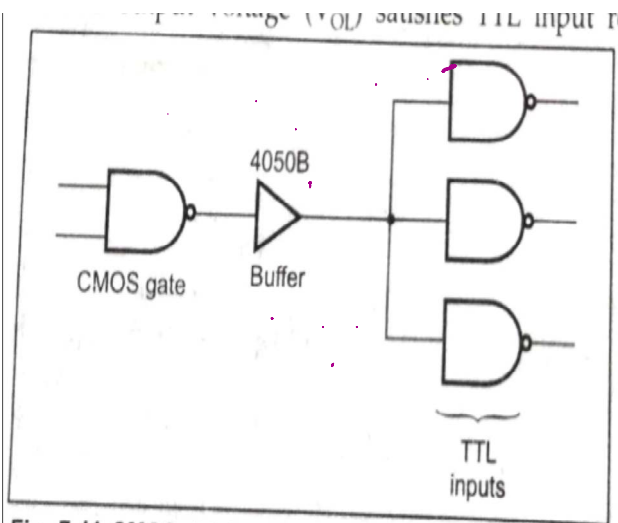
However, the current requirements in the LOW state are not satisfied. The TTL input has a relatively high input current in the LOW state (1.6 mA) and CMOS output current at LOW state (I_{OL}) is not sufficient to drive even one input of the TTL. In such situations some type of interface circuit is needed between the CMOS and TTL devices. Fig.

Fig. 7.41 CMOS driving TTL in LOW state using buffer

Fig. 7.42 Level translation using CMOS buffer
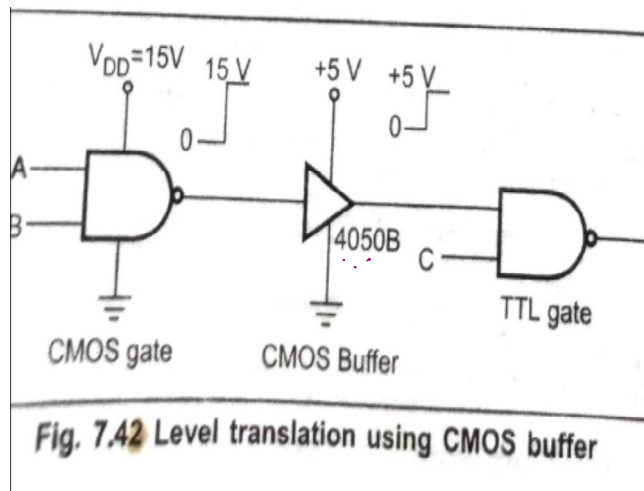
In Fig. 7.41 the CMOS 4050B, noninverting buffer is used as an interfacing circuit. It has an output current rating of $I_{OL\,(max)} = 3$ mA which satisfies the TTL input current requirement.