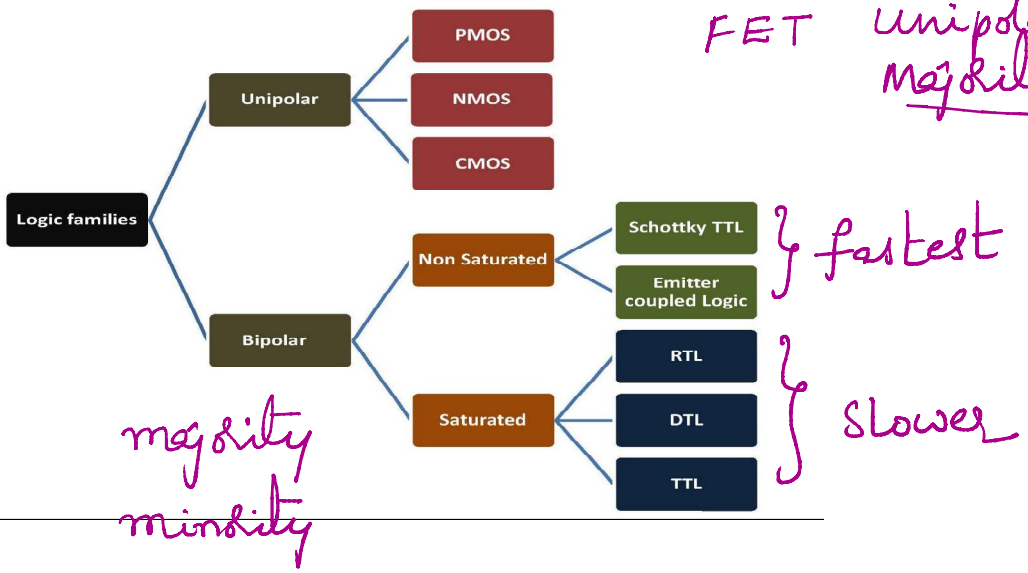
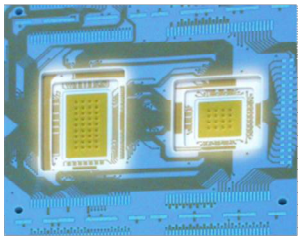
logic family_basics



- Early families (DTL, RTL)
- TTL
- Evolution of TTL family
- ECL
- CMOS family and its evolution

Integration Levels

- Gate/transistor ratio is roughly 1/10
  - SSI < 12 gates/chip
  - MSI < 100 gates/chip
  - LSI …1K gates/chip
  - VLSI …10K gates/chip
  - ULSI …100K gates/chip
  - GSI …1Meg gates/chip



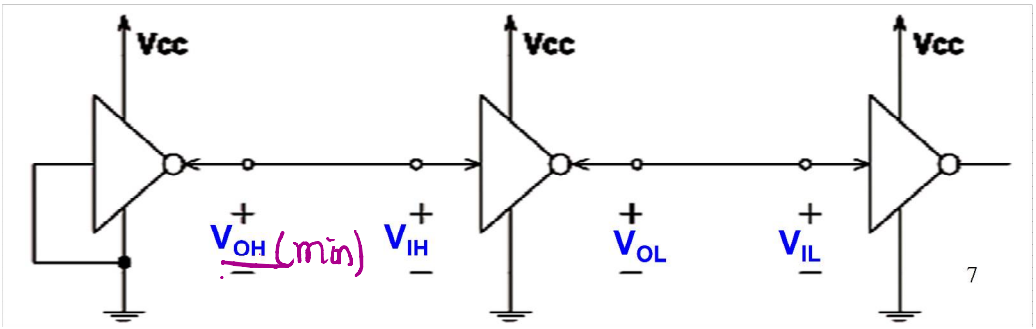
Logic families: V levels

V_{OH}(min) – The minimum voltage level at an output in the logical "1" state under defined load conditions

V_{OL}(max) – The maximum voltage level at an output in the logical "0" state under defined load conditions

V_{IH}(min) – The minimum voltage required at an input to be recognized as "1" logical state

V_{IL}(max) – The maximum voltage required at an input that still will be recognized as "0" logical state



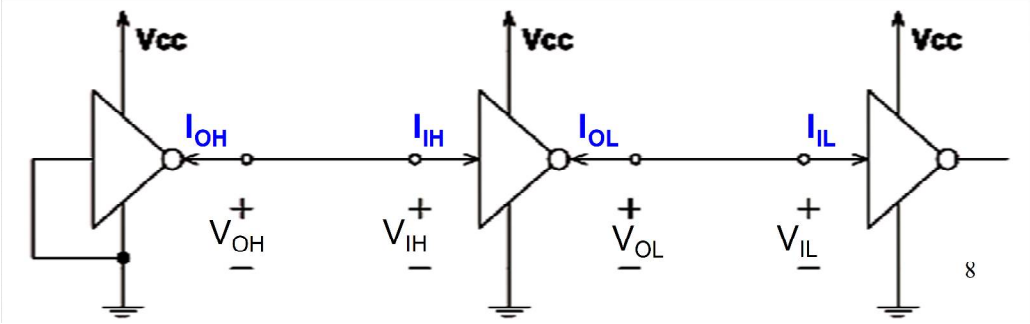
Logic families: I requirements

I_{OH} – Current flowing into an output in the logical "1" state under specified load conditions

I_{OL} – Current flowing into an output in the logical "0" state under specified load conditions

I_{IH} – Current flowing into an input when a specified HI level is applied to that input

I_{IL} – Current flowing into an input when a specified LO level is applied to that input



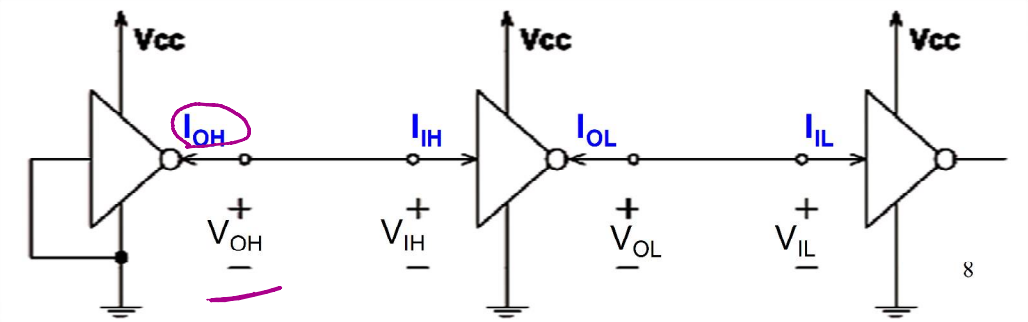
Logic families: I requirements

I_{OH} – Current flowing into an output in the logical "1" state under specified load conditions

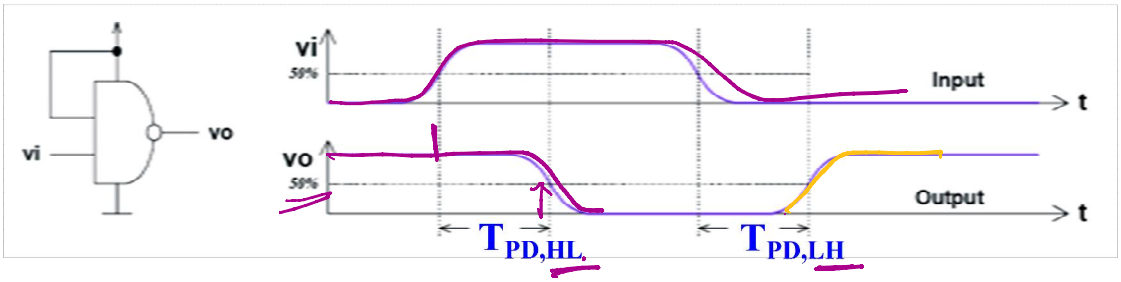
I_{OL} – Current flowing into an output in the logical "0" state under specified load conditions

I_{IH} – Current flowing into an input when a specified HI level is applied to that input

I_{IL} – Current flowing into an input when a specified LO level is applied to that input



Logic families: propagation delay

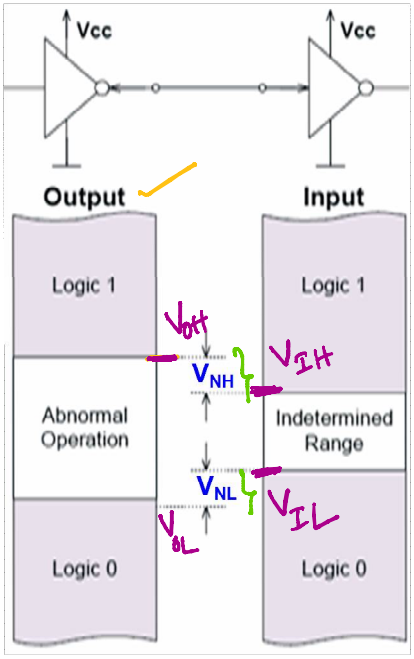


$T_{PD,HL}$ – input-to-output propagation delay from HI to LO output

$T_{PD,LH}$ – input-to-output propagation delay from LO to HI output

Speed-power product: $T_{PD} \times P_{avg}$

Logic families: noise margin



HI state noise margin:

$V_{NH} = V_{OH}(min) - V_{IH}(min)$

LO state noise margin:

$V_{NL} = V_{IL}(max) - V_{OL}(max)$

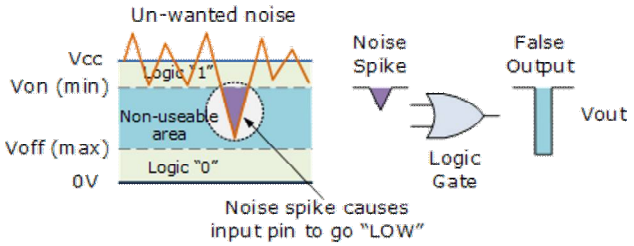
$V_{OH} > V_{IH}$

Noise margin:

$V_N = min(V_{NH}, V_{NL})$

$V_{IL} > V_{OL}$

Digital Logic Gate Noise Immunity



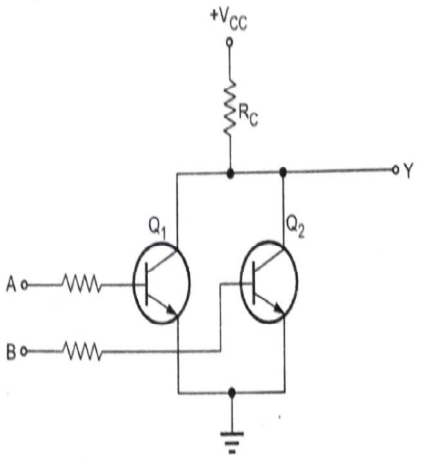
7.2.6 Speed Power Product (Figure of Merit)

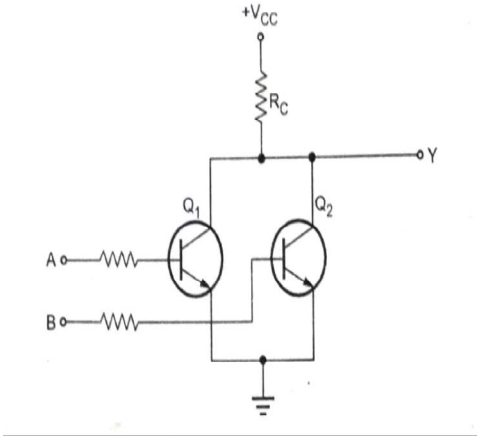
In general, for any digital IC, it is desirable to have shorter propagation delays (higher speed) and lower values of power dissipation. There is usually a trade-off between switching speed and power dissipation in the design of a logic circuit i.e. speed is gained at the expense of increased power dissipation. Therefore, a common means for measuring and comparing the overall performance of an IC family is the **speed-power product (SPP). It is also called Figure of Merit.**

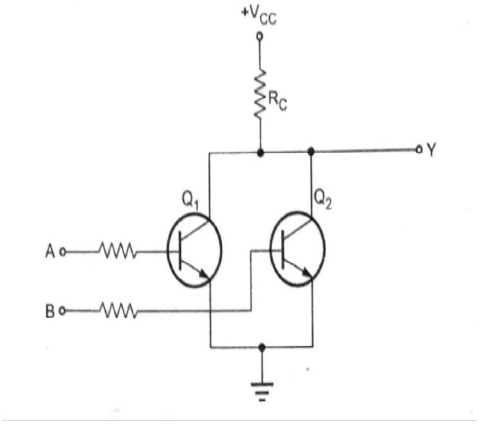
Actually, the speed-power product is computed as the product of propagation delay and average power dissipation, so the smaller the product, the better the overall performance. Notice that the product of propagation delay in seconds and power dissipation in watts (joules per second) has the units of energy - i.e. joules (J).

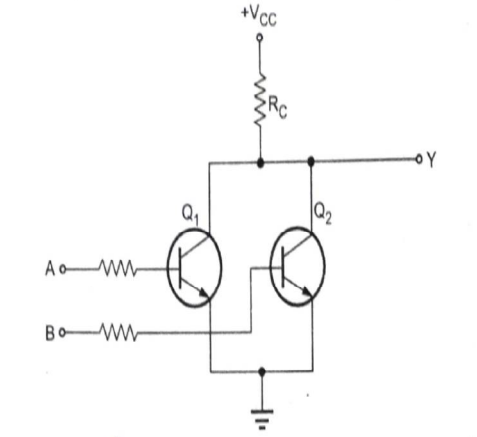
∴ Speed-power product (J) = Propagation delay (Seconds) × Power dissipation (Joules/seconds)

RTL logic family



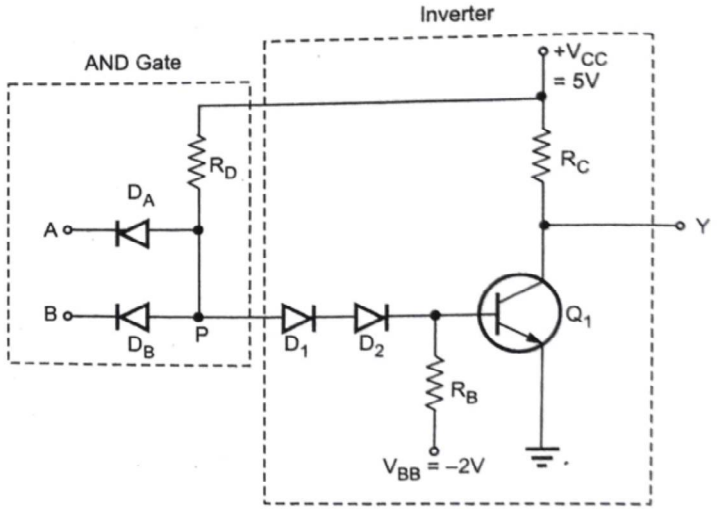


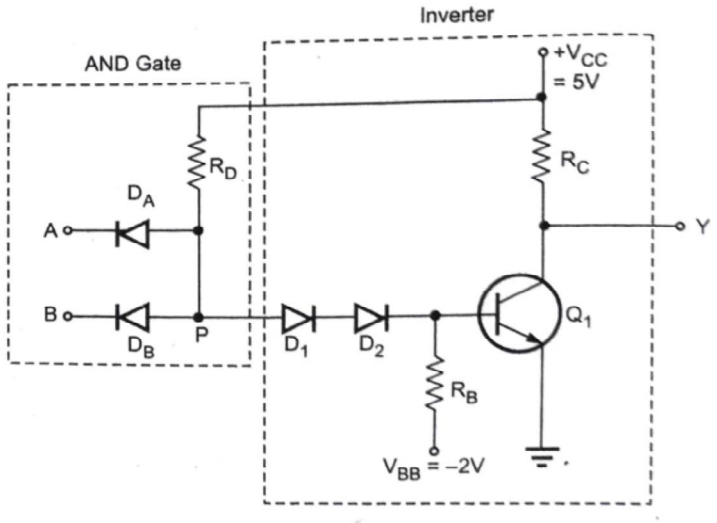


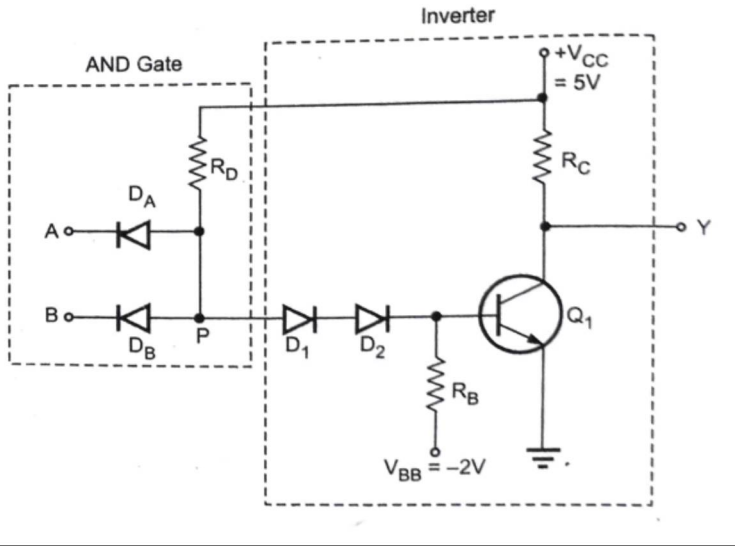


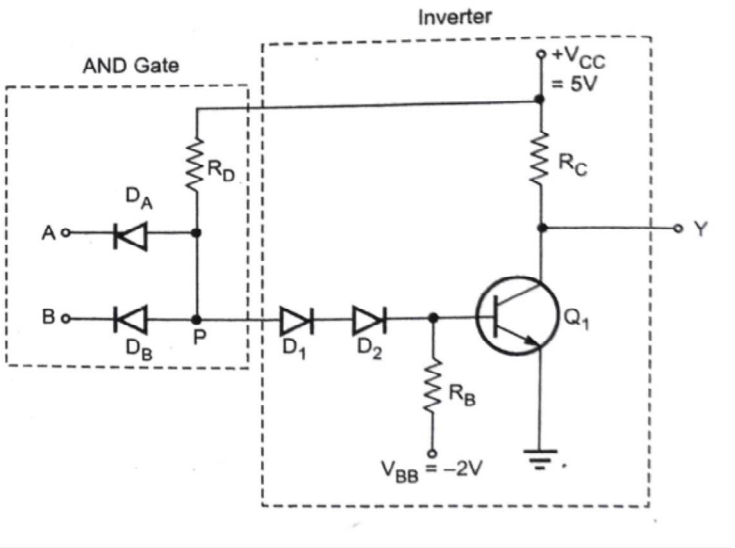
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

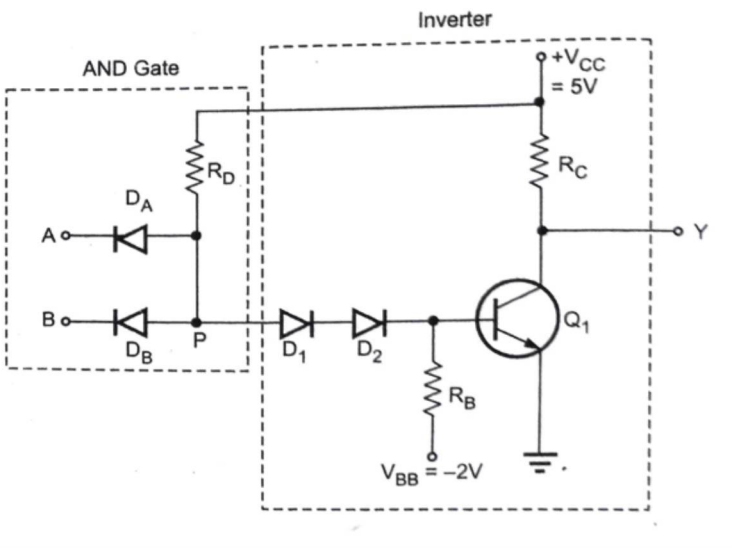
Parameter	Value
Propagative Delay	12 nsec
Power Dissipation	30-100 mW
Noise Margin	0.2 volts
Fan-out	4



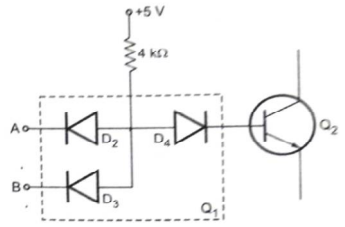


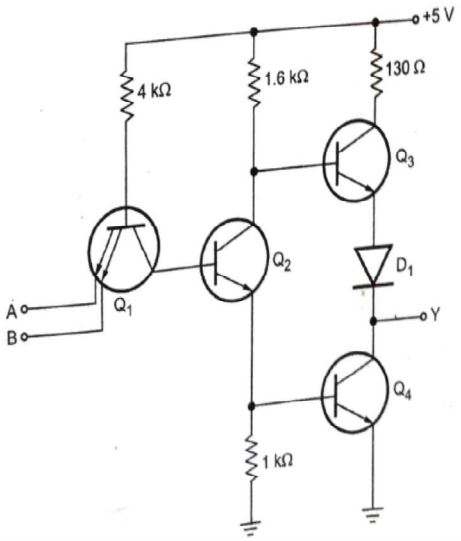

Inverter
AND Gate
+V_CC
= 5V
R_D
R_C
D_A
A
Y
B
D_B
P
D_1
D_2
Q_1
R_B
V_BB = –2V

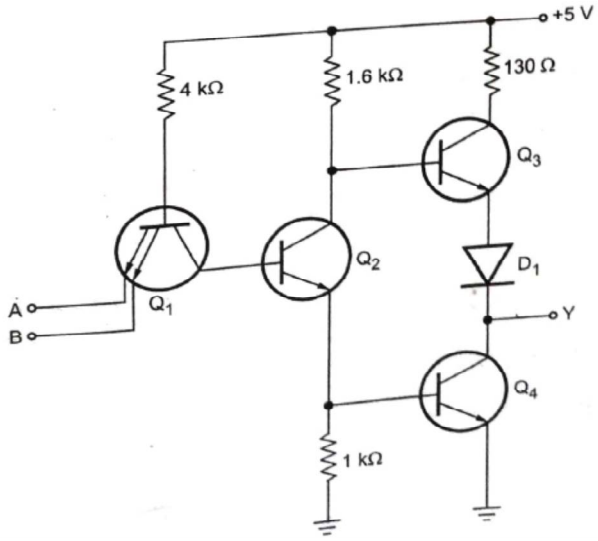

Inverter
AND Gate
+V_CC
= 5V
R_D
R_C
D_A
A
Y
B
D_B
P
D_1
D_2
Q_1
R_B
V_BB = –2V

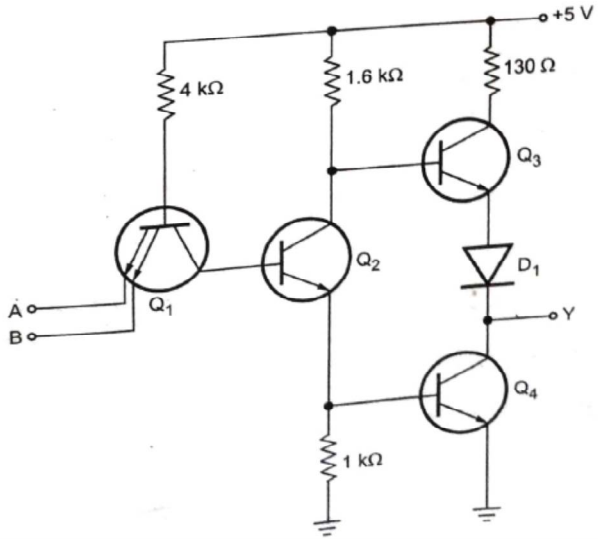

Inverter
AND Gate
+V_CC
= 5V
R_D
R_C
D_A
A
Y
B
D_B
P
D_1
D_2
Q_1
R_B
V_BB = –2V

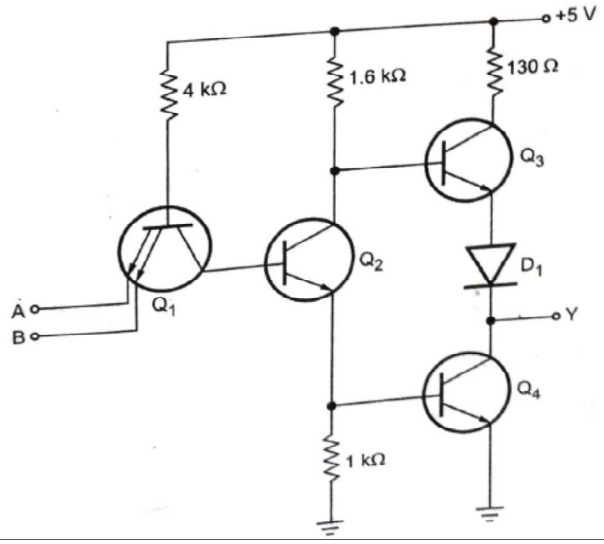
Parameter	Value
Power dissipation	60 mW
Propagation Delay	30 nsec
Noise Margin	0.7 volts
Fan out	8

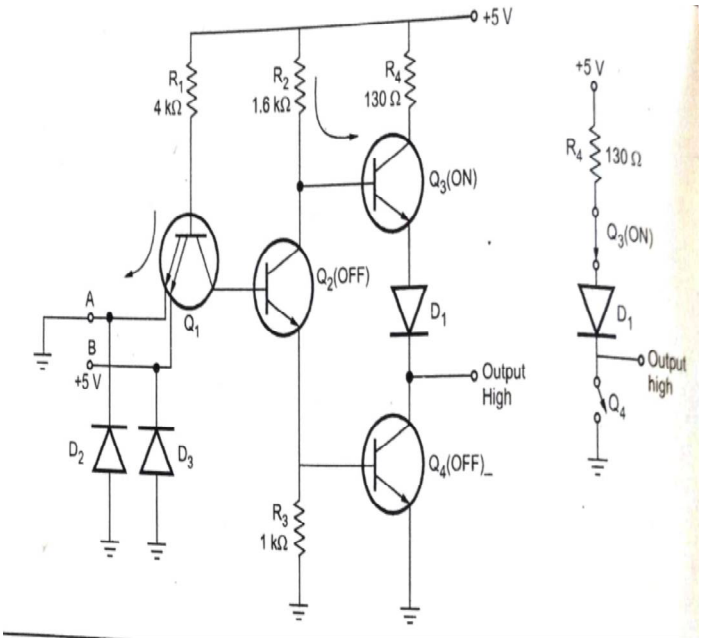


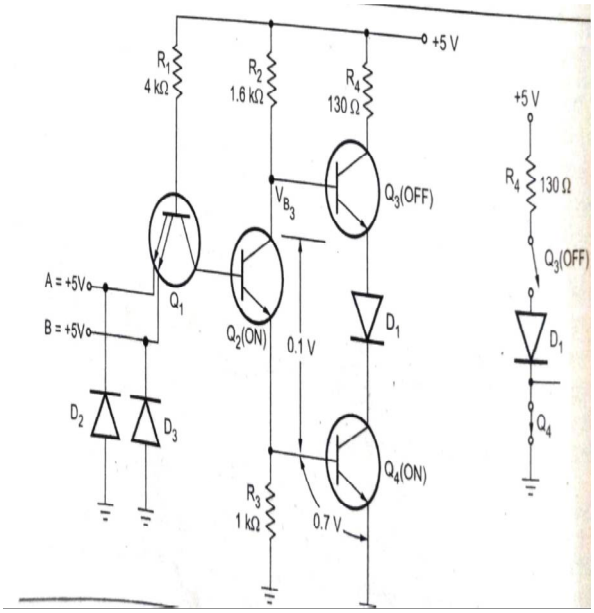


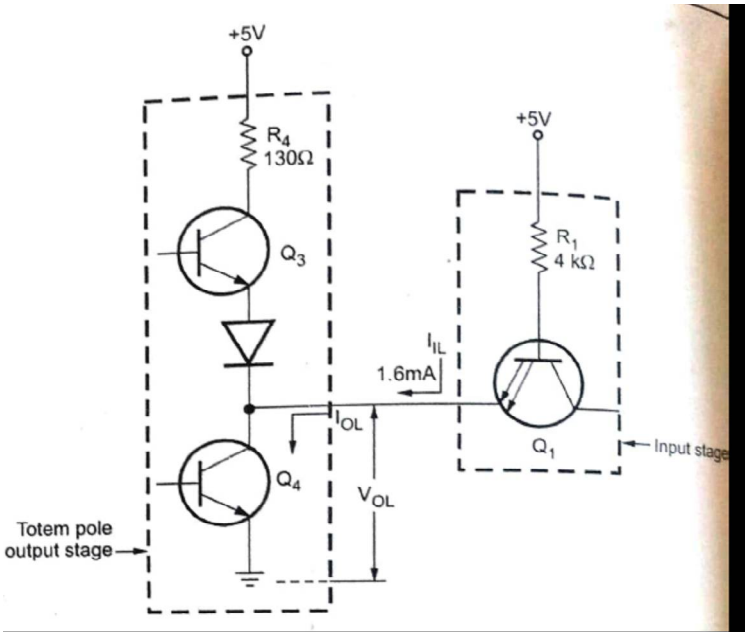

+5 V
4 kΩ
1.6 kΩ
130 Ω
Q3
Q2
D1
Q1
A
B
Y
Q4
1 kΩ

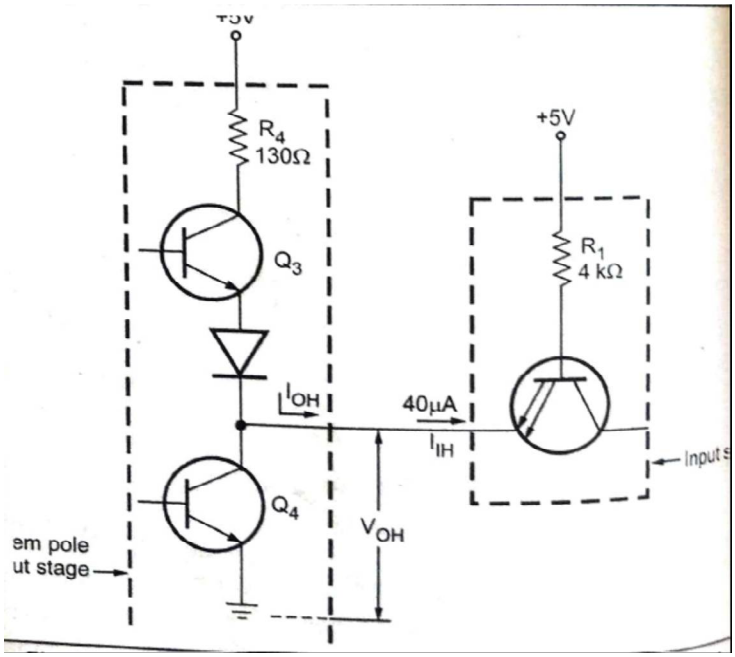

+5 V
4 kΩ
1.6 kΩ
130 Ω
Q3
Q2
D1
Q1
A
B
Y
Q4
1 kΩ


+5 V
4 kΩ
1.6 kΩ
130 Ω
Q3
Q2
D1
Q1
A
B
Y
Q4
1 kΩ


+5 V
R1
4 kΩ
R2
1.6 kΩ
R4
130 Ω
Q3(ON)
Q2(OFF)
A
B
+5 V
Q1
D1
Output
High
D2
D3
Q4(OFF)
R3
1 kΩ
+5 V
R4
130 Ω
Q3(ON)
D1
Output
high
Q4


+5 V
R1
4 kΩ
R2
1.6 kΩ
R4
130 Ω
Q3(OFF)
VB3
A = +5V
B = +5V
Q1
Q2(ON)
0.1 V
D1
D2
D3
Q4(ON)
R3
1 kΩ
0.7 V
+5 V
R4
130 Ω
Q3(OFF)
D1
Q4





logic
family_basic

Logic families

Logic family explains, how to implement a logic device using active device

→ Logic families classification is based on the active device used

→ propagation delay is related to internal capacitance effects

→ * In MOSFET, internal capacitance is in the range of fF
* In BJT, internal capacitance is in the range of nF and pF
* As capacitance is increased, charging and discharging time increases and hence propagation delay is more in FET

→ BJT logic family having less propagation delay with more power consumption compared to unipolar (FET) logic family.

→ power consumption is higher in BJT

Bipolar logic family

- Saturated logic family
  - ↓
  - BJT operating b/w cutoff & saturation regions
- Non Saturated logic family
  - ↓
  - BJT operating b/w cutoff & active region