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-: HAND WRITTEN NOTES:-

OF

ELECTRONICS & COMMUNICATION ENGINEERING

(1)

-: SUBJECT:-

ANALOG ELECTRONICS

2

2

Syllabus :-

1) Op-Amp
2) Linear Wave Shaping circuit <Taub>
3) Schimitt Trigger
4) Waveform Generator
-- Multivibrators
- Bistable Multivibrator.
- Monostable "
- Astable " (Square Wave Generator)
- Triangular Wave Generator.

5) Diode Circuits
- Rectifiers & filters
- Precision Rectifiers
- Clipper & clampers
- Voltage Doublers.

6) Bipolar Junction Transistors.
- Transistor Biasing & Stablisation
- Current Mirror Circuit
- Voltage Regulator

7) Multivibrator by using BJT. <Taub>

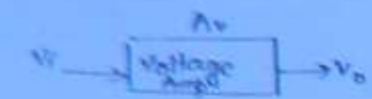
8) Amplifiers -
- Low frequency Analysis of BJT.
- High " " "
- Multistage Amp.
- Feedback " .
- Low frequency analysis of FET
- Oscillators (Sinusoidal)
- Power Amplifiers

9) 555 - Timer.
- Multivibrators

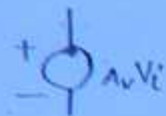
Books
- Millman - Halkias - Yellow Pad.
- Pulse Digital & Switching circuit
- Millman & Taub

Operational Amplifier :-

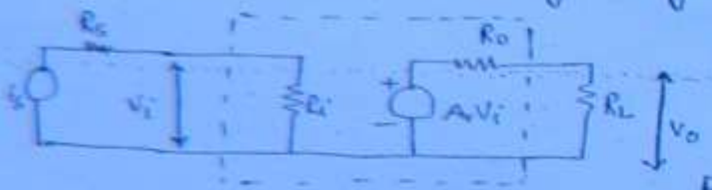
(4)

→ 

→ $A_v = \frac{V_o}{V_i}$ = Gain.

→ Op Amp is a VCVS. — 

→ Equivalent circuit for any voltage amplifier–



R_i = i/p resistance of amplifier.
R_o = o/p " " " .

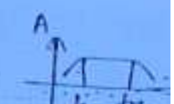
for Ideal value –

$R_i = \infty$
$R_o = 0$
$A_v = \infty$
$BW = \infty$
$G.BW = \infty$

**

→ $R_i >>> R_s$, so that $V_s \simeq V_i$

→ $R_o <<< R_L$, so that $V_o \simeq A_vV_i$

* To get $A_v \to \infty$, multistaging is done but the BW will ↓.
* BW is defined as the freq. range for which gain is independent of frequency. 

→ Gain of practical OP-Amp = 10^6.

→ Op-Amp is a multistage Amplifier.

→ $\boxed{\text{Gain} \times \text{BW} = \text{constant}}$; Ideally G.BW should be ∞.

(internal capacitance)
* BW cannot be ∞ due to the presence of C_T & C_d in multistage amplifiers.

→ for practical Op-Amp; $G.BW = 10^6$ Hz.
→ Max. possible $BW = 10^6$ Hz for gain = 1.

→ Negative feedback will ↓ the gain of the system and ↑ the B/W and hence ↑ the stability of the system.

8

Op-Amp Imp. Points –

(i) It is a monolithic IC or a semiconductor chip fabricated with VLSI by using epitaxial method

(ii) In epitaxial method, entire IC is fabricated on single crystal of Si.

(iii) It is basically a voltage controlled device or voltage amplifier or VCVS.

(iv) Popularly used op-Amp is IC-741. for IC-741, maximum power supply is ±15V.

(v) Op-Amp is versatile, predictable and economic system building block as small size, high reliability, reduced cost, low offset voltage & current and low power consumption.

(vi) It is originally invented to execute the mathematical operations, hence called op-amp.

(vii) It is a direct coupled, high gain amplifier, ie, open loop gain is very high, therefore frequency stability of the signal is less and to compensate this, small amount of -ve feedback is added so that the gain is reduced & the frequency stability increases (since BW ↑)

(viii) Op-Amps are generally operated under closed loop condition, ie, by applying -ve feedback.

(ix) In an Op-Amp, Gain × BW = constant.

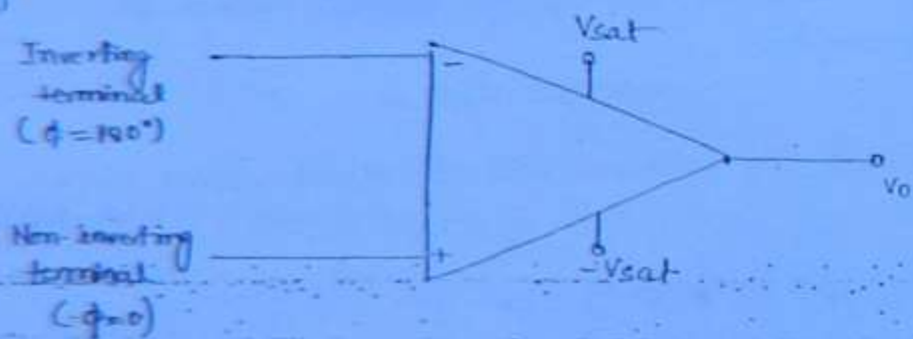
Characteristic of Operational Amplifier

6

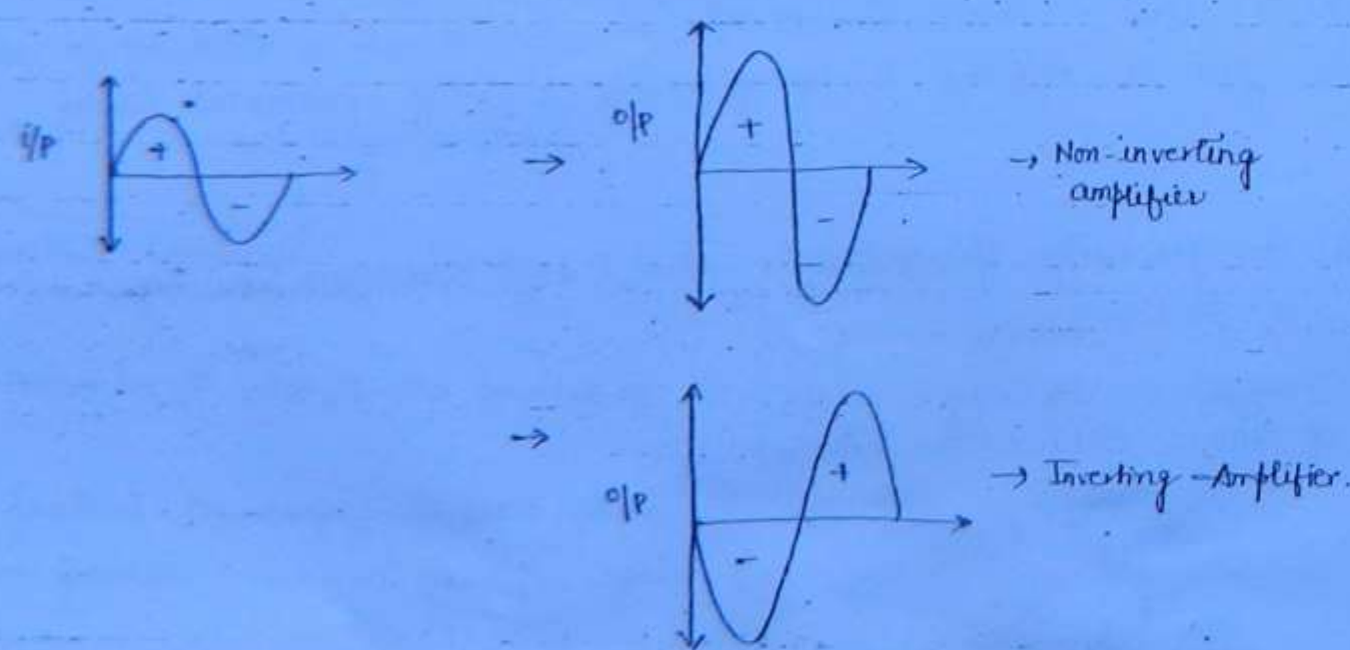
Characteristic	Ideal	Practical
- Voltage Gain, A_v	∞	10^6
- Input Resistance, R_i	∞	$1 M\Omega$
- output Resistance, R_o	0	$10 - 100 \Omega$
- G.BW	∞	$10^6 Hz$
- BW	∞	$10^6 Hz$ (for Gain = 1)
- CMRR	∞	10^6 or 120 dB
- Slew Rate [SR]	∞	$80 V/\mu sec$.

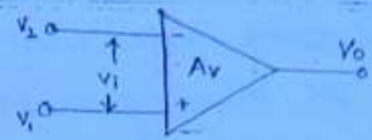
→ It is also referred as Basic linear Integrated Circuit.

Symbol :-



ϕ = phase shift





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Case 1 :- When $V_1 \neq 0$, $V_2 = 0$, then $V_0 > 0$

Case 2 :- When $V_1 \neq 0$; $V_2 \neq 0$ and $V_1 > V_2$, then $V_0 > 0$.

Case 3 :- When $V_1 = 0$, $V_2 \neq 0$, then $V_0 < 0$

Case 4 :- When $V_1 \neq 0$; $V_2 \neq 0$ and $V_2 > V_1$, then $V_0 < 0$.

Representation of Gain →

$|A_v| = 10^6$

Case 1 —

**

$\boxed{V_i = V_1 - V_2 \;;\; V_0 = A_v V_i = A_v(V_1 - V_2)}$ → If we represent like this then $A_v = 10^6$, i.e., $A_v > 0$

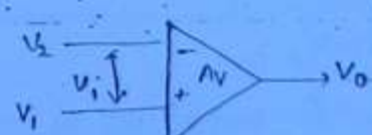
Case 2 :- $\boxed{V_i = V_2 - V_1 \quad V_0 = A_v V_i = A_v(V_2 - V_1)}$

**

then for this representation, $A_v = -10^6$, i.e., $\boxed{A_v < 0}$ *

When $A_v \to \infty$.

* $A_v \to \infty$



$V_i = V_1 - V_2$

$V_0 = \text{finite} \Rightarrow V_i = V_0/\infty = 0$.

$\Rightarrow V_1 = V_2$.

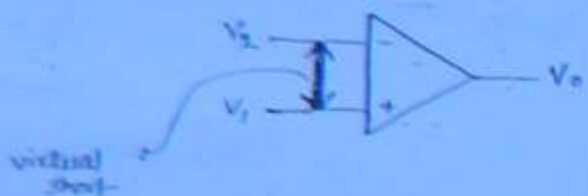
→ There is finite o/p w/o any input.

→ Now, if we attach any voltage source at V_1, the same will appear at V_2 ($\because V_1 = V_2$): but $R_i = \infty$ (ideally), hence they should be OC.

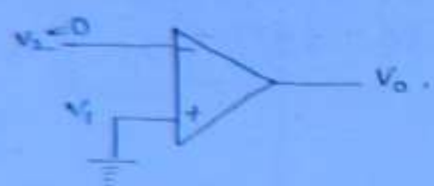
but they are behaving as sc. This condition is called Virtual Short, i.e., even though they are not physically short, they are behaving as short.

$R_i = \infty$

Symbol for Virtual Short –

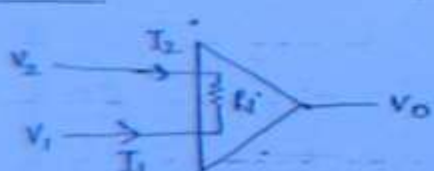


→ If we ground V_1, i.e., connect $V_1 = 0$, then V_2 will also become 0V. This is called virtual ground. It is a special case of virtual short.



Virtual Ground Process

→ When $R_i = \infty$ –



for $R_i = \infty$,
$I_1 = I_2 = 0$.

→ Internal power consumption ≈ 0.

Eg $V_o = 5V$ and $A_v = 10^6$, $R_i = 10^6 \Omega$

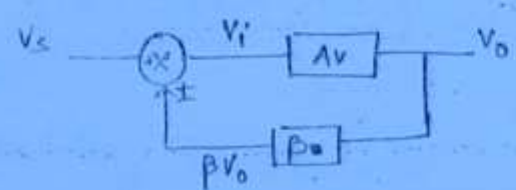
$$\Rightarrow V_i = \frac{V_o}{A_v} = 5\mu V \approx 0.$$

$$I_i = \frac{V_i}{R_i} = 5pA \approx 0$$

→ If the gain in the given problem is ↑ (very high), then we can use the concept of virtual ground. It is an approximate concept.

→ $V_s = V_i \longrightarrow \boxed{A_v} \longrightarrow V_o$ $A_{OL} = A_v \rightarrow$ open loop system.

$$A_{OL} = A_v = \frac{V_o}{V_i} = \frac{V_o}{V_s} \quad ; \quad \because V_s = V_i$$

→ 

$V_i = V_s \pm \beta V_o$

$$V_i = \begin{cases} \cdot\ V_s + \beta V_o \rightarrow \text{+ve feedback} \\ \cdot\ V_s - \beta V_o \rightarrow \text{-ve feedback.} \end{cases}$$

$$V_o = (V_s \pm \beta V_o) \cdot A_v$$

For +ve feedback –

$$\boxed{A_{CL} = \frac{V_o}{V_s} = \frac{A_v}{1 - \beta A_v} > A_v}^{*}$$ → closed loop Gain for +ve feedback

for -ve feedback –

$$\boxed{A_{CL} = \frac{V_o}{V_s} = \frac{A_v}{1 + \beta A_v} < A_v}^{*}$$ → closed loop gain for -ve feedback

→ +ve feedback is used in oscillators & -ve feedback is used in amplifier.

* Op-Amp with -ve feedback

→ $|A_{CL}| << |A_{OL}|$

we can assume $A_{OL} = A_v \rightarrow \infty$

∴ Virtual Ground process is valid.

Op-Amp with +ve feedback.

→ $|A_{CL}| >> |A_{OL}|$

we can assume $A_{OL} = \infty$, but we can't assume $A_{CL} = \infty$,

∴ Virtual ground process is invalid.

Mode of Operation

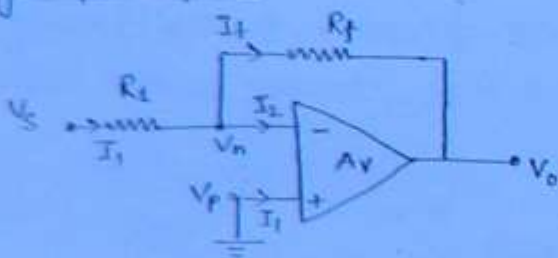
(i) Inverting Mode –

→ Phase shift = 180°

(ii) Non-Inverting Mode → ($\phi = 0°$)

(iii) Differential Mode ⇒ $V_0 \propto [V_1 - V_2]$

Inverting Op-Amp –



→ Negative feedback

→ $|A_{CL}| << |A_{OL}|$ ⇒ we can apply V.G.P.

⇒ $V_p = V_n = 0$.

→ ∵ $R_i = \infty$ ⇒ $I_2 = I_1 = 0$.

→ Incoming current = outgoing current

⇒ $I = I_f + I_2$

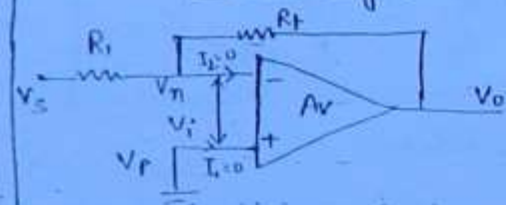
⇒ $\frac{V_s - V_n}{R_1} = \frac{V_n - V_0}{R_f} + 0$

⇒ $\frac{V_s}{R_1} = -\frac{V_0}{R_f}$

⇒ $\boxed{A_{CL} = \frac{V_0}{V_s} = \frac{-R_f}{R_1}}$

⇒ $\boxed{\phi = 180°}$

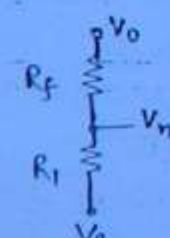
Exact Analysis



$V_i = V_p - V_n$; ⇒ {$A_V > 0$}

$V_0 = A_V [V_p - V_n]$ —(1)

$V_p = 0$ —(2)



$\frac{V_n - V_0}{R_f} + \frac{V_n - V_s}{R_1} = 0$

⇒ $V_n \left[\frac{1}{R_1} + \frac{1}{R_f}\right] = \frac{V_0}{R_f} + \frac{V_s}{R_1}$

⇒ $\boxed{V_n = \frac{V_0 R_1}{R_1 + R_f} + \frac{V_s R_f}{R_1 + R_f}}$

continued

$$I_f = I_1 + I_2 + I_3$$

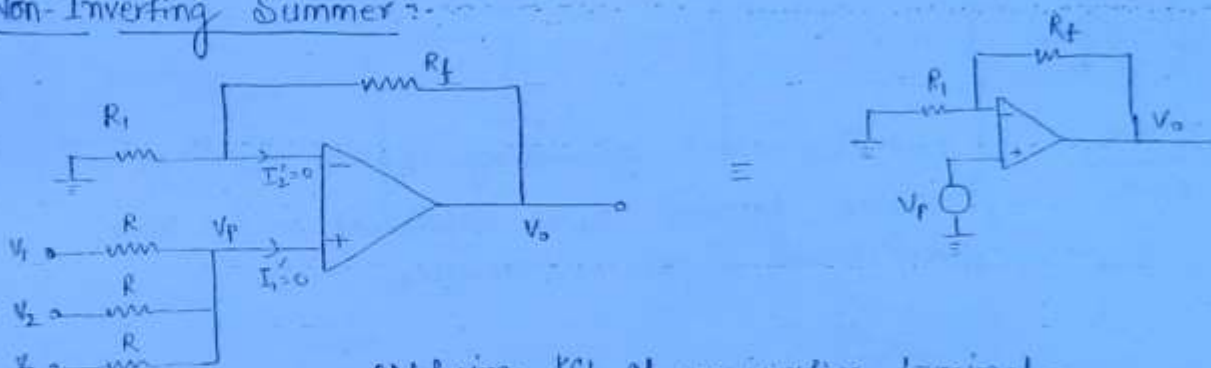
$$\frac{V_n - V_o}{R_f} = \frac{V_1 - V_n}{R_1} + \frac{V_2 - V_n}{R_2} + \frac{V_3 - V_n}{R_3}$$

$$\Rightarrow \boxed{V_o = -R_f\left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right]}$$

When $R_f = R_1 = R_2 = R_3$ –

$$\boxed{V_o = -[V_1 + V_2 + V_3]} \qquad \boxed{\phi = 180^\circ}$$

Non-Inverting Summer :-



Applying KCL at non-inverting terminal –

$$\frac{V_P - V_1}{R} + \frac{V_P - V_2}{R} + \frac{V_P - V_3}{R} = 0$$

$$\Rightarrow V_P = \frac{V_1 + V_2 + V_3}{3}$$

Now, $$\frac{V_o}{V_P} = 1 + \frac{R_f}{R_1}$$

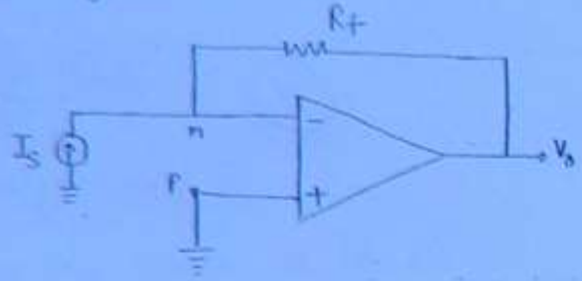
$$\Rightarrow \boxed{V_o = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{V_1 + V_2 + V_3}{3}\right)} \qquad \boxed{\phi = 0^\circ}$$

If $R_f = 2R_1$;

$$\boxed{V_o = [V_1 + V_2 + V_3]}$$

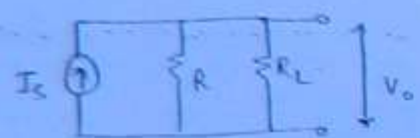
Current to Voltage Converter :-

(12)



→ $V_P = V_n = 0$

→ $\frac{V_n - V_0}{R_f} = I_S \Rightarrow \boxed{V_0 = -I_S \cdot R_f}$ → {V_0 is independent of R_L and hence it is a convertor.}



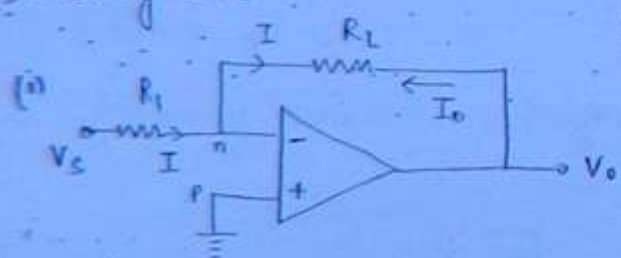
$V_0 = \frac{I_S \cdot R R_L}{R + R_L}$ ⇒ but this is not converting I_s into a voltage source because V_0 is dependent on R_L. Hence, given circuit is not a converter.

Voltage to Current Converter :-

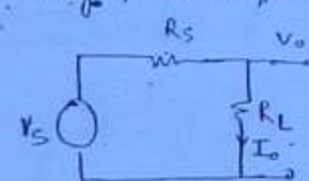
{It is standard convention to take load current I_0 in direction away from output voltage}

(a) Floating load —

(i)



{i.e., I_0 leaving from V_0}



$\frac{V_0}{R_L} = I_0 = \frac{V_S}{R_S + R_L}$

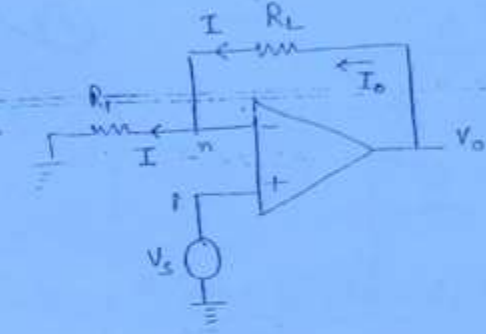
∴ I_0 depends on R_L, hence not a converter.

$I = \frac{V_S - 0}{R_1} \Rightarrow I = \frac{V_S}{R_1}$

$$\boxed{I_0 = -I = -\frac{V_S}{R_1}}$$

→ I_0 = output current independent of R_L.

(ii)



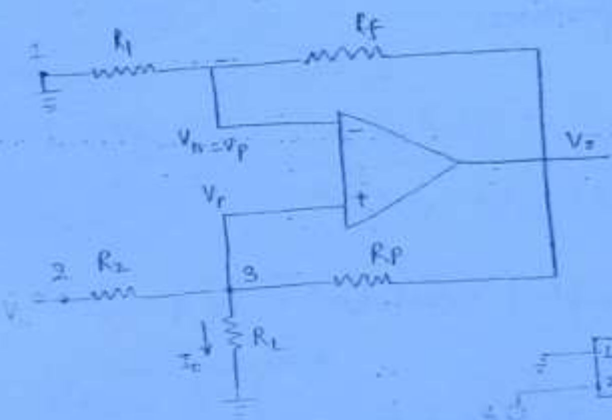
$V_n = V_s$ —①

$\frac{V_s - 0}{R_1} = I$

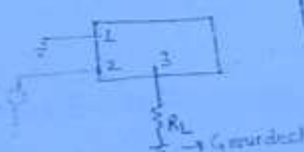
$\Rightarrow \boxed{I_o = I = \frac{V_s}{R_1}}$

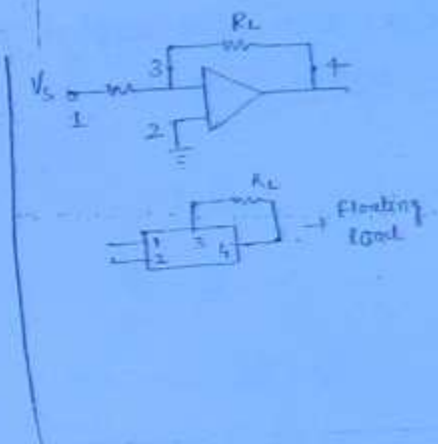
(b) Grounded Load :-

(i)



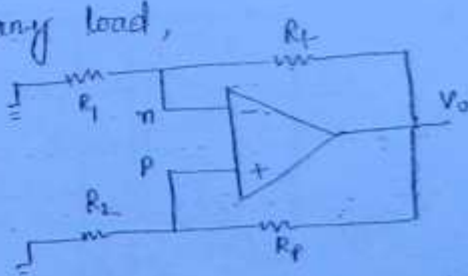
Circuit I





In the above ckt, +ve as well as -ve feedback is present. For the stability system should have -ve feedback and hence -ve feedback should be more than +ve feedback

→ Without any load,



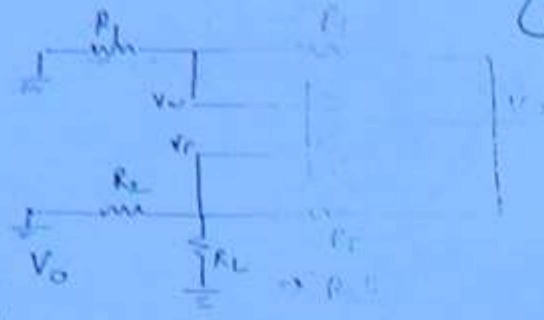
$V_n = \frac{R_1}{R_1 + R_f} V_o$

$V_p = \frac{R_2}{R_2 + R_p} V_o$

for stability, $V_n \geq V_p$ (-ve feedback more than +ve feedback)

$\Rightarrow \frac{R_1}{R_1 + R_f} \geq \frac{R_2}{R_2 + R_p}$

After R_L,



$$R_2' = R_2 \parallel R_L < R_2$$

$$V_f' = \frac{R_2'}{R_2'+R_f} V_0 = \frac{1}{1 + R_f/R_2'}$$

Now $R_2' < R_2$ and hence $V_f' < V_f$ $\Rightarrow$ +ve feedback ↓ which favourable for stability.

Hence, even after applying R_L, if original condition [illegible] then the system will remain in -ve feedback.

Now, from circuit I —

$$I_0 = \frac{V_f}{R_L} \quad \text{—— (1)}$$

$$V_f = V_n \quad \text{—— (2)} \qquad \{\text{by concept of virtual short}\}$$

applying KCL at inverting terminal —

$$\frac{V_f - [\text{illegible}]}{R_1} [\text{illegible}]$$

$$\Rightarrow \quad V_0 = \left[1 + \frac{R_f}{R_1}\right] V_f \quad \longrightarrow (3)$$

KCL at non-inverting terminal —

$$\frac{V_f - V_s}{R_2} + \frac{V_f - 0}{R_L} + \frac{V_f - V_0}{R_f} = 0$$

$$\Rightarrow V_f \left(\frac{1}{R_2} + \frac{1}{R_L} + \frac{1}{R_f} \right) - \frac{V_s}{R_2} - \frac{V_0}{R_f} = 0 \quad \text{—— (4)}$$

from (3) & (4) —

$$\Rightarrow \quad V_f \left(\frac{1}{R_2} + \frac{1}{R_L} + \frac{1}{R_f} \right) - \frac{1}{R_f}\left[1 + \frac{R_f}{R_1}\right] V_f = \frac{V_s}{R_2}$$

15

$$\Rightarrow V_P\left[\frac{1}{R_2}+\frac{1}{R_L}+\cancel{\frac{1}{R_P}}-\cancel{\frac{1}{R_P}}-\frac{R_f}{R_1R_P}\right]=\frac{V_s}{R_2}$$

$$\Rightarrow V_P\left[\frac{R_1R_PR_L+R_1R_2R_P-R_fR_2R_L}{R_1R_P\cancel{R_2}R_L}\right]=\frac{V_s}{\cancel{R_2}}$$

$$\Rightarrow \boxed{V_P=\frac{V_s R_1R_PR_L}{R_L[R_1R_P-R_2R_f]+R_1R_2R_P}}$$

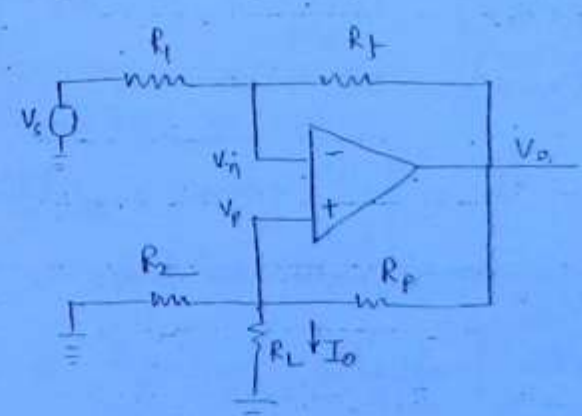
$$I_o=\frac{V_P}{R_L}=\frac{V_s R_1R_P}{R_L[R_1R_P-R_2R_f]+R_1R_2R_P}$$

If $R_1R_P=R_2R_f$

or $\boxed{\frac{R_P}{R_2}=\frac{R_f}{R_1}}$ **imp → Balanced Bridge condition

then, $\boxed{I_o=\frac{V_s}{R_2}}$ **imp

(ii)



Prove that if $\frac{R_f}{R_1}=\frac{R_P}{R_2}$ then $I_o=-\frac{V_s}{R_2}$

Applying KCL at V_P —

$$V_P\left[\frac{1}{R_2}+\frac{1}{R_L}+\frac{1}{R_P}\right]=\frac{V_o}{R_P} \quad — ①$$

Sol^n: $V_n=V_P$;

$$\frac{V_P}{R_L}=I_o \quad — ②$$

Applying KCL at V_n —

$$\frac{V_p - V_s}{R_1} + \frac{V_p - V_o}{R_f} = 0 \quad -(3)$$

$$\Rightarrow V_p\left[\frac{1}{R_1} + \frac{1}{R_f}\right] = \frac{V_s}{R_1} + \frac{V_o}{R_f}$$

Putting V_o from eqn (1) —

$$\Rightarrow V_p\left(\frac{R_f + R_1}{R_f R_1}\right) = \frac{V_s}{R_1} + \frac{R_p}{R_f} \cdot V_p\left[\frac{1}{R_2} + \frac{1}{R_L} + \frac{1}{R_p}\right]$$

On simplifying —

$$V_p = \frac{-R_2 R_L R_p R_f V_s}{R_1 R_2 R_p^2 + R_L R_p (R_p R_1 - R_2 R_f)} \quad -(4)$$

From circuit —

$$I_o = \frac{V_p}{R_L} = \frac{-R_2 R_p R_f \cdot V_s}{R_1 R_2 R_p^2 + R_L R_p (R_p R_1 - R_2 R_f)}$$

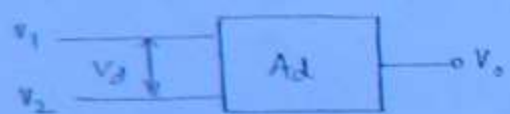
If $R_p R_1 = R_2 R_f$ —

or $\frac{R_f}{R_1} = \frac{R_p}{R_2} \Rightarrow \frac{1}{R_2} = \frac{R_f}{R_1 R_p}$

$$I_o = \frac{-V_s \cdot R_f}{R_1 R_p} = \frac{-V_s}{R_2}$$

Differential Amplifier :-

Ideal

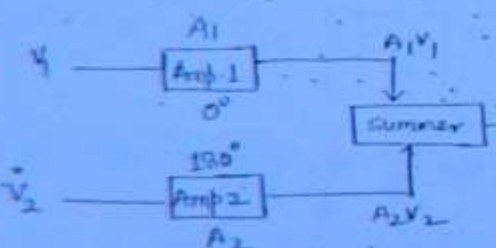


$$V_o = A_d \cdot V_d$$

$V_d = V_1 - V_2$ = difference voltage

A_d = Difference Gain

Practical



$V_o = A_1V_1 + A_2V_2$

$$\underbrace{V_o}_{o/p} = \underbrace{100}_{A_d}\underbrace{(V_1 - V_2)}_{V_d}$$

let $A_1 = 100$, $A_2 = -100$ (180° phase).

→ To write the above eqn, A_1 and A_2 should be equal with 180° phase diff. But it is not possible to have identical amplifiers.

eg: $V_o = 100V_1 - 90V_2 = 90(V_1 - V_2) + 10V_1$ Noise.

→ If there is some noise signal is present at both terminal and ideally it should cancel out but for unidentical amplifiers —

$$V_o = 100(V_1 + V_n) - 90(V_1 + V_n)$$
$$= 90(V_1 - V_2) + 10V_1 + 10V_n \quad \text{Noise.}$$

17

For Practical Amplifier,

$$\boxed{V_o = A_d V_d + \underbrace{A_c V_c}_{\text{error}}} \quad \text{— (1)}$$

where $V_d = V_1 - V_2$ — (2)

$V_c = \frac{V_1 + V_2}{2}$ = common mode signal — (3)

A_c = common mode gain

→ Ideally $A_C \to 0$

Practically $A_C \to$ very small

→ Common Mode Rejection Ratio —

Eg for Diff Amp 1 → $A_c = 10$, $A_d = 1000$ → $\frac{A_d}{A_c} = 100$

" " " 2 → $A_c = 1$, $A_d = 10$ → $\frac{A_d}{A_d} = 10$.

→ Amp 1 is better than Amp 2.

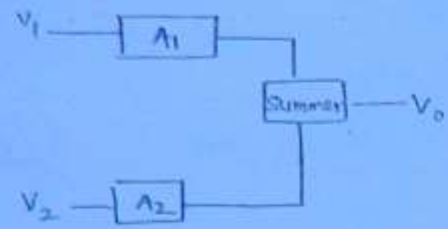
→ $\boxed{CMRR = \rho = \frac{|A_d|}{|A_c|}}$

ideally CMRR $= \infty$
Practically CMRR $= 10^6 = 120\,dB$

→ $\boxed{[CMRR]_{dB} = 20 \log \frac{|A_d|}{|A_c|}}$

→ CMRR is figure of merit of practical op-amp.

from diagram —



$$V_o = A_1V_1 + A_2V_2 \quad — (4)$$

Adding (2) and (3) —

$$2V_c + V_d = 2V_1$$

$$\Rightarrow \quad V_1 = V_c + \frac{V_d}{2} \quad — (5)$$

Substracting (2) from (3) —

$$2V_c - V_d = 2V_2$$

$$\Rightarrow \quad V_2 = V_c - \frac{V_d}{2} \quad — (6)$$

~~Putti~~

Putting 5 & 6 in (4) —

$$V_o = A_1\left(V_c + \frac{V_d}{2}\right) + A_2\left(V_c - \frac{V_d}{2}\right)$$

$$V_o = \left[\frac{A_1 - A_2}{2}\right] V_d + (A_1 + A_2) \cdot V_c \quad —(7)$$

Comparing (1) and (7) —

$$\boxed{A_d = \frac{A_1 - A_2}{2}} \quad \boxed{A_c = A_1 + A_2} \;\; **$$

↳ Here $A_2 = -ve$ due to 180° phase diff and hence $A_d > A_c$.

2nd Method :-

Calculation of A_c —

Put $V_1 = V_2 = V_s \quad \Rightarrow V_c = V_s$

$$\therefore V_d = 0 \quad \Rightarrow \quad V_o = A_dV_d + A_cV_c$$

$$\Rightarrow V_o = 0 + A_c \cdot V_s$$

$$\Rightarrow \boxed{A_c = \frac{V_o}{V_s}}$$

Calculation of A_d :-

Put $V_1 = V_s'/2$ and $V_2 = -V_s'/2$

$$\Rightarrow \quad V_d = V_s' \text{ and } V_c = 0$$

$$\Rightarrow \quad \boxed{A_d = \frac{V_o}{V_s'}}$$

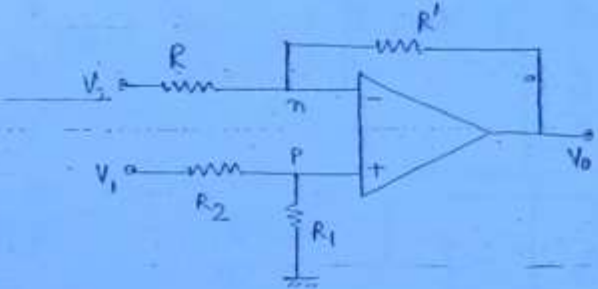
Que:- The circuit shown is a differential amplifier using an ideal op amp

(a) Find the o/p voltage V_o.

(b) Find CMRR.

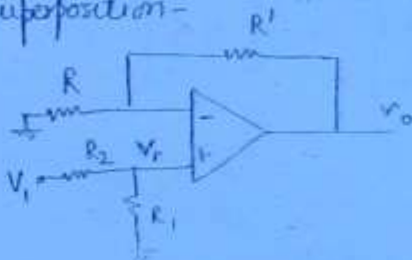
(c) Show that CMRR $= \infty$ if $\frac{R'}{R} = \frac{R_1}{R_2}$.

(19)



Solⁿ:- (a) By applying superposition -

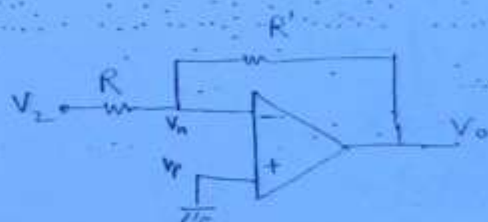
(i) Taking $V_2 = 0$ -



$$V_P = \frac{V_1 R_1}{R_1 + R_2}$$

$$V_{01} = \left[1 + \frac{R'}{R}\right] V_P \Rightarrow V_{01} = \left[1 + \frac{R'}{R}\right]\left[\frac{R_1}{R_1 + R_2}\right] V_1$$

(ii) Taking $V_1 = 0$ -



$$V_{02} = -\frac{R'}{R} V_2$$

$$\therefore V_0 = V_{01} + V_{02} = \left[1 + \frac{R'}{R}\right]\left[\frac{R_1}{R_1 + R_2}\right] V_1 - \frac{R'}{R} V_2 \quad \text{Ans}$$

(b) $V_o = A_d V_d + A_c V_c = A_1 V_1 + A_2 V_2$

$$A_c = A_1 + A_2 \Rightarrow A_c = \left[1 + \frac{R'}{R}\right]\left[\frac{R_1}{R_1 + R_2}\right] - \frac{R'}{R}$$

$$A_d = \frac{A_1 - A_2}{2} \Rightarrow A_d = \frac{1}{2}\left[1 + \frac{R'}{R}\right]\left[\frac{R_1}{R_1 + R_2}\right] + \frac{R'}{2R}$$

$$\text{CMRR} = \frac{1}{2}\;\frac{\left[\left\{1+\frac{R'}{R}\right\}\left\{\frac{R_1}{R_1+R_2}\right\} + \frac{R'}{R}\right]}{\left[\left\{1+\frac{R'}{R}\right\}\left\{\frac{R_1}{R_1+R_2}\right\} - \frac{R'}{R}\right]}$$

(c) when $\frac{R'}{R} = \frac{R_1}{R_2}$ —

$$\text{CMRR} = \frac{1}{2}\;\frac{\left[\left\{1+\frac{R_1}{R_2}\right\}\left\{\frac{R_1}{R_1+R_2}\right\} + \frac{R_1}{R_2}\right]}{\left[\left\{1+\frac{R_1}{R_2}\right\}\left\{\frac{R_1}{R_1+R_2}\right\} - \frac{R_1}{R_2}\right]}$$

$$\Rightarrow \text{CMRR} = \tfrac{1}{2}\left[\left\{2\frac{R_1}{R_2}\right\} \div \left\{0\right\}\right]$$

$$\Rightarrow \text{CMRR} = \infty$$

$$\Rightarrow \text{CMRR} = \infty \Rightarrow |A_c| = 0 \text{ or } |A_1| = |A_2|$$

$$\Rightarrow \left[1+\frac{R'}{R}\right]\left[\frac{R_1}{R_1+R_2}\right] - \frac{R'}{R} = 0$$

$$\Rightarrow \frac{R_1}{R_1+R_2} + \frac{R'}{R}\left[\frac{R_1}{R_1+R_2} - 1\right] = 0$$

$$\Rightarrow \frac{R_1}{R_1+R_2} - \frac{R_2 \cdot R'}{R(R_1+R_2)} = 0$$

$$\Rightarrow \frac{R_1}{R_2} = \frac{R'}{R} \qquad \text{Hence Proved}$$

3rd method :

Put $V_1 = V_2 = V_c \Rightarrow V_d = 0,\ V_c = V_s$

$$A_c = V_o/V_c \quad \text{—(1)}$$

$$V_o = \left[1+\frac{R'}{R}\right]\left[\frac{R_1}{R_1+R_2}\right]V_s - \frac{R'}{R}V_s \Rightarrow A_c = \frac{V_o}{V_s} = \left[1+\frac{R'}{R}\right]\left[\frac{R_1}{R_1+R_2}\right] - \frac{R'}{R}$$

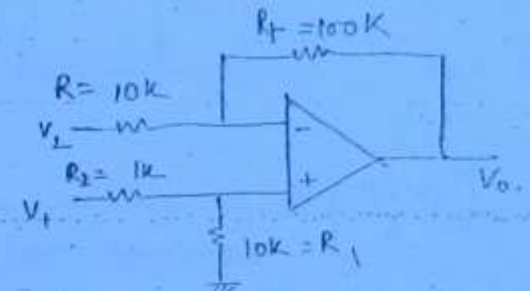
For A_d, $V_1 = \frac{V_s'}{2}$, $V_2 = -V_s'/2$ $\Rightarrow$ $A_d = \frac{V_0}{V_s'}$ and $A_c = 0$.

$$\therefore V_0 = \left[1 + \frac{R'}{R}\right]\left[\frac{R_1}{R_1+R_2}\right] \cdot \frac{V_s'}{2} + \frac{R'}{R}\frac{V_s'}{2}$$

2

$$A_d = \frac{V_0}{V_s'} = \frac{1}{2}\left[\left[1 + \frac{R'}{R}\right]\left[\frac{R_1}{R_1+R_2}\right] + \frac{R'}{R}\right].$$

Ques:



① CMRR
② A_c
③ A_d
④ if $V_1 = V_2 = V$, then $V_0 = ?$

Sol^n:- $\rightarrow$ for objective, first check $\frac{R_f}{R} = \frac{R_1}{R_2}$

$\Rightarrow \frac{100}{10} = \frac{10}{1}$ $\Rightarrow$ Since ratio is equal $\Rightarrow$ CMRR $= \infty$

$\Rightarrow A_c = 0$

④ $\rightarrow$ $V_0 = A_d V_d + A_c V_c$

$\Rightarrow V_0 = A_d \cdot (V_1 - V_2)$

$\Rightarrow V_0 = 0$

③ A_d :?

$\therefore A_c = 0 \Rightarrow |A_1| = |A_2|$

$V_0 = A_1 V_1 + A_2 V_2$

$\Rightarrow V_0 = A_1 [V_1 - V_2]$

from previous ques. $\leftarrow$ $\boxed{A_2 = -\frac{R_f}{R}} = -10 \Rightarrow A_1 = 10$

$$\therefore A_d = \frac{A_1 - A_2}{2} = \frac{10-(-10)}{2} = 10$$

[illegible] August, [illegible]

Voltage follower :- (Objective)

22

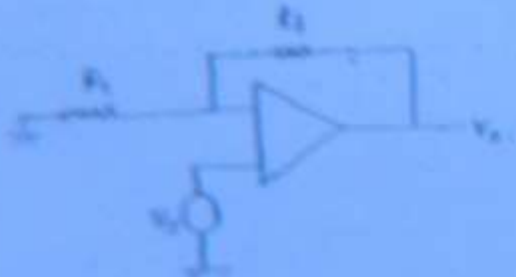
$V_f = V_n = V_i$

$\boxed{V_o = V_n = V_i}$

→ Output follows the i/p hence called voltage follower.

→ $\boxed{A_{CL} = \frac{V_o}{V_i} = 1}$ $\boxed{\phi = 0}$

→



$V_o = \left[1 + \frac{R_f}{R_1}\right] V_i$

when $R_f << R_1$,

$\boxed{V_o = V_i}$ - Acts as voltage follower

→ Voltage follower is voltage series feedback.

→ For voltage series feedback, $R_i \uparrow$ and $R_o \downarrow$.

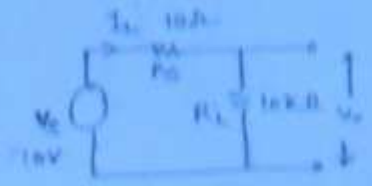
→ For voltage follower, $\boxed{R_i = 10^{11}\,\Omega}$ and $\boxed{R_o = 0.01\,\Omega \approx 0}$

→ Because of -ve feedback, $|A_{CL}| = 1$ ⇒ $\boxed{B.W. = 10^6\,Hz = 1\,MHz}$

Application -

- It is used in designing of sample and hold circuit.
- " " " " " " first order butterworth filter
- " " " as a buffer, i.e., impedance matching device b/w high
- resistance and low resistance.

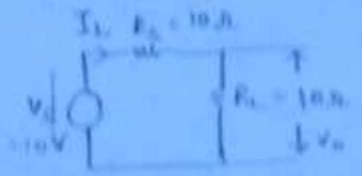
→ Application as a buffer -



$V_o = \frac{R_L}{R_S + R_L} V_s \approx V_s$ ∵ $R_L >> R_S$

$I_L = \frac{V_s}{R_S + R_L} \approx \frac{10}{10K} = 1mA$ ∴ $R_L \uparrow$ and $I_L \downarrow$

There is low loading effect.

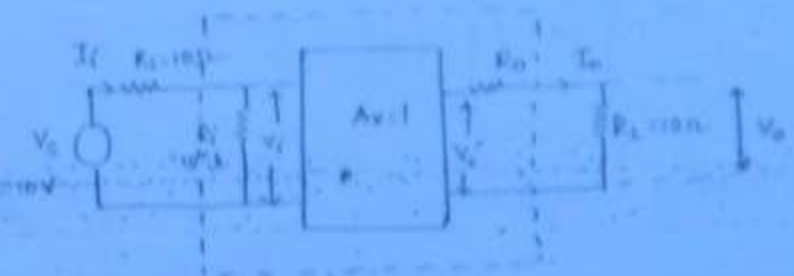


$V_o = \frac{10}{10+10} V_s = 5V$ ∴ $R_L \downarrow$, $I_L \uparrow$

$I_o = 500mA$.

There is high loading effect.

Low Load Resistance :- → R_L = very low I_L = very high } ⇒ loading effect high.	**Low Load :-** → Loading loading effect → I_L = low → R_L = high



Buffer.

∵ $R_i >> R_S$ ⇒ $V_i \approx V_s$

∵ $A_V = 1$; $V_o' = V_i = V_s$ and ∵ $R_o \approx 0$ ⇒ $V_o = V_o' = V_s$.

$I_i = \frac{10}{10 + 10^{10}} = nA$ → very small.

$I_o = \frac{10}{10} = 1A$ → This extra current is given by buffer.

Other Buffers -

→ Voltage follower by using op-amp — VCVS

→ Emitter " " " BJT } Common collector config { — CCVS

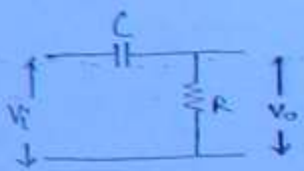
→ Source follower using FET (Common drain config) — VCVS.

Linear Wave Shaping circuit :-

- High Pass RC → Differentiator.
- low Pass RC → Integrator

- The process where by form of a non-sinusoidal signal is altered by transmission through a linear n/w is called linear wave shaping

1) High Pass RC circuit -



Gain $A = \frac{V_o}{V_i}$

$$V_o = \frac{R}{R + 1/Cs} \cdot V_i$$

$$\Rightarrow \frac{V_o}{V_i} = \frac{1}{1 + \frac{1}{RCs}} \Rightarrow \boxed{A = \frac{1}{1 - \frac{j}{\omega RC}}} \quad -(1)$$

$$\rightarrow \boxed{|A| = \frac{1}{\sqrt{1 + 1/\omega^2 R^2 C^2}}} \; -(2) \quad , \quad \boxed{\phi \text{ shift} = \tan^{-1}\left(\frac{1}{\omega RC}\right)} \; -(3)$$

→ Since ϕ shift = +ve, it is called leading circuit.

→ from eq^n (2) — as $\omega \uparrow$, gain ↑

→ At $\omega = 0$, $|A| = 0$

→ At $\omega = \infty$, $|A| = 1 = A_{max}$

→ At $\omega = \omega_L$, $|A| = \frac{A_{max}}{\sqrt{2}}$; ω_L = cutoff frequency, freq. at which gain reduces to $\frac{1}{\sqrt{2}}$ of max. value (3dB).

$$\Rightarrow \frac{1}{\sqrt{2}} = \frac{1}{\sqrt{1 + 1/\omega_L^2 R^2 C^2}}$$

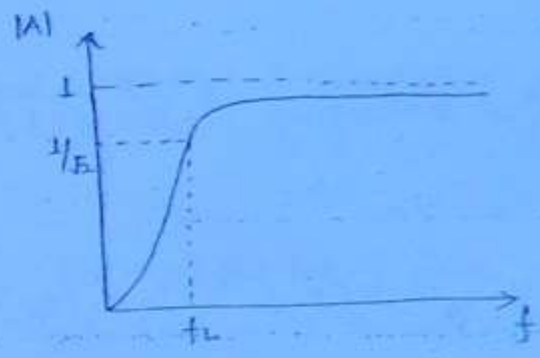
$$\Rightarrow \boxed{\omega_L = 2\pi f_L = 1/RC} \quad -(4)$$

— ω_L = 3dB frequency

from (1) and (4) –

$$A = \frac{1}{1 - j/\omega_o RC} \Rightarrow \boxed{A = \frac{1}{1 - j\,\omega_L/\omega} = \frac{1}{1 - j\,f_L/f}}$$

$$|A| = \frac{1}{\sqrt{1 + (f_L/f)^2}}$$ where f = instantaneous frequency



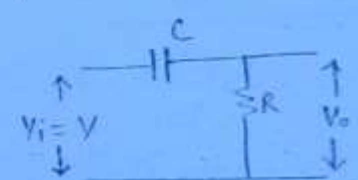
$\Rightarrow$ $f = 0$; $|A| = 0$

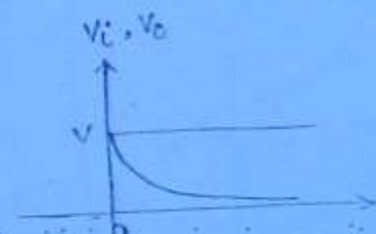
$f = f_L$; $|A| = 1/\sqrt{2}$

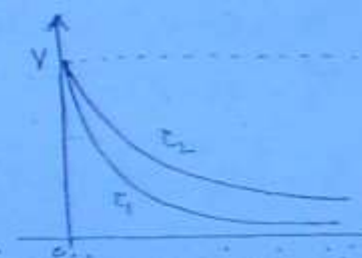
$f = \infty$; $|A| = 1$

$\Rightarrow$ $\boxed{B.W. = \infty}$

Step Response :-





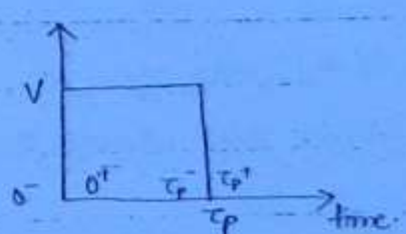


$(\tau_1 < \tau_2)$.

$\Rightarrow$ $V_0 = V_R = V e^{-t/RC}$ – $\downarrow$ exponentially

$\Rightarrow$ $V_C = V\left[1 - e^{-t/RC}\right]$ $\uparrow$ exponentially

Pulse Response



Case 1 $\frac{\tau_P}{RC} \ll 1$

τ_p = Pulse width.

Case 2 $\frac{\tau_P}{RC} \gg 1$

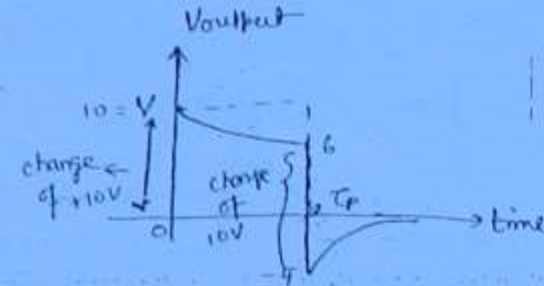
$\rightarrow v_i(0^-) = 0 \quad , \quad v_i(0^+) = V$

$V_i(\tau_p) = V , \quad V_i(\tau_p^+) = 0$

$\rightarrow V_c(0^-) = 0 = V_c(0^+) . \quad \Rightarrow V_R(0^+) = V$

$V_c = V[1 - e^{-t/RC}] \; ; \; V_R = V e^{-t/RC}$

<u>Case 1</u> $RC >> \tau_p$



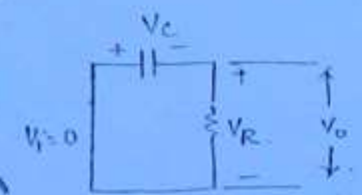
$\rightarrow V_R$ will start discharging till $0 < t < \tau_p$

At $t = \tau_p^-$, $-V_o = V e^{-\tau_p/RC} = V'$

$V_c = V - V' = V(1 - e^{-\tau_p/RC}) = V_c(\tau_p^-)$

At $t = \tau_p^+$ –

$V_c(\tau_p^+) = V_c(\tau_p^-) = V(1 - e^{-\tau_p/RC}) = (V - V')$



$V_i = 0$ at $\tau_p(0^+)$

~~$V_R = 0 - V_c = V(1 - e^{-\tau_p/RC})$~~

$V_c = (V - V') e^{-t/RC}$

$V_o = -V_c = -(V - V') e^{-t'/RC} \quad (t' = t - \tau_p)$

Time	V_o
$t < 0$	0
$t = 0^+$	V
$0 < t < \tau_p$	$V_o = V e^{-t/RC}$
$t = \tau_p^-$	$V' = V e^{-\tau_p/RC}$
$t = \tau_p^+$	$-[V - V']$
$t > \tau_p$	$-[V - V'] e^{-t'/RC}$, $t' = t - \tau_p$

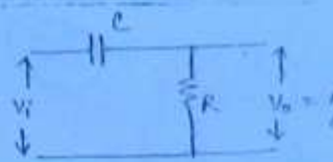
$\Rightarrow$ When there is sudden change in i/p, the same change will occur at the o/p.

$\rightarrow$ If the ~~output~~ input is maintaining some constant level, then output will tend towards zero. (between 0 to τ_p) and from (τ_p to ∞), the o/p is tending towards 0.

$\rightarrow$ Area of the pulse $= V\tau_p$ = +ve = average DC level.

For output, A_+ area $= \int_0^{\tau_p} V e^{-t/RC} dt$, $A_- = \int_{\tau_p}^{\infty} -(V - V') e^{-(t-\tau_p)/RC} dt$

$A_+ = A_-$ = (as charging = discharging)

$\rightarrow$ 

$|Z_C| = \frac{1}{2\pi f C}$ $\rightarrow$ Value of C should be high so that it acts as SC for AC.

V_o = AC only for DC $|Z_C| = \infty \Rightarrow$ DC will be blocked.

(27)

V_i = AC + DC

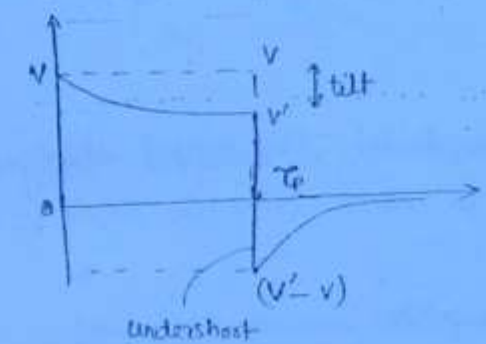
$\Rightarrow$ dc level or avg level of o/p = 0

$\rightarrow$ Total o/p area = 0

$\Rightarrow$ $A_+ = A_-$.

{ Area gives avg value of signal

$\rightarrow$ Avg. level of o/p in high pass RC signal is always 0 irrespective of the avg. level of i/p.

$\rightarrow$ 

Tilt $\rightarrow$ at the top of pulse

Undershoot $\rightarrow$ at the end of pulse

<u>Case 2</u> : $RC << \tau_p$.

$V_C(0^-) = 0 = V_C(0^+) \Rightarrow V_o = V$

$V_R = Ve^{-t/RC}$ for $0 < t < t_1'$

At $t = t_1$ —

$V_C = V \Rightarrow V_R = 0$

At $t = \tau_p^-$,

$V_C = V$

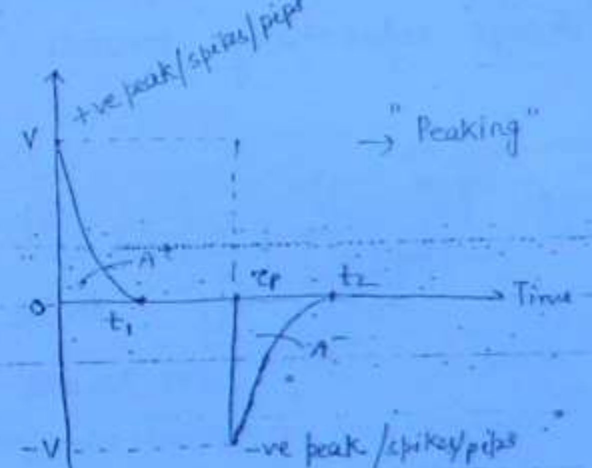
At $t = \tau_p^+$, $V_C = V$, ~~[illegible]~~

$V_i = 0 \Rightarrow V_R = -V$

Now, capacitor will start discharging, $V_C = Ve^{-t/RC}$ $(t - \tau_p)$, hence

$V_R = V_o = -Ve^{-t'/RC} \rightarrow (t' = t - \tau_p)$

At $t = t_2$, $V_C = 0$ and $\Rightarrow V_R = V_o = 0$.



$\boxed{A^+ = A^-}$

Conclusion:-

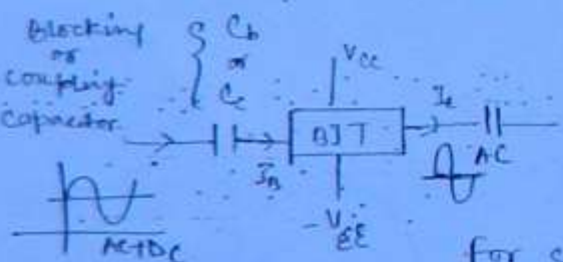
- Positive spike of amplitude 'V' at the begining of pulse and -ve of same size at the ending of pulse. This process of converting pulse into spike by means of a high pass RC circuit of short time constant is called Peaking.

For HPF -

- Average level o/p is always zero, independent of average level of i/p.
  i.e., $\boxed{A+ = A-}$

- When input changes discontinuously by amount 'V', The output changes discontinuously by an equal amount and in same direction.

- During any finite time interval, when input maintains a constant level, o/p decays exponentially towards '0' voltage.

* 

$|Z_c| = \frac{1}{2\pi f C_c}$

For DC, $|Z_c| = \infty \Rightarrow$ block DC.

For smooth passage of AC, $Z_c =$ SC

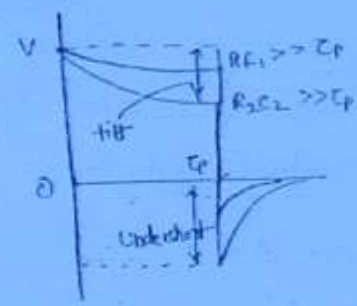
$\Rightarrow C =$ very high.

But if AC $\rightarrow$ 20Hz – 20KHz.

The low freq. components will not pass smoothly as for low frequencies $|Z|$ = high. Hence there will be distortion in the o/p. Whereas, the high freq. component will be received accurately at the o/p.

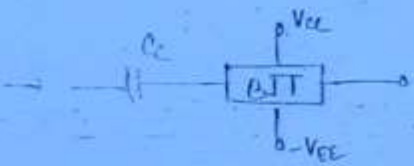
$\rightarrow$ This capacitor provides DC isolation to the BJT. The DC is blocked as it will interfere with the biasing condition of the BJT.

→ For $RC >>> \tau_p$, pulse distortion will ↓ as tilt and undershoot is ↓.

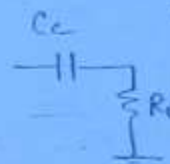


$R_1C_1 > R_2C_2$. If we keep ↑ RC, distortion will keep ↓. Tilt and undershoot are distortions.

⇒ C should be high for minimum distortion. (same as previous discussion).



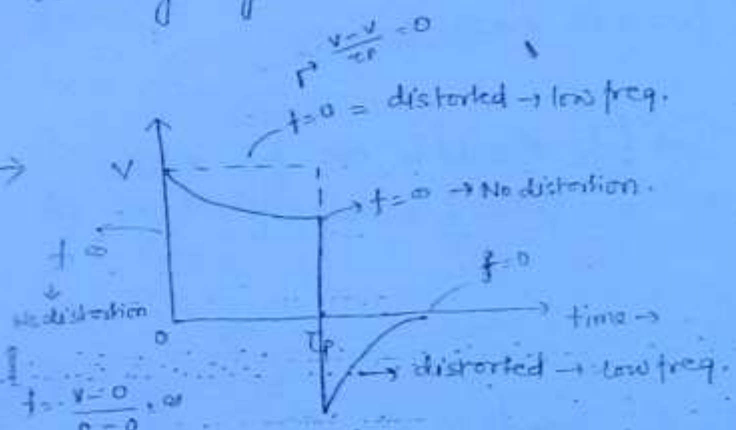
≡

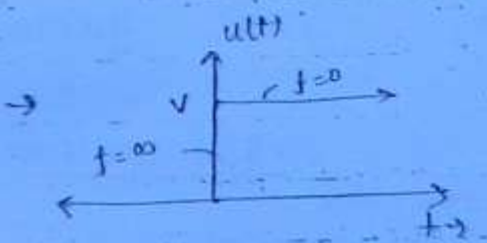


⇒ R_i should also be high.

≡ Similar to HPF.

→ For better coupling or minimum distortion, R_i and C_c, both should be very high.





→ It has both max. as well as min. freq. signals and hence it is preferred as test signal.

Tilt or Sage :-

→ $RC >>> \tau_p$.

→ $V_0 = Ve^{-t/RC}$

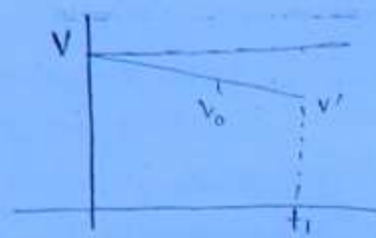
$x = t/RC$ = very small.

$e^{-x} = 1 - x + \frac{x^2}{2!} - \frac{x^3}{3!} - - -$

⇒ $e^{-x} = 1 - x$

(30)

$$\Rightarrow \quad V_0 = V\left[1 - \frac{t}{RC}\right] \quad -(1)$$



Tilt at $t = t_1 = V - V'$ — (2)

$$\% \text{ tilt} = P\% = \frac{V - V'}{V} \times 100 \quad -(3)$$

$$V' = V\left[1 - \frac{t_1}{RC}\right] \Rightarrow V - V' = \frac{V t_1}{RC}$$

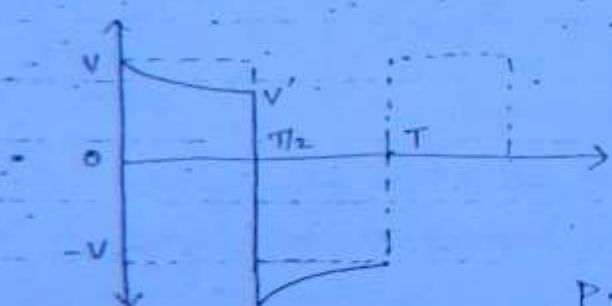
$$\Rightarrow \frac{V - V'}{V} = \frac{t_1}{RC}$$

$$\Rightarrow \boxed{P\% = \frac{t_1}{RC} \times 100\%}^{**}$$ → (when RC is ↑, tilt will ↓.)

Since, $2\pi f_L = \omega_L = 1/RC$ — { f_L = 3dB cutoff frequency }.

$$\boxed{P\% = 2\pi f_L t_1 \times 100\%}^{**}$$ → (f_L should be low for smaller tilt.)

— Tilt for symmetrical Square Wave —



$f = \frac{1}{T}$ = freq. of sq. wave

$t_1 = T/2 = \frac{1}{2f}$

$$P\% = 2\pi f_L \left(\frac{1}{2f}\right) \times 100\%$$

$$\Rightarrow \boxed{P\% = \pi\left(\frac{f_L}{f}\right) \times 100\%}^{**}$$

↳ (for high frequency signal, $\%P$ = low.) and vice versa.

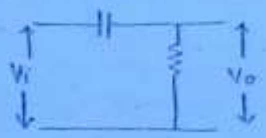
16th August, 2012

High pass RC circuit as a differentiator :-

- When time constant, RC, is very very small as compared to time period of input signal, the circuit is called differentiator.

Criteria for good differentiator –

- Ideally, $RC = 0$.



$$\frac{V_o}{V_i} = |A| = \frac{1}{1 - j/\omega RC}$$

$$|A| = \frac{1}{\sqrt{1 + 1/\omega^2R^2C^2}} \quad ; \quad \phi = \tan^{-1}\left(\frac{1}{\omega RC}\right)$$

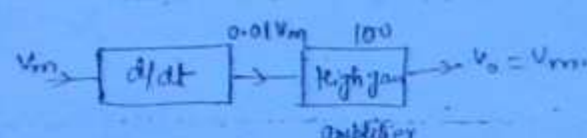
for $V_i = V_m \sin \omega t$

$$V_o = |A| \cdot V_m \sin(\omega t + \phi).$$

$$= \frac{V_m}{\sqrt{1 + \frac{1}{\omega^2R^2C^2}}} \cdot \sin(\omega t + \phi).$$

for ideal differentiator, $\phi = 90^\circ \Rightarrow \omega RC = 0$. (which is practically not possible)

	ϕ	ωRC
Ideal Diff.	90°	0
Best Diff.	89.4°	0.01
Good diff	84.3°	0.1



for Best diff. –

$\omega RC = 0.01$

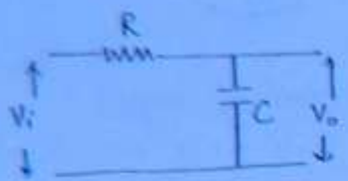
$$\Rightarrow |A| = \frac{1}{\sqrt{1 + 1/\omega^2R^2C^2}} \quad \text{but } 1/\omega^2R^2C^2 \ggg 1$$

$\Rightarrow V_o = (0.01)V_m \sin(\omega t + 89.4^\circ) \rightarrow$ Amplitude is very small affect differentiation.

→ To get amplitude, V_m, we have to follow it with a high gain amplifier

→ A high pass RC differentiator is always followed by a high gain amplifier

Low Pass RC circuit :-



$V_o = \frac{1/cs}{R + 1/cs} \cdot V_i \Rightarrow A = \frac{1}{1 + RCs}$

$\Rightarrow \boxed{A = \frac{1}{1 + j\omega RC}}$

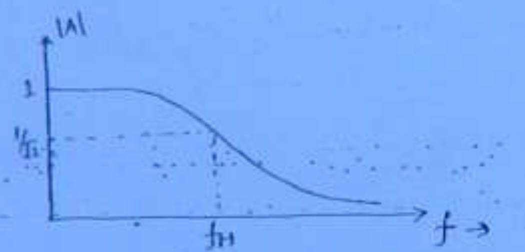
$\rightarrow \quad |A| = \frac{1}{\sqrt{1 + \omega^2 R^2 C^2}}$; $\phi = -\tan^{-1}(\omega RC) \rightarrow$ (lagging circuit)
$\phi = -ve$

$\rightarrow$ for $\omega = 0$; $|A| = 1$
$\omega = \infty$; $|A| = 0$
$\omega \uparrow$; $|A| \downarrow \Rightarrow$ Low pass filter

$\rightarrow$ At $\omega = \omega_H$; $|A| = \frac{|A_{max}|}{\sqrt{2}} = 1/\sqrt{2}$

$\Rightarrow \boxed{\omega_H = \frac{1}{RC}}$ or $2\pi f_H = 1/RC \Rightarrow \boxed{f_H = \frac{1}{2\pi RC}} \rightarrow$ 3dB cutoff frequency

$\rightarrow \boxed{A = \frac{1}{1 + j(f/f_H)}}$



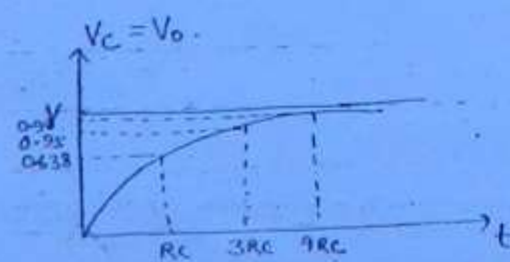
Step Response :-

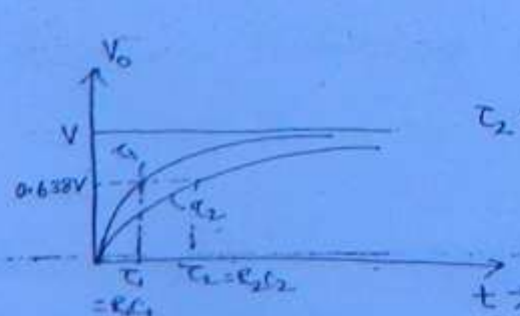
$V_c(0^-) = V_c(0^+) = 0$

At $t = 0^+$, $V_c(0^+) = 0$

At $t = \infty$, $V_c = V$

$V_c = V\left[1 - e^{-t/RC}\right]$.

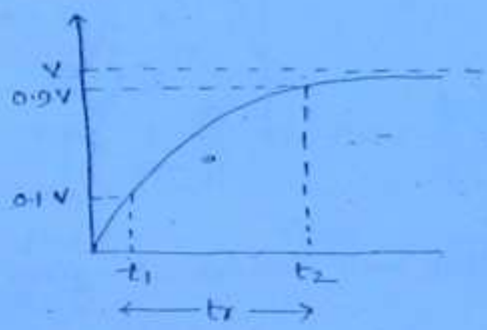




$\tau_2 > \tau_1$ (or) $R_2C_2 > R_1C_1$

Rise Time :- (t_r)

- It is the time taken by the signal to rise from 10% to 90% of its final value.



At $t = t_1$, $V_o = 0.1V \Rightarrow 0.1V = V[1 - e^{-t/RC}]$

$\Rightarrow \boxed{t_1 \cong 0.1RC}$

At $t = t_2$, $V_o = 0.9V \Rightarrow 0.9V = V(1 - e^{-t/RC})$

$\Rightarrow \boxed{t_2 \cong 2.3RC}$

$$\boxed{\text{Rise time} = t_2 - t_1 = 2.2RC}$$

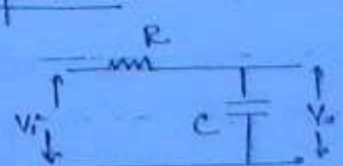
$\rightarrow \because \omega_H = 2\pi f_H = \frac{1}{RC}$

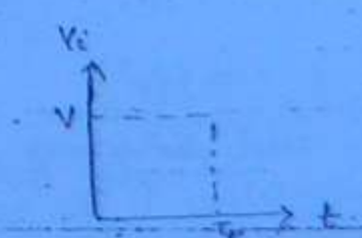
$\therefore t_r = \frac{2.2}{2\pi f_H} \Rightarrow \boxed{t_r = \frac{0.35}{f_H}}$

→ Rise time of the circuit should be low for fast response.

→ f_H should be high

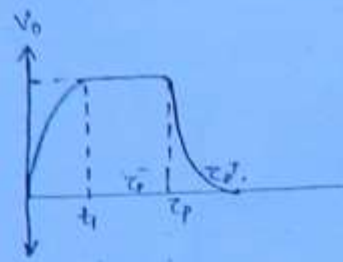
Pulse Response :-





$V_c(0^-) = V_c(0^+) = 0V.$

$\therefore V_0(0^+) = 0$



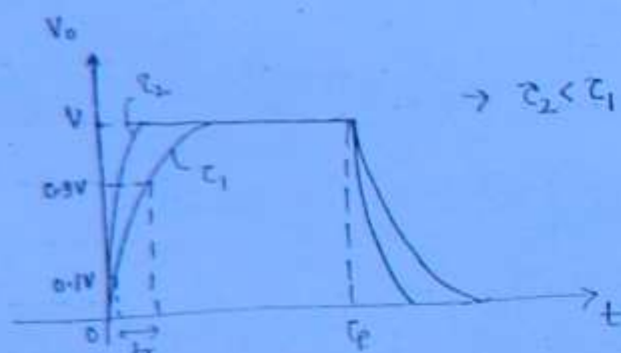
Case I :- $\frac{\tau_p}{RC} >> 1$ (or) $RC << \tau_p$

When RC = small, rate of charging is very fast.

$V_c = V$ and will remain V till $t = \tau_p^-$

$V_c(\tau_p^-) = V_c(\tau_p^+) = V$. and now the capacitor will start discharging through R.

$$V_0 = V_c = Ve^{-(t-\tau_p)/RC} \quad \text{for } t > \tau_p$$

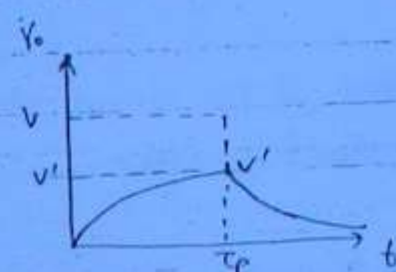


$\rightarrow \tau_2 < \tau_1$, when $RC = 0$ (ideally (practically-very small)), the capacitor will charge instantly and hence pulse shape will be preserved if

$$\boxed{f_H \geq \frac{1}{\tau_p}} \; **$$

$\rightarrow f_H \geq 1/\tau_p \Rightarrow \frac{0.35}{t_r} \geq 1/\tau_p$

$$\Rightarrow \boxed{t_r \leq 0.35\tau_p} \; **$$



Case II : $\frac{\tau_p}{RC} << 1$ or $RC >> \tau_p$

RC is high, hence rate of charging is very slow.

At $t = \tau_p^-$,

$$V' = V\left[1 - e^{-\tau_p/RC}\right] = V_c(\tau_p^+)$$

After $t = \tau_p$, V_c will start discharging,

$$V_0 = V' \cdot e^{-(t-\tau_p)/RC} \quad \text{for } t > \tau_p$$

When RC is very high, then

(35)

$$x = \frac{t}{RC} <<< 1$$

$$\therefore e^{-x} = 1 - x + \frac{x^2}{2!} - \frac{x^3}{3!} \dots \Rightarrow e^{-x} = [1 - x]$$

$$\therefore V_c = V\left[1 - \left\{1 - \frac{t}{RC}\right\}\right] \Rightarrow V_c = \frac{V \cdot t}{RC}$$ - (linear equation).

for discharging.

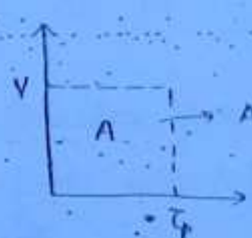
$$V_0 = V' e^{-(t-\tau_p)/RC} = V' e^{-t'/RC}, \quad \text{for } RC >>> t'$$

$$V_0 = V'\left[1 - \frac{t'}{RC}\right]$$ — (linear eqn).

* RC low pass circuit will act as an integrator when RC is very high.

* 

$$\boxed{\tau_3 > \tau_2 > \tau_1} \qquad \boxed{A = A_1 = A_2 = A_3}$$

* 

$A = V \cdot \tau_p = +ve \Rightarrow$ dc level or avg. level

* for low pass RC circuit, dc level of output is always equal to dc level of input dc level.

Low Pass RC as an integrator

> When the time constant is very large as compared to time period of i/p signal, the circuit is called integrator.

for $V_i = V_m \sin \omega t$ —

$$V_o = |A| \cdot V_m \sin(\omega t + \phi)$$

$$V_o = \frac{V_m}{\sqrt{1+\omega^2R^2C^2}} \cdot \sin(\omega t + \phi)$$

	ϕ	ωRC
Ideal $\int$	$-90°$	∞ (practically not possible)
Best $\int$	$-89.4°$	$RC > 15.1T$

for Best $\int$ —

$$-\tan^{-1}(\omega RC) = -89.4°$$

$$\Rightarrow \omega RC = \tan(89.4)$$

$$\Rightarrow RC \times \frac{2\pi}{T} = \tan(89.4)$$

$$\Rightarrow RC = 15.1T$$

$\rightarrow \boxed{\int} \rightarrow \boxed{\text{High gain ampli}} \rightarrow$ o

$$V_o = \frac{V_m}{\omega RC} \sin(\omega t - 89.4°) \quad \text{for } \omega RC >> 1$$

In this case also, amplitude is very low.

→ The o/p is followed by a high gain amplifier.

* $V_i \rightarrow \boxed{\int} \rightarrow V_o$ $\qquad$ $V_i \rightarrow \boxed{d/dt} \rightarrow V_o$

Laplace $\int \rightarrow \frac{1}{s} = \frac{1}{j2\pi f}$ $\qquad$ Laplace $d/dt = s = j2\pi f$

$\Rightarrow f\uparrow$ then $|A|\downarrow$ $\qquad$ $\Rightarrow f\uparrow$ then $|A|\uparrow$

- Integrator is prefered over differentiator because —

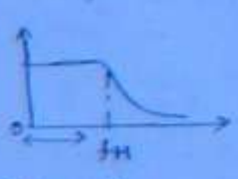
1) For spurious signals/Noise signals —

They are of high frequency.

$\bigwedge$ $V_i \rightarrow \boxed{\int} \rightarrow V_o$ = suppress the noise due to high freq.

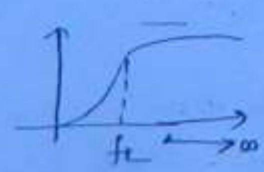
$V_i \rightarrow \boxed{d/dt} \rightarrow V_o$ Enhance the noise.

2) for LPF,



BW = f_H

For HPF,



BW = ∞.

→ Due to ∞ BW, some unwanted signals will also come above the req. signal band.

$\boxed{\text{Noise} \propto \text{BW}}$

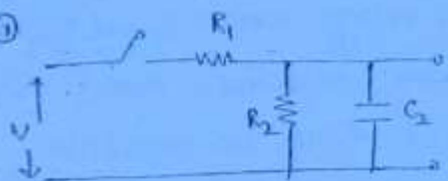
→ LPF is placed at the last stage of multi stage amplifier so as to prevent the noise to reach the output.

→ Integrator is almost preferable over differentiator for following reasons–

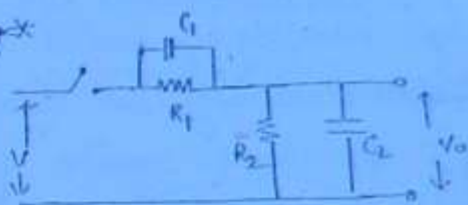
1. Since gain of $\int$ ↓ with f, whereas gain of d/dt ↑ with f therefore, it is easier to stablize $\int$ than d/dt w.r.t spurious oscillations (high freq. noise)

2. As a result of its limited BW, an $\int$ is less sensitive to d/dt noise voltage than a d/dt

Ques :- ①



② **



Switch is closed at $t=0$. $V_0(0^+) = ?$

Sol^n: ① At $V_c(0^-)=0=V_c(0^+)$ ⇒ $V_0 = 0$ at $t=0^+$ $\left\{ I(0^+) = V/R_1 = \text{finite} \right\}$

$V_0(\infty) = VR_2/R_1+R_2$

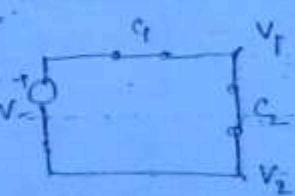
② Capacitor does not allow sudden change in voltage but only for finite value of current

Wrong result

$V_{c_1}(0^-) = 0 = V_{c_1}(0^+)$.

$V_{c_2}(0^-) = 0 = V_{c_2}(0^+)$

⇒



⇒ All paths are short

⇒ $V_0 = 0$ from o/p. $= V_1 - V_2$

and $V_1 - V_2 = V$ from i/p.

Hence KVL is violated.

∴ $V_{c_2} = V_0 = 0$ is a wrong result

Correct result.

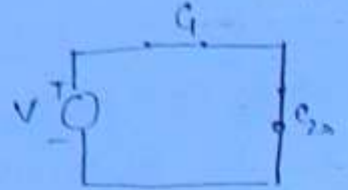
~~Due to $V_{c_2} = 0$, the current in the circuit will be~~

for $V_{c_1} = 0$ & $V_{c_2} = 0$, $V/0 = I(0^+) = \infty$. for $I(0^+) = \infty$, there will be a finite ~~voltage~~ charge in capacitors,

$$\int_{0^-}^{0^+} I(t)\,dt = q(0^+) = \text{finite}.$$

$\left\{ \right.$ I(t) will behave as impulsive current & hence C will allow sudden change of voltg

$$q(0^+) = C_{eq} \cdot V = \frac{C_1 C_2}{C_1 + C_2} V.$$



$$\therefore V_o(0^+) = V_{C_2}(0^+) = \frac{q(0^+)}{C_2}$$

$$V_o(0^+) = \frac{C_1}{C_1 + C_2} \cdot V \quad ; \quad V_{C_1}(0^+) = \frac{q(0^+)}{C_1} = \frac{C_2 V}{C_1 + C_2}$$

→ voltages will be distributed b/w C_1 and C_2.

At $t = \infty$, C_1 & C_2 will be o.c,

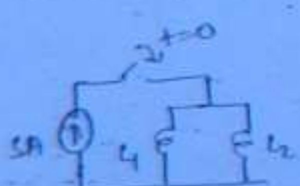
$$V_o = \frac{R_2}{R_1 + R_2} V.$$

Conclusion :-

→ As input changes abruptly by amount V at $t=0$, then voltage across C_1 and C_2 must also change discontinuously but voltage across capacitor cannot change instantaneously if current remains finite and hence an impulsive current must flow in the circuit

→ An infinite current exists for $t = 0^+$, so that a finite charge $q(0^+)$ is delivered to each capacitor and capacitor allows sudden change of voltage

Que.



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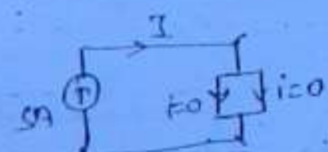


KCL violated.

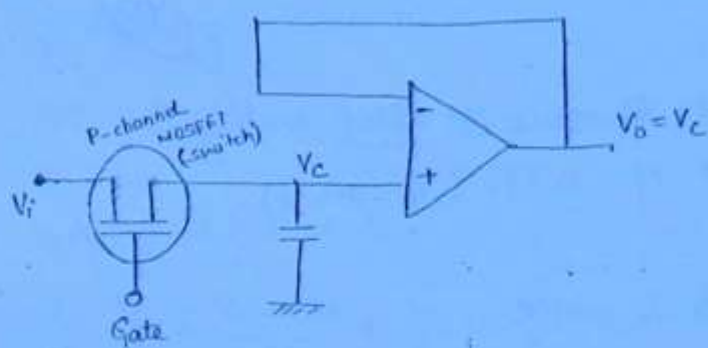
$$Z_L = \infty \quad (\because i = 0)$$

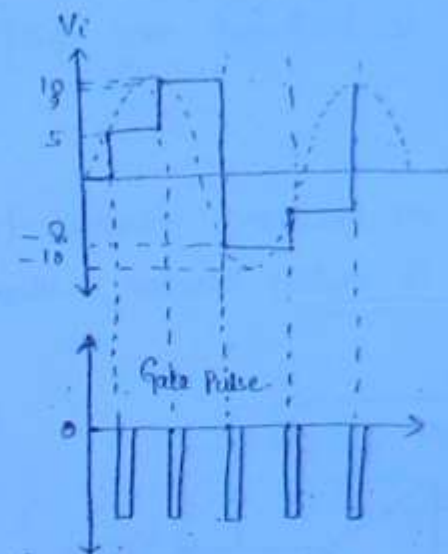
$$\Rightarrow V = 5 \times \infty = \infty = \text{impulsive voltage}$$

Hence it will allow sudden change in current.

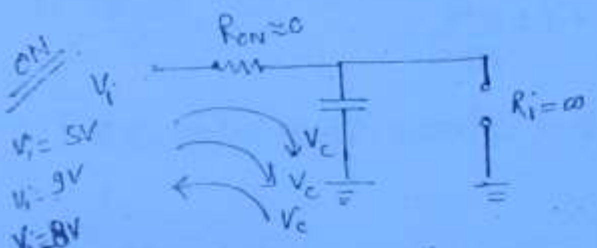
$$I_{L_2} = \frac{5L_1}{L_1 + L_2}, \quad I_{L_1} = \frac{5L_2}{L_1 + L_2}$$

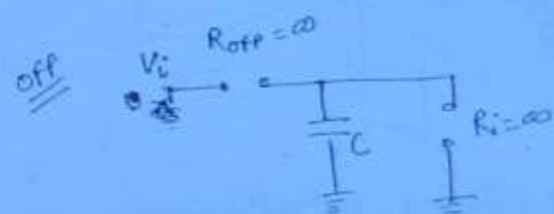
Sample and Hold Circuit :-





Switch	R_{switch}	Time constant	Remark
ON	$R_{on} \approx 0$	$R_{on}C \approx 0$	Capacitor will suddenly charge upto instantaneous value of V_i
OFF	$R_{off} \approx \infty$	$R_{off}C \approx \infty$	C will hold the value of V_i.





* When V_i is < the value hold by capacitor in that case C will discharge or C will charge towards value of V_i which is smaller than its previous value.

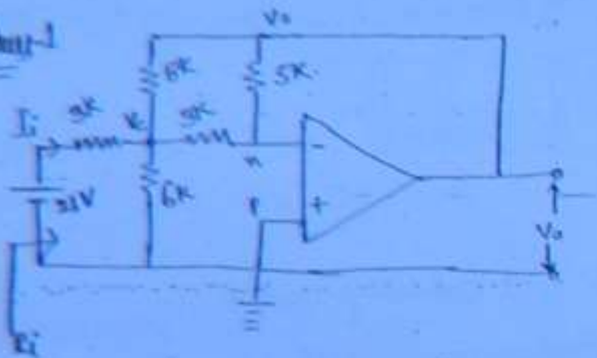
* -ve triggered P-MOSFET is used as trigger because -vely triggered pulses will not generate spikes./noise.

- The op-amp is used (voltage follower), because it will make the $R_i = \infty$ which will help capacitor to hold the value, and C will not discharge through it. (If R_i = some finite value, the hold value will discharge through it).

- Also, MOSFET is preferred over BJT as a switch because of its zero offset voltage.

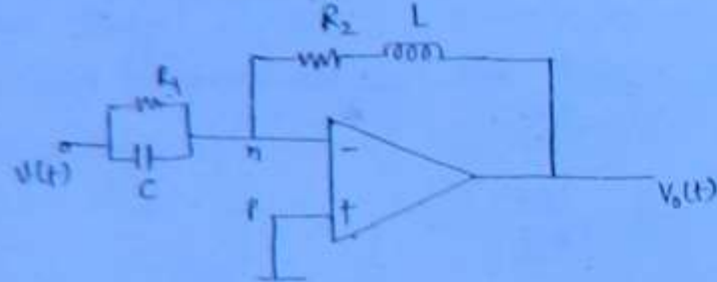
- MOSFET makes an excellent chopper (switch) because its offset voltage ($V_\gamma \approx 5\mu V$) is much smaller than that of BJT. ($V_\gamma = 0.5V$).

Ques-1



find V_c, I_i and R_i

Ques-2 :



$$-v_o = \frac{R_2}{R_1} v + \left[R_2 C + \frac{L}{R_1}\right]\frac{dv}{dt} + LC\frac{d^2v}{dt^2}.$$

Sol^n(2) :- By applying virtual ground, $V_p = V_n = 0$.

Now applying KCL at V_n -

$$\frac{V_n - V}{Z_{R_1C}} + \frac{V_n - V_o}{Z_{R_2L}} = 0$$

$$\Rightarrow \frac{V}{Z_{R_1C}} + \frac{V_o}{Z_{R_2L}} = 0$$

$$\Rightarrow \frac{V}{\left(\frac{R_1 \cdot 1/Cs}{R_1 + 1/Cs}\right)} + \frac{V_o}{R_2 + Ls} = 0$$

$$\Rightarrow \frac{V(1 + R_1Cs)}{R_1} + \frac{V_o}{R_2 + Ls} = 0$$

$$\Rightarrow V(1 + R_1Cs)(R_2 + Ls) + V_oR_1 = 0$$

$$\Rightarrow -V_oR_1 = V\left[R_2 + Ls + R_1R_2Cs + R_1LCs^2\right]$$

$$\Rightarrow -V_o = \frac{VR_2}{R_1} + \left[\frac{L}{R_1} + R_2C\right]sV + LCs^2V$$

$$\Rightarrow -V_o = \frac{R_2}{R_1}V + \left[\frac{L}{R_1} + R_2C\right]\frac{dV}{dt} + LC\frac{d^2V}{dt^2}$$

Ques By virtual ground method, $v_p = v_n = 0$

Applying KCL at 'n' –

$$\frac{0-V_c}{3} + \frac{0-V_o}{5} = 0 \Rightarrow 5V_c + 3V_o = 0 \quad -(1)$$

Applying KCL at V_c –

$$\frac{V_c}{3} + \frac{V_c-21}{3} + \frac{V_c}{6} + \frac{V_c-V_o}{8} = 0$$

$$\Rightarrow \frac{V_c}{3} + \frac{V_c-21}{3} + \frac{V_c}{6} + \frac{V_c+\frac{5}{3}V_c}{8} = 0 \quad \{\text{from (1)}\}$$

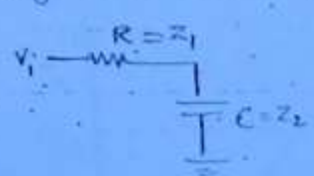
$\Rightarrow \quad V_c = 6V$

$\therefore I_i = \frac{21-V_c}{3K} = 5mA \; ; \; V_o = \frac{-5}{3}\times 6 = -10V \; ; \; R_i = \frac{V_i}{I_i} = \frac{21}{5} = 4.2\Omega$

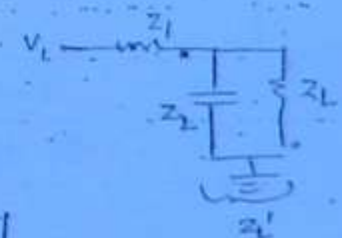
17th August, 2012

First order Buttersworth Filter:-

– Loading Effect –



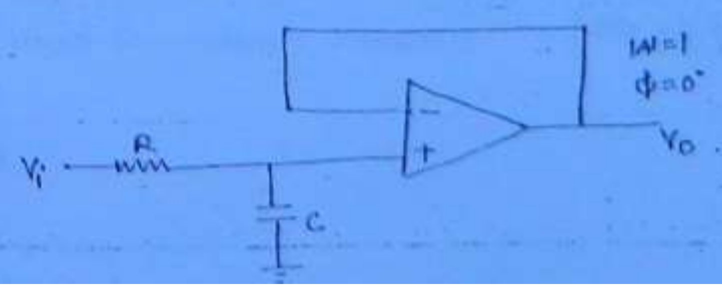
$I = \frac{V_i}{Z_1+Z_2}$



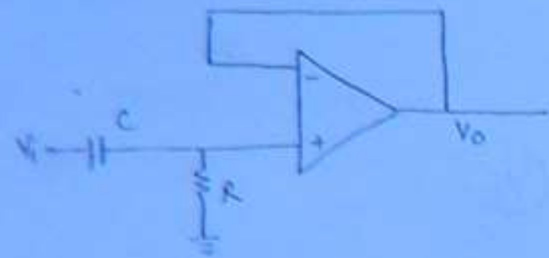
$I' = \frac{V_i}{Z_1+Z_2'}$

$\boxed{I < I'}$

→ I' will keep on ↑ as Z_L is ↑. Hence, there will be loading effect and parameters of filter will change. To avoid this, voltage follower circuit is used.



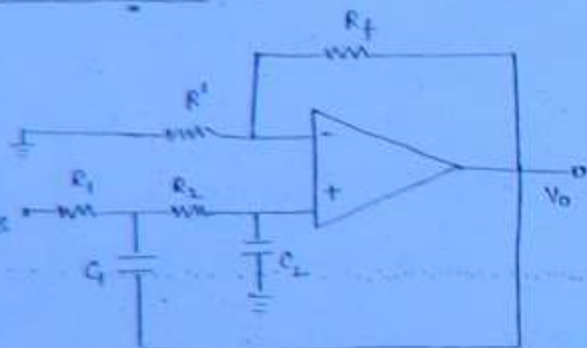
→ First order butterworth Filter.
LPF



→ HPF – First order BWF.

$$f_c = \frac{1}{2\pi RC}$$

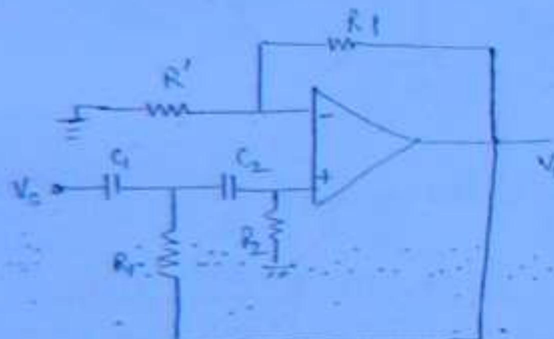
2^{nd} order LP BWF –



$$f_c = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}} = \frac{1}{2\pi RC}$$

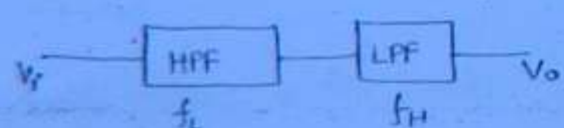
if $R_1 = R_2 = R$
& $C_1 = C_2 = C$.

2^{nd} order HP BWF –



f_c = same as above.

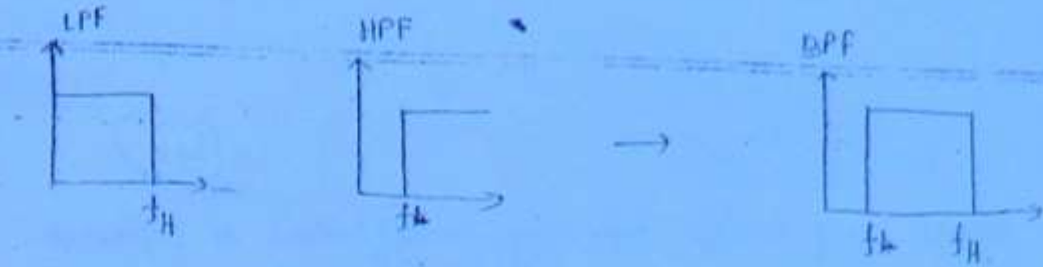
Band Pass filter :-



⇒ series connection or cascading.

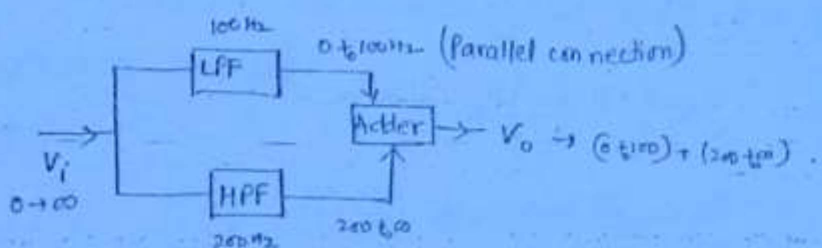
f_H = high 3dB cutoff frequency [for LPF]

f_L = low " " " [for HPF]



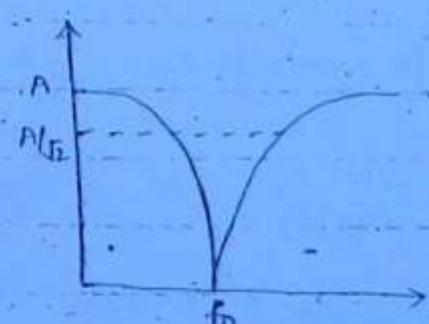
→ for BPF, $\boxed{f_H > f_L}$ **

Band Reject (or stop or Rejection) filter



→ for BSF, $\boxed{f_H < f_L}$ **

Notch Filter :-



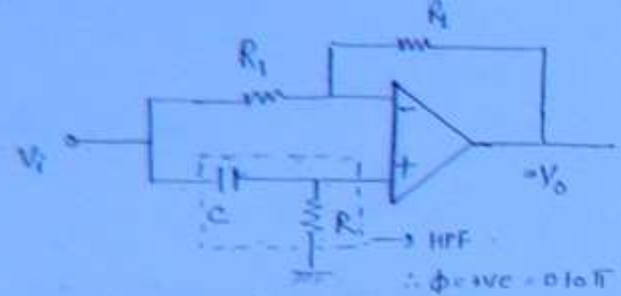
Narrow band
Band stop filter.

→ Used in communication systems. to eliminate power supply noise.
- Notch frequencies are 50Hz, 100Hz, 60 Hz etc.
- Also used to remove harmonics

All-Pass filter :

(44)

- It allows all input signal freq. to o/p w/o any amplification or attenuation.



Applying superposition -

for non-inverting terminal -

$$V_P = \frac{R}{R + \frac{1}{Cs}} \cdot V_i$$

$$V_{O_1} = \left(1 + \frac{R_1}{R_1}\right) V_P = 2V_P$$

$$V_{O_1} = \frac{2RCs}{RCs+1} \cdot V_i \quad \text{--- (1)}$$

for inverting terminal -

$$V_{O_2} = -\frac{R_1}{R_1} \cdot V_i = -V_i \quad \text{--- (2)}$$

$$\therefore V_o = V_{O_1} + V_{O_2} = V_i \left[\frac{2RCs}{1+RCs} - 1\right] \Rightarrow \left[\frac{-1+RCs}{1+RCs}\right] = \frac{V_o}{V_i}$$

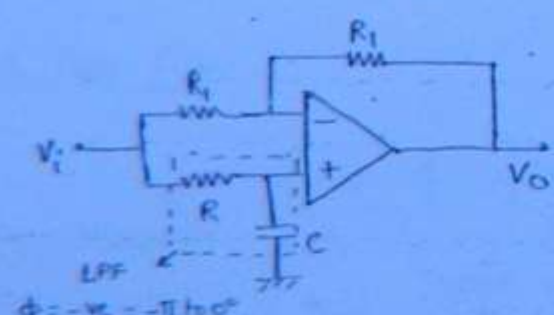
$$\Rightarrow A = -\frac{1-RCs}{1+RCs} \; ; \quad |A| = 1$$

$$\Rightarrow \boxed{\phi = 180 - 2\tan^{-1}(\omega RC)}$$ xdup

→ for $\omega = 0$ $\quad \phi = 180$ or π

for $\omega = \infty$ $\quad \phi = 0$

⇒ Range of phase - $\boxed{0 \leq \phi \leq 180^\circ}$



$$A = \frac{1-RCs}{1+RCs} \; ; \quad |A| = 1$$

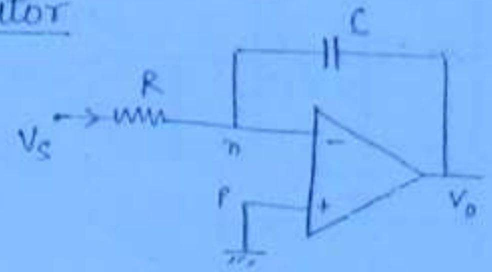
$$\boxed{\phi = -2\tan^{-1}(\omega RC)}$$ xdup

→ $\omega \to 0$ $\quad \phi = 0$

$\omega \to \infty$ $\quad \phi = -180^\circ$ or $-\pi$

$\boxed{\text{Range of } \phi = -\pi \text{ to } 0^\circ}$ xdup

Integrator



$$C\frac{d(V_n - V_o)}{dt} = \frac{V_s - V_n}{R}$$

$$\Rightarrow \frac{V_s}{R} = -C\frac{dV_o}{dt}$$

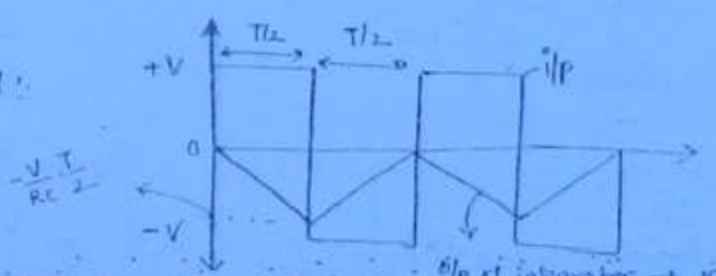
* Linear charging of capacitor is possible when we are providing constant current in the circuit and this can be achieved through current mirror circuit.

$$\Rightarrow \frac{dV_o}{dt} = \frac{-V_s}{RC} \Rightarrow V_o = \frac{-1}{RC}\int_0^t V_s\,dt + V_o(0^+)$$

$V_o(0^+)$ → initial value.

→ $\boxed{\phi = 180^\circ}$, hence called as $\boxed{\text{Inverting Integrator}}$ ***

Interview Ques:

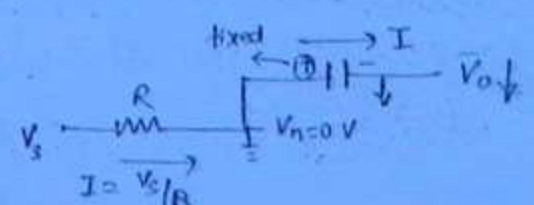


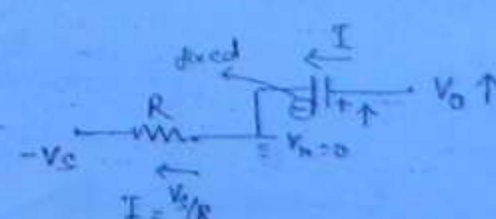
$\frac{dV_o}{dt}$ = rate of change of o/p = slope $= \frac{-V_s}{RC}$

for $V_s = +V \Rightarrow \frac{dV_o}{dt} = \frac{-V}{RC} \Rightarrow V_o \downarrow$

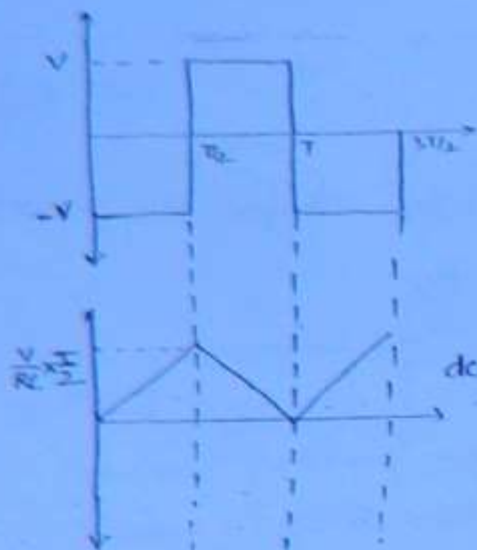
for $V_s = -V \Rightarrow \frac{dV_o}{dt} = \frac{V}{RC} \Rightarrow V_o \uparrow$

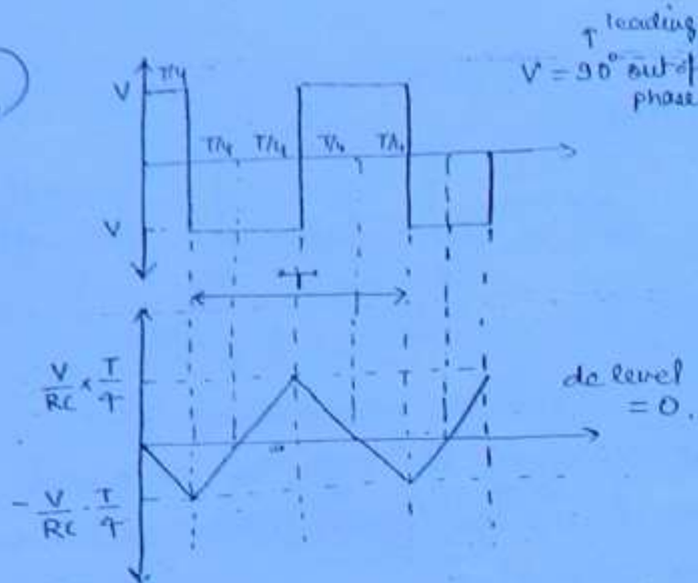
*





Eg.





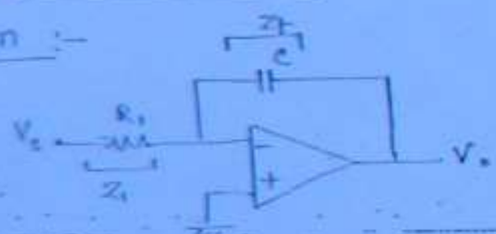
→ Time period of output = time period of input in all the three cases.

→ only change is in the dc levels of o/p.

** → Swing = $V_{max} - V_{min} = \frac{V}{RC}\times\frac{T}{2}$ is same in all the three cases.

→ $\boxed{\text{Swing} = \frac{V}{2RCf}}$

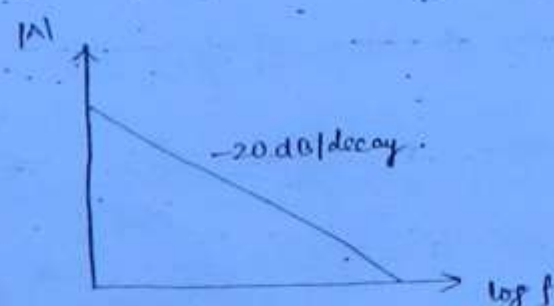
Problem :-

→ 

Gain, $A = \frac{-Z_f}{Z_1}$

$$\boxed{A = \frac{-1}{R_1 C s} = -\frac{1}{j\omega RC}}$$

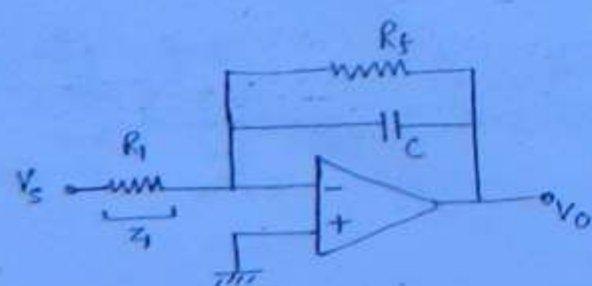
→ $|A| = \frac{1}{\omega RC}$.



→ At $\omega = 0$, $|A| = \infty$.

→ Gain is not stable for entire freq. range, hence no freq. stability. This is called Roll off problem.

Practical Integrator :-

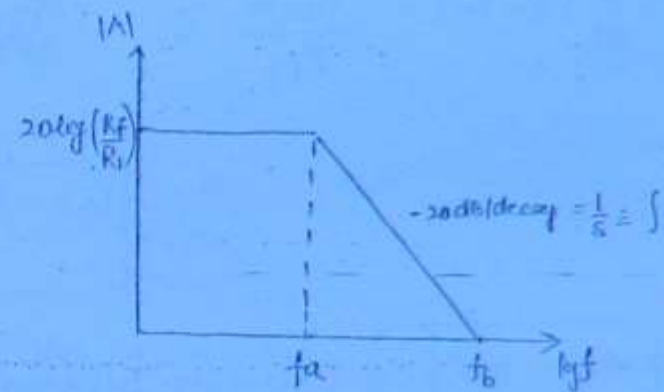


$Z_f = Z_C \| R_f = \dfrac{R_f \cdot \frac{1}{Cs}}{R_f + \frac{1}{Cs}} = \dfrac{R_f}{1 + R_f C s}$ (47)

$Z_1 = R_1$; $\therefore$ Gain, $A = -\dfrac{Z_f}{Z_1}$

$$\Rightarrow \quad A = -\frac{R_f/R_1}{1 + R_f C s}$$

$$\Rightarrow \quad A = \frac{-(R_f/R_1)}{1 + j\omega R_f C}$$



$\rightarrow$ $|A| = \dfrac{R_f/R_1}{\sqrt{1 + \omega^2 R_f^2 C^2}}$

$\rightarrow$ At $\omega = 0$, $|A|_{max} = \dfrac{R_f}{R_1}$.

$\rightarrow$ 3dB cutoff freq., $\omega_a = 2\pi f_a = \dfrac{1}{R_f C}$.

$$\Rightarrow \quad \boxed{f_a = \frac{1}{2\pi R_f C}}$$

$\rightarrow$ At $\omega = \omega_b$, $|A| = 1$

$\Rightarrow \dfrac{R_f^2}{R_1^2} = 1 + \omega_b^2 R_f^2 C^2 \Rightarrow \omega_b^2 R_f^2 C^2 \approx \dfrac{R_f^2}{R_1^2}$ {Neglecting 1}

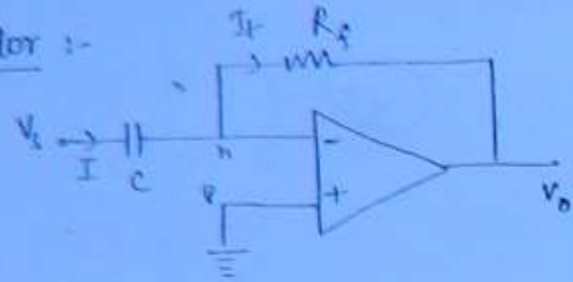
$\Rightarrow \boxed{\omega_b = \dfrac{1}{R_1 C}}$ or $\boxed{f_b = \dfrac{1}{2\pi R_1 C}}$ **imp. {(?) $f_b = G \times BW$, $\because |A| = 1$ at this freq.}

$\rightarrow$ Circuit acts as integrator between f_a and f_b.

*\$ $f_a < f_b \Rightarrow \dfrac{1}{2\pi R_f C} < \dfrac{1}{2\pi R_1 C} \Rightarrow R_1 < R_f$

48

Differentiator :-



$V_P = V_n = 0$

$I = I_f$.

$$C\frac{d}{dt}(V_s - V_n) = \frac{V_n - V_o}{R_f} \Rightarrow \frac{C\,dV_s}{dt} = \frac{-V_o}{R_f}$$

$$\Rightarrow \boxed{V_o = -R_f C \cdot \frac{d\,V_s}{dt}}$$

→ $\boxed{\phi \text{ shift} = 180^\circ}$ ⇒ Inverting Differentiator

→ $A = -\frac{R_f}{Z_1}$ ⇒ $A = -R_f C s = -j\omega R_f C$.

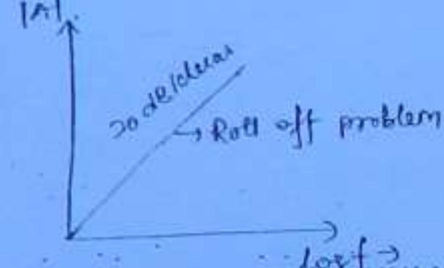
→ $|A| = \omega R_f C$.

Problem -

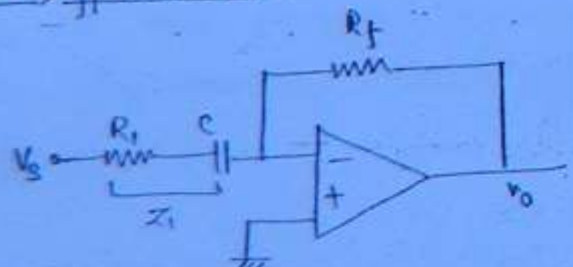
→ At $\omega = \infty$, $|A| = \infty$.

→ frequency stability is less.

→ Roll off problem.



Practical Differentiator :-

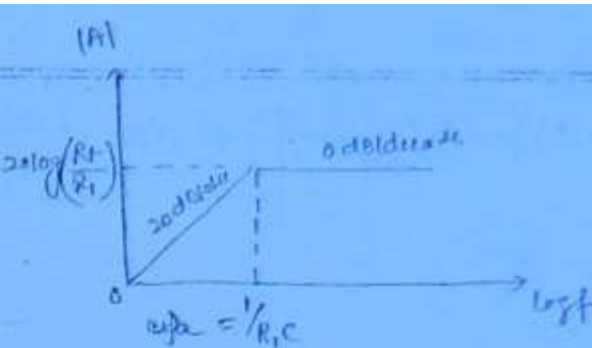


$Z_f = R_f$

$Z_1 = R_1 + 1/Cs = \frac{R_1 Cs + 1}{Cs}$.

$$\therefore A = \frac{-R_f}{R_1 + 1/Cs} = \frac{-R_f/R_1}{1 + \frac{1}{R_1 Cs}} \Rightarrow \boxed{A = \frac{-R_f/R_1}{1 - j/\omega R_1 C}}$$

$\rightarrow |A| = \dfrac{R_f/R_1}{\sqrt{1+ 1/\omega^2R_1^2C^2}}$ (49)



$\rightarrow$ As $\omega \rightarrow \infty$, $|A|_{max} = \dfrac{R_f}{R_1}$.

$\Rightarrow$ Circuit is stable at high frequency.

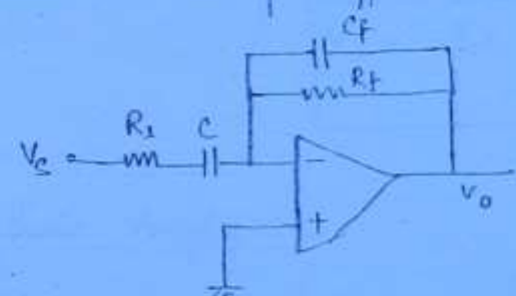
$\rightarrow A = -\dfrac{sCR_f}{1+sCR_1}$ $\rightarrow$ Plotting Bode plot

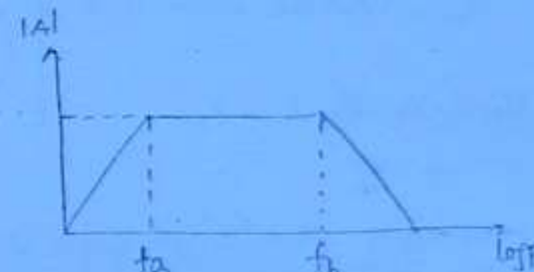
$\rightarrow \boxed{f_a = \dfrac{1}{2\pi R_1 C}}$

$\rightarrow$ Circuit will act as differentiator b/w 0 and f_a

$\rightarrow$ But, BW = ∞.

To limit the BW of Differentiator –





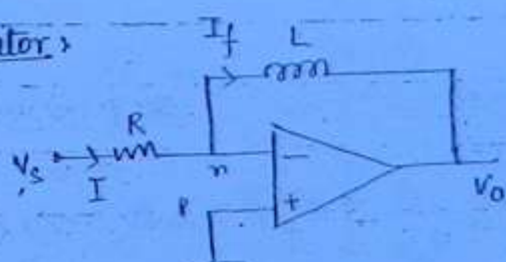
$\rightarrow$ C_f will limit the bandwidth of differentiator.

$\rightarrow$ BPF is also called as Practical differentiator.

$\rightarrow$ R_1 is added to increase the frequency stability of the output.

Differentiator:

*



$V_p = V_n = 0$

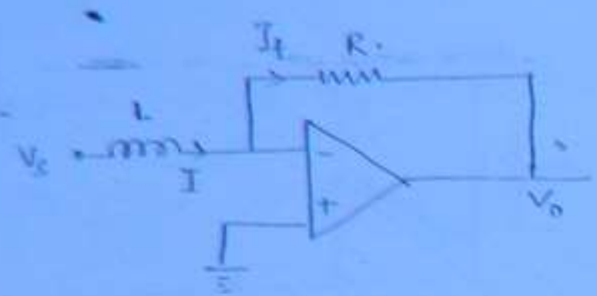
$I = I_f$

$\Rightarrow \dfrac{V_s}{R} = -\dfrac{1}{L}\int V_o\, dt$

$\Rightarrow \boxed{-\dfrac{L}{R}\dfrac{dV_s}{dt} = V_o}$

$\hookrightarrow$ Bulky and Heavy due to L.

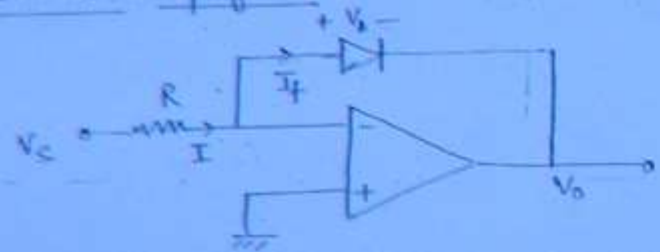
Inductor as Integrator :-



$I = I_f$

$\Rightarrow V_0 = -\frac{R}{L}\int_0^t V_s \, dt$

Logarithmic Amplifier :-



$V_p = V_n = 0$

$I = I_f = I_D$

$I_D = I_0\left[e^{V_D/\eta V_T} - 1\right]$

→ 

I_0 = reverse saturation current.

$V_D = V_n - V_0 = -V_0$

$I = I_D$

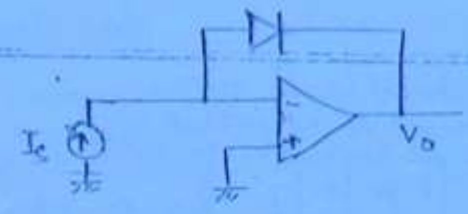
$\Rightarrow \frac{V_s}{R} = I_0\left[e^{-V_0/\eta V_T} - 1\right]$

$\Rightarrow \frac{V_s}{I_0 R} + 1 = e^{-V_0/\eta V_T} \quad \Rightarrow \frac{V_0}{\eta V_T} = -\ln\left[\frac{V_s}{I_0 R} + 1\right]$

$$\Rightarrow \boxed{V_0 = -\eta V_T \ln\left[\frac{V_s}{I_0 R} + 1\right]}$$

$\Rightarrow I_0$ is very small $\Rightarrow \frac{V_s}{I_0 R} >> 1$.

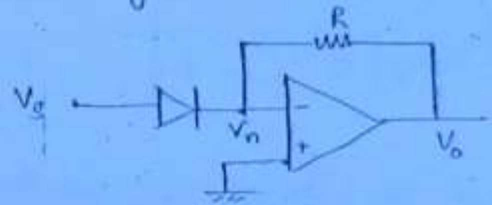
$$\therefore \boxed{V_0 = -\eta V_T \ln\left[\frac{V_s}{I_0 R}\right]}$$ → imp

* 

$$\Rightarrow \boxed{V_o = -\eta V_T \ln\left(\frac{I_c}{I_o}\right)} \quad \left\{\frac{V_s}{R} = I_s\right\}.$$

57

Anti-logrithmic Amplifier



$$V_D = V_s - V_n = V_s \;; \quad I = I_f = I_D$$

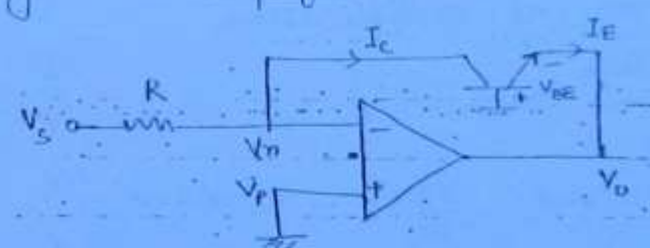
$$\therefore \; I_o\left[e^{V_s/\eta V_T} - 1\right] = \frac{V_n - V_o}{R}$$

$\Rightarrow \because V_s > 0$ and if $e^{V_s/\eta V_T} >> 1$

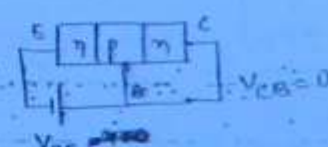
$$\Rightarrow \quad V_o = -I_o R\, e^{V_s/\eta V_T}$$

$$\Rightarrow \boxed{V_o = -I_o R \text{ antilog}\left(\frac{V_s}{\eta V_T}\right)}$$

Logrithmic Amplifier :-



Tr. should be in active region, ie, V_c = +ve so that V_o = -ve.



$$\Rightarrow V_{BE} = -V_o \quad \left\{\because V_B = 0 \text{ and } V_c = 0\right\}$$

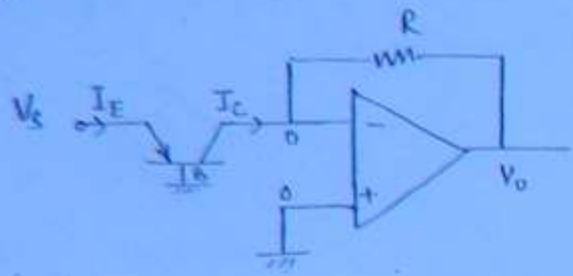
$$I_D = I_C \simeq I_E = I_{co}\left[e^{V_{BE}/\eta V_T} - 1\right] = \frac{V_s}{R}$$

$$\Rightarrow \quad \frac{V_s}{I_{co}R} + 1 = e^{V_{BE}/\eta V_T}$$

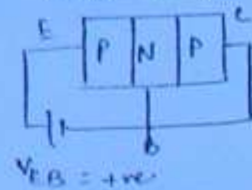
$$\Rightarrow \quad V_o = -V_T \ln\left[\frac{V_s}{I_{co}R} + 1\right] \qquad \text{for } \eta = 1$$

$$\Rightarrow \boxed{V_o = -V_T \ln\left[\frac{V_s}{I_{co}R}\right]}$$

Anti-logarithmic Amplifier :-



Tr. should be in active region, hence V_s = +ve, so that V_{EB} = +ve.



$V_{CB} = 0. \rightarrow$ RB

V_{EB} = +ve $\rightarrow$ FB.

$$V_{EB} = V_s$$

$$I_E = I_C = I_f$$

$$I_D = I_C \simeq I_E = I_{CO}\left[e^{V_s/\eta V_T} - 1\right]$$

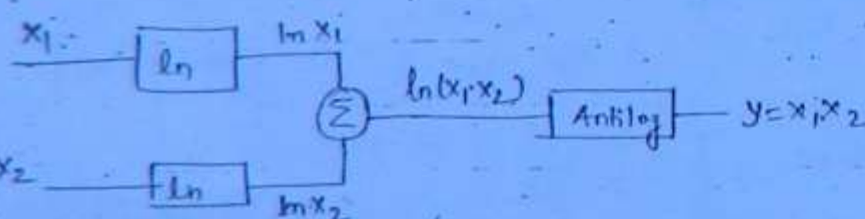
$$\Rightarrow \quad I_{CO}\left[e^{V_s/\eta V_T} - 1\right] = \frac{0 - V_o}{R}$$

$$\Rightarrow \quad V_o = -I_{CO}R\left[e^{V_s/\eta V_T} - 1\right] \quad \Rightarrow \quad \boxed{V_o \cong -I_{CO}R \text{ antilog}\left(\frac{V_s}{\eta V_T}\right)}$$

Applications

- Log and Antilog amplifiers are used in designing of multiplication, division, square root and squaring circuits.

*

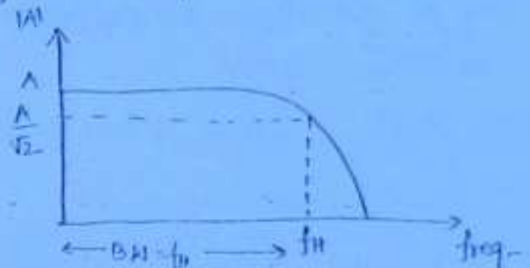


→ If the -ve sign is not set for o/p, then pass o/p through a inverting amplifier with gain = 1.

20th August, 2012

53

Frequency Response of Practical op-amp –



$|Z_C| = \frac{1}{2\pi f C}$; $f\uparrow$, $|Z_C|\downarrow$

– Op-Amp is basically a dc amplifier., It can amplify a dc signal and also an ac signal in a wide band, extendending from 0–1 MHz.

Slew Rate (S_R) –

→ It is the time rate of change of closed loop amplifier o/p voltage under large signal condition. (Typical value = 1V/μsec). Unit → V/μsec.

$$\rightarrow SR = \left.\frac{dV_o}{dt}\right|_{max} \Rightarrow SR = \frac{dV_o}{dV_i} \times \frac{dV_i}{dt}$$

$$\boxed{SR = |A_{CL}| \times \left.\frac{dV_i}{dt}\right|_{max}}$$ imp

Ex. $V_i = V_m \sin \omega t$ $\therefore \frac{dV_i}{dt} = V_m \omega \cdot \cos \omega t$ $\therefore SR = |A_{CL}| \times V_m \omega_m$

$$\Rightarrow \left.\frac{dV_i}{dt}\right|_{max} = V_m \omega_m \quad \Rightarrow \boxed{\omega_m = 2\pi f_m = \frac{SR}{|A_{CL}| \cdot V_m}} \text{ rad/sec}$$ imp

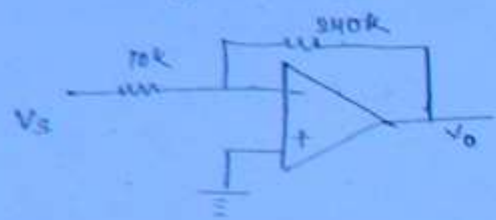
ω_m or f_m → Max freq. of operation.

⇒ For $f \le f_m$ → o/p without distortion
$f > f_m$ → " with "

Que – for an operational amplifier having a SR of 2V/μsec. ~~for the~~ What is the max. closed loop voltage gain that can be used when i/p signal changes by 0.5V in 10 μsec?

(54)

Ques: for the given circuit, determine the max freq. of operation in rad/sec that can be used by taking $SR = 0.5\ V/\mu sec$ and $V_m = 0.02V$.



Solⁿ (1) $SR = 2V/\mu sec$

$\frac{dV_i}{dt} = 0.05\ V/\mu sec$

$\therefore\ SR = |A_{CL}| \times \frac{dV_i}{dt}$

$\Rightarrow 2 = |A_{CL}| \times 0.05$

$\Rightarrow |A_{CL}| = 40.$

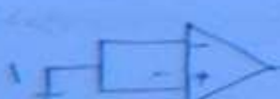
Solⁿ (2) $|A_{cl}| = \left| -\frac{240}{10} \right| = +24.$

$\omega_m = \frac{24\ 0.5 \times 10^6}{24 \times 0.02} = \frac{2.08}{2}\ rad/sec \cdot \times 10^6 = 1.04\ rad/sec \cdot \times 10^6$

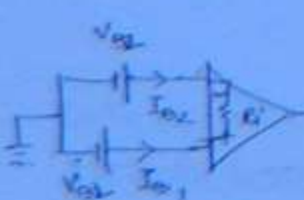
Note - If A_{cl} is not given, take $A_{cl} = 1$.

* - Slew rate is limited by internal capacitances of op-amp. hence it is not ∞.

<u>Offset voltages and currents</u> :-

→  $V_o = 0$ → Balanced op-amp.

if $V_o \neq 0 = V_{OO}$ → output offset voltage.

→ 

$V_o = 0$ → Now it is balanced.

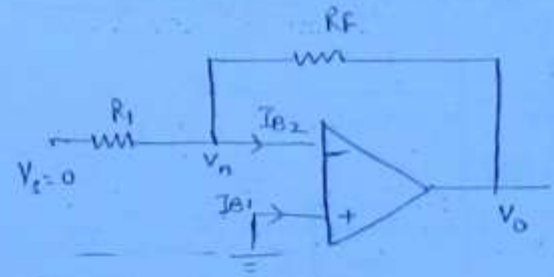
V_{os1}, V_{os2} - Biasing voltages.

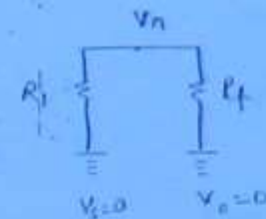
→ i/p bias current $= I_B = \frac{I_{B_1} + I_{B_2}}{2}$, when $V_o = 0$.

→ i/p offset current $= I_{io} = I_{B_1} - I_{B_2}$ when $V_o = 0$.

→ i/p offset voltage $= V_{io} = I_{io} \cdot R_i = V_{B_1} - V_{B_2}$ when $V_o = 0$.

→





$R_{eq} = R_1 || R_f$

$|V_n| = R_{eq} \cdot I_{B_2} = I_{B_2}[R_1 || R_f]$.

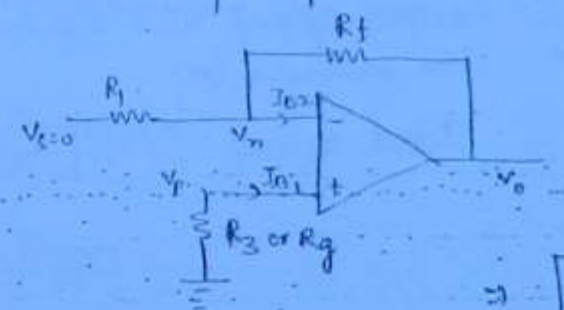
$|V_p| = 0$

– ∴ Amplifier is again unbalanced when $V_s = 0$ (ie without signal) & feedback is connected.

→ Normally, $I_{B_1} \cong I_{B_2}$.

→ To balance the op-amp, R_3 is connected to non-inverting terminal.

→



Now, $|V_p| = I_{B_1} \cdot R_3$.

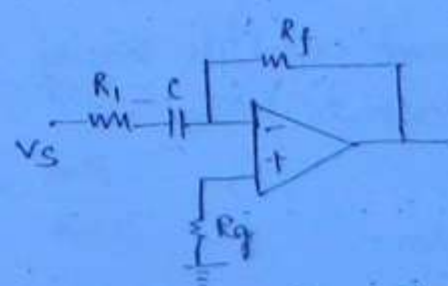
Hence, for balanced condition –

$|V_p| = |V_n|$

$\Rightarrow \boxed{R_3 = [R_1 || R_f]}$ **

* To minimise the effect of I/p bias current, one should place in non-inverting terminal, a <u>resistance equal to dc resistance seen by inverting terminal</u>.

Ques What is R_g?



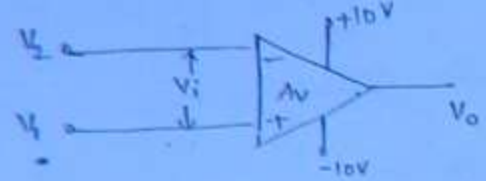
Sol^n $R_g = [R_1 + Z_C] || R_f$.

$Z_C = \frac{1}{2\pi f C} \Rightarrow Z_C = \infty$ for DC.

$\Rightarrow R_g = [R_1 + \infty] || R_f = R_f$. Ans

Transfer Characteristics of Op-Amp :-

i) Practical Op-amp :-



$A_v = 10^6$

$V_i = V_1 - V_2$

$\Rightarrow V_o = 10^6 (V_1 - V_2)$. — ①

Now, (i) $V_1 = 10\mu V$, $V_2 = 9\mu V$

$\Rightarrow V_o = 1V$

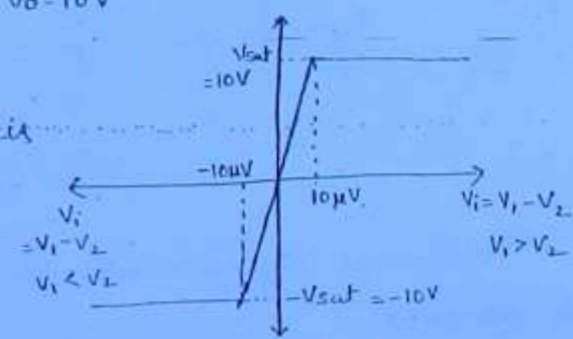
(ii) $V_1 = 100\mu V$, $V_2 = 90\mu V$

$\Rightarrow V_o = 10V$

(iii) $V_1 = 120\mu V$, $V_2 = 100\mu V$

$\Rightarrow V_o = 20V$ but $> 10\mu V$ → Op amp is saturated.

$\Rightarrow V_o = 10\mu V$



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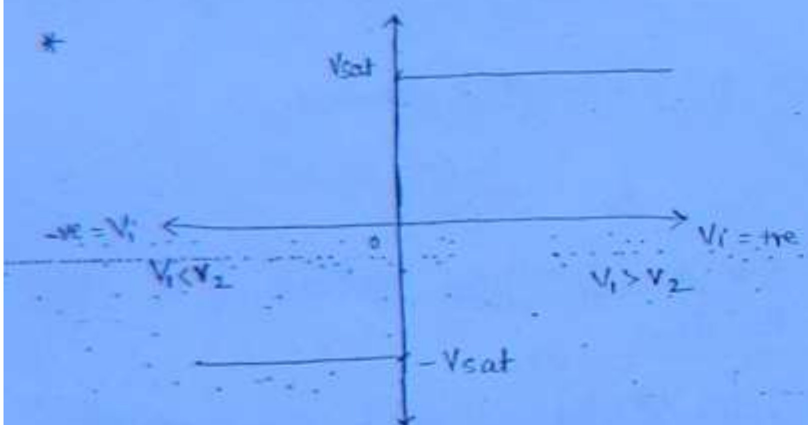


← Practical Op-amp with sufficient +ve feedback. (or)

Ideal Op-amp , i.e., $[A_v \cong \infty]$

→ As $|A|_a \uparrow$, for a very small i/p, output will shoots up to +Vsat or -Vsat depending on ~~+Vsat~~ $V_1 - V_2$ to be +ve or -ve.

→ In a practical op-amp, o/p voltage cannot exceed its biasing voltage, ie, range of o/p voltage is from - Vsat to +Vsat.

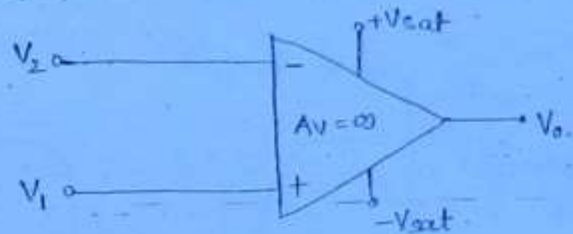
→ op-amp can enter into saturation when -

(a) large i/p signals are applied. (> than few μV).

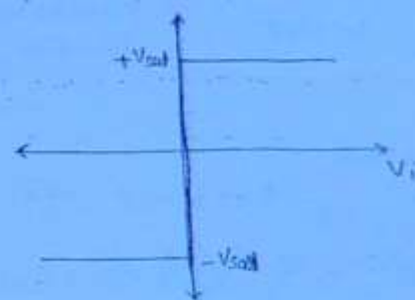
(ii) When sufficient +ve feedback is provided.

Comparator :-

Ideal comparator :-



		V_o	
1)	$V_1 > V_2$	$+V_{sat}$	1
2)	$V_1 < V_2$	$-V_{sat}$	0

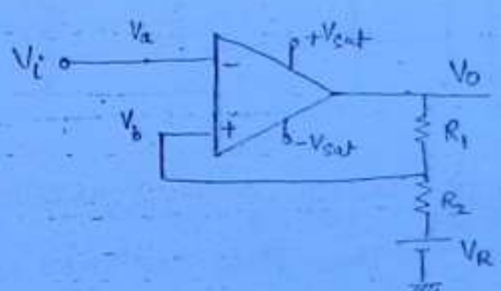


Characteristics

→ It is operated under open loop condition.

Practical Comparator :-

Schmitt - Trigger :-



$|V_R| \rightarrow$ Reference voltage $< |V_{sat}|$.

$V_b > V_a$	$+V_{sat}$	1
$V_b < V_a$	$-V_{sat}$	0

$$\rightarrow \quad V_b = \frac{V_o R_2}{R_1 + R_2} + \frac{V_R R_1}{R_1 + R_2}$$

① $V_o = +V_{sat}$

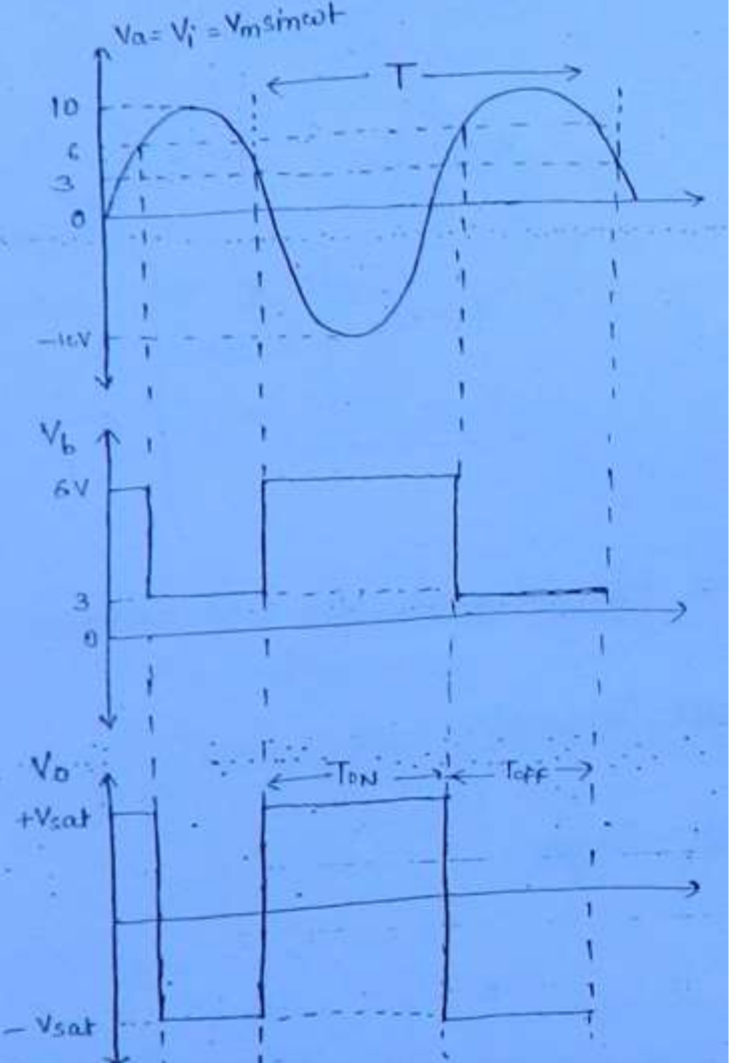
$$V_{b_1} = \frac{V_{sat} R_2}{R_1+R_2} + \frac{V_R \cdot R_1}{R_1+R_2} = V_{UTh} \rightarrow \text{Upper Threshold}$$

② $V_o = -V_{sat}$.

$$V_{b_2} = -\frac{V_{sat} \cdot R_2}{R_1+R_2} + \frac{V_R \cdot R_1}{R_1+R_2} = V_{LTH} \rightarrow \text{lower Threshold.}$$

Assumption :- let $V_{UTh} = V_{b_1} = 6V$, $V_{LTh} = V_{b_2} = 3V$. These are set, before applying V_i, on the basis of $\pm V_{sat}$ & V_R ...

$V_m = 10V$.



① At $t=0$,

let $V_o = +V_{sat}$

$\therefore V_b = V_{b_1} = 6V$.

$V_i = V_a = 0 \Rightarrow V_b > V_a \Rightarrow V_o = +V_{sat}$

Hence, our assumptions are right.

or

let $V_o = -V_{sat}$

$V_b = V_{b_2} = 3V$.

$V_i = V_a = 0 \Rightarrow V_b > V_a \Rightarrow V_o = +V_{sat}$

Hence our assumption was wrong

$V_o = +V_{sat}$

① $V_i\uparrow$; $V_a\uparrow$ & when $V_a \geq V_{b_1} = 6V$, then V_o switches from $+V_{sat}$ to $-V_{sat}$ and V_b " " $+6V$ " $+3V$.

② $V_i\downarrow$; $V_a\downarrow$ & when $V_a \leq V_{b_2} = 3V$, then V_o switches from $-V_{sat}$ to $+V_{sat}$. and V_b " " $+3V$ to $+6V$.

Thus these two steps will be repeated.

* Necessary condition —

(a) V_i should ↑ and cross V_{UTh} ; so that V_0 switches from $+V_{sat}$ to $-V_{sat}$

(b) V_i should ↓ and cross V_{LTh} ; " " V_0 " " $-V_{sat}$ " $+V_{sat}$.

* Time period of o/p = $\boxed{T_0 = T_{ON} + T_{OFF} = T =}$ time period of i/p.

→ ∵ $T_{ON} > T_{OFF}$; Duty cycle $= \frac{T_{ON}}{T_{ON}+T_{OFF}} \times 100\%$.

⇒ $D > 50\%$, ⇒ Asymmetrical square wave

→ It is a square wave converter.

Eg :- ① $V_i = 2\sin\omega t$ & $V_{b_1} = 6V$, $V_{b_2} = 3V$

∴ $V_0 = +V_{sat}$ always.

② $V_i = 4$ to 5

V_0 depends on initial condit

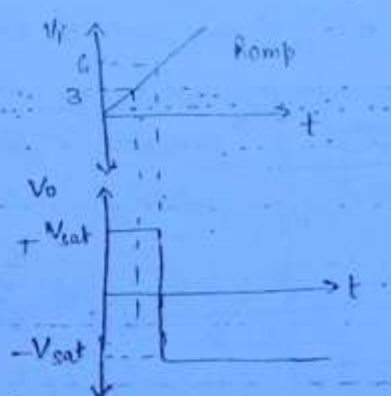
If $+V_{sat}$ then will remain $+V_{sat}$

" $-V_{sat}$ " " " $-V_{sat}$

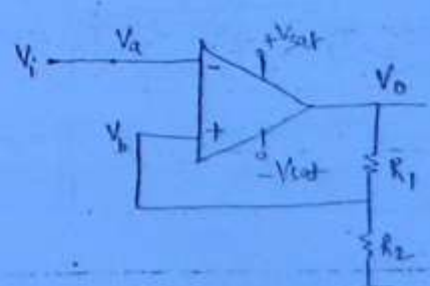
③ $V_i = > 6$ volts.

∴ $V_0 = -V_{sat}$ always.

④



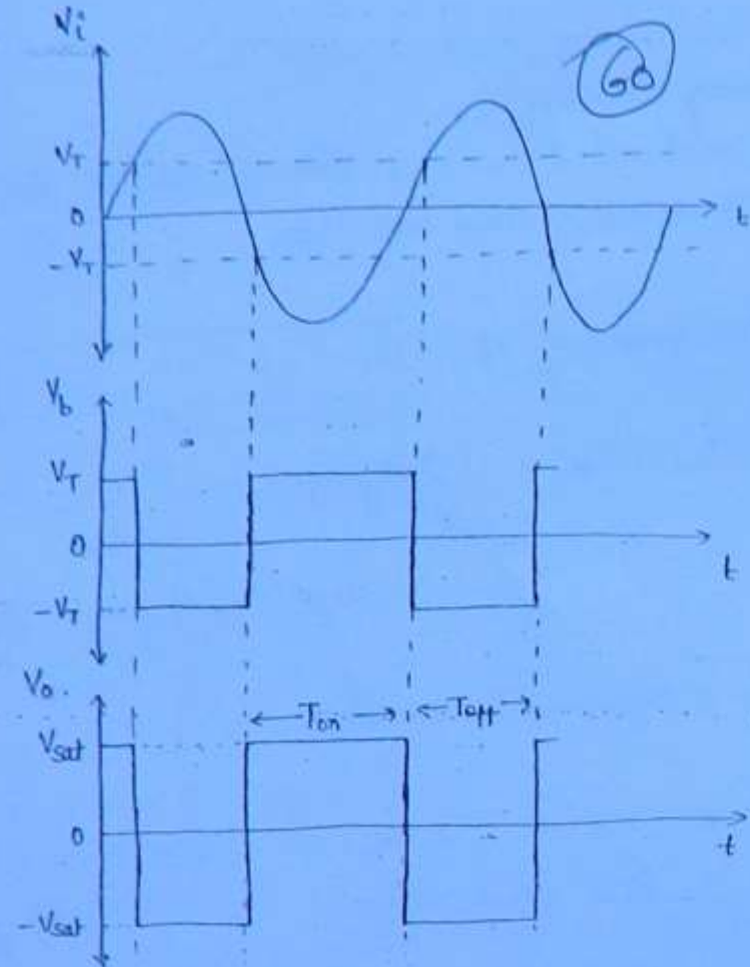
Duty cycle :- for $D = 50\%$, $V_R = 0$.



$V_{b_1} = \frac{+V_{sat} \cdot R_2}{R_1+R_2} = +V_T$

$V_{b_2} = \frac{-V_{sat} \cdot R_2}{R_1+R_2} = -V_T$

→ Time period of o/p = same as time period of i/p and hence by changing V_R we cannot change the frequency of output, we can only change the duty cycle, in turn, the avg. dc level (+ve area) of o/p will change.



→

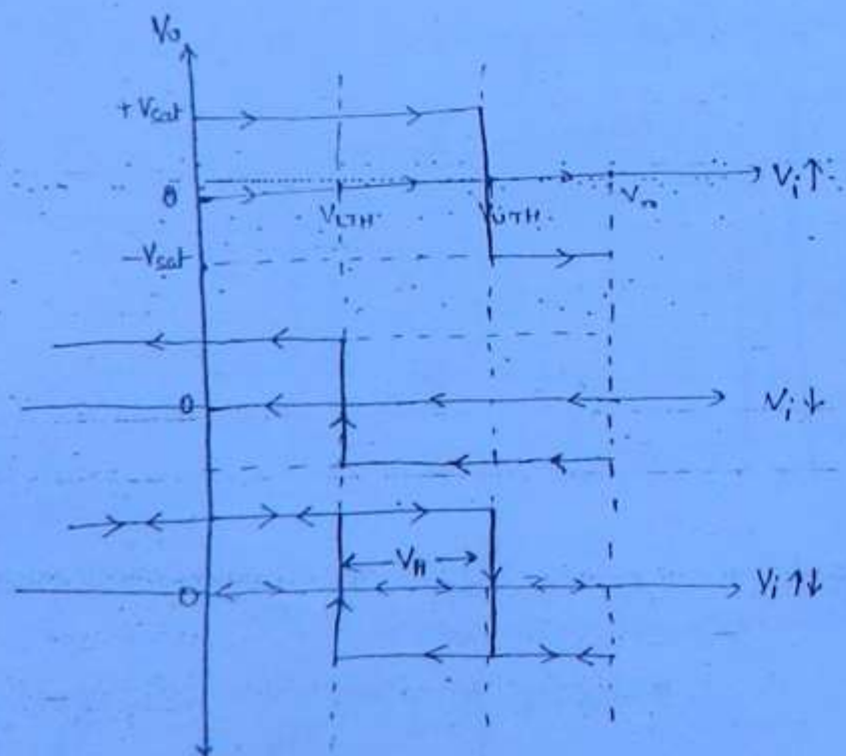
V_R = +ve	D > 50%
V_R = 0	D = 50%
V_R = -ve	D < 50%

Hysterisis Loop :-

1) For Asymmetrical Wave →

V_H = Hysterisis voltage

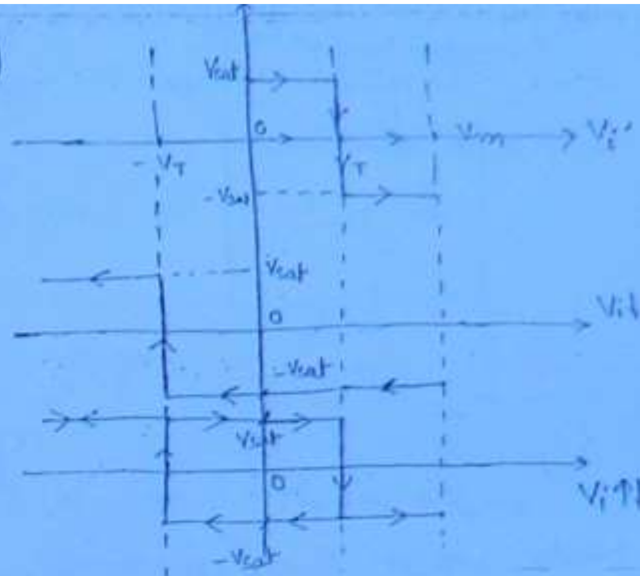
$= V_{UTH} - V_{LTH}$

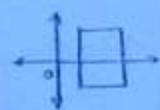
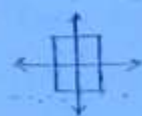
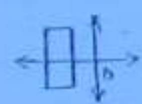


(2) For symmetrical wave —

61

$V_H = 2V_T$



V_R	Duty cycle	Avg. DC level	Hysterisis loop
$V_R > 0$	$D > 50\%$	+ve	
$V_R = 0$	$D = 50\%$	= 0	
$V_R < 0$	$D < 50\%$	< 0 or −ve	

→ This table is valid only for the circuit discussed earlier.

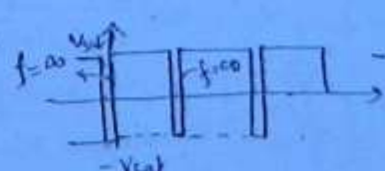
→ $V_R = \frac{R_2}{R_1+R_2} \cdot V_{sat} = \alpha \cdot V_{sat}$; $\alpha = \frac{R_2}{R_1+R_2} < 1$.

Hence, on non-inverting terminal, we are getting attenuated square wave.

→ $V_H = \left(\frac{V_{sat} \cdot R_2}{R_1+R_2} + \frac{V_R R_1}{R_1+R_2}\right) - \left(\frac{-V_{sat} \cdot R_2}{R_1+R_2} + \frac{V_R R_1}{R_1+R_2}\right)$

$\Rightarrow V_H = \frac{2V_{sat} \cdot R_2}{R_1+R_2}$ ⇒ Hysterisis voltage is independent of V_R; only the position of loop will change.

→ A slow moving waveform (sin t) can be converted into a fast moving waveform (square wave) by using schmitt trigger.

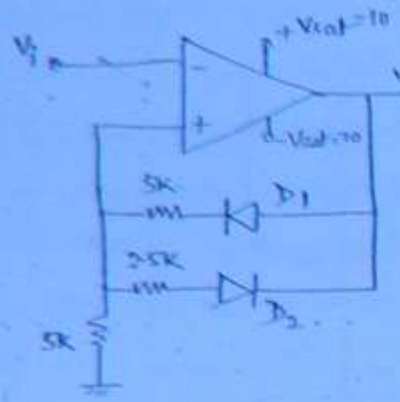


→ By adjusting duty cycle.

→ Slew Rate should be high, so that the triggering pulse reaches $+V_{sat}$ or $-V_{sat}$ very fast.

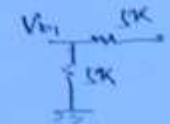
Hence, SR ↑ for triggering op-amp.

Ques



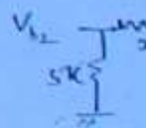
Consider schmitt tri

Sol^n For $+V_{sat}=10V$, $\Rightarrow D_1=ON$, $D_2=OFF$



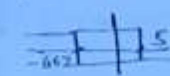
$V_0=10V \Rightarrow V_{b1}=5V$

For $V_{sat}=-10V$, $D_1=OFF$, $D_2=ON$

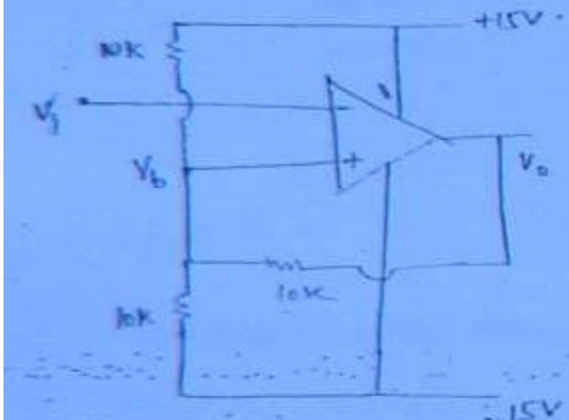


$-10V \quad \therefore V_{b2}=\frac{-10\times 5}{7.5}=-6.67V$

$\therefore$ Hysteresis loop :-



Ques Consider schmitt trigger ckt. A Δ wave which goes from -12V to +12V is applied to inverting i/p of op-amp. Assume that o/p swings from +15 to -15V. The voltage at non-inverting i/p switches b/w.



Sol^n KCL at V_b—

$$V_b\left[\frac{1}{10}+\frac{1}{10}+\frac{1}{10}\right]-\frac{15}{10}+\frac{15}{10}-\frac{V_0}{10}=0$$

$\Rightarrow 3V_b=V_0$

$\Rightarrow V_b=V_0/3$

$V_b = +5V$ to $+5V$.

Find range —

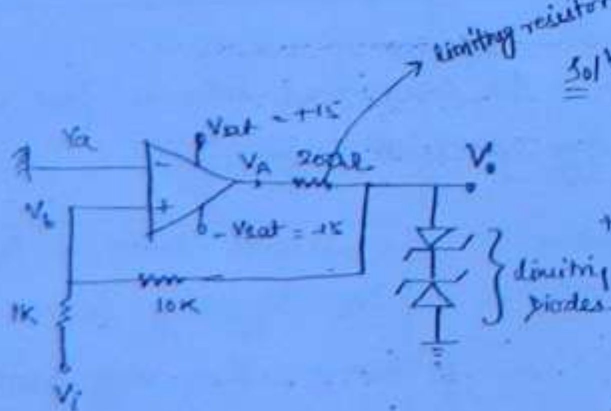
(a) -12 to 12V (c) -5 to +5V

(b) -7.5 to 7.5V (d) 0 to 5V

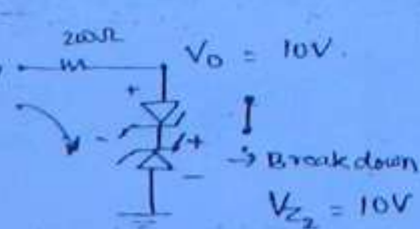
21st August, 2012

Textbook Pg-62

Ques 5



Sol^n When $V_b>V_a$, $V_A=+V_{sat}=15V$



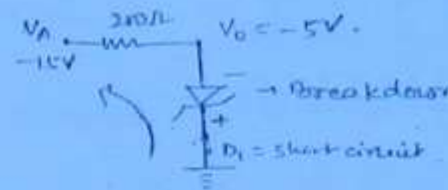
$V_0 = 10V$

$V_{Z_2}=10V$

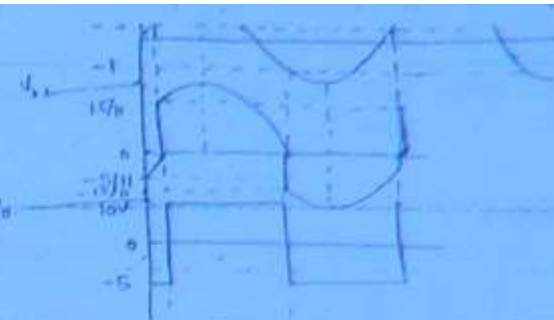
Hence, zener voltage rating $=10V$.

when $V_b < V_a$, $V_A = -V_{sat} = -15V$.

63



* For practical diodes
$V_{cc} = 0.7V$
$\therefore V_{Z1} = 4.3V$.



$\rightarrow 200\Omega$ is connected to dissipate the extra voltage.

Applying KCL at V_b —

$$V_b - V_i + \frac{V_b}{10} - \frac{V_0}{10} = 0$$

$$\Rightarrow V_b = \frac{V_0 + 10V_i}{11}$$

case I

when $V_0 = +10V$. $\Rightarrow V_b > V_a \Rightarrow V_b > 0$

$$V_b = \frac{V_i \cdot 10 + 10}{11}$$

As $V_i \downarrow$, V_b will also reduce.

and when ~~$V_b \neq V_a \Rightarrow V_b < 0$~~

$V_b = 0 \Rightarrow$ the o/p will switch from $+10V$ to $-5V$.

$\therefore V_b = \frac{10V_i + 10}{11} = 0 \Rightarrow V_i = -1V = V_{LTh}$.

Case II $V_0 = -5V \Rightarrow V_b < V_a \Rightarrow V_b < 0$

$$\Rightarrow V_b = \frac{10V_i - 5}{11}$$

As $V_i \uparrow$, V_b will also $\uparrow$.

and when $V_b = 0$, V_0 will switch from -5 to $10V \Rightarrow 10V_i - 5 = 0$

$\Rightarrow V_i = 0.5V = V_{UTh}$

At $t=0$, $V_i = 0$, $V_b = \frac{V_0}{11}$, let $V_0 = -5V$
and is $\uparrow$ (case 2) $\Rightarrow V_b = -5/11$

Multivibrator :-

$\rightarrow$ It is a device whose o/p vibrates b/w two levels, ie, low level and high level (or 0 and 1).

$\rightarrow$ These are of three types —

(i) Bistable

0 $\boxed{\text{Stable}}$
$\downarrow$ with trigger
1 $\boxed{\text{Stable}}$
$\downarrow$ with trigger
0

Eg- flip flop, binary, schmitt trigger

(ii) Monostable

Q $\bar{Q}$
1 0 $\boxed{\text{Stable}}$
$\downarrow$ $\downarrow$ with trigger
0 1 (Quasi stable)
$\downarrow$ $\downarrow$ without trigger
1 0

one shot or uni vibrator

(iii) Astable $\rightarrow$ Free running Multivibrator

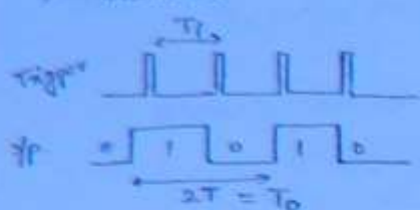
0 Quasi stable
$\downarrow$ w/o trigger
1 Quasi stable
$\downarrow$ w/o trigger
0

Square wave generator

with V_i not very high).

* when $V_i \uparrow$ then $V_o \downarrow$ and vice versa $\Rightarrow$ -ve feedback.
  " $V_i \uparrow$ " $V_o \uparrow$ and " " $\Rightarrow$ +ve feedback.

→ Bistable :-

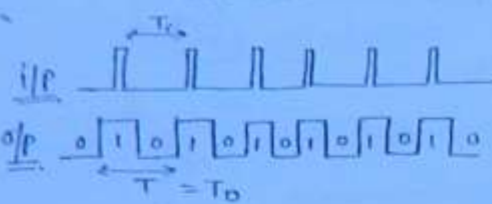


$\boxed{f_o \le f_i}$

$\Uparrow$

$\boxed{T_o \ge T_i}$

– Monostable :-



→ Bistable and Monostable are simply convertors and not square wave generators whereas for Astable Multivibrator, no need of an input / trigger to generate square wave.

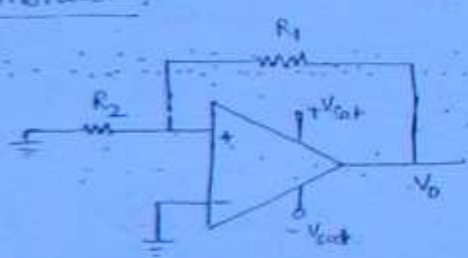
→ Fastest o/p will be given by astable multivibrator as it is not limited by frequency of input trigger.

Note

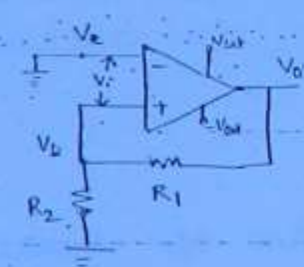
– Astable multivibrator is often used as fastest waveform generator.

Multivibrator by using operational Amplifier :-

Bistable Multivibrator :-



≡



$$V_b = \frac{R_2}{R_1+R_2} \cdot V_o$$

Initially, $V_o = 0,\ V_b = 0,\ V_a = 0$

$\Rightarrow V_i = 0 \Rightarrow V_o = 0$ (Ideally).

but because of noise :-

$V_b \uparrow \Rightarrow V_i = V_b - V_a \uparrow \Rightarrow V_o = A V_i \uparrow$.

$\Rightarrow$ V_b again $\uparrow$ due to V_o and it will keep on $\uparrow$ till it reaches $+V_{sat}$ and then ckt. will remain in one of the stable state.

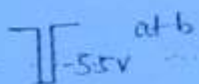
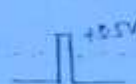
→ Because of noise, o/p initially can be at $+V_{sat}$ or $-V_{sat}$ depending on initia noise effect.

Eg let $R_1 = R_2$ and $V_{sat} = 10V \Rightarrow V_b = 5V$.

Now, to change the stable state of V_b from $+V_{sat}$ to $-V_{sat}$ –

(a) Positive trigger can be applied at V_a (or)

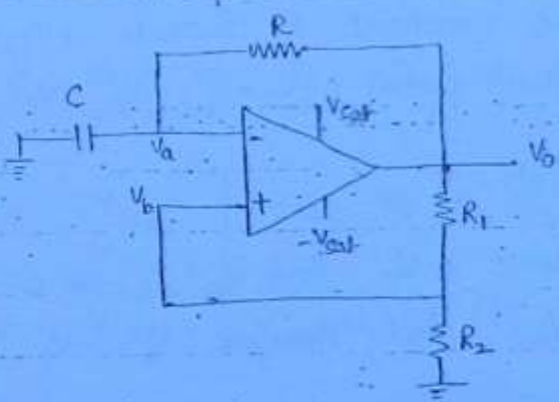
(b) Negative " " " " V_b and trigger value should be more than the present V_b value. (ie, more than 5V)

i.e; Eg  at b or  at a and the circuit will

switch ~~it~~ to its other stable state

– It has volatile memory., ie., memory is lost when power supply is interrupted.

Astable Multivibrator / Square Wave Generator :-



$$V_b = \frac{R_2}{R_1+R_2} V_o \quad \text{—(1)}$$

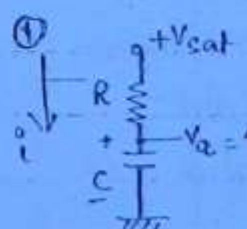
At $t=0$,

$V_o = +V_{sat}$ (by noise).

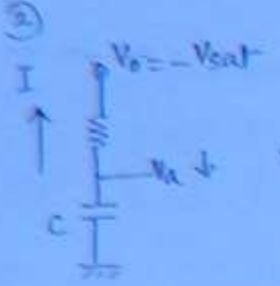
$$V_b = \frac{R_2 V_{sat}}{R_1+R_2} = V_T$$

$\therefore V_b > V_a \Rightarrow V_o = +V_{sat}$ ⇐ but $V_a = V_c = 0$

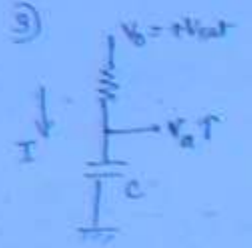
(1)



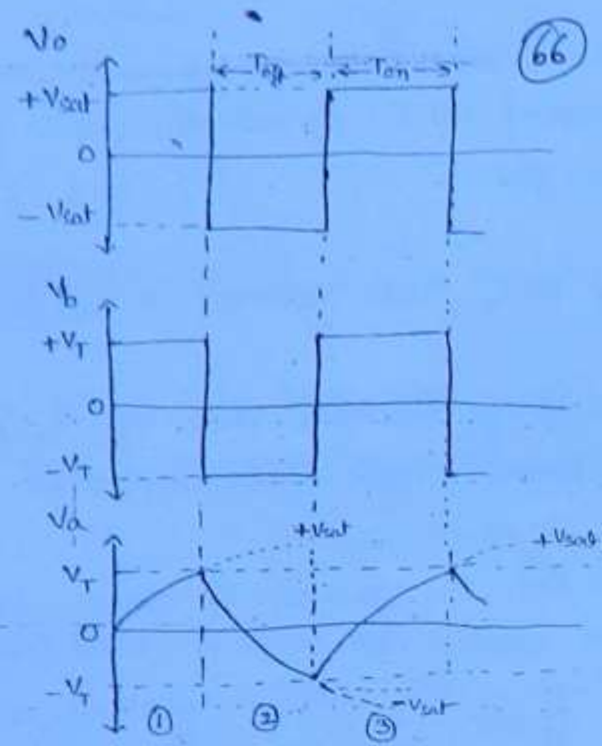
⇒ capacitor will start charging and the voltage of terminal V_a will start increasing. As soon as V_a reaches V_T, V_o will switch to $-V_{sat}$.

②


→ capacitor will start discharging or start charging towards $-V_{sat}$

③


→ capacitor will again start charging towards $+V_{sat}$.



→ V_o → square wave

V_b → attenuated square wave.

V_a → approximate triangular wave.

→ Swing of V_o = $-V_{sat}$ to $+V_{sat}$

" " V_a & V_b = $-V_T$ to $+V_T$

→ At initial condition, consider $V_o = +V_{sat}$, $V_b = +V_T$ and $V_a = V_c = 0$. Now, capacitor will charge by time constant RC towards $+V_{sat}$. Capacitor will charge upto $+V_T$; at this point $V_a = V_b = +V_T$ and op-amp comes out of saturation.

→ When the capacitor further charges above $+V_T$ then $V_a > V_b$ as a result of which V_o switch over to $-V_{sat}$ and therefore $V_b = -V_T$.

→ Now, capacitor starts discharging from $+V_T$ to $-V_T$ towards $-V_{sat}$ with time constant RC. Thus, when capacitor discharge upto $-V_T$, then $V_a = V_b = -V_T$ and op-amp comes out of saturation. When the capacitor further discharges below $-V_T$, then $V_a < V_b$, as a result of which V_o will switch over to $+V_{sat}$ and again $V_b = +V_T$. and thus, the cycle will repeat.

Derivation of T_{on}:-

capacitor charges from $-V_T$ to V_T in time T_{on}.

$$V_C = V_a = V_f - [V_f - V_i] e^{-t/\tau}$$

$V_i = -V_T$ at $t = 0$, $V_f = +V_{sat}$ at $t = \infty$.

$$\therefore \quad V_C = V_{sat} - [V_{sat} + V_T] e^{-t/RC} \quad \rightarrow \text{charging eq}^n$$

At $t = T_{ON}$ -

$$V_T = V_{sat} - [V_{sat} + V_T] e^{-T_{on}/RC}$$

$$\Rightarrow \boxed{T_{on} = RC \ln \frac{V_{sat} + V_T}{V_{sat} - V_T}}$$

Derivation of T_{off}:-

capacitor discharges from V_T to $-V_T$ in time T_{off}.

$V_i = V_T$ at $t = 0$, $V_f = -V_{sat}$ at $t = \infty$.

$$\therefore \quad V_c = -V_{sat} - [-V_{sat} - V_T] e^{-t/RC}$$

$$\Rightarrow V_c = -V_{sat} + [V_{sat} + V_T] e^{-t/RC} \quad \longrightarrow \text{Discharging eq}^n$$

At $t = T_{off}$, $V_c = -V_T$.

$$\therefore -V_T = -V_{sat} + [V_{sat} + V_T] e^{-T_{off}/RC}$$

$$\Rightarrow \boxed{T_{off} = RC \ln \frac{V_{sat} + V_T}{V_{sat} - V_T}} \Rightarrow \because T_{OFF} = T_{ON}$$

$\Rightarrow$ Duty cycle = 50%.

$\Rightarrow$ Square wave Generator.

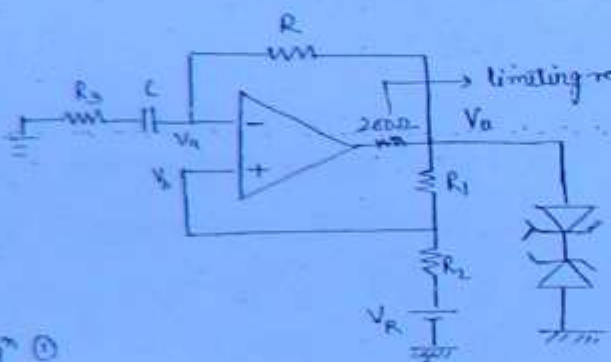
→ Astable multivibrator does not has any stable states due to continuous charging & discharging of C.

→ Time period, $\boxed{T = 2RC \ln \frac{V_{sat}+V_T}{V_{sat}-V_T}}$ — [Eqn ①]

$\because V_T = \frac{R_2}{R_1+R_2} V_{sat} \Rightarrow \boxed{T = 2RC \ln\left[1+\frac{2R_2}{R_1}\right]}$ imp

→ $\boxed{f = \frac{1}{T}}$ → frequency of symmetrical square wave generated.

*



→ New time constant for charging/discharging of C —
$\tau = (R+R_3)\cdot C$.

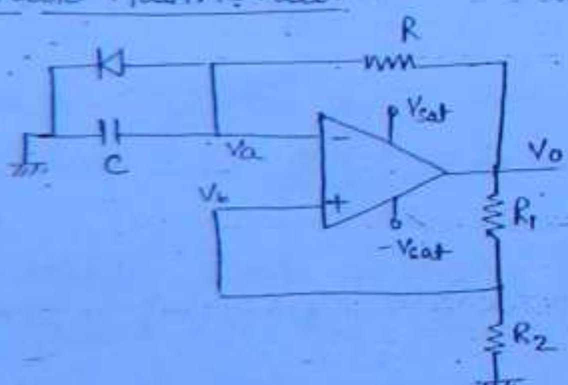
→ Duty cycle can be altered by V_R.

$V_o =$ → $\pm V_{sat}$ can be altered using limiting diodes; i.e. final voltage states of charging & discharging of C can be changed.

eqn ①

* Time period / charging of C is non linear relation, to make it linear, we can use a current mirror circuit in place of 'R'.

Monostable Multivibrator



$\underline{t<0.}$ → ckt is in stable state.

Let $V_o = +V_{sat} \Rightarrow$ Diode → ON

$\Rightarrow V_a = V_c = 0$.

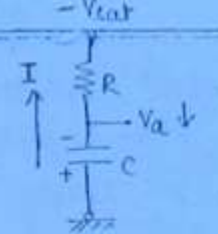
$V_b = \frac{R_2}{R_1+R_2} \cdot V_{sat} = +V_T >> V_a = 0$

$\Rightarrow \therefore V_o = +V_{sat}$.

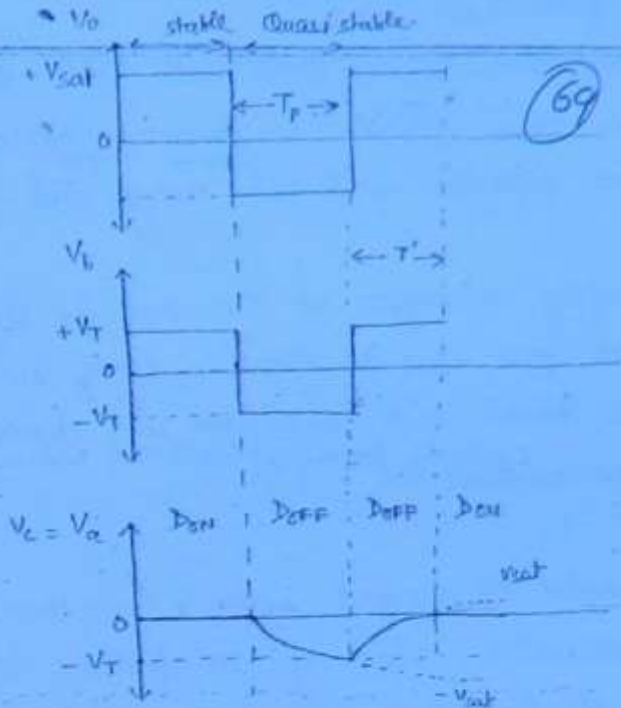
→ At $t=0$, $\sqcap$ at b is given. so that $V_b < V_a$

$\Rightarrow V_o = -V_{sat}$ and Diode = OFF

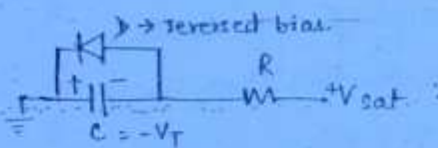
At $t=0$,



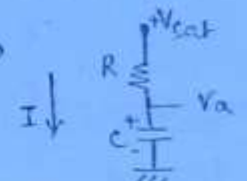
$\Rightarrow$ Hence capacitor will charge towards $-V_{sat}$



Once, V_C reaches $-V_T$, V_O will switch to $+V_{sat}$ but capacitor does not allow sudden change of voltage. and it will start charging towards $+V_{sat}$, since Diode will be 'off.'



$\Rightarrow$



$\Rightarrow$ Now, as soon as V_c reaches ~~V_{off}~~ 0, then D will be ON and ~~it will start~~ C will stop charging.

22nd August, 2012 :-

Derivation of T_p – (Pulse width) -

C discharges from 0 to $-V_T$.

$$V_c = V_a = -V_{sat} - [-V_{sat} - 0]e^{-t/RC}$$

$$\Rightarrow V_c = V_{sat}[-1 + e^{-t/RC}]$$

At $t = T_p$, $V_c = -V_T$

$$\Rightarrow -V_T = -V_{sat}[1 - e^{-t/RC}]$$

$$\Rightarrow \boxed{T_p = RC \ln \frac{V_{sat}}{V_{sat} - V_T}}$$

$$\Rightarrow \boxed{T_p = RC \ln \left[1 + \frac{R_2}{R_1}\right]} \ **$$

$\Rightarrow$ when $R_2 = R_1$,

then $\boxed{T_p = RC \ln 2 = 0.63 RC}$

Exp^n for T' :-

$$T' = RC \ln \frac{V_{sat} + V_T}{V_{sat}}$$

when $R_1 = R_2$,

$$T' = RC \ln(3/2).$$

Circuit Operation

- For $t<0$, circuit is in stable state with $V_0 = +V_{sat}$, $V_b = +V_T$, $V_c = V_a = 0$.
- Since $V_0 = +V_{sat}$, diode is forward biased & short ckt the capacitor, therefore capacitor will not charge and ckt will remain in stable state.

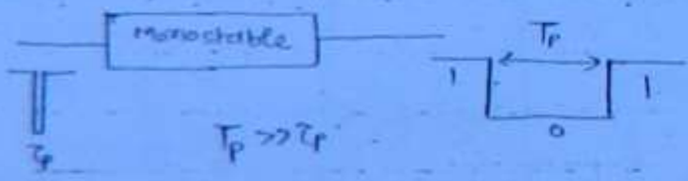
- Now we apply -ve trigger at $t=0$ and for short interval, $V_b < V_a$ and V_0 will switch from $+V_{sat}$ to $-V_{sat}$ and V_b switch from $+V_T$ to $-V_T$. Now diode is reverse biased and capacitor will discharge below 0 towards $-V_{sat}$ with a time constant RC.

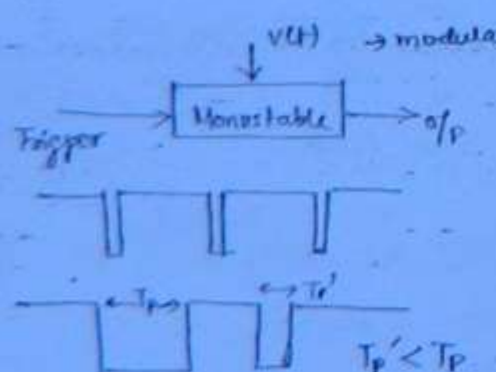
- When capacitor is discharged upto $-V_T$, then $V_a = V_b = -V_T$ and op-amp comes out of saturation, when capacitor further discharges below $-V_T$, then $V_a < V_b$ as a result of which V_0 switch over to $+V_{sat}$ and again $V_b = +V_T$.

- Now the capacitor will charge above $-V_T$ towards $+V_{sat}$ but capacitor can charge only upto 0 because when capacitor charge above 0, diode becomes forward biased and sc the capacitor.

Application :-

- It is used as Pulse stretcher circuit.

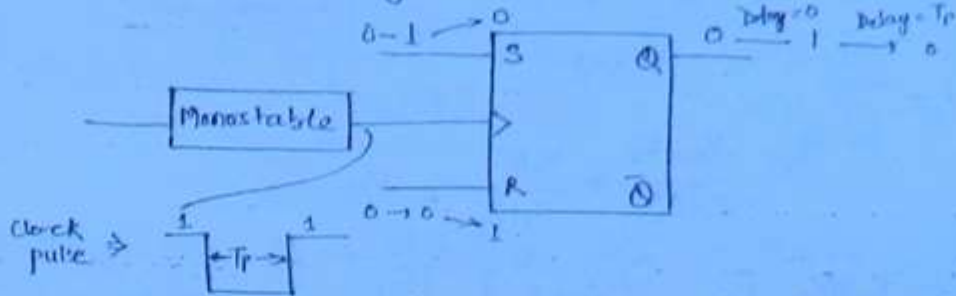
→ 

→ 

} Pulse Width Modulation.

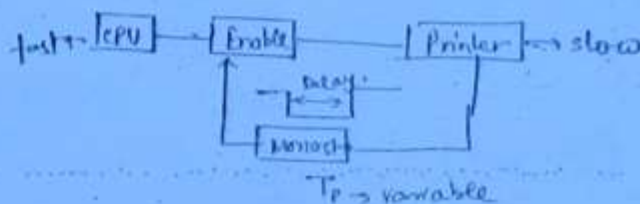
Varactor diode
$V^{-1/2} \propto C$
$V^{-1/2} \propto C$ } $V\uparrow \Rightarrow C\downarrow \Rightarrow T_P\downarrow$

→ It is used as a delay element.



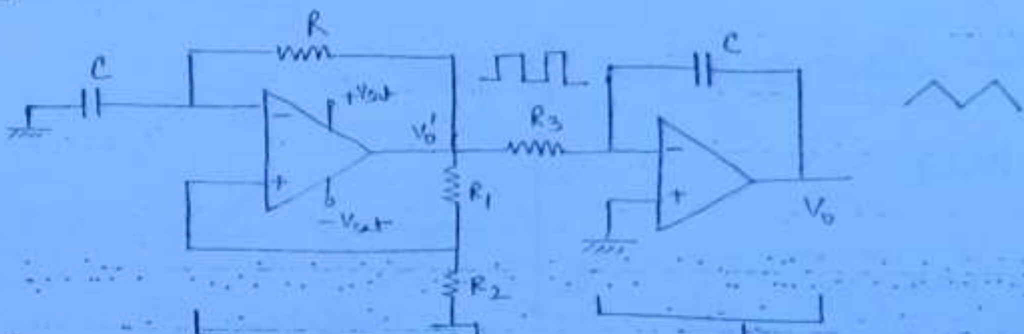
↳ Delay (reqd. for synchro. b/w fast & slow peripheral devices)

Eg



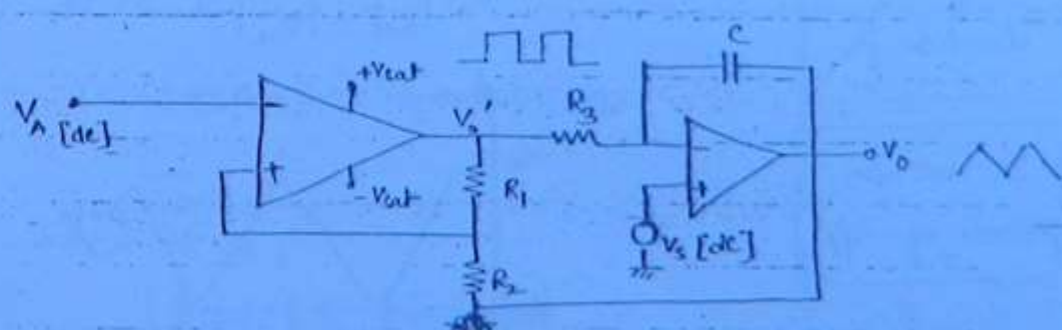
Triangular Wave Generator :-

Figure I



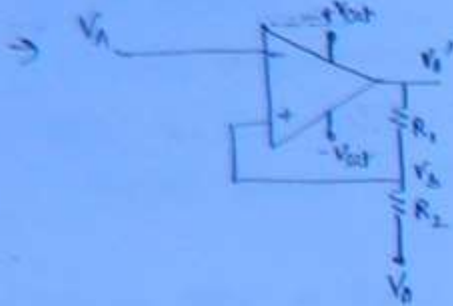
Square wave generator   Integrator (inverting).

Figure II



→ Figure 2 is better than fig. 1 due to less no. of components.

Variation of V_A :-



$$V_b = \frac{V_o' R_2}{R_1+R_2} + \frac{V_o R_1}{R_1+R_2}$$

(1) – $V_o' = +V_{sat}$

$$\Rightarrow V_b = \frac{V_{sat} R_2}{R_1+R_2} + \frac{V_o R_1}{R_1+R_2} = V_A$$

$$\Rightarrow V_o = \frac{R_1+R_2}{R_1}\left[V_A - \frac{V_{sat} R_2}{R_1+R_2}\right] = \text{lower amplitude of } \triangle \text{ wave.}$$

(2) – when $V_o' = -V_{sat}$

$$\Rightarrow V_{b_2} = \frac{-V_{sat} R_2}{R_1+R_2} + \frac{V_o R_1}{R_1+R_2} = V_A$$

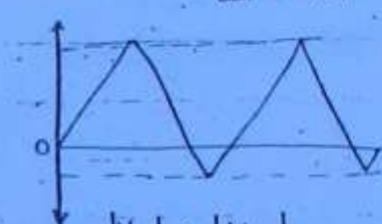
$$\Rightarrow V_o = \frac{R_1+R_2}{R_1}\left[V_A + \frac{V_{sat} R_2}{R_1+R_2}\right] = \text{upper amplitude of } \triangle \text{ wave.}$$

Case I – when $V_A = 0$, $V_{OU} = \frac{R_2}{R_1} V_{sat}$, $V_{OL} = \frac{-R_2}{R_1} \cdot V_{sat}$

$$|V_{OU}| = |V_{OL}|$$

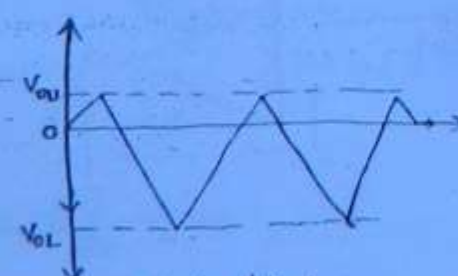
$|V_{OL}| = |V_{OU}|$

Case II – when $V_A \uparrow$, waveform will move in upward direction.



$|V_{OU}| > |V_{OL}|$

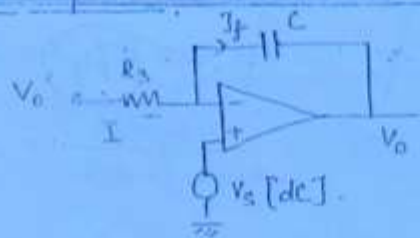
Case III when $V_A \downarrow$, wave form will move in downward direction –



$|V_{OL}| > |V_{OU}|$

$\boxed{\text{Hence, by changing } V_A \text{, we can control the amplitude of o/p.}}$

Variation of V_s



(73)

$V_p = V_n = V_s$.

$I_f = I$

$$C\frac{d}{dt}(V_s - V_o) = \frac{V_o' - V_s}{R_3}$$

$\rightarrow$ Since V_s = dc $\Rightarrow \frac{dV_s}{dt} = 0 \Rightarrow -C\frac{dV_o}{dt} = \frac{V_o' - V_s}{R_3}$

$$\Rightarrow \frac{dV_o}{dt} = \frac{-[V_o' - V_s]}{R_3C} \quad \text{— (1)}.$$

$\rightarrow$ When $V_o' = +V_{sat}$,

$$\Rightarrow \frac{dV_o}{dt} = \frac{-[V_{sat} - V_s]}{R_3C} \quad \text{— (2)}$$

= -ve slope ($\because V_{sat} > V_s$).

= constant. { $\because V_{sat}, V_s, R_3, C$ = constants

$\Rightarrow$ $V_o \downarrow$ linearly

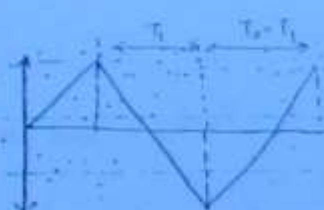
$\rightarrow$ When $V_o' = -V_{sat}$,

$$\frac{dV_o}{dt} = \frac{V_{sat} + V_s}{R_3C} \quad \text{— (3)} \Rightarrow V_o \uparrow \text{ linearly}$$

Case I :- $V_s = 0$; in (2) & (3) -

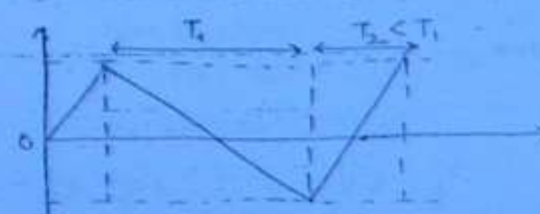
$$\frac{dV_o}{dt} = -\frac{V_{sat}}{R_3C} \quad ; \quad \frac{dV_o}{dt} = \frac{+V_{sat}}{R_3C}$$

$\Rightarrow$ $|\downarrow \text{slope}| = |\uparrow \text{slope}|$



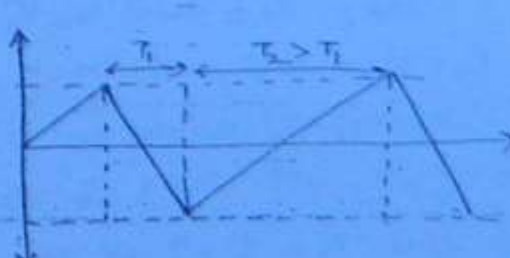
Case II :- When $V_s > 0$,

$|\uparrow \text{slope}| > |\downarrow \text{slope}|$.



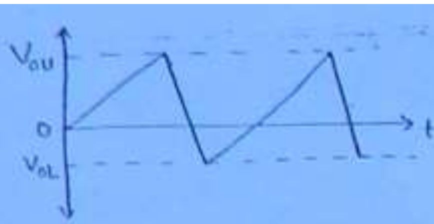
Case III When $V_s < 0$;

$|\uparrow \text{slope}| < |\downarrow \text{slope}|$



Hence by varying V_s, we can change the slope of o/p.

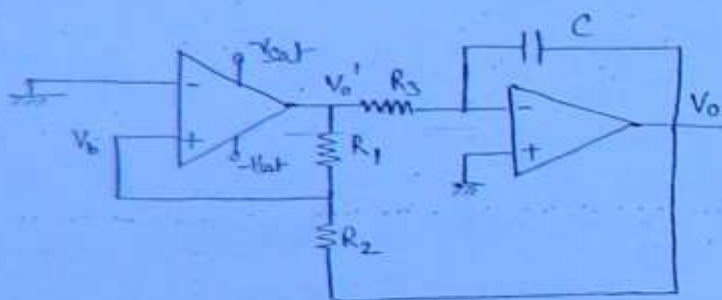
Eg for $V_A = 2V$, $V_S = -2V$.



⇒ ∵ V_A = +ve ⇒ $|V_{OU}| > |V_{OL}|$

V_S = −ve ⇒ |↓ slope| > |↑ slope|

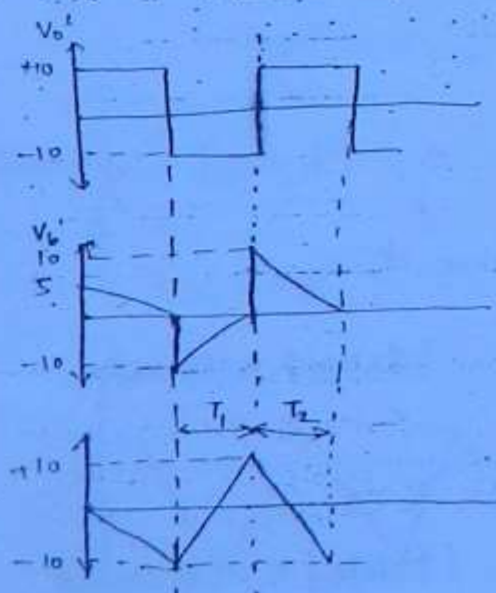
Symmetrical Triangular Wave (with $V_A = 0$ and $V_S = 0$) :-



① If $V_o' = +V_{sat}$, V_o will ↓ with slope $\frac{dV_o}{dt} = \frac{-V_{sat}}{R_3C}$ upto

$$V_{OL} = -\frac{R_2}{R_1}V_{sat}.$$

② When $V_o' = -V_{sat}$, V_o will ↑ with slope $\frac{dV_o}{dt} = \frac{+V_{sat}}{R_3C}$ upto $V_{OU} = \frac{R_2}{R_1}\cdot V_{sat}$.



Eg :- Let $R_1 = R_2$ and $V_{sat} = 10V$.

$$V_b = \frac{R_2}{R_1+R_2}\cdot V_o' + \frac{R_1}{R_1+R_2}\cdot V_o = \frac{V_o'}{2} + \frac{V_o}{2}$$

due to noise.

Let at $t=0$, $V_o' = +V_{sat} = 10V$

$V_o = 0$ {due to C}.

∴ $V_b = 5V > V_a = 0$ ⇒ $V_o' = +V_{sat}$

∵ $V_o' = +V_{sat}$, V_o↓ and in turn V_b↓.

When $V_o = V_{OL} = -10V$, $V_b = \frac{10}{2} - \frac{10}{2} = 0V$.

Now, ∵ $V_b \le V_a$, V_o' switches from $+V_{sat}$ to $-V_{sat}$

$V_b = -\frac{10}{2} - \frac{10}{2} = -10V$. and ∵ $V_o' = -V_{sat}$, ⇒ V_o will ↑ and V_b↑ and when $V_o = V_{OU} = 10V$

then $V_b = -\frac{10}{2} + \frac{10}{2} = 0V$ and ∵ $V_b \ge V_a$; V_o' switches from $-V_{sat}$ to $+V_{sat}$ and cycle will be repeated.

Calculation of T_1 and T_2 :-

$$\text{Time} = \frac{\text{Change}}{\text{Rate of change}} = \frac{V_{final} - V_{initial}}{\text{slope}}$$

$$\Rightarrow \quad T_1 = \frac{V_{OU} - V_{OL}}{dV_0/dt} = \frac{R_2/R_1\, V_{sat} - \left(-\frac{R_2}{R_1}\right) \cdot V_{sat}}{V_{sat}/R_3C} \Rightarrow \boxed{T_1 = \frac{2R_2R_3C}{R_1}}$$

$$T_2 = \frac{V_{OL} - V_{OU}}{dV_0/dt} = \frac{-\left(\frac{R_2}{R_1}\right)V_{sat} - \left(\frac{R_2}{R_1}\right)V_{sat}}{-V_{sat}/R_3C} \Rightarrow \boxed{T_2 = \frac{2R_2R_3C}{R_1}}$$

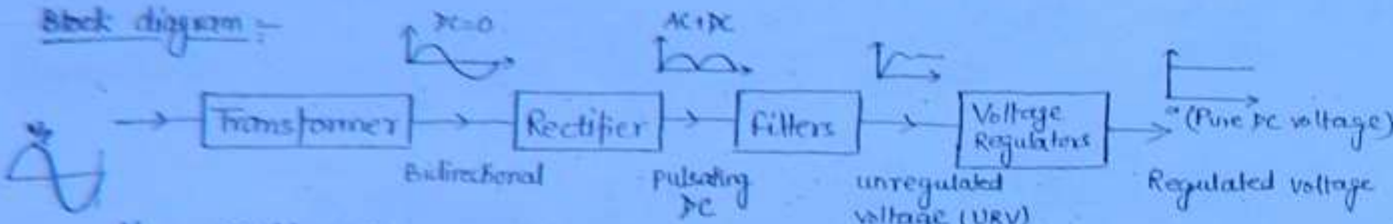
→ $\because T_2 = T_1 \quad \therefore$ V_0 = symmetrical triangular wave.
V_0' = symmetrical square wave.

→ Time period = $T = T_1 + T_2 \Rightarrow \boxed{\frac{4R_2R_3C}{R_1} = T}$ or $\boxed{f = \frac{R_1}{4R_2R_3C}}$ **

Diode Circuit :-

* Rectifiers:-

Block diagram :-



$V_{rms} = 230V$, 50Hz .

$V_P = 230\sqrt{2}$, 50Hz

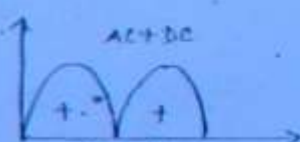
- Basic purpose of a rectifier is to convert a bidirectional voltage or current waveform into unidirectional voltage or current waveforms.

Important terms :-

- Average or DC level ; $I_{dc} = \frac{1}{2\pi}\int_0^{2\pi} I(t)\,d(\omega t)$.

- Rms value , $I_{Rms} = \left[\frac{1}{2\pi}\int_0^{2\pi} I^2(t)\cdot d(\omega t)\right]^{1/2}$.

- Ripple Voltage :-



(Fig 1)

$V = V_{ac} + V_{DC}$

$V_{rms} = \sqrt{V_{dc}^2 + V_{acrms}^2}$

$\Rightarrow V_{acrms} = \sqrt{V_{rms}^2 - V_{dc}^2}$

V_{dc} = dc value of o/p

V_{rms} = RMS value of o/p.

V_{acrms} = RMS value of ac component

Eg let $V_{dc} = 8V$ and $V_{acrms} = 3V \Rightarrow V_{acpk} = 3\sqrt{2}$

$\therefore V = 8 + \underbrace{3\sqrt{2}\sin\omega t}_{\text{Ripple}}$

→ Mathematical representation, fig 1. is actual representation.

(Variation of o/p voltage $\angle$ from pure dc)

(Ripple superimposed on dc.)

- It is the deviation of o/p voltage from its dc value. The waveform after rectification is not pure dc. It has an AC component called Ripple superimposed on dc.

→ <u>Ripple factor</u> :- $r = \frac{\text{rms value of ac component}}{\text{dc value}}$

$$\Rightarrow \boxed{r = \frac{V_{acrms}}{V_{dc}}}$$; <u>ideally</u> $V_{acrms} = 0$ or $\boxed{r = 0}$

$$\Rightarrow r = \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{dc}} \Rightarrow \boxed{r = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}}$$

→ <u>form factor</u> :-

$$F = \frac{V_{rms}}{V_{dc}} \Rightarrow \boxed{r = \sqrt{F^2 - 1}}$$

- $\boxed{\text{Ideally}, \ F = 1}$

→ <u>Crest factor</u> :- $C = \frac{\text{Peak value}}{\text{RMS value}}$

- It should be as low as possible

<u>Eg.</u>

⇒ RMS is same for both then (ii) signal should be preferred since peak is ↓ and circuit elements will have to be designed accordingly.

→ <u>Peak Inverse Voltage (PIV)</u>.

- It is the max voltage across the diode in reverse direction, ie., when the diode is reverse biased.
- Diode is selected on the basis of PIV rating.
- PIV should be as low as possible.
- We can ↑ PIV of ckt by cascading two or more diodes in series.

Rectifier Efficiency :- $\eta = \frac{\text{o/p dc power}}{\text{i/p ac power}} \times 100\%$.

Transformer Utilization factor (TUF) :-

- It indicates how much is the utilization of transformer in the circuit.
- It should be as ↑ as possible.

Types of Rectifiers.

1) Half wave Rectifier
2) Full wave rectifier — (a) Center tapped transformer type
(b) Bridge Rectifier.

Workbook

Chap. 10.

1) $(A_v)_{dB} = 20 \log A_v = 80$
$\Rightarrow A_v = 10^4$.
$G \cdot BW = A_v \times BW = 20 \times 10^4 = 200 kHz$.

Alternate
Find the point where 20dB/dec is intersecting freq. axis.

3) $V_n = V_p = 2V$
$\therefore I_E = \frac{10-2}{1K} = 8mA$
I_B = negligible
$\Rightarrow I_E = I_C = 8mA$
$\rightarrow$ 3.(a).

2) $\because \frac{10K}{1K} = \frac{10K}{1K} \Rightarrow CMRR = \infty \Rightarrow A_c = 0$
$\Rightarrow V_o = A_d(V_1 - V_2)$
$\Rightarrow V_o = 0$.

4) $V_o = \left(1 + \frac{4.14}{10}\right) \cdot V_p = \sqrt{2} \cdot V_p$; $V_p = \left(\frac{1/cs}{R + 1/cs}\right) \sin t = \left(\frac{1}{1+j}\right) \sin t$

$\Rightarrow V_o = \frac{\sqrt{2} \sin(t)}{(1+j)} \Rightarrow V_o = \sin(t - \pi/4)$.

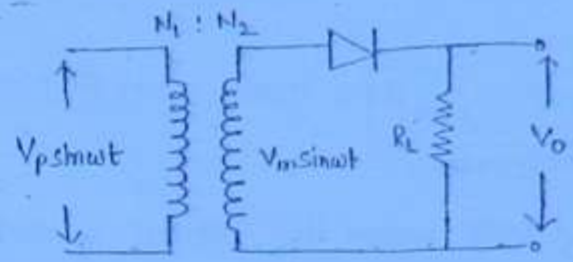
5) (c).

6) $V_o = \left(1 + \frac{2R}{R}\right)\left[\frac{\sin(100t) + 2 - 2}{2}\right] = \frac{3}{2} \cdot \sin(100t)$

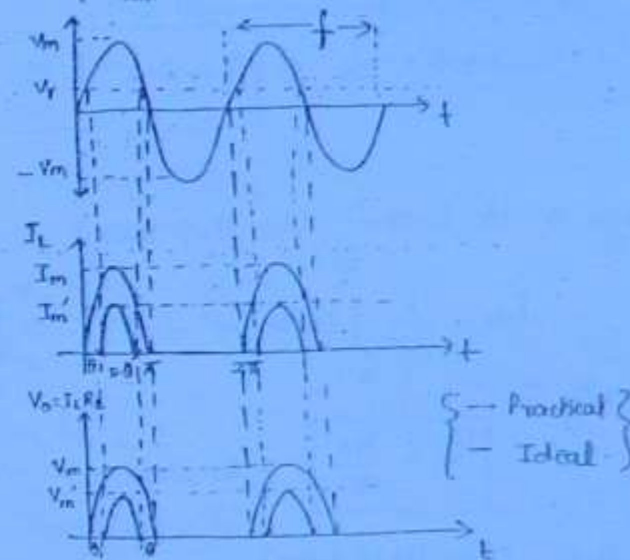
10) $CMRR = \frac{A_d}{A_c}$, $\%\text{ error} = \frac{A_c V_c}{A_d V_d} \times 100 = \frac{1}{1000} \times \frac{10}{1} \times 100 = 1\%$.

23/08/2012

Half-Wave Rectifier :-



$$\frac{V_p}{V_m} = \frac{N_1}{N_2}$$



Assuming ideal circuit,

① $V_i \geq 0$, $D \to FB \to$ short ckt.

② $V_i < 0$, $D \to RB \to$ Open ckt

→ When $D \to ON$ — $I_L = \dfrac{V_m \sin\omega t}{R_L}$

→ $I_m = \dfrac{V_m}{R_L}$ = max. or peak current through R_L

→ $V_o = I_L R_L = V_m \sin\omega t$ (ideal case).

→ When $D \to OFF$, $I_L = 0 \Rightarrow V_o = 0$

→ The o/p frequency or ripple frequency $= f_r =$ supply frequency f

→ Conduction angle $\phi = \pi$ or 180°.

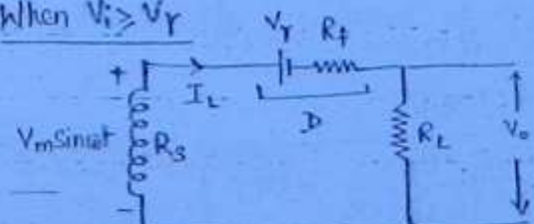
- Practical circuit — ① $V_i < V_\gamma$, $D \to OFF \to RB$

② $V_i \geq V_\gamma$, $D \to ON \to FB$

$V = 0.7$ or $V = V_\gamma + I R_f$

$R_f = \dfrac{V_1 - V_2}{I_1 - I_2}$ = very low.

When $V_i \geq V_\gamma$



* $V_D = V_\gamma + I R_f \approx 0.7V$ for Si

R_s = Resistance of secondary coil

$$\boxed{I_L = \frac{V_m \sin\omega t - V_\gamma}{R_s + R_f + R_L}}$$

$$\boxed{I_m' = \text{max. current} = \frac{V_m - V_\gamma}{R_s + R_f + R_L} < I_m \text{ (ideal)}}$$

When $V_i < V_\gamma$ — D → off ⇒ $I_L = 0$

→ When D = ON, $V_m' = I_m' \cdot R_L$

→ Ripple frequency will remain same as ideal case.

→ Conduction angle $\boxed{\phi = \pi - 2\theta}$ {< 180°} **

$V_m \sin\theta = V_\gamma \Rightarrow \boxed{\theta = \sin^{-1}\left(\frac{V_\gamma}{V_m}\right)}$ **

— Average or dc level — (For Half wave)

$$I_{dc} = \frac{1}{2\pi}\int_0^{\pi} I_m \sin\omega t \; d(\omega t). \Rightarrow \boxed{I_{dc} = \frac{I_m}{\pi}} \quad \text{— for Ideal}$$

Similarly,

$$\boxed{V_{dc} = \frac{V_m}{\pi}} \quad \text{— for Ideal}$$

— RMS value — (For Half wave).

$$\boxed{I_{rms} = \frac{I_m}{2}}, \quad \boxed{V_{rms} = \frac{V_m}{2}}$$

— Form factor $= \frac{V_{rms}}{V_{dc}} \Rightarrow \boxed{F = 1.57}$ **

— Ripple factor $= \frac{V_{ac\,rms}}{V_{dc}} = \sqrt{F^2 - 1} \Rightarrow \boxed{\gamma = 1.21}$ **

— Crest factor $= \frac{V_{peak}}{V_{rms}} \Rightarrow \boxed{C = 2}$ **

— $\boxed{PIV = +V_m}$ (Drop across $R_L = 0$, $\because I_L = 0$).

— Rectifier Efficiency, $\eta = \frac{\text{o/p dc power}}{\text{i/p ac power}} \times 100\%$

$\Rightarrow \eta = \frac{I_{dc}^2 \cdot R_L}{I_{rms}^2 (R_L + R_s + R_f)} \times 100\%$

$\Rightarrow \boxed{\eta = \frac{4}{\pi^2} \cdot \frac{R_L}{R_L + R_f + R_s} \times 100\%}$

$$\Rightarrow \eta = 0.406 \times \frac{1}{\frac{R_s+R_f}{R_L}+1} \times 100\%$$

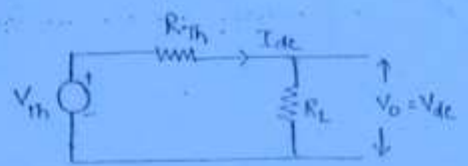
81

{ $\eta = 40\%$ means only 40% ac power is converted to dc

If $R_L >>> R_f + R_s$, then $\boxed{\eta_{max} = 40.6\%}$

→ If the efficiency is 40%, it means that 40% of ac power is converted into dc and remaining 60% (approx) power is in form of ripple (ac component at o/p).

Thevenin's equivalent of Half Wave Rectifier



$$I_{dc} = \frac{V_{Th}}{R_{Th}+R_L} \quad —(1)$$

$$V_{dc} = I_{dc} \times R_L$$

$$I_{dc} = \frac{1}{2\pi}\int_{\theta}^{\pi-\theta} I_L \, d\omega t \; ; \; \theta = \sin^{-1}\left(\frac{V_\gamma}{V_m}\right) \; ; \; I_L = \frac{V_m \sin\omega t - V_\gamma}{R_s + R_f + R_L}$$

Let $V_\gamma = 0$, $\Rightarrow \theta = 0$; $I_L = \frac{V_m \sin\omega t}{R_s+R_f+R_L} = I_m' \sin\omega t$.

$$\therefore I_{dc} = \frac{1}{2\pi}\int_0^{\pi} I_m' \sin\omega t \, d\omega t = \frac{I_m'}{\pi} = \frac{V_m}{\pi(R_s+R_f+R_L)} \quad —(2)$$

Comparing (1) and (2) :-

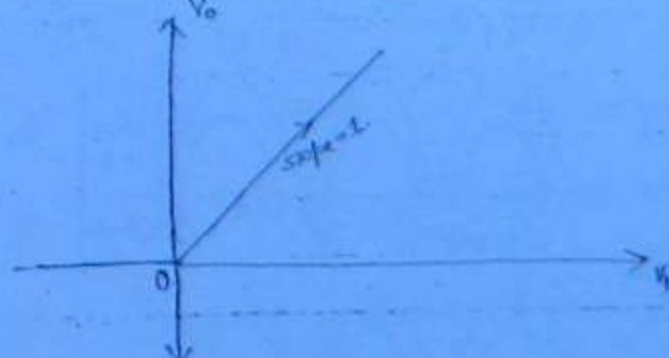
$$\boxed{V_{Th} = \frac{V_m}{\pi} \; , \; R_{Th} = R_s + R_f}$$

* R_{Th} is the o/p resistance of ckt & it represents the losses occurring at o/p.

Transfer Curve:-

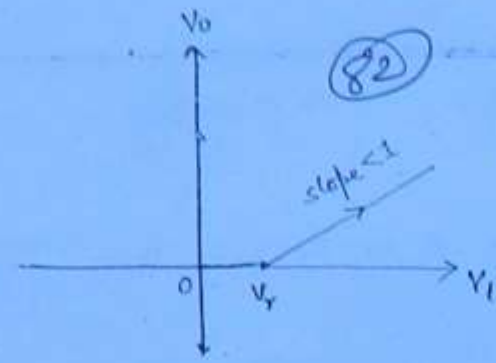
Ideal :

V_i	D	V_o
$V_i \le 0$	off	0
$V_i \ge 0$	ON	V_i



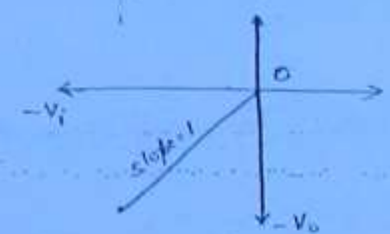
Practically:

V_i	D	V_o
$V_i \le V_\gamma$	OFF	0
$V_i \ge V_\gamma$	ON	$I_L R_L = \frac{(V_i - V_\gamma)}{R_s + R_L + R_f} \times R_L$



$$\text{slope} = \frac{R_L}{R_s + R_L + R_f} < 1$$

* If diode polarity is reversed, then charac. will come into III quadrant



→ Transfer Utilization factor –

$$\boxed{TUF = 0.286} \rightarrow \text{(very low)}$$

Que: A HWR is supplied by a 230V, 50Hz supply with a step down ratio of 3:1 to a resistive load $R_L = 10K\Omega$. If $R_f = 75\Omega$ and $R_s = 10\Omega$,

Calculate –

① Max, average and rms value of current

② DC value of o/p voltage

③ Efficiency.

Solⁿ $V_{rms} = \frac{230}{3} V \Rightarrow V_m = \frac{230\sqrt{2}}{3} V. = 108.4V$

$\therefore I_m = \frac{V_m - \overset{=0 \{\because \text{ not mentioned}\}}{V_\gamma}}{R_f + R_L + R_s} \approx \frac{230\sqrt{2}}{3(10K)} = \frac{23\sqrt{2}}{3} mA. = 10.84 mA$

$I_{dc} = I_{avg} = \frac{I_m}{\pi} = \frac{23\sqrt{2}}{3\pi}. mA = 3.45 mA$

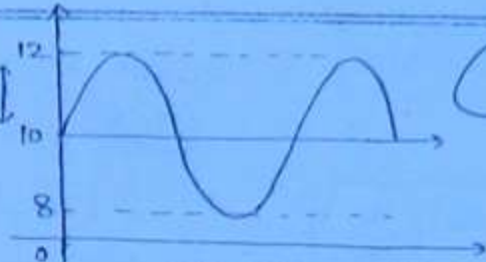
$\cancel{I_{rms}} = \cancel{\frac{230}{3 \times 10K}} \times \cancel{\frac{23}{3}} \cancel{mA} = \cancel{7.66 mA}$

$V_{dc} = I_{dc} \times R_L = \frac{23}{3\pi}\sqrt{2} \times 10 V = 34.5V$

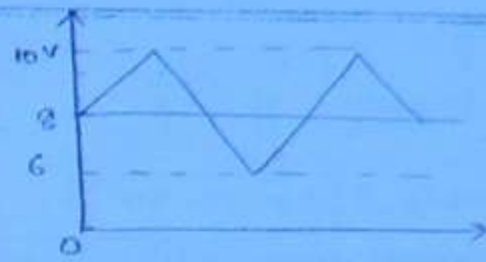
$\eta = \frac{0.406 \times 10K}{10K + 85} \approx 40.6\%$

$I_{rms} = \frac{I_m}{2} = 5.42 mA.$

Ques :- (1)



(2)



Calculate ripple factor r

(1) $F = \dfrac{V_{rms}}{V_{dc}} = \dfrac{\sqrt{10^2 + (2/\sqrt{2})^2}}{10} = \dfrac{\sqrt{102}}{10}$

$\therefore r = \sqrt{F^2 - 1} = \dfrac{1}{5\sqrt{2}}$

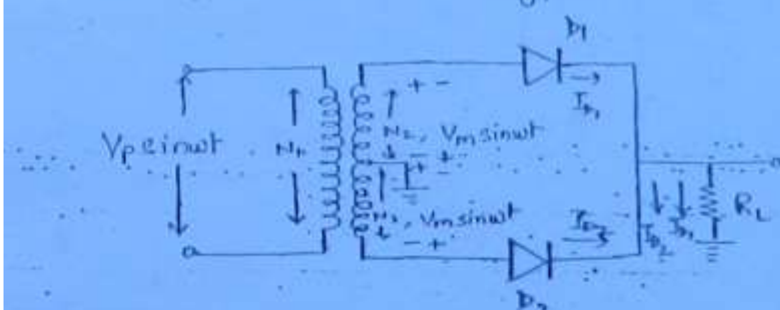
OR $r = \dfrac{V_{ac\,rms}}{V_{dc}} = \dfrac{(2/\sqrt{2})}{10}$

$r = \dfrac{1}{5\sqrt{2}}$

(2) $r = \dfrac{V_{ac\,rms}}{V_{dc}} = \dfrac{(2/\sqrt{3})}{8} = \dfrac{1}{4\sqrt{3}}$

Full Wave Rectifier :-

a) Center Tapped Transformer Type :-



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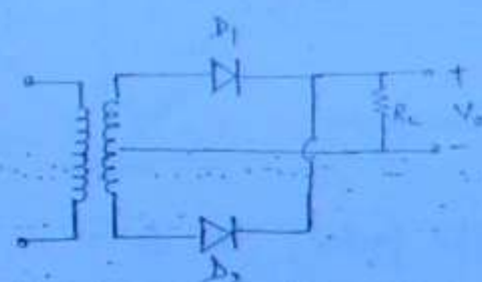


$\dfrac{V_p}{V_m} = \dfrac{N_1}{N_2}$

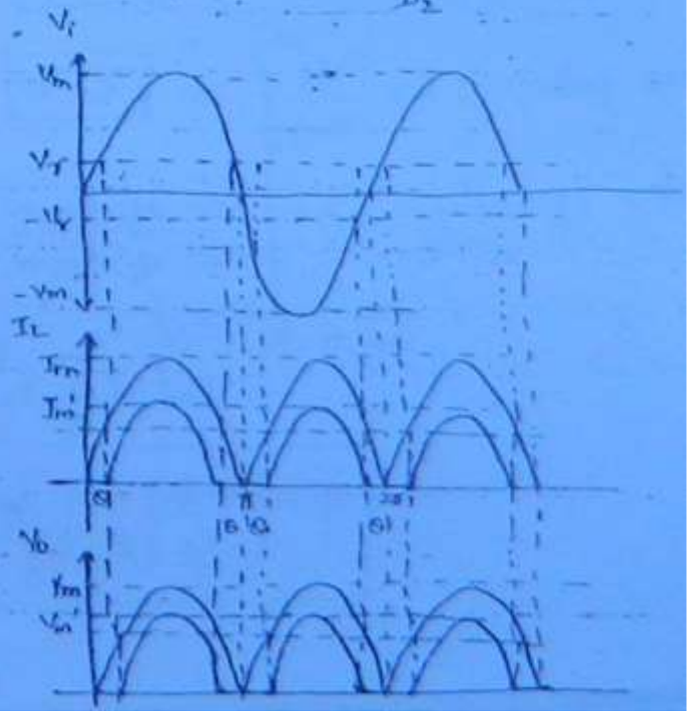
Ideally: $I_L = \dfrac{V_m \sin\omega t}{R_L} = I_m \sin\omega t$; $I_m = \dfrac{V_m}{R_L}$

$V_o = I_L R_L = V_m \sin\omega t$

→ Ripple frequency = $\boxed{f_r = 2f}$ **

→ conduction Angle = $\boxed{\phi = 2\pi}$ **

for individual diode ; $\boxed{\phi = \pi}$ **



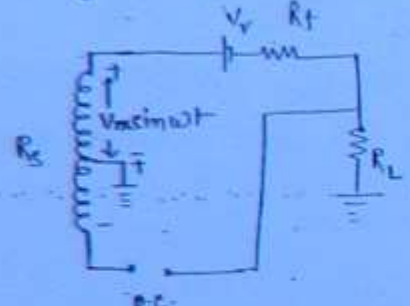
Practically:

→ Ripple frequency, $f_r = 2f$

→ for circuit, $\boxed{\phi = 2\pi - 4\theta}$; $\boxed{\theta = \sin^{-1}\left(\frac{V_r}{V_m}\right)}$

for individual diode, $\boxed{\phi = \pi - 2\theta}$

→ During +ve cycle –



$$\boxed{I_L = \frac{V_m \sin\omega t - V_r}{R_f + R_L + \frac{R_s}{2}}}^{**\text{Imp.}} \; ; \; \boxed{I_m' = \frac{V_m - V_r}{R_f + R_L + \frac{R_s}{2}}}^{**} (< I_m)$$

$$V_o = V_L \cdot I_L$$

→ $I_{dc} = \frac{1}{\pi}\int_0^{\pi} I_m \sin\omega t \cdot d\omega t \Rightarrow \boxed{I_{dc} = \frac{2I_m}{\pi}}^{**}$, $\boxed{V_{dc} = \frac{2V_m}{\pi}}^{**}$

→ $\boxed{I_{rms} = \frac{I_m}{\sqrt{2}}}^{**}$; $\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}^{**}$

→ form factor, $F = \frac{V_m/\sqrt{2}}{2V_m/\pi} \Rightarrow \boxed{F = 1.11}^{**}$

→ Ripple factor, $r = \sqrt{F^2 - 1} \Rightarrow \boxed{r = 0.48}^{**}$

→ Crest factor, $C = \frac{V_m}{V_m/\sqrt{2}} \Rightarrow \boxed{C = \sqrt{2}}^{**}$

→ Rectifier efficiency, $\eta = \frac{\text{dc o/p power}}{\text{ac i/p power}} \times 100\%$

$$\Rightarrow \eta = \frac{I_{dc}^2 \cdot R_L}{I_{rms}^2\left(\frac{R_s}{2} + R_f + R_L\right)} \times 100\%$$

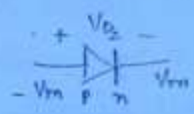
$$\Rightarrow \boxed{\eta = \left(\frac{0.812 \times R_L}{\frac{R_s}{2} + R_f + R_L}\right) \times 100\%}$$

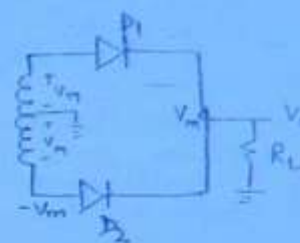
$$\Rightarrow \eta = \frac{0.812 \times 100\%}{\left(1 + \frac{R_f}{R_L} + \frac{R_s}{2R_L}\right)}$$

If $R_L >> R_f + R_s/2$

$$\Rightarrow \boxed{\eta_{max} = 81.2\%}$$

→ Peak Inverse voltage ⇒ $\boxed{PIV = 2V_m}$ 88





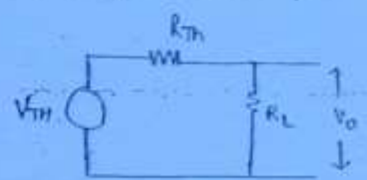
$$V_{D_2} = V_P - V_n = -V_m - V_m$$

$$\Rightarrow V_{D_2} = -2V_m$$

; $\begin{cases} \text{when } V_D \geq 0 & D \to FB \\ V_D \leq 0 & D \to RB \end{cases}$

$$\Rightarrow \boxed{PIV = 2V_m}$$

Thevenin's Equivalent :- of FWR :-

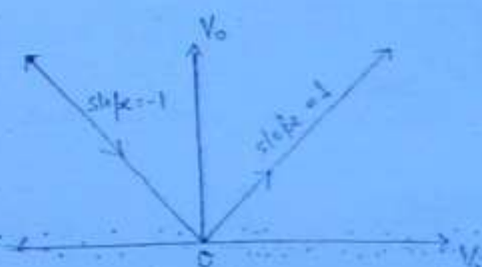


$$\boxed{R_{Th} = \frac{R_s}{2} + R_f \qquad V_{TH} = \frac{2V_m}{\pi}}$$ **

Transfer curve :-

Ideally :

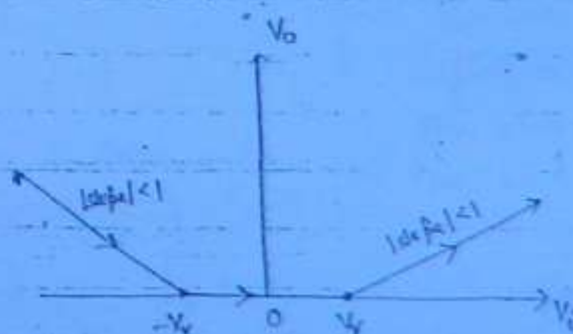
V_i	D_1	D_2	V_o
$V_i < 0$	off	on	$-V_i$
$V_i > 0$	on	off	V_i



$$\therefore V_o = |V_i|$$

Practically :-

V_i	D_1	D_2	V_o
$V_i \leq -V_\gamma$	off	ON	V_o'
$-V_\gamma \leq V_i \leq V_\gamma$	off	off	0
$V_i > V_\gamma$	on	off	V_o'



$$V_o' = I_L R_L = \frac{V_i - V_\gamma}{\frac{R_s}{2} + R_f + R_L} \times R_L$$

$$\text{slope} = \frac{R_L}{\frac{R_s}{2} + R_f + R_L} \; (< 1) \quad \Rightarrow \boxed{|\text{slope}| < 1}$$ **

→ If the polarity of diodes is reversed, then transfer curve will be present in III and IV quadrant.

→ In practical condition, it is not possible to rectify very small signals using centre tapped Transfer rectifier.

for eg. $V_i = 5\sin\omega t$ mV ⇒ $V_m = 5mV = 0.005V << V_\gamma$, hence o/p will be 0.

→ TUF – $\boxed{TUF = 0.693}$

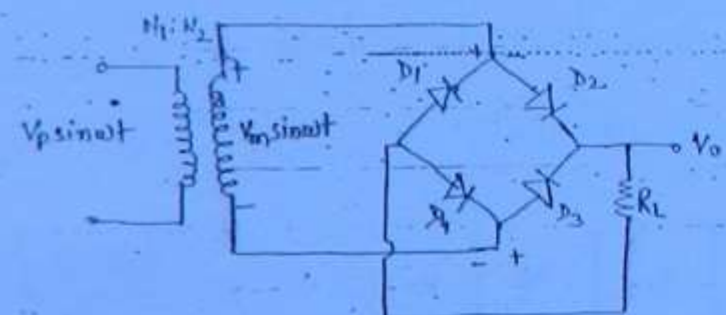
→ Workbook

Pg 57 (chap-10).

(12) c

24th August, 2012

Bridge Rectifier :-



$$\frac{V_p}{V_m} = \frac{N_1}{N_2}$$

for positive half –

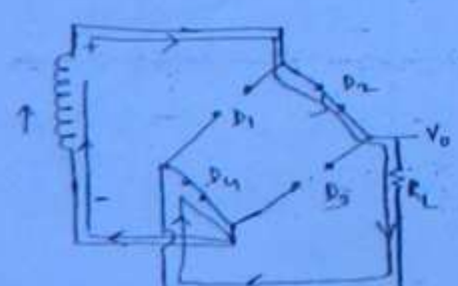
D_1 & D_3 off.

D_2 & D_4 ON

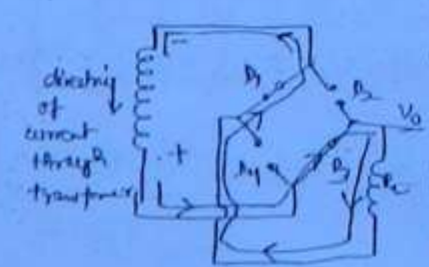
for –ve half –

D_1 & D_3 ON

D_2 & D_4 off.



+ve cycle



–ve cycle

- The current through transformer coil is bidirectional, hence avg. dc component is zero, which in turn results in minimum loss in X^{mer}.
- TUF is maximum for Bridge rectifier due to above mentioned reason.
- zero dc prevents the Eddy current, hysteresis losses and saturation of X^{mer}.

* **Ideally**

→ $V_{dc} = \frac{2V_m}{\pi}$; $I_{dc} = \frac{2I_m}{\pi}$

→ $I_{rms} = \frac{I_m}{\sqrt{2}}$; $V_{rms} = \frac{V_m}{\sqrt{2}}$

→ $r = 0.48$

→ $F = 1.11$

→ $C = \sqrt{2}$

→ $\phi = 2\pi$

→ Individual diode, $\phi = \pi$

Practically.

→ $I_L = \frac{V_m \sin\omega t - 2V_\gamma}{R_s + 2R_f + R_L}$

→ $I_m' = \frac{V_m - 2V_\gamma}{R_s + 2R_f + R_L}$

→ $\boxed{\eta = 0.812 \times \frac{1}{\frac{R_s + 2R_f}{R_L} + 1} \times 100\%}$

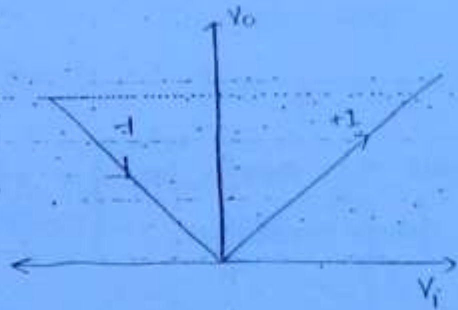
→ $\boxed{\eta_{max} = 81.2\%}$

→ $\boxed{\phi = 2\pi - 4\theta}$; $\boxed{\theta = \sin^{-1}\frac{2V_\gamma}{V_m}}$

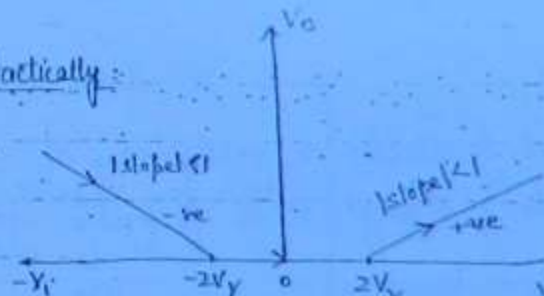
→ Individual diode, $\phi = \pi - 2\theta$.

Transfer Curve

Ideally :

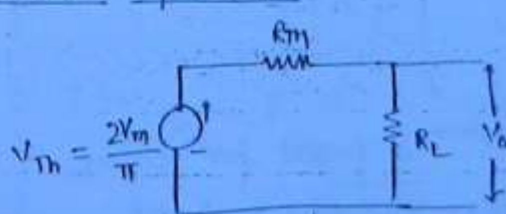


Practically :



Slope: $\frac{R_L}{R_s + 2R_f + R_L}$ (<1)

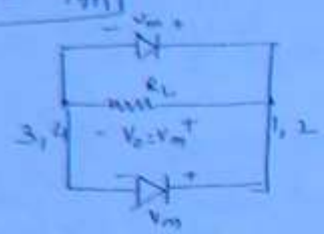
Thevenin's Equivalent :

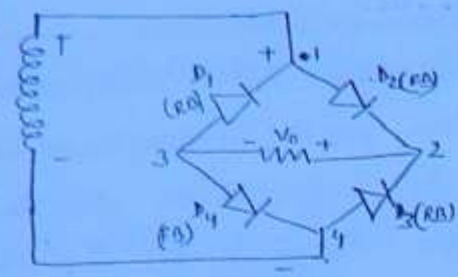


$R_{TH} = R_s + 2R_f$

(88)

→ $\boxed{PIV = V_m}$





→ $\boxed{TUF = 0.812}$

Advantages of Bridge Rectifier

- TUF is highest.
→ Transformer can be replaced by ac source if step up/down of voltage is not required.
→ PIV is smaller as compared to centre tap.
→ Voltage required to deliver same power is smaller w.r.t half wave rectifier, hence, to do so, no. of turns is more in HWR, hence the size of transformer used in Bridge rectifier is smallest.

Disadvantage -
- It cannot be used for rectification of small signals as cutoff voltage req. for response is $2V_\gamma$., though it is preferable for high power ratings.

V_m	$2V_\gamma$	loss
2	1	50%
10V	1	10%
20V	1	5%

By Sir :- Advantages :-
(i) The current in both primary & secondary of X^{mer} is present for entire cycle and hence for a given power o/p, power X^{mer} of a small size and less cost may be used.

→ No centre-tap is required in x^{mer} secondary, hence wherever possible, ac voltage can directly be applied to bridge.

→ The current in secondary of x^{mer} is in opposite direction in two half cycles and hence net dc component through x^{mer} coil is zero. Which reduces the losses and reduces the danger of saturation of x^{mer}

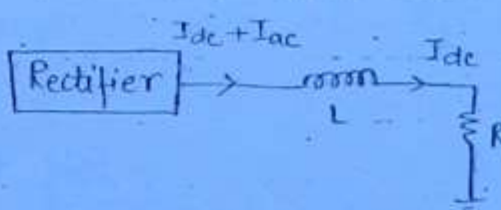
→ As two diodes conduct in series, in each half cycles, inverse voltage appearing across the diode get shared hence the circuit can be used for high voltage applications. (since PIV is less)

Filter Circuits :-

- To minimise ripple (ac component) at the o/p, filter circuits are used. We are using inductor & capacitor in filter circuits.

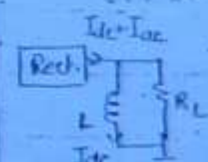
▷ Inductor :- $\cdot\ |Z_L| = \omega L = 2\pi f L$

for dc, $f = 0 \Rightarrow Z_L = 0 \Rightarrow$ L acts SC for dc.



$\rightarrow |Z_L|$ should be very high so that it blocks ac

$\boxed{L \rightarrow \text{very high}}$



Wrong arrangem
No I_{dc} through R_L.

$\rightarrow L\uparrow$, and/or $f\uparrow \Rightarrow |Z_L|\uparrow \Rightarrow$ ac at o/p $\downarrow \Rightarrow$ Ripple $\downarrow \Rightarrow r\downarrow$

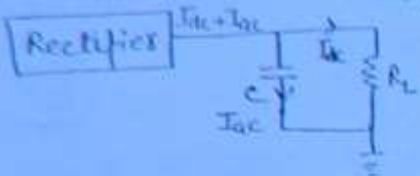
$$\boxed{r \propto \frac{1}{fL}} \quad -①$$

$\rightarrow \tau\uparrow \Rightarrow \frac{L}{R_L}\uparrow \Rightarrow L\uparrow$ and $R_L\downarrow \Rightarrow$ variation in current $\downarrow$.

$\Rightarrow r\downarrow$

$$\therefore \boxed{r \propto \frac{1}{\tau}} \quad -②. \qquad \text{From ① \& ② -} \quad \boxed{r \propto \frac{R_L}{fL}}$$

2) Capacitance :- $|X_C| = \frac{1}{2\pi f C}$ — for dc, $f = 0 \Rightarrow X_C = \infty$.



$\Rightarrow$ C acts as O.C for dc.

wrong arrangement

- $|X_C|$ should be very ~~high~~ low for ac to bypass it

$\Rightarrow$ $\boxed{C \rightarrow \text{very high}}$

- $C\uparrow$ and/or $f\uparrow$ $\Rightarrow$ $|X_C|\downarrow$ $\Rightarrow$ ac through $R_L \downarrow$ $\Rightarrow$ ripple & $r \downarrow$

$\Rightarrow r \propto \frac{1}{C \cdot f}$

→ $\tau = R_L C$ ⇒ should be very ↑ ⇒ variation is ↓ ⇒ ripple & r ↓.

$r \propto \frac{1}{\tau}$ ⇒ $\tau = R_L C$ ⇒ $\boxed{C\uparrow \text{ and } R_L\uparrow}$ for $r\downarrow$

→ $\boxed{r \propto \frac{1}{fCR_L}}$

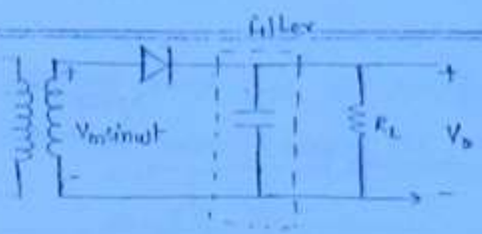
* Hence, for low load resistance, inductor is preferred and for high load resistance, capacitor is prefered.

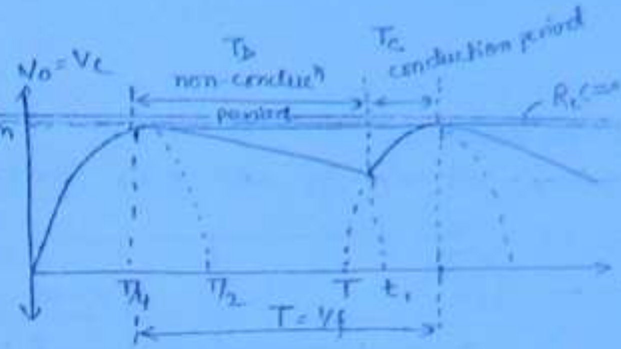
Alternatively, for low load (R_L high) capacitor is prefered and for high load (R_L low) inductor is preferred.

Types of filter —

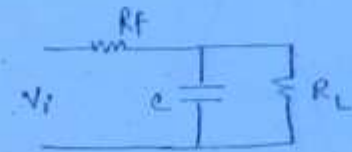
1) Capacitor Filter (imp)
2) Choke or Inductor filter
3) L section or L-C filter
4) π or CLC filter
5) π or CRC filter for compact circuit.

→ Capacitor Filter :- HWR with capacitor filter

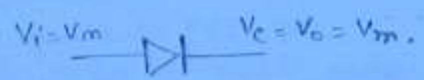




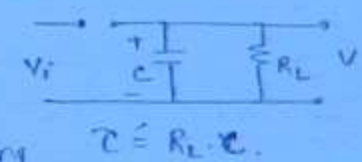
- $V_C(0^-) = V_C(0^+) = 0V$. Initially C acts as S.C and $V_0 = V_C = 0V$.
- For the first half of V_i, $D \to FB \to ON$.
- $\tau = (R_f \| R_L) \cdot C$
  $= R_f \cdot C$ $(\because R_f << R_L)$



- τ should be such that $\tau << T \Rightarrow$ rate of charging of C should be very high.
- At $T = T/4$, $V_i = V_m$ and $V_c = V_0 = V_m$.



- for $T > T/4$, $V_i \downarrow$ & when $V_i < V_0$, $\Rightarrow D \to RB \to$ off.



→ $\tau' R_L C$ should be $>> T$, so that rate of discharging of C is very slow. $\Rightarrow V_c \downarrow$. exponentially.

→ V_i will $\downarrow$ and then $\uparrow$ and when $V_i \geq V_C \Rightarrow D \to FB \to$ on and it will again charge C with $\tau = R_f C$: upto V_m. Thus, the cycle repeats.

→ from plot →

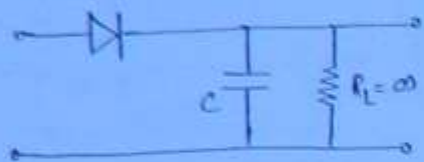
$\boxed{T_D + T_C = T}$ = time period of signal.

→ When we $\uparrow R_L C$, then $T_D \uparrow$, $T_C \downarrow$, variation $\downarrow$, $r \downarrow$.

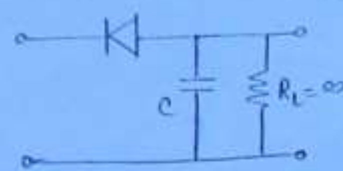
$\therefore$ For best filter, $T_D >> T_C$
or $\boxed{T_D \simeq T = 1/f}$ — ①

<u>Ideal Condition:</u>–
→ If $R_L C = \infty$, $V_0 = V_m$ → pure dc
$\Rightarrow r = 0$, $F = 1$; $C = 1$..

Peak Detector :-

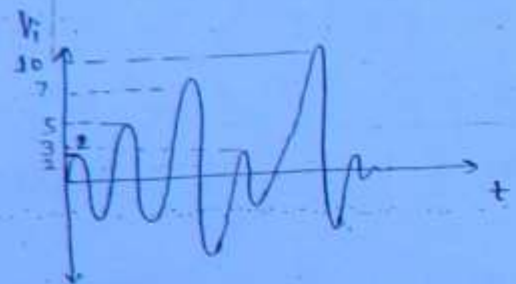


+ve Peak detector



-ve peak detector

Eg :



V_o = will charge upto

(i) 2V and hold

~~(ii) 8V and hold~~

(ii) 5V " "

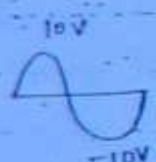
(iii) 7V " "

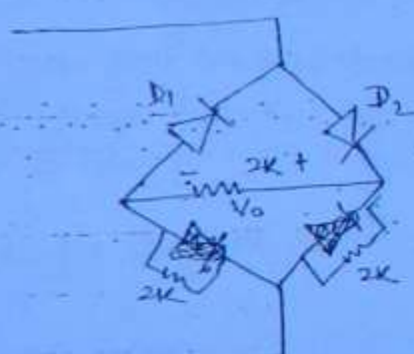
(iv) 3V → donot change → $V_o = 7V$ (diode will be RB).

(v) 10V → charge upto 10V.

Hence, the o/p will always hold the max. value of i/p.

Ques :-





Assume ideal diodes

① - Draw the o/p waveform.

② - find o/p dc level

③ - find PIV.

② o/p dc level $= \frac{2 \times V_m}{\pi} = \frac{10}{\pi}$

③ PIV = from fig ① $PIV = V_1 - V_3 = 10 - 5 = 5V$. Ans

Sol^n for +ve half–

$V_{24} = V_{234} = 10V$

$\therefore V_o = \frac{10}{2} = 5V$.

During -ve half

again $V_o = \frac{10}{2} = 5V$

in same direction.

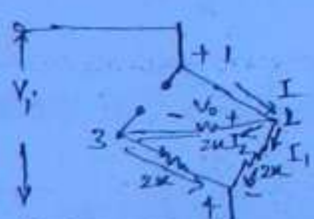
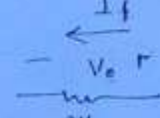
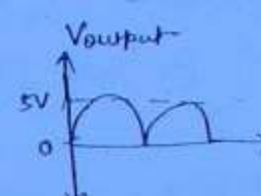
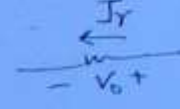


fig ①



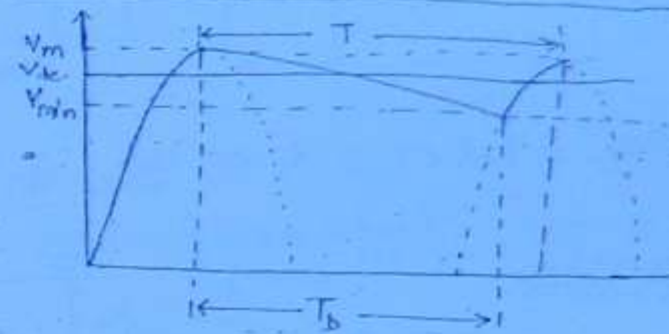




* The circuit of given ques is comparable to HWR since the o/p for the same i/p would have been same as $\frac{10V_m}{\pi}$.

Approximate solution

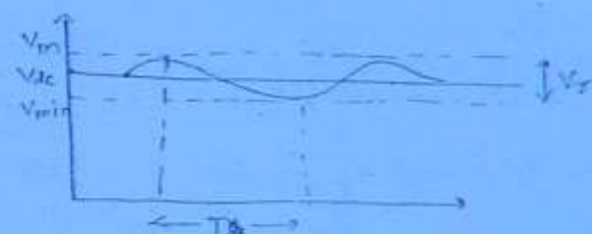
*



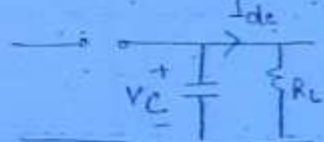
- $T_D \simeq T = 1/f$ — ①
- $R_L C$ = very high
- During T_D, C will discharge

$$V_o = V_c = V_m e^{-t/R_L C}$$

$$V_c \simeq V_m\left[1 - \frac{t}{R_L C}\right] \quad \{\because R_L C \text{ very high}\}$$



- $V_{dc} = \frac{V_m + V_{min}}{2}$ — ②
- V_r = peak to peak value of ripple voltage.
- $\therefore V_{dc} = V_m - \frac{V_r}{2}$ — ③
- $V_r = V_m - V_{min}$ = change in V_c during time T_D.
- $V_r = \frac{Q(\text{discharge})}{C}$
- $I_m = \frac{V_m}{R_L}$, $I_{min} = \frac{V_{min}}{R_L}$



$\therefore I_{dc} = \frac{1}{2}\left(\frac{V_m + V_{min}}{R_L}\right) = \frac{V_{dc}}{R_L}$

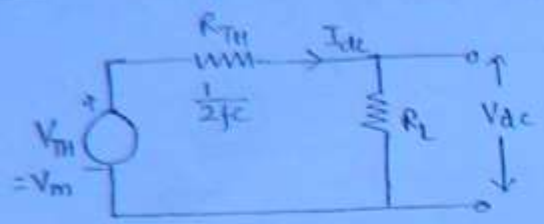
$\therefore Q(\text{discharge}) = \frac{V_{dc}}{R_L} \times T_D = I_{dc} \times T \quad \{\because T = T_D\}$

$\therefore V_r = \frac{I_{dc} \cdot T}{C} \Rightarrow \boxed{V_r = \frac{I_{dc}}{C \cdot f}}$ imp. or $\boxed{V_r = \frac{V_{dc}}{R_L \cdot C \cdot f}}$ imp

from ③ —

$\rightarrow \boxed{V_{dc} = V_m - \frac{I_{dc}}{2fC}}$ imp $\quad \left\{V_{dc} = \frac{I_{dc}}{R_L}\right\}$

Thevenin's Equivalent :-



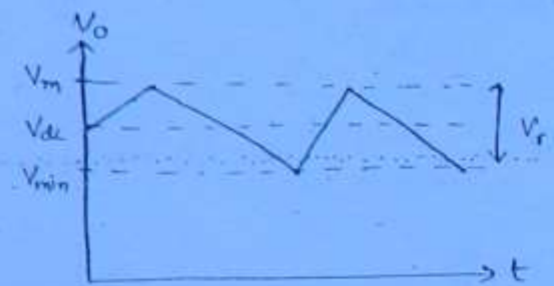
$V_{dc} = V_{TH} - I_{dc}(R_{TH})$.

Comparing with last eqn-

$V_{TH} = V_m$; $R_{Th} = \frac{1}{2fC}$

* When $f \uparrow$ & $C \uparrow$ or $R_L \to \infty$ then $V_{dc} \approx V_m$. (Ideal case → pure dc in o/p)

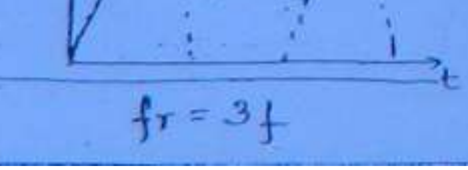
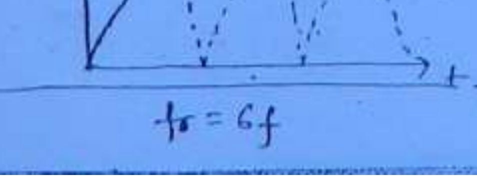
Ripple factor :-



$V_{acrms} = \frac{V_P}{\sqrt{3}} = \frac{V_r}{2\sqrt{3}}$

$= \frac{I_{dc}}{2\sqrt{3} fC} = \frac{V_{dc}}{2\sqrt{3} fCR_L}$

$\left\{ \because V_r = V_{P-P} \text{ and } \frac{V_{P-P}}{2} = V_P \right\}$ $\Rightarrow \gamma = \frac{V_{acrms}}{V_{dc}} \Rightarrow \boxed{\gamma = \frac{1}{2\sqrt{3}\, f.C.R_L}}$ Imp

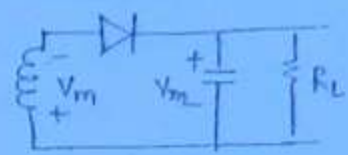
	HWR with C	FWR with C (Bridge/center tapped)
f_r	f	$2f$
Ripple Voltage, V_r	I_{dc}/fC	$I_{dc}/2fC$
V_{dc}	$V_{dc} = V_m - \frac{I_{dc}}{2fC}$	$V_{dc} = V_m - \frac{I_{dc}}{4fC}$
Thevenin's equivalent	$V_{TH} = V_m$, $R_{Th} = 1/2fC$	$V_{TH} = V_m$, $R_{TH} = \frac{1}{4fC}$
γ	$\gamma = \frac{1}{2\sqrt{3} fCR_L}$	$\gamma = \frac{1}{4\sqrt{3} \cdot f C \cdot R_L}$
Waveform.		
→ 3φ rectifier	$f_r = 3f$	$f_r = 6f$

* Peak Inverse voltage with C —

HWR

C → max. charged

⇒ $V_C = V_m$.

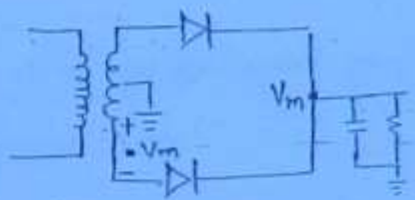


$V_D = V_m - (-V_m)$

$= 2V_m$.

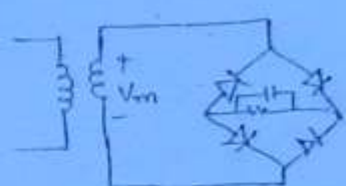
$\therefore \boxed{PIV = 2V_m}$ *imp

FWR



Center Tapped

$\boxed{PIV = 2V_m}$ *imp { same as before i.e. (w/o C) }



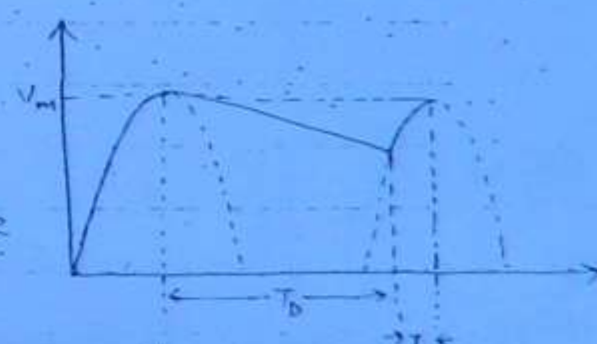
Bridge.

$\boxed{PIV = V_m}$ *imp { same as before, i.e. w/o C filter

Surge Current or Peak Diode Current :-

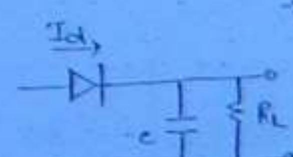
During T_D → C discharge

$Q(\text{discharge}) = I_{dc} \cdot T_D$.



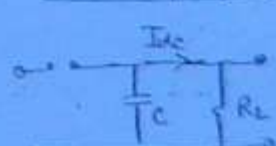
During T_C → Diode → ON → C will charge

$Q(\text{charge}) = I_d \cdot T_C$.



According to law of conservation of Q —

$I_D \cdot T_C = I_{dc} \cdot T_D$



$\Rightarrow \boxed{I_D = \dfrac{I_{dc} \cdot T_D}{T_C}}$

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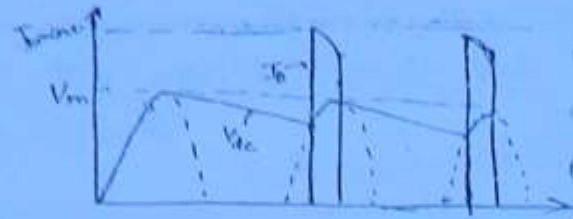
96



* If $R_LC \uparrow$, then $T_D \uparrow$, $T_C \downarrow$ $\boxed{r \downarrow \text{ (adv.) but } I_D \uparrow \text{ (Disadv.)}}$ **

Eg for best filter,

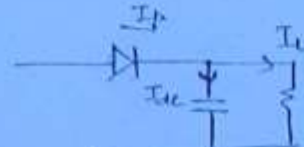
$T_D \gg T_C$.

$\Rightarrow V_{dc} \approx V_m$, $I_{dc} \approx I_m = \frac{V_m}{R_L}$ $\Rightarrow$ For $V_m = 10V$ & $R_L = 10k\Omega \rightarrow I_m = 1mA$

for $f = 50Hz$, $T = 1/f = 20msec$, $T_D = 19.98\ mA$, $T_C = 0.02mA$ (say)

I_D = surge current = $\frac{1mA \times 19.98}{0.02} \approx 1000\ mA$. (very large) → High power dissi.
→ diode damage.

Conduction Angle :- $\boxed{\phi = \omega T_c = \sqrt{\frac{2V_r}{V_m}}}$, $\omega = \frac{d\theta}{dt}$ rad/sec



$\rightarrow V_r = \frac{V_{dc}}{fR_LC}$

* $\boxed{I_{Dmax} = I_L\left[1 + 2\pi\sqrt{\frac{2V_m}{V_r}}\right]}$

$\rightarrow V_{dc} = V_m - \frac{V_r}{2}$; $V_{dc} \cong V_m$; $I_L \cong I_{DC} \cong I_m$.

$\Rightarrow I_m = \frac{V_m}{R_L}$, $I_{dc} = \frac{V_{dc}}{R_L}$

for FWR :-

$\phi = \omega T_c = \sqrt{\frac{2V_r}{V_m}}$

$\rightarrow V_r = \frac{I_{dc}}{2fC}$

$\rightarrow I_{Dmax} = I_L\left[1 + 2\pi\sqrt{\frac{V_m}{2V_r}}\right]$

$\rightarrow V_m \cong V_{dc}$; $I_L \cong I_m = I_{dc}$.

Pg.30 (Workbook)

(1) (Conventional) –

(97)

Given – $V_{dc} = 30V$, $r \le 0.01$, $R_L = 500\Omega$, $f = 50Hz$.

$I_{Dmax} = ?$, $C = ?$

$\because r = \frac{1}{2\sqrt{3} f C R_L} \le 0.01 \Rightarrow C \ge 1154\,\mu F$

$I_{Dmax} = I_L\left[1 + 2\pi\sqrt{\frac{2V_m}{V_r}}\right]$

$I_L \cong I_{dc} \cong \frac{V_{dc}}{R_L}$.

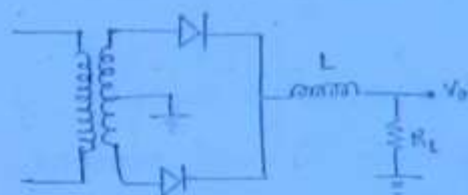
$V_r = \frac{V_{dc}}{f C R_L} = \frac{30}{50 \times 1154 \times 10^{-6} \times 500} = 1.02V$

$V_m = V_{dc} + \frac{V_r}{2} = 30.51V$

Substitute, I_L, V_r and V_m & calc. I_{Dmax}.

Inductor Filter (or) Choke filter :-

→ $\boxed{r = \frac{2}{3\sqrt{2}} \cdot \frac{1}{\sqrt{1 + (X_L/R_L)^2}}}$ **

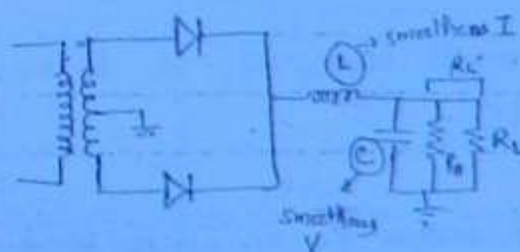


$\boxed{\begin{matrix} X_L = \omega L \text{ for HWR} \\ X_L = 2\omega L \text{ for FWR.} \end{matrix}}$ **

→ If $\left(\frac{X_L}{R_L}\right)^2 \gg 1 \Rightarrow r \propto \frac{R_L}{X_L} \Rightarrow \boxed{r \propto \frac{R_L}{f L}}$ (imp. **) $= \boxed{r \propto \frac{1}{f \tau}}$ (imp. **)

L-section or LC filter :

→ $\boxed{r = \frac{\sqrt{2}}{3} \cdot \left(\frac{X_C}{X_L}\right); \; X_C = \frac{1}{\omega C}; \; X_L = \omega L \text{ for HWR} \quad X_C = \frac{1}{2\omega C}; \; X_L = 2\omega L \text{ for FWR.}}$ **

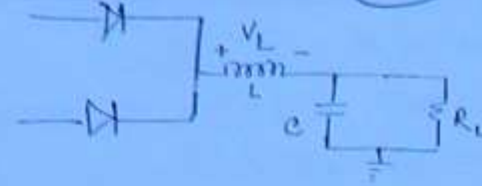


→ $\boxed{r \propto \frac{1}{f^2}}$ (** imp) $\therefore$ r → very small.

→ $\boxed{r \text{ is independent of } R_L}$. (** imp)

R_B = Bleeder Resistance.

$R_L' = R_B \| R_L \cong R_L \; \boxed{(\because R_B \gg R_L)}$ (chk.)



* When there is sudden change in current – then $\frac{dI}{dt}$ = large.

$\therefore V_L = L\frac{dI}{dt}$ = very large. → Back emf.

This V_L, will act as reverse bias for both diodes,

⇒ This sudden change occurs when circuit is ON w/o R_L.

$\therefore \tau = \frac{L}{R_L} = 0 \quad \left(\because R_{Leq} = \infty \atop (o.c)\right)$

$\because \tau = 0$, then $\frac{dI}{dt}$ = large ⇒ V_L = large.

Hence, R_B is attached in the o/p. so that even if $R_L = \infty$. (o.c) effective resistance : $R_L' = R_B \| \infty = R_B$ and hence $\tau = \frac{L}{R_L'}$ is never equal to 0. Therefore, no sudden change of current.

⇒ When R_B is attached across a capacitor, it helps C to discharge through it. when supply and R_L are removed.

By sir

* The basic req. of this filter is the current through choke must be continuous. An interrupted current through choke may develope large back emf which may be in excess of PIV rating of diode. and/or max rating of capacitor.

· To eliminate back emf, a bleeder resistance R_B is connected across o/p terminal.

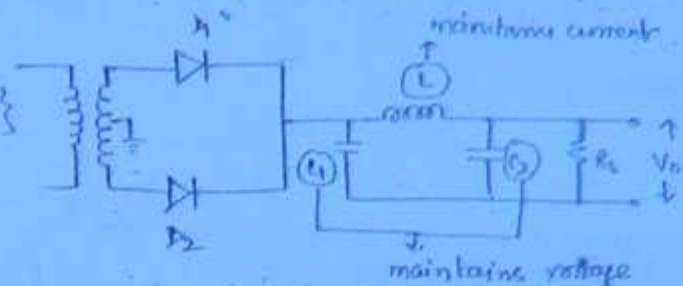
* Another reason for R_B is to bleed off voltage stored in filter capacitor when supply is turned off.

*

Potential Divider → Different o/p's from diff. points from R_B.

π or CLC Filter :-

$\rightarrow r = \dfrac{\sqrt{2} \cdot X_{C_1} X_{C_2}}{R_L \cdot X_L} = \dfrac{\sqrt{2} \cdot (X_C)^2}{R_L \cdot X_L}$ $\{C_1 = C_2\}$



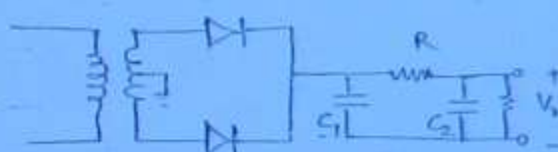
$\rightarrow X_C = \dfrac{1}{\omega C}$; $X_L = \omega L$ for HWR

$\rightarrow X_C = \dfrac{1}{2\omega C}$; $X_L = 2\omega L$ for FWR.

$\rightarrow$ $r \propto \dfrac{1}{\omega^3 \cdot C_1 C_2 L R_L}$ $\Rightarrow$ $\boxed{r \propto \dfrac{1}{f^3}}$ $\therefore$ r = very small.

π or CRC filter :-

$r = \dfrac{\sqrt{2} \cdot X_{C_1} \cdot X_{C_2}}{R_L \cdot R} = \dfrac{\sqrt{2}(X_C)^2}{R_L \cdot R}$ (for $C_1 = C_2$).



$\rightarrow$ $X_C = 1/\omega C$ for HWR

$\rightarrow$ $X_C = 1/2\omega C$ FWR

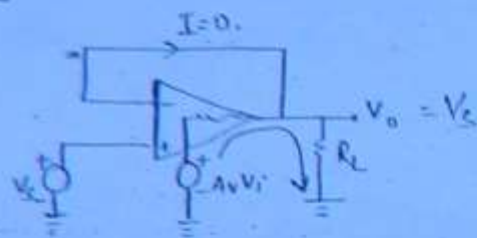
$\rightarrow$ $r \propto \dfrac{1}{\omega^2 C_1 C_2 R_L \cdot R}$ $\Rightarrow$ $\boxed{r \propto \dfrac{1}{f^2}}$ r = small (relatively more than CLC filter)

* C	L	LC	CLC
$\rightarrow$ $r \propto 1/f$	$r \propto 1/f$	$r \propto \dfrac{1}{f^2}$	$r \propto 1/f^3$
$\rightarrow$ $r \propto 1/\tau$	$r \propto 1/\tau$	$r \propto 1/\tau_1\tau_2$	$r \propto \dfrac{1}{\tau_1 \cdot \tau_2 \cdot \tau_3}$
$\rightarrow$ $\tau = R_L C$	$\tau = L/R_L$	$\tau_1\tau_2 = \dfrac{L}{R_L} \cdot R_L C = LC$	$\tau_1 \tau_2 \tau_3 = (R_L C_1)(R_L C_2) \times \dfrac{L}{R_L} = C_1 C_2 L R_L$
$\rightarrow$ $r \propto \dfrac{1}{R_L C}$	$r \propto L/R_L$	$\therefore r \propto 1/LC$	$r \propto \dfrac{1}{C_1 C_2 L R_L}$

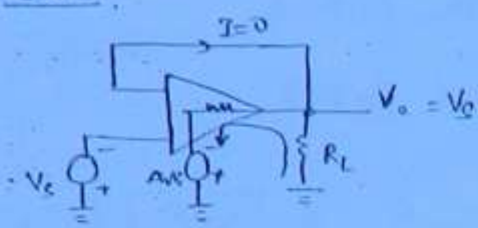
Precision Rectifiers :-

– Voltage Follower –

$V_s > 0$



$V_s < 0$.

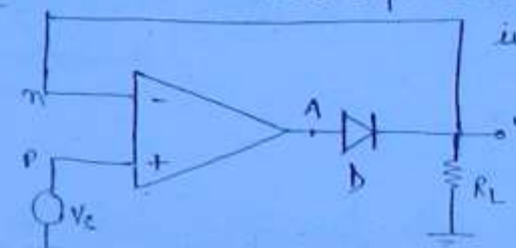


Hence, to maintain V_o at level of input V_s, op-amp should provide a current as indicated above. If this current = 0, then $V_o = 0$.

– Precision HWR :-

→ Assuming Ideal op-amp & practical diode.

(This circuit is also called superdiode since cut in voltage is very small, ≈ µV.)



V_S	V_A	D	V_o
$V_S > 0$ (very small) ≈ µV	↑ towards $+V_{sat}$ Reaches till $V_A \cong 0.7V$	ON	V_S
$V_S < 0$	$V_A \downarrow (-V_{sat})$ Reaches to final value $= -V_{sat}$	OFF	0 (since there is no current due to D is RB)

→ Till the time D is about to 'ON', the op-amp will act as open loop. When D is on, the due to –ve feedback, applying virtual ground,

Hence, gain is very high.

(see next page V_o vs V_i plot) explain

$V_P = V_n = V_s = V_o$.

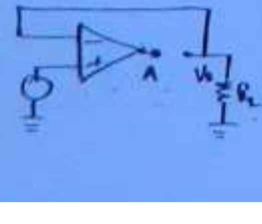
$\therefore V_A = 0.7V + V_o$

$\Rightarrow V_A = 0.7V + V_s$.

$\Rightarrow V_A \cong 0.7V$.

Hence, the diode D will avoid op-amp to go into positive saturation.

When $V_s < 0$ —

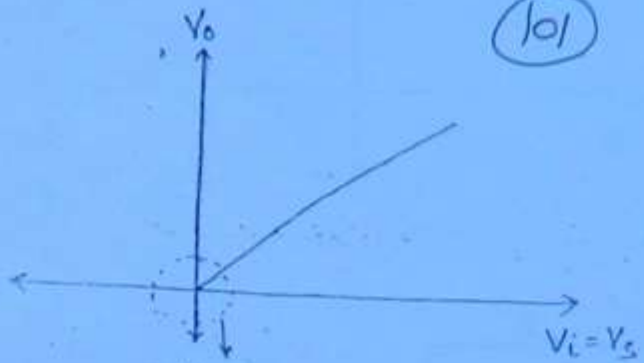


Op-amp will behave as open loop and $A_V = 10^6$

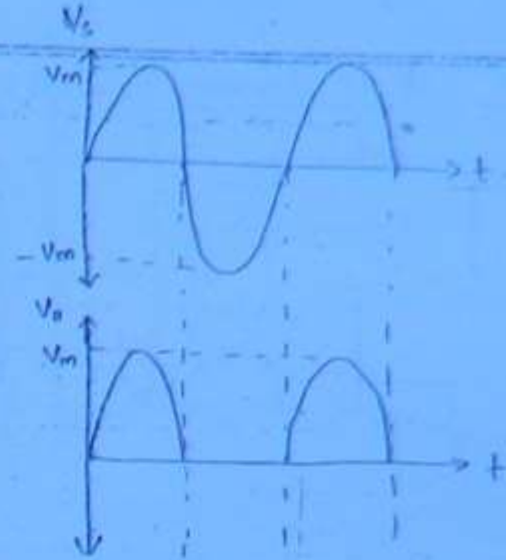
$\therefore$ for small V_s,

$V_A = -V_{sat}$.

→ PIV for the diode D is $-V_{sat}$.



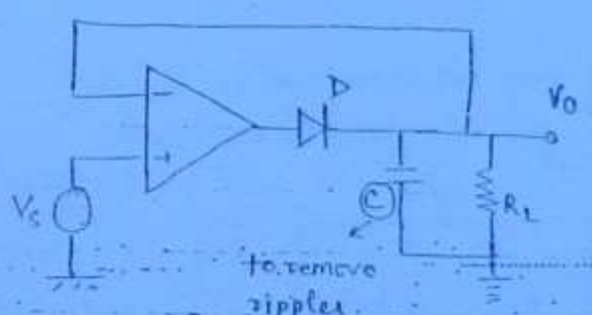
cutin voltage is very small, $\approx 0.7\mu V$



$\left\{ \text{When } V_i = 0.7\mu V, \; V_A = A_V \cdot V_i = 10^6 \times 0.7\mu V = 0.7V = V_\gamma \right\}$

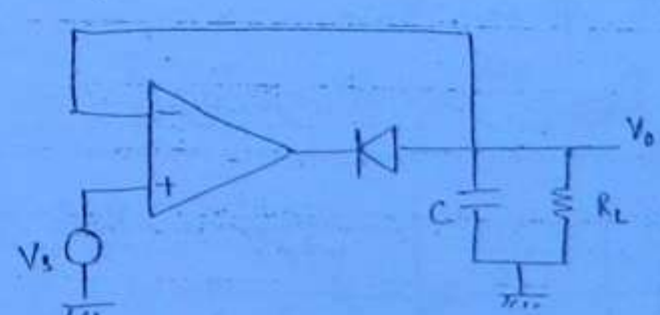
<u>Drawback</u> : PIV is very high.

*



* If $R_L C = \infty$, then above circuit will act as +ve peak detector

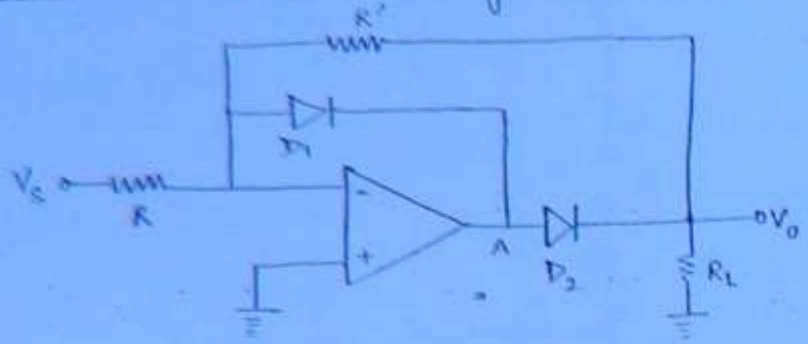
*

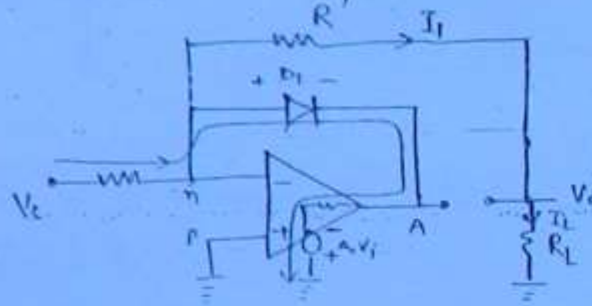


→ This circuit will avoid −ve saturation for $V_s < 0$.

→ If $R_L C = \infty$, then it will act as −ve peak detector.

Precision HWR (i/p at Inverting Terminal).





When $V_s > 0$ –

D_1 = FB, D_2 = RB

$V_n = V_p = 0$.

$V_m = 0.7V$, $\therefore$ $V_A = -0.7V$

$\therefore$ D_1 will avoid negative saturation when i/p is +ve.

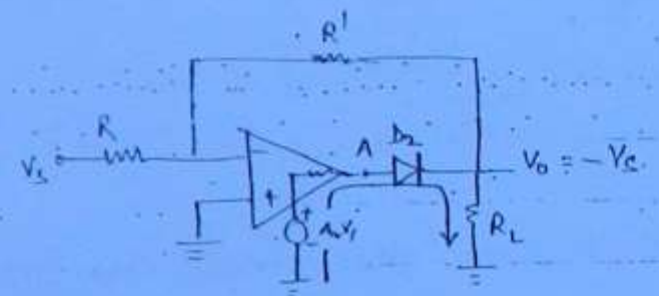
$I_1 = I_L = 0 \Rightarrow V_o = 0$.

→

$\Rightarrow$ PIV = 0.7 V. { very less as compared to V_{sat} as we were getting in last case }

When $V_s < 0$

D_1 = RB; D_2 = FB



→ $V_o = -\frac{R'}{R} V_s = -V_s$ { if $R' = R$ }

→ $V_A = 0.7 - V_s \approx 0.7V$

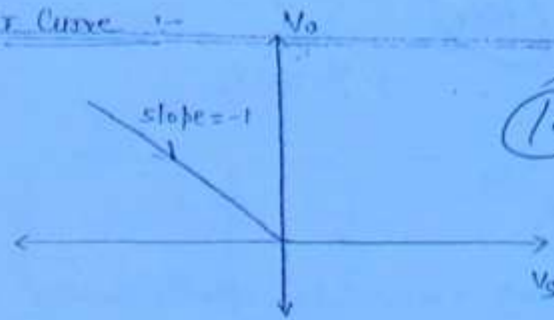
$\therefore$ D_2 will avoid positive saturation when i/p is −ve

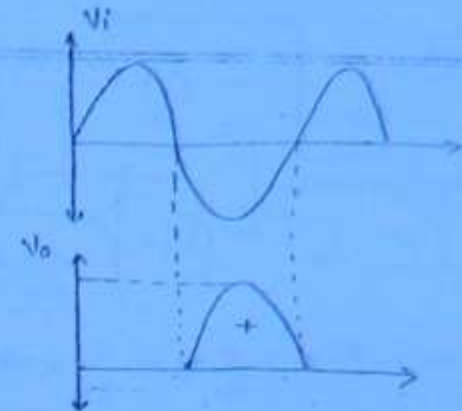
→

$\Rightarrow$ PIV = 0.7 V.

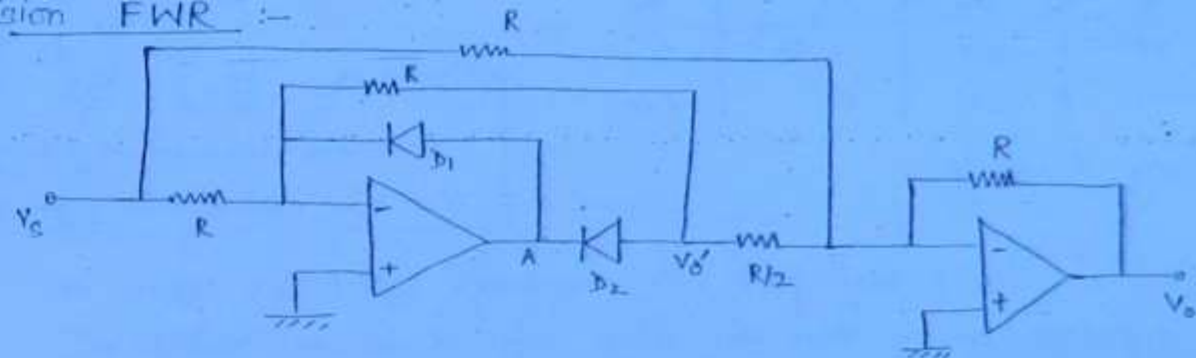
V_s	V_A	D_1	D_2	V_o	PIV
→ $V_s > 0$	↓ towards $-V_{sat}$ $(-0.7V)$	ON	OFF	0	0.7 V for D_2
→ $V_s < 0$	↑ towards $+V_{sat}$ $(0.7V)$	OFF	ON	$-V_s$	0.7 V for D_1

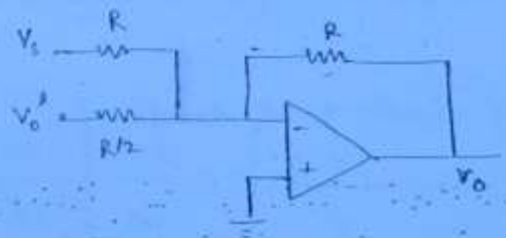
Transfer Curve :-





Precision FWR :-

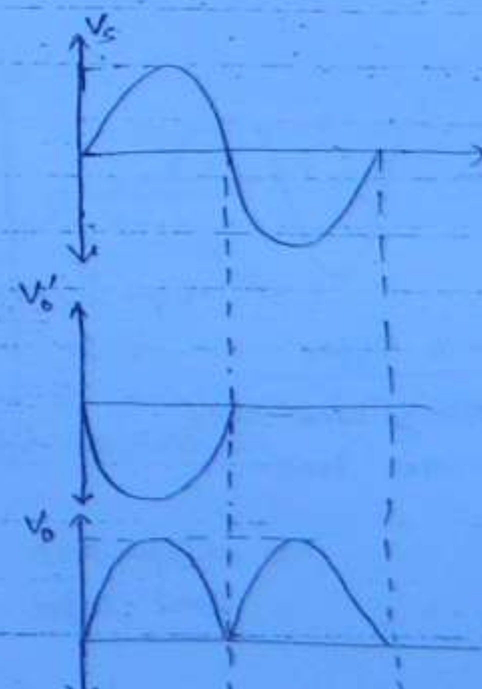




$$V_o = \frac{-R}{R/2} \cdot V_o' - \frac{R}{R} V_s$$

$$\Rightarrow V_o = -2V_o' - V_s \quad -(1)$$

V_s	V_A	D_1	D_2	V_o'
$V_s > 0$	$\downarrow -V_{sat}$ $(-0.7V)$	OFF	ON	$-V_s$
$V_s < 0$	$\uparrow +V_{sat}$ $(0.7V)$	ON	OFF	0



for +ve half -

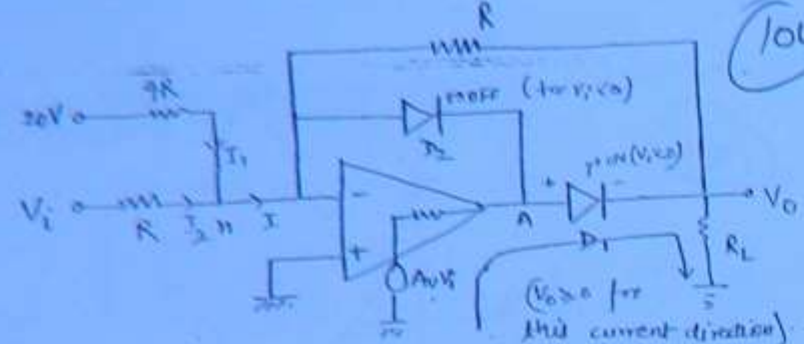
$V_s > 0 = 5$ (let) $\therefore V_o' = -5V$

$\therefore V_o = -2(-5) - 5 = 5V$ (from eq^n (1))

for -ve half -

$V_s < 0$, $V_o' = 0 \Rightarrow V_o = 5V$.

Ques:- Draw → V_o (vs) V_i.



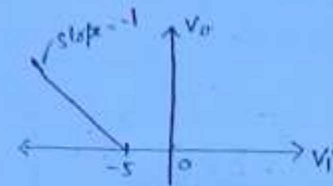
($V_o \geq 0$ for this current direction) → current in opposite direction not possible as D_1 will be RB.

Sol^n:-

for $V_i < 0$, (D_1 = ON, D_2 = OFF)

$$V_o = -\frac{R}{R}V_i - \frac{R}{4R} \times 20 = -V_i - 5$$

but, $V_o \geq 0 \Rightarrow -V_i - 5 > 0 \Rightarrow V_i \leq -5$



V_i	D_1	D_2	V_o	V_n
$V_i \leq -5$	OFF	ON	$-V_i-5$	≥ 0
$V_i > -5$	ON	OFF	0	<0

* $I = I_1 + I_2 = \frac{20}{4R} + \frac{V_i}{R} = \frac{V_i+5}{R}$

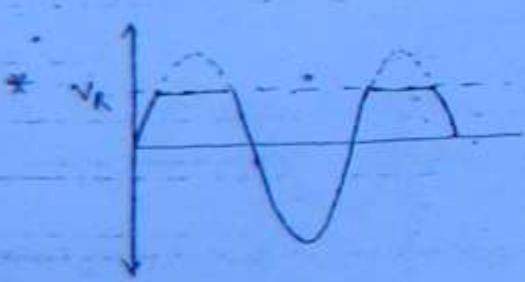
$I > 0$ ⇒ V_i effectively +ve ⇒ V_o = -ve (not possible)

$I \leq 0$ ⇒ V_i effectively -ve ⇒ V_o = +ve (possible)

Clippers / Limiting Circuits :-

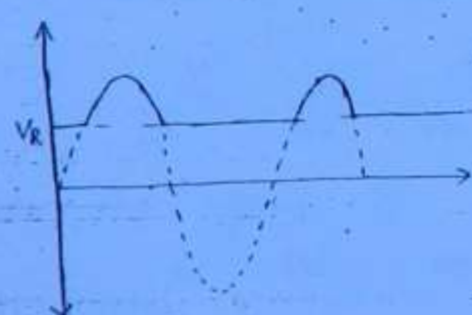
- These are used to select that part of waveform which lies above or below some reference level. These are also referred to as voltage or current limiters, amplitude selectors or slicers.

- These are of two types (according to the position of diode w.r.t. load) -
  (a) Series clipper
  (b) Shunt clipper



+ve Clipper

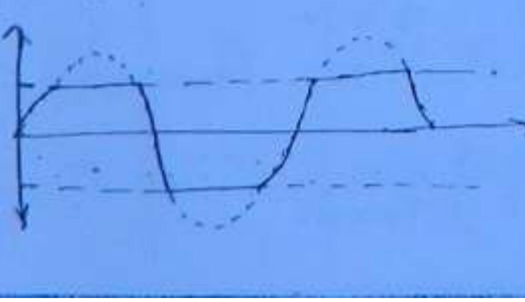
→ clipping above some reference level.



-ve clipper

→ clipping below some reference level.

Two independent level clipper ←



28th August, 2012

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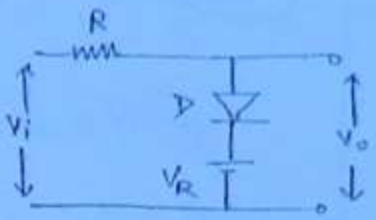
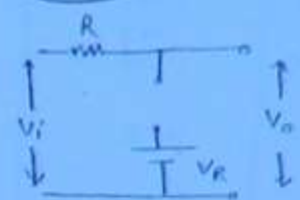
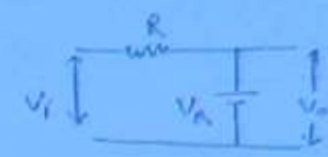


Shunt Clipper (Positive)



D → RB

$(V_R > V_i)$

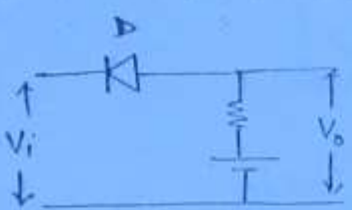


D → FB

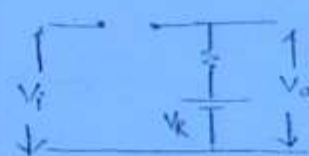
$(V_R < V_i)$

V_i	D	V_o
$V_i \leq V_R$	OFF	V_i
$V_i \geq V_R$	ON	V_R

*



Series Clipper (positive)



D → RB

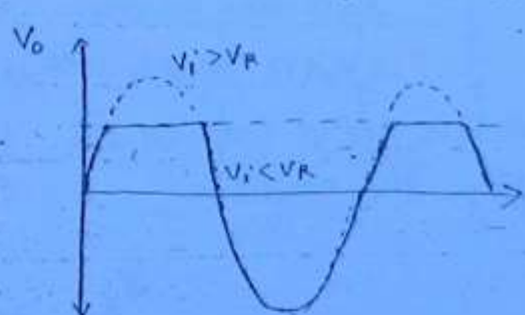
$(V_i > V_R)$

D → FB

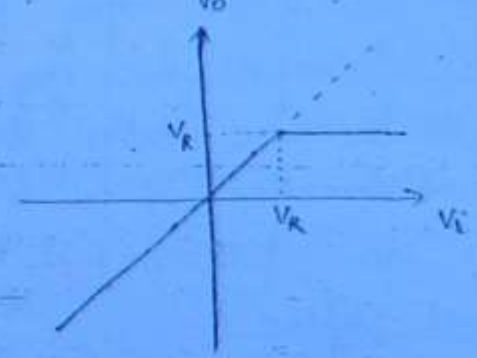
$(V_i < V_R)$

V_i	D	V_o
$V_i \leq V_R$	ON	V_i
$V_i > V_R$	OFF	V_R

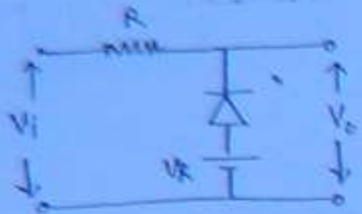
*



o/p

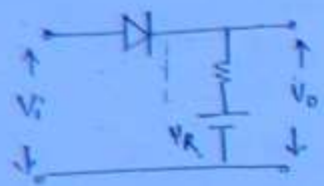


Transfer Characteristic



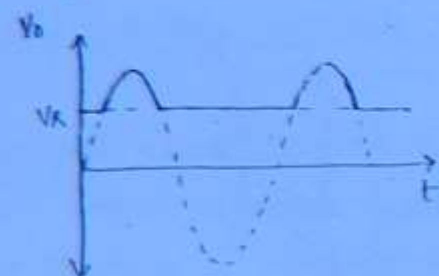
V_i	D	V_o
$V_i \geq V_R$	OFF	V_i
$V_i \leq V_R$	ON	V_R

Shunt clipper (Negative)

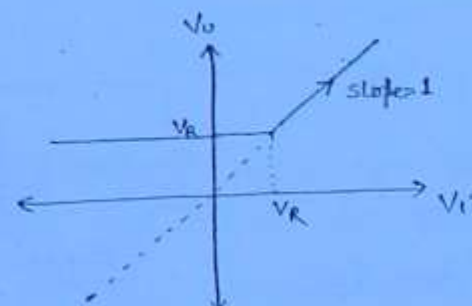


V_i	D	V_o
$V_i \geq V_R$	ON	V_i
$V_i \leq V_R$	OFF	V_R

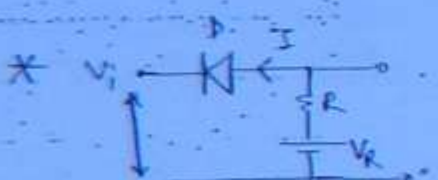
Series Negative Clipper



O/p curve



Transfer Characteristic



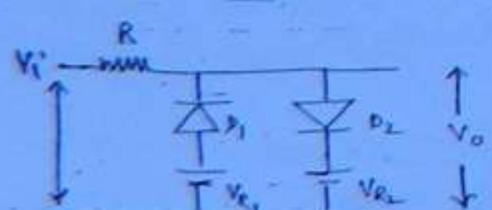
$$I = \frac{V_i - V_R}{R}$$

$I \geq 0$ then $D \rightarrow$ ON ; $I \leq 0$ then $D \rightarrow$ OFF

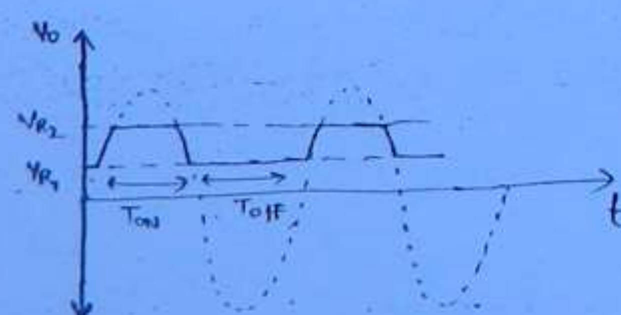
$\Rightarrow V_i \geq V_R$ then $D \rightarrow$ ON $\Rightarrow V_i \leq V_R$ then $D \rightarrow$ OFF

→ It is easiest way to determine whether diode is ON or OFF. Calculate the current in forward direction of diode and apply the condition.

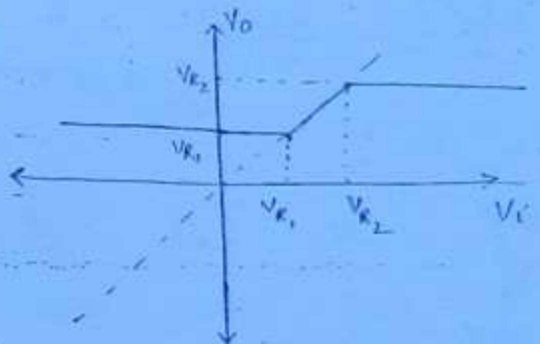
→ Two Independent level clipper :-



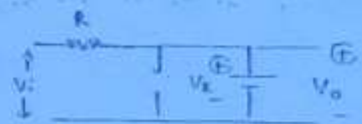
$(V_{R_2} > V_{R_1})$.



Range of V_i	D_1	D_2	V_o
$V_i \le V_{R_1}$	ON	OFF	V_{R_1}
$V_{R_1} \le V_i \le V_{R_2}$	OFF	OFF	V_i
$V_i \ge V_{R_2}$	OFF	ON	V_{R_2}

→ 

→ To conclude that V_{R_1} & V_{R_2} are +ve, check polarity at V_o wherever o/p is V_R. If same polarity then V_R = +ve, else −ve.

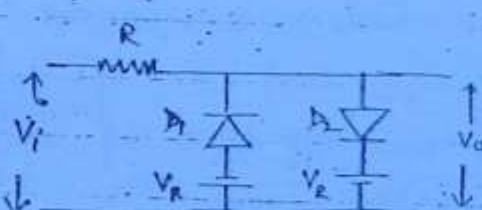


⇒ V_R = +ve.

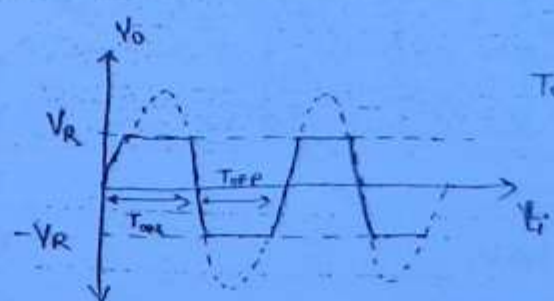
→ from o/p curve, $T_{off} > T_{ON}$ ⇒ $D < 50\%$. output is an asymmetrical square wave.

→ This circuit is used as a means of converting a sinusoidal waveform into a square wave.

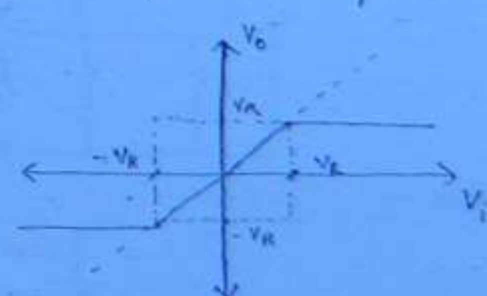
→ To generate a symmetrical square wave, V_{R_1} and V_{R_2} are adjusted to be numerically equal but are of opposite sign.

→ 

V_i	D_1	D_2	V_o
$V_i \le -V_R$	ON	OFF	$-V_R$
$-V_R \le V_i \le V_R$	OFF	OFF	V_i
$V_i \ge V_R$	OFF	ON	V_R.

→ 

$T_{ON} = T_{OFF}$
⇒ $D = 50\%$



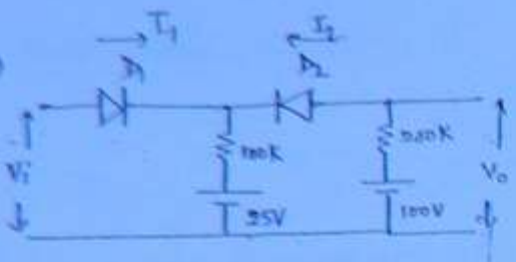
Transfer characteristic

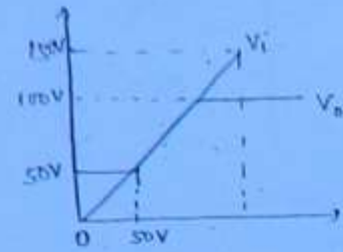
→ Symmetrical Sq. wave / Symmetrical clipping

Que: (1) The i/p voltage V_i to the two level clipper shown in fig. varies linearly from 0 to 150V. Sketch the o/p voltage V_o. to the same time scale as the i/p voltage. Assume ideal diodes.

108

(a)





Sol^n

Range of V_i	D_1	D_2	V_o.
$0 \le V_i \le 50$	OFF	ON	50V.
$50 \le V_i \le 100$	ON	ON	V_i
$V_i \ge 100$	ON	OFF	100 V

$\rightarrow I_1 = \dfrac{V_i - 25}{100k} + \dfrac{V_i - 100}{200k}$

For D_1 = ON, $I_1 \ge 0 \Rightarrow \dfrac{V_i - 25}{100k} + \dfrac{V_i - 100}{200k} \ge 0$

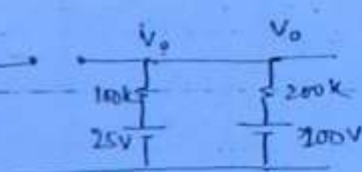
$\Rightarrow V_i \ge 50$

$\rightarrow I_2 = \dfrac{-V_i + 100}{200k}$, for D_2 = ON –

$I_2 \ge 0$

$\Rightarrow V_i \le 100$.

$\rightarrow$ When $0 \le V_i \le 50$,



$\dfrac{V_o - 100}{200k} + \dfrac{V_o - 25}{100k} = 0.$

$\Rightarrow V_o = 50V$.

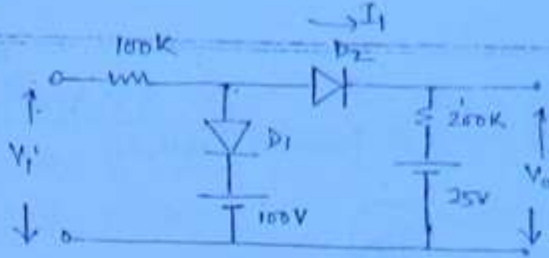
$\rightarrow$ When $50 \le V_i \le 100$

$V_o = V_i$

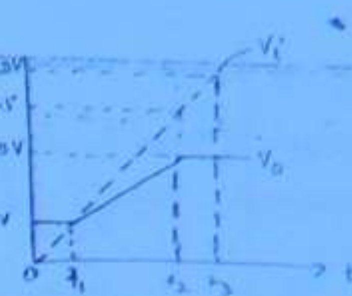
$\rightarrow$ When $V_i \ge 100$ –

$\Rightarrow V_o = 100V$.

(b)



(109)



Solⁿ: Since voltage across D_1 is very high (100V), then D_2 will ON before D_1.

$\therefore \quad I_1 = \dfrac{V_i - 25}{300K}$, for $D_2 = ON$
(Assuming D_2 off)

$I_1 > 0$

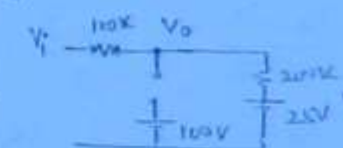
$\Rightarrow V_i > 25$ — (Breakpoint.)

V_i	D_1	D_2	V_o
$0 \leq V_i \leq 25$	OFF	OFF	25V
$25 \leq V_i \leq 137.5$	OFF	ON	$\dfrac{2V_i + 25}{3}$
$V_i \geq 137.5$	ON	ON	100V

For $V_i > 25$, V_o will be -

$$\frac{V_o - 25}{200} + \frac{V_o - V_i}{100} = 0$$

$$\Rightarrow V_o = \frac{2V_i + 25}{3}$$



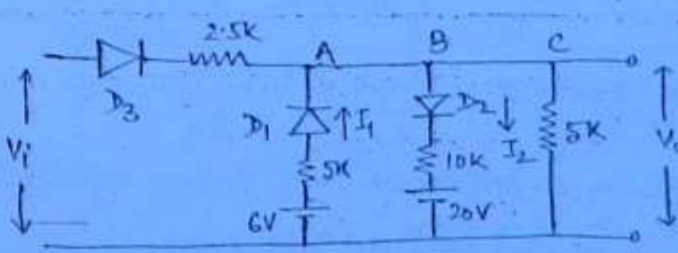
Now for $D_2 = ON$ -

$V_o \geq 100V$

$\Rightarrow \dfrac{2V_i + 25}{3} \geq 100 \Rightarrow V_i \geq 137.5V$.

↳ (Breakpoint

Ques:- Assume that the diodes are ideal, make a plot of V_o vs V_i for the range of V_i from 0 to 50V. Indicate all slopes and voltage levels. Indicate for each region, which diodes are conducting.



Solⁿ

Solⁿ:- When $V_i = 0$,

voltage across $D_2 = \cancel{\infty}$ is large ($\approx 20V$) and D_1 = forward biased.

Due to D_1, ~~current~~ voltage at A,

$$V_A = 3V.$$

1|10

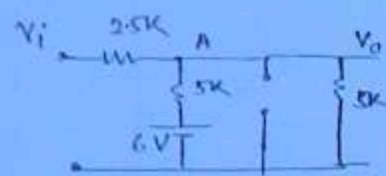
Now, this V_A is making diode D_3 RB.

Now, when $V_i \geq 3V$ then $D_1 = ON$. ↳ Break point.

for $0 \leq V_i \leq 3$, $V_0 = V_A = 3V$

for $V_i \geq 3$,

$D_1 = ON$, $D_2 = OFF$, $D_3 = ON$.



$$\frac{V_A - V_i}{2.5K} + \frac{V_A - 6}{5} + \frac{V_A}{5} = 0$$

$$\Rightarrow \frac{4V_A}{5} = \frac{2V_i}{5} + \frac{6}{5}$$

$$\Rightarrow V_A = \frac{V_i + 3}{2}$$

Now diode D_1 will remain in FB till

$V_A \leq 6$

$\Rightarrow \frac{V_i + 3}{2} \leq 6$

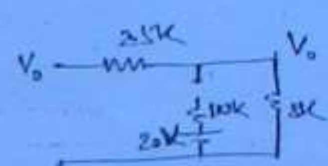
$\Rightarrow V_i \leq 9V$ → Break point.

$\left\{ I_1 = \frac{V_A - 6}{5} \geq 0 \text{ for } D_1 = ON \;\; \Rightarrow V_A \geq 6 \right\}$

∴ for $3 \leq V_i \leq 9$; $V_0 = V_A = \frac{V_i + 3}{2}$.

for $V_i \geq 9V$,

$D_1 = OFF$, $D_2 = OFF$, $D_3 = ON$.



$$\left\{ \begin{aligned} I_2 &= \frac{V_A - 20}{10} \geq 0 \\ &= 2/3 V_i \geq 20 \\ &\Rightarrow V_i \geq 30 \end{aligned} \right.$$

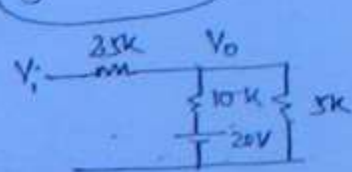
$$V_0 = \frac{5}{7.5} V_i = \frac{2}{3} V_i$$

Now for D_2 to be ON, $\frac{2}{3} V_i \geq 20V$ $\Rightarrow V_i \geq 30V$. → Break point.

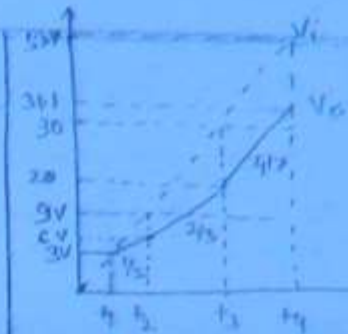
for $V_i \geq 30V$,

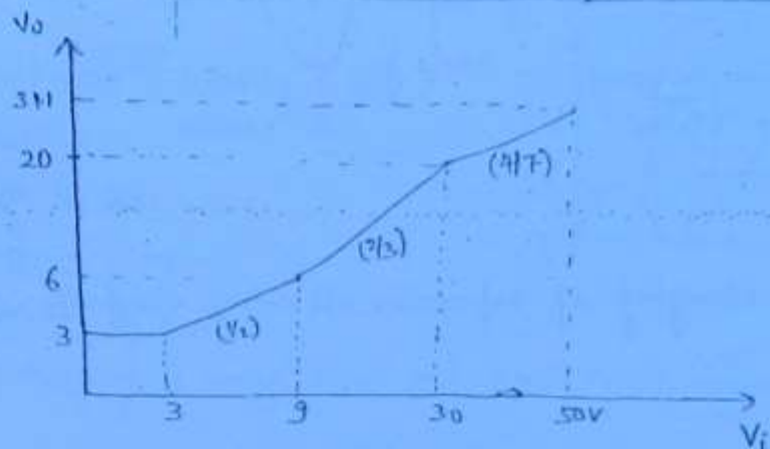
on applying KCL,

$$V_0 = \frac{4V_i + 20}{7}.$$

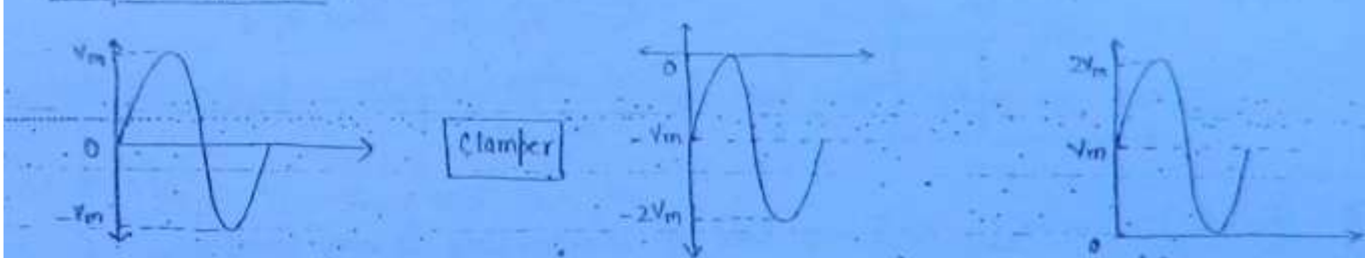


Range of V_i	D_1	D_2	D_3	V_o
$0 \le V_i \le 3$	ON	OFF	OFF	3V
$3 \le V_i \le 9$	ON	OFF	ON	$\frac{V_i+3}{2}$
$9 \le V_i \le 30$	OFF	OFF	ON	$\frac{2}{3} V_i$
$30 \le V_i \le 50$	OFF	ON	ON	$\frac{4}{7} V_i + \frac{20}{7}$





Clamper Circuit :-



(Input)	(Negative Clamper)	(Positive clamper)
Swing = $2V_m$	Swing = $2V_m$	Swing = $2V_m$
f = 50Hz	f = 50Hz	freq = 50Hz
dc level = 0	dc level = $-V_m$	dc level = V_m

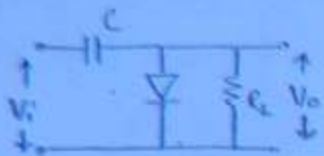
→ Clamper circuits are also called as dc translator, dc restorer, dc inserter.

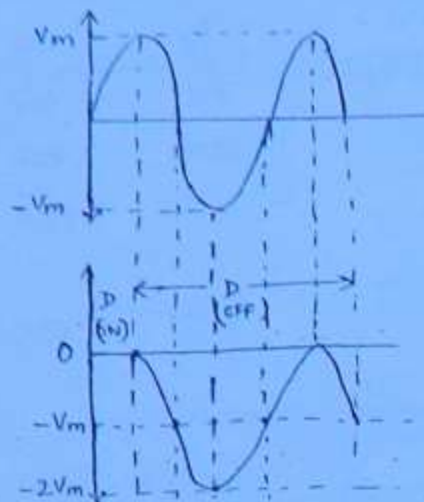
→ The circuit which are used to add a dc level as per the requirements to ac o/p signal are called clamper circuit.

→ These are of two types — Negative Clamper → adds −ve dc level to ac o/p sig
Positive clampler → adds +ve level.

29th August, 2012

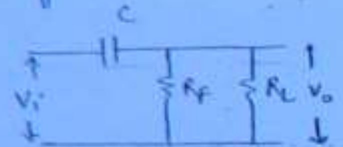
Negative Clamper :-





Initially, $V_c(0^-) = V_c(0^+) = 0$.
hence, C will act as S.C.

During I^{st} +ve half,
$D \rightarrow FB$.

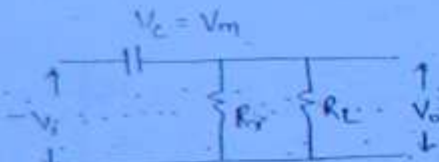


$\tau = (R_f \| R_L) C$
$\approx R_f C \; \{\because R_f \ll R_L\}$

$\{ R_f C \ll T$. Hence, rate of charging of capacitor is very high. It will charge till maximum value Vm.

→ At $t = T/4$, $V_i = V_m$ & $V_c = V_m$.
$\because D \rightarrow ON$, $R_f \approx 0$ and hence, $V_D \approx 0$. $\therefore V_o = V_D = 0$.

→ for $t > T/4$,

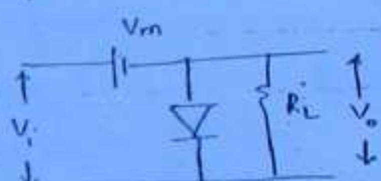


$V_D = V_i - V_m$ and $V_i \downarrow$
and ~~when~~ $V_i \leq V_m$
$\therefore D \rightarrow RB$.

$\tau = (R_f \| R_L) C \approx R_L C \gg T \Rightarrow$ Rate of discharging is very small ≈ 0.

→

V_i	$V_o = V_i - V_m$
V_m	0
0	$-V_m$
$-V_m$	$-2V_m$

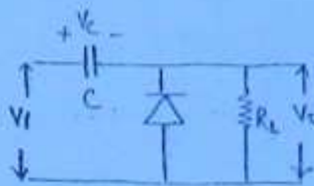


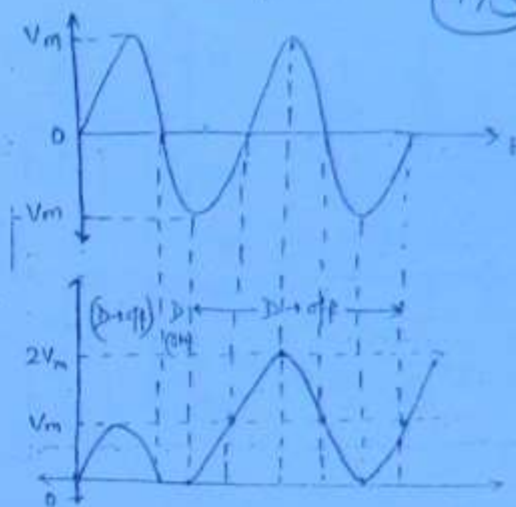
→ Diode will remain off. after this instant.

* We cannot use a dc battery instead of capacitor as the value of battery will vary w.r.t the peak value of signal.

→ Once the capacitor is charged till V_m, it will act as battery of value V_m

Positive Clamper:- It adds positive dc level to ac o/p.

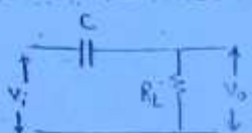
→ 



→ $V_c(0^-) = V_c(0^+) = 0V$ → initially C will act as S.C.

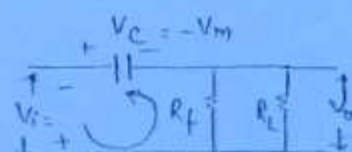
During 1^{st} +ve half —

→ Diode D will be RB.

∴ 

$\tau = R_L C >> T$

∴ Rate of charging is very low and C will remain uncharged till $t = T/2$.

→ for $t > T/2$ — 

→ During first -ve half

D → ON; $\tau \approx R_f C << T$

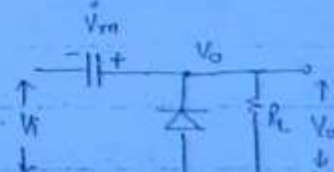
Now, the rate of charging is very high and will charge till $t = 3T/4$.

→ At $t = 3T/4$, $V_i = -V_m$, and $V_c = -V_m$.

→ for $t \geq 3T/4$ —

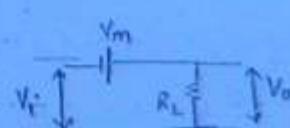
V_i	$V_o = V_i + V_m$
$-V_m$	0V
0	V_m
V_m	$2V_m$

$V_o = V_i + V_m$



∴ Voltage across D is always -ve, hence D → off
(V_o = +ve)

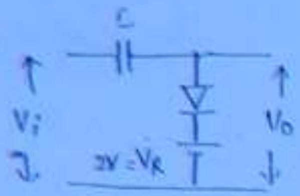
and ∵ D is off, C will never discharge.

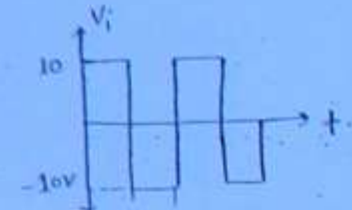


→ $\boxed{R_{L_{min}} = \sqrt{R_f \cdot R_r}}$ — For proper functioning of clamper

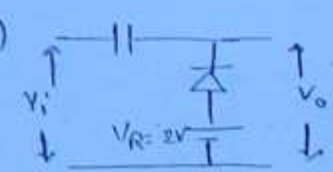
→ During first negative half, capacitor gets charged upto $-V_m$ through FB diode D. The capacitor once charged to $-V_m$, will act as a battery of $-V_m$ and therefore $V_0 = V_i + V_m$.

Ques :- (i)

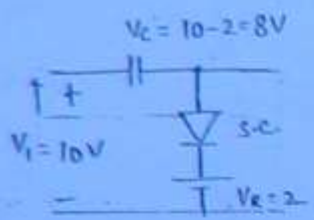


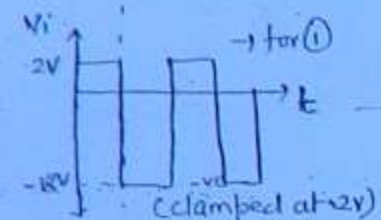


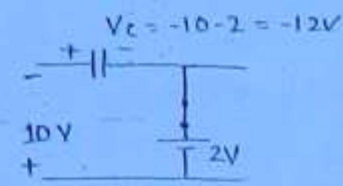
(ii)

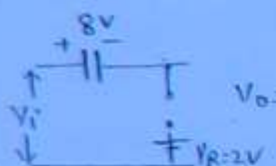


Sol^n

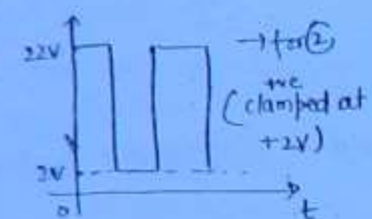


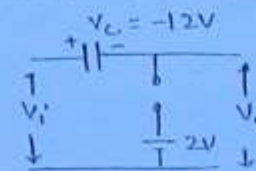






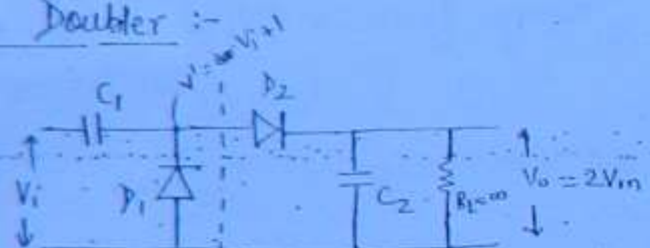
$V_0 = V_i - 8$



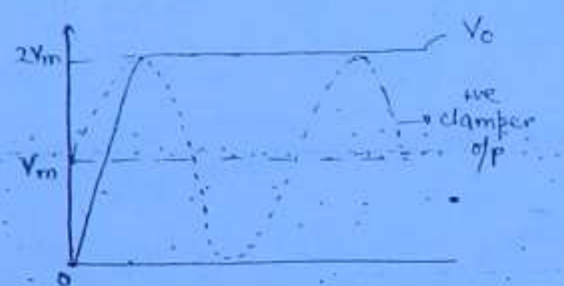


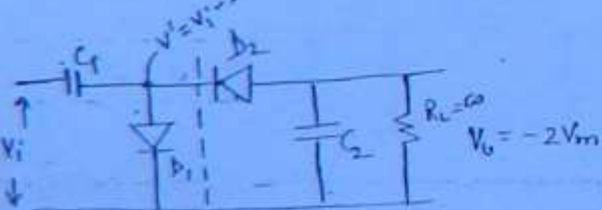
$V_0 = V_i - V_c$
$= V_i + 12$

Voltage Doubler :-

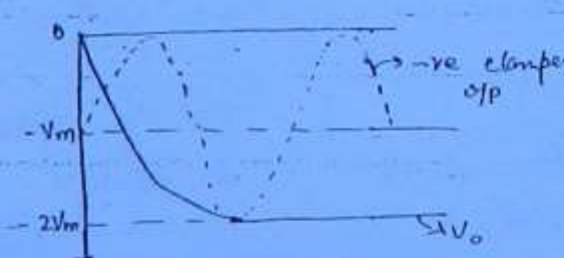


+ve clamper | +ve peak detector





-ve clamper | -ve peak detector.



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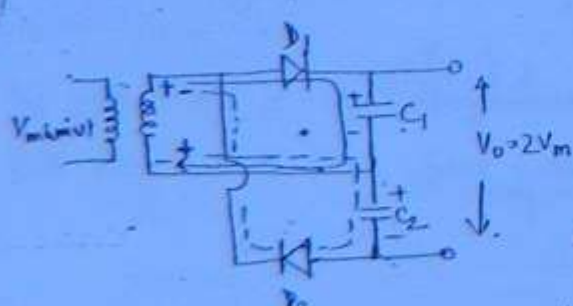


C_1 = will charge till $+V_m$ during +ve half

C_2 = will charge till $+V_m$ during -ve half.

V_p —D1— V_n $\quad V_D = V_p - V_n = V_p - V_m \geq 0$ for FB

Not possible ⇒ $V_p \geq V_m$ for FB of D1 hence D1 & D2 will remain off.

$V_p = -V_m$ —D2— V_n $\quad V_D = V_p - V_n$
$= -V_m - V_n \geq 0 \Rightarrow \underline{V_n \leq -V_m}$ for FB of

Workbook

Pg. 27

(1)

V_i	D_1	D_2	V_o
$V_i < 0$	OFF	OFF	0
$0 \le V_i \le 20$	ON	OFF	$V_i/2$
$V_i \ge 20$	ON	ON	10 V

(9) d

(10) b

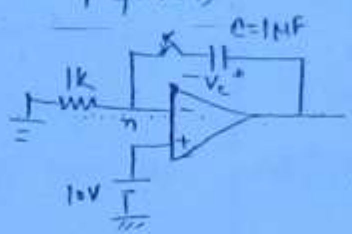
(11) a

(12) d

Chapter 10 Pg. 56

Q7 c, a (c preferred)

(15)



$V_n = 10V$

$V_o = 10 + V_c$.

$\therefore$ Ans 0V → (a).

for V_c = values in option—

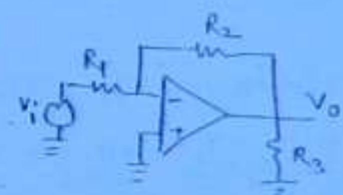
$\therefore V_o = 10V + 0 = 10V$.

$\left\{ \begin{array}{l} V_o = 16.3V \\ V_o = 19.5V \\ V_o = 20V \end{array} \right\}$ ✗ cannot exceed 15V

(18) c (22) c (23) b

(25) (a)

$$\frac{0 - V_i}{R_1} + \frac{0 - V_o}{R_2} = 0 \Rightarrow V_o = -\frac{R_2}{R_1}$$



Conventional

(2) When switch is ON, gain = -1 ; S → OFF, gain = -2.

(3) $R_1 = 3k\Omega$, $R_2 = 2k\Omega$

R = dc resistance seen by inverting terminal; $R = R_1 \| R_2 \| 6K = 1k$

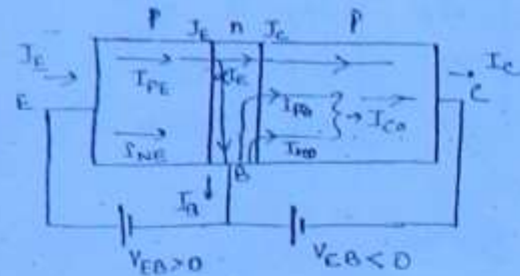
30th August, 2012

Bipolar Junction Transistor :-

p-n-p transistor in active mode :-

$I_E = I_{PE} + I_{NE} \approx I_{PE}$ {Minority carrier injection} → (Diffusion)

(I_{PE} → holes, I_{NE} → e^-)

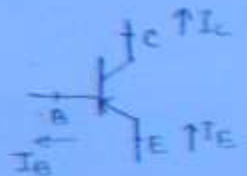


$I_{CO} = I_{PCO} + I_{NCO}$ {Majority carrier inj^n} → (Drift)

* $\boxed{I_C = \alpha I_E + I_{CO}}$; α = large signal current gain or α_{dc}.

(valid only for active ~~current~~ region)

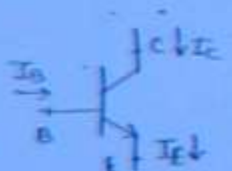
α or $\alpha_{dc} = \dfrac{I_C - I_{CO}}{I_E}$ ⇒ $\boxed{\alpha \approx \dfrac{I_C}{I_E}}$ for CB configuration.



$I_E = I_C + I_B$; $I_C = \alpha I_E$.

(I_E, I_B, I_C = all +ve with this direction)

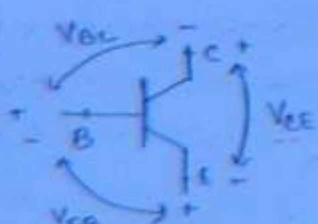
P-n-P

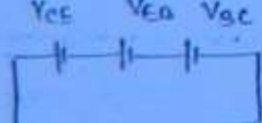


$I_E = I_C + I_B$; $I_C = \alpha I_E$

(I_E, I_B, I_C = all +ve with this direction).

n-p-n





$V_{CE} + V_{EB} + V_{BC} = 0.$ {CEB}

($V_{BE} = -V_{EB}$; $V_{EC} = -V_{CE}$; $V_{CB} = -V_{BC}$).

To

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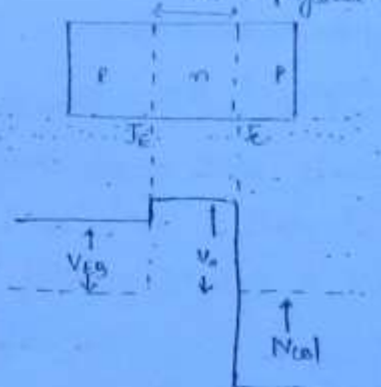
Note:- Guys Be Cool Dude I am here for help You ☺

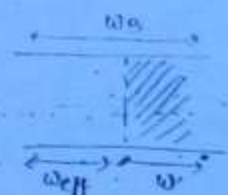
	Common Emitter	(Emitter follower) Common Collector	Common Base
1) Input Terminal	B	B	E
2) Output Terminal	C	E	C
3) Common Terminal	E	C	B
4) Current Gain, A_I	high (moderate)	very high.	very low (< 1)
5) Voltage Gain, A_V	high (moderate)	very low (< 1)	very high
6) Input Resistance, R_i	high (moderate)	very high	very low
7) Output Resistance, R_o	high (moderate)	very low	very high
8) Power Gain ($A_P = A_V \cdot A_I$)	Highest	Moderate	Moderate
9) Phase Shift	180°	0°	0°
10) Normally used as	Amplifier in multistage	Buffer (voltage).	High freq. applicatio Buffer (current)

Early effect / Base width Modulation :-

w_B = physical base width



When collector junc^n is RB —

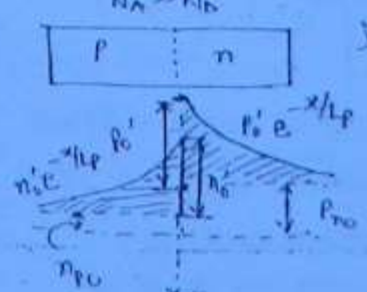


w_{eff} = effective base width = $w_B - w'$

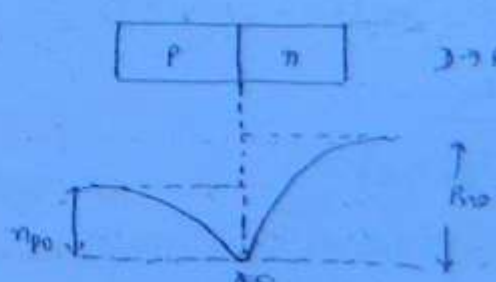
w' = depletion width.

$\therefore$ As $|V_{CB}| \uparrow$; J_C becomes more RB and $w_{eff} \downarrow$, therefore recombination and hence $I_B \downarrow$ and $\alpha \uparrow$.

* $N_A >> N_D$

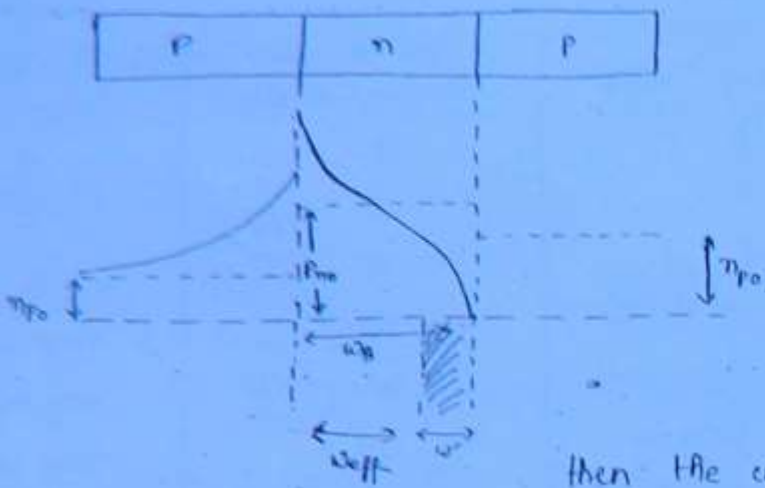


D → FB



D → RB

→ (118)



I_E = diff current

$I_E = qD_P \cdot \frac{dP}{dx}$

$\therefore I_E \propto \frac{dP}{dx} = \frac{dP}{W_{eff}}$

Now, due to early effect, $W_{eff} \downarrow$ and I_E will $\uparrow$. When $W_{eff} = 0$, then the condition is called reach through or punch through. & I_E will be very large.

→ The variation of effective ~~base~~ width with $|V_{CB}|$ is called Base width modulation or early effect. This results in following–

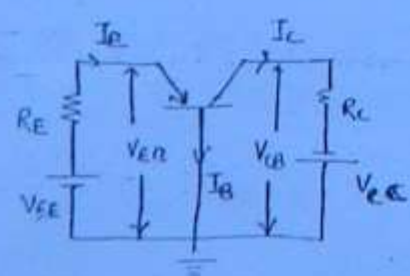
i) There is less chance of recombination in Base region as effective base width reduces. Therefore, $\alpha \uparrow$ causing an $\uparrow$ in collector current I_C.

ii) conc. gradient of injected holes (minority carriers in base region) also $\uparrow$ due to reduced base width. Since, diffusion current is directly proportional to conc. gradient, I_E also $\uparrow$.

iii) for large value of V_{CB}, effective base width may be reduced to 0 causing extremely large I_E. This result in breakdown of transistor and is called punch through or reach through.

Input and Output Characteristics :-

Common Base configuration :-



V_{CB} = –ve
V_{EB} = +ve.

i/p characteristic —

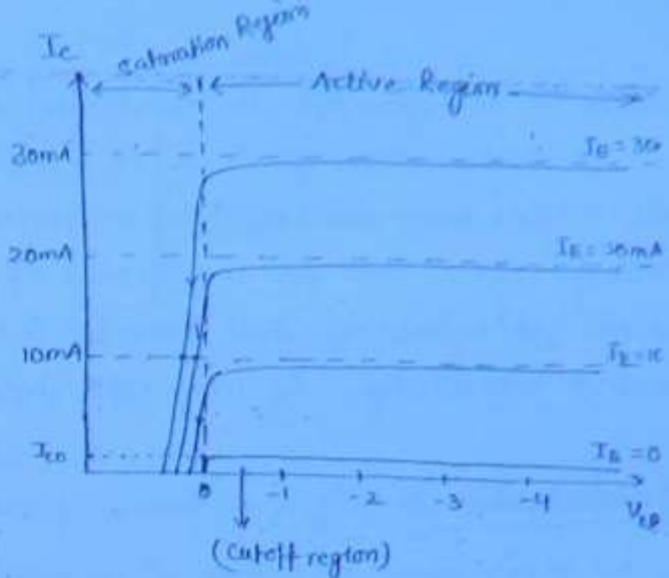
$V_{EB} = f_1(I_E, V_{CB})$

o/p characteristic —

$I_C = f_2(I_E, V_{CB})$

Output characteristic (119)

$I_C = \alpha I_E + I_{C0}$



1) Cutoff Region -

$I_E = 0$; $I_C = I_{C0}$

& $I_C + I_B = I_E \Rightarrow I_B = -I_{C0}$.

2) Active Region :-

$I_C \approx \alpha I_E$ & $\because \alpha < 1 \Rightarrow I_C < I_E$

Now, as $|V_{CB}| \uparrow$, junction is more RB.

& $\alpha \uparrow$ due to early effect. (but the effect is very small).

→ In this region, $I_C \propto I_E$ and is almost constant of V_{CB} variation, hence transistor in this config can be used as CCCS.

3) Saturation Region :-

$\boxed{p}\boxed{n}\boxed{p}$

$\xrightarrow{\alpha I_E}$

$\xleftarrow{I_{C0}[e^{V_{CB}/V_T} - 1]}$

$V_{CB} = +ve$ = since collector junⁿ is FB.

$\therefore I_C = \alpha I_E - \underbrace{I_{C0}\left[e^{V_{CB}/\eta V_T} - 1\right]}_{I_C'}$

(1) $\alpha I_E \approx$ almost constant ; Hence, as $V_{CB} \uparrow$ (+ve value), I' will $\uparrow$ and hence I_C will decrease as $V_{CB} \uparrow$ towards +ve value for constant i/p current.

(2) When ~~we or~~ from circuit, $V_{CB} = -V_{CC} + I_C R_C$.

If we $\uparrow I_E$, then $I_C \uparrow \Rightarrow I_C R_C \uparrow \Rightarrow V_{CB}$ will move towards +ve.

When $|I_C R_C| > |V_{CC}|$, then $V_{CB} = +ve$ → junction J_C = FB.

After this,

when $I_E \uparrow$, → $I_C \uparrow \Rightarrow V_{CB} \uparrow \Rightarrow I' \uparrow$ and $I_C = \overset{(\alpha I_E)\uparrow}{\alpha I_E} - I' \approx$ constant

hence o/p current will not change after this and the transistor will move into saturation.

Important Points :-

- Cutoff → Region below $I_E = 0$.
- Active → I_C is almost independent of o/p voltage V_{CB}.
  - o/p characteristic of CB is called constant current characteristic.
  - It is a CCCS.

- Saturation → The region left to $V_{CB}=0$ and above $I_E=0$.

→ As the collector junⁿ is FB, the holes flow from p-type collector towards n-type base and constitute a current I' in a direction opposite to direction of $+I_C$. Even for small value of $+V_{CB}$, large change in I_C take place and characteristics fall towards 0 as V_{CB} is made more & more +ve. Since, $I' \uparrow$ exponentially, I_C may even become -ve.

Input Characteristics :-

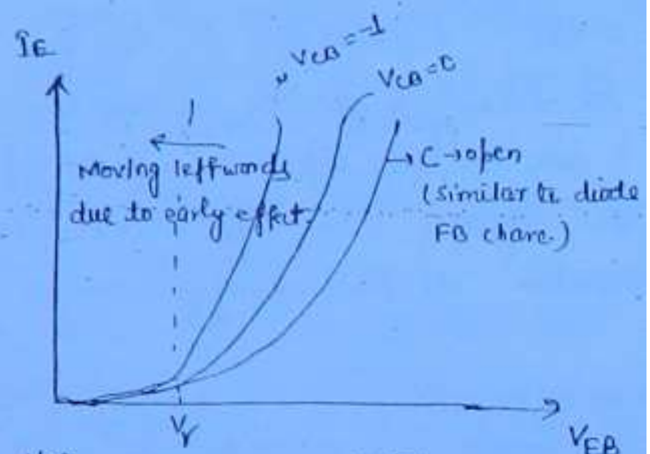
$V_{EB} = f(I_E, V_{CB})$.

When $V_{CB} = \infty$, i.e., C-B → O.C. then chare will be similar to diode.

When $V_{CB}=0$, J_C = slightly RB.

Due to early effect, $I_E \uparrow$ more rapidly.

Now, As $V_{CB}\uparrow$, more early effect



(OR)

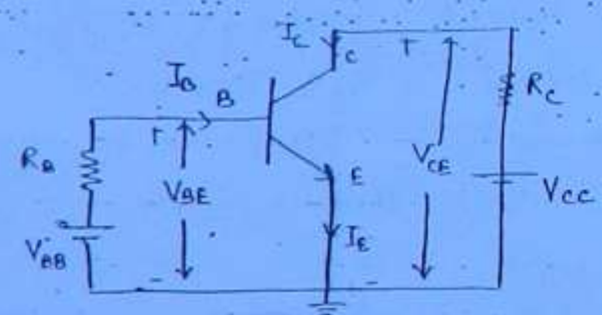
II) COMMON EMITTER CONFIGURATION :-

i/p charc –

$V_{BE} = f_1(I_B, V_{CE})$.

o/p charc –

$I_C = f_2(I_B, V_{CE})$.

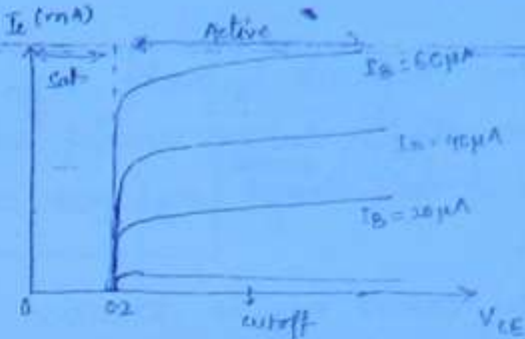


$I_C = \alpha I_E + I_{CO}$

$\Rightarrow I_C = \alpha(I_C + I_B) + I_{CO}$

$\Rightarrow \boxed{I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \frac{I_{CO}}{(1-\alpha)}}$ or $\boxed{I_C = \beta I_B + (\beta+1) I_{CO}}$; $\boxed{\beta = \frac{\alpha}{1-\alpha}}$

$\Rightarrow \beta \gg \alpha$.



Output Characteristic :-

Active Region

- $I_c = \beta I_B + (\beta+1) I_{co} \approx \beta I_B$.
- $V_{CE} = V_c - V_E = V_c$.

As $V_{CE} \uparrow \Rightarrow V_c \uparrow \rightarrow J_c$ more RB $\Rightarrow$ width $\downarrow$ & $\alpha \uparrow$

Now, $\alpha \rightarrow 0.98 \rightarrow 0.985 \rightarrow 0.5\% \uparrow$

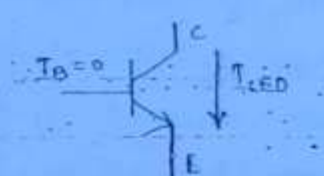
$\beta \rightarrow 49 \rightarrow 63 \rightarrow 34\% \uparrow \rightarrow$ can't be neglected.

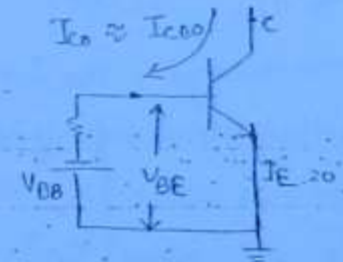
$\rightarrow$ current gain is high, i.e, small change in I_B results in large change in I_c

Cutoff Region

- When $I_B = 0$, $I_c = (\beta+1) I_{co}$ $\rightarrow I_c \neq I_{co}$ and hence transistor is not in cut off.
- $\boxed{I_{CEO} = (\beta+1) I_{co} = \frac{I_{co}}{1-\alpha}}$ $\boxed{I_{CEO} >> I_{co}}$, $\because \beta >> 1$.

- Now, for $I_c = I_{co}$; I_E should be 0.
- When $I_E = 0$





$\boxed{I_{CEO} >> I_{CBO} > I_{co}}$

- The I_c in a physical (real & non-idealised) device when $I_E = 0$ is designated by symbol I_{CBO}.
- Cutoff is defined as a condition where $I_c = I_{co}$ and $I_E = 0$. In order to cutoff transistor, it is not enough to reduce I_B to 0, instead it is necessary to RB the emitter junc^n slightly, i.e, $V_{BE} = -ve$.

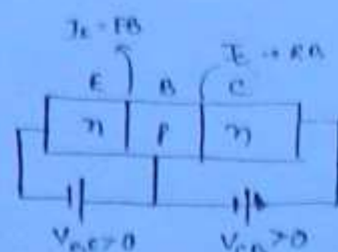
$$V_{BE} = -0.1 \text{ for Ge} ; 0.0 \text{ for Si}.$$

- The actual I_c with collector junc^n RB & base o.c is designated by symbol I_{CEO}.
- I_{CBO} = reverse collector saturation current.

- Two factors cooperate to make I_{CBO} larger than I_{CO} –
  a) There exist a leakage current which flows not through junc^n, but around it and ~~through~~ across surfaces and it is $\propto$ to voltage across the junc^n.
  b) New carrier may be generated by collision in J_C transition region leading to avalanche multiplication of current.
- I_{CBO} = μA for Ge
  nA for Si.
- I_{CBO} approximately doubles for every 10° rise in temp for both Ge & Si and Si can be used upto about 200°C and Ge upto about 100°C.

31st August, 2012 :

- Saturation :-



→ $J_E \to FB$, $J_C \to RB$.

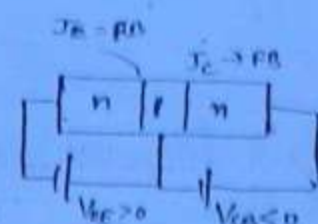
→ $I_C = \beta I_B$; $V_{CE} = V_{CC} - I_C R_C$ (from ckt).

→ When we $\uparrow V_{BE}$, then $I_B \uparrow$ (due to barrier lowering) , then $I_C\uparrow$ and $V_{CE}\downarrow$.

→ When $V_{BE} = 0.8V$ & $V_{CE} = 0.2V$ and is constant for further $\uparrow$ in V_{BE}.

$$\therefore V_{CEsat} = 0.2V$$

$$I_{Csat} = \frac{V_{CC} - V_{CEsat}}{R_C}$$



Now, $V_{CE} + V_{EB} + V_{BC} = 0 \Rightarrow V_{CE} - V_{BE} + V_{CB} = 0$

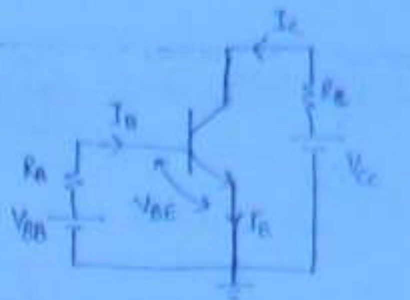
$$\Rightarrow V_{CB} = 0.2 - 0.8 = -0.6V.$$

$\therefore$ Now , J_C = FB . and a reverse current will start flowing which will oppose I_E and the ~~diode~~ Transistor will go into saturation
$\{ I' = I_{CO} [e^{V_{CB}/\eta V_T} - 1] \}$

→ If V_{BE} = kept constant and V_{CC} is changed –
When $V_{CC}\downarrow$, $\Rightarrow$ $V_{CE}\downarrow$

$V_{CB} = V_{CE} - V_{BE}$ ⇒ $V_{CB}\downarrow$ and when it is –ve then $J_C \to FB$.
Hence, ~~Transistor~~ will be in saturation.

Checking Transistor for saturation :-



123

* Let Q is in saturation.

Then $V_{CE} = V_{CEsat}$ & $V_{BE} = V_{BEsat}$

$$\therefore I_{Csat} = \frac{V_{CC} - V_{CEsat}}{R_C}$$

and $\because I_C = \beta I_B \Rightarrow I_{Csat} = \beta I_{Bmin} \Rightarrow \boxed{I_{Bmin} = \frac{I_{Csat}}{\beta}}$

Now, if $I_B \geq I_{Bmin}$, then transistor is in saturation.

$$I_B = \frac{V_{BB} - V_{BEsat}}{R_B}$$

To bring transistor in saturation —

1) Increase I_B by $\uparrow V_{BB}$ so that $I_B = I_{Bmin}$

2) If I_B = constant, then $\downarrow I_{Bmin}$ so that $I_{Bmin} = I_B$ by $\downarrow V_{CC}$ and/or $\uparrow R_C$.

3) If I_B = constant & I_{Csat} = constant, then $\uparrow \beta$ so that $I_{Bmin} = I_B$.

At $\beta = \beta_{forced}$,

$$I_{Bmin} = \frac{I_{Csat}}{\beta_{forced}} = I_B \Rightarrow \boxed{\beta_{forced} = \frac{I_{Csat}}{I_B}}$$

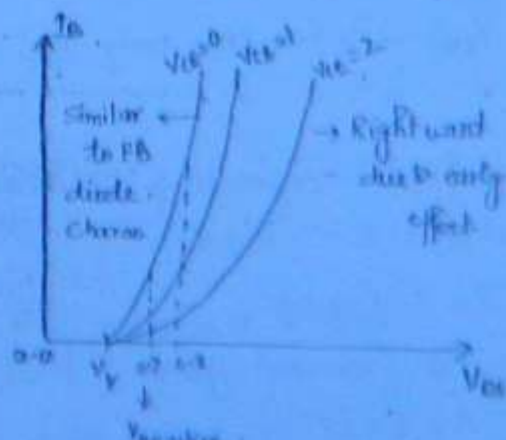
Important Points for saturation —

→ Both J_E & J_C are FB by cutin voltage V_γ.

→ If a transistor has to be operated in saturation region, we should design the ckt, so that $I_B > I_{Bmin}$ by a factor of 2 to 10.

→ The ratio of I_{Csat} & I_B to ensure saturation is called forced β.

Input Characteristic :-

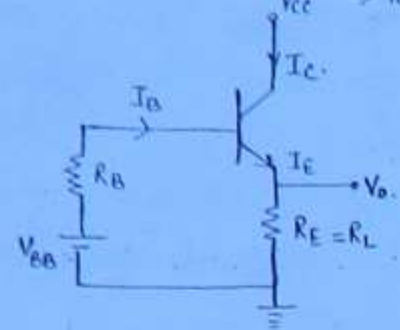


→ $V_{BE} = f(I_B, V_{CE})$.

When $V_{CE} = 0$, i/p char. similar to diode

When $V_{CE} \uparrow \Rightarrow V_C \uparrow$ {$\because V_E = 0$} and due to early effect (V_{CB} more RB), $I_B \downarrow$.

III Common Collector Configuration



I/p char. :-

$V_{BC} = f(I_B, V_{EC})$

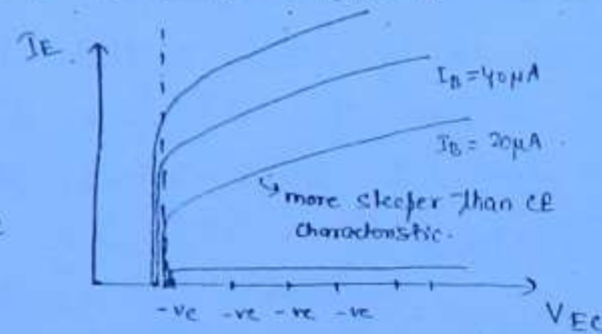
o/p char. :

$I_E = f(I_B, V_{EC})$

Output characteristic :

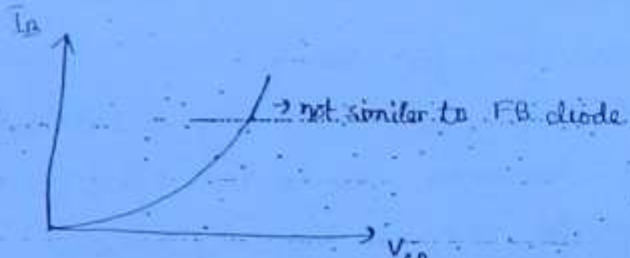
$I_c = \beta I_B + (1+\beta) I_{co}$

$\Rightarrow I_E - I_B = \beta I_B + (1+\beta) I_{co} \Rightarrow I_E = (1+\beta) I_B + (1+\beta) I_{co} \simeq (1+\beta) I_B$

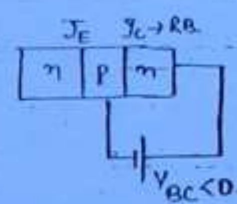


- When $V_{EC}\downarrow$ (-ve), $V_{CE}\uparrow$ & J_c is more RB.
  & due to early effect $\alpha\uparrow$ and $\beta\uparrow$.
- Curve is more steeper than CE config. since $(\beta+1)$ varia^n is > β varia^n.

Input Characteristic



→ I/p characteristic is not similar to forward biased diode charac. since it is taken across RB junction.



→ $V_{BC}\uparrow \Rightarrow V_{CB}\downarrow \Rightarrow J_c$ less RB, early effect ↓ & $I_B\uparrow$.

Important points regarding CC config. :-
- Highest R_i (50kΩ – 500kΩ)
- Lowest R_o (< 100 Ω)
- Highest A_i (current gain) ; $|A_I| = \dfrac{I_E}{I_B} = (1+\beta)$ { lowest for CB = α ; Moderate " CE = β. }
- lowest A_V (< 1) ; typical value = 0.98. Max. $A_V = 1$ (ideal cond^n), hence it
- is also called emitter follower.
- It is basically CCVS.

- Emitter follower is analogous to voltage follower in Op-amp and source follower in FET.

Voltage follower & source follower are VCVS. (125)

lowest Power gain ; Typical value = 48.

Phase shift = 0°.

Application —

i) Highest i/p resistance device.

ii) As a buffer amplifier, i.e, an impedance matching device b/w high resistance & low resistance device.

iii) As an audio freq. power amplifier

mportant Points for CB configuration:-

- lowest R_i $(<100\Omega)$
- Highest R_o $(>1M\Omega)$
- Lowest A_I $(=\alpha)$
- Highest A_V
- Moderate A_P : typical value = 68
- Phase shift = 0°
- CB amplifier will offer largest bandwidth & hence more suitable for high freq. applications.

Application —

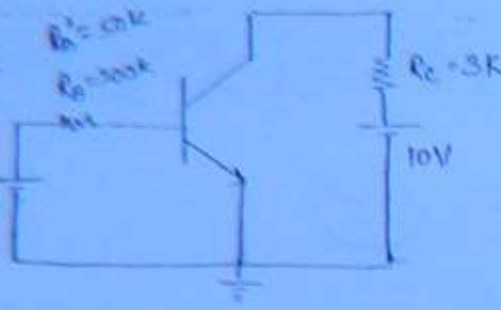
(i) As a constant current source

ii) As an non-inverting voltage amplifier

iii) As a high frequency amplifier

iv) As an impedance matching device b/w low resistance & high resistance.

Ques :



find transistor currents in ckt.
$\beta = 100$, $I_{CO} = 20nA$, Si transistor.

(126)

* Typical Junc^n voltages for npn transistor at 25°C –

	Si	Ge
$V_{CE\,sat}$	0.2	0.1
$V_{BE\,sat} = V_\sigma$	0.8	0.3
$V_{BE\,active}$	0.7	0.2
$V_{BE\,cutin} = V_\gamma$	0.5	0.1
$V_{BE\,cutoff}$	0.0	−0.1
$V_{CE\,active}$ ($V_{EC\,active}$ for pnp)	>0.2	>0.1

* For pnp transistor, sign of all the entries should be reversed.

Sol^n – ① $R_B = 200k\Omega$.

$\because V_{BB} = +ve = 5V \Rightarrow V_{BE} = +ve \Rightarrow J_E = FB.$

let Tr is in active region –

$I_C = \beta I_B + (1+\beta) I_{CO}$

$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5 - 0.7}{200k} = 0.0215\ mA.$

$I_C \simeq \beta I_B = 2.15mA.$

$V_{CE} = 10 - 3K \cdot I_C \Rightarrow V_{CE} = 10 - 3 \times 2.15 = 3.55V >> 0.2V$ hence, transistor is in active region.

Alternatively, $V_{CB} = V_{CE} - V_{BE}$
$= 3.55 - 0.7$
$= 2.85V \Rightarrow$ junction is definately RB.

② $R_B = 50K$.

$I_B = \frac{5 - 0.7}{50} = 0.086\ mA$

$\therefore I_C = 8.6mA \Rightarrow V_{CE} = 10 - 3K(8.6) = -15.8 < 0.2 \Rightarrow Tr \Rightarrow$ saturation.

our assumption was wrong

$\therefore V_{BE} = V_{BEsat} = 0.8$
$V_{CE} = V_{CEsat} = 0.2$
$\therefore I_{Csat} = \frac{10 - 0.2}{3k} = 3.27mA$ Ans
$I_B = \frac{5 - 0.8}{50k} = 0.084mA$ Ans

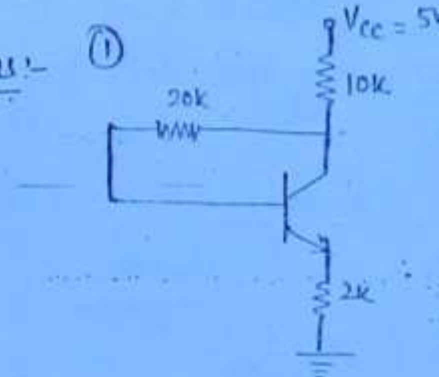
* $\boxed{\text{Overdrive factor} = \frac{I_B}{I_{Bmin}}}$

Eg $I_{Bmin} = \frac{3.27\,mA}{100} = 0.0327\ mA.$

127

overdrive factor $= \frac{0.084}{0.0327} = 2.5$ times → Hence, transistor is well in saturatio

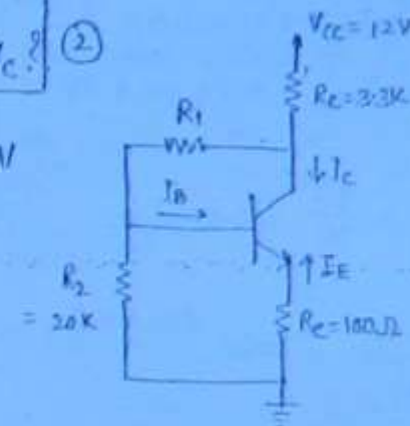
Ques:- (1)



$\beta = 75$, Si diode find V_C?

Ans:- $I_B = 4.61\,\mu A$
$V_C \approx 1.49V$

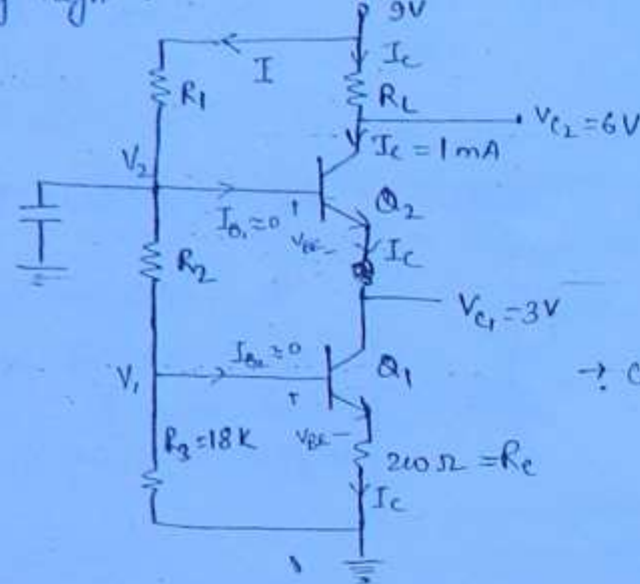
(2) If $\alpha = 0.98$ and $V_{BE} = 0.7\,V$ find R_1 in circuit for an emitter current $I_E = -2mA$ Neglect reverse sat. current.



Soln.

~~Early Voltage~~:-

Ques In the given ckt, determine the value of R_1, R_2 and R_L so that collector current through the transistor is 1mA. $V_{C_1} = 3V$, $V_{C_2} = 6V$. Take $V_{BE} = 0.7V$. and let β of transistors are very high.



→ Cascode Amplifier

Sol^n. $V_1 = V_{BE} + I_c R_E$

$V_1 = 0.7 + 0.2 \times 1 = 0.9V$

$V_2 = V_{BE} + V_{CE_1} = 0.7 + 3 = 3.7V$

$I = \dfrac{V_1}{R_3} = \dfrac{0.9}{18} = 0.05\,mA$

$\therefore R_1 = \dfrac{9 - V_2}{I} = 106K$

$R_2 = \dfrac{V_2 - V_1}{I} = 56K.$

$- R_L = \dfrac{9-6}{1mA} = 3K.$

$\left\{ \because \beta = \text{very high} \Rightarrow \alpha \simeq 1 \right.$
$\left. \Rightarrow I_C \approx I_E \;\&\; I_B \approx 0 \right\}.$

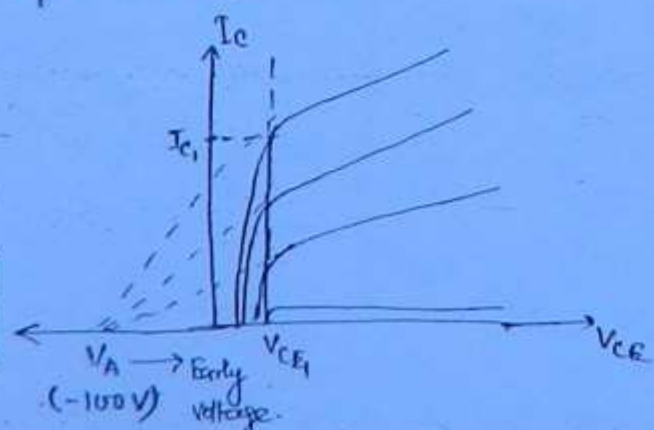
Early Voltage:-

- It helps in finding o/p resistance of transistor.

$\vec{\text{Slope}} = \dfrac{I_{C_1} - 0}{V_{CE_1} - (-V_A)} = \dfrac{I_{C_1}}{V_{CE_1} + V_A} \simeq \dfrac{I_{C_1}}{V_A} = \dfrac{1}{r_o}$

→ $|V_A| \gg V_{CE1}$

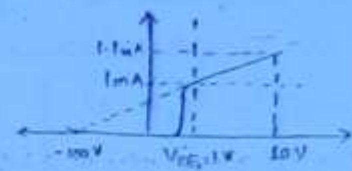
→ $\boxed{r_o = \dfrac{V_A}{I_{C_1}} = \text{o/p resistance of ckt}}$



→ V_A = very high for CB. ⇒ r_0 = very high. ≈ MΩ
→ V_A for CC is slightly less than V_A of CE. ⇒ $r_{occ} < r_{oce}$
→ $V_{ACB} \gg V_{ACE} > V_{ACC}$ or $r_{ocb} \gg r_{oce} > r_{occ}$

03rd September, 2012

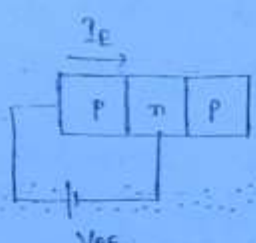
Ques: In a CE transistor, at $V_{CE} = 1V$, V_{BE} is adjusted to give a collector current of 1mA. Keeping V_{BE} constant, V_{CE} is ↑ to 11V. Find new value of I_C if $V_A = 100V$.

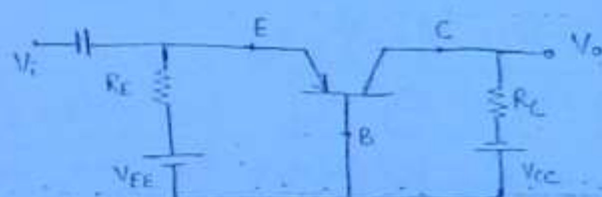


Soln: $\frac{0 - 1mA}{-100 - 1} = \frac{x - 1}{11 - 1}$

$\Rightarrow \frac{+10}{101} = x - 1 \Rightarrow$ ~~x = 99/34~~ $x = \frac{111}{101} = 1.09\ mA$.

Transistor as an Amplifier :-





* $r_e = \frac{\eta V_T}{I_E} = \frac{V_T}{I_E}$ [dynamic resistance or incremental resistance]

→ Transistor is in active region
$J_C \to FB$, $J_E \to RB$
$I_C = \alpha I_E + I_{C0} \cong \alpha I_E$.

AC analysis –

On applying signal at V_i. If V_i ↑ by ΔV_i, then I_E ↑ by ΔI_E & I_C also increases.

$$I_C + \Delta I_C = \alpha [I_E + \Delta I_E]$$

$$\Rightarrow \boxed{\Delta I_C = \alpha \Delta I_E}$$

Now, V_o will also ↑, ⇒ $\Delta V_o = \Delta I_C \cdot R_C$ ⇒ $\Delta V_o = \alpha \Delta I_E \cdot R_C$.

Change in i/p, $\Delta V_i = \Delta I_E \cdot r_e$.

∴ Voltage gain, $A_V = \frac{\Delta V_o}{\Delta V_i} \Rightarrow \boxed{A_V = \frac{\alpha R_C}{r_e} \approx \frac{R_C}{r_e}}$ {for α ≈ 1}

→ Power gain will also be ↑.
⇒ $A_V \gg 1$ → Hence, amplifier

→ Transistor provides power gain as well as voltage or current amplification. Current in low resistance i/p ckt is transferred to high resistance o/p ckt. The word transistor which originated as a contraction of transfer resistor is based upon above physical picture of device.

130

Photo Transistor :- (Photo-duo-diode)

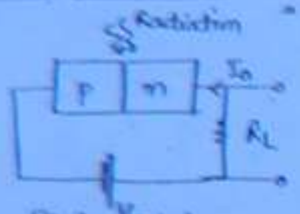


Photo Diode

I_0 : Reverse saturation current

Due to radiation T↑ ; I_0 ↑es by ΔI_0

V_0 also increases by ΔV_0 ∴ $\Delta V_0 = \Delta I_0 . R_L$

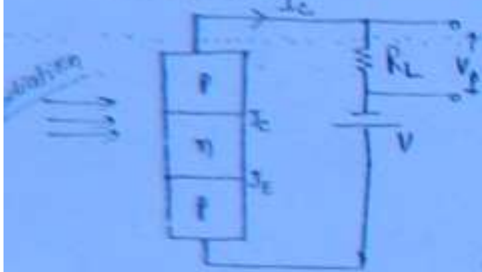


Photo Transistor

$J_E \rightarrow FB$, $J_C \rightarrow RB$ ⇒ $\boxed{\text{Photo transistor is in active region}}$

$I_C = \beta I_B + (1+\beta) I_{C0}$ but $I_B = 0$, since base is open

⇒ $I_C = (1+\beta) I_{C0}$

Now, due to radiation , T↑ ; I_{C0}↑ ; I_C↑ by ΔI_C.

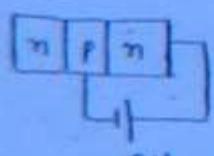
$$\Delta I_C = (1+\beta)\, \Delta I_{C0}$$

V_0 ↑es by : $\Delta V_0 = \Delta I_C . R_L$ ⇒ $\boxed{\Delta V_0 = (1+\beta) \Delta I_{C0} . R_L}$

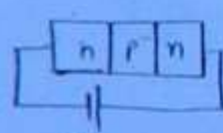
Therefore, Photo transistor is more sensitive than photo diode by a factor $(1+\beta)$.

Maximum Voltage rating of Transistor :-

1) Avalanche Multiplication :-



BV_{CBO}



BV_{CEO}

$\boxed{BV_{CBO} > BV_{CEO}}$

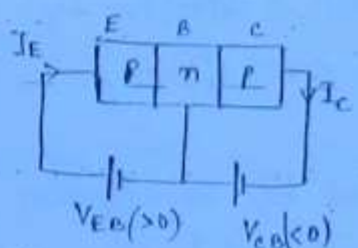
- BV_{CBO} → maximum reverse biasing voltage which may be applied before breakdown b/w C & B of transistor, keeping E open., i.e., $I_E = 0$.

- $-BV_{CEO} \rightarrow$ For CE configuration, collector to emitter breakdown voltage with open circuit base.

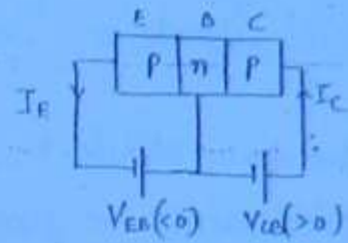
Note.

- In a particular transistor, voltage limit is determined by punch-through or breakdown (due to avalanche multiplication) whichever occur at the lower voltage.

Ebers Moll Model :-



(Forward or Normal Active mode)
(α_F or α_N)



(Reverse or Inverse Active Mode)
(α_I)

$J_E \rightarrow FB$, $J_C \rightarrow RB$

$$\boxed{I_C = \alpha_N I_E + I_{CO}} \quad \text{—} (1)$$

$J_E \rightarrow RB$, $J_C \rightarrow FB$.

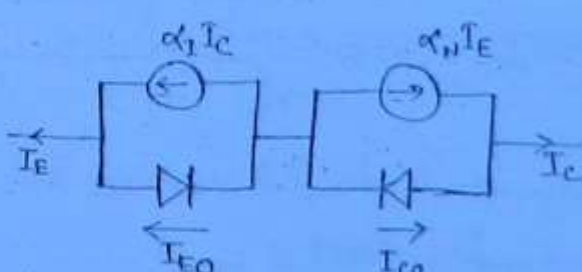
$$\boxed{I_E = \alpha_I \cdot I_C + I_{EO}} \quad \text{—} (2)$$

$\rightarrow$ parameters $\alpha_N, \alpha_I, I_{CO}, I_{EO}$ are not independent (experimentally).
They depend on each other as $\boxed{\alpha_N \cdot I_{EO} = \alpha_I \cdot I_{CO}}$

$\rightarrow$ $I_{EO} = 0.5 I_{CO}$ to I_{CO} } i.e, $I_{EO} < I_{CO}$ as conc. of E $\geq$ conc. of C
$\Rightarrow$ conc. of minority in E < conc. of minority in C
($\Rightarrow I_{EO} \leq I_{CO}$)

$\rightarrow$ $\dfrac{\alpha_N}{\alpha_I} = \dfrac{I_{CO}}{I_{EO}} \Rightarrow \boxed{\alpha_N \geq \alpha_I}$ **

$\rightarrow$



Ebers Moll Model

Now, if $\alpha_I = \alpha_N = 0$;
then

→ Model involves two ideal diodes placed back to back with reverse saturation current I_{Co} & I_{Eo} and two dependent cccs shunting ideal diodes. (132)

→ Observe from the figure that, dependent current source can be eliminated from this figure provided $\alpha_I = \alpha_N = 0$. For eg., by making base width much larger than diffusion length of minority carrier in base, then all minority carriers will recombine in base and none will survive to reach collector. for this case current gain α will be 0. Under this condition transistor action ceases. and we simply have two diodes placed back to back.

→ This discussion shows why it is impossible to construct a transistor by simply connecting two separate or isolated diode in series opposing.

→ A cascade of two p-n diode exhibits transistor properties like amplification only if carrier injected across one juncn diffuse across 2nd junction.

Cutoff Mode:

J_E & J_C → RB. ⇒ $I_E = 0$.

from eqn ① –

$$\boxed{I_C = I_{Co}}$$

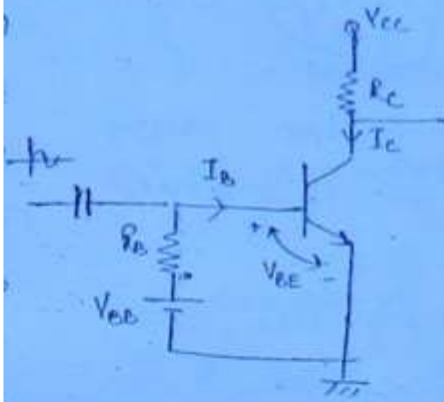
Saturation

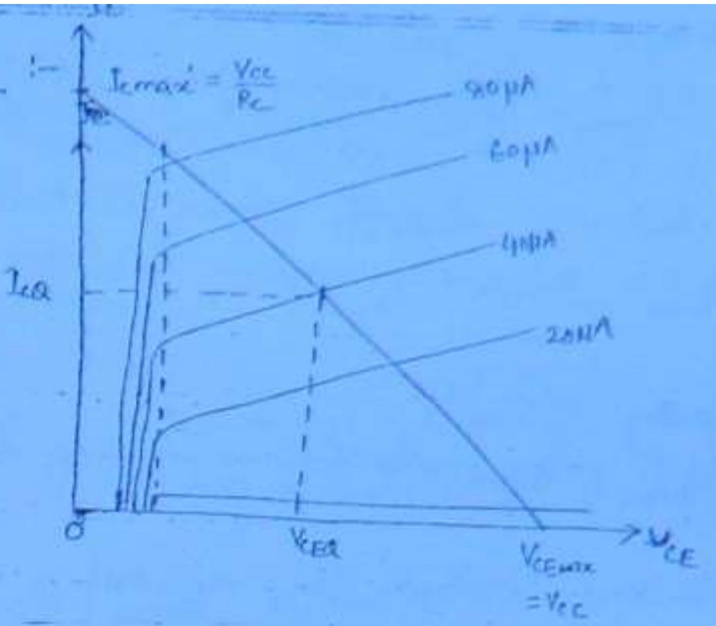
J_E & J_C → FB.

From eqn ① –

$$\boxed{I_C = \alpha_N I_E - I_{Co}\left[e^{V_{CB}/V_T} - 1\right]}$$

Transistor Biasing and Stablization :-





- $J_E \to FB$, $J_C \to RB$.

- $I_B = \dfrac{V_{BB} - V_{BE}}{R_B}$ — ①

- $I_C = \beta I_B + (1+\beta) I_{CO}$

- $V_{CE} = V_{CC} - I_C R_C$ — ② $\Rightarrow I_C R_C = V_{CC} - V_{CE} \Rightarrow I_C = -\dfrac{V_{CE}}{R_C} + \dfrac{V_{CC}}{R_C}$ — ③ ↳ DC load line.

Eqn (3) is similar to $y = mx + c$; slope $= -1/R_C$

When, $V_{CE} = 0$, $I_{Cmax} = \dfrac{V_{CC}}{R_C}$

When $I_C = 0$, $V_{CEmax} = V_{CC}$

from eqn (1) ; set $I_B = 40\mu A$, then

$$\boxed{\beta = \frac{I_{CQ}}{I_B}}$$

→ Q = Quescient Point / Operating point.

→ $Q = f(I_B, I_C, V_{CE})$.

On application of input –

$I_b = \underset{(DC)}{I_B} + \underset{(AC)}{i_b} \Rightarrow I_C' = \beta I_b = \beta(I_B + i_b) = I_C + i_c$

Eg①: Now, let $I_B = 40\mu A$ & $i_b = 20\sin\omega t\,\mu A$, then $I_b = 40 + 20\sin\omega t$

$\therefore I_{bmax} = 60\mu A$, $I_{bmin} = 20\mu A$

Hence, Q point lies well within the active region. Therefore, no distortion in the output.

Eg 2) $I_B = 40\mu A$, $i_b = 40 \sin \omega t$
$\therefore I_{bmax} = 80\mu A$, $I_{bmin} = 0$

Hence, transistor is just in active region.

Eg 3. $I_B = 40\mu A$, $i_b = 50 \sin \omega t$

$I_{bmax} = 90\mu A$, $I_{bmin} = -10$, Now, there will be distortion in the o/p.

Eg 4. Adjusting $I_B = 20\mu A$, $i_b = 20 \sin \omega t$
$I_{bmax} = 40\mu A$, $I_{bmin} = 0\ A$

Eg 5. $I_B = 20\mu A$, $i_b = 40 \sin \omega t$
$I_{bmax} = 60$, $I_{bmin} = -20$ → cutoff

Eg 6. $I_B = 60\mu A$, $i_b = 30 \sin \omega t \Rightarrow I_{bmax} = 90$ → saturation , $I_{bmin} = 30$

Important Points:

- The collector charc or o/p charc of transistor is divided into saturation, cutoff and active regions.
- Transistor can work as a switch when operated in saturation and cutoff region, ie, extreme ends of the characteristics.

- Procedure to plot DC load line & Q point -

1) Identify the value of V_{cc} & I_{cmax} of the circuit & locate this point on given charac.
2) Draw a straight line joining I_{cmax} & V_{cc} & this straight line is called dc load line.
3) Find the operating values I_B, I_C & V_{CE} for the given ckt & locate these values on given charac.
4) Project three operating values on dc load line & the intercepting point is called Q-point.

- The transistor is said to be under quiescent condn when zero i/p signal is applied.

→ Transistor can work as an amplifier if Q point is within active region but Q point is temp. sensitive, i.e., as T ↑, I_C ↑ and V_{CE} ↓, so that Q point will be moving towards saturation region and if entered into saturation region, transistor will stop working as an amp.

135

→ Trans. will provide more power gain or amplification, when Q point is in middle of dc load line.

→ for a given trans., Q point is plotted to get faithful reproduction of i/p signal.

→ If shape of o/p signal differs from shape of i/p signal, it is said to be distorted.

→ for a stable circuit, the variation in Q-point due to temp. must be small.

Bias Stability:-

- Stability is effected due to —

1) Temp. Instability

(a) I_{CO} → It doubles for every 10° rise in temp.

$T\uparrow \Rightarrow I_{CO}\uparrow \Rightarrow I_C\uparrow \Rightarrow$ Q point shift towards saturation.

(b) V_{BE} →

$$\frac{dV_D}{dt} = -2.5\,mV/^\circ C, \quad \text{similarly} \quad \frac{dV_{BE}}{dt} = -2.3\,mV/^\circ C.$$

$$\therefore I_B = \frac{V_{BB} - V_{BE}}{R_B}$$, As T ↑, V_{BE} ↓, $I_B \uparrow \Rightarrow I_C \uparrow$ & V_{CE} ↓ ⇒ Q → saturation.

Note - β ↑ with temp but change is negligible.

2) Replacement of Transistor — β is highly affected due to replacement of transistor.

(∵ Since small change in α results in large change in β).

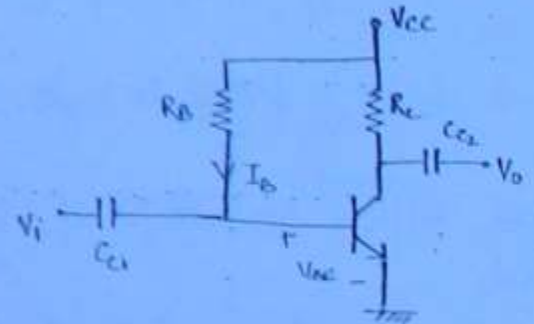
Stablisation Techniques

Biasing Techniques
(1) C-B Biasing.
(2) Self-Biased

Compensation Techniques
(1) Diode compensation
(2) Sensistor & Thermistor compensation.
(3) Transistor compensation

Fixed Biased circuit :-

→ $I_B = \dfrac{V_{CC} - V_{BE}}{R_B}$ = constant

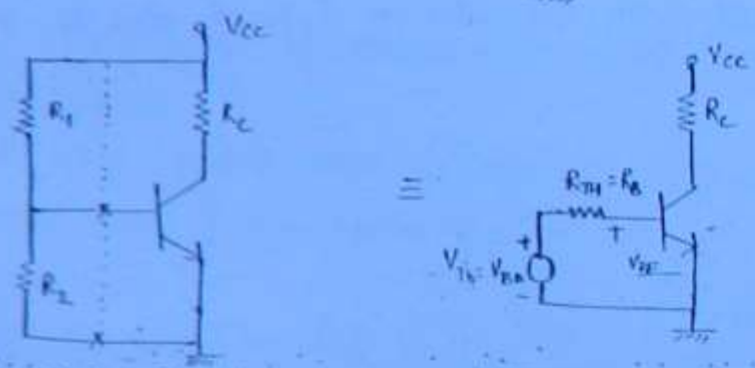


⇒ (Unstable)

→ $V_{TH} = \dfrac{R_2}{R_1 + R_2} \cdot V_{CC}$

$R_{TH} = R_1 \parallel R_2$

Normally,
$R_1 \cong 10 R_2$
ie, $R_1 \gg R_2$



→ (Unstable)

$I_B = \dfrac{V_{BB} - V_{BE}}{R_B}$ (= constant)

Stability factors :-

→ $\boxed{S = \left.\dfrac{dI_C}{dI_{CO}}\right|_{V_{BE} \,\&\, \beta = \text{constant}}}$

→ $\boxed{S'' = S_\beta = \left.\dfrac{dI_C}{d\beta}\right|_{I_{CO} \,\&\, V_{BE} = \text{constant}}}$

→ $\boxed{S' = \left.\dfrac{dI_C}{dV_{BE}}\right|_{I_{CO} \,\&\, \beta = \text{constant}} = S_V}$

* As T↑, I_{CO}↑, I_C↑ ⇒ $S = +ve$

As T↑, V_{BE}↓, I_C↑ ⇒ $S' = S_V = -ve$

As ~~T↑~~, β↑, I_C↑ ⇒ $S'' = +ve$

(because of replacement)
(not bcoz of temp)

Stability Factor, S :-

$$S = \left.\frac{dI_C}{dI_{CO}}\right|_{V_{BE}\ \&\ \beta = \text{constant}}$$

(137)

In active region,

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

$$\Rightarrow \frac{dI_C}{dI_{CO}} = \beta \cdot \frac{dI_B}{dI_{CO}} + (1+\beta)$$

$$\Rightarrow \frac{dI_C}{dI_{CO}} = \beta \cdot \frac{dI_B}{dI_C} \cdot \frac{dI_C}{dI_{CO}} + (1+\beta)$$

$$\Rightarrow \frac{dI_C}{dI_{CO}} \left[1 - \beta \cdot \frac{dI_B}{dI_C}\right] = (1+\beta)$$

$$\Rightarrow \boxed{S = \frac{1+\beta}{1 - \beta \cdot \frac{dI_B}{dI_C}}}$$

→ If I_B = constant, $\frac{dI_B}{dI_C} = 0 \Rightarrow \boxed{S = (1+\beta)}$ → ckt is unstable → Eg. fixed Biase

→ If $I_C \uparrow$ then I_B should $\downarrow$, i.e., $dI_B/dI_C < 0$. In ideal case,

$$\frac{dI_B}{dI_C} = -1 \Rightarrow \boxed{S = 1} \rightarrow \text{Highly stable.}$$

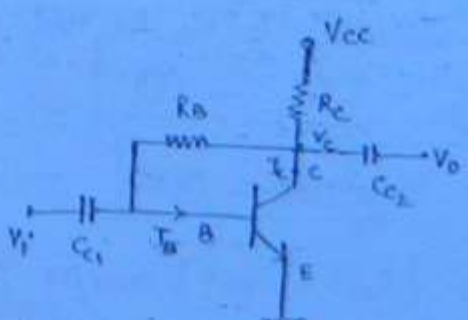
→ For $\boxed{S < 1+\beta}$ → circuit is stable

→ Range of S → $\boxed{1 \leq S \leq (1+\beta)}$ **

Techniques :-

1) Collector - Base Bias -

→ During DC analysis, C_{C_1} & C_{C_2} will act as open circuit.



When transistor is in active region –

$$I_C = \beta I_B + (1+\beta) I_{CO} \quad — ①$$

On manipulating ① –

$$S = \frac{dI_C}{dI_{CO}} = \frac{1+\beta}{1-\beta \cdot \frac{dI_B}{dI_C}} \quad — ②. \qquad (\text{Keeping } V_{BE} \text{ \& } \beta \text{ constant})$$

Applying KVL at i/p – $V_{CC} = (I_C + I_B) R_C + I_B R_B + V_{BE}$

Differentiating w.r.t I_C – $0 = (R_C + R_B)\frac{dI_B}{dI_C} + R_C + 0$

$$\Rightarrow \frac{dI_B}{dI_C} = \frac{-R_C}{R_C + R_B} \quad — ③$$

Substituting ③ in ② –

$$S = \frac{1+\beta}{1 + \frac{\beta R_C}{R_C + R_B}} < (1+\beta) \quad \text{Hence circuit is Stable.}$$

$$\Rightarrow S = (1+\beta) \cdot \frac{R_C + R_B}{R_B + R_C(1+\beta)}$$

→ If $R_C(1+\beta) >> R_B$, then $\boxed{S = 1 + \frac{R_B}{R_C}}$ ans

→ If $R_C \uparrow$ & $R_B \downarrow$ then $S \downarrow$; Hence S depends on load resistance.

→ It is voltage shunt feedback, hence $R_i \downarrow$ and $R_o \downarrow$.

→ There is unnecessary -ve feedback, circuit is not preferable.

<u>Theoretical Analysis</u> –

From circuit, $V_C = V_{CC} - (I_C + I_B) R_C$ and $I_C = \beta I_B + (1+\beta) I_{CO} \approx \beta I_B$

$\Rightarrow V_C \approx V_{CC} - I_C R_C$. — ① $\qquad \because \frac{I_C}{\beta} = I_B \Rightarrow I_C >> I_B$

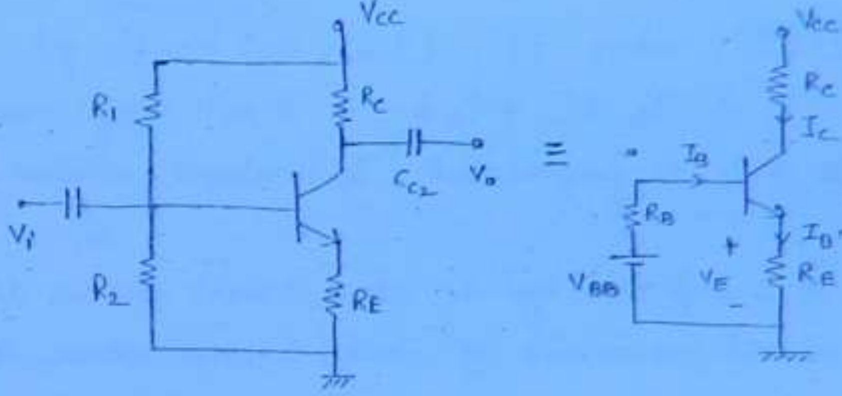
$$I_B = \frac{V_C - V_{BE}}{R_B} \quad — ②$$

from ① & ② – If $T\uparrow$, $[I_{CO}\uparrow$ & $V_{BE}\downarrow]$ and/or $\beta\uparrow$, then $I_C\uparrow$ then $V_C \downarrow$ but $I_B \downarrow$ with $V_C \uparrow \Rightarrow I_C \downarrow$. → -ve feedback.

Therefore, rise in I_c is compensated and I_c is almost constant.

- This circuit will compensate for all type of variations, ie., I_{co}, V_{BE} or β.

Self-Biased Circuit :



→ $V_{BB} = V_{Th} = \frac{R_2}{R_1+R_2} \cdot V_{CC}$

→ $R_{Th} = R_B = R_1 \| R_2$

→ $I_c = \beta I_B + (1+\beta) I_{co}$ —①

→ $S = \frac{1+\beta}{1-\beta \frac{dI_B}{dI_c}}$ —②.

Writing KVL at i/p—

$V_{BB} = I_B R_B + V_{BE} + (I_B + I_c) R_E$

→ Differentiating w.r.t I_c — ⇒ $0 = (R_B + R_E)\frac{dI_B}{dI_c} + R_E$

⇒ $\frac{dI_B}{dI_c} = \frac{-R_E}{R_B+R_E}$ —③.

→ Substituting in eqⁿ ② —

imp

∴ $\boxed{S = \frac{1+\beta}{1+\frac{\beta R_E}{R_B+R_E}}}$ < $(1+\beta)$ → Hence ckt is stable.

⇒ $S = (1+\beta) \cdot \frac{R_E+R_B}{R_B+(1+\beta)R_E}$

→ If $(1+\beta)R_E >> R_B$, then,

imp

$\boxed{S = 1 + \frac{R_B}{R_E}}$ → {Advantage — Independent of load resistance R_c}

→ Ideally, $\boxed{R_E = \infty, \quad S = 1,}$ Hence, $\boxed{R_E \uparrow \text{ and/or } R_B \downarrow \text{, then } S \downarrow}$ obj.

* Input & o/p resistance will increase.
* It is current series feedback.

Explanation :

- $V_E = (I_B + I_C) R_E \approx I_C R_E$. $\{\because I_C >> I_B\}$ —(1)

(140)

- $I_B = \dfrac{V_{BB} - V_{BE} - V_E}{R_B}$ —(2)

from (1) & (2), when $T\uparrow$, $[I_{CO}\uparrow, V_{BE}\downarrow]$ and/or $\beta\uparrow$, then $I_C\uparrow \Rightarrow V_E\uparrow$

$\Rightarrow I_B\downarrow \Rightarrow I_C\downarrow$ → It will control variation due to all factors.

∴ Rise in I_C is compensated, I_C is almost constant.

* If R_E is replaced by an ideal current source, then S will become 1. (as internal resistance of active (current) source is very high, ideally ∞)

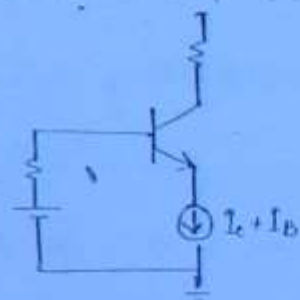
Ideal current source,

$R_S = R_E = \infty$

→ $S = 1$

Practical current source,

R_E = very high.



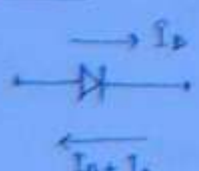
* Self-biased circuit is also called as voltage divider / Potential divider or emitter bias circuit.

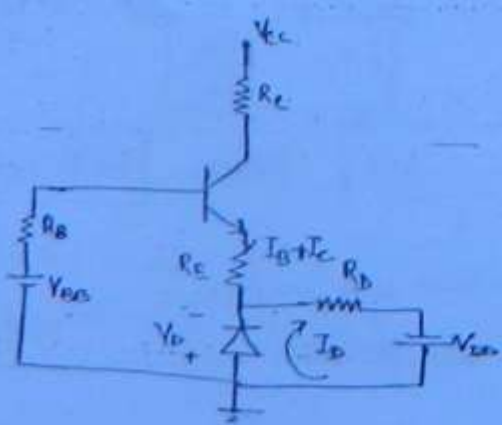
Compensation Techniques :- (Bias Compensation) -

→ compensation techniques refers to use of temp. sensitive devices like diode, thermistor, sensistor etc.

1) Diode Compensation -

a) for V_{BE} :-





$\rightarrow I = I_D - (I_B + I_C)$

$\rightarrow I_D = \dfrac{V_{DD} - V_D}{R_D}$ — (2)

From eq^n, for diode to be FB —

$I \geq 0 \rightarrow I_D > I_B + I_C$

Hence, if we set I_D based on eq^n(2) then we can make D forward bias.

→ When D → FB, then

→ Transistor is in active region

→ $I_C = \beta I_B + (1+\beta) I_{CO}$ — (1)

and, $\dfrac{I_C - (1+\beta) I_{CO}}{\beta} = I_B$ — (2)

from circuit, $V_{BB} = I_B R_B + V_{BE} + (I_C + I_B) R_E - V_D$ — (3).

from (2) & (3) :-

$$I_C = \frac{\beta\left[V_{BB} - (V_{BE} - V_D)\right] + (R_B + R_E)(1+\beta) I_{CO}}{R_B + R_E(1+\beta)} \quad \text{— (4)}$$

If, transistor & diode are of similar materials —

$$\therefore \frac{dV_{BE}}{dT} = \frac{dV_D}{dT} = -2.5\,mV/^\circ C$$

$\therefore$ I_C depends on $(V_{BE} - V_D)$

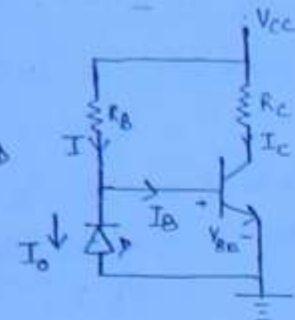
for $1^\circ C$ change in T, $(V_{BE} - 2.5) - (V_D - 2.5) = (V_{BE} - V_D)$,

$\therefore$ Hence, I_C will remain constant, even if V_{BE} is changing.

→ The change of V_{BE} with temp contribute significantly to change in I_C of Silicon transistor, therefore circuit is useful for stabilising Si transistor.

→ The diode is kept forward biased by source V_{DD} and resistance R_D. If the diode is of same material & type, voltage V_D across diode will have same temp. coeff as V_{BE}, then from eq^n (4). it is clear that I_C will be insensitive to variation in V_{BE}.

(b) for I_{co} :-



→ For Ge, $V_{BE} = 0.2V$ = voltage across (diode) since they are in parallel

→ $I_B = I - I_o$.

→ $I = \frac{V_{cc} - V_{BE}}{R_B}$ = constant {considering V_{BE} = constant}

→ $I_c = \beta I_B + (1+\beta) I_{co}$

$\Rightarrow I_c = \beta[I - I_o] + (1+\beta) I_{co} \Rightarrow I_c = \beta I - \beta I_o + \beta I_{co}$ {$\because \beta >> 1$}

$$\Rightarrow \boxed{I_c = \underbrace{\beta I}_{\text{constant}} + \beta\,(I_{co} - I_o)}$$

→ for Ge transistor, change in Ico with temp. play more important role in collector current stability, therefore, this ckt is useful for stablising Ge Tr.

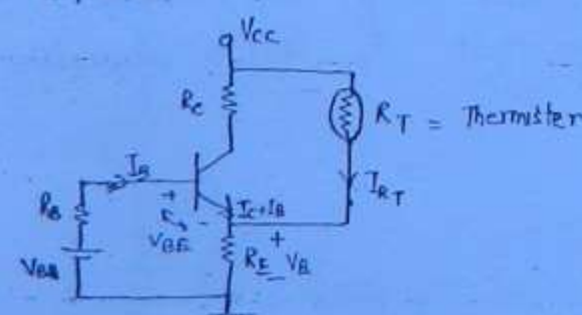
→ If the diode & Tr. are of same type, then I_o of diode will ↑es with T at same rate as I_{co}. Therefore, I_c will be insensitive to variation in I_{co}.

2> Thermister and Sensister compensator :-

→ Thermister → NTC of resistivity ; T↑ σ↑
(lightly doped)

→ Sensister → PTC of resistivity ; T↑, σ↓
(highly doped)

→ $I_B = \frac{V_{BB} - V_{BE} - V_E}{R_B}$

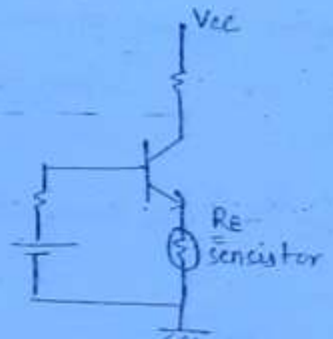


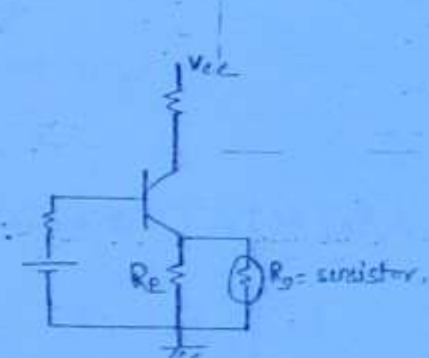
$\rightarrow V_E = (I_B + I_C + I_{R_T}) R_E \approx (I_C + I_{R_T}) R_E$

Now, when $T\uparrow$, $(I_{CO}\uparrow, V_{BE}\downarrow)$, then $I_C\uparrow$, $R_T\downarrow \Rightarrow I_{R_T}\uparrow \Rightarrow V_E \uparrow\uparrow$
$\Rightarrow I_B\downarrow \Rightarrow I_C\downarrow$

Hence, rise in I_C is compensated.

By using sensister :-

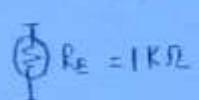




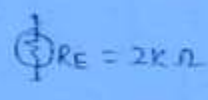
(Preferable)

* Re replaced by a sensister or we can place a sensister parallel to R_E.

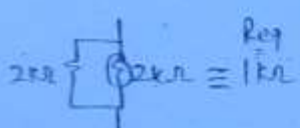
eg :-



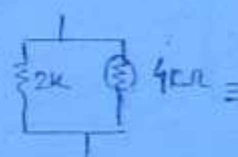
$\xrightarrow{T\uparrow}$



$\Delta R_E = 100\%$.



$\overset{R_{eq}}{\equiv 1k\Omega} \xrightarrow{T\uparrow}$



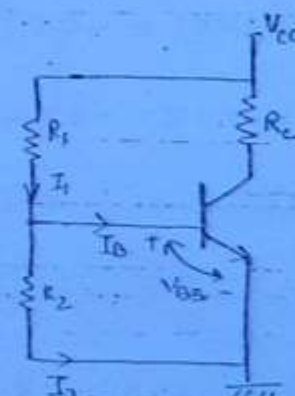
$\equiv R_{eq} = 1.33k\Omega$, $\Delta R_E = 33\%$.

→ Hence, controlled feedback by using sensister.

* $I_B = I_1 - I_2$

$I_1 = \dfrac{V_{CC} - V_{BE}}{R_1}$

$I_2 = \dfrac{V_{BE}}{R_2}$



Now, when $T\uparrow$, $(I_{CO}\uparrow$ & $V_{BE}\downarrow)$ then $I_C\uparrow$, then to compensate we want $I_B\downarrow$. or

$\Rightarrow I_1\downarrow$ and/or $I_2\uparrow$

$\Rightarrow R_1\uparrow$ and/or $R_2\downarrow$

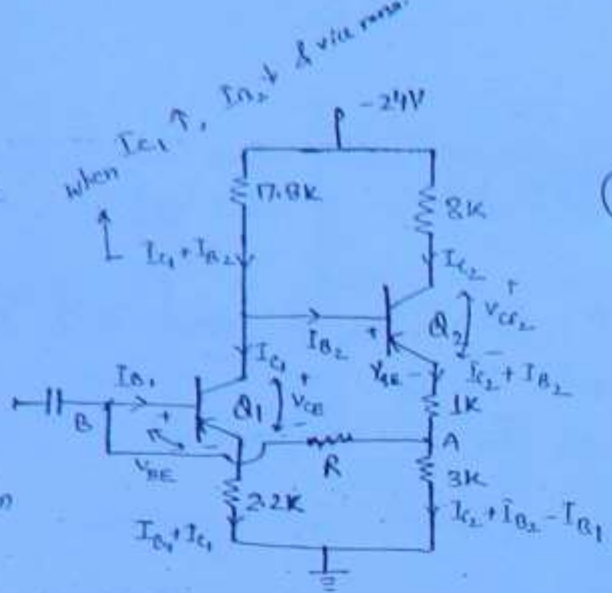
Hence, R_1 can be replaced by sensistor & R_2 can be replaced by Thermistor. or R_1 can be replaced by sensistor in ‖ & R_2 with thermistor in ‖.

Ques: In two stage ckt, assume $\beta = 100$ for each transistor

(a) Determine R so that quescient conditions are $V_{CE_1} = -4V$, $V_{CE_2} = -6V$

(b) Explain how Q-point stablisation is obtained.

Take $V_{BE} = 0.2V$.



Solⁿ Since $\beta >> 1$, $I_{B_2} << I_{C_2}$ & $I_{B_1} << I_{C_1}$. $\Rightarrow$ we will neglect I_{B_1} & I_{B_2}.

By KVL —

$$-24 - 17.8(I_{C_1}) - V_{CE_1} - 2.2(I_{C_1}) = 0 \Rightarrow -24 - (-4) = 17.8 I_{C_1} + 2.2 I_{C_1}$$

$$\Rightarrow -20 I_{C_1} = 20$$

$$\Rightarrow I_{C_1} = -1 mA$$

By KVL —

$$-24 - 8 I_{C_2} - V_{CE_2} - 1(I_{C_2}) - 3(I_{C_2}) = 0$$

$$\Rightarrow I_{C_2} = -1.5 mA$$

Now,

$$R = \frac{V_A - V_B}{I_{B_1}} \quad ; \quad V_A = 3K \times (-1.5) = -4.5 V$$

$$V_B = V_{BE} + I_{C_1} \times 2.2 = -0.2 - 1 \times 2.2$$

$$\Rightarrow V_B = -2.4 V.$$

$$\rightarrow \quad I_{B_1} = \frac{I_{C_1}}{\beta} = -0.01 mA$$

$$\therefore R = \frac{-4.5 - (-2.4)}{-0.01} = 210 K\Omega.$$

(b) When $T\uparrow$, $|I_{C_2}|\uparrow$, $|V_A|\uparrow$, $|I_{B_1}|\uparrow$, $|I_{C_1}|\uparrow$, $|I_{B_2}|\downarrow$, $|I_{C_2}|\downarrow \rightarrow$ Compensated.

When $T\uparrow$, $|I_{C_1}|\uparrow$, $|I_{B_2}|\downarrow$, $|I_{C_2}|\downarrow$, $|V_A|\downarrow$, $|I_{B_1}|\downarrow$, $|I_{C_1}|\downarrow \rightarrow$ "

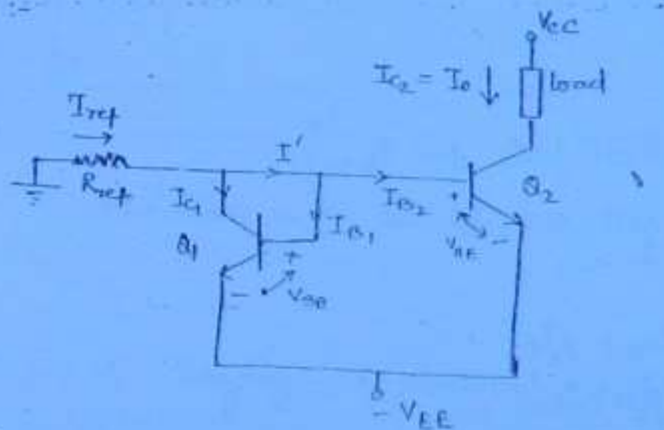
04th September, 2012

Current Mirror Circuit :-

195

- The output current is forced to equal the i/p current., i.e., o/p current is a mirror image of i/p current.
- They are widely used in designing of differential amplifiers & ICs.
- Their major advantages are—
  a) Simplicity in circuit design.
  b) Easy to fabricate
  c) Minimum no. of components are reqd.
  d) Low cost.

- Basic Diagram :-



Reqd. conditions :-
→ Both Tr. are in active region
→ Both Tr. are identical, i.e., $\beta_1 = \beta_2 = \beta$ & $V_{BE_1} = V_{BE_2} = V_{BE}$.
→ β should be very large.

Writing KVL —

$$0 - I_{ref} \cdot R_{ref} - V_{BE} = -V_{EE}$$

$$\Rightarrow \boxed{I_{ref} = \frac{V_{EE} - V_{BE}}{R_{ref}}} \rightarrow \text{independent of load.}$$

from figure—

$$I_{B_1} = I_{B_2} \quad \{\because I' \text{ is divided among two identical paths}\}$$

$$\because \beta_1 = \beta_2 \Rightarrow \boxed{I_{C_1} = I_{C_2}}$$

Since, $I_{ref} = I_{C_1} + I' \Rightarrow I_{ref} = I_{C_2} + 2I_{B_2}$

$$\Rightarrow I_{ref} = I_{C_2} + \frac{2I_{C_2}}{\beta}$$

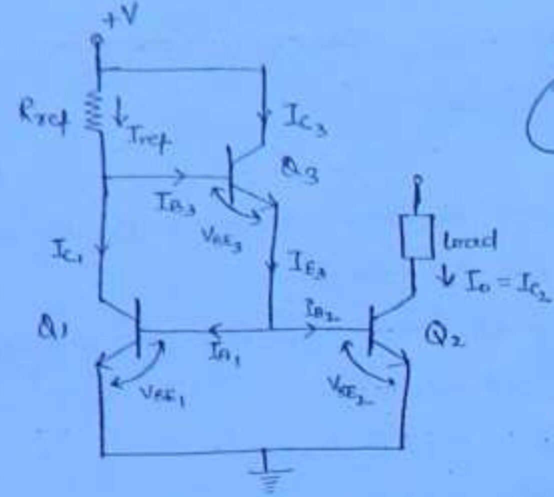
$$\Rightarrow \boxed{I_{ref} \simeq I_{C_2}} \quad \text{if } \beta \text{ is very large.}$$

→ Q_1, Q_2, Q_3 are in active region

→ Q_1, Q_2, Q_3 should be identical,

i.e., $\beta_1 = \beta_2 = \beta_3 = \beta$ & $V_{BE_1} = V_{BE_2} = V_{BE_3} = V_{BE}$

→



By applying KVL -

$$V_+ = I_{ref} \cdot R_{ref} + V_{BE_3} + V_{BE_2}$$

$$\Rightarrow \boxed{I_{ref} = \frac{V_+ - 2V_{BE}}{R_{ref}}} \quad \text{— (1).} \qquad \{\text{Independent of load}\}.$$

Now,

$$\boxed{I_{ref} = I_{C_1} + I_{B_3}} \quad \text{— (2)}$$

from fig.,

$$I_{B_1} = I_{B_2} \quad \{\because \text{identical paths for } I_{E_3}\}.$$

$$\Rightarrow \boxed{I_{C_1} = I_{C_2}} \quad \{\because \beta_1 = \beta_2\} \quad \text{— (3)}$$

$$\rightarrow I_{B_3} + I_{C_3} = I_{E_3} \Rightarrow I_{E_3} = I_{B_3} + \beta_3 I_{B_3}$$

$$\Rightarrow I_{E_3} = (\beta_3 + 1) I_{B_3}$$

$$\Rightarrow 2 I_{B_2} = (\beta_3 + 1) I_{B_3}$$

$$\Rightarrow \frac{2 I_{C_2}}{\beta} = (\beta_3 + 1) I_{B_3}.$$

$$\Rightarrow \boxed{I_{B_3} = \frac{2 I_{C_2}}{\beta(1+\beta_3)}} \quad \text{— (4)}$$

from (3) & (4) in (2) -

$$\therefore I_{ref} = I_{C_2} + \frac{2 I_{C_2}}{\beta(1+\beta_3)} \Rightarrow \boxed{I_o = \frac{I_{ref}}{1 + \frac{2}{\beta(1+\beta_3)}}}. \qquad \{\because I_o = I_{C_2}\}.$$

Since $\beta >> 1$ -

$$I_o = \frac{I_{ref}}{1 + 2/\beta^2} \Rightarrow \boxed{I_o \approx I_{ref}} \qquad \Rightarrow \boxed{I_o = \left(\frac{\beta^2 + \beta}{\beta^2 + \beta + 2}\right) \cdot I_{ref}}.$$

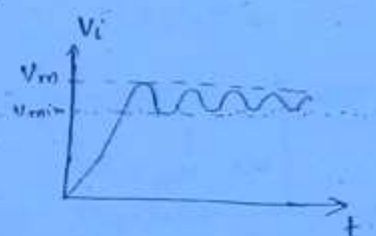
chk ✗✗

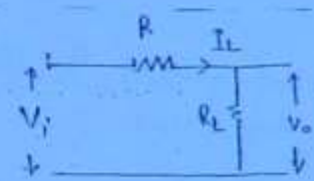
→ It is necessary that Q_1 & Q_2 are identical. If Q_3 is not identical then–

$$I_0 = \frac{I_{ref}}{1 + \frac{2}{\beta(1+\beta_3)}} \qquad \{\beta_3 \to \text{for } Q_3\}.$$

→ In this circuit, it is not required to have very high β, since a term of β^2 is appearing in denominator which will be very large.

→ <u>Voltage Regulator Circuit</u> :-





→ Line variation :- variation in V_o due to variation in line voltage V_i.
→ load variation :- " " " " " " load resistance R_L.

<u>Line Regulation</u> :- V_i = varying, R_L = constant, V_o should be constant.

∵ $V_o = I_L R_L$ ∴ hence I_L should be constant for V_o to be constant.

Hence in line regulation, line voltage is varying but load current remains constant.

<u>load Regulation</u> :- V_i = constant, R_L = varying,

for V_o to be constant, when $R_L \uparrow$, I_L should $\downarrow$ and vice versa.
Hence, in load regulation, R_L varying but V_o remains constant.

<u>Voltage Regulator</u> :-
– It regulates load voltage.
– In regulator circuit, load voltage V_o will be maintained almost constant irrespective of load variations & i/p voltage variations (line varia^n).

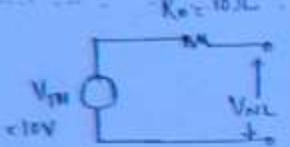
- Performance of a regulator ckt is analysed by its regulation, ie,

$$\boxed{\%\ \text{Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%}$$

→ V_{NL} = No load voltage, $I_L \to 0$ or $R_L \to \infty$.
V_{FL} = Full load voltage, $I_L \to I_{Lmax}$ or $R_L \to R_{Lmin}$.

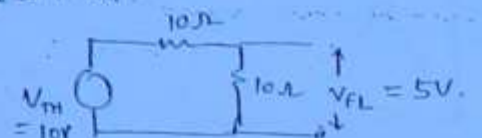
→ Ideally, $\boxed{V_{NL} = V_{FL} \quad \& \quad \%\ \text{Regulation} = 0\%}$

Eg



$V_{NL} = 10V$

$R_L = 10\Omega$ to $10K\Omega$



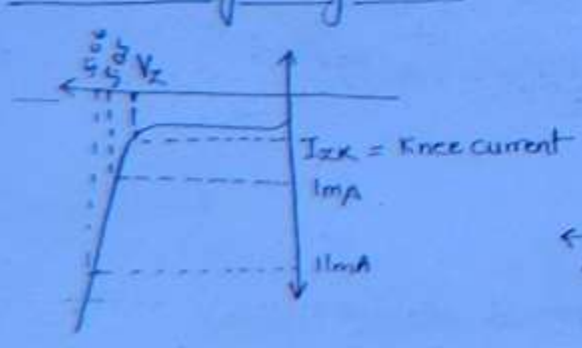
$\therefore$ % Regulation $= \frac{10-5}{5} \times 100 = 100\%$ → very poor.

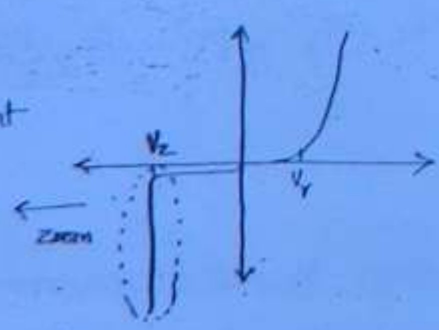
Note: For better performance of ckt, % regulation should be as low as possible.

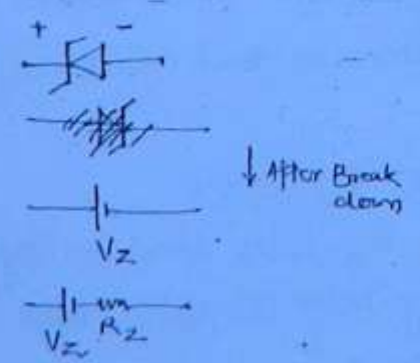
Types of Voltage Regulator :-

- Zener VR
- By using BJT
  - Series VR
  - Shunt VR
- IC VR
  - 78 series (+ve VR)
  - 79 series (-ve VR).

Zener Voltage Regulator :-







* I_{ZK} = Knee current or minimum current reqd. for zener diode to go in breakdown

→ $P_{zmin} = I_{ZK} \times V_Z$.

→ I_{zmax} = maximum current across zener diode without damaging it.

→ $P_{zmax} = I_{zmax} \times V_Z$. ⇒ $I_{zmax} = \frac{P_{zmax}}{V_Z}$.

→ V_Z is almost constant but not exactly constant.

Eg from plot, slope $= \frac{1}{R_Z} = \frac{11-1}{5.06-5.05} = 1000\,mA/V = 1A/V$

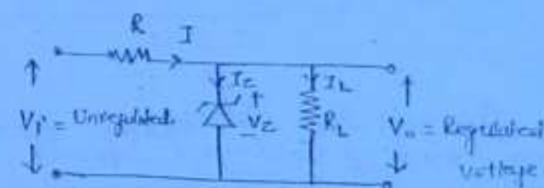
$\Rightarrow R_Z = 1\Omega$

Hence, exact representation of zener diode BD is battery followed by R_Z.

— Zener Voltage Regulator —

V_i = unregulated voltage

V_o = Regulated "



→ for voltage regulation,

zener diode should be in BD for entire range of V_i (V_{min} to V_{max}).

∴ $\boxed{V_0 = V_Z}$

→ ∴ $I = \frac{V_i - V_o}{R}$ and $I = I_Z + I_L$

→ $I_L = \frac{V_0}{R_L} = \frac{V_Z}{R_L}$ Case I If R_L = constant, then I_L = constant

Now, V_i → varying then I → varying & I_L = constant

∴ I_Z = varying

Hence, for satisfactory performance of ckt

$\boxed{I \geq I_{ZK} + I_L}$ {∵ Range of I_Z, $I_{ZK} \leq I_Z \leq I_{zmax}$ to be working in BD}

→ $I_{min} = \frac{V_{imin} - V_Z}{R}$, $I_{max} = \frac{V_{imax} - V_Z}{R}$

→ $\boxed{I_{min} \geq I_{ZK} + I_L}$ **

Case II: V_i = constant, R_L = varying

$\Rightarrow$ I = constant $= \frac{V_i - V_z}{R}$

I_L = variable

$\rightarrow$ $I = I_z + I_L$

$\rightarrow$ $\boxed{I_{Lmax} = \frac{V_z}{R_{Lmin}}}$ if $R_L = R_{Lmin}$.

$\Rightarrow$ $\boxed{I = I_{zmin} + I_{Lmax} \quad \& \quad I_{zmin} \geq I_{zK}.}$

$\Rightarrow$ When $\boxed{I_{Lmin} = \frac{V_z}{R_{Lmax}}}$

$\Rightarrow$ $I = I_{zmax} + I_{Lmin}$ & hence $\boxed{I_{zmax} \leq \frac{P_{zmax}}{R_z}}$.

$\rightarrow$ Combining both cases, the eqn for satisfactory operation of regulator circuit -

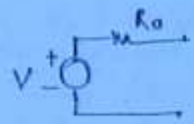
$$\boxed{\frac{V_{imin} - V_z}{R} \geq I_{zK} + \frac{V_z}{R_{Lmin}}}^{**}$$ $\rightarrow$ zener diode to be in BD.

$\rightarrow$ Power dissipation across zener diode $\leq$ P_{max}, hence the following condition should be satisfied -

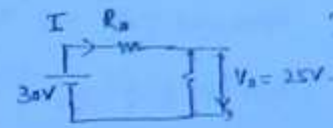
$$\boxed{\frac{V_{imax} - V_z}{R} \leq I_{zmax} + \frac{V_z}{R_{Lmax}}}^{**}$$ $\rightarrow$ ZD not to burn

Workbook – Chap.1. Pg.29.

Ques.13 :- $V_{NL} = 30V$, $V_{FL} = 25V$ % Regulation $= \frac{30-25}{25} \times 100 = 20\%$.
(a).



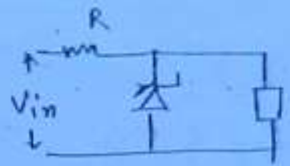
$V = V_{NL} = 30V.$ $\Rightarrow$



$I = 1A.$

$\therefore R_{Lmin} = \frac{25}{1} = 25\Omega$, o/p resistance $= R_o = \frac{5V}{1A} = 5\Omega.$

Ques.15 :
(a)



$V_Z = V_o = 10mA.$

V_{in} = 30 to 50V. for satisfactory o/p – $I \geq I_{ZK} + I_L$

$\Rightarrow \frac{V_{min} - V_Z}{R} \geq (1+10)mA \Rightarrow \frac{30-10}{R} \geq 11mA$

$\Rightarrow R \leq 1818 k\Omega$

Ques.16 : $I_L \to$ 100 to 500mA.
(d) $V_{in} = 12V$
$I_{ZK} \simeq 0.$

~~Basic~~ $\frac{V_{in} - V_Z}{R} \geq I_{ZK} + I_{max}$ $\{ I_{max} = \frac{V_Z}{R_{Lmin}}$

$\Rightarrow \frac{12-5}{R} = 0 + 500mA \Rightarrow R = 14\Omega.$

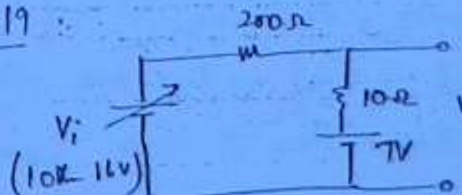
Ques17 . $V_I \to$ 20 to 30V.
(c) load current max. $\Rightarrow$ min zener current.

$\frac{V_{inmin} - V_Z}{R} \geq I_{ZK} + I_{Lmax} \Rightarrow \frac{20-5.8}{1k\Omega} \geq 0.5mA + I_{Lmax}$

$\Rightarrow I_{Lmax} \leq 14.2 - 0.5$

$\Rightarrow I_{Lmax} \leq 13.7mA.$

Ques.19 :
(c)



when $V_i = 10V$ –

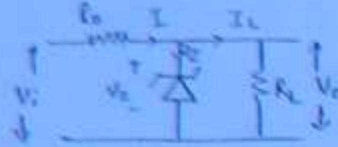
$i = \frac{10-7}{210} = 1/70 A$

$V_o = 7 + \frac{1}{70} \times 10 = 7.14V$

when $V_i = 16V$ –

$i = \frac{16-7}{210} = 3/70 A$ $\therefore V_o = 7 + \frac{3}{70} \times 10 = 7.1$

- Line Regulation using zener diode -



$V_i \to$ varying, R_L = constant

$I = \frac{V_i - V_z}{R}$, $I = I_z + I_L \Rightarrow I_L = I - I_z$

When $V_i \uparrow$, $I\uparrow$, $V_z \uparrow$ (slightly) , $\underline{I_z \uparrow\uparrow}$, I_L remains constant

When $V_i \downarrow$, $I\downarrow$, $V_z \downarrow$ (slightly) , $I_z \downarrow\downarrow$, I_L " " ,

- Load Regulation using zener diode -

V_i = constant , R_L = varying. $I \to$ constant $\Rightarrow I_L = I - I_z$.

When $R_L \uparrow$, $V_0 \uparrow$ (slightly) , $V_z \uparrow$ (slightly) , $I_z \uparrow\uparrow$, $I_L \downarrow$.

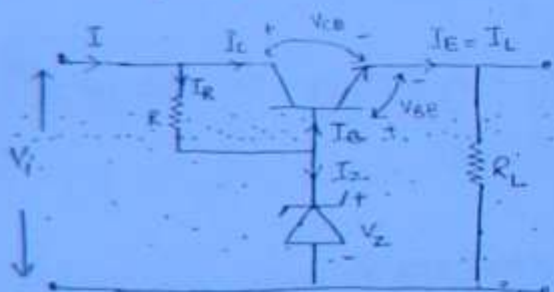
$\therefore \quad V_0 = I_L R_L$ = constant

When $R_L \downarrow$, $V_0 \downarrow$ (slightly) , $V_z \downarrow$ (slightly) , $I_z \downarrow\downarrow$, $I_L \uparrow$.

$\therefore V_0 = I_L R_L$ = constant.

Voltage Regulation by using BJT :-

Series Voltage Regulator



→ BJT should be in active region & zener diode in Breakdown region for full range of V_i from V_{min} to V_{max}.

from ckt -

→ $V_0 = V_z - V_{BE}$. (→ Regulated Voltage)

→ $I_R = \frac{V_i - V_z}{R}$

→ $I_R = I_B + I_z$.

→ $I_C = \beta I_B$ and $I_L = I_E = I_C + I_B \Rightarrow I_E = I_L = (1+\beta) I_B$.

→ $V_{CE} = V_i - V_0$ = URV − RV

power dissipation :-

Across Zener diode :- $\boxed{P_Z = V_Z \cdot I_Z \leq P_{Zmax}.}$

Across BJT :- $\boxed{P_T = I_C \cdot V_{CE}.}$

Line Regulation –

$V_i \to$ vary, R_L = constant. $I_B = I_R - I_z$.

$V_i \uparrow$, $I \uparrow$, $I_R \uparrow$ (I_C is not controlled by V_i, it is controlled by I_B),
then $V_z \uparrow$ (slightly) $I_z \uparrow \Rightarrow I_B$ = constant $\Rightarrow I_E$ = constant

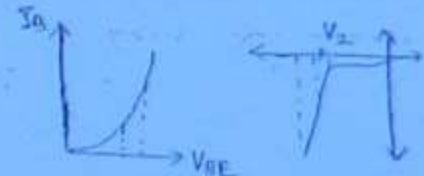
$I_E = I_L$ = almost constant, therefore V_o = constant.

Load Regulation :-

V_i = constant, R_L = vary. $V_o = V_Z - V_{BE}$, $I_R = \uparrow I_E + I_B \downarrow$ = constant.

$R_L \uparrow$, $V_o \uparrow$, $\begin{pmatrix} V_Z \uparrow & I_Z \uparrow \\ V_{BE} \downarrow & I_B \downarrow \end{pmatrix}$, $I_E \downarrow \{ \because I_B \downarrow \}$, $I_L \downarrow$

$\therefore V_o = I_L R_L$ = constant.



* The circuit is in common collector configuration and hence this regulator is also called emitter follower VR.

Note.

* let I_Z variation is $\Delta I_Z = 1$ to $11\,mA \Rightarrow \Delta I_Z = 10\,mA$.

$$\left.\begin{aligned} \Delta I_L &= 10\,mA \\ \Delta R_L &= \frac{V_Z}{\Delta I_L} \end{aligned}\right\} \text{ for zener diode ckt}$$

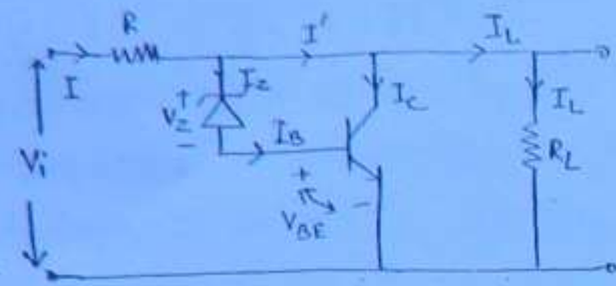
$$\left.\begin{aligned} \Delta I_Z &= 10\,mA = \Delta I_B \\ \Delta I_E &= (1+\beta)\,\Delta I_B = 1000\,mA \\ & \text{for } \beta = 99 \end{aligned}\right\} \text{ for BJT ckt.}$$

Hence, BJT ckt regulation can bear more variations in R_L as compared to zener ckt.

But, for V_i variation, same problem is present in both.

for BJT, As $V_i \uparrow$, $I_R \uparrow$, $I_Z \uparrow$ hence for large V_i variation, I_Z will vary to I_{Zmax} and P_Z will cross P_{Zmax}.

Shunt Regulator :-



Tr → Active

V_z → BD

→ $V_o = V_z + V_{BE}$ → RV

→ $I = \frac{V_i - V_o}{R}$

$\left\{ = \frac{URV - RV}{R} \right\}$ ↳ limiting resistor

* Transistor is in common emitter configuration.

→ $P_T = V_{CE} \cdot I_c$ → $I_B = I_Z$

→ $P_z = V_z \cdot I_z$ → $I_c = \beta I_B$.

→ $I = I_Z + I_c + I_L$ — (1)

Line Regulation :- V_i = vary, R_L = constant

When $V_i \uparrow$, $I \uparrow$, $\left\{ \begin{matrix} V_z \uparrow & I_z \uparrow \\ V_{BE} \uparrow & I_B \uparrow \end{matrix} \right\}$, $I_c \uparrow$ {due to I_B}, I_L (constant).

Eg:- let ΔI = 1000 mA, then $\Delta I_Z = \Delta I_B$ = 10 mA,

$\Delta I_c = \beta \Delta I_B$ = 990 mA

Since the total change is distributed b/w I_z & I_C {from (1)}
& I_L = constant.

Load Regulation :- V_i = constant, R_L = vary.

→ V_i = constant ⇒ I = constant.

→ when $R_L \uparrow$, $V_o \uparrow$, $\left\{ \begin{matrix} V_z \uparrow & I_z \uparrow \\ V_{BE} \uparrow & I_B \uparrow \end{matrix} \right\}$, $I_c \uparrow$, $I_L \downarrow$. {$I = I_c + I_L + I_z$ = constant}

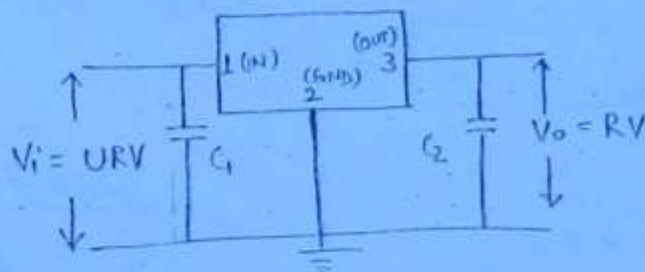
∴ $R_L \cdot I_L = V_o$ = constant.

→ This ckt is suitable for high variation of R_L as well as V_i.

Regulator:

155

- three terminal voltage regulator, IN, OUT and GROUND.



C_1 & C_2 is connected to bypass high frequency noise.

78 series (+ve o/p voltage)	V_o	79 series (-ve output voltage)	V_o
7805	+5 V	7905	-5V
7810	+10V	7910	-10V
7812	+12V	7912	-12V
7815	+15V	7915	-15V
7824	+24V	7924	-24V

Low frequency Analysis of BJT :-

h-parameters :-

$$V_1 = h_{11} I_1 + h_{12} V_2$$
$$I_2 = h_{21} I_1 + h_{22} V_2$$

→ $h_{11} = \frac{V_1}{I_1}\Big|_{V_2=0}$ = i/p impedance when o/p is sc.

→ $h_{12} = \frac{V_1}{V_2}\Big|_{I_1=0}$ = Reverse voltage gain when i/p is o.c.

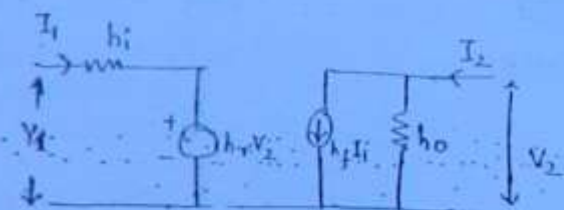
→ $h_{21} = \frac{I_2}{I_1}\Big|_{V_2=0}$ = forward current gain when o/p is s.c.

→ $h_{22} = \frac{I_2}{V_2}\Big|_{I_1=0}$ = o/p admittance with i/p o.c.

* $$\boxed{\begin{array}{ll} h_{11} = h_i \; ; & h_{12} = h_r \\ h_{21} = h_f \; ; & h_{22} = h_o \end{array}}$$

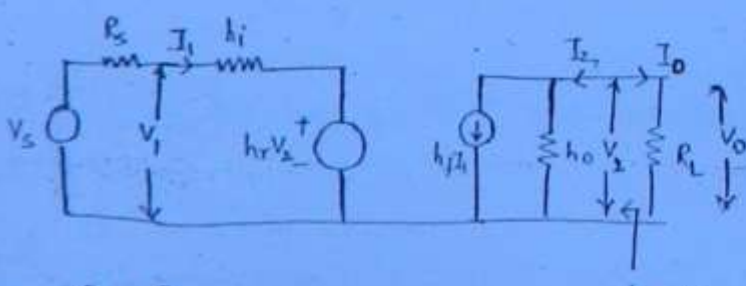
Hence, $V_1 = h_i I_1 + h_r . V_2$

$I_2 = h_f I_1 + h_o . V_2$



Derivation of A_I, R_i, A_V, A_{VS}, R_o :-

Current Gain A_I



$$A_I = \frac{I_o}{I_1} = -\frac{I_2}{I_1}$$

$I_2 = h_f I_1 + h_o V_2$ — ①

$V_2 = I_o R_L = -I_2 R_L$ — ②

from ① & ② -

$$I_2 (1 + h_o R_L) = h_f I_1$$

$$\Rightarrow \boxed{A_I = \frac{-h_f}{1 + h_o R_L}}$$

Input Resistance R_i :-

$\rightarrow R_i = V_1/I_1$

$\rightarrow V_1 = h_i I_1 + h_r V_2$.

$\rightarrow V_2 = -I_2 R_L = A_I I_1 R_L$

$$V_1 = h_i I_1 + A_I I_1 R_L h_r$$

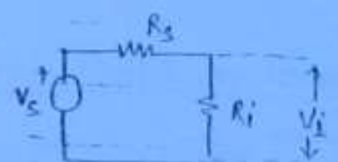
$$\Rightarrow \boxed{R_i = h_i + h_r A_I \cdot R_L}$$

Voltage Gain, Av :-

$$A_V = \frac{V_2}{V_1} = \frac{-I_2 R_L}{I_1 R_i} \Rightarrow A_V = \frac{A_I R_L}{R_i} \quad \text{or} \quad \boxed{A_V R_i = A_I \cdot R_L}$$

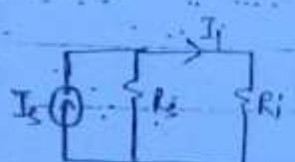
Overall voltage Gain, A_{vs} :-

$$A_{vs} = \frac{V_o}{V_s} = \frac{V_2}{V_s} = \frac{V_2}{V_1} \times \frac{V_1}{V_s} = A_V \cdot \frac{V_1}{V_s}$$



$$\frac{V_1}{V_s} = \frac{R_i}{R_i + R_s} \Rightarrow \boxed{A_{vs} = \frac{A_V \cdot R_i}{R_i + R_s} = \frac{A_I \cdot R_L}{R_i + R_s}}$$

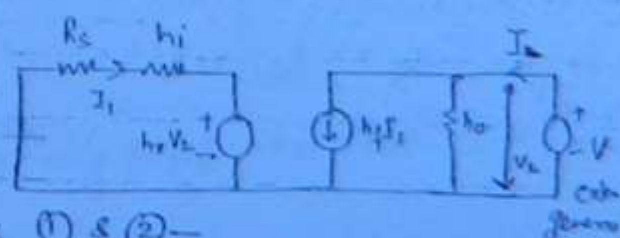
* If current source is present instead of V_s -



$$A_{Is} = \frac{I_o}{I_s} = -\frac{I_2}{I_s} = -\frac{I_2}{I_1} \times \frac{I_1}{I_s} = A_I \cdot \frac{I_1}{I_s}$$

$$\frac{I_1}{I_s} = \frac{R_s}{R_s + R_i} \quad \therefore \boxed{A_{Is} = A_I \cdot \frac{R_s}{R_s + R_i}}$$

Output Resistance, R_o :-



$\rightarrow I = h_f I_1 + h_o V$ —— (1)

$\rightarrow$ KVL at i/p $\rightarrow \dfrac{-h_r V_2}{R_s + h_i} = I_1$ —— (2)

from (1) & (2) -

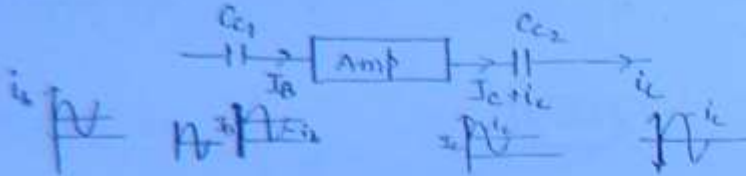
$$\boxed{Y_o = \frac{I}{V} = h_o - \frac{h_f \cdot h_r}{R_s + h_i}} = 1/R_o$$

$\rightarrow \boxed{R_o' = R_o \parallel R_L}$

05/09/2012

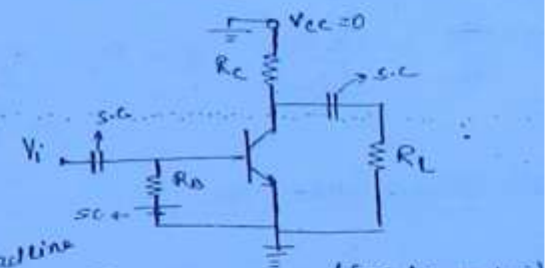
$I_c + i_c = \beta_{dc} I_B + \beta_{ac} i_b$

$|A_I| = \dfrac{i_c}{i_b}$

*


Tr in active region.

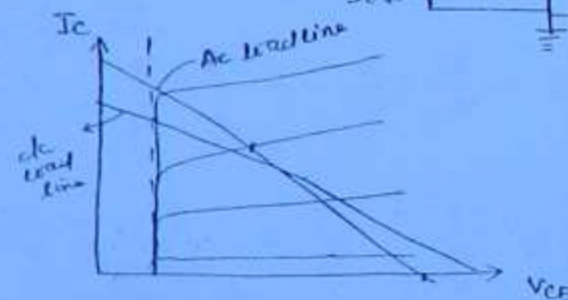
* We can neglect DC sources in ac analysis as long as they are keeping ~~ckt in~~
* During AC analysis —
  - All DC sources = 0, i.e, voltage source = S.C, current source = O.C.
  - Coupling capacitors C_{c_1} & C_{c_2} (C_{b_1} & C_{b_2}) & bypass capacitor acts as S.C.



(For AC analysis)

* $\beta_{dc} = \dfrac{|I_c|}{|I_B|} = h_{FE}$; $\beta_{ac} = \dfrac{|i_b|}{|i_c|} = h_{fe}$

AC load line :-

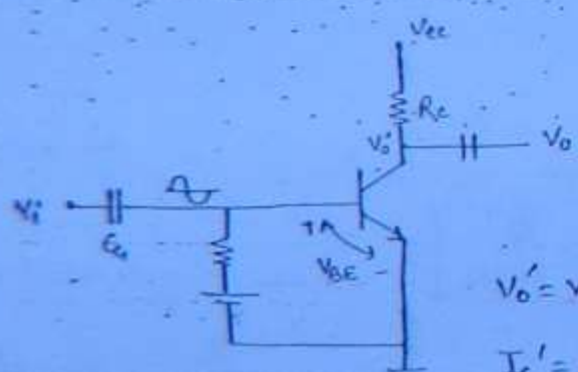


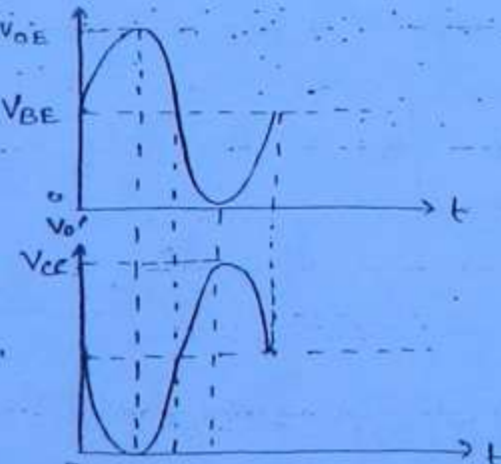
* Slope of dc load line $= -1/R_c$

$R_L' = R_c \| R_L < R_c$.

Slope of ac load line $= -1/R_L'$

$-\dfrac{1}{R_L'} = -\left(\dfrac{1}{R_c} + \dfrac{1}{R_L}\right)$

*




$V_o' = V_{cc} - I_c' R_c$

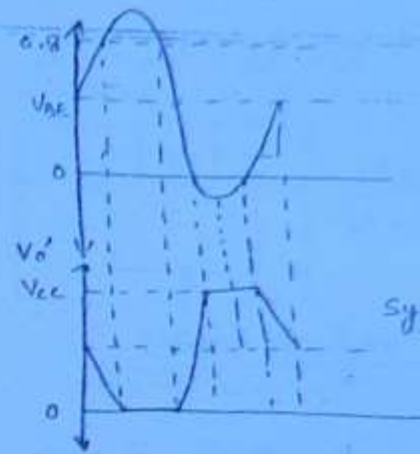
$I_c' = I_c + i_c$

for +ve i/p cycle, $V_{BE} \uparrow$, $I_B \uparrow \Rightarrow I_c \uparrow \Rightarrow V_o' \downarrow$
for −ve " ", $V_{BE} \downarrow$, $I_B \downarrow \Rightarrow I_c \downarrow \Rightarrow V_o' \uparrow$.
$\Big\}$ ⇒ 180° phase shift.

Symmetrical clipping –

Ideally, voltage swing = V_{CC}

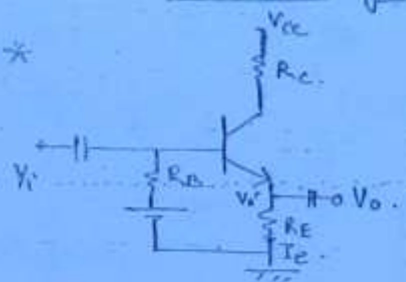
Practically, " = $V_{CC} - V_{CEsat}$



Symmetrical clipping.

Common Collector Config. :

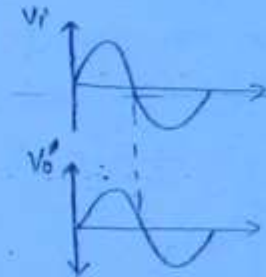
*



$V_0 = I_e \cdot R_E$

$\{ V_{BE}\uparrow, I_B\uparrow, I_E\uparrow, V_0\uparrow \}$.

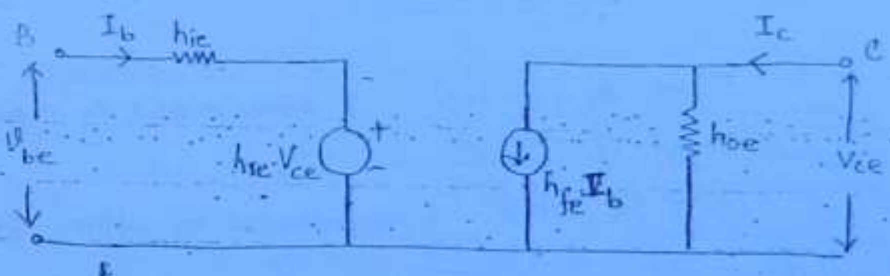
Common collector



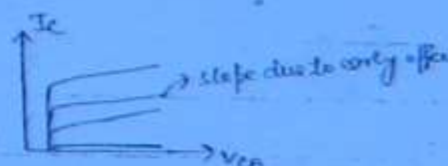
Hence, for CC configuration,

$\boxed{\text{phase shift} = 0^\circ}$

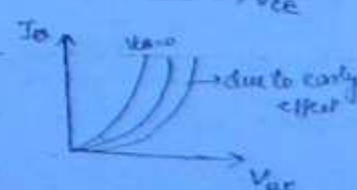
Hybrid Model for Common Emitter Configuration :-



$$V_{be} = h_{ie} I_b + \underbrace{h_{re} V_{ce}}_{\text{Due to early effect.}} \quad \text{— (1)}$$



$$I_c = h_{fe} I_b + \underbrace{h_{oe} \cdot V_{ce}}_{\text{Due to early effect}} \quad \text{— (2)}$$



* $h_{oe} = 1/r_0$; $r_0 = \dfrac{V_A}{I_C}$; V_A = early voltage.

* Typical value – $h_{ie} = 1.1 K\Omega$, $h_{re} = 2.5 \times 10^{-4}$

$h_{fe} = 50$, $h_{oe} = 1/40K$.

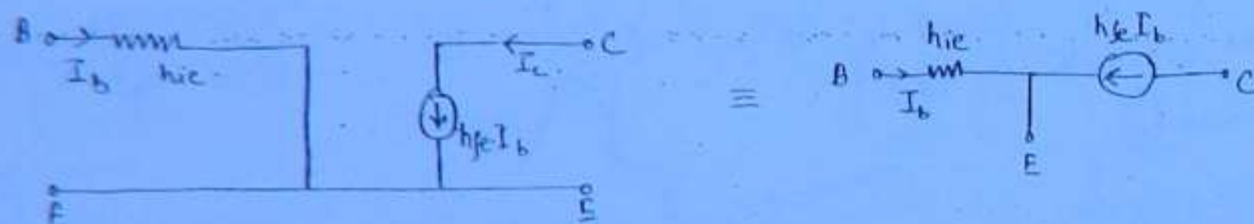
* $A_I = \frac{-h_{fe}}{1 + h_{oe}R_L}$; $R_i = h_{ie} + h_{re} \cdot A_I \cdot R_L$; $A_V = \frac{A_I R_L}{R_i}$

$A_{VS} = \frac{A_V R_i}{R_S + R_i} = \frac{A_I R_L}{R_S + R_i}$; $Y_0 = 1/R_0 = h_{oe} - \frac{h_{re}h_{fe}}{R_S + h_{ie}}$

Simplified/Approximate Hybrid Model –

→ If $h_{oe}R_L \leq 0.1$, then error in approx calculation $\leq 10\%$, therefore we can use approximate model, ie, we can neglect early effect.

$h_{re} = 0$, $h_{oe} = 0$ (⟹ admittance $= 0$ ⟹ resistance $= \infty$ → open)



→ It is valid for CE, CC & CB configuration and for npn as well as pnp Tr.

* Exact | Approximate

for $h_{oe} = 0.1$

→ $A_I = \frac{-h_{fe}}{1.1}$ → $A_I = -h_{fe}$ → overestimated by approx 10%

→ $R_i = h_{ie} + \underbrace{h_{re}A_I R_L}_{-ve}$ → $R_i = h_{ie}$ → overestimated by approx 5%.

→ $A_V = \frac{A_I R_L}{R_i}$ → A_V is overestimated by 5%.

→ $Y_0 = h_{oe} - \frac{h_{re}h_{fe}}{R_S + h_{ie}} \approx \frac{1}{40K}$ → $Y_0 = 0$ ⟹

⟹ $R_0 = 40K$ ⟹ $R_0 = \infty$. → overestimated (but not large)

Miller's Theorem :-

$K = \frac{V_2}{V_1}$

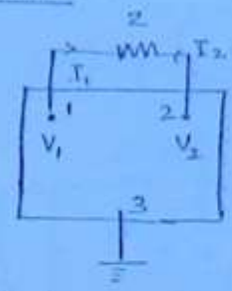


Fig 1.

$\equiv$

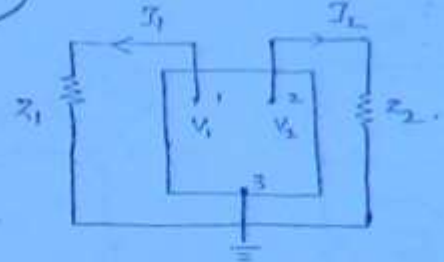


Fig. 2

from fig. 1 —

$$I_1 = \frac{V_1 - V_2}{Z} = \frac{V_1}{Z_1} \quad (\text{from fig 2})$$

$$\Rightarrow Z_1 = \frac{V_1 Z}{V_1 - V_2} \Rightarrow Z_1 = \frac{Z}{1 - \frac{V_2}{V_1}} \Rightarrow \boxed{Z_1 = \frac{Z}{1-K}}$$

Similarity,

$$I_2 = \frac{V_2 - V_1}{Z} = \frac{V_2}{Z_2}$$

$$\Rightarrow \boxed{Z_2 = \frac{KZ}{K-1}}$$

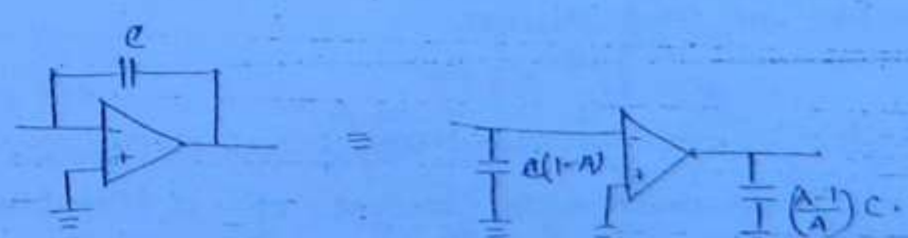
When $Z =$ capacitor —

$$Z_1 = \frac{Z}{1-K} \Rightarrow \frac{1}{\omega C_1} = \frac{1/\omega C}{1-K} \Rightarrow \boxed{C_1 = (1-K)C}$$

$$Z_2 = \frac{KZ}{K-1} \Rightarrow \frac{1}{\omega C_2} = \frac{K(1/\omega C)}{K-1} \Rightarrow \boxed{C_2 = \left(\frac{K-1}{K}\right) \cdot C}$$

Workbook.

Chap 10 Q. 23



→ Hence i/p & o/p capacitances increases and impedance will decrease.
↓
{ parallel cap. }

→ Due to this capacitance, i/p path will be short (low impedance) & i/p to amp. of. amp will be low & overall gain will ↓ .

Dual of Miller's Theorem:-

$$\boxed{A_I = -\frac{I_2}{I_1}}$$

from fig ① & ② -
$$V_1 = (I_1 + I_2)Z = I_1 Z_1$$
$$\Rightarrow Z_1 = \left[1 + \frac{I_2}{I_1}\right] Z \Rightarrow \boxed{Z_1 = (1 - A_I)Z}$$

Similarly,
$$V_2 = (I_1 + I_2)Z = I_2 Z_2$$
$$\Rightarrow Z_2 = \left(1 - \frac{1}{A_I}\right) Z \Rightarrow \boxed{Z_2 = \left(\frac{A_I - 1}{A_I}\right) \cdot Z}$$

Advantage of h parameters:-

1) They are real nos at low frequency.
2) They are graphically obtained from i/p & o/p characteristics of transistor.

Disadvantages -

1) All four h-parameters are temp. sensitive.

Application -

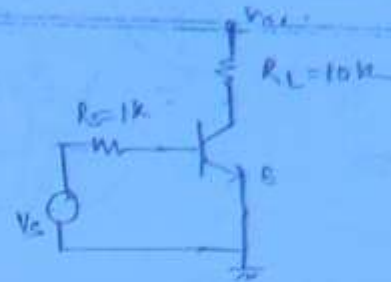
1) They are obtained only for small signal analysis of a transistor amplifier.

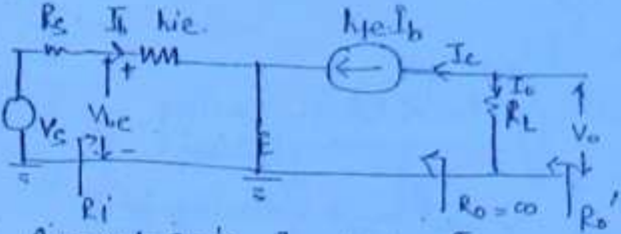
Ques If $R_L = 10K\Omega$, $R_S = 1K\Omega$. find the various gains & i/p & o/p impedances.

$h_{ie} = 1.1 K\Omega$, $h_{fe} = 50$, $h_{re} = h_{oe} = 0$.

Sol^n. Since $h_{oe} = h_{re} = 0$ then we can use simplified model.

(163)





Current gain : $A_I = \frac{I_o}{I_b} = -\frac{I_c}{I_b} = -\frac{h_{fe} I_b}{I_b}$

$$\Rightarrow A_I = -h_{fe} = 50$$

I/p Resistance :

$$R_i = \frac{V_{be}}{I_b} = h_{ie} = 1.1\ K\Omega.$$

Internal voltage gain : $A_V = \frac{V_o}{V_{be}} = \frac{-h_{fe} \cdot R_L \cdot I_b}{V_{be}} = -\frac{h_{fe} \cdot R_L}{R_i}$

$$\Rightarrow A_V = -454.$$

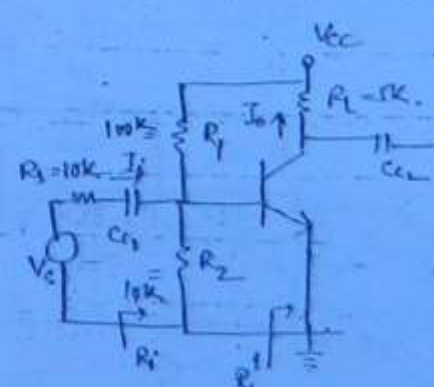
Voltage gain – $\cancel{A_{vs} = \frac{V_o}{V_{be}}}$ $\quad A_{Vs} = \frac{V_o}{V_s} = \frac{V_o}{V_{be}} \times \frac{V_{be}}{V_s}$

$$\Rightarrow A_{Vs} = A_V \cdot \frac{R_i}{R_i + R_s} \Rightarrow A_{Vs} = -237$$

O/p resistance –

$$R_o' = R_o \| R_L = \infty \| R_L = R_L = 10K.$$

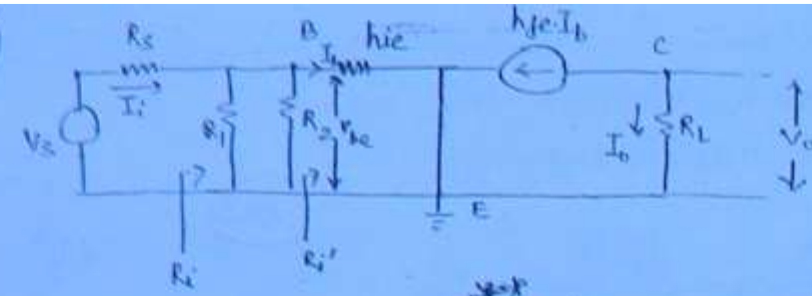
Ques : Given – $h_{fe} = 50$
$h_{ie} = 1.1K$
$h_{re} = h_{oe} = 0$



Find
$A_I = I_o / I_i$
R_i, R_i', A_V, A_{Vs}

Sol^n.

164



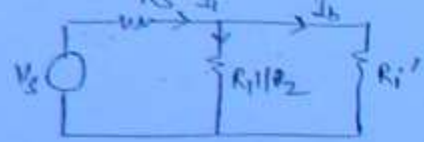
$\rightarrow A_I' = \dfrac{I_0}{I_b} = \dfrac{-h_{fe}\cdot I_b}{I_b}$

$A_I' = -h_{fe} = -50$

$\rightarrow R_i' = \dfrac{V_{be}}{I_b} = h_{ie} = 1.1k.$

** { $R_i' \neq R_i \rightarrow$ Biasing problem } { R_1 & R_2 is reducing i/p resistance }

$\rightarrow R_i = R_1 \| R_2 \| R_i' = (100k)\|(10k)\|(1.1)k = 980\Omega.$



$\rightarrow A_I = \dfrac{I_0}{I_i}$

$= \dfrac{-h_{fe} I_b}{I_b} \times \dfrac{I_b}{I_i}$ $\quad I_b = \dfrac{R_1 \| R_2 \; I_i}{R_i' + (R_1 \| R_2)} \Rightarrow \dfrac{I_b}{I_i} = \dfrac{9.09}{1.1 + 9.09}$

$\therefore A_I = -50 \times \dfrac{9.09}{10.19} \approx -45$

$\rightarrow A_V = \dfrac{V_0}{V_{be}} = \dfrac{-I_0 \cdot R_L}{I_b \cdot R_i'} = \dfrac{-\cancel{I_b} \cdot h_{fe} \cdot R_L}{\cancel{I_b} \cdot R_i'} = -227.3$

$\rightarrow A_{VS} = \dfrac{V_0}{V_s} = \dfrac{V_0}{V_{be}} \times \dfrac{V_{be}}{V_s} = A_V \cdot \dfrac{V_{be}}{V_s} = A_V \cdot \dfrac{R_i}{R_i + R_s} = -20.5$ { very small due to low i/p resistance }

Ques :- $h_{ie} = 1.1k$

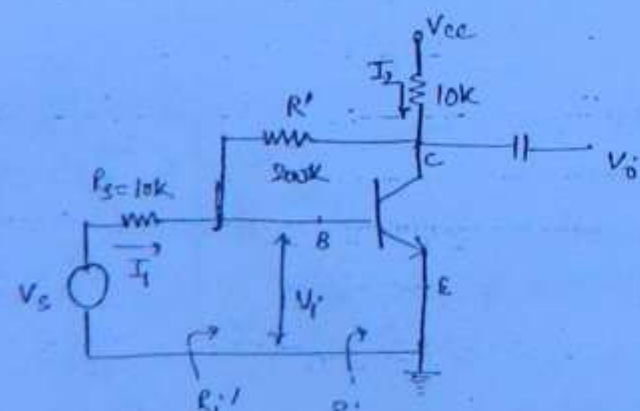
$h_{fe} = 50$

$h_{re} = h_{oe} = 0$

Calculate

$R_i, R_i', A_I,$

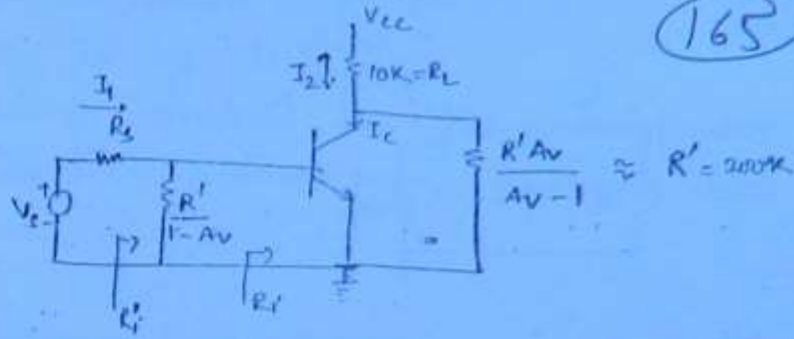
$A_I' = \dfrac{-I_2}{I_1}, A_V, A_s.$



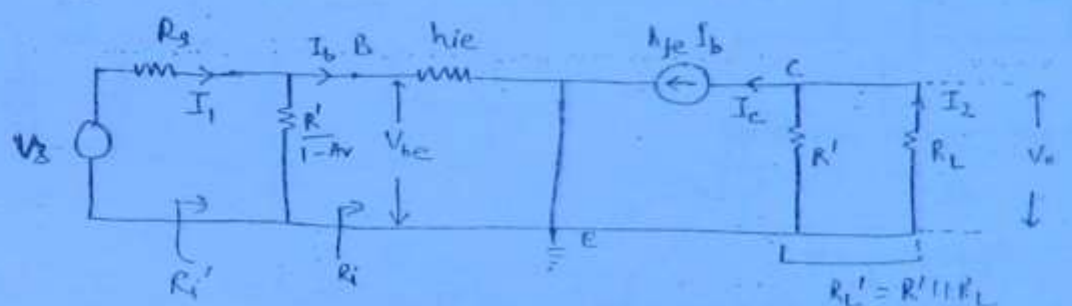
165

Soln · $|A_v| >> 1$ for CE configuration.

Apply Miller's theorem –



Using approximate model –



$$A_v = \frac{V_o}{V_{be}} = \frac{\cancel{I_2} R_L}{\cancel{I_b} h_{ie}} = \frac{\left(\frac{-R' R_L}{R_L + R'}\right) h_{fe}}{h_{ie}} = \frac{(-h_{fe} I_b) \cdot R_L'}{I_b \cdot h_{ie}} = \frac{-h_{fe} R_L'}{h_{ie}} = -433$$

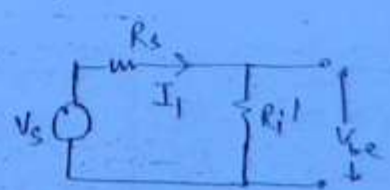
$$A_I = \frac{-I_c}{I_b} = -h_{fe} = -50$$

$$R_i' = \frac{V_{be}}{I_b} = h_{ie} = 1.1K.$$

$$x = \frac{R'}{1-A_v} = \frac{200}{1-(-433)} = 0.46K\Omega$$

$$R_i' = R_i \| \left(\frac{R'}{1-A_v}\right) = 1.1 \| 0.46 = 0.30 K\Omega.$$

∴



$$A_{vs} = \frac{V_o}{V_s} = \frac{V_o}{V_{be}} \times \frac{V_{be}}{V_s}$$

$$= -433 \times \frac{R_i'}{R_s + R_i'}$$

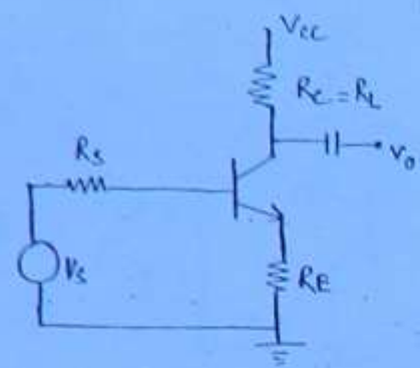
$$A_{vs} = -12.6 \text{ Ans.}$$

$$\Rightarrow A_I' = \frac{-I_2}{I_1} = \frac{V_o/R_L}{V_s/R_s + R_i'}$$

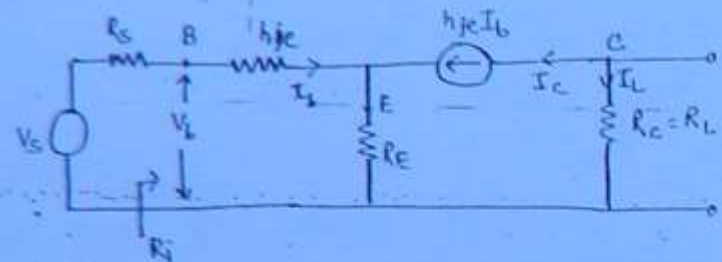
$$\text{or } A_I' = \frac{V_o}{V_s}\left(\frac{R_s + R_i'}{R_L}\right) = (-12.6)\left(\frac{10+0.3}{10}\right) = -12.99 \text{ Ans}$$

Common Emitter with unbypassed emitter resistor, R_E –

→ If $h_{oe}(R_E+R_L) \le 0.1$ then we can use approximate model.



→



→ $A_I = \dfrac{-h_{fe}I_b}{I_b} = -h_{fe}$ ⇒ it will remain unaffected.

→ i/p resistance $R_i = \dfrac{V_b}{I_b}$ –

Applying KVL –

$$V_b = I_b \cdot h_{ie} + R_E(1+h_{fe})I_b$$

$$\Rightarrow \boxed{R_i = h_{ie} + R_E(1+h_{fe})} \Rightarrow R_i \text{ increases}$$

→ $A_V = \dfrac{V_o}{V_b} = \dfrac{-h_{fe} \cdot I_b \cdot R_L}{I_b[h_{ie}+R_E(1+h_{fe})]} \Rightarrow \boxed{A_V = \dfrac{-h_{fe}R_L}{h_{ie}+(1+h_{fe})R_E}}$ ⇒ $A_V \downarrow$ due to –ve feedback

If $(1+h_{fe})R_E >> h_{ie}$ & $h_{fe} >> 1$, then $\boxed{A_V = -\dfrac{R_L}{R_E} = -\dfrac{R_C}{R_E}}$ (approx).

→ Due to –ve feedback, gain is highly stable as it is independent of Tr parameters (which in turn depends on temp.).

→ $A_{V_s} = A_V \cdot \dfrac{R_i}{(R_i+R_s)}$; if $R_i >> R_s$ then $\boxed{A_{V_s} \approx A_V \approx -\dfrac{R_C}{R_E}}$ (approx).

Effect of using R_E –

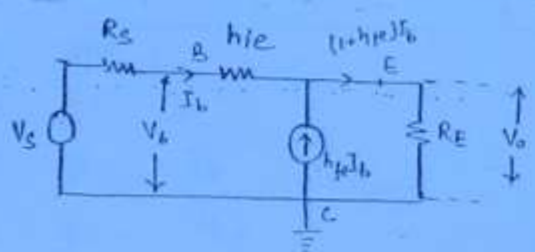
→ Current gain will remain unaffected.

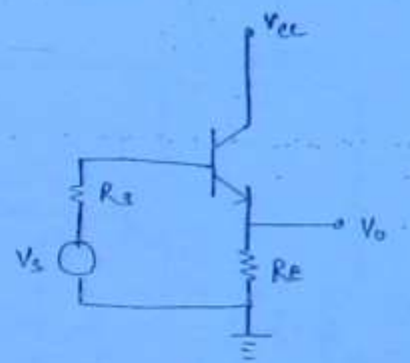
→ i/p resistance ↑es by $(1+h_{fe})R_E$.

→ Voltage gain is stablized., i.e, A_V is independent of any Tr. parameters.

→ o/p resistance ↑es. (current series feedback, check dual of miller ckt).

Common Collector or Emitter Follower :–





→ $A_I = \frac{I_o}{I_b} = \frac{(1+h_{fe})I_b}{I_b} \Rightarrow \boxed{1+h_{fe} = A_I}$, $\phi = 0°$

→ i/p resistance – $R_i = \frac{V_b}{I_b}$ By applying KVL –

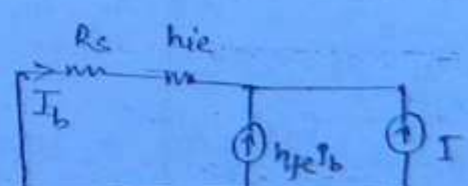
$$V_b = h_{ie} I_b + (1+h_{fe}) I_b \cdot R_E$$

$$\Rightarrow R_i = h_{ie} + (1+h_{fe}) R_E .$$ → (high due to R_E.)

→ Voltage Gain : $A_V = \frac{V_o}{V_b} = \frac{(1+h_{fe}) R_E \cdot I_b}{R_i I_b} \Rightarrow \boxed{A_V = \frac{(1+h_{fe})R_E}{h_{ie} + (1+h_{fe})R_E}}$ (< 1)

If $(1+h_{fe})R_E >> h_{ie}$, $\boxed{A_V = 1}$

→ o/p resistance : R_o –



$$V = (R_s + h_{ie})(I + h_{fe} I_b)$$

$$I_b + h_{fe} I_b + I = 0$$

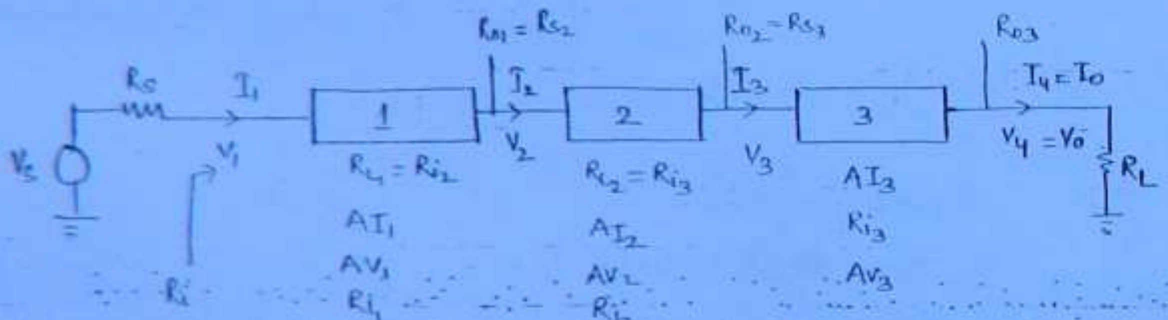
$$\Rightarrow (1+h_{fe}) I_b = -I$$

$$\therefore V = (R_s + h_{ie})\left(I - \frac{I h_{fe}}{1+h_{fe}}\right)$$

$$\Rightarrow \boxed{R_o = \frac{(R_s + h_{ie})}{(1+h_{fe})}}$$

	CE	CE with R_E	CC
A_I	$-h_{fe}$	$-h_{fe}$	$(1+h_{fe})$
R_i	h_{ie}	$h_{ie}+(1+h_{fe})R_E$	$h_{ie}+(1+h_{fe})R_E$
A_V	$\frac{A_I \cdot R_L}{R_i}$	$\frac{-h_{fe} \cdot R_C}{h_{ie}+(1+h_{fe})R_E}$	$\frac{(1+h_{fe})R_E}{h_{ie}+(1+h_{fe})R_E}$
R_o	∞	∞	$\frac{h_{ie}+R_s}{1+h_{fe}}$
R_o'	$R_o \| R_L = R_L$	$R_o \| R_L = R_L$	$R_o \| R_L$

Cascaded Amplifier :-



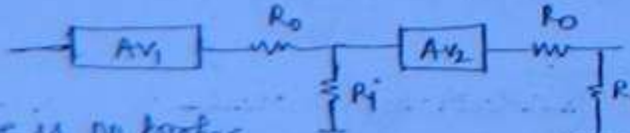
→ $A_V = \frac{V_o}{V_1} = \frac{V_o}{V_3} \times \frac{V_3}{V_2} \times \frac{V_2}{V_1} = Av_3 \cdot Av_2 \cdot Av_1$

→ $20 \log A_V = 20 \log Av_1 + 20 \log Av_2 + 20 \log Av_3$

→ $A_I = \frac{I_o}{I_1} = \frac{I_o}{I_3} \times \frac{I_3}{I_2} \times \frac{I_2}{I_1} = A_{I_3} \cdot A_{I_2} \cdot A_{I_1}$.

→ $20 \log A_I = 20 \log A_{I_3} + 20 \log A_{I_2} + 20 \log A_{I_1}$

→ $A_P = A_V \cdot A_I$.

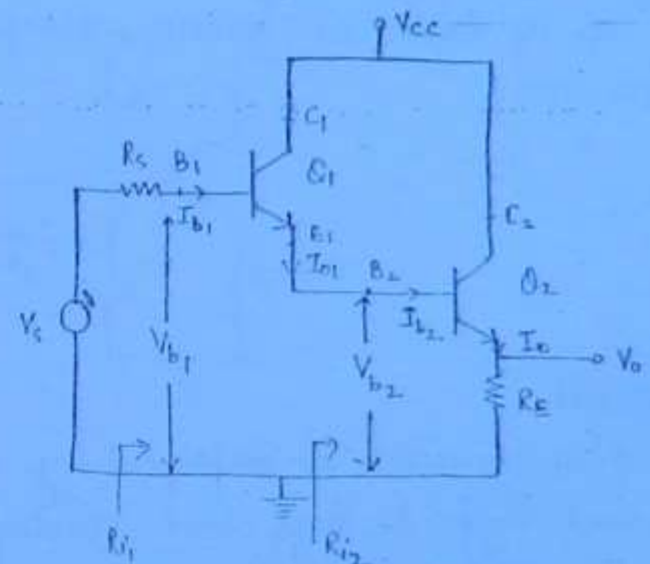
* 

$= Av_1 \times \left(\frac{R_i}{R_i+R_o}\right) \times Av_2 \times \left(\frac{R_i}{R_i+R_o}\right)$

(If there is no proper impedance matching)

* If i/p source is voltage source, then input stage should be common coll
* " " " current " , " " " " " common base
* " o/p is delivering voltage, then last stage should be common collech
* " " " " current, " " " " " " base.
* All the intermediate stages should be common emitter config.
* CC is used in first & last stage due to high R_i & low R_o respec.
* CB " " " " " " " " " low R_i & high R_o " .

Darlington Pair (CC-CC) :-



2nd stage - CC.

$$A_{I_2} = \frac{I_o}{I_{b_2}} = (1+h_{fe})$$

$$R_{i_2} = \frac{V_{b_2}}{I_{b_2}} = h_{ie} + (1+h_{fe})R_E$$

$$\boxed{R_{i_2} \approx (1+h_{fe})\, R_E}$$

$$A_{V_2} = \frac{A_{I_2} \cdot R_L}{R_{i_2}} \Rightarrow A_{V_2} \leq 1$$

1st stage - CC.

$\rightarrow R_{L_1} = R_{i_2} = (1+h_{fe})\, R_E$.

$\rightarrow A_{I_1} = \dfrac{I_{o1}}{I_{b_1}} = (1+h_{fe})$

$\rightarrow R_{i_1} = \dfrac{V_{b1}}{I_{b_1}} = h_{ie} + (1+h_{fe})\, R_{L_1}$

$\Rightarrow R_{i_1} = h_{ie} + (1+h_{fe})^2 R_E$

$\Rightarrow \boxed{R_{i_1} \approx (1+h_{fe})^2 R_E}$ → very large.

$\rightarrow A_{V_1} \leq 1$

Overall current gain -

$$A_I = \frac{I_o}{I_{b_1}} = \frac{I_o}{I_{b_2}} \times \frac{I_{b_2}}{I_{b_1}}$$

$A_I = A_{I_1} \times A_{I_2}$.

$\Rightarrow \boxed{A_I = (1+h_{fe})^2}$

$\rightarrow A_V = A_{V_1} \cdot A_{V_2} \leq 1$.

For n-stages in cascade:-

Assuming $h_{ie} = h_{re} = h_{oe} = 0$,

$$\boxed{R_i = (1+h_{fe})^n \cdot R_E}$$

$$\boxed{A_I = (1+h_{fe})^n}$$

Advantage:-

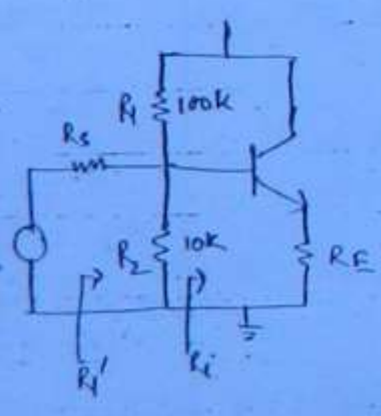
→ Very high current gain Darlington integrated transistor pairs are commercially available with h_{fe} as high as 30,000., therefore this is also called super β transistor.

→ Very large i/p resistance.

Disadvantage:

- Highly expensive circuit.
- leakage current of first transistor is amplified by second, hence the overall leakage current may be high and darlington connection of 3 or ~~more~~ transistor is usually impractical.

Biasing Problem :-



for CC -

$R_i = h_{ie} + (1+h_{fe}) R_E$

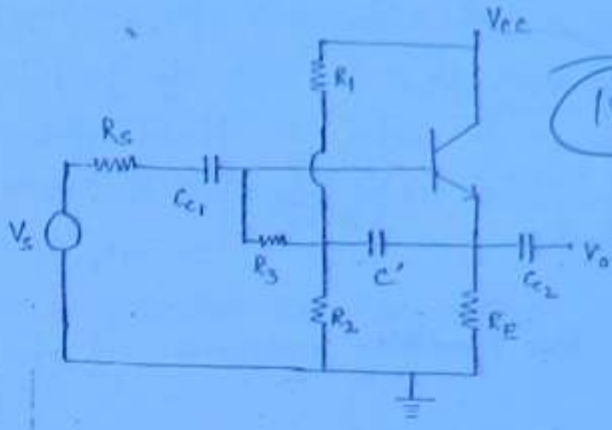
for $h_{ie} = 1k$, $h_{fe} = 99$, $R_E = 2k$

→ $R_i \simeq 200k$.

Now ~~the~~ $R_i' = R_i \| R_1 \| R_2$ and Resultant $R_i' < 10K$. But we need R_i' to be high so that whole V_s is transferred to i/p

→ Even if a darlington pair is attached with $R_i = 2.5 M\Omega$, then also $R_i' < 10K$. This is called biasing problem.

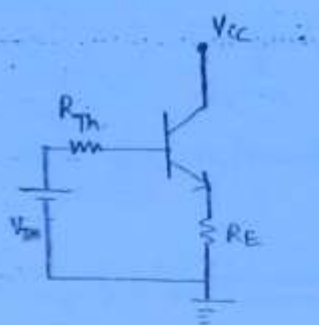
Boot strapping :-



→ value of C' should be very high so that it acts as S.C for AC.

→ for dc analysis, C_{C_1}, C_{C_2} & C' will act as O.C.

DC analysis :



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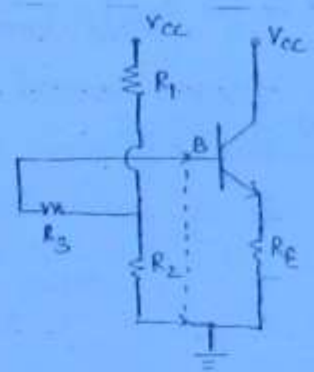

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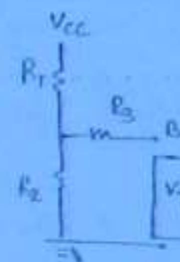
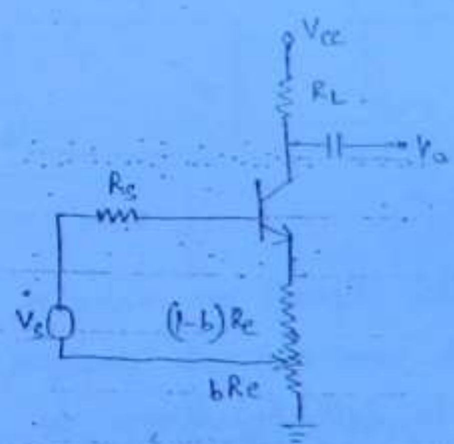


$$\boxed{V_{Th} = \frac{R_2}{R_1+R_2} \cdot V_{CC}}$$

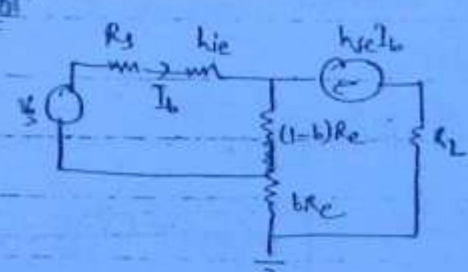
$$\boxed{R_{TH} = (R_1 \| R_2) + R_3}$$

Ques :- Calculate $A_{V_S} = \frac{V_o}{V_s}$

$R_i = \frac{V_s}{I_b}$



Sol^n



$$V_s - I_b(R_s + h_{ie}) - (1-b)R_e(1+h_{fe})I_b = 0$$

$$\Rightarrow \frac{V_s}{I_b} = (R_s + h_{ie}) + (1-b)(1+h_{fe})R_e = R_i$$

$$V_o = -h_{fe} I_b \cdot R_L$$

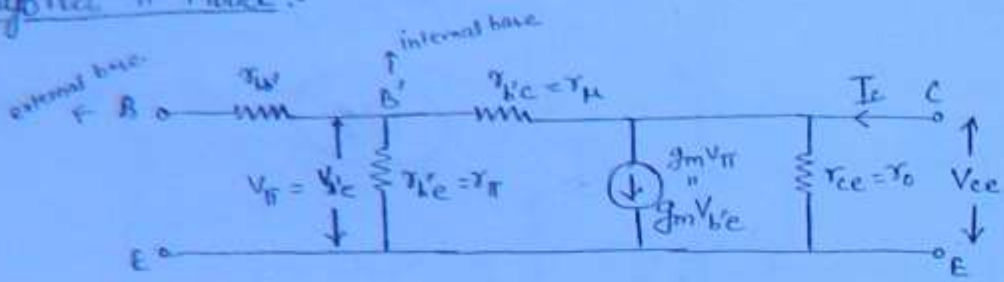
if b ↑, then R_i ↓es, gain ↑es.

$$A_{V_S} = \frac{V_o}{V_s} = \frac{V_o}{I_b} \times \frac{I_b}{V_s} \Rightarrow A_{V_S} = \frac{-h_{fe} R_L}{(R_s + h_{ie}) + (1-b)(1+h_{fe})R_e}$$

06 Sep.

Hybrid π Model :-

172



→ $r_{bb'}$ or r_b = ohmic base spreading resistance (small A, R↑ for base).

→ $r_{ce} = r_0$ → early effect.

→ $g_m V_{b'e}$ ⇒ shows dependence of I_c on I_B (or V_{BE}).

→ $r_{b'e}$ ⇒ forward junc^n resistance.

→ $r_{b'c}$ ⇒ shows early effect for J_c junction → high.

→ g_m = Transconductance ⇒ $\boxed{g_m = \frac{|I_{cQ}|}{V_T}}$; $V_T = \frac{T}{11600}$ volt

→ $\boxed{r_{b'e} = r_\pi = \frac{h_{fe}}{g_m} = \frac{\beta}{g_m}}$

→ $I_c = g_m V_\pi + \underbrace{\frac{V_{ce}}{r_0}}_{\text{early effect}}$

→ g_m and r_π in model depends on value of dc quiescent current I_{cQ} and hence provide more accurate analysis of transistor.

→ Model is applicable to both pnp & npn tr w/o change of polarities.

→ Tr. is represented as a VCCS.

→ $r_{bb'}$:- Base region of Tr. is very thin compared to emitter & collector region & its resistance lies b/w 40 to 400Ω. The ohmic resistance of E & C is usually of order of 10Ω. and can be neglected in comparison to that of base region.

→ r_π → Incremental resistance of E-B diode which is FB in active region

→ r_μ → It accounts for feedback from o/p to i/p due to base width modulation or early effect. The value of r_μ is usually very high (several $M\Omega$) and will be neglected in analysis.

123

→ r_0 → o/p resistance and is also due to Early effect.

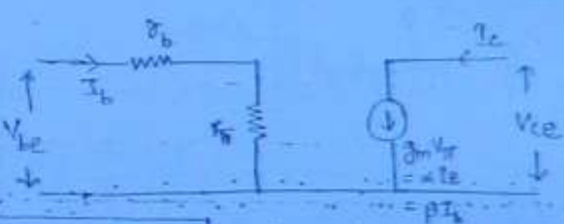
$$\boxed{r_0 = \frac{V_A}{|I_{cQ}|}}$$

→ $g_m V_\pi$ → any small signal voltage V_π at emitter junction results in a signal collector current $g_m V_\pi$ when $V_{CE} = 0$. BJT is represented as a VCCS when controlled current is $g_m V_\pi$ & controlling voltage is V_π. g_m represents transconductance of Tr.

Simplified / Approximate Model :-

$$g_m = \frac{|I_{cQ}|}{V_T}, \quad r_\pi = \frac{\beta}{g_m}$$

$$r_\pi = \frac{h_{fe}}{g_m} = \frac{\beta}{g_m}$$

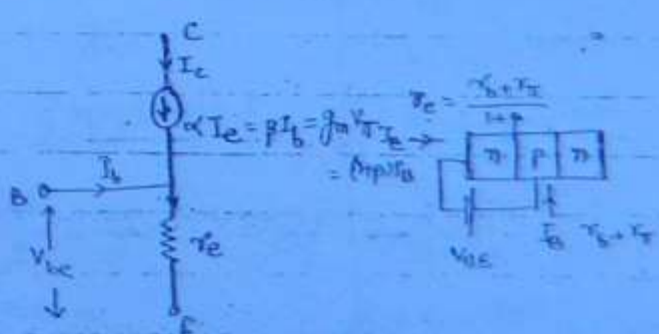


$$\boxed{R_i = \frac{V_{be}}{I_b} = r_b + r_\pi}$$

r_e or T-Model :-

$$r_e = \frac{V_T}{|I_{EQ}|}$$

$$\frac{V_{be}}{I_b} = \boxed{R_i = (1+\beta) r_e}$$



* $\boxed{r_b + r_\pi = (1+\beta) r_e = h_{ie}}$ ** ; $\boxed{g_m V_\pi = \beta I_b = \alpha I_e}$ **

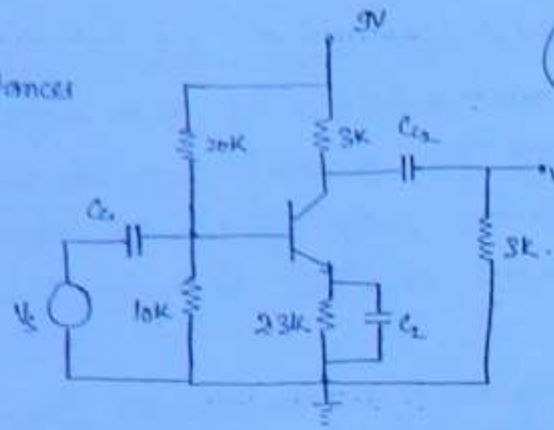
$r_b \ll r_\pi$, $\beta \gg 1$ ∴ $\boxed{r_\pi = \beta r_e = h_{ie}}$

Ques:- $V_{BE} = 0.7V$, β & all capacitances are v. large.

$r_e = \frac{25mV}{|I_E|}$

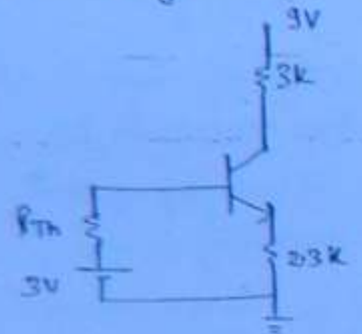
→ Find dc biasing current I_E

→ Find midband voltage gain.



Sol^n Method I

DC analysis—



$I_B \approx 0$.

$3 - 0.7 = 2.3K\, I_E$

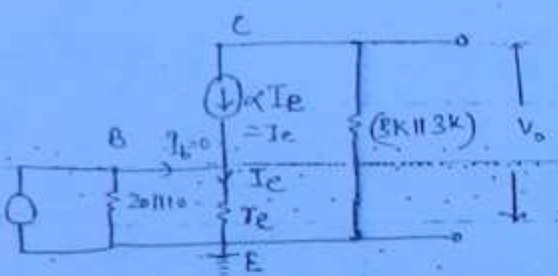
$\Rightarrow I_E = 1mA$

$\therefore r_e = \frac{25mV}{1mA} = 25\Omega$.

AC analysis—

C_1, C_{C2}, C_2 will act as short.

$I_b \approx 0,\ \alpha = 1 \quad \{\because \beta = \text{very high}\}$



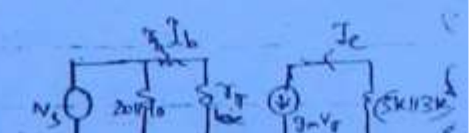
$V_s = I_e r_e$

$V_o = (-1.5K)\alpha I_e$

$\therefore \frac{V_o}{V_s} = \frac{-1.5 \times 10^3}{25} = -60$.

Method II

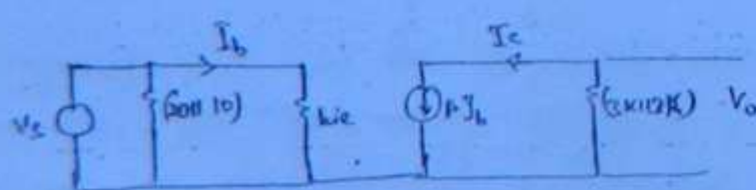
$r_e = \frac{V_T}{|I_E|} = \frac{V_T}{|I_C|} \{\because \beta = \text{large}\} = 1/g_m$



$\therefore g_m = 1/25$

$\frac{V_o}{V_s} = \frac{g_m v_\pi (1.5K)}{I_b(r_b + r_\pi)} = \frac{-\beta I_b (1.5K)}{I_b(\beta r_e)} = -60$

Method III



$\frac{V_o}{V_s} = \frac{-\beta I_b \cdot (1.5K)}{I_b \cdot h_{ie}} = \frac{-1.5K}{r_e} = -60$.

$r_b + r_\pi = h_{ie} = (1+\beta) r_e$.

$h_{ie} = \beta r_e$

$\Rightarrow h_{ie}/\beta = r_e$.

Note

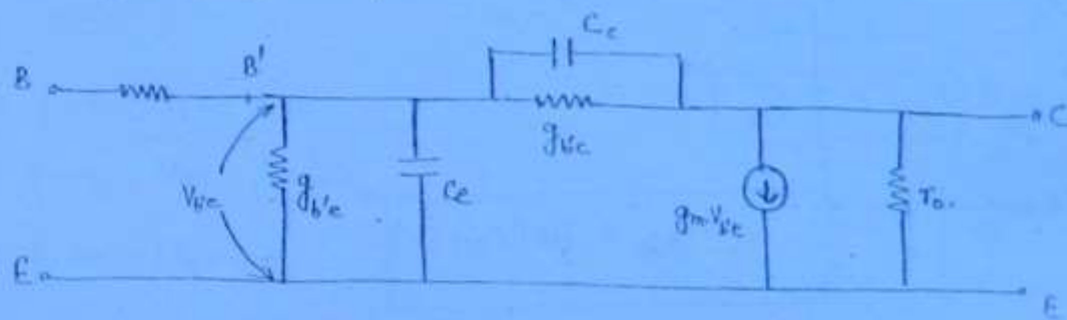
* If R_E is unbypassed – $\boxed{\frac{V_o}{V_s} = \frac{-R_C}{R_E + r_e} \simeq \frac{-R_C}{R_E}}$ ** → (overestimated).

* If R_E is bypassed – $\boxed{\frac{V_o}{V_s} = -\frac{R_C}{r_e}}$ **

* If an extra R_L is present in o/p –

$$\boxed{\begin{aligned} R_E \text{ unbypassed} &= \frac{-(R_C \parallel R_L)}{R_E} \\ R_E \text{ bypassed} &= \frac{-(R_C \parallel R_L)}{r_e} \end{aligned}}$$ **

High Frequency Analysis of BJT :-



Giacoletto Model

→ $g_{b'e} = 1/r_{b'e} = \frac{g_m}{h_{fe}}$

→ $g_{b'c} = 1/r_{b'c}$

$\because r_{b'c} >> r_{b'e}$

$\Rightarrow g_{b'c} << g_{b'e}$

→ $g_m = \frac{|I_c|}{V_T}$

→ $C_\pi = C_e = C_D$ → Diffusion capacitance

→ $C_c = C_T = C_{ob} = C_\mu$ → Transition capacitance

Typical Values

→ $g_m = 50\,mA/V$

→ $r_b = r_{bb'} = 100\Omega$

→ $r_{b'e} = r_\pi = 1K$

→ $r_{b'c} = 4M\Omega$

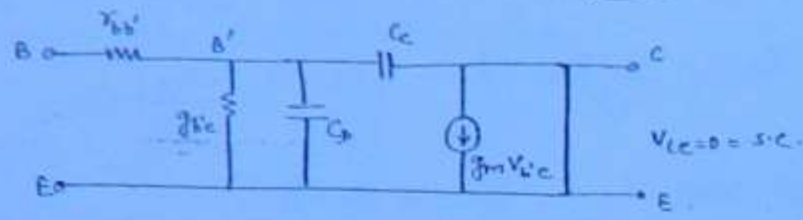
→ $r_o = r_{ce} = 80K$

→ $C_c = 3pF$

→ $C_D = C_e = 100pF$

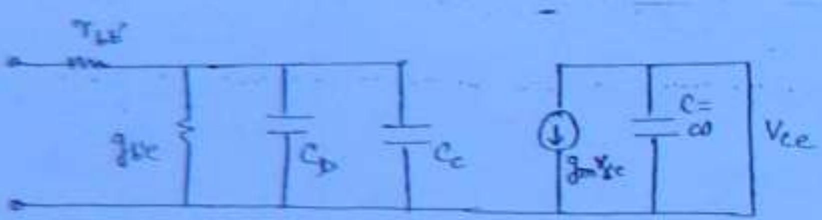
CE short circuit current gain :-

→ $A_V = \frac{V_{ce}}{V_{b'e}} = 0$.



→ Now applying Miller's theorem –

$C_1 = C_c(1 - A_V) = C_c$; $C_2 = \frac{C_c(A_V - 1)}{A_V} = \infty$ (short).



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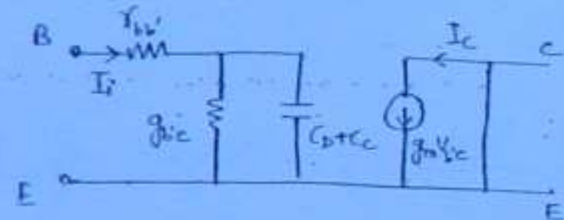


i/p capacitance :- $\boxed{C_i = C_D + C_c}$ **

i/p conductance :- $\boxed{Y_i = \frac{I_i}{V_{b'e}} = g_{b'e} + j\omega(C_D + C_c)}$ **

Current gain :-

$$A_I = \frac{I_o}{I_i} = \frac{-g_m \cdot V_{b'e}}{V_{b'e} \cdot Y_i} \Rightarrow A_I = \frac{-g_m}{Y_i}$$

$$\Rightarrow \boxed{A_I = \frac{-g_m}{g_{b'e} + j\omega(C_D + C_e)}}$$ → This will act as LPF at higher frequency.

Rearranging, $A_I = \frac{-g_m / g_{b'e}}{1 + j\omega \frac{(C_D + C_e)}{g_{b'e}}}$, Now $\because r_{b'e} = \frac{1}{g_{b'e}} = \frac{h_{fe}}{g_m}$

$\Rightarrow g_m / g_{b'e} = h_{fe}$.

$$\Rightarrow \boxed{A_I = \frac{-h_{fe}}{1 + j\omega \cdot \frac{(C_D + C_e)}{g_{b'e}}}}$$ **

$\rightarrow |A_I| = \dfrac{h_{fe}}{\sqrt{1+\left[\dfrac{\omega(C_D+C_e)}{g_{b'e}}\right]^2}}$, $|A_I|_{max} = h_{fe}$ at $\omega = 0$.

177

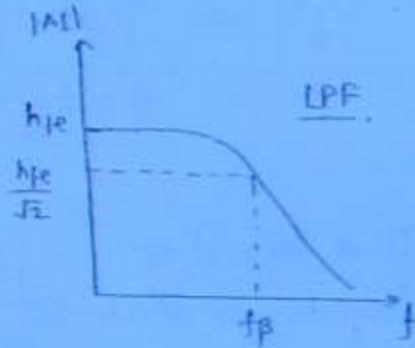
$\rightarrow$ At $\omega = \omega_\beta$, $|A_I| = |A_I|_{max}/\sqrt{2}$ $\Rightarrow \dfrac{h_{fe}}{\sqrt{2}} = \dfrac{h_{fe}}{\sqrt{1+\left[\dfrac{\omega_\beta(C_D+C_e)}{g_{b'e}}\right]^2}}$

On solving, -

$$\boxed{\omega_\beta = 2\pi f_\beta = \frac{g_{b'e}}{C_D+C_e}} \quad \text{or} \quad \boxed{f_\beta = \frac{1}{2\pi\, r_{b'e}\,(C_D+C_e)}}$$

f_β = 3dB cutoff freq.

Hence, $\boxed{A_I = \dfrac{-h_{fe}}{1+j(\omega/\omega_\beta)} = \dfrac{-h_{fe}}{1+j(f/f_\beta)}}$



$\rightarrow$ At $f=0$, $|A_I| = h_{fe}$

At $f = f_\beta$, $|A_I| = h_{fe}/\sqrt{2}$

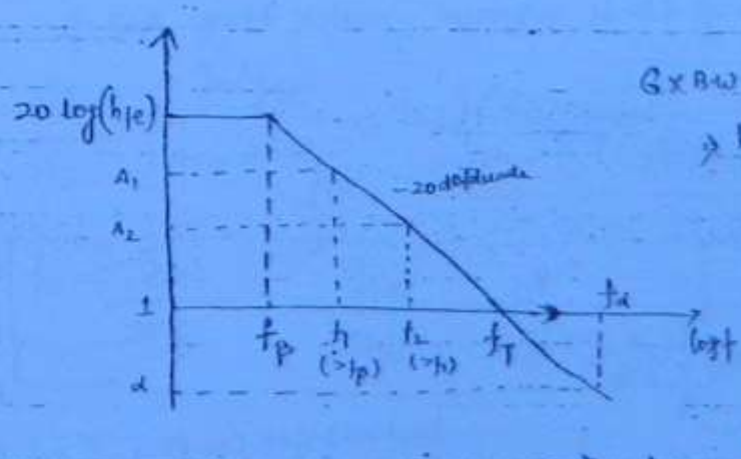
At $f = \infty$, $|A_I| = 0$.

$\rightarrow$ At $f = f_T$, $|A_I| = 1$ $\rightarrow$ frequency till transistor will act as amplifier.

$$1 = \frac{h_{fe}}{\sqrt{1+(f_T/f_\beta)^2}} \Rightarrow \left(\frac{f_T}{f_\beta}\right)^2 = h_{fe}^2 - 1 \Rightarrow \left(\frac{f_T}{f_\beta}\right)^2 \approx h_{fe}^2$$

Bode Plot :

$\Rightarrow \boxed{f_T = h_{fe} \cdot f_\beta} \Rightarrow f_T >> f_\beta$.



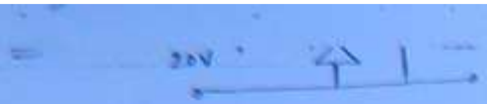
$G \times BW$ = constant

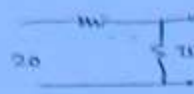
$\Rightarrow h_{fe} \cdot f_\beta = A_1 \cdot f_1 = A_2 f_2 = f_T = \alpha \cdot f_x$

$\boxed{f_T = \text{unity gain bandwidth product}}$

$$f_T = h_{fe} f_\beta = \frac{h_{fe} \cdot g_{b'e}}{2\pi(C_D+C_e)}$$

$\Rightarrow$ ~~f_T~~





$V_Z' = \frac{75}{225} \times 20 = 6.67V\ (< 10V)$

hence zener is not in BD

Hence, $I_Z = 0$, $P_Z = 0$, $V_0 = 6.67V$ $(\neq 10V)$

** V.V. Imp

→ $\boxed{f_T = \dfrac{g_m}{2\pi(C_D + C_e)}}$

(178)

→ $\boxed{f_\beta << f_T < f_\alpha}$; f_α = frequency at which gain < 1, i.e., gain of CB = α

$h_{fe} \cdot f_\beta = \dfrac{h_{fe}}{1+h_{fe}} \cdot f_\alpha \Rightarrow \boxed{f_\alpha = (1+h_{fe}) f_\beta}$ **

& $\boxed{f_T = h_{fe} f_\beta}$ **

→ $f_\beta \Rightarrow$ 'β' cutoff frequency and also called as bandwidth of CE at high freq. Typical value —

$$\boxed{f_\beta = 1.6\ MHz.}$$

→ $f_T \Rightarrow$ It is defined as

1> Frequency at which SC CE current gain attains unit magnitude.

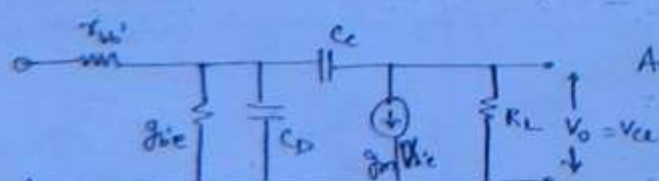
2> Highest freq. upto which CE tr. will be working as an amplifier.

3> freq. where CE tr. β reduces to unity.

4> Unity gain bandwidth product of CE tr. and this ($G \times BW$) is limited by junc^n capacitance.

→ $f_\alpha \Rightarrow$ 'α' cutoff frequency. It is also called BW of CB transistor at high frequency. The BW of CB is always greater than BW of CE or BW of CC. tr.

Common Emitter with Resistive load R_L :-



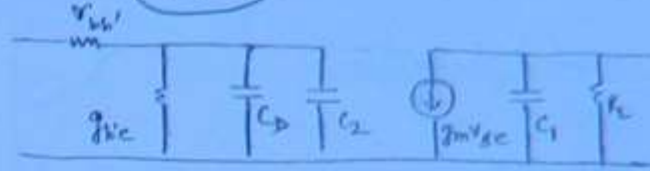
$A_V = \dfrac{V_{ce}}{V_{b'e}} = \dfrac{V_0}{V_{b'e}}$.

$|A_V| >> 1$ for CE Tr.

Apply Miller's theorem —

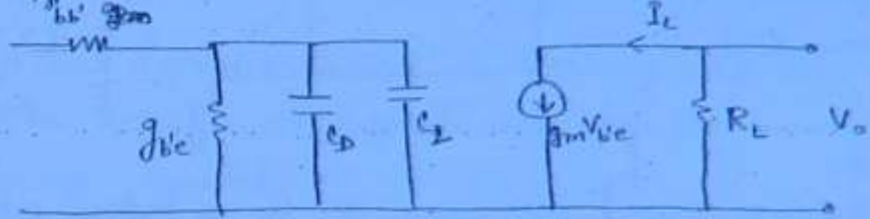
$C_2 = C_c(1-A_v)$

$C_1 = \frac{C_c(A_v-1)}{A_v} \approx C_c \quad \{\because |A_v| \gg 1\}$



$Z_{C_1} = \frac{1}{2\pi f C_1}$; $C_1 \equiv pF$ even if $f \equiv MHz \Rightarrow Z_C \approx 10^6\,\Omega \Rightarrow Z_C \parallel R_L = R_L$

Therefore, approximate model —



Now,

$A_V = \frac{-g_m V_{b'e} \cdot R_L}{V_{b'e}}$

$\Rightarrow \boxed{A_V = -g_m R_L}$

$\therefore C_2 = C_c(1 + g_m R_L)$.

$\therefore \rightarrow$ Input capacitance :- $\boxed{C_i = C_D + C_c(1 + g_m R_L)}$

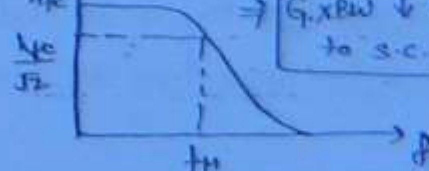
$\rightarrow$ Input conductance :- $\boxed{Y_i = g_{b'e} + j\omega C_i}$

$\rightarrow$ Due to miller's effect, $C_i \uparrow$, $Y_i \uparrow$, $Z_i \downarrow \Rightarrow$ Gain $\downarrow$.

$\rightarrow \quad \left.\begin{array}{l} I_o = -g_m V_{b'e} \\ I_i = Y_i \cdot V_{b'e} \end{array}\right\} \quad \therefore A_I = \frac{I_o}{I_i} = \frac{-g_m}{Y_i} \Rightarrow A_I = \frac{-g_m}{g_{b'e} + j\omega C_i}$

$\therefore A_I = \frac{-g_m/g_{b'e}}{1 + j\omega C_i/g_{b'e}} \Rightarrow \boxed{A_I = \frac{-h_{fe}}{1 + j(\omega/\omega_H)} = \frac{-h_{fe}}{1 + j(f/f_H)}}$

$\rightarrow \boxed{f_H = \frac{g_{b'e}}{2\pi C_i} = \frac{g_{b'e}}{2\pi(C_D + C_c(1 + g_m R_L))}}$; f_H = 3dB cutoff frequency



$\rightarrow$ G.×BW ↓ as comp to S.C. CE

$\rightarrow \boxed{f_H < f_\beta}$; $\boxed{f_\beta = \lim_{R_L \to 0} f_H}$

$\Rightarrow \boxed{GBW_{R_L} < GBW_{sc}}$

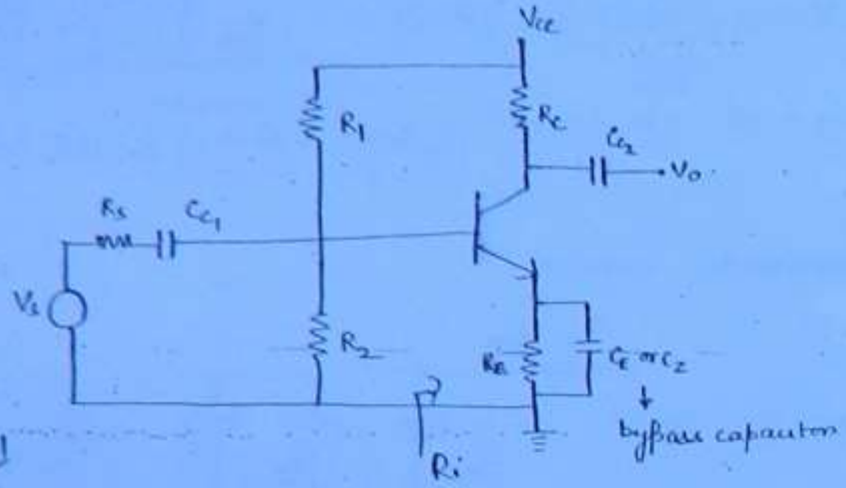
Multistage Amplifiers :-

RC coupled Amplifier :-

1) Single stage —

→ Audio freq. amplifier (20Hz – 20KHz)

→ CE configuration, ie, 180° phase shift

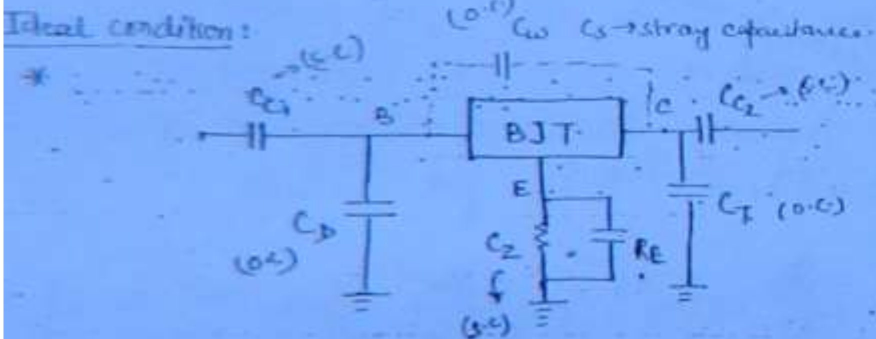


$R_i = h_{ie} + (1+\beta)R_E$ $R_i = h_{ie} + \cancel{R_E}$

$R_i \uparrow$, $A_v \downarrow$ $A_v \uparrow$, $R_i \downarrow$

* C_Z is bypass capacitor & its value should be high so that its will act as short for AC.

Ideal condition :



$C_{C_1}, C_{C_2}, C_Z \rightarrow$ very high

$C_D, C_T \rightarrow pF$

$C_S, C_W \rightarrow 10^{-14} F$

$$Z_C = \frac{1}{2\pi f C}$$

Low Frequency

→ As $f \downarrow$, $Z_C \uparrow$

∴ All capacitive impedancy → ∞, and they will act as O.C. Gain will ↓ due to C_{C_1}, C_{C_2} & C_Z.

Mid frequency

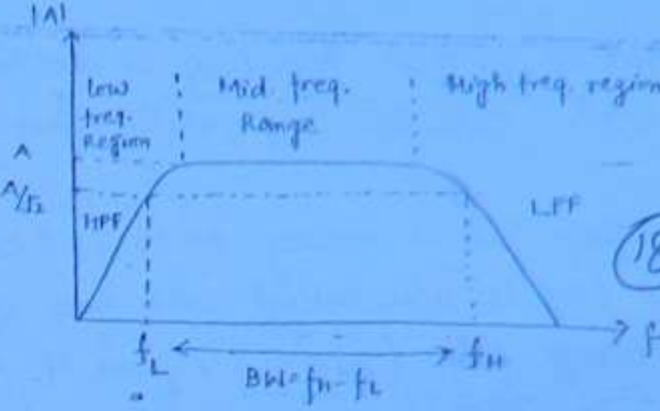
→ Z_C is not decided by f, decided by the value of C. Hence, ideal condⁿ achieved and gain is independent of freq.

High frequency

→ As $f \uparrow$, $Z_C \downarrow$,

∴ All capacitive Impedance → 0 and they will act as short. Gain will ↓ due to C_D, C_T, C_S, C_W.

→ Frequency Response Curve :-



(181)

Important Point —

→ It is audio freq. amplifier.

→ Single stage RC couple introduce a phase shift of 180° & two stages introduce 360° or 0°.

→ Coupling capacitors (C_{c1} & C_{c2}) are also called dc blocking capacitors (C_{b1} & C_{b2}) and are used to couple ac signals and simultaneously block dc current or biasing current.

→ By using emitter resistor, w/o a bypass capacitor, there will be a -ve feedback across R_E. and this reduces the voltage gain and ↑s i/p resistance of amplifier.

→ Bypass capacitor (C_Z or C_E) is used to bypass ac signal current through it. For dc current or biasing current, C_Z is open. By using C_Z, -ve feedback (due to ac signal) across R_E is eliminated, therefore voltage gain ↑ and i/p resistance ↓.

→ In an amplifier, for better performance, R_E & C_E combination is used.

Freq. Response Curve :-

→ The fall of gain in low freq. region is due to effect of C_{c1}, C_{c2} and C_Z.

→ In mid frequency region, all coupling & bypass capacitor will be treated as ac short. All junc^n capacitors (C_D & C_T), wiring capacitor (C_W) & stray capacitor (C_S) will be treated as open.

→ The gain of amp is max & almost independent of f at mid freq. and hence the amplifier analysis is generally done at mid freq. range.

→ The fall of gain at high freq is due to the effect of jun^n capacitor (C_b, C_T) & C_w, C_s. and early effect.

(182)

→ High freq. fall is mainly due to C_D & C_c.
→ cutoff freq. is also called 3dB freq. or half power freq.
→ At cutoff freq. (f_H or f_L), gain of amp reduces to 70.7% of peak value, ie, $|A_{md}|/\sqrt{2}$. and o/p power of amplifier is reduces to 50% of peak value.

→ At cutoff frequency, the relative gain of amp is reduced by 3dB from its peak value.

Bandwidth :-

→ It is the band of i/p signal frequencies where the gain of amp. is almost constant.
→ $\boxed{BW = f_H - f_L}$

⇒ Larger BW indicates better reproduction of i/p signal.
→ In an amplifier, gain - bandwidth product is always constant, ie, when one ↑es, other ↓es & vice versa.

Disadvantage :- Smaller gain × BW.

Note - Amplifiers are connected in cascade to get larger Gain × BW product.

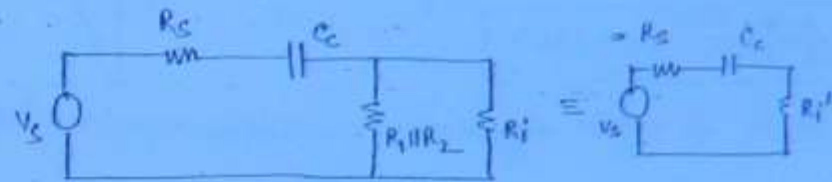
Calculation of f_L :-

(183)

→ f_L due to C_{c_1} :- Assume C_{c_2} & $C_E \to \infty$ & act as s.c

→ We can replace transistor with its input resistance.

→ $R_i = h_{ie} = \beta r_e = r_\pi + r_b$.



→ $R_i' = R_1 \| R_2 \| R_i \approx R_i$

$\therefore f_L = \frac{1}{2\pi R_{eq} C} \Rightarrow \boxed{f_L = \frac{1}{2\pi (R_s + R_i') \cdot C_c}}$

→ for high BW, C_c & R_i' values should be as high as possible.
(R_s should not be high as it will ↑ loss in i/p)

→ f_L due to C_{c_2} :- Assume C_{c_1} & $C_E \to \infty$ & acts as s.c

→

$\therefore \boxed{f_L = \frac{1}{2\pi (R_c + R_L) \cdot C_c}}$

* If f_L due to C_{c_1} & C_{c_2} is different then take the bigger value.
* If f_H due to C_w / C_s or C_D, C_T " " " " smaller value.

Low frequency Analysis .

→ RC coupled amplifier acts as HPF for low freq.

→ Total phase shift $= \underset{\text{due to CE config}}{180^\circ} + \underset{\text{due to HPF}}{\tan^{-1}\left(\frac{f_L}{f}\right)} \Rightarrow \boxed{\text{At } f = f_L,\ \phi_T = 225^\circ}$ obj ***

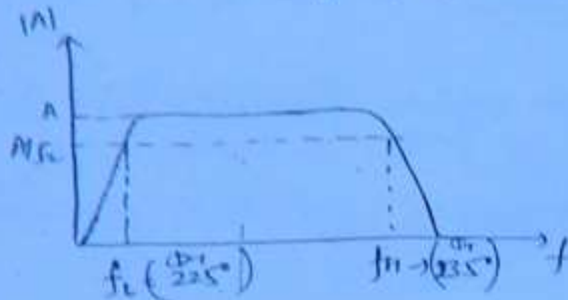
→ $A = \frac{1}{1 - j(f_L/f)}$

High freq. analysis :-

→ $A = \frac{1}{1+j(f/f_H)}$: RC coupled amplifier acts as LPF at high freq.

→ $\phi_T = 180 - \tan^{-1}\left(\frac{f}{f_H}\right)$.

→ $\boxed{\text{At } f = f_H, \quad \phi_T = 135^\circ}$



Cascaded Amplifier / Multistage Amplifier :-

1) Amplifiers are connected in cascade to get larger gain × BW.

→ When amplifiers are connected such that o/p of one is given to i/p to other, they are said to be cascaded.

- When amplifiers are cascaded, proper impedance matching must be provided in b/w stages so that —
    1) o/p will not be distorted.
    2) Max. power will be transferred from one to another stage.

Note: If mismatch is more in amplifier, o/p will be highly distorted.

Different types of coupling —

i) RC coupling → (for voltage amplifier)

ii) Transformer coupling → (for power amplifiers)

iii) Direct coupled → (basically used for dc amplification).

→ In a multistage amplifier, G×BW = constant.

Note → G×BW of two stage amplifier is greater than that of single stage amp.

→ In multistage amp, BW reduces.

Bandwidth of Multistage Amplifier :- (Basics)

185

$\rightarrow BW^* = f_H^* - f_L^*$
$\rightarrow BW = f_H - f_L$

$BW^* \rightarrow$ Bandwidth of multistage Amp.
$BW \rightarrow$ " " single stage amp.
$f_H^*/f_L^* \rightarrow$ High/low 3dB cutoff freq. of multistage A
$f_H/f_L \rightarrow$ " " " " single stage

Case - n-identical non-interacting (proper impedance matching) stages in cascade

Derivation of f_H^* :-

Gain for individual stage, $|A| = \frac{1}{\sqrt{1+(f/f_H)^2}}$

for n-such stages, $|A^*| = \left[\frac{1}{\sqrt{1+(f/f_H)^2}}\right]^n$

$\rightarrow$ At $f=0$, $|A^*_{max}| = 1$.

$\rightarrow$ At $f = f_H^*$, $|A^*| = 1/\sqrt{2} \Rightarrow \frac{1}{\sqrt{2}} = \left[\frac{1}{1+(f_H^*/f_H)^2}\right]^{n/2}$

$$\Rightarrow \boxed{f_H^* = f_H\left[\sqrt{2^{1/n}-1}\right]}$$

$\rightarrow \boxed{f_H^* < f_H}$,

$n=2$, $f_H^* = 0.64\, f_H$
$n=3$, $f_H^* = 0.51\, f_H$

Derivation of f_L^* :-

Gain for individual stage, $|A| = \frac{1}{\sqrt{1+(f_L/f)^2}}$

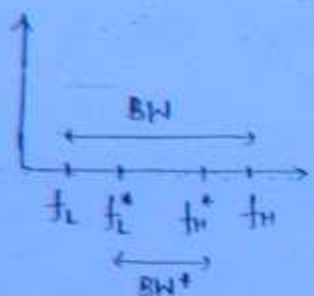
for n-such stages, $|A^*| = \left[\frac{1}{\sqrt{1+(f_L/f)^2}}\right]^n$

→ At $f = \infty$, $|A^*_{max}| = 1$.

→ At $f = f_L^*$, $|A^*| = 1/\sqrt{2}$ ⇒ $\frac{1}{\sqrt{2}} = \left[\frac{1}{\sqrt{1+\left(f_L/f_L^*\right)^2}}\right]^n$

⇒ $\boxed{f_L^* = \frac{f_L}{\sqrt{2^{1/n}-1}}}$ *imp

→ $\boxed{f_L^* > f_L}$; $n=2$ $f_L^* = 1.56$, $n=3$ $f_L^* = 1.96$

* 

$\boxed{BW^* < BW}$ → There is shrinkage in BW.

Approximate Bandwidth :- → $BW = f_H - f_L \cong f_H$ $(f_H >> f_L)$

→ $BW^* = f_H^* - f_L^* \cong f_H^*$ $(f_H^* >> f_L^*)$

⇒ $\boxed{BW^* = \left(\sqrt{2^{1/n}-1}\right) \cdot BW}$; $(BW^* < BW)$

Case - n- non-identical interacting (ie, no proper impedance matching). stages in cascade.

→ $\boxed{\frac{1}{f_H^*} = 1.1 \times \sqrt{\frac{1}{f_{H_1}^2} + \frac{1}{f_{H_2}^2} + \cdots + \frac{1}{f_{H_n}^2}}}$

→ $\boxed{f_L^* = 1.1 \times \sqrt{f_{L_1}^2 + f_{L_2}^2 + \cdots f_{L_n}^2}}$

→ Rise time, $\boxed{t_r^* = 1.1 \times \sqrt{t_{r_1}^2 + t_{r_2}^2 + \cdots + t_{r_n}^2}}$

→ If t_{r_0} = Rise time of signal, $\boxed{t_r^* = 1.1 \times \sqrt{t_{r_0}^2 + t_{r_1}^2 + t_{r_2}^2 + \cdots t_{r_n}^2}}$

Note Disadvantages

→ BW ↓

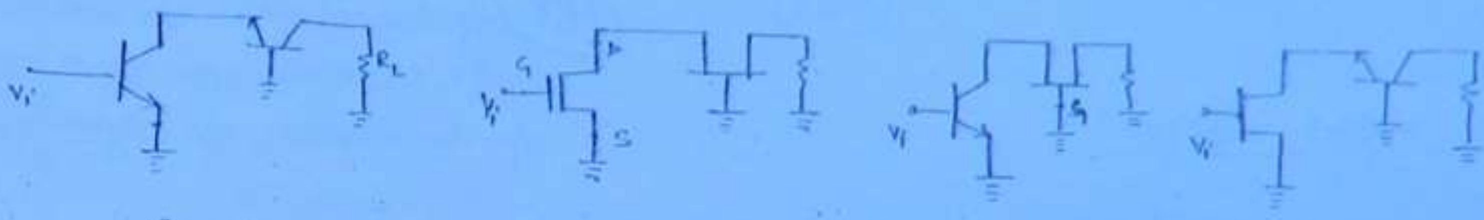
→ Rise time ↑

(due to multistag

∴ (slow response)

07th sep, 2012

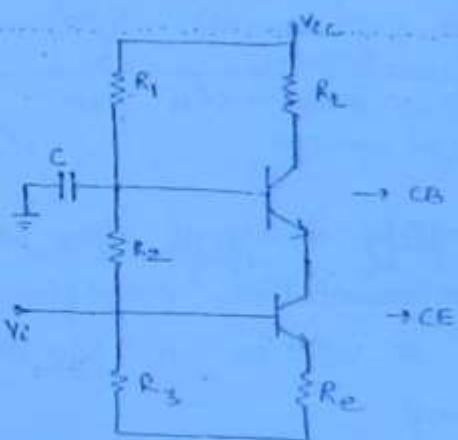
Cascode Amplifier :



CE – CB   CS – CG   CE – CG   CS – CE

→ These all are series connections.

Basic Diagram:



→ C → Bypass capacitor ; its value should be very low so that it charges quickly.

→ Purpose of this 'C' is to maintain CB in active region.

Transconductance -

$$g_{m_1} = \frac{I_{o1}}{V_s}$$

for CB, $A_I \approx 1$, it acts as buffer. for current.

$$\therefore \quad g_m = \frac{I_o}{V_s} = \frac{\alpha I_{o1}}{V_s} \Rightarrow \boxed{g_m = \frac{\beta}{1+\beta} \cdot g_{m_1}} - \text{(exact)} \qquad g_m \approx g_{m_1}$$

if $\beta = 100$,

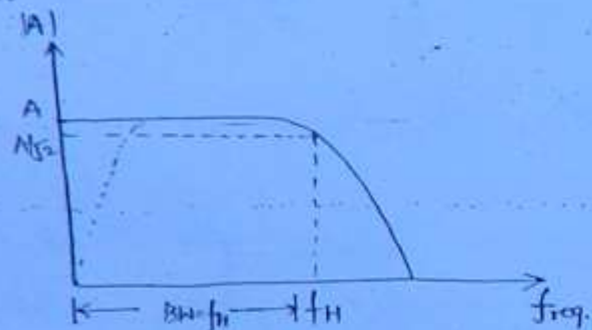
Imp. Points :-

→ It is specially designed multistage amplifier The type of coupling provide is direct coupled, therefore suitable to amplify ac & dc signal but major application is as a high freq. amplifier.

→ The i/p resistance is equal to i/p resistance CE & o/p resistance is decided by o/p resistance of CB.

Direct Coupled Amplifier :

Frequency curve :-



→ It is suitable to amplify dc signal along with a wideband of AC signals.

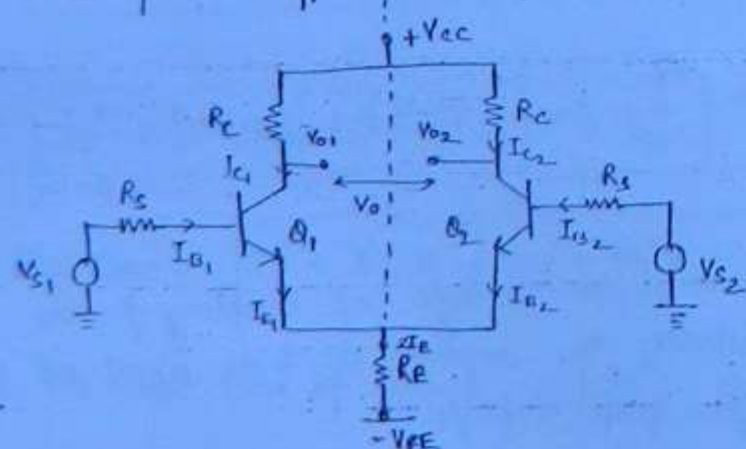
→ Widely used as instrumentation amplifier.

→ There is no proper dc isolation in b/w the stages, therefore stability is less.

→ Any direct coupled D.C amplifier suffers from drift problem. Drift problem is mainly due to I_{CO}. { gain or o/p of amp. drift with temp as I_{CO} changes }

→ Popularly used direct coupled amp is emitter coupled differential amp.

Emitter Coupled Differential Amplifier :-



$V_O = V_{O1} - V_{O2}$ → Balanced o/p.

(Q_1, Q_2 are almost identical)

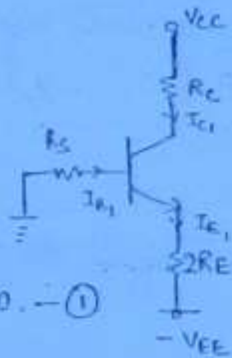
Mode of operation –

1) Dual i/p balanced o/p.
2) Dual i/p unbalanced o/p.
3) Single i/p balanced o/p.
4) Single i/p unbalanced o/p.

DC Analysis :–

→ $V_{s_1} = V_{s_2} = 0$

Applying KVL –



→ (because of feedback)
(potential, should be equal to $2I_E R_E$ but I_{E_1} cannot be doubled, hence resistance is doubled)

$I_{B_1} R_s + V_{BE} + (1+\beta) I_{B_1} \cdot 2R_E - V_{EE} = 0$. — (1)

$V_{CC} = I_{C_1} R_C + V_{CE} + (1+\beta) I_{B_1} \cdot 2R_E - V_{EE}$. — (2)

$I_{C_1} = \beta I_{B_1}$ — (3)

Now, if $V_{CE} > 0.2$, transistor is in active region.

AC analysis :– $V_{EE} = V_{CC} = 0$. ; ~~$V_{s_1} + V_{s_2} = V_s$~~

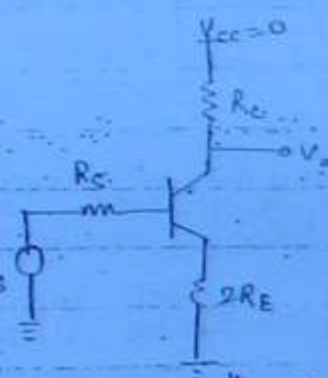
→ A_c → common mode gain.
→ A_d → differential "

Now, for A_c – $V_{s_1} = V_{s_2} = V_s$

$\therefore V_o = A_c V_c + A_d V_d$.

$V_d = V_{s_1} - V_{s_2} = 0 \Rightarrow V_o = A_c V_s$

$V_c = \frac{V_{s_1} + V_{s_2}}{2} = V_s. \Rightarrow A_c = \frac{V_o}{V_s}$.



Common emitter with emitter resistance $2R_E$.

From circuit,

$A_I = -h_{fe}$, $R_i = h_{ie} + (1+h_{fe})(2R_E)$

$$A_{vs} = \frac{V_o}{V_s} = \frac{A_I R_L}{R_s + R_i} \Rightarrow \boxed{A_c = \frac{-h_{fe} \cdot R_c}{h_{ie} + (1+h_{fe}) 2R_E}}$$

Approximate value, $\boxed{A_c = \frac{-R_c}{2R_E}}$ → when $h_{fe} >> 1$.

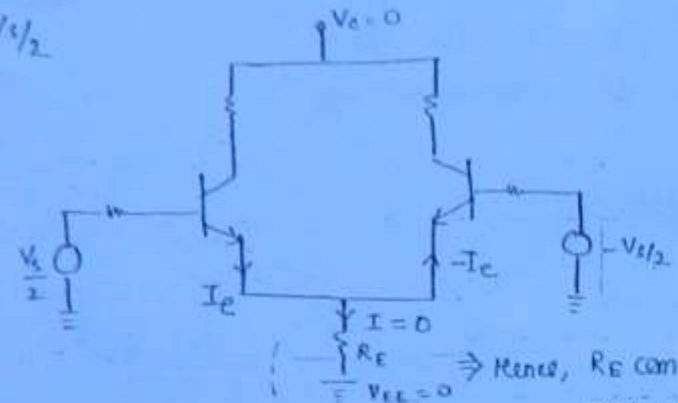
→ Ideally, $A_c = 0$, ⇒ $R_E \to \infty$. (Possible with current mirror ckt).

→ As $R_E \uparrow$, $A_c \downarrow$.

for A_d — $V_{s_2} = -V_s/2$, $V_{s_1} = V_s/2$

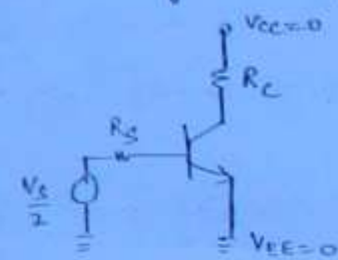
$\therefore V_d = V_s$; $V_c = 0$.

$A_d = \dfrac{V_o}{V_s}$



⇒ Hence, R_E can be removed or s.c.

Now, dividing the ckt ↓



← fig(2)

from fig (2) —

$A_I = -h_{fe}$, $R_i = h_{ie}$

$A_{v_s} = \dfrac{V_o}{(V_s/2)} = \dfrac{-h_{fe} \cdot R_c}{R_s + h_{ie}}$

$\Rightarrow 2 \cdot A_d = \dfrac{-h_{fe} \cdot R_c}{R_s + h_{ie}}$

$$\Rightarrow \boxed{A_d = \frac{-h_{fe} \cdot R_c}{2(R_s + h_{ie})}}$$

→ (It does not depend on R_E)

$\Rightarrow \therefore CMRR = \dfrac{|A_d|}{|A_c|}$ ⇒ $CMRR = \dfrac{R_s + h_{ie} + [1 + h_{fe}] \cdot 2R_E}{2\,[R_s + h_{ie}]}$

if $(1 + h_{fe}) 2R_e >> R_s + h_{ie}$, then

$$\boxed{CMRR = \frac{[1 + h_{fe}] \cdot R_E}{R_s + h_{ie}}} \;**$$

($As\ R_E \to \infty,\ CMRR \to \infty$) (Ideal value).

Effect of increasing R_E :-

* $g_m = \dfrac{|I_c|}{V_T}$ ⇒ as $R_E \uparrow$, $V_{EN} \uparrow$ → feedback ↑ ⇒ $I_B \downarrow$ or $I_c \downarrow$.

1) Negative feedback across R_E ↑es.

2) A_c ↓es, CMRR ↑es, $g_m \downarrow$, gain ↓ { ∵ gain ∝ g_m }

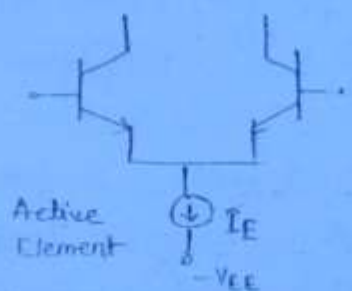
3) $R_i \uparrow$

Application :-

- It is used as the first internal stage in op-amp.
- As an instrumentation amp.
- As a very good clipper
- As a linear amplifier, i.e. we can apply superposition theorem.
- It is used in designing of AVC (Automatic voltage control) or AGC (auto. gain control).
- ~~Any if~~

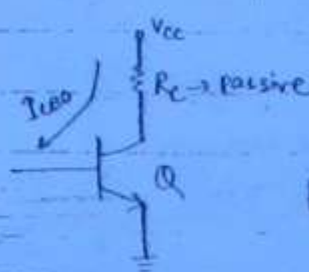
Note

* Any ideal diff. amplifier can be designed by connecting an ideal current source in place of R_E.



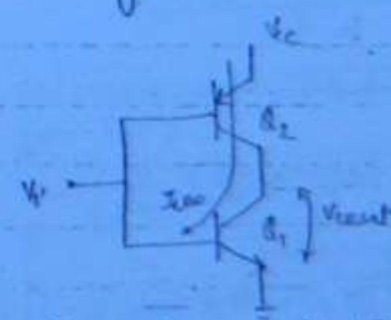
	Ideal source	Practically
source resistance	$= \infty = R_E$	R_E = Very high
A_c	$= 0$	Very low
CMRR	$= \infty$	Very high.

→ In a practical diff. amplifier, active load is connected to get best performance. In place of passive load R_C; pnp transistor is used to get maximum peak to peak o/p voltage or maximum swing.



Ideal swing $= V_{CC}$

Prac. swing $= V_{CC} - \underbrace{I_{CBO}R_C}_{\downarrow \text{ High}} - V_{CEsat}$



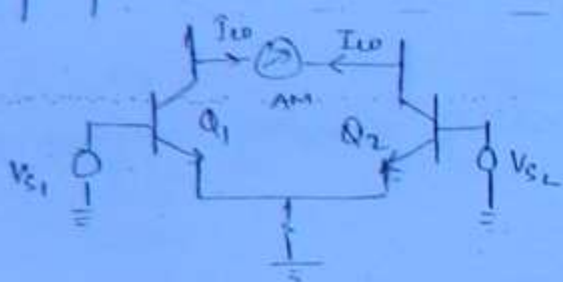
	Q	Ideal V_o	Practical V_o
$V_i >> 0$	saturation	0	V_{CEsat}
$V_i << 0$	cutoff	V_{CC}	$V_{CC} - I_{CBO}R_C$

V_i	Q_1	Q_2	R_{Q_2}	V_o Prac
$V_i >> 0$	on	off	$\cong \infty$	V_{CEsat}
$V_i << 0$	off	on	$\cong 0$	$\cong V_{CC}$

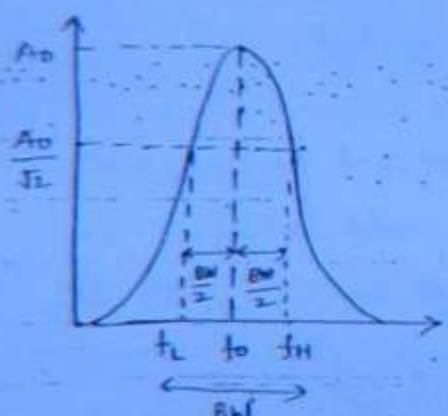
∴ $\boxed{\text{Swing} \uparrow}$ → I_{CBO} is still present but Resistance ≈ 0.

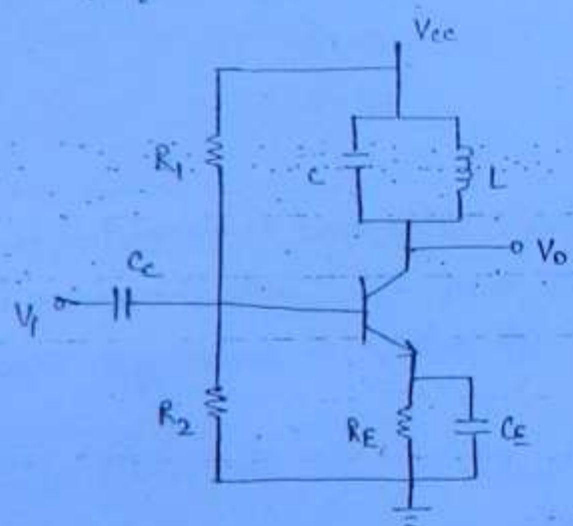
→ Differential amplifier is often used in dc application. It is difficult to design dc amplifier using Tr. because of drift due to variations of h_{fe}, V_{BE} & I_{CBO} with temp.

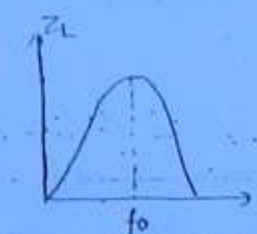
→ With Q_1 and Q_2 having almost identical characteristic, any parameter changes due to temp will cancelled out and o/p will not vary.
for eg., leakage current of Q_1 & Q_2 are equal in magnitude but flowing in opposite direction into ammeter & they get cancelled, and hence drift problem is eliminated in emitter coupled diff. amp.



Tuned Amplifier (class C amplifiers):-







$$A_V = \frac{A_I \cdot Z_L}{R_i}$$

$Z_L \rightarrow$ LC tank circuit.

→ Resonance freq. :- $f_0 = \frac{1}{2\pi\sqrt{LC}}$

→ $BW = f_0/Q$; $Q \rightarrow$ quality factor

→ $\boxed{\text{As } Q\uparrow, BW\downarrow}$ ⇒ $\boxed{\text{selectivity} \propto Q.}$

To change the BW, Q should be changed and not f_0, as changing f_0 will change the centre frequency.

$\rightarrow$ $\boxed{f_H = f_0 + \frac{BW}{2}}$; $\boxed{f_L = f_0 - \frac{BW}{2}}$

→ It is also called tuned voltage amplifier.
→ I/p signal freq. range :- 30KHz to 300KHz. (RF band, hence also called RF amplifier)
→ Working principle is parallel resonance.

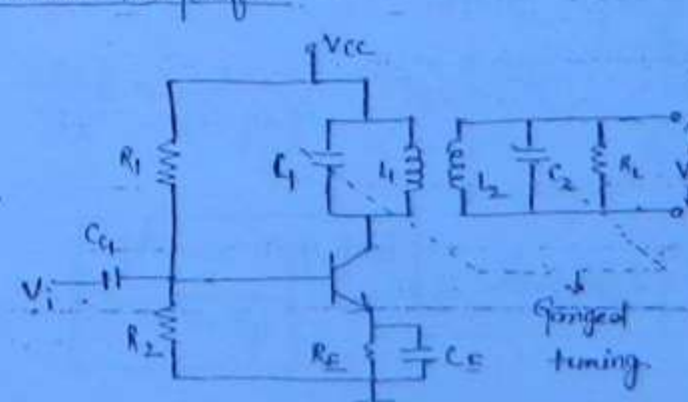
→ Ability of amplifier to reject unwanted frequencies is called selectivity
→ It has ability to select a particular station signal for amplification by rejecting all other unwanted station signals, i.e, selectivity is very high.
→ front end selectivity of receiver is done by RF amplifier, therefore tuned amplifier is first stage in superheterodyne receiver.

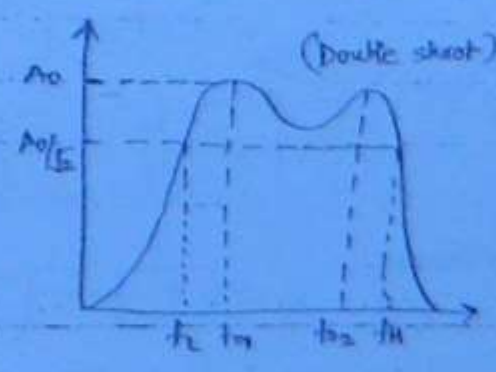
→ Tuned amp is class C amplifier and it is a non-linear amp.
→ for a tank circuit, Q is very large (100-500).
→ BW is very small and this is due to –
 i) Larger Q.
 ii) larger gain (∵ Gain × BW = constant).

→ It is also called Narrow Band amplifier.

Disadvantage: Narrow BW. (with ↑ in quality, BW requirement ↑es but with ↑ed BW, gain ↓es).

Double-Tuned Amplifier





$\rightarrow f_{o1} = \dfrac{1}{2\pi\sqrt{L_1 C_1}}$, $f_{o2} = \dfrac{1}{2\pi\sqrt{L_2 C_2}}$

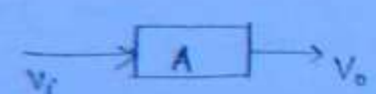
→ In double tuned amplifier, two tank circuits which are tuned to resonant freq. are inductively coupled and placed in collector ckt.

→ BW can be ↑ed w/o reducing gain of amp, hence gain × BW is not a constant

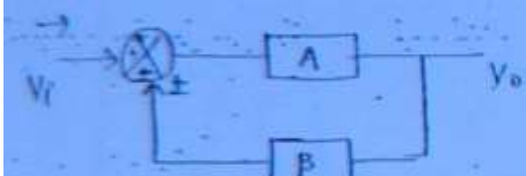
Advantage:-

- A larger BW when compared to a single tuned voltage amp.

FEEDBACK AMPLIFIERS

→ 

$$A_{OL} = \frac{V_o}{V_i} = A$$

→ 

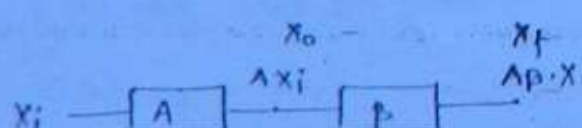
↳ feedback factor

For +ve feedback — (Regenerative feedback) $A_f = \dfrac{A}{1-\beta A}$ $(> A)$

For −ve feedback — (Degenerative FB) $A_f = \dfrac{A}{1+\beta A}$ $(< A)$

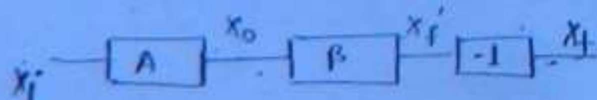
→ Loop Gain (Return Ratio):- { OLTF }* (by me)

→ +ve feedback -



$$\boxed{\text{loop gain} = \frac{x_f}{x_i} = A\beta}$$

→ −ve feedback:-



$$\boxed{\text{loop gain} = -A\beta}$$

Return Difference :- $\boxed{D = 1 - \text{loop gain}}$; [illegible]

195

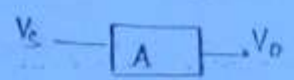
→ for +ve feedback – $D = 1 - A\beta$

→ for –ve feedback – $D = 1 + A\beta$.

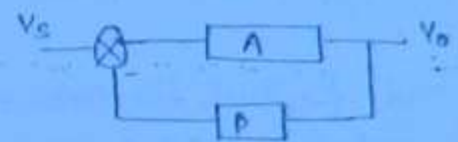
Advantage of Negative feedback :-

→ Stability of transfer gain increases.

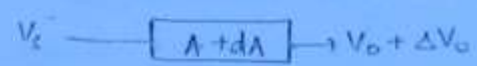
(a) Desensitivity of transfer gain



$V_o = AV_s$



$V_o = \frac{A}{1+\beta A} \cdot V_s \Rightarrow A_f = \frac{A}{1+\beta A}$



$\Delta V_o = dA \cdot V_s$.

$\frac{dA}{A}$ = fractional variation in A w/o feedback.

$\frac{dA_f}{A_f}$ = fractional variation with feedback.

→ if $\boxed{\frac{dA_f}{A_f} < \frac{dA}{A}}$, then gain after feedback is stable.

Sensitivity :- $S = \frac{dA_f/A_f}{dA/A}$

→ For stability ; $\boxed{S < 1}$

→ Desensitivity , $\boxed{D = 1/S}$; $\boxed{D > 1}$ for stability after feedback.

Now, $\frac{dA_f}{dA} = \frac{1}{(1+\beta A)^2} \Rightarrow \boxed{\frac{dA_f}{A_f} = \frac{dA/A}{(1+A\beta)}}$

→ $\boxed{S = \frac{1}{1+A\beta}}$; $\boxed{D = 1 + A\beta}$

(b) If feedback n/w contains only stable passive elements then there is improvement in stability

$$A_f = \frac{A}{1+A\beta} = 1/\beta \text{ if } A\beta >> 1.$$

Hence, β should consist of stable passive elements.

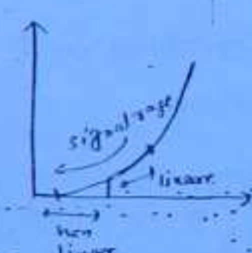
Reduction in Frequency Distortion :-

Frequency Distortion :- Variation in magnitude of gain with frequency.
Phase Distortion :- Variation in phase of gain with freq.

→ If $A_f = 1/\beta$ and feedback n/w does not contain reactive element, then overall gain is not a func^n of freq., and there is reduction in frequency & phase distortion.

Reduction in non-linear distortion :-

$$\cos\omega t \longrightarrow \boxed{BJT} \longrightarrow V_o$$



$$y_o = \underbrace{B_0}_{dc} + \underbrace{B_1 \cos\omega t}_{\text{desired (fundamental component)}} + \underbrace{B_2 \cos 2\omega t + B_3 \cos 3\omega t + \dots}_{\text{undesired}}$$

→ $\omega \uparrow$, Amplitude $\downarrow$, $B_1 >> B_2 >> B_3 \dots$

→ D_2 = 2nd Harmonic Distortion $= \frac{|B_2|}{|B_1|}$

D_3 = 3rd —— " —— $= \frac{|B_3|}{|B_1|}$

D_4 = 4th —— " —— $= \frac{|B_4|}{|B_1|}$.

→ After -ve feedback—

$$\boxed{D_{2f} = \frac{D_2}{1+A\beta}}^{**}$$

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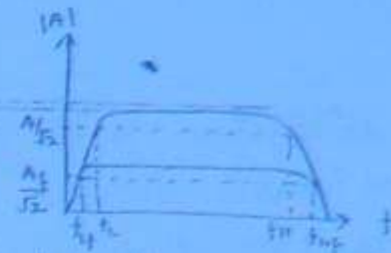
Note:- Guys Be Cool Dude I am here for help You ☺

→ Bandwidth Increases – $\boxed{BW_f = BW\,[1 + A\beta]}$



→ Since G×BW constant & gain ↓ by $(1+A\beta)$ after feedback.

→ Reduction in Noise :- $N_{of} = \dfrac{N_o}{1 + A\beta}$

197

other advantages –

→ It modifies i/p & o/p resistance.

→ It ↑es thermal stability & freq. stability of o/p signal.

Disadvantage :-

– It reduces gain

Application :-

– -ve feedback is widely used in designing of amp. ckt and control system.

Positive feedback :-

→ Advantage :- ↑es gain of amp.

→ Disadvantage :-

→ Reduces BW, hence reproduction of i/p signal is very bad.

– It ↑ noise & harmonic distortion at the o/p.

– It reduces stability of amp.

Application

– In designing of oscillator circuits.

Ques An amplifier w/o feedback gives a fundamental o/p of 36V with 7% 2nd harmonic distortion when i/p is 0.028 V.

198

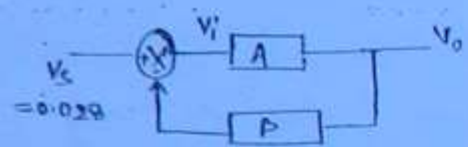
a) If 1.2% of o/p is feedback into i/p in a -ve voltage series feedback ckt, what is o/p voltage.

b) If fundamental o/p is maintained at 36V, but the 2nd harmonic distortion is reduced to 1%, what is i/p voltage.

Sol $v_i = V_s = 0.028$ —[A]— $36 + D_2$ ($= 7\%$)

$$\therefore A = \frac{36}{0.028} = 1285$$

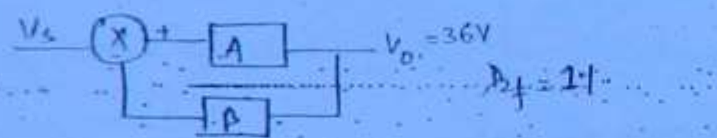
a) $\beta = 1.2\% = 0.012$



$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + A\beta}$$

$$A_f = \frac{1285}{1 + 1285 \times 0.012} = 78.2 \quad , \quad \therefore V_o = 78.2 \times 0.028 = 2.19 \text{ Volt}$$

b)



$$D_{2f} = \frac{D_2}{1 + A\beta}$$

$$\Rightarrow 1 = \frac{7}{1 + A\beta} \Rightarrow 1 + A\beta = 7$$

$$\therefore A_f = \frac{A}{1 + A\beta} = \frac{A}{7} \quad \because \quad \frac{V_o}{V_{s_1}} = A \quad , \quad \frac{V_o}{V_{s_2}} = A_f$$

$$\Rightarrow \frac{V_{s_2}}{V_{s_1}} = \frac{A}{A_f} \Rightarrow V_{s_2} = 7 \times 0.028 = 0.196\text{V Ans}$$

→ Feedback is often expressed in dB.

$$\boxed{N_{dB} = 20 \log \left| \frac{A_f}{A} \right|}$$

- For +ve feedback, $\boxed{N_{dB} = 20\log\left(\frac{1}{1-A\beta}\right)}$ $\Rightarrow$ $N_{dB} > 0$ or +ve.
- For -ve feedback, $\boxed{N_{dB} = 20\log\left(\frac{1}{1+A\beta}\right)}$ $\Rightarrow$ $N_{dB} < 0$ or -ve.

Ques: An amp. with open loop voltage gain of 1000 delivers 10W of o/p power at 10% 2nd harmonic distortion, when i/p is 10 mV. If 40 dB -ve voltage series feedback is applied and o/p power is to remain at 10W, determine
(a) Required i/p signal.
(b) % harmonic distortion.

Soln $-40 = 20\log\left(\frac{1}{1+A\beta}\right) \Rightarrow 1+A\beta = 100$

$\Rightarrow \beta = \frac{99}{1000}$

$\rightarrow A_f = \frac{A}{1+A\beta} \Rightarrow A_f = 10$

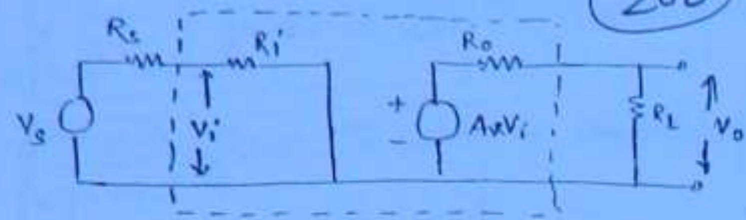
$\rightarrow D_{2f} = \frac{D_2}{1+A\beta} = \frac{10}{100} = 0.1\%$

$\rightarrow V_i' = \frac{1000}{10} V_i = 100 \times 10\,mV = 1V$

Classification of Amplifiers:-

1) Voltage Amplifiers
2) Current "
3) Transconductance.
4) Trans resistance.

Voltage Amplifiers :-



→ $R_i >> R_s$, $R_i = \infty$ (ideally)

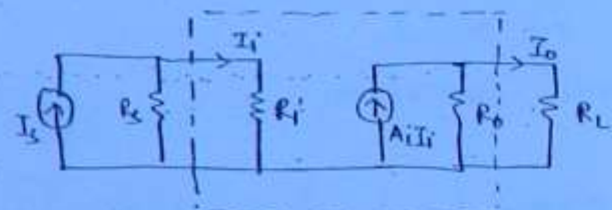
→ $R_o << R_L$, $R_o = 0$ (ideally).

→ A_v → internal gain , A_V → external gain.

→ $V_o = \frac{A_v V_i \cdot R_L}{R_o + R_L}$ ⇒ $\boxed{A_V = \frac{A_v \cdot R_L}{R_o + R_L}}$; $\boxed{A_v = \lim_{R_L \to \infty} A_V}$

When $R_L = \infty$, external gain = internal gai

Current Amplifier :-



→ $R_i << R_s$, i.e, $R_i = 0$ (ideally)
so that whole current passes through R_i

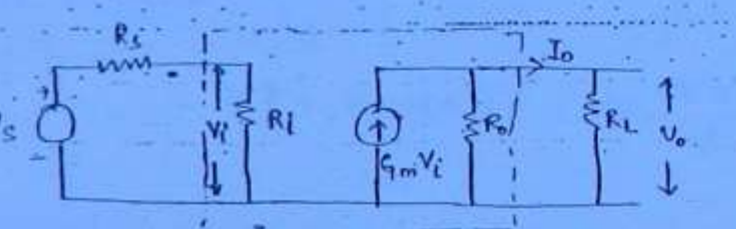
→ $R_o >> R_L$, i.e, $R_o = \infty$ (ideally)
so that max current is delivered to load.

→ A_I = ext. gain , A_i = internal gain .

$\boxed{A_I = \frac{I_o}{I_i} = \frac{A_i R_o}{R_o + R_L}}$

$\boxed{A_i = \lim_{R_L \to 0} A_I}$

Transconductance :-

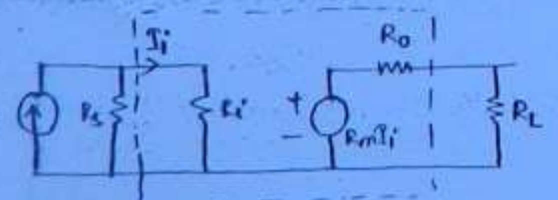


→ $R_i >> R_s$; ideally $R_i = \infty$

→ $R_o >> R_L$, " $R_o = \infty$.

→ $I_o = \frac{G_m V_i \cdot R_o}{R_o + R_L}$ ⇒ $\boxed{G_M = \frac{G_m R_o}{R_o + R_L}}$ $\boxed{G_m = \lim_{R_L \to 0} G_M}$

Transresistance :-

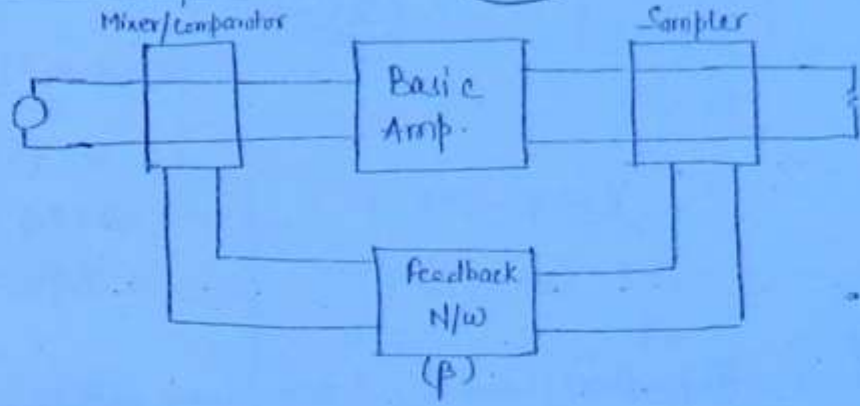


→ $R_s << R_i$, ideally $R_s = 0$

→ $R_o << R_L$, " $R_o = 0$

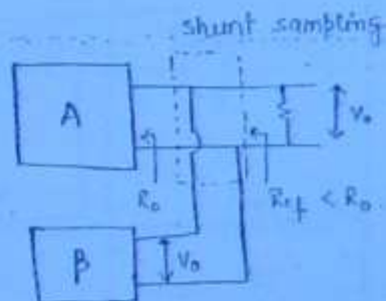
→ $V_o = \frac{R_m I_i R_L}{R_o + R_L}$ ⇒ $\boxed{R_M = \frac{R_m R_L}{R_o + R_L}}$, $\boxed{R_m = \lim_{R_L \to \infty} R_M}$

Feedback Concept :-



Sampler :-

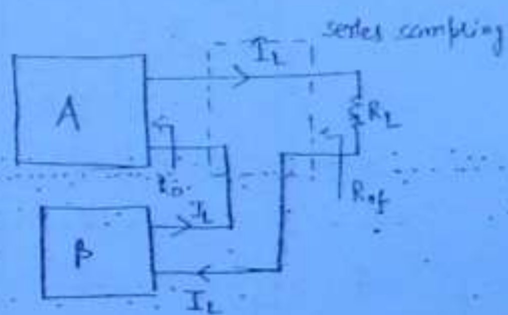
a) Voltage Sampler :-



→ sampled voltage in feedback is same as o/p voltage.

→ $R_{of} < R_o$

(b) Current Sampler :-

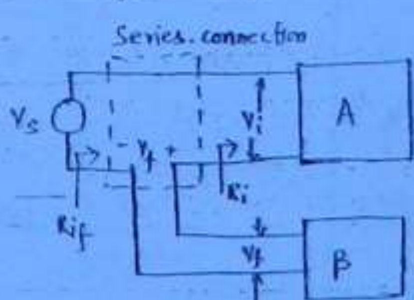


→ $R_{of} > R_o$.

→ sampled current in feedback is same as o/p current.

Mixer :-

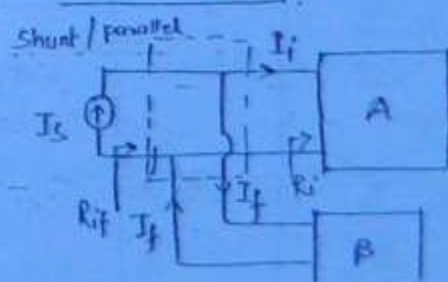
(a) Voltage Mixer



→ $R_{if} > R_i$; Before mixing $V_i = V_s$

After " $V_i = V_s - V_f$

(b) Current Mixer



$R_{if} < R_i$, Before mixing → $I_i = I_s$

After → $I_i = I_s - I_f$

voltage / current — sampler   mixer: series → voltage i/p; shunt → ~~with~~ current i/p

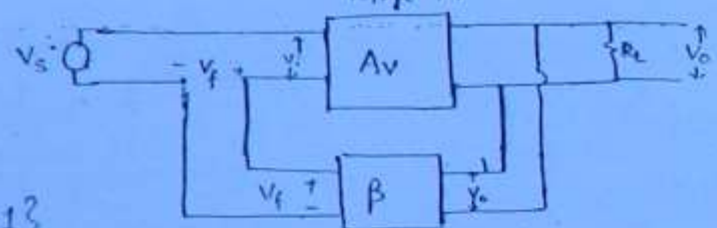
Feedback Topology :-

(202)

1) Voltage Series feedback.
2) Current Series "
3) Voltage Shunt "
4) Current Shunt "

Derivation of R_{if} (input resistance with feedback) and R_{of} (o/p resistance with FB) for Voltage Series feedback :-

Voltage Amp



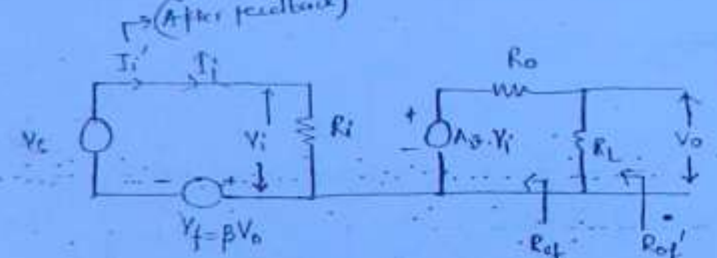
$\rightarrow V_f = \beta V_o$

$\Rightarrow \beta = \frac{V_f}{V_o}$ = unitless.

$A_{vf} = \frac{A_v}{1+\beta A_v} = \frac{1}{\beta}$ $\{\beta A_v \gg 1\}$

$\rightarrow R_{of} < R_o$ & $R_{if} > R_i$

(After feedback)



Calculation of R_{if} —

Before feedback :-

$V_i = V_s$.

i/p resistance $= \frac{V_s}{I_i} = \frac{V_i}{I_i} = R_i$

After feedback :-

$V_s = V_i + V_f \Rightarrow V_i = V_s - V_f$.

(There is -ve feedback).

i/p resistance : $R_{if} = \frac{V_s}{I_i'}$

Applying KVL —

$V_s = I_i' R_i + V_f$

$V_s = I_i' R_i + \beta V_o$

but $V_o = \frac{A_v \cdot V_i' R_L}{R_o + R_L} = A_v \cdot V_i'$

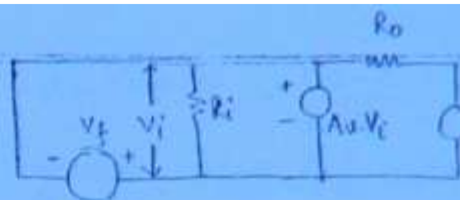
$\therefore V_s = I_i' \cdot R_i + \beta \cdot A_v \cdot V_i'$

$\Rightarrow V_s = I_i' R_i + \beta A_v R_i I_i'$

$\Rightarrow \frac{V_s}{I_i'} = R_{if} = R_i + \beta A_v R_i$

$\Rightarrow \boxed{R_{if} = R_i (1+\beta A_v)} \Rightarrow \boxed{R_{if} > R_i}$

Calculation for R_{of}: (203)



$\beta V_o = \beta V$

$\rightarrow V = IR_o + A_{ve} \cdot V_i$

$\rightarrow V_i + V_f = 0$

$\Rightarrow V_i + \beta V = 0$

$\Rightarrow V_i = -\beta V$

$\therefore V = IR_o - \beta A_{ve} . V$

$\Rightarrow V(1+\beta A_{ve}) = IR_o$

$\Rightarrow R_{of} = \frac{V}{I} = \frac{R_o}{1+\beta A_v}$ $\{R_{of} < R_o\}$.

$R_{of}' = R_{of} \| R_L$

	Voltage Series	Current Series	Voltage Shunt	Current Shunt
Output	V	I	V	I
Input	V	V	I	I
Basic Amplifier	Voltage Amp. $A_v = V_o/V_i$	Transconductance $G_m = I/V$	Transresistance $R_m = V/I$	Current Amp $A_I = I_o/I_i$
Stablised Gain	$A_{vf} = \frac{V_o}{V_s} = 1/\beta$	$G_{mf} = \frac{I_o}{V_s} = 1/\beta$	$R_{mf} = \frac{V_o}{I_s} = \frac{1}{\beta}$	$A_{If} = \frac{I_o}{I_s} = \frac{1}{\beta}$
Unit of β	Unit less	ohm	mho	unit less
Another name (i/p - o/p)	Series - Shunt	series - series	Shunt - shunt	Shunt - series
Effect on R_i	↑es	↑es	↓es	↓es
" " R_o	↓es	↑es	↓es	↑es

Voltage Series	Current Series	Voltage Shunt	Current Shunt
$\rightarrow$ V_i — [A_v] — V_o; R_i↑ R_o↓	V — [G_m] — I; R_i↑ R_o↑	I — [R_m] — V; R_i↓ R_o↓	I — [A_I] — I_o; R_i↓ R_o↑
$\rightarrow R_{if} = (1+A_v\beta)R_i$	$\rightarrow R_{if} = (1+\beta G_m) \cdot R_i$	$\rightarrow R_{if} = \frac{R_i}{1+\beta R_m}$	$\rightarrow R_{if} = \frac{R_i}{1+\beta A_I}$
$\rightarrow R_{of} = \frac{R_o}{1+\beta A_v}$	$\rightarrow R_{of} = (1+\beta G_m)R_o$	$\rightarrow R_{of} = \frac{R_o}{1+\beta R_m}$	$\rightarrow R_{of} = R_o(1+\beta A_I)$
$\rightarrow$ Normally, $A_v = A_{ve}$ (i.e., $R_L \approx \infty$)	$\rightarrow G_M \simeq G_m$	$\rightarrow R_M \simeq R_m$	$\rightarrow A_f \approx A_i$

$\rightarrow R_{of}' = R_{of} \| R_L$

Workbook

Pg 33 : Q.16. (Ch.2)

$$I_B = \frac{5-0.7}{10^3 k\Omega} = 4.3\times10^{-3}\,mA.$$

204

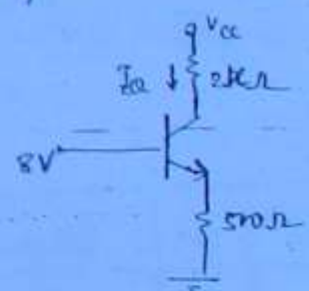
$$I_c = \beta I_B = 100\times4.3\times10^{-3} = 0.43mA$$

$$\frac{V_o-12}{2K} + \frac{V_o}{4} + I_c = 0 \Rightarrow \frac{V_o}{2}+\frac{V_o}{4} - 6 + 0.43 = 0$$

$$\Rightarrow V_0 = 7.43V$$

Q.17 Since, the circuit is amplifier, then $V_{CE} > 0.2$.

$\rightarrow V_c - V_E > 0.2V$



$V_E = 8-0.7 = 7.3V$

$V_c = V_{cc} - I_{cQ}\cdot 2k$

$\Rightarrow V_{cc} - 6 - 7.3 > 0.2V$

$\Rightarrow V_{cc} > 13.5V$

For pnp, $V_{cc} < -13.5V$

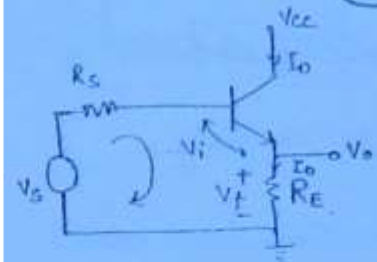
10th Sep, 2012

Voltage Series Feedback :-

Best practical examples are-
- emitter follower (CC configuration)
- source follower (CDrain ")
- voltage follower (Non-inverting op-amp)

→ Basic Assumptions :-
- The basic amplifier is unilateral from i/p to o/p, i.e. it does not allow signal from o/p to i/p.
- Feedback n/w is unilateral, from o/p to i/p., i.e., it does not allow signal from i/p to o/p
- β is independent of source resistance R_s & load resistance R_L.

Emitter Follower :-



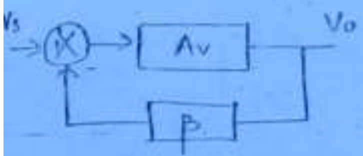
Let R_s is very small, hence drop across R_s can be neglected.

Without fb :- (or w/o R_E) $\Rightarrow$ $V_i = V_s$.

With fb :- $V_i = V_s - V_f$

Since $V_i \downarrow$ with feedback, hence -ve feedback.

& series comparison (∵ voltage is changing).



→ Also, $V_o = V_f$

$\Rightarrow \beta = 1$ $\{ \because V_f = \beta V_o \}$.

& there is voltage sampling.

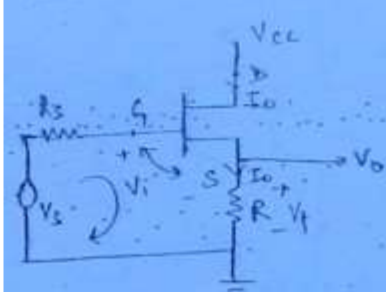
→ $A_{vf} = \frac{V_o}{V_s} = 1/\beta = 1$; $\phi = 0$

→ If we assume current sampling, then

$V_f = \beta I_o \Rightarrow \beta = \frac{V_f}{I_o} = \frac{I_o R_E}{I_o} = R_E$.

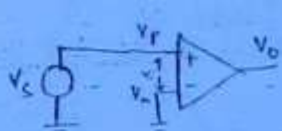
but β depends on R_E, hence not a current sampling.

Source Follower:



- Results will be similar to Emitter follower.
- For both circuits :-
  - There is max. -ve feedback
  - Gain is highly stable (∵ β is independent)

Voltage follower :



w/o feedback

$V_i = V_s - V_o = V_s$

$V_o = A_v \cdot V_i$

with fB $V_i = V_s - V_f \Rightarrow V_i \downarrow$, -ve feedback & series mixer.

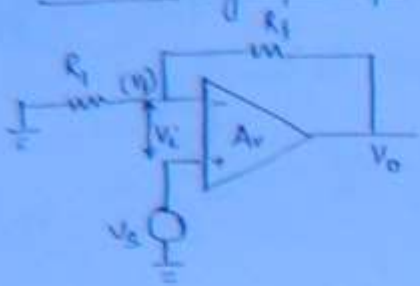
$V_f = V_o$. $\Rightarrow \beta = 1$ & there is voltage sampling.

$A_{vf} = \frac{V_o}{V_s} = 1/\beta = 1$; $R_{if} = (1 + A\beta) \cdot R_i = (1 + 10^4 \cdot 1) \cdot 10^6 = 10^4 M\Omega$

$R_{of} = \frac{R_o}{1 + A\beta} = \frac{100}{10^4} \simeq 0.01 \Omega = 0\Omega$

$BW_f = (1 + A\beta) \cdot BW = 10^4 (BW)$

Non-Inverting op-Amp



$V_i = V_s - V_f \Rightarrow$ -ve feedback, voltage mixing comparison (series)

$V_f = \frac{R_1}{R_1+R_f} \cdot V_o \Rightarrow V_f = \beta V_o \Rightarrow$ voltage sampling.

β is constant ($\because R_1, R_f$ are neither source resistance, nor load resistance).

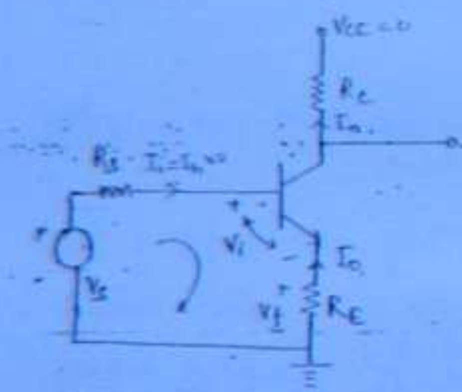
$\rightarrow A_{vf} = 1/\beta = \left(1 + \frac{R_f}{R_1}\right) \rightarrow$ (approximate)

$\rightarrow A_{vf} = \frac{A_v}{1+\beta \cdot A_v} \rightarrow$ (exact).

$\rightarrow \boxed{R_{if} = (1+\beta A_v) \cdot R_i}$; $\boxed{R_{of} = \frac{R_o}{1+\beta A_v}}$; $\boxed{BW_f = (1+\beta A_v) BW}$

Current Series feedback :-

(1) CE with unbypassed R_E :-



let drop across $R_s \simeq 0$

w/o R_E :- $V_i = V_s$

with R_E :- $V_i = V_s - V_f$

$\therefore$ There is series comparison

Now, let there is voltage sampling,

$V_f = \beta V_o \quad \therefore \beta = \frac{V_f}{V_o} \Rightarrow \beta = -\frac{I_o R_E}{I_o R_C} \Rightarrow \beta = -\frac{R_E}{R_C}$.

$\rightarrow A_{vf} = \frac{V_o}{V_s} = 1/\beta = -\frac{R_C}{R_E}$.

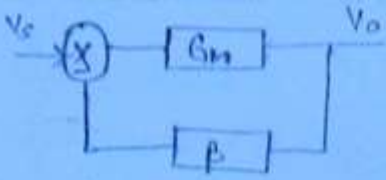
But, $\because \beta$ is dependent on load $R_L = R_C$, hence our assumptions are wrong.

Hence, there is current sampling.

$\therefore V_f = \beta I_o \Rightarrow \beta = \frac{I_o}{V_f} = \frac{I_o}{-I_o R_E} \Rightarrow \beta = -1/R_E$.

$\Rightarrow \beta = \frac{V_f}{I_o} \Rightarrow \boxed{\beta = -R_E}$ (Transconductance)

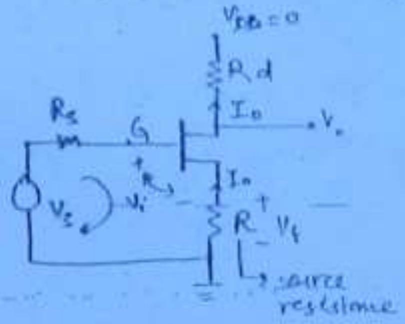
Hence β is independent of R_C



$$\boxed{G_{mf} = \frac{I_o}{V_s} = \frac{1}{\beta} = -\frac{1}{R_E}}$$

$$\therefore A_{vf} = \frac{V_o}{V_s} = \frac{I_o R_c}{V_s} \Rightarrow \boxed{A_{vf} = -\frac{R_c}{R_E}}$$

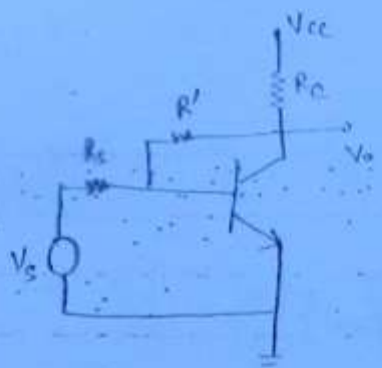
Common source with unbypassed source resistance :-



$$\boxed{\begin{aligned} \beta &= -R \\ G_{Mf} &= -\frac{1}{R} \\ A_{vf} &= -\frac{R_d}{R} \end{aligned}}$$

Voltage Shunt Feedback :-

(a) ~~CB~~ Collector Bias circuit :-



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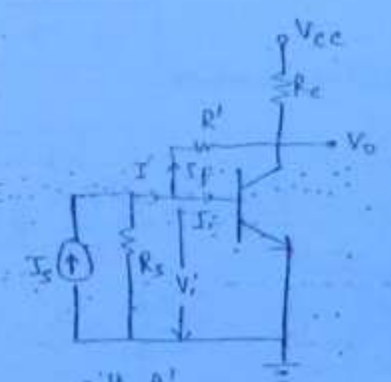
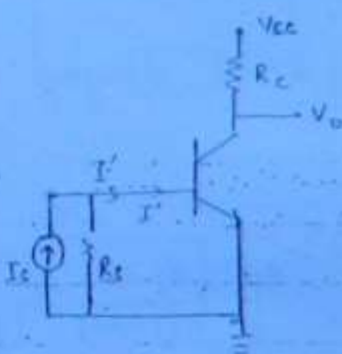


with R'



w/o R'

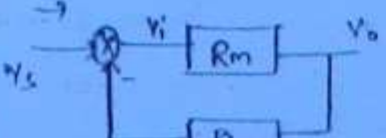
→ w/o feedback, $I_i = I'$

→ with fb — $I_i = I' - I_f \rightarrow I_i \downarrow$, hence shunt ~~voltage~~ comparison

→ for A CE configuration, $|A_v| \gg 1 \Rightarrow V_o \gg V_i$

→ $I_f = \frac{V_i - V_o}{R'} \Rightarrow I_f = -\frac{V_o}{R'} \Rightarrow \boxed{\beta = -\frac{1}{R'}}$

→

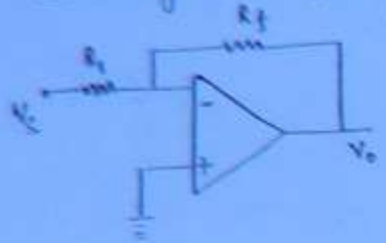


$$R_{Mf} = \frac{V_o}{I_s} \Rightarrow \boxed{R_{Mf} = -R'}$$

$$A_{vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s R_s} \Rightarrow \boxed{A_{vf} = -\frac{R'}{R_s}}$$

**** V. V. Imp

Inverting Op-amp :-



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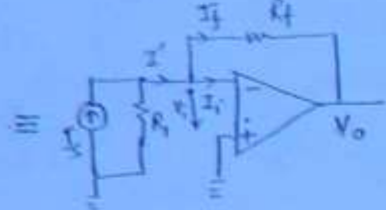
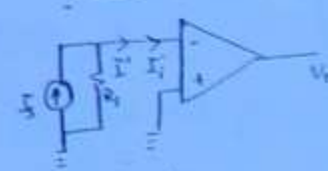


with feedback



w/o feedback

w/o feedback :- $I_i = I'$

with feedback: $I_i = I' - I_f$ ⇒ shunt mixing comparison

Now, $V_i = V_n - V_p$; $V_o = A_v \cdot V_i$; $A_v < 0$

∵ $|A_v| >> 1$ ⇒ $V_o >> V_i$

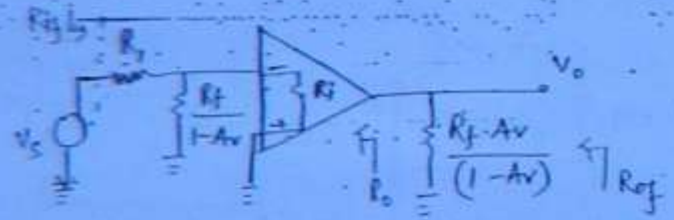
→ $I_f = \frac{V_i - V_o}{R_f}$ ⇒ $I_f = -\frac{V_o}{R_f}$ ⇒ $\boxed{\beta = -1/R_f}$ ** —(Imp)

→ $R_{mf} = 1/\beta = -\frac{1}{1/R_f}$ → $A_{vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s R_s}$ ⇒ $\boxed{A_{vf} = -\frac{R_f}{R_1}}$ **

⇒ $R_{mf} = -R_f = \frac{V_o}{I_s}$

→ To calculate R_{if} & R_{of}, applying Miller's theorem —

Fig 5:



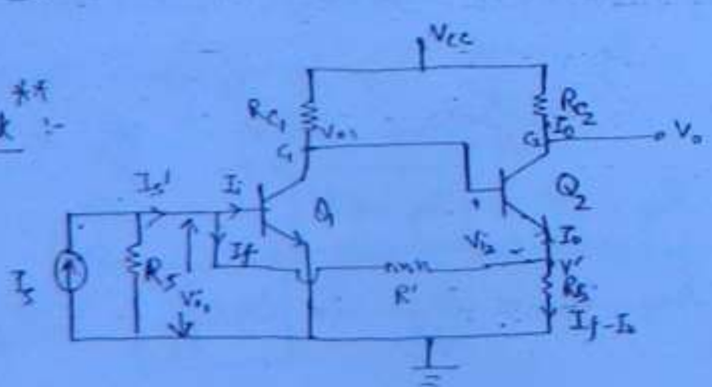
$R_{if} = R_1 + \left(\frac{R_f}{1-A_v} \| R_i\right)$

∵ $\frac{R_f}{1-A_v} \approx 0$ {∵ $|A_v| >> 1$}

⇒ $R_{if} = R_1$ hence Reduced i/p resistance

⇒ $R_{of} = R_o \| \left(\frac{R_f A_v}{1-A_v}\right) \approx R_o \| R_f$, Hence, o/p resistance also ↓es.

Current Shunt Feedback ** :-



w/o feedback → $I_i = I_s'$

with feedback → $I_i' = I_s' - I_f$ ⇒ shunt ~~mixing~~ comparison

Now, $A_{v_1} = \frac{V_{o1}}{V_i} >> 1 \Rightarrow V_{o1} >> V_i$ $\{\because$ CE configuration$\}$.

Now, $V' = V_{o1} - V_{i_2} \approx V_{o1}$ $\{\because V_{i_2} << V_{o1}$, V_{i_2} = small signal$\}$.

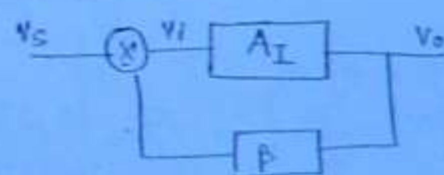
$\Rightarrow V' = V_{o1} >> V_i$

→ $I_f = \frac{V_i - V'}{R'} \Rightarrow I_f = -\frac{V'}{R'}$, but $V' = (I_f - I_o)R_E$.

$\Rightarrow I_f = -\frac{(I_f - I_o)R_E}{R'}$

$\Rightarrow \boxed{I_f = \frac{R_E}{R' + R_E} I_o}$ → ∵ I_f depends on I_o, hence current sampling.

$\Rightarrow I_f = \beta I_o \Rightarrow \boxed{\beta = \frac{R_E}{R' + R_E}}$



→ $\boxed{A_{If} = \frac{V_o}{V_s} = 1/\beta = 1 + \frac{R'}{R_E}}$

→ $A_{vf} = \frac{V_o}{V_f} = \frac{I_o \cdot R_{C_2}}{I_s R_s} \Rightarrow \boxed{A_{vf} = \frac{1}{\beta} \cdot \frac{R_{C_2}}{R_s}}$

FET

→ $i_d = f(V_{gs}, V_{ds})$

→ $\boxed{i_d = g_m V_{gs} + \frac{V_{ds}}{r_d}}$ —— ①

Change in i_d due to V_{gs} & V_{ds} —

$$di_d = g_m \, dV_{gs} + \frac{dV_{ds}}{r_d}$$

When $V_{ds} = \text{constant}$; $\boxed{g_m = \left.\frac{di_d}{dV_{gs}}\right|_{V_{ds}=\text{constant}} =}$ Transconductance.

When $V_{gs} = \text{constant}$; $\boxed{r_d = \left.\frac{dV_{ds}}{di_d}\right|_{V_{gs}=\text{constant}}}$ = drain resistance

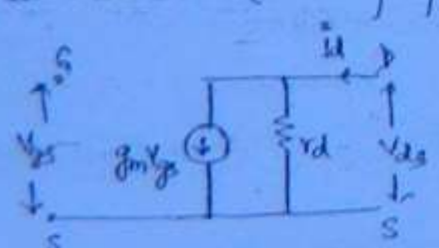
→ μ = amplification factor ⇒ $\boxed{\mu = g_m \times r_d}$

→ $g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$; $g_{mo} = \frac{2I_{DSS}}{|V_P|} = g_m\Big|_{V_{gs}=0}$.

→ $I_{DS} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$; $I_{DSS} = I_{DS}\Big|_{V_{GS}=0}$; I_{DS} = saturation drain current

→ $g_{m} = \frac{2}{|V_P|}\sqrt{I_D \cdot I_{DSS}}$

Small signal Model :— (at low frequency)



Workbook :-

(211)

Chap-7 :-

Q.1 b (All wrong answers)

Q.2 (a)

Q.3 (d)

Q.8 (b)

Q.12 :-

$G_{mf} = \frac{I_o}{V_s} = -1\ mA/V$

$A_{vf} = -4$

$D = 1 + \beta . G_m = 50$

$\beta = -R_E$

Q.4 (c)

Q.5 (b)

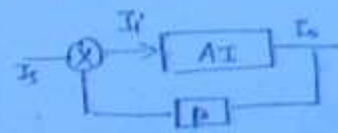
Q.6 (a)

Q.7 (b)

Q.9 (a)

Q.10 (c)

Sol^n (5) $A_v = 50$; $\beta = 0.2$



$R_{if} = \frac{R_i}{1 + A_I \beta}$

$A_v = \frac{V_o}{V_i} = \frac{I_o R_o}{I_i R_i} = \frac{A_i R_o}{R_i}$

$\Rightarrow A_i = \frac{50 \times 1}{2.5} = 20$

$\therefore R_{if} = 1/5\ \Omega$

$G_{mf} \approx 1/\beta \approx -1/R_E$

$\Rightarrow -1 \approx -1/R_E$

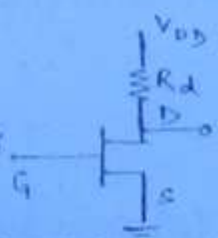
$\Rightarrow R_E \approx 1k\Omega$

Exact $G_{mf} = \frac{G_m}{1 + \beta G_m} \Rightarrow -1 = \frac{G_m}{50} \Rightarrow G_m = -$

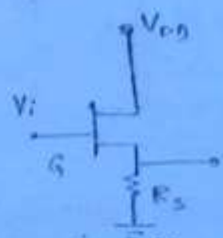
$1 + \beta(-50) = 50 \Rightarrow \beta = -\frac{49}{50} = -R_E$

$\Rightarrow R_E = 0.98\ K\Omega$

*



Common Source



Common Drain

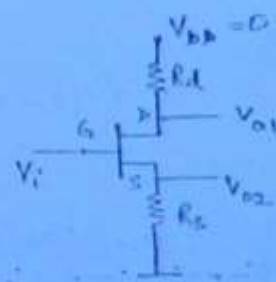
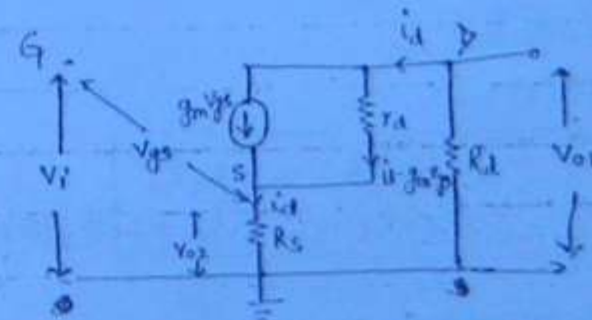


Fig.1

$V_o = V_{o1}$ = CS with source resistance R_s

$V_o = V_{o2}$ = CD with drain resistance R_d.

* Small Signal Analysis :-



(From fig. 1)

KVL at i/p :-

$V_{o1} = -i_d . R_d$ — (1)

$V_{o2} = i_d R_s$ — (2)

$V_{gs} = V_i - i_d R_s$ — (3)

KVL at o/p .

$-i_d R_d - r_d(i_d - g_m V_{gs}) - i_d R_s = 0$

$\Rightarrow i_d(R_d + r_d + R_s) - g_m r_d V_{gs} = 0$

$\because \mu = g_m \times r_d$ & eq^n (3) —

$i_d(R_d + r_d + R_s) - \mu(V_i - i_d R_s) = 0$

$\Rightarrow \; i_d = \dfrac{\mu \cdot V_i}{R_d + r_d + (1+\mu)R_s}$ — (4)

for CS with source resistance R_s —

$V_{o1} = -i_d \cdot R_d$.

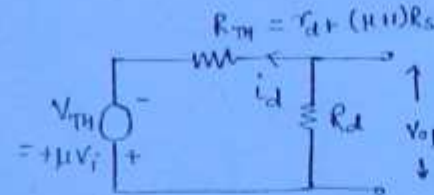
$\Rightarrow V_{o1} = \dfrac{-\mu \cdot V_i R_d}{R_d + r_d + (1+\mu)R_s}$ — (5) $\Rightarrow \boxed{A_V = \dfrac{-\mu \cdot R_d}{R_d + r_d + (1+\mu)R_s}}$; $\boxed{\phi = 180^\circ}$ — (6)

→ if $(\mu+1)R_s >> (R_d + r_d)$ —

$\boxed{AV = -\dfrac{R_d}{R_s}}$ — (7) → Independent of any parameter for FET, hence gain is highly stable.

Thevenin's equivalent :-

$V_{o1} = \dfrac{R_d}{R_d + R_{TH}} \cdot V_{TH}$ — (8)



from (5) & (8) :-

$\boxed{R_{Th} = R_o = r_d + (\mu+1)R_s}$
$\boxed{V_{Th} = -\mu V_i}$ — (9)

→ o/p resistance increases due to current series feedback. (Effect on i/p resistance is neglected as it is already ∞)

for Common source (w/o R_s) :-

Put $R_s = 0$ in eq^n (6) —

$\boxed{A_V = -\dfrac{g_m r_d \cdot R_d}{R_d + r_d} = -g_m R_d'}$; $\boxed{R_d' = R_d \| r_d}$

From eq^n(9) —

$\boxed{R_o = r_d = R_{TH}}$

Note * if r_d is not given, then take it ∞.

For Common Drain with drain resistance R_d :-

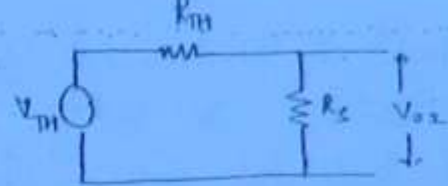
$$V_{o2} = i_d \cdot R_s$$

$$\therefore V_{o2} = \frac{\mu V_i R_s}{R_d + r_d + (\mu+1) R_s} \quad \text{—— (12)}$$

$$\Rightarrow A_V = \frac{V_{o2}}{V_i} \Rightarrow \boxed{A_V = \frac{\mu \cdot R_s}{R_d + r_d + (\mu+1) R_s}} \text{ — (13)}, \quad \boxed{\begin{array}{l}\phi \text{ shift} = 0^\circ \\ |A_V| < 1\end{array}}$$

Thevenin's Equivalent :-

$$\frac{V_{TH} \times R_s}{R_s + R_{TH}} = V_{o2} \quad \text{—(14)}.$$



Dividing numerator & denominator by $(\mu+1)$ in eq^n (12) —

$$V_{o2} = \frac{\left(\frac{\mu}{\mu+1}\right) V_i \cdot R_s}{\frac{R_d + r_d}{(\mu+1)} + R_s} \quad \text{— (15)}$$

Comparing (14) & (15) ——

$$\boxed{V_{TH} = \left(\frac{\mu}{\mu+1}\right) \cdot V_i} \; ; \; \boxed{R_{TH} = \frac{R_d + r_d}{\mu+1} = R_o} \text{ — (16)}.$$

For common drain (w/o R_d) :-

Putting $R_d = 0$ in eq^n. (13) —

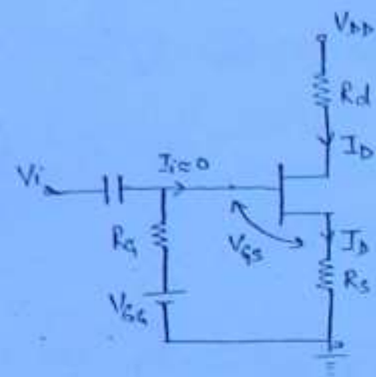
$$A_V = \frac{\mu R_s}{r_d + (\mu+1) R_s} \; ; \text{ if } (\mu+1) R_s \gg r_d \;\&\; \mu \gg 1,$$

$$\Rightarrow \boxed{A_V \simeq 1} \rightarrow \text{Circuit is called source follower.}$$

from eq^n (16) —

$$\rightarrow R_o = \frac{r_d}{\mu+1} \approx \frac{r_d}{\mu} \approx \frac{r_d}{g_m r_d} \Rightarrow \boxed{R_o = 1/g_m} \text{ Imp}$$

Source Self Biasing :-



DC analysis

$V_{GG} = I_i R_G + V_{GS} + I_D R_S$

$\Rightarrow V_{GG} = V_{GS} + I_D R_S$

$\Rightarrow \boxed{V_{GS} = V_{GG} - I_D R_S}$

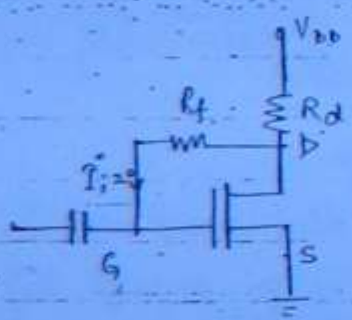
if $V_{GG} = 0$; $V_{GS} = -I_D R_S$.

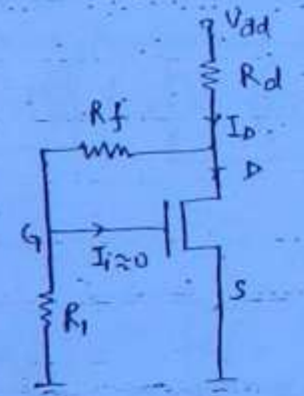
if $R_S = 0$; $V_{GS} = V_{GG}$ — (fixed Biased ckt)

→ Self bias technique cannot be used to establish an operating point for enhancement type MOSFET as voltage drop across R_S is in a direction to reverse bias the gate and forward gate bias is required for E-MOSFET.

→ This is used for JFET or depletion type MOSFET.

Drain-Gate Biasing for Enhancement Type MOSFET :-





$V_{DS} = I_i R_f + V_{GS}$

$\Rightarrow V_{DS} = V_{GS}$

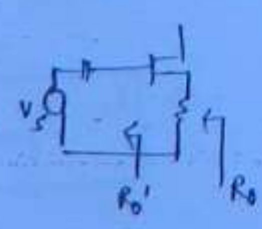
$$V_{GS} = \frac{R_1}{R_1 + R_f} \cdot V_{DS}.$$

Workbook (Chap-4)

① (b) $\mu = \frac{dV_{DS}}{dV_{GS}}$

② (c) $R_o = R_o' \parallel R_S$

$R_o' = 1/g_m = \frac{1000}{3}$



$R_o = \frac{1000}{3} \parallel 3000$

$= 300$

Ques 5: $\frac{V_o}{V_i} = -g_m R_d'$, $R_d' = r_d \| R_d = \infty \| R_d = R_d$

$\Rightarrow R_d' = 3K\Omega$.

$\because V_{GG} = 0$, $V_{GS} = -I_D \cdot R_S$

$= -2.5V$.

$\therefore g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right] = \frac{2\times10}{5}\left(1 - \frac{2.5}{5}\right) = 2$

$\therefore A_V = -2\times3 = -6$

Ques 4: $V_{GS} = V_{GG} = -2V$

$g_m = \frac{2\times10}{8}\left(1 - \frac{2}{8}\right) =$ ~~[illegible]~~ $1.875\,mS$

$A_V = -g_m R_d'$; $R_d' = 20K \| 2K$

$\Rightarrow A_V = -3.41$

Ques 6 (a)

Ques 7 (b) $A_V = -g_m R_d' = -g_m (R_d)$.

~~[illegible]~~ for ac analysis, $V_{DD} = 0$, $C \to$ short, $R_D = 5K \| 5K$.

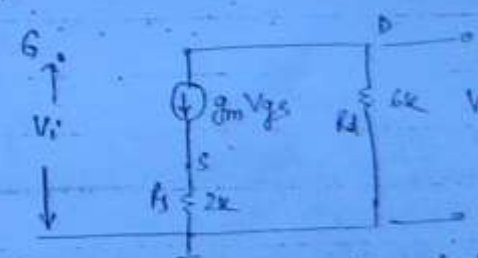
$|A_V| = 2\times(5\|5) = 5$

Ques 8 (c) $R_i' = 20 \| 100k \| \infty$

$R_i' = 16.67\,K\Omega$

Ques 9 (d) $A_V \approx -\frac{R_D}{R_S} = -3 = 2.66$ (shortcut

By model.



$\because r_d$ not given ($r_d = \infty$)

$V_o = -g_m V_{gs} \cdot R_d$.

$V_i = V_{gs} + g_m V_{gs} \cdot R_s$.

$A_V = \frac{V_o}{V_i} = \frac{-g_m R_d}{1 + g_m R_s} = \frac{-4\times6}{1+4\times2} = -2.6$

Ques 10: (a) $V_{GS} = -I_D = i_D$

$i_D = 12\left(1 + \frac{V_{GS}}{4}\right)^2$

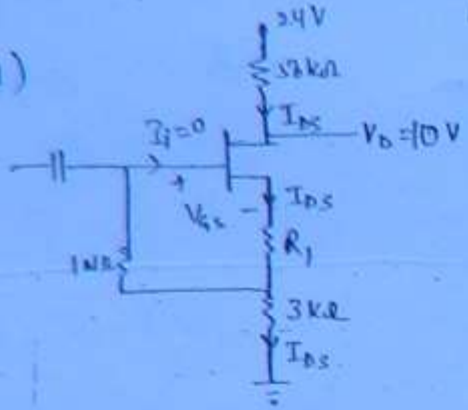
$\Rightarrow i_D = 12\left(1 + \frac{i_D}{4}\right)^2$

$\Rightarrow$ on solving,

$i_D = 2.26\,mA$.

Conventional :-

Sol^n (1)



Assuming FET is in saturation

$$V_{GS} + I_{DS} \cdot R_1 = 0$$

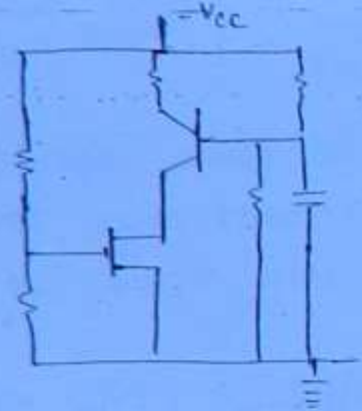
$$I_{DS} = \frac{24-10}{56} = \frac{1}{4} mA$$

$$I_{DS} = \frac{2}{1}\left(1 - \frac{V_{GS}}{(-1)}\right)^2$$

$$\Rightarrow 0.25 = 2(1 + V_{GS})^2 \Rightarrow V_{GS} = \frac{1}{2\sqrt{2}} - 1$$

Chapter 3 :-

Ques-2 :-



$$g_m = \frac{\beta}{1+\beta} \cdot g_{m1}$$

$$= \frac{99}{100} \times 2$$

$$= 1.98 \text{ mA/V}$$

1st Sep, 2012

Oscillators (Sinusoidal)

$X_f = \beta X_o = \beta A X_i$

$X_f' = -\beta A X_i$

→ Loop gain $= \frac{X_f'}{X_i} = -A\beta$

$X_f' = X_i$ then there is

→ If finite o/p w/o any i/p ; ckt acts as oscillator

$\therefore$ loop gain $= Y = (-A\beta) = 1$ → Barkhausen Criterion

phase shift $\phi = 0, 360$ or $2n\pi$.

→ $|\text{loop gain}| = A\beta = 1$.

Now, $A_f = \frac{A}{1+A\beta}$ for system satisfying Barkhausen criteria — 217

$$A_f = \frac{A}{1-1} = \infty.$$

Barkhausen Criterion :- It states that—

1) Total phase shift around as loop as signal proceeds from i/p through amplifier, feedback n/w and back to i/p again, completing a loop is multiple integral of 2π, ie,

$$\boxed{\phi = 2n\pi} \; ; \; n = 0, 1, 2 \ldots$$

2) The magnitude of product of open loop gain of amplifier, A and feedback factor β is unity.

$$\boxed{|A\beta| = 1.}$$

Practical Consideration :—

Practically magnitude of loop gain, ie, $|A\beta|$ should be kept slightly greater than unity. Then amplitude of oscillation is controlled by onset of non-linearity present in system, in other words, in a practical oscillator, loop gain is kept slightly greater than one to overcome the circuits internal losses.

Oscillators :-

→ Oscillator is basically a waveform generator, used in designing of signal generator and function generators.

→ It is also defined as an amplifier with ∞ gain.

Amplifier	Oscillator
1) Gain is finite	1) Gain is ∞.
2) Negative feedback	2) Positive feedback.
3) Excellent stability	3) less stable.

4) External i/p signal is compulsory

4) External i/p signal is not reqd. I/p signal will be noise.

Note :

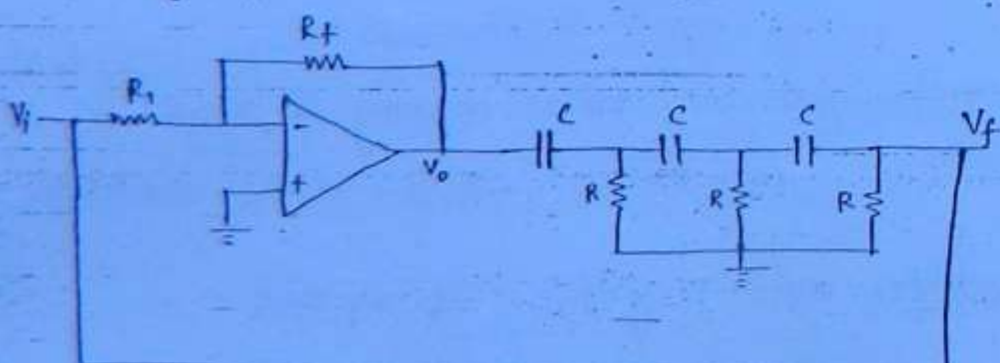
→ An amplifier can be converted into an oscillator by applying +ve feedback & increasing the gain to ∞.

→ Oscillators

- AF oscillator
  $f_o \to$ 20Hz to 20KHz
  - RC phase shift osc.
    - → By using op-Amp
    - → By using FET
    - → By using BJT
  - Wein Bridge oscillator
- RF oscillator
  $f_o >$ 20KHz
  - → Hartley
  - → Colpitt
  - → Clapp.
  - → Crystal oscillator

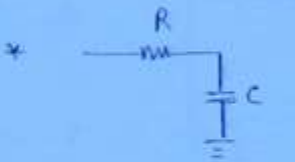
RC Phase Shift Oscillator —

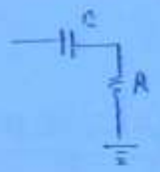
→ By using Op-Amp —



→ If $V_f = V_i$; circuit acts as an oscillator

→ feedback mechanism :- Voltage series



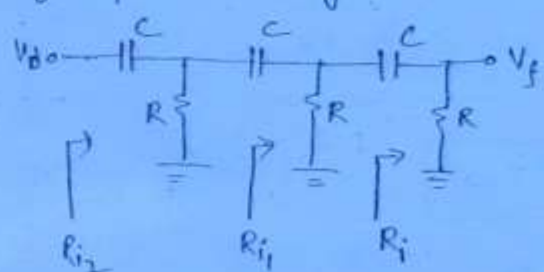


$\phi = -\tan^{-1}(\omega RC)$

$\phi = \tan^{-1}\left(\frac{1}{\omega RC}\right)$ → Preferable as lower values of R & C are required to maintain higher phase shift.

→ To get the overall gain equal to 180°, the phase shift is distributed among all the stages.

→ In this RC phase shift, three stages are added but the individual phase shift of each stage is not 60°. This is due to loading effect.



$R_{i_1} = R_i \parallel R < R$

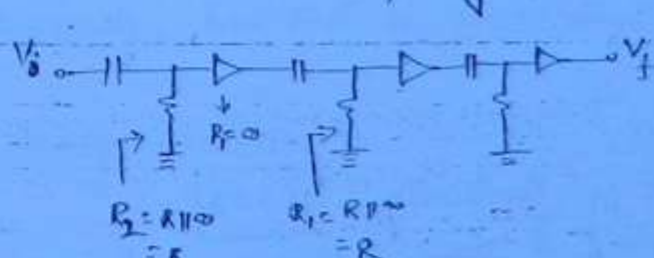
$R_{i_2} = R \parallel R_{i_1} < R.$

} Hence, phase shift of individual stage will be > 60° in this case and hence, overall $\phi > 180°$.

→ $\beta = V_f/V_o$.

→ To ~~calculate~~ set the overall $\phi = 180°$, calculate $\frac{V_f}{V_o}$ and set imaginary part equal to 0 and set values of R & C for given ω such that real part ~~= 0~~ is −ve. In this way, total $\phi = 180°$ but individual ϕ of stages is not known.

→ We can use buffer in b/w the stages to prevent loading effect but not used due to its complexity.



Voltage follower = Buffer.

→ freq. of oscillation :-

$$\beta = \frac{V_f}{V_o} = X + jY \quad . \quad \text{On putting } Y = 0 -$$

→ freq of oscillation ; $\boxed{f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi RC\sqrt{6}}}$

Substituting f_0 in β —

$\boxed{\beta = X = \frac{-1}{29}}$ ⇒ −ve real part ⇒ 180° phase shift

→ Condition for oscillation — $|A\beta| = 1$.

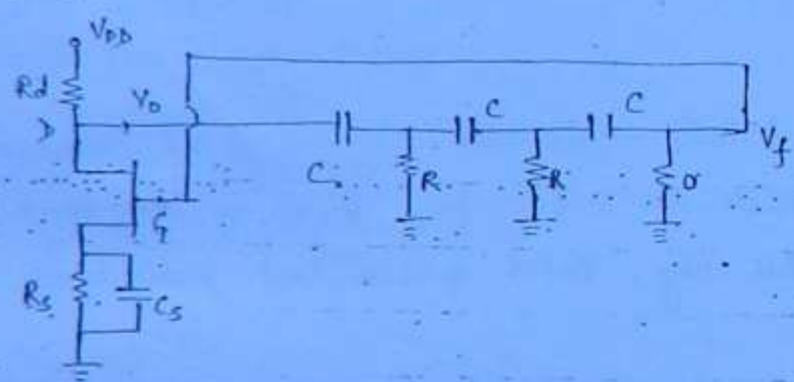
$\Rightarrow |A| = 29$

for inverting op-amp, $A = -\frac{R_f}{R_1}$

$\Rightarrow \frac{R_f}{R_1} = 29 \Rightarrow \boxed{R_f = 29R_1}$ ** Imp.

Practically, $|A\beta| \geq 1 \Rightarrow \boxed{R_f \geq 29R_1}$ {only slightly $\geq 29R_1$}.

By Using FET :-



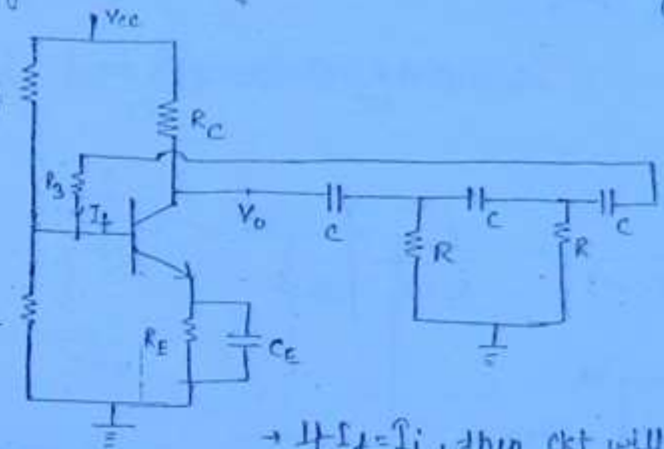
→ Voltage series FB

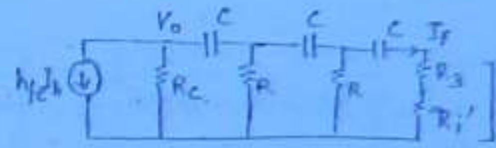
→ Condition for oscillation :- $|A\beta| = 1$

→ $A_V = -\frac{V_{ds}}{V_{gs}} = \mu$

$\Rightarrow \boxed{\mu = 29}$ → Amplification factor ; Practically, $\boxed{\mu \geq 29}$

By using BJT :-



$\equiv$ 

$R_i' = R_1 \| R_2 \| h_{ie} \approx h_{ie}$; $R_3 + R_i' = R$

→ If $I_f = I_i$, then ckt will act as oscillator.

→ Type of feedback — $\boxed{\text{Voltage Shunt}}$ ** Imp.

→ $$\boxed{f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi RC\sqrt{4K+6}} \quad ; \quad K = \frac{R_C}{R}}$$ **

→ Putting $|A_\beta| = 1$; $\boxed{h_{fe} = 4K + 23 + \frac{29}{K}}$ **

→ Diff. w.r.t. K, $\frac{d\,h_{fe}}{dK} = 0 \Rightarrow$ $\boxed{K \simeq 2.7}$ ** ; $\boxed{h_{fe\,min} = 44.54}$ **

Note.

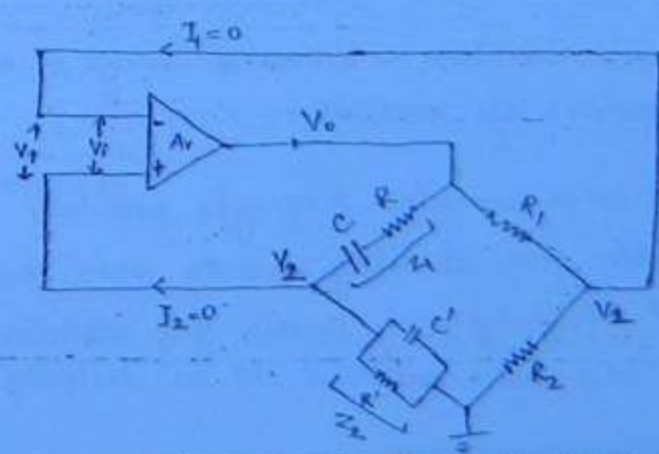
→ An FET with $\mu < 29$ cannot be used in RC phase shift oscillator.

→ A Tr. with small signal CE short ckt current gain, i.e, h_{fe} less than 44.54 cannot be used in this oscillator.

→ RC phase shift oscillator is considered as a fixed freq. oscillator since to change f_0, we have to change value of R & C of all three sections simultaneously, but this is practically very difficult.

Wein Bridge Oscillator :-

If $V_i = V_f$, then ckt acts as an oscillator.



$\rightarrow V_f = V_2 - V_1$; $\Rightarrow V_f = \frac{Z_2}{Z_1+Z_2} V_0 - \frac{R_2}{R_1+R_2} V_0$

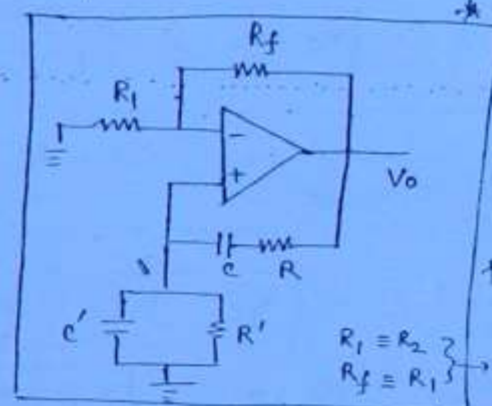
$$\therefore \beta = \frac{V_f}{V_0} = \left[\frac{Z_2}{Z_1+Z_2} - \frac{R_2}{R_1+R_2}\right] \quad ; \quad Z_2 = R' \parallel \frac{1}{sC'} \;;\; Z_1 = R + \frac{1}{Cs}$$

$$\Rightarrow \beta = \left[\frac{\omega R'C}{\omega(RC+R'C+R'C') - j(1-\omega^2 RR'CC')} - \frac{R_2}{R_1+R_2}\right]$$

Imp. part = 0

$$\Rightarrow \boxed{f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{RR'CC'}}}^{**} \text{ — Imp}$$

* check workbook Que 1 (conventional)



→ Another circuit for wein bridge osc.

→ analogous from original ckt.

Putting ω_0 in β —

$$\beta = \left[\frac{R'C}{RC+R'C+R'C'} - \frac{R_2}{R_1+R_2}\right]$$

Condition for oscillation — $|A_v \beta| = 1$

$$\Rightarrow \beta = \frac{1}{|A_v|} = \frac{1}{\infty} = 0$$

$$\Rightarrow \boxed{\frac{R'C}{RC+R'C+R'C'} - \frac{R_2}{R_1+R_2} = 0}^{**} \text{ Imp.}$$

If $R = R'$, $C = C'$ —

$$\boxed{f_0 = \frac{1}{2\pi RC}}^{*} \text{ obj}$$

Condition :— $\frac{1}{3} - \frac{R_2}{R_1+R_2} = 0 \Rightarrow \boxed{R_1 = 2R_2}^{*}$ obj.

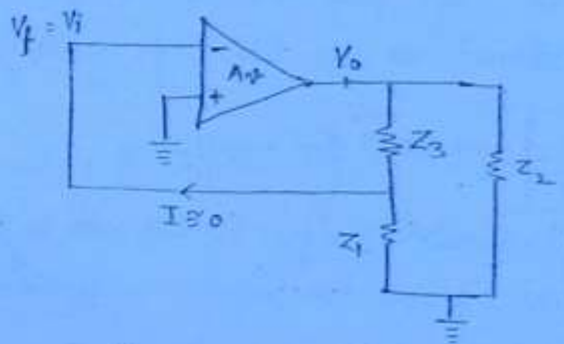
→ An oscillator circuit in which a balanced bridge is used as a feedback n/w. is called wein bridge oscillator.

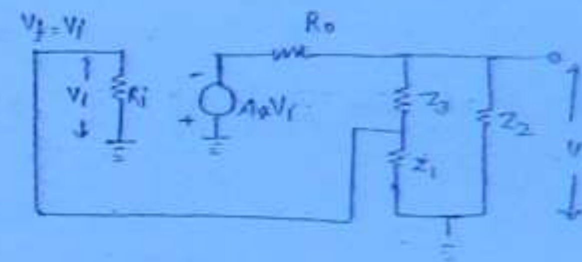
→ Advantage :- It is a variable freq. type oscillator
- Better freq. stability due to wein bridge.

→ Application — 1) Popularly used audio freq. oscillator
2) As a master oscillator ckt in designing of signal generator

RF oscillator :-

General form of oscillator circuit :-





→ $Z_L = (Z_1 + Z_3) \parallel Z_2 \quad \{ \because I \approx 0 \}$ — ①

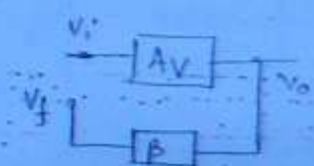
→ Z_1, Z_2 & Z_3 are all reactive ; $Z_1 = jX_1$; $Z_2 = jX_2$; $Z_3 = jX_3$ — ②

→ $V_f = \dfrac{Z_1}{Z_1 + Z_3} \cdot V_o \quad \Rightarrow \quad \beta = \dfrac{V_f}{V_o} = \dfrac{Z_1}{Z_1 + Z_3}$ — ③

→ Overall gain, $A_V = \dfrac{V_o}{V_i}$

From equivalent ckt, $V_o = \dfrac{-A_v \cdot V_i \, Z_L}{R_o + Z_L}$

$$\Rightarrow A_V = \frac{-A_v \cdot Z_L}{R_o + Z_L}$$



Now, $A_V \beta = \dfrac{-A_v \cdot Z_L}{R_o + Z_L} \times \dfrac{Z_1}{Z_1 + Z_3}$

$$= \frac{-A_v \cdot Z_1 Z_2}{R_o (Z_1 + Z_2 + Z_3) + Z_2 (Z_1 + Z_3)} \qquad \left\{ \text{on putting } Z_L = \frac{Z_2 (Z_1 + Z_3)}{Z_1 + Z_2 + Z_3} \right\}$$

On substituting from eq^n (2) :-

$$A_V \beta = \frac{A_v \cdot X_1 X_2}{jR_o (X_1 + X_2 + X_3) - X_2 (X_1 + X_3)}$$

for freq. oscillation, $I_m = 0$

$$\Rightarrow \boxed{X_1 + X_2 + X_3 = 0}$$

Now, on substituting in β -

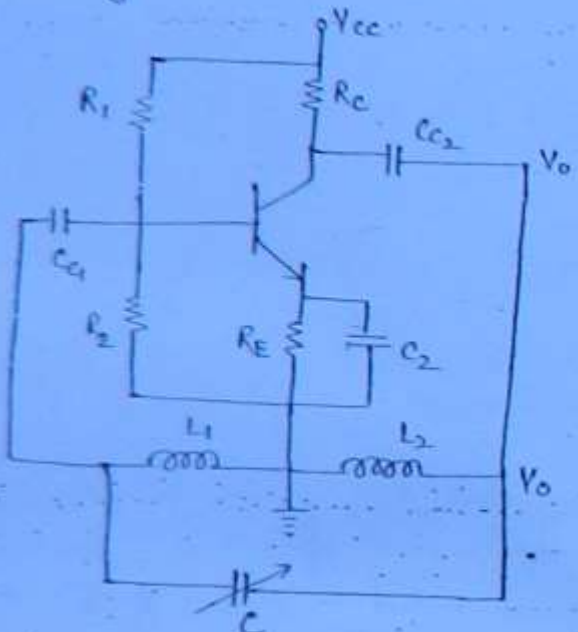
224

$$A_v\beta = \frac{A_v\, X_1 X_2}{-X_2(X_1+X_3)} = \frac{-A_v \cdot X_1}{(X_1+X_3)}$$

$$\Rightarrow A_v\beta = \frac{A_v \cdot X_1}{X_2}$$

Now, for oscillation, $|A_v\beta| \geq 1 \Rightarrow \boxed{A_v \geq \frac{X_2}{X_1}}$ → condⁿ for oscillation

Hartley Oscillator :-



$Z_1 = j\omega L_1$; $Z_2 = j\omega L_2$, $Z_3 = \frac{-j}{\omega C}$

X_1, X_2, X_3

Freq. of oscillation :-

$$X_1 + X_2 + X_3 = 0$$

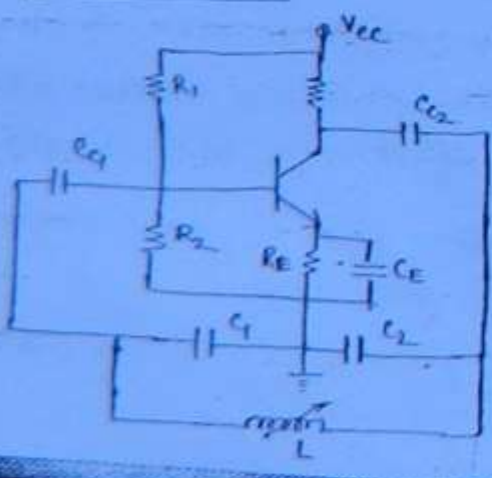
$$\Rightarrow \omega L_1 + \omega L_2 - \frac{1}{\omega C} = 0$$

$$\Rightarrow \omega = 2\pi f = \frac{1}{\sqrt{(L_1+L_2)\cdot C}}$$

$$\Rightarrow \boxed{f = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}}$$

Condition for oscillation :- $A_v \geq \frac{X_2}{X_1} \Rightarrow \boxed{A_v \geq \frac{L_2}{L_1}}$

Colpitt Oscillator :-



$Z_1 = -j/\omega C_1$, $Z_2 = \frac{-j}{\omega C_2}$, $Z_3 = j\omega L$

$$X_1 + X_2 + X_3 = 0$$

$$\Rightarrow \omega = \frac{1}{\sqrt{L \cdot \frac{C_1 C_2}{C_1+C_2}}} \; ; \; \boxed{f = \frac{1}{2\pi\sqrt{L \cdot \frac{C_1 C_2}{C_1+C_2}}}}$$

Condition:- $A_V \geq \frac{X_1}{X_2} \Rightarrow \boxed{A_V \geq \frac{C_1}{C_2}}$ — Imp (225)

Common Points :-

→ They are variable freq. type RF oscillator

→ Working principle is ~~to~~ parallel resonance.

Hartley Oscillator

→ It is also called Tapped inductor type oscillator

Advantage: Capacitive tuning, ie., no wear & tear problem.

Disadvantage:- Bulky & expensive because of two inductors.

Applications:- i) In designing of local oscillator ckt in receiver

Colpitt Oscillator

→ It has better freq. stability and it is obtained by reducing net capacitance of modified tank ckt.

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \; ; \; Q = \frac{1}{\omega RC} \; ; \text{ as } C \downarrow, Q \uparrow \Rightarrow \text{stability} \uparrow$$

Advantage:-

- It is smaller in size and economical

Disadvantage:- Inductive Tuning, ie, wear & tear problem.

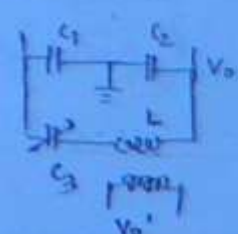
Application :- i) As a local oscillator in receiver.

Clapp Oscillator :-

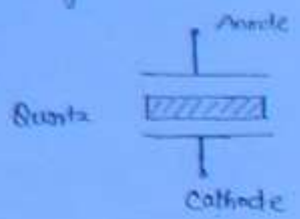
It is a modification of colpitt osc. where variable inductor is replaced by a variable capacitor C_3 in series with an inductor L and o/p is inductively obtained.

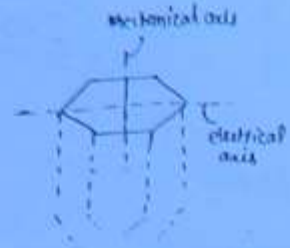
→ Working principle is series resonance, therefore

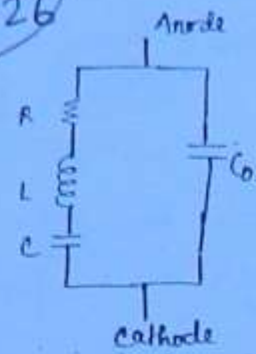
$$\boxed{f_0 = \frac{1}{2\pi\sqrt{LC_3}}}$$



Crystal Oscillator :-







AC equivalent circuit

R → internal losses or viscous daming

L → Mass of crystal

C → Stiffness = $\frac{1}{\text{spring constant}}$; C_0 = capacitance b/w anode & cathode plate.

Series resonance :- Due to RLC in series ;

→ Impedance ⇒ minimum.

→ $\boxed{f_s = \frac{1}{2\pi\sqrt{LC}}}$

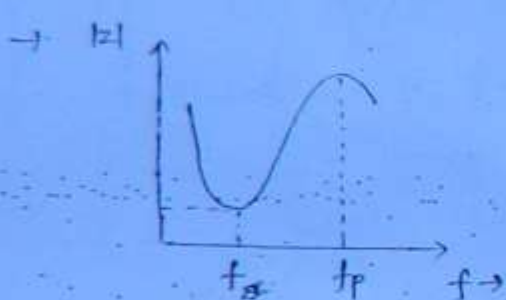
Parallel Resonance :-

→ impedance maximum

→ $\boxed{f_p = \frac{1}{2\pi\sqrt{LC_{eq}}}}$; $C_{eq} = \frac{CC_0}{C+C_0}$

→ $\boxed{f_p > f_s}$, and freq. of oscillator varies b/w f_s and f_p.

→



→ f_0 depends of l, b, t → Physical dimensions (frequency of oscillation)

→ $\boxed{f_0 \propto \frac{1}{\text{thickness}}}$ ⇒ on higher frequencies, crystal becomes weak.

→ It is a fixed frequency type RF oscillator.

→ It works on principle of piezoelectric effect.

- It has two resonating freq. , ie, f_s & f_p. Oscillating frequencies lies b/w f_s & f_p.
- Due to high quality factor Q of a resonance ckt, it provides very good freq. stability.
- freq. of oscillation, generated by crystal depends on its physical dimensions but mainly on thickness.
- On high freq., t should be small but it makes crystal mechanically weak.

Advantage :-
- Excellent freq. stability
- Simplest RF oscillator ckt.

Disadvantage :-
- Fixed freq type oscillator.

Application :- 1) To generate carrier in AM & FM transmission.
2) In designing of timer circuit.

Frequency Stability –
- freq. stability of an oscillator is measure of its ability to maintain as nearly a fixed freq as possible over as long a time interval as possible

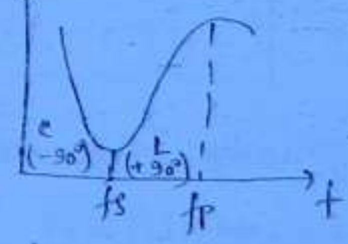
- If $d\theta$ is small change in phase angle and corresponding freq change is df, then

$$\frac{d\theta}{df} = \text{figure of merit and its value should be high.}$$

- Ideally, $\frac{d\theta}{df} = \infty$.

(reactive β n/w)

- Inverting op-amp is prefered as compared to non-inverting (resistive β n/w) as it has β n/w which is adaptable due to freq. change, ie, when ϕ changes due to temp variations, β n/w will adjust ~~itself~~ its phase so that overall change in freq. is very small.

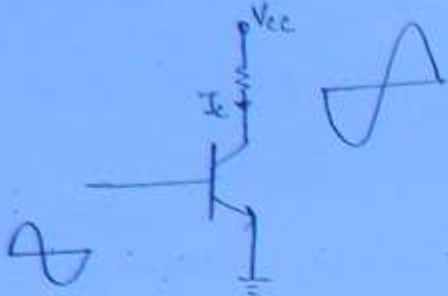


$$df = f_s^+ - (\cdot f_s^-)$$

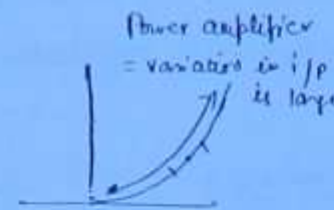
$$d\theta = 90 - (-90) = 180$$

$$\frac{d\theta}{df} = \frac{180}{f_s^+ - f_s^-} = \frac{180}{0} \simeq \infty \text{ (ideal) for crystal oscillator}$$

Power Amplifiers :-



$P_{dc} = V_{dc} \cdot I_{dc} = V_{cc} \cdot I_{CQ}$.



1) It is last stage in multistage amplifier.
2) Power amplification is defined as ability of amplifier to convert available o/p dc power into ac signal power with the application of i/p signal.

Small Signal Amp.	Large signal Amp.
→ i/p signal amplitudes are very small (μV or mV)	→ i/p signal amplitudes are very large, ($\geq 1V$)
→ operated only in linear region	→ operated both in linear & nonlinear region of i/p charc. curve.
→ Important specifications are - A_I, A_V, R_i, R_o, ϕ	→ Important specifications are - power conversion efficiency, η. - dc power available at o/p - ac " " " " - distortions at o/p.
→ Analysis of amp. will be done by using graphical as well as mathematical analysis	- By only graphical analysis.

→ Transistors used in power amp. are called power tr.

→ Power amplifiers are designed mostly by BJT & they are generally in CE mode

Harmonic Distortion :-

→ In a power amp, signal amplitudes are very large, hence signal is operated in linear & non-linear portion of i/p charac. curve., so we get harmonics in o/p & harmonic distortion is present at o/p.

— Harmonic distortion is a non-linear distortion.

fourier series expan of collector current of power transistor :- (gauss) considered

$$\rightarrow i_c = \underbrace{I_c + B_0}_{DC} + \underbrace{B_1 \cos \omega t}_{\text{fundamental}} + \underbrace{B_2 \cos 2\omega t + \cdots}_{\text{Harmonics}} \quad \rightarrow \omega t \uparrow, \text{ Amplitude } \downarrow.$$

$\rightarrow$ 2nd Harmonic distortion — $D_2 = \left|\frac{B_2}{B_1}\right|$

$\rightarrow$ 3rd ——— " ——— — $D_3 = \left|\frac{B_3}{B_1}\right|$

$\rightarrow$ AC power o/p due to fundamental component

$$\boxed{P_{ac} = I_{rms}^2 \cdot R_0 = \left(\frac{B_1}{2}\right)^2 \cdot R_0} \; \{= P_1\}$$

$\rightarrow$ Total Harmonic Power — (THP) —

$$P_T = \frac{B_1^2}{2} \cdot R_0 + \frac{B_2^2}{2} \cdot R_0 + \cdots$$

$$\Rightarrow P_T = \frac{B_1^2}{2} \cdot R_0 \left[1 + \left(\frac{B_2}{B_1}\right)^2 + \left(\frac{B_3}{B_1}\right)^2 + \cdots\right]$$

$$\Rightarrow P_T = P_1 \left[1 + D_2^2 + D_3^2 + \cdots\right]$$

— Total Harmonic Distortion (THD) —

$$D = \sqrt{D_2^2 + D_3^2 + \cdots}$$

$$\therefore \boxed{P_T = P_1 \left(1 + D^2\right)} \text{ — (imp)}$$

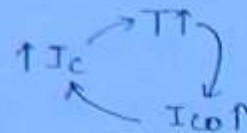
for THD = 10%, $D = 0.1$

$$\Rightarrow P_T = P_1(1 + 0.01) = 1.01 P_1$$

$\Rightarrow P_T \simeq P_1$, ie, if THD is kept $\leq 10\%$, then THP is almost equal to fundamental power.

dT_j
$1/\theta \rightarrow$ rate of heat dissipation

Thermal Runaway :-



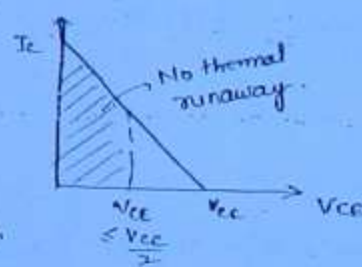
230

→ The process where a transistor is subjected to self destruction due to excess heat produced in CB junc^n

→ It is due to I_{co}.

→ BJT suffers from thermal runaway. In FET there is no thermal runaway.

Condition to eliminate thermal runaway :-



- Q point of Tr is so selected that $\boxed{V_{CE} \leq \frac{V_{cc}}{2}}$,

- $\boxed{\frac{dP_c}{dT_j} \leq \frac{1}{\theta}}$, P_c = max. collector power dissipation in W.

  T_j = junc^n temp. at collector junc^n

  θ = Thermal resistivity in °C/watts. (θ should be small)

→ $T_j - T_A \propto P_D$ T_A = ambient temp.

→ $\boxed{T_j - T_A = \theta P_D}$ —①

→ Area of collector ↑, θ↓.

→ Diff ① w.r.t T_j —

$$1 - 0 = \theta \frac{dP_D}{dT_j} \Rightarrow \boxed{\frac{dP_D}{dT_j} = \frac{1}{\theta}}$$

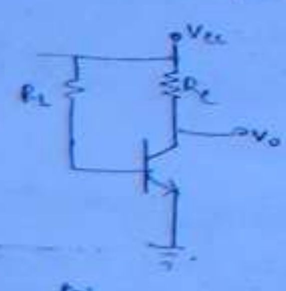
Rate of heat dissipation in atmosphere

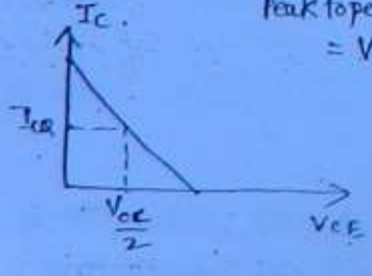
Classifications of Amplifiers :-

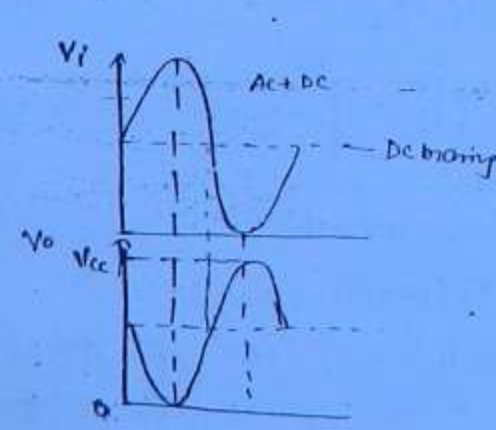
Class A operation —

Cond^n angle $= 2\pi$

Peak to peak $= V_{cc}$







— " Transformer is , $\eta = 50\%$.

— $\eta = \dfrac{\text{AC power}}{\text{DC power}}$

→ Collector current flows for entire 360° of i/p signal ; conducⁿ angle = 2π
→ Q point is located at centre of ac load line

Advantage :- → Minimum distortion
→ Excellent thermal stability, ie, no thermal runaway problem

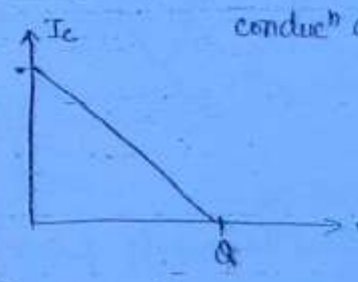
Disadvantage :- – Small power conversion efficiency
– Reduced power gain , – Introduces Power drain –
When signal is not applied , transistor is consuming max. power & it is called power drain. When signal is applied, tr. is using less power.

Application :- . designing of audio freq. amp.

Note – class A amplifier is always designed with a single amplifier, ie, single ended, ie, one Tr. per stage.

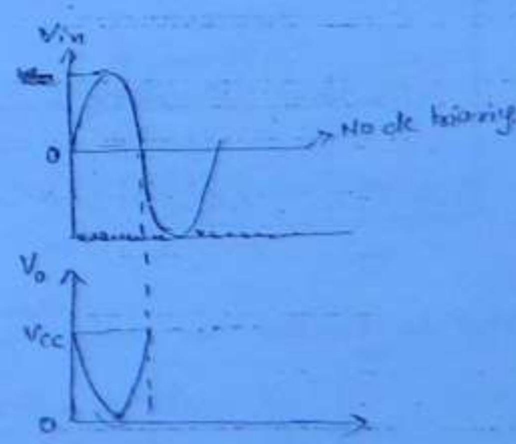
→ Power rating of transformer $P_D(max)$ → maximum allowable heat dissipation, is defined at room temp, ie., 25°C.
→ In class A operation, power dissipated by Tr is equal to max. signal power o/p.
→ For class A, $P_D = P_{omax}$; ie., max. power o/p.
Eg To design a class A amp. with 20W o/p signal power, Tr must dissipate 20W of power.

Class B operation :-



conducⁿ angle = π

$I_{CQ} = 0$; Q at cutoff.



amplifier

— for class B amplifier " ⇒ 2Vcc

- Collector current flows exactly for 180° of i/p signal (232)
- Q point is located at cutoff
- It is a double ended amplifier, i.e. two transistor in one stage.

Advantage :- - Higher efficiency. (78.5%)
- Power drain is eliminated.

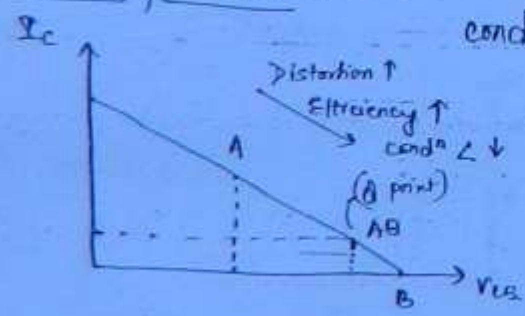
Disadvantage :- - Higher distortion
- Thermal stability is less.
- Introduce crossover distortion (COD) → major disadvantage.

Application :- - Used in designing of Power amp., for ex., push-pull power amp., complementary symmetry push pull power amp.

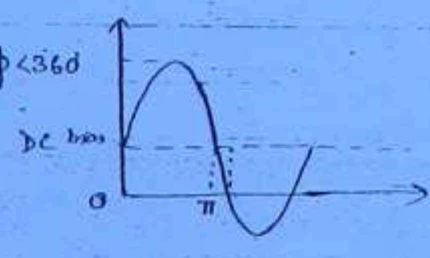
Note
- When signal is applied, Tr is consuming power & when signal is absent, Tr. will not consume any power, therefore no power drain.
- Power dissipated by single Tr. in ckt,
$P_D = 0.2\, P_{omax}$ P_{omax} = max. o/p signal power.
- Power dissipated by circuit, ie, by two tr.
$P_D = 0.4\, P_{omax}$.

For eg, to design a class B amplifier, with 20W o/p signal power, power dissipated by single transistor should be 4W.

Class AB operation :-



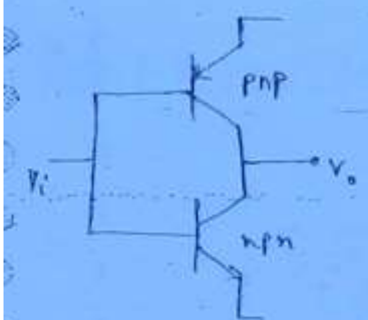
condⁿ angle - $180 < \phi < 360$

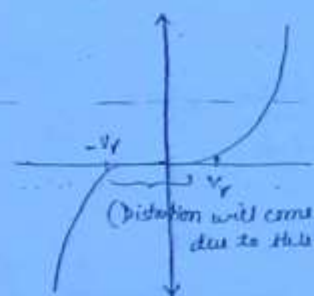


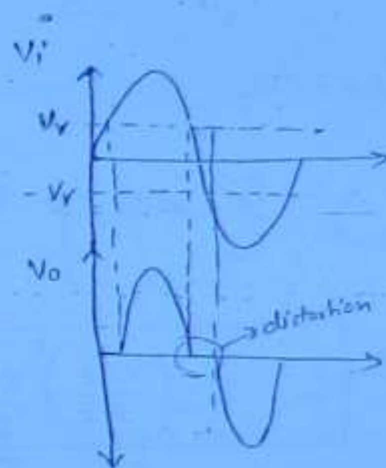
→ Q point is located in active region but very close to cutoff point.

→ Distortion & noise interference is more as compared to class A & less when compared to class B.
→ It is used in power amp for ex. push pull power amp.
→ The main advantage of class AB operation is it eliminates COD.
→ Max. efficiency is approx. 60%.

Crossover Distortion :-





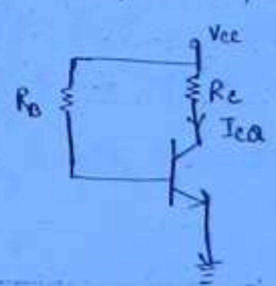


→ It is a distortion arising when conduction transfer from one tr. to other.
→ It is a non-linear distortion.
→ It is due to operating the signal over non-linear portion of charac. curve.
→ Class B introduce COD. and class AB eliminates COD.
→ The most suitable remedy to minimise COD is to use Ge Tr. in place of Si Tr. But this will reduce power handling capability of circuit.

12/09/2012

Class A amplifier :-

Direct Coupled Amplifier :-



$I_{CQ} = \frac{I_{Cmax}}{2} = \frac{V_{CC}}{2R_C}$. (∵ Q point is in centre)

DC Power :- $P_{dc} = V_{dc} \cdot I_{dc}$

$\Rightarrow \quad P_{dc} = V_{CC} \cdot I_{CQ} \Rightarrow \boxed{P_{dc} = \frac{V_{CC}^2}{2R_C}}$

AC power:

RMS $P_{AC} = V_{rms} \cdot I_{rms} = \boxed{\dfrac{V_{rms}^2}{R_L}}$

Peak $P_{AC} = \dfrac{V_P}{\sqrt{2}} \cdot \dfrac{I_P}{\sqrt{2}} = \dfrac{V_P I_P}{2} = \boxed{\dfrac{V_P^2}{2R_L}}$

Peak-Peak $P_{AC} = \dfrac{V_{P-P}}{2\sqrt{2}} \times \dfrac{I_{P-P}}{2\sqrt{2}} = \dfrac{V_{PP} \cdot I_{P-P}}{8} = \boxed{\dfrac{V_{P-P}^2}{8R_L}}$ **

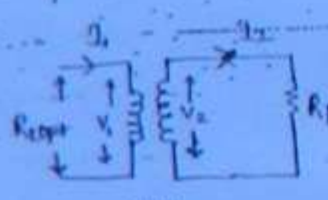
* Ideally, $V_{P-P} = V_{CC}$.

Efficiency: $\eta = \dfrac{P_{AC}}{P_{DC}} \times 100 \Rightarrow \eta = \dfrac{V_{P-P}^2/8R_L}{V_{CC}^2/2R_L} \times 100$

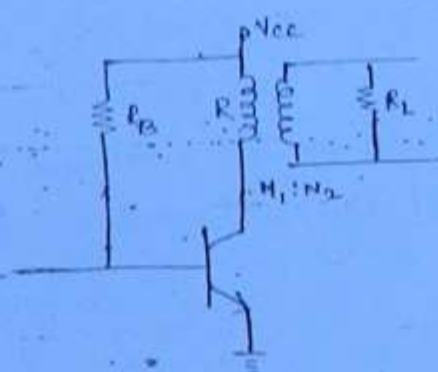
$$\Rightarrow \boxed{\eta = \frac{1}{4}\left(\frac{V_{P-P}}{V_{CC}}\right)^2 \times 100\%}$$

$\rightarrow \eta_{max} = \dfrac{1}{4} \times 100 \times \left(\dfrac{V_{CC}}{V_{CC}}\right)^2 \Rightarrow \boxed{\eta_{max} = 25\% \; ; \text{ Practically} \rightarrow 10-15\%}$

Transformer Coupled Amplifier:



$N_1 : N_2$.



→ It is used when R is very small

$\dfrac{V_1}{V_2} = \dfrac{N_1}{N_2}$; $\dfrac{I_2}{I_1} = \dfrac{N_1}{N_2}$; R_{Lopt} = optimum resistance or reflected resistance.

$R_{Lopt} = \dfrac{V_1}{I_1}$; $R_L = \dfrac{V_2}{I_2} \Rightarrow \dfrac{R_{Lopt}}{R_L} = \left(\dfrac{N_1}{N_2}\right)^2$

$\Rightarrow \boxed{R_{Lopt} = \left(\dfrac{N_1}{N_2}\right)^2 \times R_L}$ ** —(Imp).

Transformer provides-
- DC isolation
- R_L adjustment

From Graphical analysis :

$$\eta = 50 \times \left(\frac{V_{CEmax} - V_{CEmin}}{V_{CEmax} + V_{CEmin}} \right)^2 \%$$

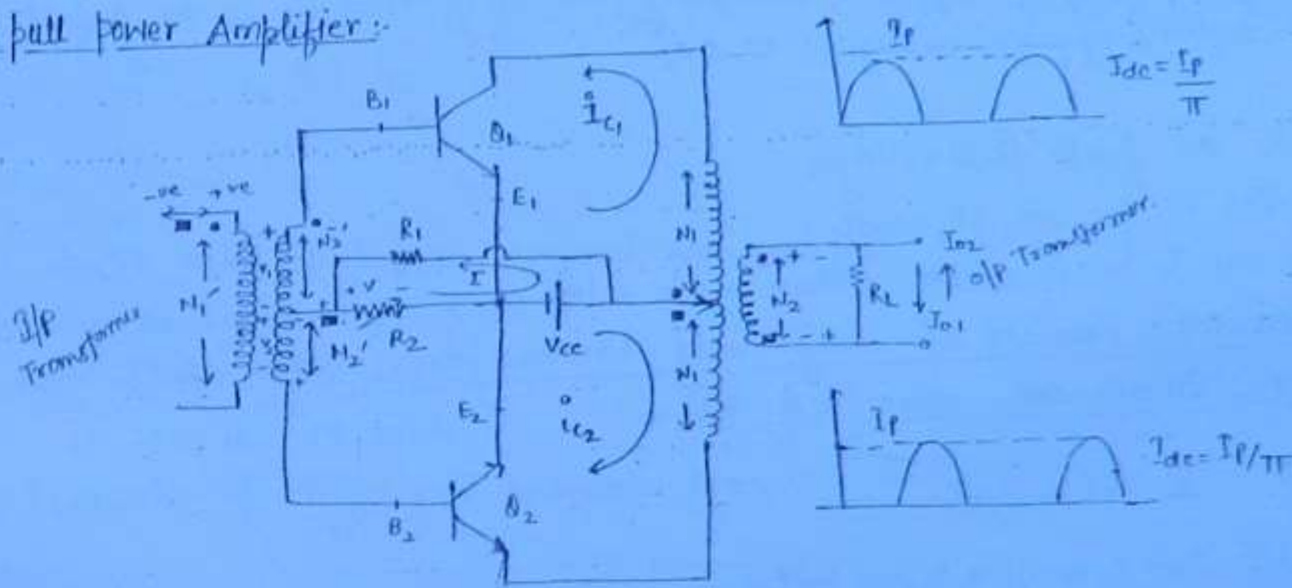
235

→ ideally , $V_{CEmin} = 0$

$\Rightarrow$ $\boxed{\eta_{max} = 50\%}$

Practically, $\boxed{\eta \Rightarrow 30-35\%}$

Push pull power Amplifier :-

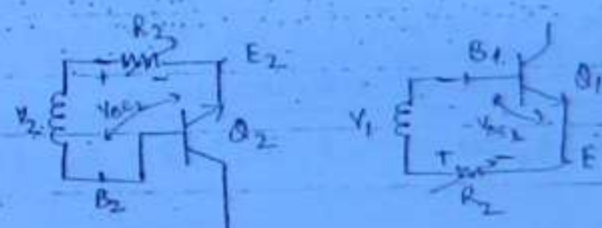


During +ve half , Q_1(ON) , Q_2(OFF)

$I_{o1} \propto i_{c_1}$

During -ve half, Q_1 (OFF) , Q_2 (ON)

$I_{o2} \propto i_{c_2}$



$\therefore\ I_o \propto (i_{c_1} - i_{c_2}) \Rightarrow I_o = K(i_{c_1} - i_{c_2})$

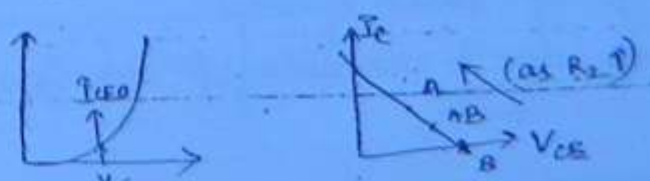
When signal is absent — $V_1 = V_2 = 0$.

→ let $R_2 = 0$, $\Rightarrow V_{BE_1} = V_{BE_2} = 0$ ⇒ both Q_1 & Q_2 in cutoff → class B operation

→ $R_2 \uparrow \Rightarrow IR_2 \uparrow$ and when $IR_2 = V_\gamma$ $\therefore V_{BE_1} = V_{BE_2} = V_\gamma$ → class AB operation

→ $R_2 \uparrow$, $IR_2 \uparrow$ and $V_{BE} \uparrow$ and Q will move towards saturation

↳ class A operation



→ I_{CEO} is the stand by current during class AB operation.

236

→ It is double ended amp.
→ It can be class B or class AB operated.
→ Designed with identical ~~transformers~~ Tr.
→ The ckt operates in class B when $R_2 = 0$.
→ For class AB operation, voltage drop across R_2 is adjusted to be approx. equal to V_γ, where a small standby current flows at zero excitation.
→ The funcⁿ of centre tapped secondary coil of i/p transformer is to provide two equal & opposite voltages V_1 & V_2.

→ V_1 & V_2 are push pull voltages
→ Both the Tr. are in CE mode.
→ When one Tr is in active, other is in cutoff.
→ <u>o/p current consists of only odd harmonic terms since in o/p I, even harmonic terms are cancelled out.</u>

<u>Proof</u> ⇒ $\because I_0 = K(i_{c_1} - i_{c_2})$ (6 marks)

$$i_{c_1} = B_0 + B_1 \cos\omega t + B_2 \cos 2\omega t + \dots$$
$$i_{c_2} = B_0 + B_1 \cos(\omega t + \pi) + B_2 \cos 2(\omega t + \pi) + \dots$$
$$= B_0 - B_1 \cos\omega t + B_2 \cos 2\omega t + \dots$$
$$\therefore \boxed{I_0 = 2K(B_1 \cos\omega t + B_3 \cos 3\omega t + B_5 \cos 5\omega t + \dots)}$$

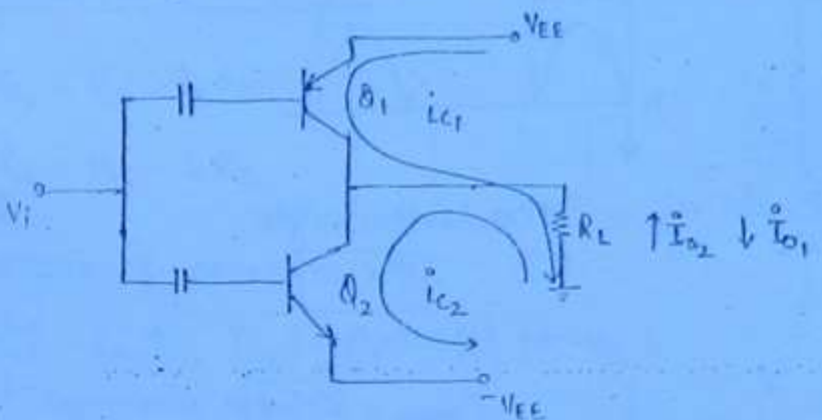
→ <u>First available harmonic distortion</u> $\boxed{,\ D_3 = \left|\frac{B_3}{B_1}\right|}$ = (very small)

<u>Note</u> If Q_1 & Q_2 are not identical, then even harmonics will be present in o/p & distortion will be large.

<u>Advantage</u>: 1) Higher o/p power due to double ended.
2) " Efficiency if class B operated
3) less distortion due to cancellation of even harmonics.

Disadvantage :- Very bulky & highly expensive due to requirement of bulky transformer.

Complementary - Symmetry Push Pull Power Amplifier :-



For $V_i > 0$ —
$Q_1 = OFF$, $Q_2 = ON$, $i_{o_2} = i_{c_2}$

for $V_i < 0$ —
$Q_1 = ON$, $Q_2 = OFF$, $i_{o_1} = i_{c_1}$

→ It is double ended amplifier designed with matched pairs of Tr.
→ Popularly used Power amp ckt.
→ Always class B operated.
→ Both Tr. are in CE mode.
→ o/p I consists of only odd harmonic terms.

Advantage :- – same as push pull B amplifier.
– circuit is smaller in size & economical due to elimination of bulky transformer.

Disadvantage :- – Requires two power supply
– introduces COD

Efficiency :- $\eta = \frac{P_{ac}}{P_{dc}} \times 100\%$

→ ideally, $V_P = V_{cc}$.

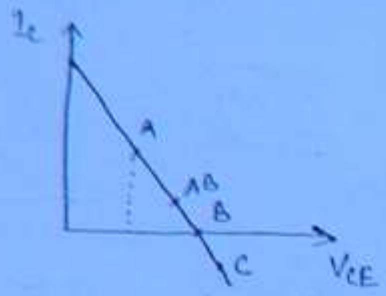
$\therefore \boxed{P_{ac} = \frac{V_P^2}{2R_L}}$

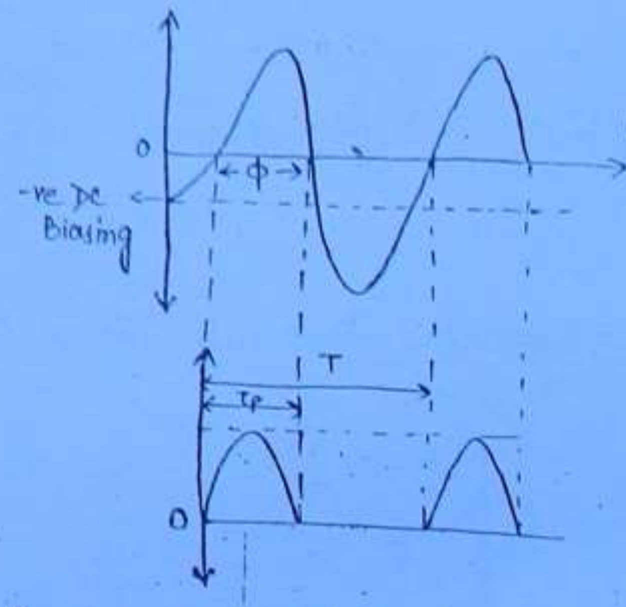
$P_{dc} = \underset{\text{when } Q_1 \text{ ON}}{V_{cc} \times \frac{I_P}{\pi}} + \underset{\text{when } Q_2 \text{ ON}}{V_{cc} \times \frac{I_P}{\pi}}$.

$\Rightarrow \boxed{P_{dc} = \frac{2V_{cc} \cdot I_P}{\pi} = \frac{2V_{cc} \cdot V_P}{\pi R_L}}$ —(imp)

$\therefore \boxed{\eta = \frac{\pi}{4} \times \left(\frac{V_P}{V_{cc}}\right) \times 100\%}$ ** ; $\eta_{max} = \frac{\pi}{4} \times 100\% \Rightarrow \boxed{\eta_{max} = 78.5\%}$ **

Class C amplifier :-





→ Duty cycle : $\boxed{\frac{\tau_P}{T} \times 100\% = D}$

→ Power dissipation across Tr. during τ_P –

$$\boxed{P_D = V_{CE} \cdot I_C}$$

→ Energy dissipation across Tr during τ_P –

$$\boxed{E_D = P_D \cdot \tau_P}$$

→ Avg. power dissipation during one cycle :-

$$P_{Davg} = \frac{E_D}{T} = \frac{P_D \cdot \tau_P}{T} \Rightarrow \boxed{P_{Davg} = P_D \cdot D}$$

→ conduction angle

$$\boxed{\phi < 180^\circ}$$

→ Efficiency –

$$\boxed{\eta_{max} = 87.5\%}$$

→ Distortion is very high.

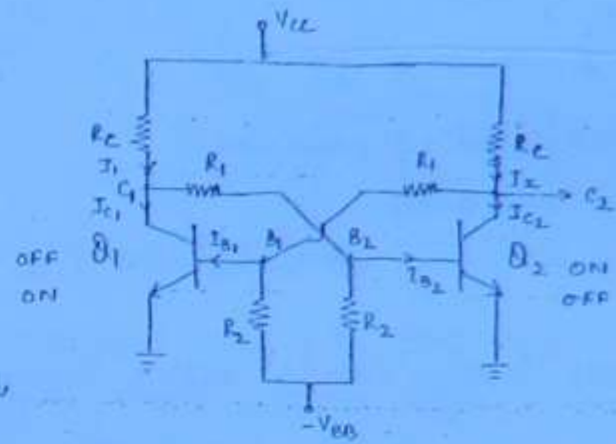
Class D Amplifier :-

– They are special amplifier designed to operate with digital pulse signal.
→ Efficiency of class D is above 90%.
→ It is not a power amplifier.
→ Widely used in commercial application.

Multivibrator by using Transistors :-

Bistable Multivibrator —

a) Fixed Bias Binary —



$V_{C_2} = V_{cc} - I_2 R_c$

$V_{C_1} = V_{cc} - I_1 R_c$

→ Because of noise —

$V_{B_2}\uparrow,\ I_{B_2}\uparrow,\ I_{C_2}\uparrow,\ I_2\uparrow,\ V_{C_2}\downarrow,\ V_{B_1}\downarrow$

"Regenerative action"

$V_{C_1}\uparrow,\ I_1\downarrow,\ I_{C_1}\downarrow,\ I_{B_1}\downarrow$

→ Finally Q_2 in saturation and Q_1 in cutoff.

$$Q = V_{C_2} = V_{CEsat} = 0 \quad ; \quad \bar{Q} = V_{C_1} \simeq V_{cc} = 1.$$

When a -ve pulse is applied —

at B_2 — $V_{B_2}\downarrow,\ I_{B_2}\downarrow,\ I_{C_2},\ I_2\downarrow,\ V_{C_2}\uparrow,\ V_{B_1}\uparrow,\ I_{B_1}\uparrow,\ I_{C_1},\ I_1\uparrow,\ V_{C_1}\downarrow$

"Regenerative action"

Finally Q_2 in cutoff & Q_1 in saturation —

$$Q = V_{C_2} \simeq V_{cc} = 1 \quad ; \quad \bar{Q} = V_{C_1} = V_{CEsat} = 0.$$

When Q_2 = on ; Q_1 = off ⇒ Q_2 should be well in saturation & Q_1 should be well in cutoff.

$$V_{C_2} = V_{CEsat}, \quad V_{C_1} = \frac{V_{cc}R_1}{R_1+R_c} + \frac{V_{BEsat}R_c}{R_1+R_c} \simeq V_{cc}$$

→ $I_{C_1} = I_{B_1} = 0$

→ $V_{B_1} = \dfrac{V_{CEsat}R_2}{R_1+R_2} - \dfrac{V_{BB}\cdot R_1}{R_1+R_2}$; $V_{B_1} \approx 0$ when $V_{BB} = 0.0$ ⇒ Noise Margin $\overset{0.5}{\underset{0}{\uparrow}}$ less

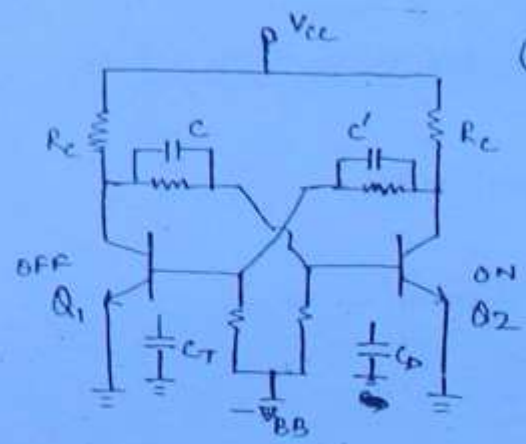
V_{B_1} = well in cutoff when V_{BB} is present (Reqd) ⇒ Noise margin more

0.5

↑ = +2.5

−2 (more)

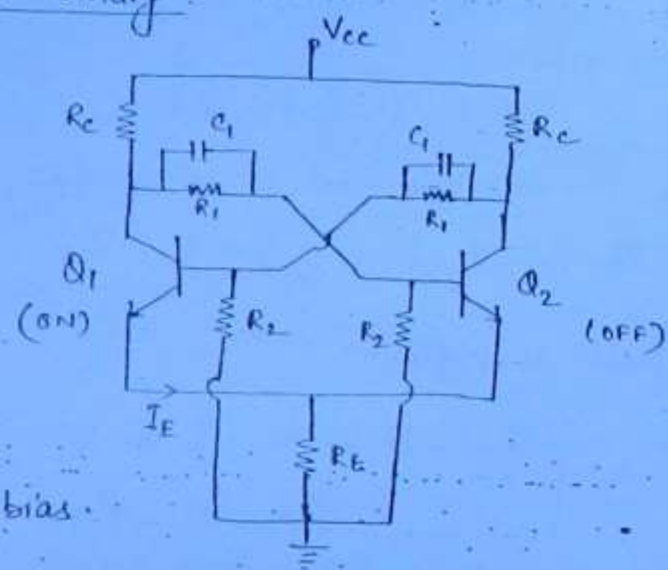
Commutating Capacitors – (C & C')



→ C_D & C_T are transition & diffusion capacitances of ON & OFF Tr. respectively.

→ C & C' are speed up capacitors.
→ C & C' → very small
→ Due to C & C' → ↓ in transition time or ↓ in propagation delay.

Self Biased Binary / Emitter Coupled Binary :

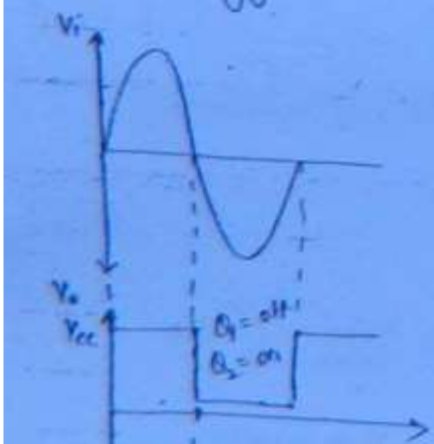


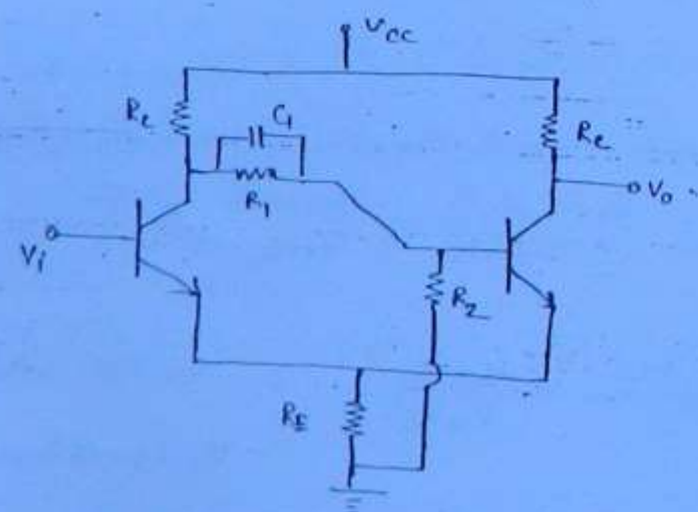
→ 

but there will be drop across RE due to I_E in ON Tr.

and its min. voltage reqd. to ON Q_2 is at least $(V_E + 0.5)$ and hence $-V_{BB}$ is not required in this ckt.
→ Other operation is same as fixed bias.

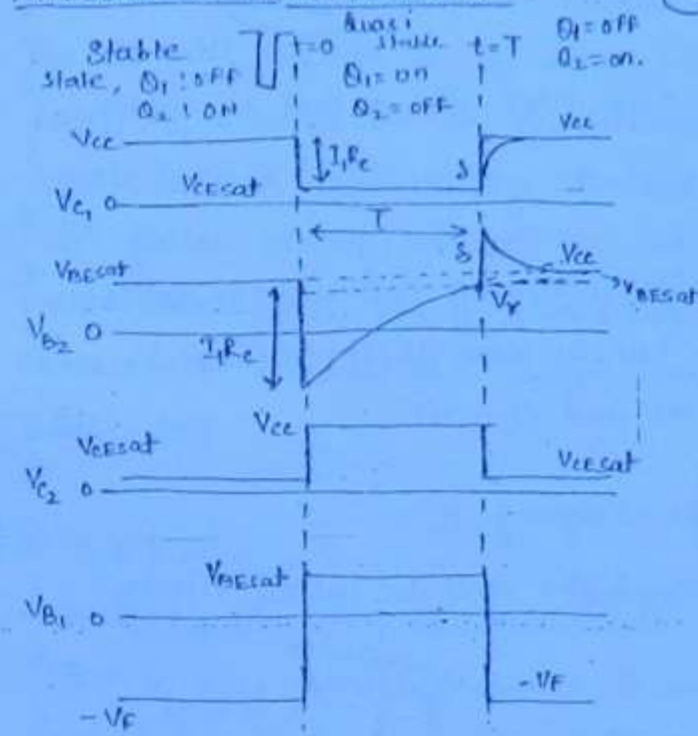
Schmitt Trigger :

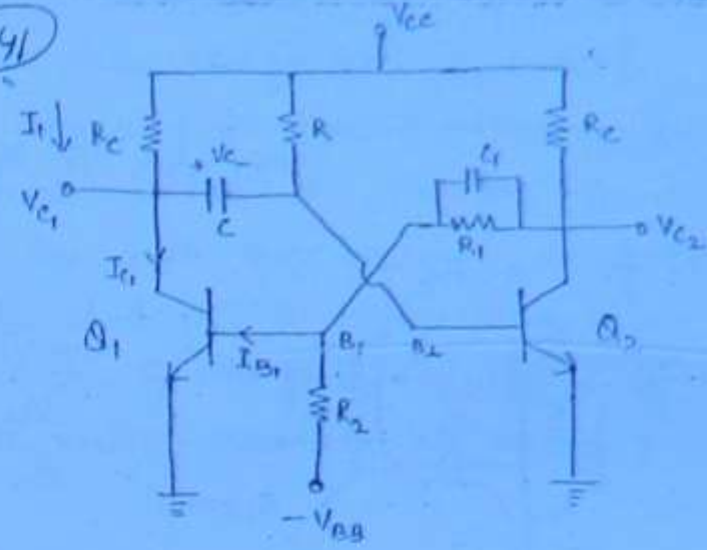




Monostable Multivibrator :-

(241)





For $t<0$ ckt is in stable state.

$$\boxed{Q_1 : \text{OFF}, \quad Q_2 : \text{ON}}$$

$V_{c_2} = V_{CEsat}$; $V_{B_2} = V_{BEsat}$

$\because$ capacitor will act as open circuit.

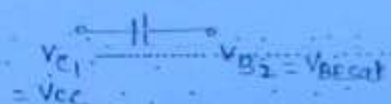
$I_{c_1} = I_{B_1} = 0$, $\therefore$ current through $R_c \to 0$

Hence $\forall$ ~~Vcc~~ = $\boxed{V_{c_1} = V_{cc}}$

and $V_{B_1} = \dfrac{V_{CEsat} \cdot R_2}{R_1 + R_2} - \dfrac{V_{BB} \cdot R_1}{R_1 + R_2} = -V_F$

→ At $t \le 0$, voltage across C -

$\therefore \boxed{V_c = V_{cc} - V_{BEsat}}$



→ For $t>0$ A trigger is applied and Q_2 : OFF & Q_1 : ON.

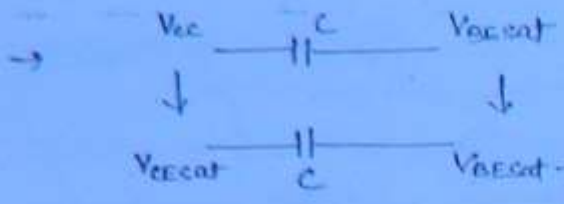
When Q_2 = OFF, $V_{c_2} = V_{cc}$ and it will be transferred to B_1 by commutating capacitor.

& Now, Q_1 will be ON due to this. & $V_{c_1} = V_{CEsat}$

→ Capacitor C is called timing element (capacitance) and its value is very large and it does not allow sudden change.

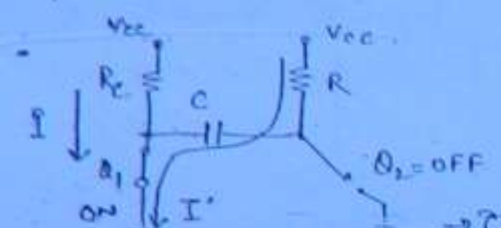
→ A current I_1 will flow in Q_1 -

$$I_1 = \frac{V_{cc} - V_{CEsat}}{R_c}$$

→ 

$V_{BEsat} - I_1R_1 \Rightarrow V_{BE} << 0$ and Q_2 is well in cutoff.

→ Now, for $0 \le t \le T$ –



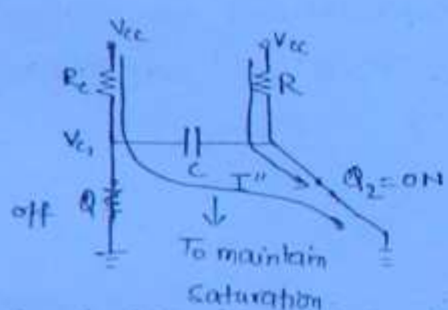
I' will start charging capacitor towards V_{cc}, but as soon as it reaches V_γ, Q_2 = ON and Q_1 = OFF

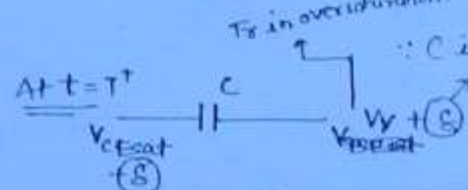
→ $\tau = RC$ – for charging C.

R & C → very high. and are called timing elements.

For $t > T$

At $t = T^+$,





∵ C is large, it does not allow sudden change

$(\delta >> V_\gamma)$

Now, I'' will start charging C and V_{C_1} will start ↑ towards V_{cc} and $V_\gamma + \delta$ will start discharging and will settle at V_{BEsat}. (see graph)

Important Points:

→ Waveform:–

for $t<0$:- The circuit is in stable state with Q_2 (ON) & Q_2 (OFF). Capacitor C will act as open ckt.

for $0 \le t \le T$ + Quasi Stable state.

- On application of -ve trigger, at $t=0$ to base B_2, a regenerative action takes place driving Q_2 below cutoff. Now voltage at C_2 rises to V_{cc} (off) and because of cross coupling b/w C_2 & B_1, Q_1 comes into saturation
- Now current I_1 exist in R_c of Q_1 and V_{C_1} drops abruptly by an amount I_1R_c upto V_{CEsat}. The voltage at B_2 drops by same amount I_1R_c since C_1 & B_2 are capacitively coupled.

- Now the multivibrator is in Quasi stable state with Q_1 (ON) & Q_2 (OFF).
- The ckt will remain in QS state for only a finite time T because base B_2 is connected to V_{cc} through a resistance R, therefore V_{B_2} starts to rise exponentially towards V_{cc} with time constant RC & when it passes cutin voltage V_γ of Q_2 at $t=T$, a regenerative action will take place as a result of which Q_1 will go into cutoff & Q_2 comes into conduction and multivibrator returns to its initial stable state.

For $t \geq T$ –

- At $t=T^+$, Q_1 = OFF, Q_2 = conducted. V_{C_2} drops to V_{CEsat}. V_{B_1} returns to $-V_F$. Now V_{C_1} rises abruptly since Q_1 is off. This ↑ in V_{C_1} transmitted to base of Q_2 and Q_2 goes into over saturation. Hence an overshoot δ develops in V_{B2} at $t=T^+$ which decays as exp the capacitor recharge

Derivation of T :

C will charge

$$V_{B_2} = V_f - (V_f - V_i)e^{-t/\tau}$$

→ $V_f = V_{cc}$; $V_i = V_{BEsat} - I_1 R_c$ where $I_1 R_c = V_{cc} - V_{CEsat}$

$$\Rightarrow V_i = V_{BEsat} - V_{cc} + V_{CEsat}$$

→ $\tau = RC$

$$\therefore \quad V_{cc} - (V_{cc} - V_{BEsat} + V_{cc} - V_{CEsat})e^{-t/RC} = V_{B_2}$$

$$\Rightarrow V_{B_2} = V_{cc} - \left[2V_{cc} - (V_{CEsat} + V_{BEsat})\right] e^{-t/RC}$$

- at $t=T$, $V_{B_2} = V_\gamma$ –

$$V_\gamma = V_{cc} - \left[2V_{cc} - (V_{CEsat} + V_{BEsat})\right] e^{-T/RC}$$

$$\Rightarrow \boxed{T = RC \ln \frac{(2V_{cc} - (V_{CEsat} + V_{BEsat}))}{V_{cc} - V_\gamma}}$$

$$\Rightarrow T = RC\ln 2 + RC\ln\left(\frac{V_{CC} - \frac{V_{BEsat}+V_{CEsat}}{2}}{V_{CC}-V_r}\right)$$

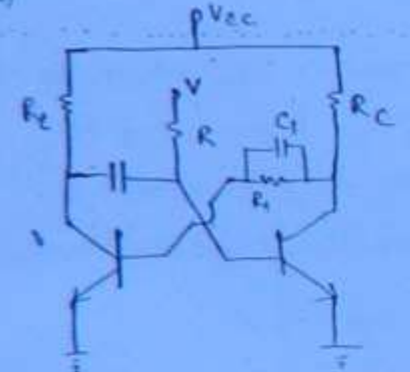
For Si —

$$\frac{V_{BEsat}+V_{CEsat}}{2} = \frac{0.8+0.2}{2} = 0.5 = V_r.$$

$$\therefore\ T = RC\ln 2 + RC\ln\left(\frac{V_{CC}-V_r}{V_{CC}-V_r}\right)$$

$$\Rightarrow \boxed{T = RC\ln 2 = 0.69\,RC}\ **$$

(Workbook)
*
Chap 11
Conv-1

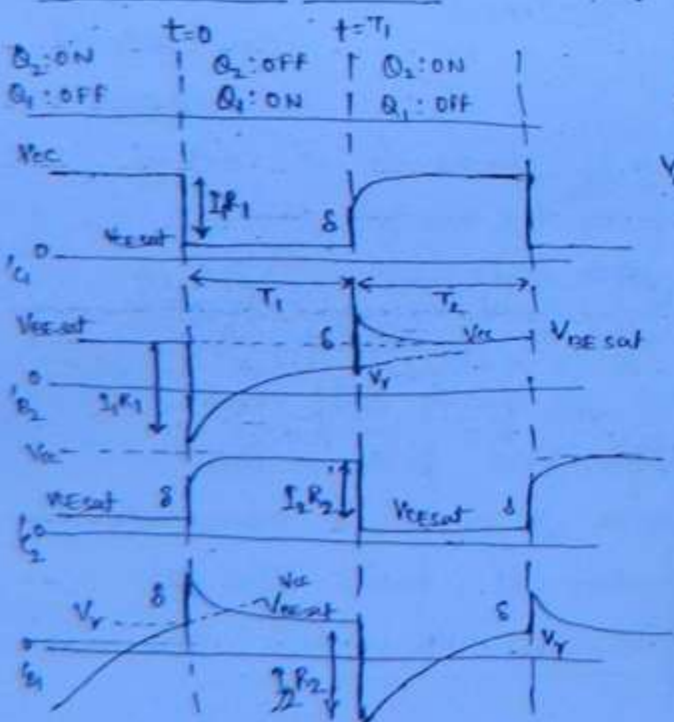


→ In the above derivation change $V_f = V$ & assume $V_{BEsat}+V_{CEsat} \ll V + V_{CC}$ & $V_\gamma \ll V$.

$$\rightarrow \boxed{T = RC\ln\left(1+\frac{V_{CC}}{V}\right)}$$

Diagram for voltage controlled f (or T)

Astable Multivibrator



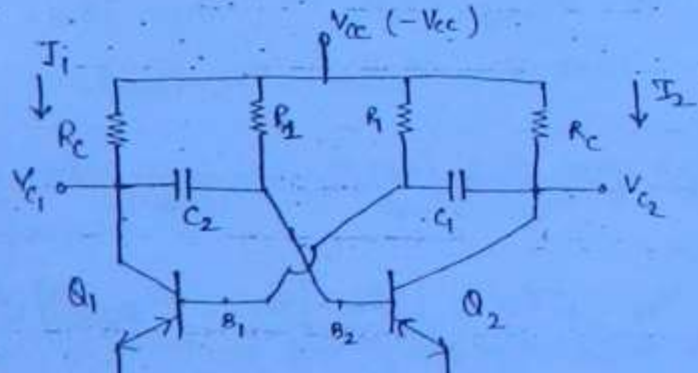


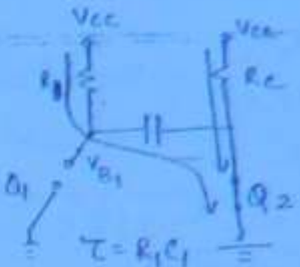
Fig 1

245

for $t<0$ Q_1 : OFF , Q_2 : ON

$V_{C_2} = V_{CEsat}$; $V_{B_2} = V_{BEsat}$

$I_{C_1} = I_{B_1} = 0$; $V_{C_1} = V_{CC}$ & $V_{B_1} < 0$.

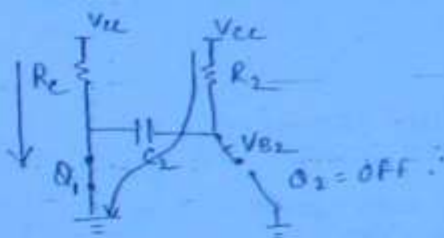


For $t \le 0$

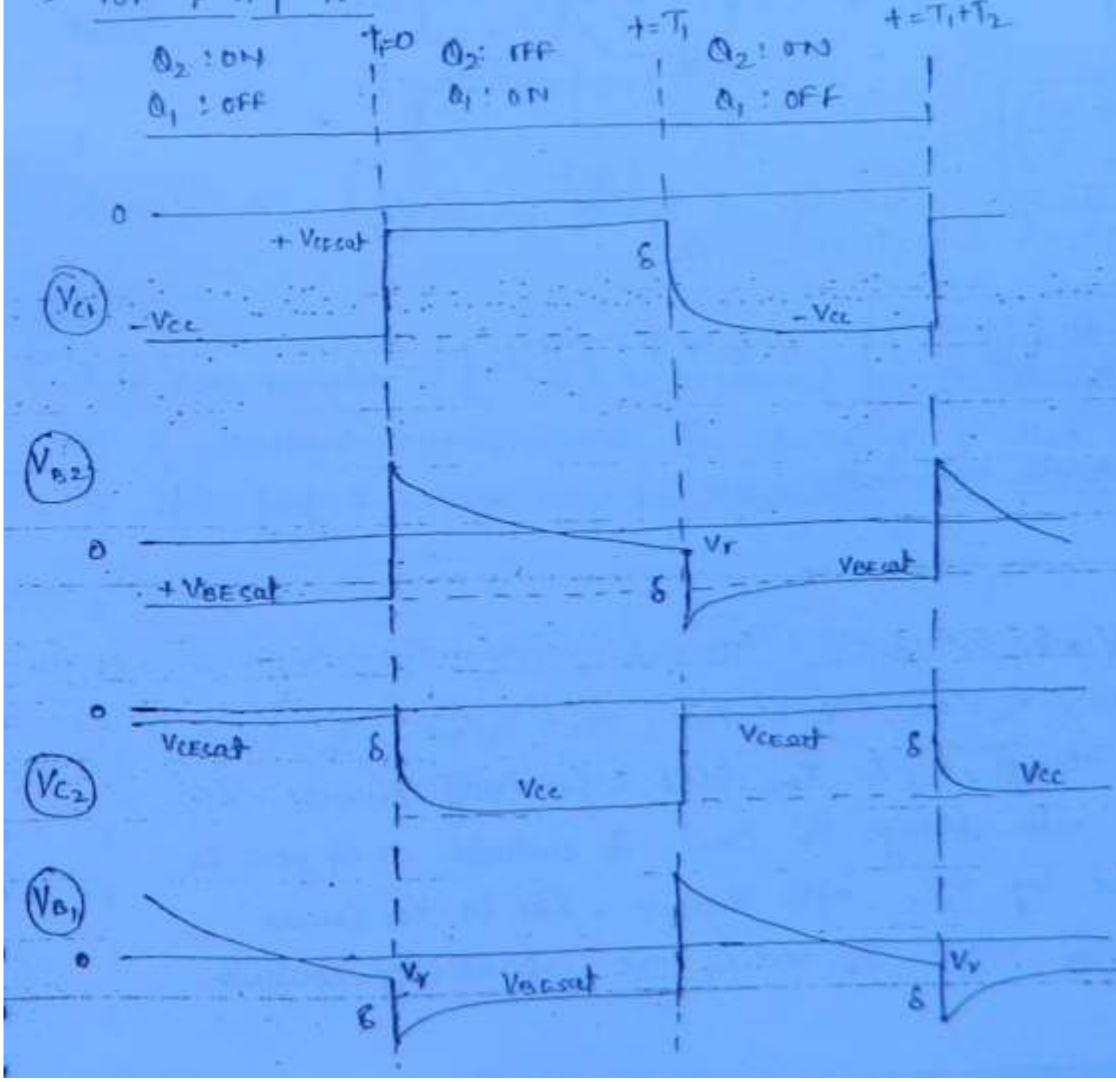
→ C_1 will charge & $V_{B_1} \uparrow$ till V_γ & then states will change with sudden change in V_{C_2} & V_{B_1}.

for $0 \le t \le T_1$ — Q_2 : OFF ; Q_1 : ON

Now C_2 will ~~start~~ charging & similar process as above will be repeated.



→ for p-n-p Tr



$\rightarrow$ $T_1 = 0.69 R_2 C_2$
$T_2 = 0.69 R_1 C_1$ } $\because T_1 \neq T_2$; $D \neq 50\%$ $\Rightarrow$ Asymmetrical square wave

246

$\rightarrow$ $T = T_1 + T_2 = 0.69 (R_1 C_1 + R_2 C_2)$

$\rightarrow$ $\boxed{f = \frac{1}{T} = \frac{1.44}{R_1 C_1 + R_2 C_2}}$; if $R_1 = R_2 = R$ & $C_1 = C_2 = C$ then $\boxed{T = 1.38RC}$

For asymmetrical sq. wave — For symmetrical sq. wave

$\rightarrow$ Voltage to freq. converter :-

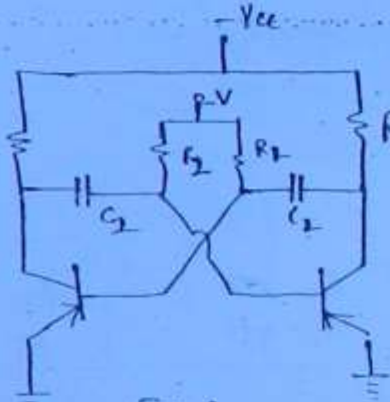


Fig 2

$T_1 = R_2 C_2 \ln\left(1 + \frac{V_{cc}}{V}\right)$

$T_2 = R_1 C_1 \ln\left(1 + \frac{V_{cc}}{V}\right)$

$$\boxed{T = (R_1 C_1 + R_2 C_2) \ln\left(1 + \frac{V_{cc}}{V}\right)}$$

$\rightarrow$ $f = 1/T$ & if $R_1 = R_2 = R$ & $C_1 = C_2 = C$ then

$$\boxed{T = 2RC \ln\left(1 + \frac{V_{cc}}{V}\right)}$$ $\therefore$ as $V\uparrow$, $T\downarrow$ & $f\uparrow$.

Important Points for Astable Multivibrator :-

Waveform (pnp)

for $t<0$ Q_1 : OFF , Q_2 : ON

Hence, for $t<0$, $V_{B_1} = +ve$, $V_{C_1} = -V_{cc}$, $V_{B2} = V_{BEsat}$, $V_{C_2} = V_{CEsat}$

$\rightarrow$ Capacitor C_1 charges through R_1 & V_{B_1} falls exponentially towards $-V_{cc}$.

$\rightarrow$ At $t=0$, V_1 reaches cutin voltage V_γ and Q_1 conducts. As Q_1 goes to saturation, V_{C_1} rises by $I_1 R_C$ upto V_{CEsat}. Rise in V_{C_1} causes equal rise $I_1 R_C$ in V_{B_2} since B_2 and C_1 are capacitively coupled.

- Rise in V_{B2} cuts off Q_2 and its collector falls towards $-V_{cc}$. This fall in V_{C_2} is coupled through capacitor C_1 to base B_1 causing undershoot δ. in V_{B_1} and abrupt amou drop by same amount δ in V_{C_2}.

- The voltage V_{B_2} is $V_{BEsat} + I_1R_c$ at $t = 0^+$. and $\downarrow$ exponentially with time constant R_2C_2 towards $-V_{cc}$.

At $t = T_1$; base B_2 reaches cutin level V_γ and reverse transition takes place

In Fig(1), the frequency of oscillation may be varied over the range from Hz to MHz by adjusting R or C. It is also possible to change T electrically by connecting R_1 & R_2 to an auxillary voltage $-V$ (fig.2) (The collector supply remains $-V_{cc}$). then,

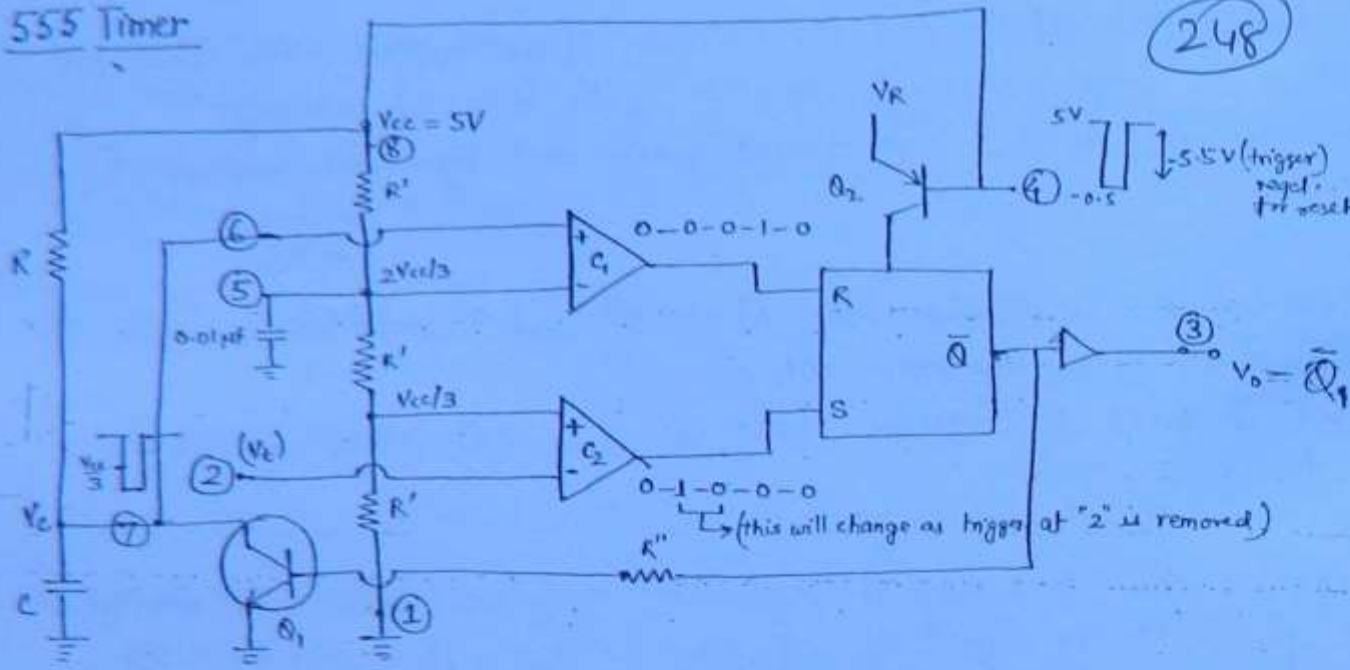
$$T = 2RC \ln\left(1 + \frac{V_{cc}}{V}\right).$$

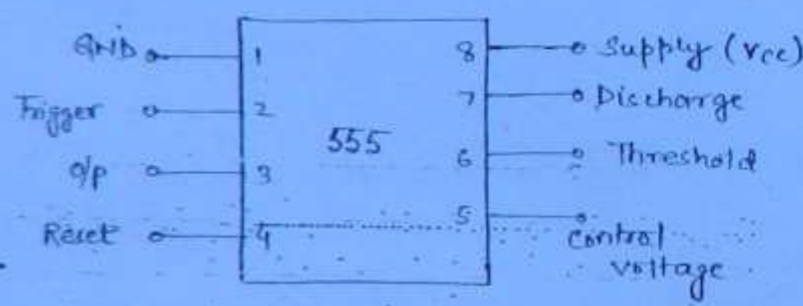
Such a ckt (fig 2) is voltage to frequency converter.

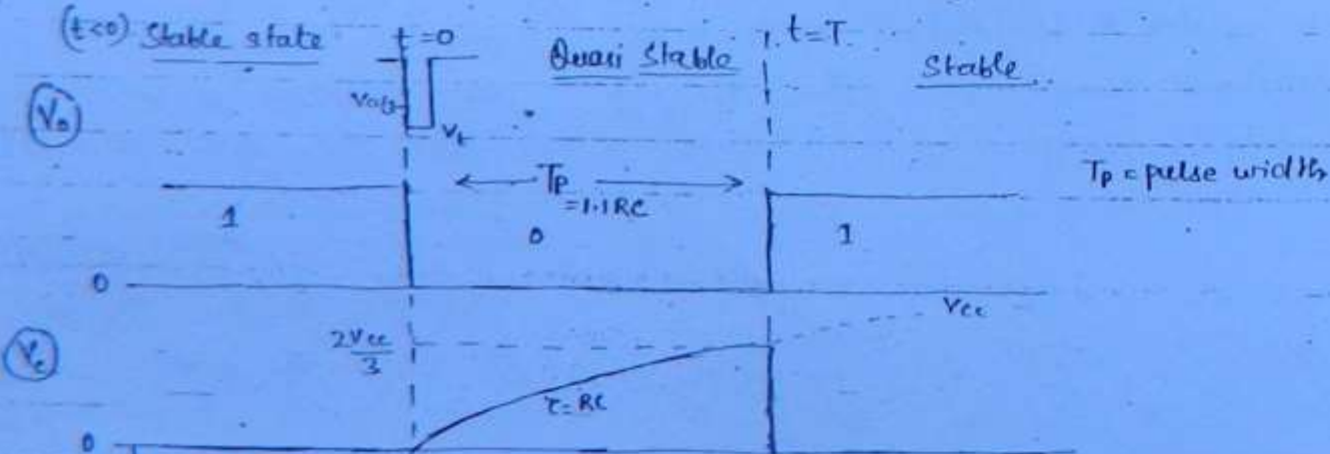
Note

- If each resistor R (R_1 & R_2) is replaced by a transistor which acts as a constant current source for charging C then excellent linearity b/w freq. & voltage may be attained.

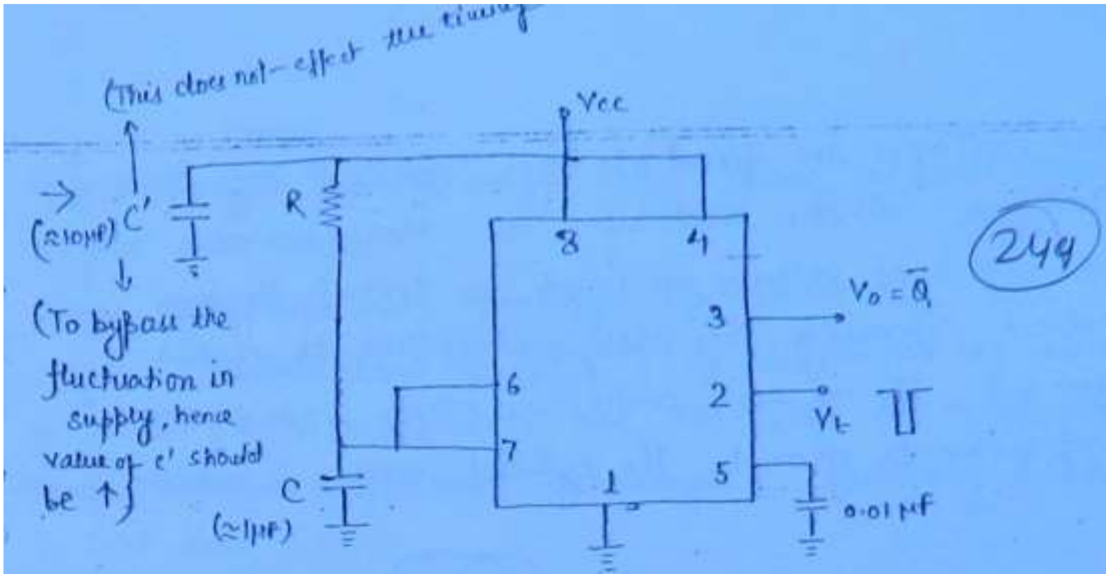
555 Timer







S	0	1	0	0	0
R	0	0	0	1	0
Q	0	1	1	0	0
$\bar{Q}$	1	0	0	1	1
Q_1	on	off	off	on	on



555 in Monostable Mode

Derivation of T_p —

→ V_c → change from 0 to $\frac{2V_{cc}}{3}$

→ $V_c = V_f - (V_f - V_i)e^{-t/\tau}$; $V_f = V_{cc}$, $V_i = 0$, $\tau = RC$

$\therefore V_c = V_{cc}(1 - e^{-t/RC})$

At $t = T_p$ — $\frac{2V_{cc}}{3} = V_{cc}(1 - e^{-T/RC})$

$\Rightarrow T_p = RC \ln 3$

$\Rightarrow \boxed{T_p = 1.1 RC}$ ** — Imp

→ The device 555 is a monolithic timing ckt that can produce accurate & highly stable time delays or oscillations.

Constructional Details :-

– The device consists of two comparators (C_1 & C_2) that drive set & reset terminals of a flip flop which inturn controls ON & OFF cycles of discharge tr Q_1.

→ comparator reference voltages are fixed at $\frac{2V_{cc}}{3}$ for C_1 & $\frac{V_{cc}}{3}$ for C_2. by means of a voltage divider made up of three series resistors R'. These reference voltages are reqd. to control timing.

→ Timing can be controlled externally by applying voltage to control voltage terminal (pin 5). If no such control is reqd., pin 5 can be bypassed by a capacitor to ground. The typical value is about 0.01μf.

250

Function:-

- When voltage is applied at trigger terminal grows -ve & passes through reference level $\frac{V_{cc}}{3}$, the o/p of C_2 changes its state. This change of state (S=1, R=0) will set the flip flop with $\bar{Q}=0$ & Tr. Q_1 = off.

- When voltage applied at threshold terminal (pin 6) grows +ve & passes through $\frac{2V_{cc}}{3}$, o/p of C_1 changes its state (S=0, R=1). This change of state will reset the flip flop with $\bar{Q}=1$ and Tr. Q_1 = ON.

Pin-4 (Reset Pin)

- A separate reset terminal is provided which is used to reset the FF externally. Normally when Pin 4 is not used, it should be connected to +ve supply +Vcc to avoid any false triggering. Transistor Q_2 acts as a buffer, isolating the ckt from false reset.

555 timer in Monostable state :-

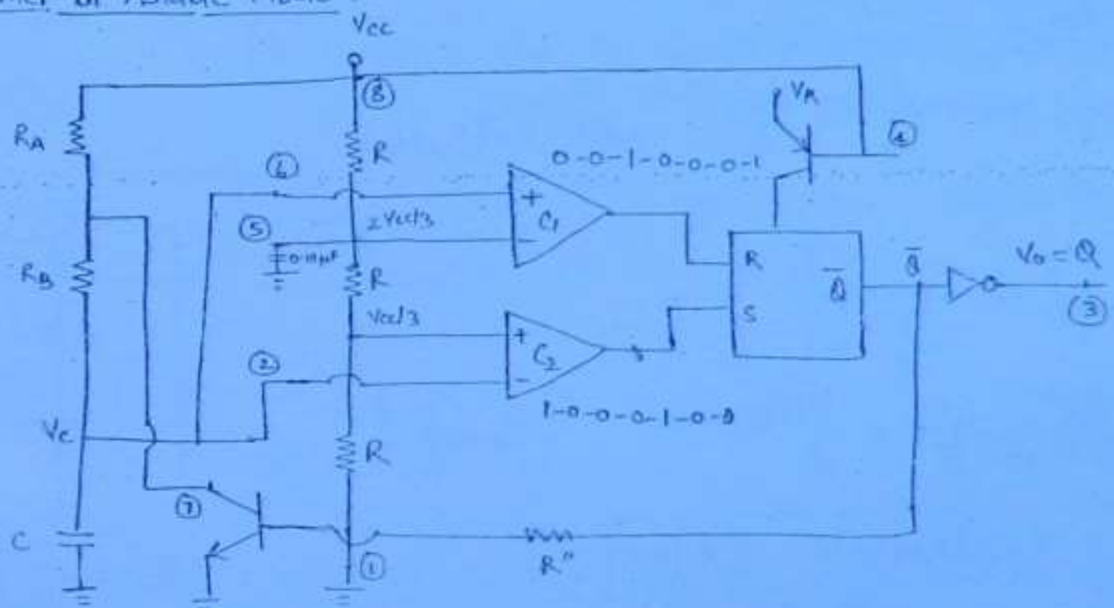
- for t<0, ckt is in stable state. V_t (trigger voltage) = V_{cc}, $V_o = \bar{Q} = 1$ & $V_c = 0$, and S=R=0.

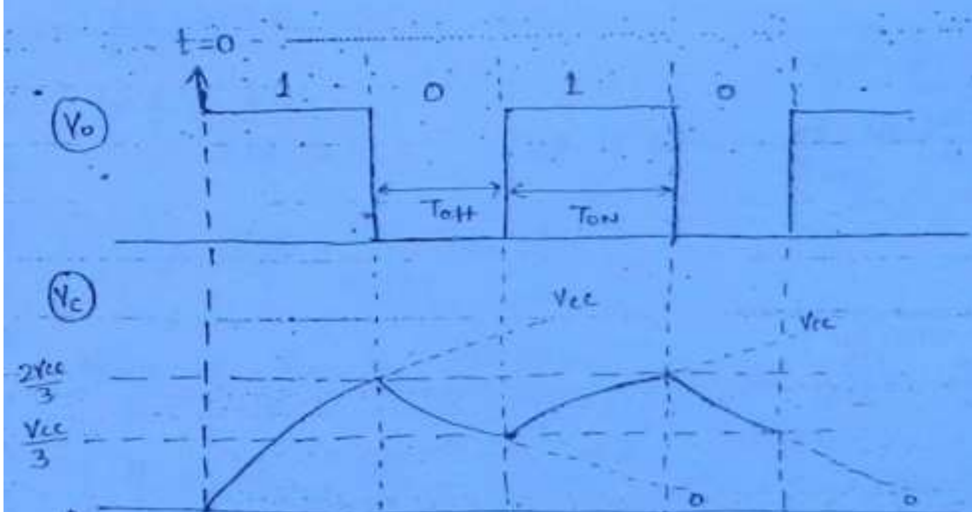
→ At t=0, on application of -ve trigger less than $\frac{V_{cc}}{3}$ causes o/p of C_2 to be high. This will set ff with $\bar{Q} = V_o = 0$ and Q_1 = off.

- Note that after termination of trigger pulse, FF will remain in $\bar{Q} = 0$ state (since $S=0, R=0$).

- Now, timing capacitor C charges up towards V_{CC} with $\tau = RC$. When V_c reaches threshold level of $\frac{2V_{cc}}{3}$, C_1 will switch its state. This change of state ($R=1, S=0$) resets the FF with $\bar{Q} = V_o = 1$ and Q_1 = on. Then the saturation resistance of Q_1 discharges C suddenly & ckt reach to its initial state.

555 timer in Astable Mode :-





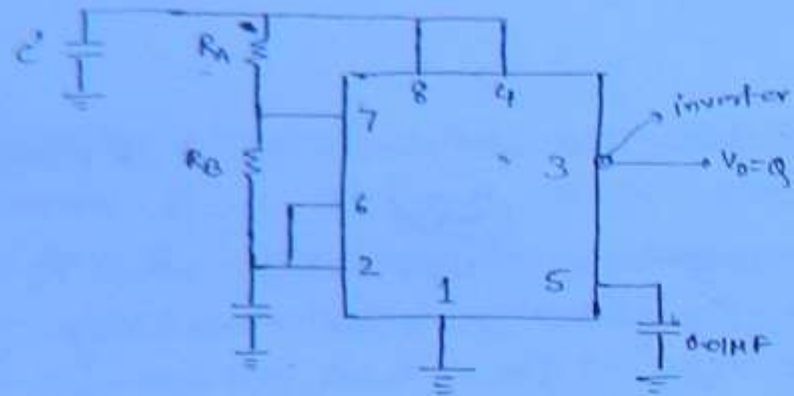
S 1-0 —— 0 — 0 - 1 - 0 — 0

R 0 - 0 —— 1 — 0 - 0 - 0 — 1

Q 1 —— 0 — 1 —— 0

$\bar{Q}$ 0 —— 1 — 0 —— 1

Q_1 off —— on — off —— on



(252)

Astable Mode

Derivation of Ton :-

Capacitor charge from $\frac{V_{cc}}{3}$ to $\frac{2V_{cc}}{3}$ with $\tau = (R_A + R_B)C$

$V_f = V_{cc}$, $V_i = \frac{V_{cc}}{3}$.

$$\therefore V_c = V_{cc} - \left[V_{cc} - \frac{V_{cc}}{3}\right] e^{-t/\tau}$$

At $t = t_{on}$
$\Rightarrow$

$$\frac{2V_{cc}}{3} = V_{cc} - \frac{2V_{cc}}{3} \cdot e^{-t_{on}/(R_A+R_B)C}$$

$$\Rightarrow \boxed{t_{on} = 0.69\,(R_A + R_B)C = \tau \ln 2}$$

Derivation of Toff :-

Capacitor discharges from $\frac{2V_{cc}}{3}$ to $\frac{V_{cc}}{3}$. with $\tau' = R_B C$.

$V_i = \frac{2V_{cc}}{3}$, $V_f = 0$.

At $t = T_{off}$ -

$$\frac{V_{cc}}{3} = 0 - \left(0 - \frac{2V_{cc}}{3}\right) e^{-T_{off}/\tau'}$$

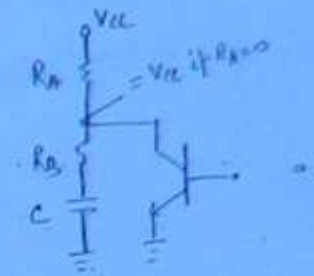
$$\Rightarrow \boxed{T_{off} = 0.69\,R_B C}$$

→ ∵ $\boxed{T_{on} > T_{off}}$ ⇒ $D > 50\%$. ⇒ Asymmetrical sq wave.

→ ∴ $T = T_{on} + T_{off} = 0.69\,(R_A + 2R_B)\,C$

$$\therefore \boxed{f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C}}$$

Duty Cycle $\boxed{D = \frac{R_A + R_B}{R_A + 2R_B} \times 100\%}$



When $V_0 = Q$, $D > 50\%$

When $V_0 = \overline{Q}$, $D < 50\%$

→ For $R_A = 0\,\Omega$, $\boxed{D = 50\%}$ – but R_A cannot be 0 since pin 7 will be directly connected with Vcc and Tr. will burn

→

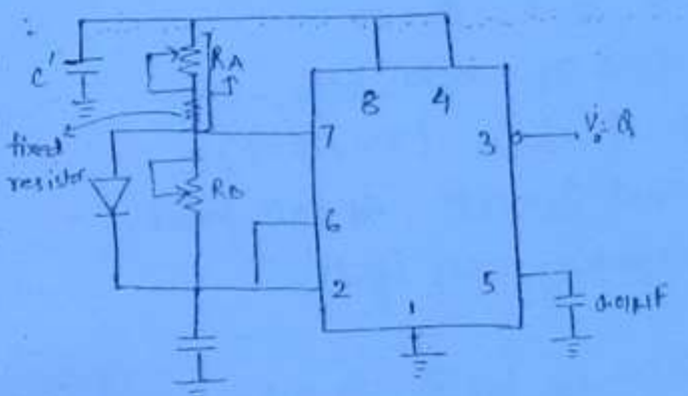
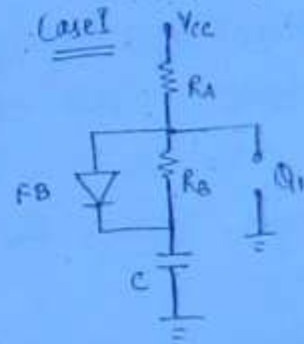


Fig 2

Case I



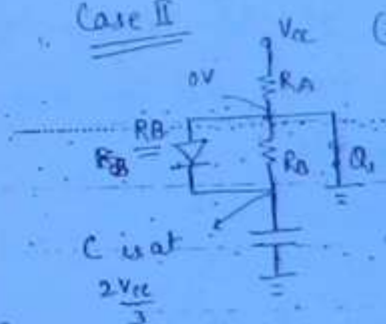
① Q_1 = OFF

C charge from $\frac{V_{cc}}{3}$ to $\frac{2V_{cc}}{3}$

$\tau = R_A C$

$T_{on} = 0.69 R_A C$

Case II



② Q_1 = ON

C discharge from $\frac{2V_{cc}}{3}$ to $\frac{V_{cc}}{3}$

$\tau = R_B C$

$T_{OFF} = 0.69 R_B C$

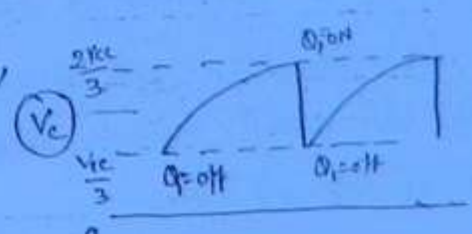
→ $T = 0.69 (R_A + R_B) C$

$$f = \frac{1}{T} = \frac{1.44}{(R_A + R_B)C}$$

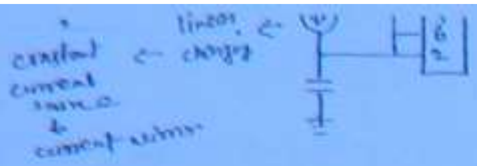
$$D = \frac{T_{on}}{T} \Rightarrow \boxed{D = \frac{R_A}{R_A + R_B} \times 100\%} \quad **$$

Now if $R_A = R_B$, $D = 50\%$

→ If $R_B = 0$,



⇒ This sawtooth pulse is achieved across capacitor and not on o/p.



⇒ o/p at V_C will be [illegible]

→ Potentiometer is provided in o/p as of duty cycle can be adjusted by changing R_A & R_B. (also all diodes & resistor are not ideal and R_A & R_B can be set accordingly to get symm. sq. o/p).

→ A fixed resistor is added to prevent pin 7 to directly connected to V_{CC} even if potentiometer at R_A is set at 0.

Important Points:-

For Fig ①

- In this mode, timing capacitor C charges up towards V_{CC} through $R_A + R_B$ upto $\frac{2V_{CC}}{3}$ then C_1 switches its state. This change of state ($S=0$, $R=1$) reset the FF with $V_0 = Q = 0$, $\bar{Q} = 1$, $Q_1 = $ on.
  Then capacitor C discharges through R_B & Q_1 upto $\frac{V_{CC}}{3}$, then C_2 switches its state. This change of state ($S=1$, $R=0$) set the FF with $V_0 = Q_0 = 1$, $\bar{Q} = 0$ and $Q_1 = $ off. At this point capacitor starts to charge again, thus completing the cycle.

- Duty cycle will always be < or > 50% for fig ①. To achieve 50% duty cycle we should make $R_A = 0$, however with $R_A = 0\Omega$ pin 7 is directly connected to $+V_{CC}$ and this may damage tr. Q_1 when Q_1 is ON.

→ In fig ② —

Capacitor charges through R_A and diode D upto $\frac{2V_{CC}}{3}$ and discharge through R_B and Q_1 upto $\frac{V_{CC}}{3}$. Then cycle repeats.

→ To obtain a square wave o/p R_A must be a combination of a fixed resistor & potentiometer so that potentiometer can be adjusted for exact sq. wave. Fixed resistor will avoid direct connection of pin 7 to V_{CC} when potentiometer is set at 0Ω.

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directly connecting reference voltage will change

V_c variation limits from $\frac{2V_{cc}}{3}$ or $\frac{V_{cc}}{3}$.

555

(using pin 5).

Application

1) It is used as Freq. modulator, i.e. voltage to freq. converter.
2) It is used as missing pulse detector.