PRODUCT DOCUMENTATION

ILXSPARTAN3E

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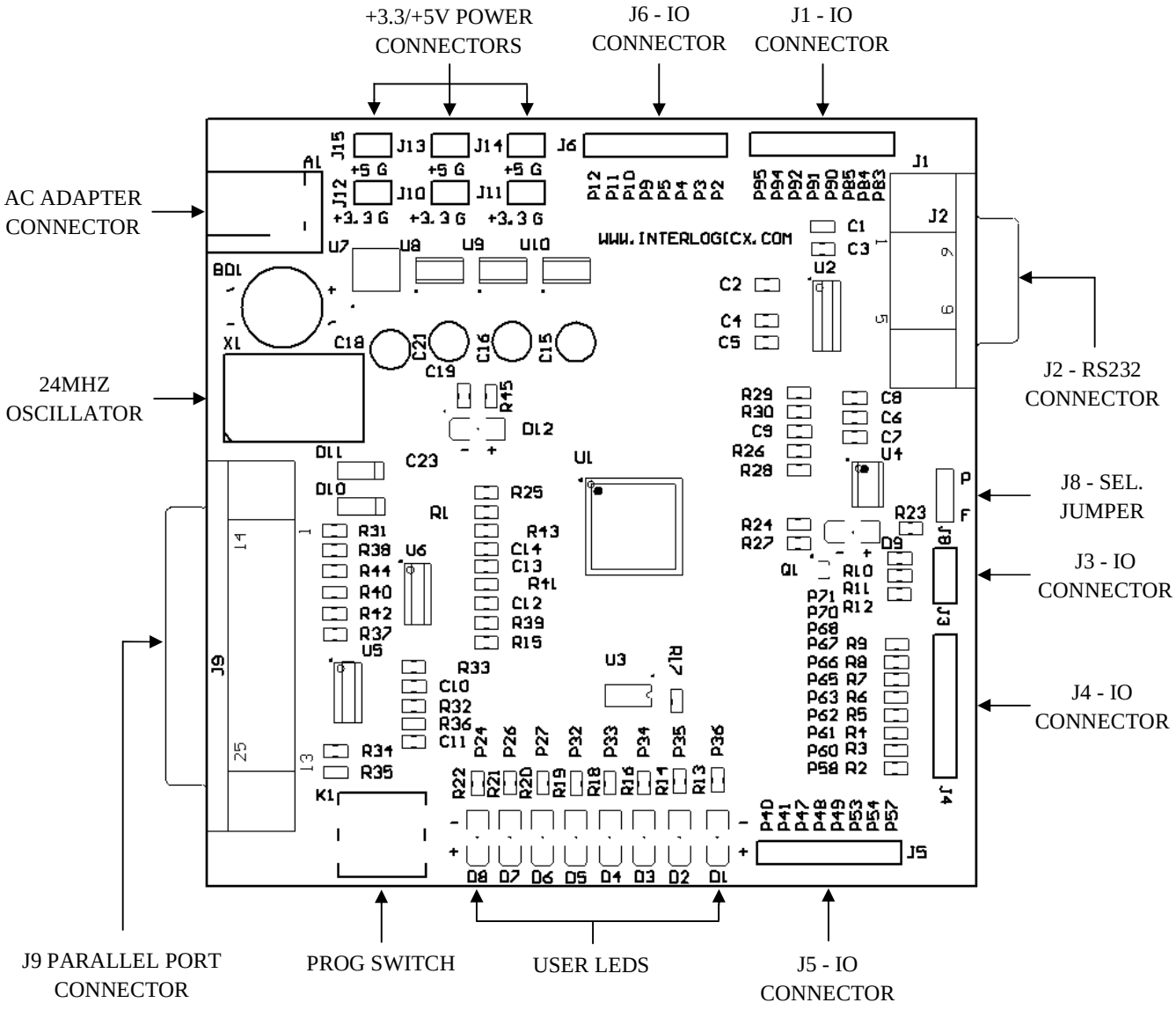

ILXSPARTAN3E BOARD LAYOUT

BOARD FEATURES

XC3S100E FPGA:

100K GATES WITH 2160 LOGIC ELEMENTS.

XCF01S PROM:

1MB CONFIGURATION PROM TO STORE FPGA CONFIGURATION DATA.

PROGRAMMING:

PARALLEL PORT JTAG PROGRAMMER TO LOAD CONFIGURATION DATA INTO THE FPGA OR PROM.

IO CONNECTORS:

35 USER I/Os' AND 8 DEDICATED USER LEDs.

POWER ADAPTER REQUIREMENTS:

→ **9V AC – 1Amp**

On-Board Power Supplies:

S.No	V	Designator	Purpose	Maximum Sourcing Capacity	Port connectors
1	+5V	U7	External Board Interface – Input to other regulators	500mA	3 Nos
2	+3.3V	U10	Power Supply to all onboard ICs	500mA	3 Nos
3	+2.5	U9	FPGA configuration rail power supply	500mA	NO
4	+1.2	U8	FPGA internal core logic power supply	500mA	NO

Note:

Although individual voltage regulators are capable of sourcing 500mA of power, the total collective power drawn from the board SHOULD NOT EXCEED 500mA.

On-Board IO Connectors:

1. 8Pin Berge IO Connector:

J1		
Connector Pin	**FPGA pin**	**FPGA BANK**
1	**P83**	**BANK0**
2	**P84**	**BANK0**
3	**P85**	**BANK0**
4	**P90**	**BANK0**
5	**P91**	**BANK0**
6	**P92**	**BANK0**
7	**P94**	**BANK0**
8	**P95**	**BANK0**

2. 3Pin Berge IO Connector:

J3		
Connector Pin	**FPGA pin**	**FPGA BANK**
1	**P71**	**BANK1**
2	**P70**	**BANK1**
3	**P68**	**BANK1**

3.8 Pin Berge IO Connector:

J4		
Connector Pin	**FPGA pin**	**FPGA BANK**
1	**P67**	**BANK1**
2	**P66**	**BANK1**
3	**P65**	**BANK1**
4	**P63**	**BANK1**
5	**P62**	**BANK1**
6	**P61**	**BANK1**
7	**P60**	**BANK1**
8	**P58**	**BANK1**

4.8 Pin Berge IO Connector:

J5		
Connector Pin	**FPGA pin**	**FPGA BANK**
1	**P57**	**BANK1**
2	**P54**	**BANK1**
3	**P53**	**BANK1**
4	**P49**	**BANK2**
5	**P48**	**BANK2**
6	**P47**	**BANK2**
7	**P41**	**BANK2**
8	**P40**	**BANK2**

5.8 Pin Berge IO Connector:

J6		
Connector Pin	**FPGA pin**	**FPGA BANK**
1	**P2**	**BANK3**
2	**P3**	**BANK3**
3	**P4**	**BANK3**
4	**P5**	**BANK3**
5	**P9**	**BANK3**
6	**P10**	**BANK3**
7	**P11**	**BANK3**
8	**P12**	**BANK3**

6. USER LEDs – 8Nos:

USER LEDs		
Designator	**FPGA pin**	**FPGA BANK**
D1	**P36**	**BANK2**
D2	**P35**	**BANK2**
D3	**P34**	**BANK2**
D4	**P33**	**BANK2**
D5	**P32**	**BANK2**
D6	**P27**	**BANK2**
D7	**P26**	**BANK2**
D8	**P24**	**BANK2**

7. RS232 – SERIAL COMMUNICATION:

J2		
Designator	**FPGA pin**	**FPGA BANK**
TX	**P78**	**BANK0**
RX	**P79**	**BANK0**

8. Crystal Oscillator:

X1		
Designator	**FPGA pin**	**FPGA BANK**
CLK	**P86**	**BANK0**

NOTE BEFORE PROGRAMMING THE FPGA:

BOARD POWER ON INDICATION:

LED D12 will glow when the board is turned on.

FPGA CONFIGURATION DONE:

LED D9 will glow when the FPGA is successfully configured.

FPGA/PROM SELECTION JUMPER (J8):

Placing the jumper cap on F and middle pin of jumper J8, shows only FPGA in configuration chain when initializing chain on ISE impact software.

Placing the jumper cap on P and middle pin of jumper J8, shows both FPGA & configuration PROM in configuration chain when initializing chain on ISE impact software.

Care should be taken to place the Jumper cap on anyone of the above mentioned configuration to successfully detect devices on board. Removing the jumper cap and initializing the chain will return with no device found.

PROG SWITCH:

Pressing this key once erases FPGA's configuration data and initializes the FPGA to receive new configuration data's.

To load configuration data from XCF01S PROM. After programming the PROM (XCF01S), PROG SWITCH must be pressed once to start loading the configuration data into the FPGA.

PARALLEL PORT CONNECTOR (J9);

Connect DB25 pin parallel port cable provided with the board on to connector J9 to and then start programming the FPGA.

On-Board ICs:

S.No	Designator	IC Name
1	U1	Xilinx Spartan 3E XC3S100E
2	U2	MAX3232
3	U3	74HC245
4	U4	XCF01S
5	U5,U6	74HC125
6	X1	24MHZ OSC

1. Xilinx Spartan 3E – XC3S100E FPGA:

This is our on-board FPGA it has 2160 logic elements. The board features four numbers of 8 pin ports (J4, J5, J6, and J7) and one 3 pin port (J3).

Port no J3 and J4 are dedicated ports for 16X2 LCD interface and can also be interfaced with TTL logic (+5V) devices; however these two ports can also be used to interface CMOS devices.

Remaining Ports should only be interfaced with CMOS devices.

2. MAX3232:

CMOS to RS232/RS232 to CMOS level converter. DB9 Female Connector (J2) provided for interfacing RS232 cables to communicate between PC and FPGA Board.

Only RX & TX pins of the MAX device are wired to the FPGA. Serial communication using hand shake (DTS, RTS) logic cannot be done with this interface.

3. 74HC245:

CMOS Buffer for driving user leds'.

4. XCF01S:

Configuration PROM used for storing FPGA configuration data. It can store up to 1MB of configuration data.

5. 74HC125:

CMOS latches used to configure FPGA through parallel port.

6. CRYSTAL OSCILLATOR:

24MHZ fixed crystal oscillator provides clock signals for user defined programming.