EELE 466

Lab 3 Report:

Implementing the Madgwick Orientation Filter in VHDL

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February 6, 2018

1.0 Summary

The purpose of this lab is to implement a Madgwick Orientation Filter in VHDL and explore the possible uses of it. In order to complete this, we segmented the code and made a test bench for each of the segments. For the normalize function, we used 14 bits of precision for all of the inputs. For the correction and update test benches, all of the inputs were normalized to be between 0 and 1. With these test benches complete, we finalized the resource utilization table using resource-sharing values of 1 and 4. The values were recorded in the table below.

2.0 Lab Design Components

Resource Utilization Table					
	Matlab Function	Madgwick qDot	Madgwick normalize	Madgwick correction	Madgwick update
Resource Sharing = 1	Multipliers	12	12	124	4
	Adders	9	2	133	8
	Registers	4	4	4	4
	RAMs	0	0	0	0
	Multiplexers	0	18	14	0
	Output Latency	1 cycle	1 cycle	1 cycle	1 cycle
Resource Sharing = 4	Multipliers	4	7	45	4
	Adders	14	6	167	8
	Registers	36	40	605	4
	RAMs	0	0	0	0
	Multiplexers	20	32	208	0
	Output Latency	2 cycles	3 cycles	9 cycles	1 cycles

Table 1: Resource Utilization Table

2.0 Conclusion

We found that the output latency was affected by the resource sharing value. With a resource sharing of value of 1, the output latency was one cycle for each function. When the resource sharing value was increased to 4, the output latency increased and the multipliers decreased. This trade off shows the utility of the resource sharing parameter. With these test benches, we can compute quaternion math.